LOW-NOISE CMOS IMAGE SENSORS FOR RADIO-MOLECULAR IMAGING

LOW-NOISE CMOS IMAGE SENSORS FOR RADIO-MOLECULAR IMAGING

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Yue CHEN

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Prof.dr.ir. A.J.P. Theuwissen

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Rector Magnificus,	voorzitter
Prof.dr.ir. A.J.P. Theuwissen,	Technische Universiteit Delft, promotor
Prof.dr. F.J. Beekman,	Technische Universiteit Delft
Prof.dr. P.J. French,	Technische Universiteit Delft
Prof.dr. E. Charbon,	Technische Universiteit Delft
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Dr.ir. I.M. Peters,	Teledyne DALSA Professional Imaging, Eindhoven
Prof.dr.ir. G.C.M. Meijer,	Technische Universiteit Delft, reservelid

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PRINTED IN THE NETHERLANDS

獻給我的父親母親

To my parents

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1

Introduction

The field of nuclear medicine, one of the most sensitive methods for obtaining information on biological function for the purpose of medical diagnoses, precedes the development of image-forming radiation detectors by several decades [1.1]. The development of radiation detectors capable of delivering spatial information about gamma-ray interactions was one of the key enabling technologies for nuclear medicine imaging [1.2] and, eventually, single-photon emission computed tomography (SPECT). SPECT is a nuclear medicine tomographic imaging technique that uses gamma rays. It is very similar to conventional nuclear medicine planar imaging, which uses a gamma camera. However, SPECT is able to provide true three-dimensional information. This information is typically presented as cross-sectional slices through the object, but can be freely reformatted or manipulated as required. The key to the SPECT imaging technique is the gamma-ray detector. Here, often-used detectors are the scintillation gamma cameras, which consist of scintillation crystals coupled to the image sensors. Incident gamma photons are captured in the scintillation crystal, which converts their energy into visible light photons. The image sensors convert light photons into electrical signals. The quality of the captured image is then highly dependent on the performance of the image sensor. The objective of this thesis is to develop and

demonstrate low-noise image sensors for SPECT imaging by improving the noise generated in imagers.

In this chapter, the background of medical imaging is briefly presented in Section 1.1. The fundamental knowledge of single-photon emission computed tomography (SPECT) is introduced in Section 1.2. The high-resolution gamma-ray detectors for SPECT imaging are discussed in Section 1.3. The solid-state imagers used in SPECT system are introduced and analyzed in Section 1.4. The motivation and challenges in developing low-noise CMOS imagers for SPECT imaging are presented in Section 1.5. A brief organization of the thesis is presented in Section 1.6.

1.1 Medical Imaging Techniques

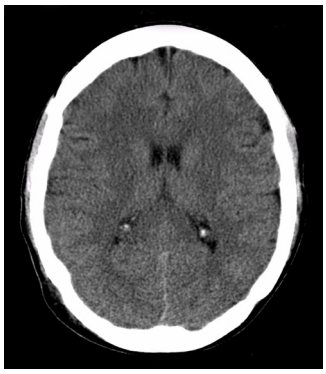
The role of accurate investigation and diagnosis in the management of all diseases is unquestionable. Central to the diagnostic process is the medical imaging techniques [1.3]. Medical imaging not only provides for diagnosis but also serves to assist with planning and monitoring the treatment of malignant disease [1.3]. Medical imaging techniques can be generally divided into two categories: anatomical and molecular imaging.

Anatomical imaging, also known as structural imaging, deals with the location, outline, and structure of biological organs or tissues and the diagnosis of gross (large scale) diseases, such as tumors, hyperplasia and injuries. Anatomical imaging includes methods such as computed tomography (CT), magnetic resonance imaging (MRI), ultrasonography, etc.

Molecular imaging, also referred to as functional imaging, is used to diagnose metabolic diseases and lesions on the cellular level (finer scale). It is also used for building brain-computer interfaces [1.4]. Molecular imaging includes methods such as positron emission tomography (PET) and single-photon emission computed tomography (SPECT). Figure 1-1 shows examples of anatomical and molecular images of the human brain [1.5-1.8].

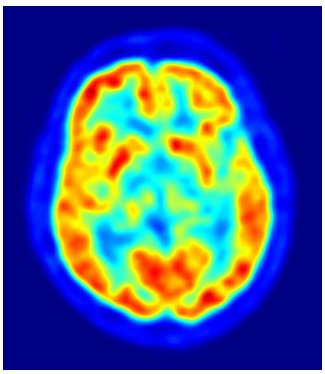
Single-photon emission computed tomography (SPECT) is a quintessential molecular imaging modality. SPECT can measure the distributions of a wide variety of *tracers* (i.e. radioactively labeled molecules) *in vivo*. This enables the visualization of functional properties such as receptor density, state of cells (for example apoptotic and necrotic), perfusion, oxygenation, glucose uptake, etc [1.9-1.13].

Compared to MRI using targeted activatable contrast agents and PET, SPECT is among the most sensitive of the molecular *in vivo* imaging technologies, with its spatial scale covering the resolution required for imaging small laboratory animals and humans [1.14].

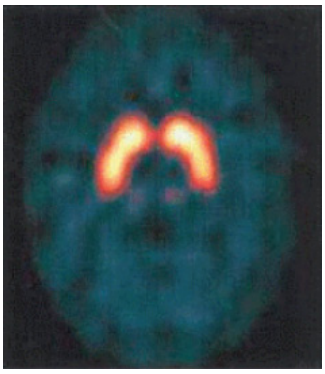


a) X-Ray CT Scan [1.5]

b) MRI Scan [1.6]



c) PET [1.7]



d) SPECT [1.8]

Figure 1-1: *a) and b) Anatomical imaging outlining the human brain; c) and d) Molecular imaging showing the function of glucose uptake (PET) and dopamine transporters (SPECT) of the human brain*

1.2 SPECT System Fundamentals

The SPECT system uses gamma-ray detectors surrounding the patient or laboratory animal to detect single gamma photons emitted from the radiotracers. An essential part of any SPECT system is the collimator. The collimator is placed between the object and the gamma-ray detector. It ensures that only gamma photons from a particular direction are detected because no suitable lenses exist for gamma photons. This creates a necessary correspondence between the pixels of the image and the volume elements (voxels) of the object. Collimation results in a very large fraction of the gamma photons (generally exceeding 99%) to be absorbed [1.15].

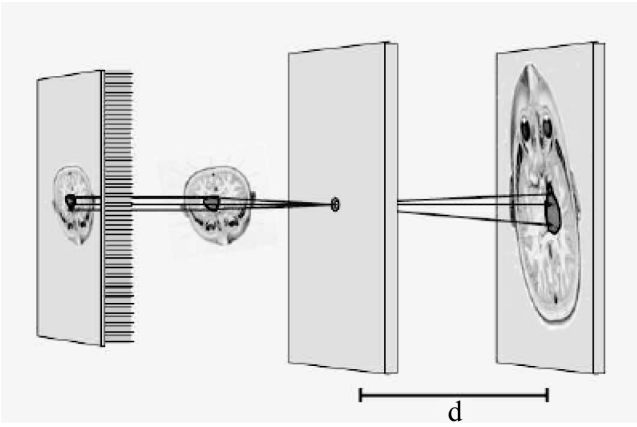


Figure 1-2: *left) Parallel-hole collimation; right) pinhole collimation (d is the distance between the collimator and detector) [1.15]*

Figure 1-2 shows the two most commonly used types of collimators: the parallel-hole collimator and the pinhole collimator. In parallel-hole collimation, as shown in Figure 1-2(left), a "plate" of parallel holes, separated by a septa of dense, gamma-ray absorbing material (most often lead), creates a pixilated image of the object on the camera. In parallel-hole collimation, only those gamma photons incident at an angle approximately normal to the detector are detected. Parallel-hole collimators are the most commonly used collimators in clinical imaging. Often-used variations on this method apply magnifying geometries (fan- and cone-beam collimators), which can improve system performance.

In pinhole collimation, as shown in Figure 1-2(right), in analogy to optical pinhole imaging, a small opening in an otherwise opaque material is used to project an inverse image of the object onto the detector. Here, the image can be magnified or demagnified by varying the distance between the collimator and detector (*d* in Figure 1-2). In an imaging system, magnification can improve the spatial resolution by reducing the adverse effect of intrinsic detector resolution, while demagnification allows the use of more pinholes (around the object) and thus improves the overall system sensitivity. Although one can increase sensitivity by allowing the projections through the pinholes to overlap, the improved sensitivity is outweighed by resolution loss and image artifacts due to loss of information on the exact origin of the detected gamma photons [1.16][1.17].

Using a gamma-ray detector that provides spatial information on individual gamma photon interactions with the collimator allows for the creation of two-dimensional (2D) projection images of the radiotracer distribution. SPECT imaging involves the reconstruction of three-dimensional (3D) radiotracer distributions from such 2D projection images acquired at multiple angles. The preferred tomographic reconstruction methods are iterative algorithms that apply known or estimated 2D detector responses to calculate the projections of an *estimation* of the 3D tracer distribution [1.18]. By comparing the calculated projections to the measured projections, the 3D distribution estimation can iteratively be improved. Because iterative algorithms model the response of the detectors (including collimators), they allow for partial correction of resolution loss.

Small-Animal SPECT

Small-animal SPECT is a key tool used to the study models of human diseases on the molecular scale. A better understanding of the diseases will lead to the development of new medicines and tracers to track these diseases. For small-animal SPECT, pinhole imaging has the most appeal because of the relatively small fields-of-view which allows large numbers of pinholes to be placed close to the object. Pinhole imaging in small animals can lead to ultra-high resolutions, as has been demonstrated with the U-SPECT-I [1.19] and U-SPECT-II [1.20] systems. These U-SPECT systems, which were developed at the University Medical Center in Utrecht, the Netherlands, are capable of sub-half-mm resolution imaging despite the use of large clinical detectors that have a relatively low

intrinsic spatial resolution of approximately 3.5mm. Figure 1-3(a) illustrates the U-SPECT-II system, which is a small-animal SPECT system based on pinhole collimation. The highly magnifying pinhole collimation scheme shown as Figure 1-3(b), creates a large number of non-overlapping images on the detector, which is shown as Figure 1-3(c). However, a large magnification of the object [see Figure 1-3(b)], is necessary to overcome the adverse effect of detector blurring. This puts a limit on the number of pinholes that can be used before projections start to overlap and thus limits sensitivity [1.15].

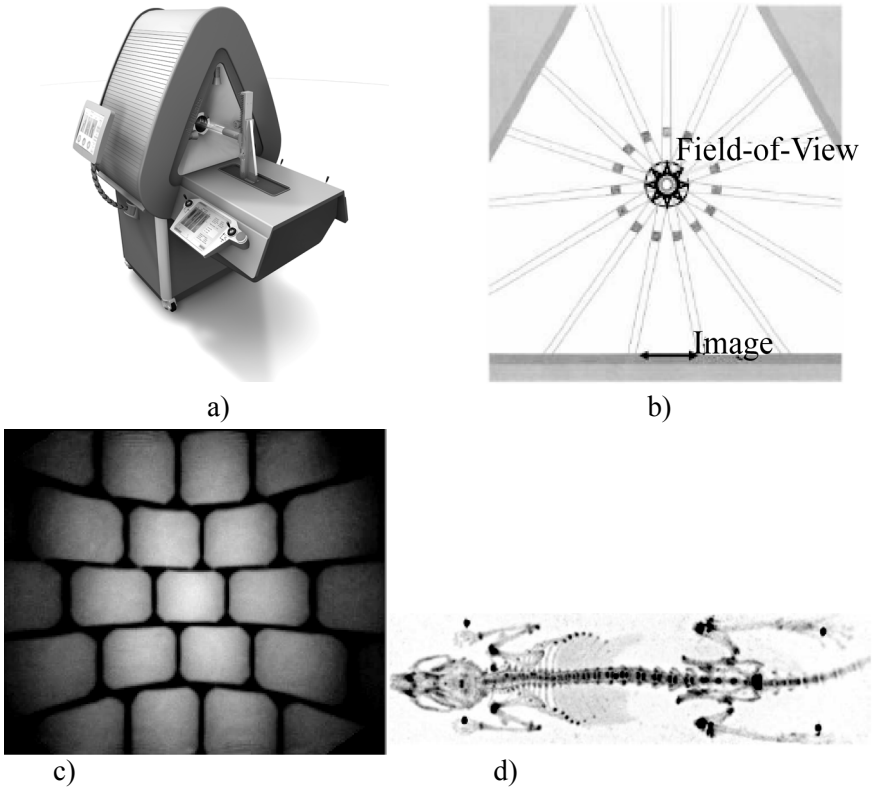


Figure 1-3: *a) U-SPECT-II system [1.20]; b) the highly magnifying pinhole collimation scheme [1.15]; c) a large number of non-overlapping images on the detector [1.15]; d) U-SPECT image showing bone turnover in a living mouse [1.15] (Dynamic U-SPECT images can be viewed at www.milabs.com/galler)*

Therefore, as has been shown in the studies by [1.21-1.25], a high intrinsic detector resolution combined with energy discrimination capabilities is essential for the improvement of future (pinhole) SPECT systems. High intrinsic spatial resolution will allow close placement of the detectors to the collimator, which facilitates a higher number of pinholes and thus improves the system's sensitivity-resolution trade-off. Knowledge of the individual energy values allows the simultaneous imaging of different isotopes and exclusion of, or correction for, the scattered gamma photons in the reconstruction process which are detected but degrade the resolution [1.15].

1.3 High-Resolution Gamma-Ray Detectors

Compact high-resolution gamma-ray detectors are extremely useful for radiation monitoring, autoradiography and the high-resolution planar imaging of radiotracers. As mentioned in Section 1.2, a high intrinsic detector resolution combined with energy discrimination capabilities is essential for the improvement of future SPECT systems [1.21-1.25]. A large number of laboratories are currently developing high-resolution gamma-ray detectors for applications ranging from astronomy and particle physics to biomedical imaging [1.26-1.37].

There are many different approaches to making a gamma-ray detector for SPECT imaging [1.2]. Regardless of the approach, the objective is to convert the gamma-ray photon's energy into an electrical signal. The limiting factor in the performance of a well-designed system is the number of information carriers at the point of conversion to an electrical signal. These information carriers are in the form of scintillation photons, electron-hole pairs, or electron-ion pairs, depending on the detector technology.

Two classes of position-sensitive gamma-ray detectors are currently of great interest for SPECT. The first class of detectors uses the scintillating material to convert gamma rays into visible light photons, which are subsequently detected by position-sensitive light photon detectors, such as (arrays of) Photo-Multiplier Tubes (PMTs) [1.19][1.20], Silicon PMTs [1.38], Avalanche Photo Diodes (APDs) [1.37] or CCDs [1.35][1.36]. Another important class of detectors relies on the direct conversion of the gamma radiation into electrical signals using solid-state semiconductor materials [1.2], for instance Si, Ge, CdTe or CdZnTe (CZT) detectors. For medical imaging, scintillation crystals coupled to

PMTs are currently the most commonly used gamma detectors [1.2]. However, the selection of either scintillator-based or solid-state detectors must be based on a number of considerations, depending on the eventual application of the gamma-ray detector and the costs.

One of the novel ways to obtain a very high spatial resolution (<100μm) with a gamma-ray detector is to use a scintillation layer composed of a bundle of parallel micro-columnar crystals, which is read out by a CCD suitable for operating at high frame rates. Figure 1-4 shows a simulated high-resolution gamma-ray detector based on a CCD [1.32][1.39]. The use of columnar scintillation layers prevents resolution loss arising from light spreading. The scintillation crystal captures the gamma photon and converts its energy into visible light photons. Between the scintillator and the CCD, a fiber-optic taper can be placed in order to increase the effective size of the detector surface. The interaction of the gamma photons with the scintillator results in the generation of between several hundreds and a few thousand (visible) light photons [1.15], which are detected by the CCD as very low-light conditions. Gamma photon-counting algorithms have been developed to analyze the CCD frames for the presence of scintillation light spots and to provide an estimate of the center-of-gravity and the relative energy content of the individual interactions [1.35][1.39]. The quality of the images captured out of the gamma-ray detector is hereby largely dependent on the performance of the CCD used in the detector.

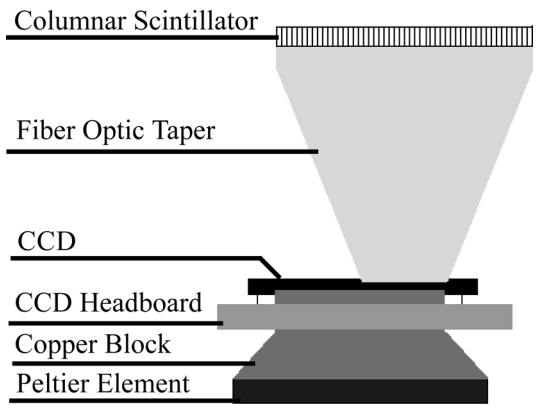


Figure 1-4: *Simulated schematic of a high-resolution gamma-ray detector based on a CCD (modified from [1.39])*

Because of the high-resolution requirement, a SPECT imaging system requires a gamma-ray detector with high detective quantum efficiency (DQE). DQE is defined as the square of the signal-to-noise ratio (SNR) at the detector output over the SNR at the detector input. The SNR of an image sensor used in the detector is defined as the ratio between the signal and the noise at a given input light level. Therefore, the SNR at a SPECT detector output largely depends on the SNR of the image sensor used in the system, for instance the CCD.

Consequently, the SNR of the image sensor in low-light conditions (only several hundreds to a few thousand light photons) is the key to the gamma-ray detector used in SPECT imaging. In general, to obtain a high SNR, a large light detection area and low-noise readout are necessary for the image sensor. More explanation about the SNR of an image sensor is provided in Chapter 2.

1.4 Solid-State Imagers for SPECT: EMCCD vs. CMOS Image Sensor

CCDs have been used in scientific imaging for decades [1.40][1.41]. For scintillator-based SPECT imaging, there are two main types of CCD-related noise that complicate the detection of scintillation events [1.39]: dark current and readout noise. Dark current can be adequately suppressed by cooling the CCD, but the additional cooling devices increase the total system cost. In most CCDs, the readout noise becomes a serious problem at high frame rates. This degrades the SNR of the CCDs and thus the performance of the gamma-ray detector for SPECT imaging. To overcome this hindrance, electron-multiplying CCDs (EMCCDs) are used [1.15][1.32][1.35][1.39], which allows the construction of a compact photon-counting CCD-based gamma camera that in some cases resulted in spatial resolutions of about 60μm [1.32].

An EMCCD [1.40] is a CCD with an additional feature: internal gain. This internal gain is provided by the electron multiplication, which is also referred to as avalanche multiplication or impact ionization, in the gain register. This gain register is split up into a large number of electron-multiplying (EM) stages. In each EM stage the electrons are multiplied by impact ionization in a similar way to an avalanche diode. Impact ionization is the process in which an electron with enough kinetic energy can knock a bound electron out of its bound state (in the valence band) and promote it to a state in the conduction band, creating an

electron-hole pair. The overall gain from the gain register can be very high, thus with a single input electron many thousands of output electrons can be generated. This eventually provides higher light sensitivity for the CCD. In very low-light conditions, EMCCDs show very good performance with respect to SNR [1.40]. Unfortunately the EMCCDs also have specific limitations such as:

- EMCCDs always need to be deeply cooled, as the dark current of the sensor is also amplified along with the signal in the EM stages;
- The gain of the EMCCDs largely depends on the temperature, for a temperature change of 60°C, the gain changes by a factor of 10 (the higher the gain, the higher its dependency on temperature) [1.42];
- The gain of EMCCDs is also very sensitive to the voltage amplitude of the clock pulses. A small variation in clock pulse amplitude results in a large variation in gain [1.42];
- The price of these devices is usually very high;
- The EM amplification shows aging effects: at constant voltage and constant temperature, the overall gain of the sensor will drop over time, depending on the total amount of charge that has been transported through the gain channel [1.42][1.43]. Although the aging effects can be minimized if the sensor is used with due care and attention, for example, cannot over-saturate the detector while using the EM amplification, it constrains the usage conditions for the sensor [1.43].

CMOS image sensors over the years have evolved in performance and are now comparable to CCDs [1.44-1.46]. CMOS image sensors over EMCCDs for SPECT imaging can have several advantages such as:

- They can be lower in cost;
- More circuitry and functionalities such as amplifiers or analog-to-digital convertors (ADCs) can be integrated on-chip and even within the pixel (pixel size for SPECT imaging is usually large);
- The video-signals can be read in parallel, decreasing the analog bandwidth and lowering the readout noise.

However, CMOS image sensors suffer from a poor SNR compared to EMCCDs, resulting in poor image quality in low-light conditions. This is a main drawback in using CMOS image sensors for the application requiring a high SNR in low-light conditions, such as SPECT imaging.

1.5 Challenges and Motivation

With high-resolution commercial SPECT imaging systems, such as the U-SPECT systems [1.19][1.20], images can be acquired with sub-half-mm resolution. This allows the imaging of organ and tissue functions. A high intrinsic detector resolution combined with energy discrimination capabilities will significantly benefit future versions of (pinhole) SPECT systems [1.21-1.25]. The EMCCD-based gamma-ray detectors for SPECT imaging [1.15][1.35] suffer from specific limitations, as mentioned in Section 1.4. Therefore, it is necessary to develop new gamma-ray detectors that overcome the limitations of EMCCDs for SPECT systems with better performance.

CMOS image sensors are a potential candidate to meet the requirements for SPECT imaging. However, the low SNR of CMOS image sensors is the main barrier. The desired noise level for the CMOS image sensors to be used in SPECT systems is $0.3e^-$/pixel/frame at room temperature [1.47]. Therefore the main challenge is to develop a new CMOS image sensor with a better SNR and the noise level required for SPECT imaging. The motivation for this thesis is to design a CMOS image sensor with a high SNR in low-light conditions. To obtain the high SNR, new techniques need to be developed to reduce the sensor noise floor to as low as $0.3e^-$/pixel/frame at room temperature.

1.6 Thesis Organization

This thesis consists of six chapters. Chapter 2 gives a brief overview of (introduction to) CMOS image sensors. The concept of light detection in silicon technology is presented. Further on, the various performance parameters used in characterizing an CMOS image sensors are discussed

In Chapter 3, a brief introduction to the pixel temporal noise in modern deep sub-micron CMOS technology is presented. Then, the technical approach adopted to reduce the noise level is explained. A buried-channel source follower is illustrated and evaluated as the in-pixel

amplifier replacement for the standard surface-mode source follower. Device simulations and test transistor characterizations are discussed as well. An overview of the test sensor made in 0.18μm CMOS technology is given together with some measurement results.

Chapter 4 focuses on the important technological considerations of designing low-noise CMOS imagers using the Correlated Multiple Sampling (CMS) technique. The principle of CMS and its impact on SNR are discussed. The main approaches and designs to implementing CMS are illustrated and analyzed. A theoretical model and a numerical simulation of the noise reduction effects are presented as well.

In Chapter 5, the design of a low-noise CMOS imager using column-parallel digital CMS is shown and discussed. A new topology of the low-noise column-parallel circuits is introduced and their operation principles are described. A detailed noise analysis based on the proposed column-parallel circuits is presented and discussed.

In Chapter 6, the realization of a low-noise CMOS imager using the approaches in Chapter 3 and Chapter 5 is presented. An overview of the sensor design is given followed by the measurement results.

Finally, Chapter 7 presents the main conclusions of this thesis and gives suggestions for future work.

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2

An Overview of CMOS Image Sensors

This chapter gives an overview of background knowledge on the CMOS image sensors. The purpose is to briefly introduce several important performance parameters which are usually used as trade-offs for CMOS image sensor design considerations, especially with regard to noise. As the intention of this thesis is to investigate approaches to reduce the noise floor of CMOS imagers, it is essential to clarify the physical origin and evaluation method of different noise sources in CMOS imagers.

This chapter starts with the definition of some critical parameters to characterize the performance of a CMOS image sensor, in Section 2.1. Next, an overview of the physical origin and characterization approach of the spatial noise in CMOS imagers is given in Section 2.2. Finally, in Section 2.3, the temporal noise in CMOS imagers is introduced and discussed.

2.1 Performance Standards

For every electronic system, there are a number of parameters that define its performance. In the following sections, some of the important performance parameters of CMOS image sensors, such as signal-to-noise

ratio, quantum efficiency, dynamic range and pixel conversion gain, are explained and discussed.

2.1.1 Signal-to-Noise Ratio

The signal-to-noise ratio (SNR) is a key parameter that describes the overall performance of an imager. The SNR for a CMOS imager is defined as the ratio between the signal and the noise at a given input light level. It can be expressed as follows:

$$SNR = 20\log\left(\frac{QE \cdot P}{\sqrt{n_{SN}^2 + n_{DN}^2 + n_{RN}^2 + n_{FPN}^2}}\right)[dB] \qquad (2\text{-}1)$$

where QE is the quantum efficiency of the pixels, which will be explained more in Section 2.1.2, P is the number of input photons on the pixel area, n_{SN} is the photon shot noise, n_{DN} is the dark current shot noise, n_{RN} is the read noise, and n_{FPN} is the fixed-pattern noise (FPN). The first three noise terms are the temporal (random) noise sources, whereas the last one represents the spatial noise source of the CMOS imagers. A detailed introduction and discussions about these noise sources are presented in Section 2.2 and Section 2.3. Every imager and imaging system strives to achieve the highest possible SNR. In general, the image is of good quality if SNR>20dB [2.1].

Figure 2-1 shows a simulated SNR plot as a function of the input photons based on Eq. (2-1). For the simulation, 50% QE, $1e^-$ dark current shot noise, $5e^-$ read (readout) noise, and 1% FPN were assumed. Under low-light conditions, which are the research interest for this thesis, the dark current shot noise and read (readout) noise are the dominant noise sources. In an ideal case, the SNR of a CMOS imager is mainly limited by the read noise. As the number of input photons increases, the photon shot noise becomes the dominant noise source and the SNR increases by the square root of the signal, because the photon shot noise is equal to the square root of the number of input photons. For higher signals, the SNR is dominated by FPN noise and becomes constant.

In conclusion, a high SNR is a fundamental criterion for image quality in terms of noise. For different illumination levels, the tendency of the SNR shows its dependency on different noise sources. As mentioned in Chapter 1, the research focus of this thesis is to improve the SNR of a CMOS imager under low-light conditions by reducing the sensor noise

floor to as low as 0.3e$^-$/pixel/frame at room temperature; therefore, it is important to investigate and summarize the noise sources in CMOS imagers, which are presented as Section 2.2 and Section 2.3 in this chapter.

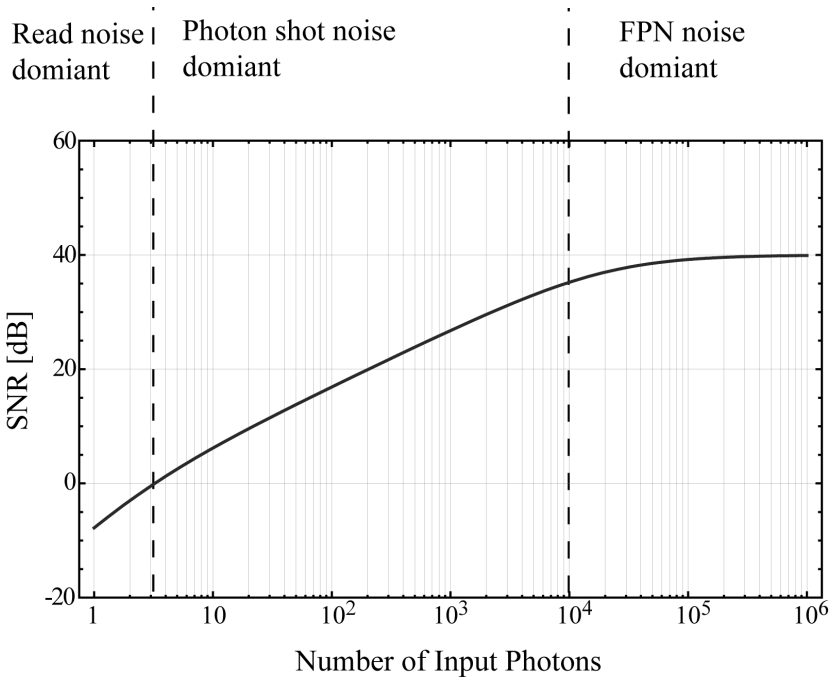

Figure 2-1: *Illustration of SNR as a function of input photons*

2.1.2 Quantum Efficiency and Spectral Responsivity

The photon-sensitivity of an imager can be characterized in two ways: with quantum efficiency or spectral responsivity. Quantum efficiency (QE) represents the imager's ability to intercept incidence photons, and to generate and collect signal charges through the photoelectric effect. It is defined as the percentage of incident photons hitting the photodetector surface that produce electron-hole pairs. It is given as:

$$QE(\lambda) = \frac{N_{sig}(\lambda)}{P(\lambda)} \tag{2-2}$$

where N_{sig} is the number of collected signal charges, P is the number of incident photons, and λ is the photon wavelength. An ideal imager would have 100% QE at all wavelengths.

Normally spectral responsivity is also used to characterize the photon-sensitivity of an imager. It is defined as the ratio of the photocurrent to the optical incident power. It is given as:

$$R(\lambda) = \frac{I_{ph}}{P_{ph}} = \frac{qN_{sig}(\lambda)}{E_{ph}P(\lambda)} = \frac{q\lambda}{hc}QE(\lambda) \tag{2-3}$$

where I_{ph} is the photocurrent, P_{ph} is the optical incident power, q is an electron charge, E_{ph} is the photon energy, h is the Planck's constant, and c is the speed of light. From Eq. (2-3) it can be seen that the spectral responsivity of an imager on a specific photon wavelength also relies on its QE.

To achieve a high photon response, three QE-loss mechanisms have to be minimized: absorption, reflection, and transmission. Absorption loss is associated with optically dead structures, which are typically located above, but also within, the pixels. Reflection and transmission losses are inherent to the physical properties of silicon. At certain wavelengths, the reflection loss is significant. For instance, at 250nm, the reflection loss reaches a maximum of 70% for a raw silicon surface [2.1]. Transmission loss occurs when incoming photons pass through the imager's photosensitive volume, which is a region of the photodiode that is typically 10µm thick, without generating a signal charge [2.1]. This problem is pronounced at very long (>1100nm) and very short (<0.2nm) wavelengths, i.e., the near-IR and soft x-ray sections of the spectrum [2.1].

There are several approaches to improve the QE performance of CMOS imagers. First of all, for front-side illuminated imagers, the ratio of the photodiode to the total pixel area, i.e. the fill factor, should be as high as possible to minimize the absorption loss. The CMOS imagers can also be thinned and illuminated from the backside, delivering spectral coverage from the soft x-ray to the near-infrared (0.1-1000nm) [2.1], which is a dedicated technology referred to as backside illumination (BSI). BSI can eliminate the absorption loss by offering a pixel with a 100% fill factor. If BSI is not available, a microlens can significantly increase the pixel's fill factor and QE as well. A microlens can increase the light-collecting ability by focusing the incoming light onto the photo-active part of the pixel. The biggest advantage of using microlenses on top of the pixels is: the smaller

the fill factor, the more QE is improved. In addition, applying anti-reflection coating (ARC) layers on top of the sensor can minimize reflection loss. In principle, the incident photons with a longer wavelength can penetrate deeper into the silicon before being absorbed. This physical property of the photons can cause signal charges to be generated outside the depletion region of the photosensitive volume, and may be recombined before being collected. This phenomenon often introduces a significant QE reduction, particularly for photons with a long wavelength. Therefore, in order to minimize the transmission loss caused by this phenomenon, it is essential to maintain a wide and deep depletion region of photosensitive volume.

2.1.3 Dynamic Range and Pixel Conversion Gain

Dynamic range (DR) is the ratio of the maximum signal over the minimum signal that a system can detect. For a CMOS imager, the dynamic range is defined as the ratio of the signal saturation level over its noise floor in the dark. It quantifies the ability of an imager to adequately image both bright lights and dark shadows in the same scene. In general, it can be given as:

$$DR = 20\log\left(\frac{S_{sat}}{n_{DK}}\right)\ [dB] \tag{2-4}$$

where S_{sat} is the signal level at saturation, and n_{DK} is the noise floor in the dark, which includes the pixel dark current shot noise and read noise. As can be seen from Eq. (2-4), there are two ways to increase the DR: by increasing the maximum amount of signal an imager can handle or by reducing the dark noise level. It can be also concluded that the read noise level is not only an important parameter for the SNR in low-light conditions but also for the DR of a CMOS imager.

For the pixels in an imager, the output is always an analog signal, which in most cases is an analog voltage. Thus, there is an important charge-to-voltage conversion process that takes place inside the pixels [2.1]. The pixel conversion gain is the parameter which quantifies the efficiency of this process. In general, the conversion gain represents how much voltage change is produced by one electron at the output of the in-pixel source follower. Depending on the pixel architecture, the charge-to-voltage conversion process takes place at either the

photo-sensing node or the charge-detection node. The conversion gain is mathematically defined as:

$$CG = \frac{q}{C_{CG} + C_P} \cdot A_{SF} \, [\mu V/e^-] \tag{2-5}$$

where q is an electron charge, C_{CG} is the capacitance of the photo-sensing node or charge detection node, C_p is the parasitic capacitance connected to C_{CG} and A_{SF} is the gain of the in-pixel source follower. The response linearity, uniformity, light sensitivity and random noise of the pixels are all influenced by the conversion gain value and its variation from pixel to pixel. These characteristics also make the conversion gain to be one of the most important parameters of a CMOS imager pixel.

2.2 Spatial Noise in CMOS Image Sensors

The amount of noise in a CMOS imager's output signal depends on a number of noise sources. In general, the noise in CMOS imagers can be divided into two main categories: spatial and temporal noise. The output variation from pixel to pixel under the same illumination condition is referred to as spatial noise. The noise fluctuation over time from an individual pixel is referred to as temporal or random noise. Spatial noise is generally known as fixed-pattern noise (FPN), because it results in a "fixed-pattern" which is visible regardless of the images captured. In this section, the FPN is firstly introduced and discussed with a focus on its physical origin and evaluation method. Then the physical origins of some main temporal noise sources in CMOS imagers are described in Section 2.3.

For CMOS imagers, the components that contribute to spatial noise or FPN can be divided into two categories: offset and gain variation. The artifacts created by the FPN are highly visible to the human eye. This causes a major problem in the output images. Figure 2-2 [2.2] shows a simulated image containing both pixel and column FPN. In Figure 2-2, for both the pixel and column FPN, a Gaussian distributed offset with a standard deviation of 5% of full-scale was added [2.2]. As shown in Figure 2-2, while the amount of pixel and column FPN is equal, the column FPN is much more visible than the pixel FPN. This is because the human eye is often more sensitive to the stripes introduced by column

FPN. According to [2.3], pixel FPN of about 0.5% and column FPN of about 0.1% are generally well-accepted specifications.

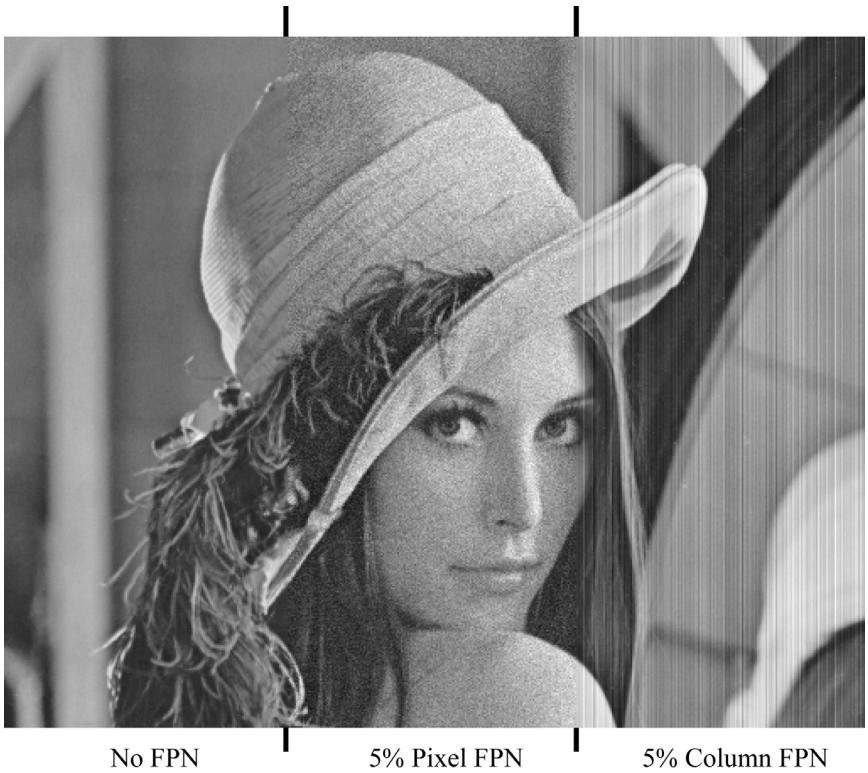

Figure 2-2: *Simulated effects of pixel and column FPN on an image [2.2] (Courtesy of M. Snoeij)*

2.2.1 Fixed-Pattern Noise in Dark

Offset variation is normally the main source of FPN in the dark. There are two main sources of this offset-caused FPN: the mismatch of in-pixel or column-level transistors, and the dark current generation non-uniformity inside the pixels. The dark current generation non-uniformity is due to random variations in the dark current in each pixel. Dark current is the current generated in the pixel in the absence of light. It is not desirable as it contributes to the total noise in the dark.

The imperfection mismatch introduced during the fabrication process of in-pixel transistors induces the pixel-level FPN on images. However, a so-called double sampling (DS) pixel readout scheme is an efficient way to correct this type of FPN. The DS scheme is applied in this way: by sampling the pixel output before and after the charge integration and then subtracting these two samples. In the end, the offset variation caused by the in-pixel transistor mismatch can be reduced and becomes negligible; for example, only a residual pixel offset of 0.09% was reported in [2.4].

The mismatch of the column circuitry in CMOS imagers will cause the column FPN on images. As mentioned above, column FPN is much more noticeable than pixel FPN. However, unfortunately, column FPN is more difficult to remove through circuitry solutions than pixel FPN. Because of this, column FPN is usually corrected in the digital domain of image processing procedures.

Because the DS readout scheme is used, the dark current generated inside the pixels becomes the primary dark FPN source. Although the imager is not illuminated, there is still the dark current generated in the pixel. Since the dark current generated in each pixel is actually non-uniform over the whole pixel array, the dark FPN caused by this dark current generation non-uniformity has to be corrected pixel-by-pixel.

Dark FPN is usually characterized by the dark signal non-uniformity (DSNU), which represents the distribution of the pixel dark output of the whole pixel array. Because the extracted DSNU is normalized with respect to the dark current, it is independent of the exposure time.

2.2.2 Fixed-Pattern Noise under Illumination

Apart from offset, gain variation among the pixels or column circuits also leads to FPN. This gain variation-caused FPN is usually found to be proportional to the illumination levels. Therefore, the gain variation is the main source of FPN under illumination. There are several sources of gain variation in CMOS imagers. Gain variation can be induced by photon collection variations, photon-electron conversion non-uniformities, electron-voltage conversion variations inside the pixels, gain variations among the column circuitry. Therefore, determining exactly what the dominant source is of the gain variation-caused FPN becomes rather difficult. Therefore, any type of FPN is often corrected in the digital domain process with a gain map or a look-up table, as described in [2.5].

The FPN under illumination is normally evaluated by the photo-response non-uniformity (PRNU). The definition of PRNU is the

same as DSNU except it is characterized under illumination conditions. Because PRNU represents the gain FPN under illumination, its absolute value is proportional to the exposure time. However, it is important to be aware that the FPN under illumination is also influenced by DSNU. Thus, the DSNU needs to be subtracted from the raw image data before an accurate PRNU value can be obtained.

2.3 Temporal Noise in CMOS Image Sensors

As discussed in the previous section, FPN in CMOS imagers is fixed in space regardless of the images captured, which makes it relatively easy to be corrected in digital-domain image processing. This leaves the temporal (random) noise as the major limiting performance factor in terms of noise for CMOS imagers. Temporal noise contains several major noise components in CMOS imagers: photon shot noise, dark current shot noise, and read (readout) noise, which generally includes reset noise, thermal noise and *1/f* noise. The physical origins of these different noise sources are described one by one in this section.

2.3.1 Photon Shot Noise

Photon shot noise is the most fundamental noise in all imagers. It is caused by the fact that energy and matter have a fundamentally discrete nature, as best described in the theory of quantum mechanics, rather than by IC technology or imager design. If the photodetector is exposed to a perfectly uniform light source, the number of photon-generated charges will have a random Poisson distribution [2.6]. Therefore, the magnitude of the photon shot noise is equal to the square root of the mean number of charges stored in the photo-sensing area, and given by:

$$n_{SN} = \sqrt{N_{sig}} \tag{2-6}$$

The rms noise voltage in the photo-sensing node or charge detection node is therefore given by:

$$\overline{V_{SN}^2} = CG \cdot N_{sig} \tag{2-7}$$

where n_{SN} is the photon shot noise, N_{sig} is the number of collected signal charges, $\overline{V_{SN}^2}$ is the photon shot noise in volts rms, and CG is the pixel conversion gain defined in Eq. (2-5).

Eq. (2-5) and Eq. (2-7) seem to suggest that an increase in capacitance C_{CG} would improve the photon shot noise, but as shown in Eq. (2-1) and Figure 2-1, the SNR of the imager is actually independent of C_{CG} and mostly determined by the signal level while the photon shot noise is dominating the overall noise: the higher the signal level, i.e. the photon-generated charges, the higher the SNR of the imager.

The constant magnitude dependence on the illumination level is an important and unique property of the photon shot noise. Moreover, because the photon shot noise is caused by a fundamental physical law, it will exist in all imagers without exceptions. Therefore, its square root dependency on the signal level is widely used to characterize the performance of imagers [2.7].

2.3.2 Dark Current Shot Noise

As mentioned in Section 2.2.1, there is dark current generated in the photo-sensing area even without illumination. This generation mechanism is a thermal process which exponentially depends on temperature. Similar to the photon shot noise, dark current generation also follows Poisson statistics, and can be given by:

$$n_{DN} = \sqrt{N_{DK}} \tag{2-8}$$

where N_{DK} is the dark current. The dark current is always referred back to the photo-sensing node or charge detection node of the pixels. The signal source is electrons, thus the dark current shot noise is mostly represented by electrons as well.

The only way to reduce the dark current shot noise is to lower the dark current itself. The dark current generation mechanism and reduction techniques in CMOS imagers are described elaborately in [2.8-2.12].

2.3.3 Reset Noise

Reset noise originates from the thermal noise of the reset switch in CMOS imager pixels, which is usually implemented by an nMOS transistor. While the transistor is switched on, it can be considered a resistor which contains thermal noise. This noise is then sampled and held

by the capacitor of either the photo-sensing area or the charge detection node after the transistor is switched off. If the operation of the photo-sensing elements or charge detection nodes requires a periodic reset operation before the integration mode, this periodic reset operation will lead to reset noise [2.2]. The reset noise power is provided by integrating the thermal noise power over all frequencies. The reset noise in rms voltage can be calculated as:

$$\overline{V_{RS}^2} = \int_0^\infty \frac{4kTR}{1+(2\pi fRC_{PD})} df = \frac{kT}{C_{PD}} \tag{2-9}$$

where k is Boltzmann's constant, T is the temperature, R is the on-resistance of the nMOS transistor switch, f is the bandwidth, and C_{PD} is the capacitance of the photo-sensing area or charge detection node.

There is a very efficient approach to cancel the pixel reset noise, which is the so-called correlated double sampling (CDS) technique [2.13]. To cancel the reset noise, the CDS is configured firstly by taking two *correlated* samples, where one sample contains the reset noise and the other contains the same reset noise and the signal as well, and then subtracting the two *correlated* samples from each other either in the analog domain or digital domain. In this case, CDS is able to reduce the reset noise to negligible levels [2.13]. Although CDS cancels out the *correlated* noise sources, it increases the *uncorrelated* noise: in fact, the *uncorrelated* noise power doubles after CDS subtracting configuration.

2.3.4 Thermal Noise

Thermal noise, also called "white" noise or Johnson noise, is caused by the random thermal motion of charge carriers in conductors. In CMOS imagers, there are two main contributing sources to the overall thermal noise floor: the thermal noise generated by the in-pixel source follower transistor, and the thermal noise from the column circuitry. In general, the thermal noise in rms voltage can be give by:

$$\overline{V_{Th}^2} = 4kTR \cdot BW \tag{2-10}$$

where BW is the bandwidth of the circuit. Therefore, from Eq. (2-10), it can be concluded that the thermal noise can be reduced by modifying the circuit design, i.e. by decreasing the bandwidth of the circuit. A more

in-depth discussion of the design techniques that can largely decrease the thermal noise in CMOS imagers is presented in Chapter 4 and Chapter 5.

2.3.5 *1/f* Noise

Apart from the reset noise and thermal noise, *1/f* noise, also called "pink" noise or flicker noise, is also a main noise source generated inside an MOS transistor. In CMOS imagers, it mainly appears from the in-pixel source follower transistor [2.14]. The first *1/f* noise spectrum was illustrated by McWhorter in 1955 [2.15]. According to McWhorter, the cause of this type of noise is the lattice defects at the interface of the Si-SiO_2 channel inside the MOS transistor. These defects introduce a random current fluctuation by trapping and de-trapping the conducting carries, which is what causes the *1/f* noise. In general, *1/f* noise shows up as a low-frequency phenomenon, while for higher frequencies it is normally overshadowed by white noise from other sources. Therefore, *1/f* noise is often characterized by the corner frequency between the regions dominated by each type.

The amount of *1/f* noise generated inside an MOS transistor can be described as a voltage source in series with the channel, with an approximate spectral density of [2.16]:

$$\overline{V_n^2} = \frac{K}{C_{ox}WL} \cdot \frac{1}{f} \tag{2-11}$$

where K is a process-dependent parameter, C_{ox} is the gate capacitance per unit of gate area, W and L are the width and length of the transistor, and f is the frequency. From Eq. (2-11), it is suggested that to constrain *1/f* noise, only the transistor gate area needs to be carefully designed. However, Eq. (2-11) is only a simplified *1/f* noise power estimation. In reality, particularly as CMOS processes continue scaling down to deep-submicron technology, the actual *1/f* noise power becomes much more complex and involves more design factors [2.17].

The use of CDS can also constrain the *1/f* noise of the in-pixel transistor, but it is only effective when the *1/f* noise is correlated between the two CDS samples. Also, in the frequency domain, the CDS frequency has to be at least twice as high as the *1/f* corner frequency [2.18]. Since *1/f* noise is highly technology-dependent, how it changes as CMOS processes scale down becomes a very important question. From Eq. (2-11), it already clearly shows the inversely proportional relation between *1/f* noise

and the gate area that leads to an expected increase in *1/f* noise as the transistor sizes decrease. More accurate predictions about this tendency are presented in [2.19].

2.3.6 RTS Noise in Deep-Submicron MOS Transistors

As CMOS processes continue scaling down to deep-submicron technology, random telegraph signal (RTS) noise, which is generally considered a special type of *1/f* noise, becomes a dominant noise source for the noisy pixels and limits the imaging quality under low-light conditions [2.20][2.21]. A brief introduction about RTS noise in deep-submicron CMOS imagers is presented and discussed in this section.

Over 50 years of research has gone into *1/f* noise in electronic devices, but the discussion continues about the exact physical mechanisms behind the *1/f* noise in MOS transistors. However, as explained in the previous section, it is generally accepted that lattice defects at the interface of the Si-SiO_2 channel inside the MOS transistor play the most important role [2.15]. When McWhorter [2.15] first showed that the trapping/detrapping process can lead to a *1/f* type spectrum, to this end, he also described the behavior of every single trap as a random telegraph signal (RTS), i.e. a signal that randomly fluctuates between two states. If the power spectral density (PSD) of a single signal is plotted, it yields a Lorentzian spectrum, as depicted in Figure 2-3(a). The corner frequency in this PSD depends on the statistical properties of the RTS noise, which in turn is related to the physical properties of the interface trap. An MOS transistor will usually contain a large number of traps; assuming that these traps do not interact with one another, the PSDs of the individual traps can be added to yield the PSD of the noise generated by the transistor. McWhorter showed that if all the traps inside the transistor generate an RTS with the same amplitude, and the corner frequency of the corresponding PSDs is exponentially distributed, then a *1/f* noise spectrum will result. This is clearly illustrated in Figure 2-3(b). This resulting noise model is called the McWhorter or ΔN model, where ΔN represents the fluctuation of the number of carriers in the transistor channel.

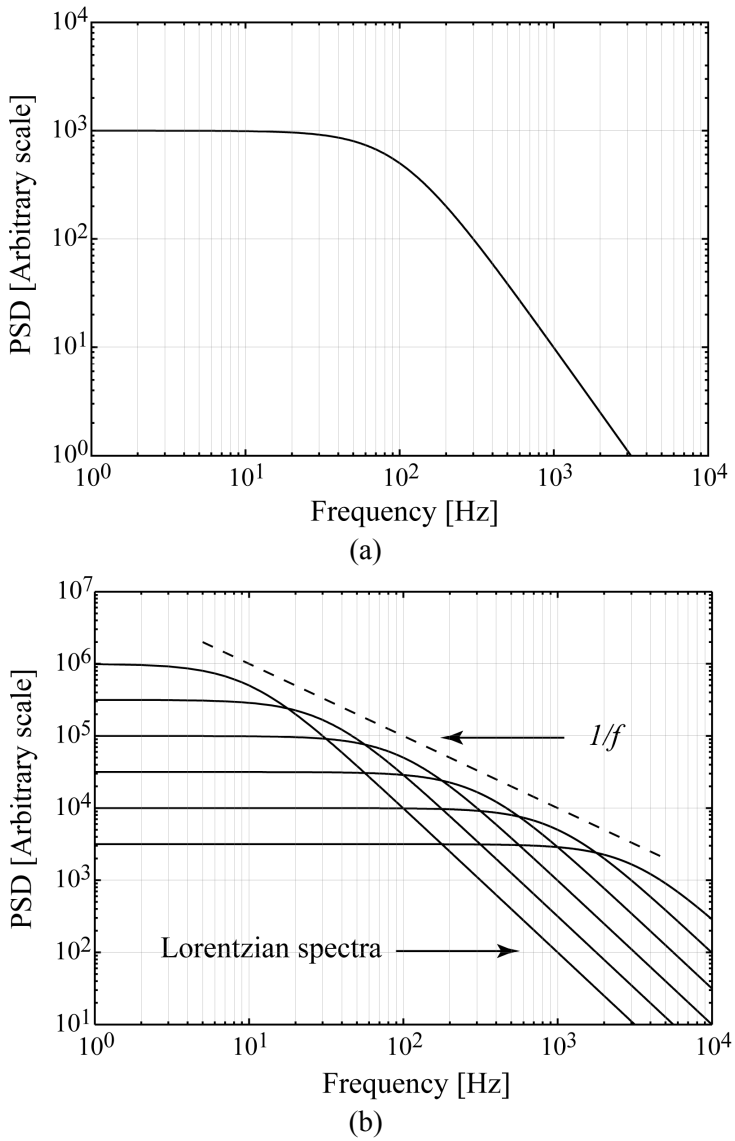

Figure 2-3: *(a) PSD of an RTS spectrum; (b) PSD of the RTS and 1/f spectrum*

Apart from the ΔN model, in 1969, Hooge [2.22] proposed the $\Delta\mu$ model, which considers *1/f* noise to be caused by fluctuations in the

mobility of charge carriers in silicon. The debate between the ΔN and $\Delta\mu$ models went on for years. In 1990, Hung [2.23][2.24] proposed another unique model that includes both the ΔN and $\Delta\mu$ models. This model with the correct parameters agrees well with the measurement results from large MOS transistors. Nowadays, it is generally accepted that pMOS transistors are reported to show behavior in accordance with the $\Delta\mu$ model, while nMOS transistors are more often better suited by the ΔN model.

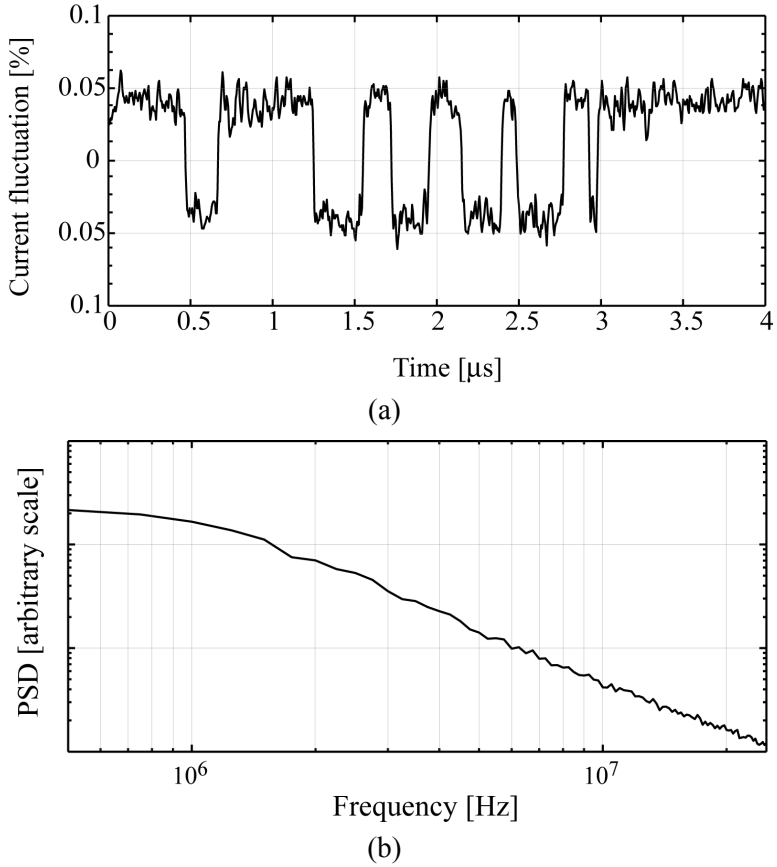

Figure 2-4: *(a) Measured RTS noise in an MOS transistor [2.18]; (b) Corresponding PSD of the measured RTS noise [2.18]*

On the other hand, the McWhorter model makes an interesting prediction for small-area transistors in deep submicron processes. With a

relatively small gate area, small transistors in deep-submicron processes might contain only a few or even only one trap per gate area. Based on the McWhorter model, small transistors with a single trap inside the gate area exhibit an RTS rather than a *1/f* noise spectrum [2.20][2.25]. An example of a measurement from a small transistor in a deep-submicron process is shown in Figure 2-4(a), where the current fluctuation is shown of a transistor with a gate area of 0.18μm^2 [2.19]. As shown in Figure 2-4(a), the current fluctuation clearly has an RTS fluctuation. Figure 2-4(b) shows the corresponding PSD which is a Lorentzian-like spectrum [2.19].

Both the McWhorter model and the experimental results lead to the conclusion that the low frequency noise [2.19] generated by the small in-pixel transistors with a single trap inside the gate area in CMOS imagers will have an RTS noise spectrum, rather than a *1/f* spectrum. As mentioned in the beginning of Section 2.3.6, for the CMOS imagers in deep-submicron technology, the RTS noise in the in-pixel source follower transistor is the dominant noise source, which limits the imaging quality under low-light conditions [2.20][2.21]. Even though extensive efforts have been made in recent years to investigate RTS noise behavior [2.20][2.26-2.28], there is still no convincing evidence that explains the exact mechanism of this noise. However, there are still several approaches to reduce the RTS noise in CMOS imagers. For instance, the RTS noise can be reduced with an increased CDS frequency [2.20] but the increase in CDS frequency can only suppress the RTS noise and not eliminate the noise completely. From the technology perspective, using the in-pixel buried-channel source follower presented in [2.29][2.30] drastically minimizes RTS noise. A more detailed discussion on this technical solution to minimize the RTS noise in CMOS imager pixels is presented in Chapter 3.

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3

A CMOS Imager with In-Pixel Buried-Channel Source Follower

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This chapter presents a CMOS image sensor with 4-Transistor active pixels and a pinned-photodiode which use an in-pixel buried channel source follower and an optimized row selector. The test sensor was fabricated in a 0.18μm CMOS process. The sensor characterization was carried out successfully, and the results show that compared to a regular imager with the standard nMOS-transistor surface mode source follower, the new pixel structure reduces dark random noise by 50%, and improves the output swing by almost 100% without any conflicts with the signal readout operation of the pixels. Furthermore, the new pixel structure is able to drastically minimize the in-pixel random telegraph signal (RTS) noise.

This chapter starts with an introduction to the *1/f* and RTS noise in CMOS imagers and a brief analysis of how to deal with these noise sources. The solution, which uses a buried-channel nMOS transistor, is

proposed. Then, in Section 3.2, the buried-channel device concept is first introduced, and then the simulation and test device characterization results found in [3.1] are mentioned and briefly summarized. Next, the sensor design overview is given in Section 3.3. The measurement results of the test sensor are presented in Section 3.4. At the end of this chapter, some conclusions are addressed.

3.1 Introduction

For year, many attempts have been made to reduce the random noise in CMOS imagers, which is mainly composed of *1/f* and random telegraph signal (RTS) noise [3.2]. Research has revealed that the dominant random noise sources in CMOS image sensors (CIS) are due to the lattice defects at the Si-SiO_2 interface of the in-pixel source follower (SF) transistor [3.3][3.4]. However, the exact mechanism of the RTS and *1/f* noise is still not completely clear [3.5], and the use of correlated double sampling (CDS) cannot fully eliminate *1/f* and RTS noise [3.6][3.7]. Therefore, reducing these noise sources becomes very difficult. Moreover, as CMOS processes scale down, the gate area of the transistors becomes so small that it can easily only have one active interface trap underneath the gate of the transistor, which will induce the quantization of the *1/f* noise, which is the RTS noise. Because of this single electron trapping and de-trapping during transistor operation, the RTS appears in pixels which have only one active interface defect and dominates the pixel temporal noise. RTS noise limits the imaging quality under low-light conditions [3.7][3.8]. Therefore, as long as a perfectly clean gate interface cannot be guaranteed, the *1/f* or RTS noise will stay dominant in the random noise behavior of the pixels.

It has been proven that reducing these noises using circuit techniques is difficult [3.9]. Therefore, the most effective technique can be found in improving of the processing technology. One common method is to adjust the annealing process in order to optimize the gate oxide properties [3.1][3.10]. However, this approach is very process-dependent, and requires very precise control over the annealing temperatures and time. Furthermore, from the noise perspective, simply reducing the number of Si-SiO_2 interface traps through annealing optimization may not help too much. If there are any residual traps that are not removed by the annealing process, the reduction in the interface defect-induced noise by the annealing process will be less significant since a single interface defect

can already introduce an RTS noise level as high as millivolts [3.1]. Therefore, if only a perfectly clean gate interface can be guaranteed, the interface defect-induced noise can be improved by the annealing process, otherwise the annealing process does not help too much.

In order to deal with the imperfect Si-SiO_2 interface-introduced random noise, an alternative approach can be used, i.e. taking the conducting carriers away from the Si-SiO_2 interface by creating a buried-channel nMOS transistor in a modern CMOS imager process. In this chapter, an in-pixel source follower based on a buried channel nMOS transistor is introduced. The buried channel requires only one extra implantation, which pushes the highest potential in the channel away from the Si-SiO_2 interface. Thus, the possibility of carriers being trapped by lattice defects can be minimized and the *1/f* and RTS noise can be diminished. As a result, the random noise level of the imager can be significantly reduced. Furthermore, because the buried channel transistor has a negative threshold voltage, the output swing of the pixels can be drastically improved by the buried-channel source follower (BSF) transistor in combination with an optimized row selector. This means that "digital" transistors with reduced power supply voltages can be used in the pixel without limiting the pixel's output swing, saturation level and dynamic range.

3.2 Buried-Channel nMOS Transistor

In principle, buried-channel transistors represent transistors in which the majority of their conducting carriers flow far beneath the gate Si-SiO_2 interface during operation. Actually in modern CMOS processes, which use a single gate poly process, the p-type MOS transistors are naturally buried-channel devices because of the compensation threshold voltage (V_t) adjustment implantation process during fabrication. Therefore, the expected structure of a buried-channel nMOS transistor is very straightforward, i.e. a total region-reversal from a pMOS transistor, as shown in Figure 3-1.

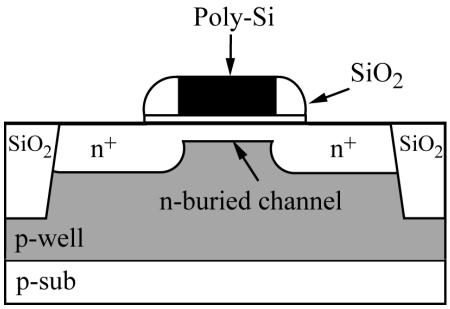

Figure 3-1: *Cross section of a buried-channel nMOS transistor*

The device simulations were done with MEDICI and presented in [3.1]. The device structure, material and doping information were generated by the process simulator TSUPREM. The original simulation files were supplied by TSMC, which described the standard fabrication steps for an in-pixel SF transistor in a 0.18μm CMOS process.

To verify the device characteristics under different implantation conditions, the potential difference between the channel potential and gate interface potential, and the channel depth of the buried channel devices were well simulated, analyzed and discussed in [3.1]. The simulation results shown in [3.1] verify the "buried" concept and feasibility of creating such devices in a modern CMOS process.

The simulated and measured gate characteristics of the surface- and buried-channel test transistors were also compared in [3.1]. The results show that under the same gate bias condition, the transconductance (g_m) increases when increasing the buried channel implantation dose. Meanwhile, the g_m of the buried-channel device is almost half of that of the surface-mode device, which is because the channel is buried into bulk silicon, thus reducing gate-modulation capability, which is an effect similar to increasing the gate oxide thickness. The decreased g_m may cause a longer settling time, but this difference between buried- and surface-mode devices in charging/discharging the column load is not considered, because not the speed operation, but rather low noise, is a design factor.

The buried-channel implantation in fact also changes the gate capacitance of the SF, thus a change in g_m is observed. The BSF pixels should have a smaller capacitance at the floating diffusion (FD) node, but this decrease in the FD capacitance due to buried-channel implantation is

not obvious, because the capacitance of the FD node measured consists of FD active capacitance, SF capacitance (only 1/3), TG overlap capacitance and other parasitic capacitances. According to [3.1], the voltage gain of the SF is increased by buried-channel implantation, thus BSF pixels should have a higher conversion gain at the output of the SF. Here, the voltage gain is defined as the ratio of the output voltage versus the input voltage at the source node of the SF.

In order to inspect how much CMOS imagers may benefit from BSFs in terms of read-out noise, a large number of buried-channel nMOS transistors need to be measured to acquire enough statistical data. Thus the benefits from BSFs in terms of read-out noise can only be proven by measuring the actual sensors.

3.3 Sensor Design Overview

A prototype sensor with BSFs was first fabricated in a 0.18μm 1P3M CMOS process by TSMC. The characterization results of the prototype sensor were already presented and well analyzed in [3.1][3.12]. The noise improvement achieved by using BSFs inside the pixels was rather significant. However, as explained in [3.1], a fundamental trade-off between the maximum pixel output and the image lag did exist in the prototype BSF pixels. Thus, this BSF-induced trade-off leads to a further optimization for such pixels.

3.3.1 Design Goal

Because of the buried-channel doping, the threshold voltage of the nMOS transistor shifts towards a negative value. This helps to increase the pixel output swing, which is the FD node reset voltage minus the voltage drop caused by the dark current on FD node, the SF transistor threshold voltage, and the minimum voltage required to bias the column current source. However, such an improvement is limited by the row select switch, which is normally realized by a standard nMOS transistor. The maximum voltage that can pass through the row select switch is then determined by the gate voltage and threshold voltage of this row select transistor. Therefore, the FD node reset voltage is expected to be reasonably low in order to ensure that the video signal can be properly readout by the row select switch. Meanwhile, a small FD voltage is also preferred in relation to the random noise [3.12]. However, reducing the

FD reset voltage brings the potential risk of an incomplete charge transfer from the photodiode to the FD region, thus introducing image lag. This trade-off actually limits the feasibility and performance of the BSFs pixels. Therefore maintaining the random noise improvement without the design trade-off mentioned above is the sensor design goal.

3.3.2 Design Overview

The new test sensor was fabricated in a 0.18μm 1P4M CMOS process by TSMC. The chip micrograph is shown with several fundamental functional blocks of the prototype chip in Figure 3-2. The pixel array is 200 rows x 150 columns with 10μm pixel pitch. All the pixels are pinned-photodiode 4T designs with BSF, in which 5 columns of pixels are designed with both a BSF and an optimized row selector.

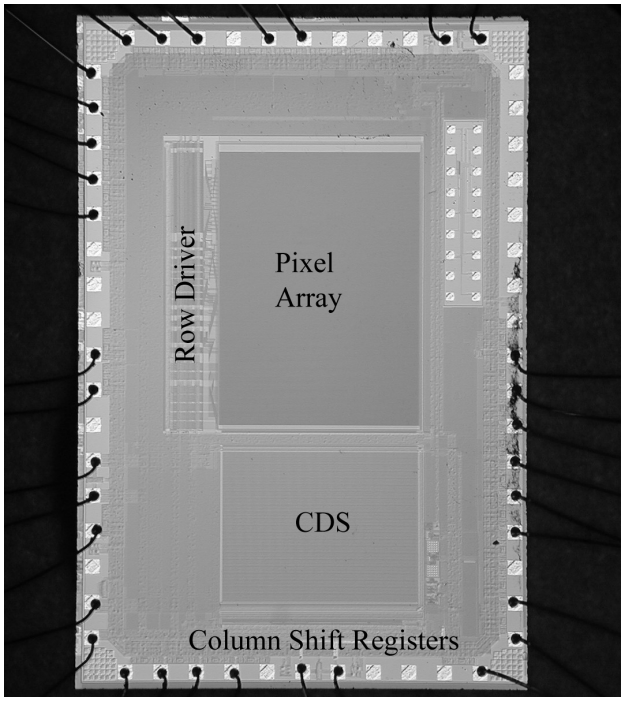

Figure 3-2: *Pixel output swing measurement with different implantation doping and bias currents*

The schematic of the pixel is shown in Figure 3-3, in which BSF stands for the BSF transistor, S/H_R and S/H_S are the column switches for reset and signal level sampling, C_1 and C_2 are the sampling capacitance for the pixel reset and signal level, respectively, and CDS stands for the correlated double sampling. A transmission gate (nRS, pRS) is used as the row selector. An inverter (Mp and Mn) generates the inverted signal pRS for the transmission gate. In the pixel design, the gate signal of the reset transistor (RT) and the charge transfer transistor (TX) can be supplied individually. The row and the column addressing circuitry are realized by the shift register structure.

CDS at each column is used to cancel out the pixel offset, the pixel reset noise, and reduce the *1/f* noise. The pixel output can be amplified 10 times by the CDS amplifier to achieve good noise measurement accuracy. The imager operation timing is supplied by an external FPGA. The 10MHz sensor clock frequency is generated in the FPGA, which is defined as a unit clock signal (clk). The sensor signal is readout during each line time, which is 3000clk cycles in this case. During these 3000clk cycles, one line of pixels is readout to the column bus, CDS is performed, and video signals are readout by an output amplifier one by one from the same line of pixels. The integration time is set by *n* times of the line time, while *n* can be adjusted by an Inter-IC (I^2C) interface and the FPGA coding program. The sensor has a rolling shutter operation. The SF settling time is 0.5µs, which is 5clk cycles. For the noise measurement, the CDS time interval is 1.5µs and the charge transfer period is 1µs. The outputs of the imager are analog signals that are converted into digital signals by an off-chip image processor with a 12bit ADC. The exact analog signal processing chain of a CMOS imager is well explained in [3.13].

3.4 Measurement Results

The new test imager was successfully fabricated and tested. The measurement results are presented and discussed as follows.

Pixel random noise can be measured by calculating the standard deviation of each pixel output from multiple frames. However, in order to distinguish the random noise from the pixels or from the analog processing, one common approach is to switch off the row select (RS) transistor and the column load transistor during operation. The signal on the column connects to a DC voltage, and then the measured random noise

is the noise of the analog chain. After switching on the RS transistor and the column load transistor, if there is any additional random noise introduced by either the in-pixel transistors, the column load transistor or photodiode operation, there is evidence that the measured noise indeed stems from the pixel-readout noise sources instead of the analog chain. Then, after switching on the RS transistor, if there is any additional random noise introduced by the in-pixel transistor or photodiode operation, there is evidence that the measured noise indeed stems from the pixel-level noise sources instead of the analog chain. In order to exclude the contribution of the photon shot noise from the total noise floor, all the noise measurements were carried out in complete darkness

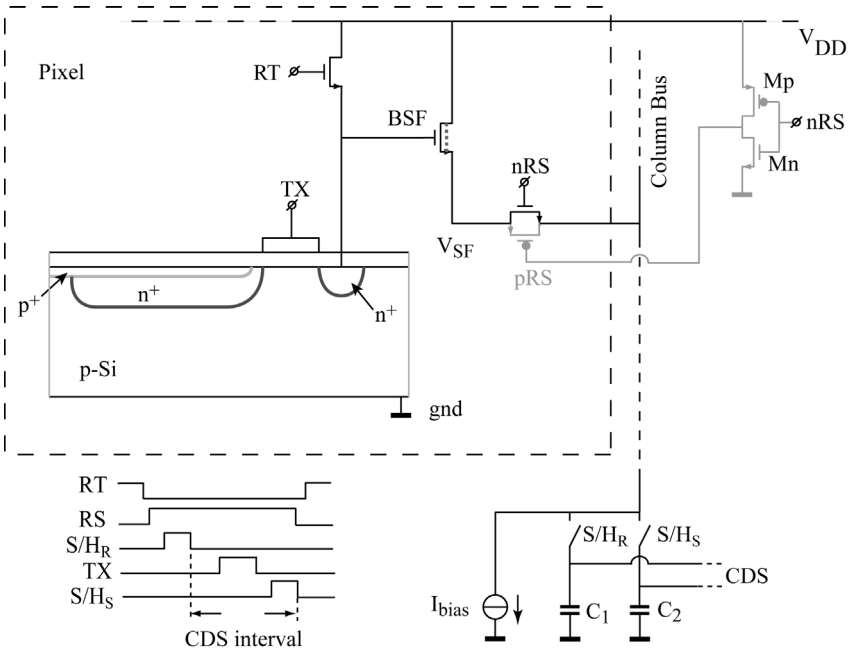

Figure 3-3: *Pixel schematic and front-end read-out timing*

The dark random noise of BSF and SSF pixels was measured with the new test sensor. Both the BSFs and SSFs were biased with 6μA current, which is the lowest bias current available for the pixel source followers for measurements. A lower bias current helps to bury the channel deeper [3.1], which will consequently help to reduce the random noise. In the prototype sensor, the FD reset voltage (V_{rt}) of the SSF pixels was 2.6V,

while in order to ensure the row select transistor works properly, the measurement was done with a low FD reset voltage on the BSF pixels, i.e. 1.8V [3.1]. Yet with the optimized row selector, the dark random noise can be measured with a 3V FD reset voltage on the BSF pixels in the new test sensor.

The measurement results from the prototype sensor are presented in [3.12]. The results from the new BSF pixels with the optimized row selector are shown in Figure 3-4. The transistor dimension for both the BSFs and SSFs are the same in the prototype and the new test sensors, i.e. W/L=0.42µm/0.5µm. The measurements were processed with an analog sensor gain of 10, at 17fps, at room temperature and with an off-chip 12bit ADC. The CDS interval is 1.5µs with the transfer gate (TX) transistor grounded. The FD reset voltage of both the new BSF pixels with optimized row selector and the SSF pixels is 3V. For the new BSF pixels with the optimized row selector (10µm pixel pitch), the fill factor is 33% and the conversion gain is 41µV/e^-.

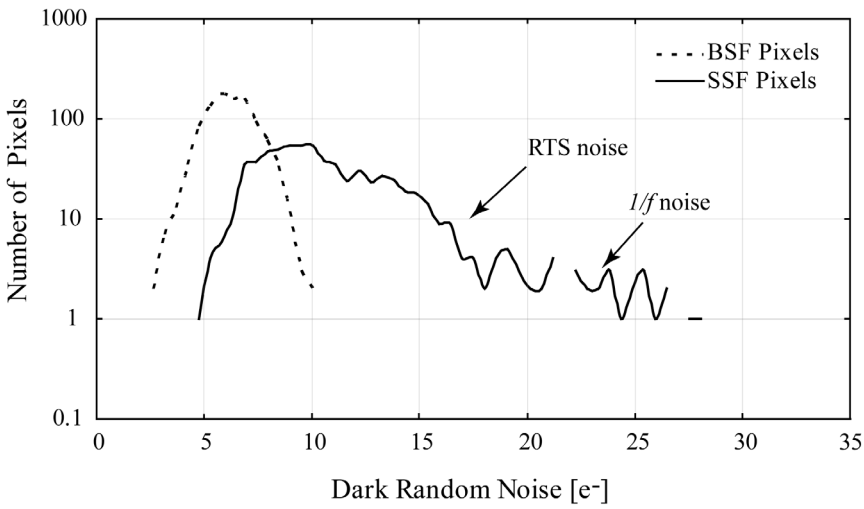

Figure 3-4: *Histograms of the dark random noise for BSF and SSF pixels in the new test sensor*

The random noise of each pixel was obtained by calculating the standard deviation over the recorded output of 20 frames. The asymmetric distribution of the pixels around the peak of the SSF pixel curve indicates the dominance of the SSF *1/f* and RTS noise. Compared to previous results

[3.12], the same random noise improvement is still shown in the pixels with BSFs and the optimized row selectors. The average dark random noise of the BSF pixels is about 5e$^-$, which is a reduction of about 50% compared to the SSF pixels, and the noise histogram of the BSF pixels closely approximates a true Gaussian distribution with a significantly reduced noise spread.

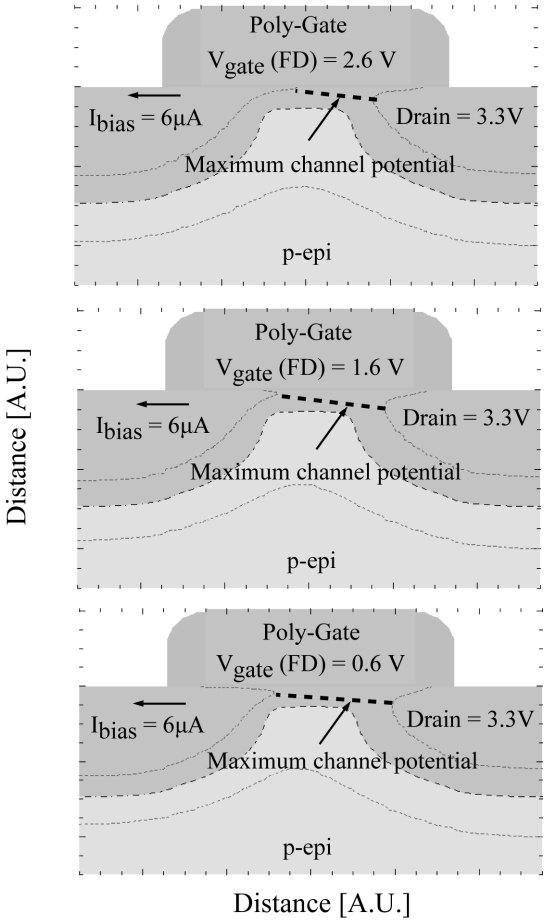

Figure 3-5: *Simulation of the depletion region and the channel location of a BSF with different gate biases [3.1]*

As shown in Figure 3-5 [3.1], the simulation results of the depletion region and the channel location change of a BSF pixel with varying FD

voltages are presented. It can be seen that the FD reset voltage (gate bias) has a strong influence on the potential distance between the channel potential and both the gate interface potential and depletion region at the Si-SiO_2 interface. Reducing the gate bias helps to push the channel deeper, extending the depletion region at the interface further toward the source side. This condition means the total channel length will have more area working as a buried-channel mode rather than a surface mode; in other words, it can be concluded that the total buried-channel length is increased by reducing the gate bias.

From the new test sensor, the measurement result of the average dark random noise as a function of different FD voltages, V_{rt}, is shown in Figure 3-6. Clearly, the relationship between pixel random noise and source-follower channel depth is confirmed by the results. The channel is buried deeper by lower FD voltages; therefore, the measured random noise is smaller for lower FD voltages. However, a low FD voltage may introduce image lag because of the incomplete charge transfer.

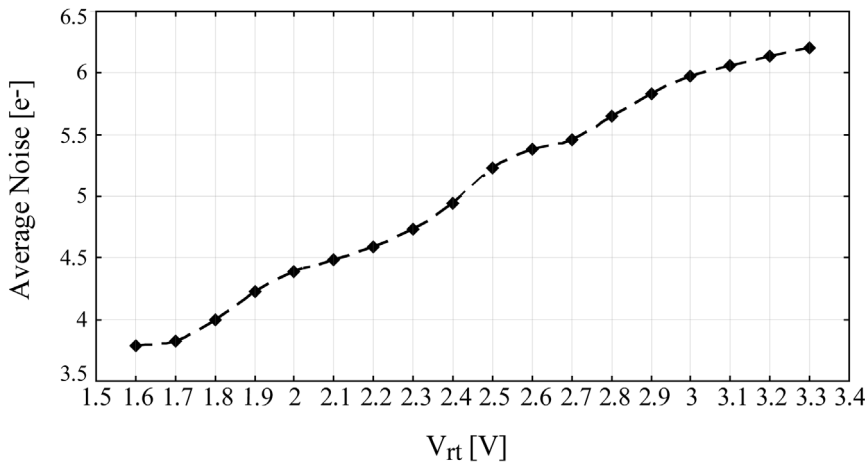

Figure 3-6: *Dark random noise measurement with different FD voltages*

Figure 3-7 shows the QE measurement results of the pinned-photodiode in the SSF and BSF with optimized RS pixels, respectively. The pixel fill factor is not included for the results shown in Figure 3-7, which is 33% for BSF pixels with optimized RS pixels and 45% for SSF pixels. As is shown, the optimized RS contains a pMOS

transistor introduces an n-well inside the pixel. During pixel configuration, this n-well remains biased to a high voltage, i.e. the power supply, which turns it into an additional photon-generated-electron sink during exposure, thus hurting the QE of the pinned-photodiode, especially for longer wavelengths of light detection. However, it should be noticed that the QE for 550-600nm wavelengths, at which the pixels have the most sensitive QE, is only decreased by about 10% due to the optimized RS. This QE decrease does not negatively impact the SNR of BSF pixels too much, because with a 50% random noise improvement, the SNR of BSF pixels still increases by x1.8 times.

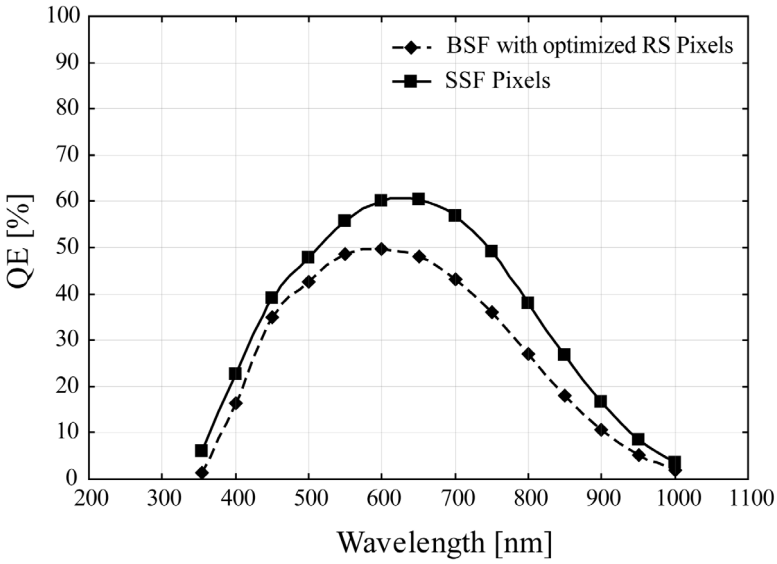

Figure 3-7: *Quantum efficiency of pinned-photodiode in SSF and BSF with optimized RS pixels (without microlens)*

3.5 Conclusions

A CMOS image sensor with an in-pixel buried-channel source follower and an optimized row selector has been presented. Compared to a conventional surface-mode source follower design, the buried-channel source follower can reduce dark random noise by more than 50%, improve the noise spread, and significantly reduce the *1/f* and RTS noise component, with the cost of QE attenuation. However, because of the

noise reduction capability of the BSF technique, such a penalty on QE will not hurt the SNR of the BSF pixels. Compared to previous work [3.12], the newly designed buried-channel source follower with an optimized row selector still shows the same attractive dark random noise performance and, moreover, is able to eliminate the trade-off between the noise reduction and the pixel output swing improvement.

3.6 Acknowledgement

The device simulation results were provided by Dr. X. Wang in his work in [3.1] and [3.12]. The author would like to thank him for his substantial contribution and support in this chapter, and especially thank Dr. S. G. Wu's team at TSMC for their support in modifying the process flow.

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4

Noise Reduction by Correlated Multiple Sampling

In Chapter 3, a technological point of view to reduce the pixel random noise was introduced. In this chapter, the research focus of this thesis is shifted from technology to design. This chapter mainly introduces and discusses the correlated multiple sampling (CMS) technique. CMS is a very effective technique to suppress the read noise floor of CMOS imagers.

This chapter starts with an introduction in Section 4.1 about the work principle of the CMS technique in CMOS imagers. The SNR improvement resulting from the use of a CMS technique in CMOS imagers is also presented and analyzed in the this section. Next, in Section 4.2, two different approaches to implement the CMS technique in CMOS imagers are introduced and analyzed with design samples. Then, based on theoretical modeling and simulations, the noise reduction effects achieved by the CMS technique are discussed in Section 4.3. At the end, in Section 4.4, the conclusions are outlined.

4.1 Introduction

For CMOS image sensors, correlated double sampling (CDS) is an indispensable noise reduction technique, because it can effectively reduce

reset noise and pixel output offset. However, for low-light level imaging, an extremely low-noise floor is a must-have property for CMOS imagers, and CDS is not that sufficient to achieve such a requirement. Therefore more advanced noise reduction techniques are required. Correlated multiple sampling (CMS) is thus developed and used in the column-parallel noise reduction circuits for low-noise CMOS imagers [4.1-4.6].

4.1.1 Principle of CMS Technique

Figure 4-1 shows the concept and sampling diagram of CMS in the sensor output from a 4T pixel structure. The reset level of the pixels is firstly sampled *m*-times (A_1, A_2...A_m) and then after the charge transfer, the signal level is also sampled *m*-times (B_1, B_2...B_m). The *m*-times sampling sum of reset and signal levels are subtracted from each other and then averaged. This process can be expressed as:

$$V_{out} = \frac{1}{m}\sum_{i=1}^{m}(A_i - B_i) \tag{4-1}$$

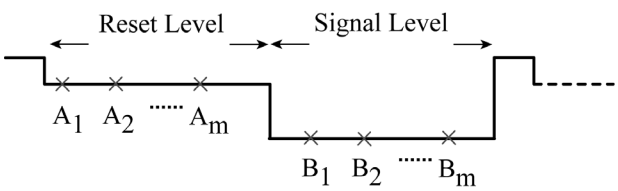

Figure 4-1: *Sampling diagram and the sensor output with CMS*

This approach can effectively reduce the read noise in a flat spectrum, for instance the thermal noise, by a factor of $\sqrt{m}$ [4.1]. According to [4.2-4.4], when *m* is very large, the CMS technique also reduces the random telegraph signal (RTS) noise, which is the dominant random noise source in noisy pixels. More about the noise reduction effects by the CMS technique is addressed in Section 4.3 of this chapter.

4.1.2 SNR Estimation after CMS

As mentioned in Chapter 1, compared to the popularly-used EMCCDs for low-light imaging [4.7], CMOS imagers with a high SNR are desired. By assuming the absence of fixed-pattern noise, then Eq. (2-1) can be simplified as:

$$SNR = 20\log\left(\frac{QE \cdot P}{\sqrt{n_{SN}^2 + n_{DN}^2 + n_{RN}^2}}\right)[dB] \tag{4-2}$$

where QE is the quantum efficiency of the pixels, P is the number of input photons on the pixel area, n_{SN} is the photon shot noise, which equals $\sqrt{QE \cdot P}$, n_{DN} is the dark current shot noise and n_{RN} is the read noise. If the CMS technique is applied, and assuming the read noise in a flat spectrum is dominant, the SNR of the CMOS imagers can be then expressed as:

$$SNR = 20\log\left(\frac{QE \cdot P}{\sqrt{QE \cdot P + n_{DN}^2 + \frac{n_{RN}^2}{m}}}\right)[dB] \tag{4-3}$$

where m is the number of samples taken for the CMS.

On the other hand, for the sake of comparison, the SNR of EMCCDs can be calculated as:

$$SNR = 20\log\left(\frac{QE \cdot P}{\sqrt{F^2 \cdot (n_{SN}^2 + n_{DN}^2) + \frac{n_{RN}^2}{g^2}}}\right)[dB] \tag{4-4}$$

where F is the excess noise factor contribution by the noise in the electron multiplication process [4.8], and g is the electron multiplication gain in EMCCDs. Based on Eq. (4-3) and Eq. (4-4), the figure-of-merit of the SNR of CMOS images and EMCCDs for low-light level imaging can be investigated and compared.

Figure 4-2 shows the theoretical plot of the SNR comparison between an EMCCD and CMOS image sensor (CIS) with the CMS technique. In

order to obtain the plot, a number of assumptions were made. *QE* was assumed to be 70%, very low temperature was assumed so that dark current can be ignored, *g* was assumed to be 1000, and the read noise of CMOS imagers was assumed to be $5e^-$. *F* and the read noise of the EMCCD were set as 1.41 [4.8] and $10e^-$, respectively. For the CMS technique, 1, 4, 16 and 64 times of multiple samplings were applied, where *m*=1 signifies the CDS configuration. The readout circuits were assumed to be fully settled during the CMS implementation.

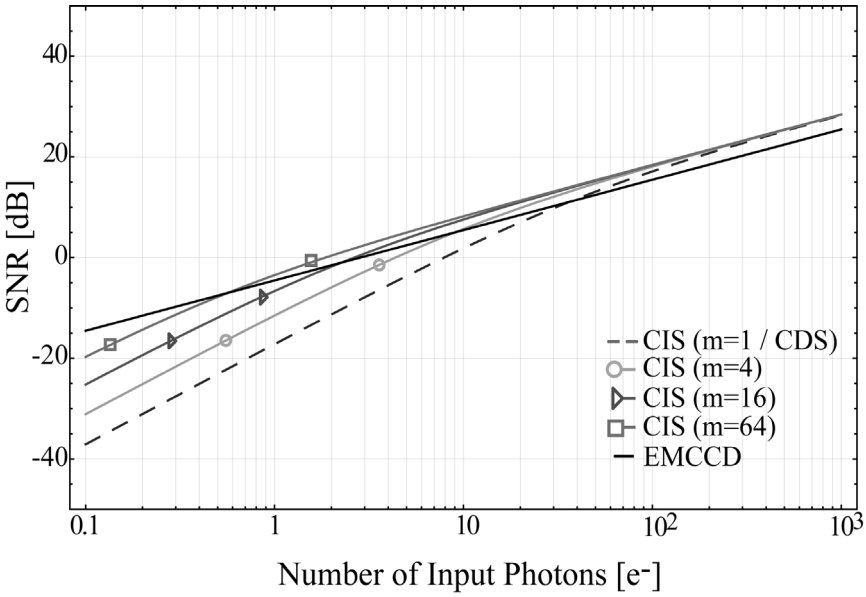

Figure 4-2: *SNR comparison between the EMCCD and CMOS image sensor (CIS) with the CMS technique*

Figure 4-2 shows that the EMCCD has a better SNR for low-light level imaging than the conventional CIS with only CDS. However, applying the CMS technique can improve the SNR of the CIS. As the number of sampling times increases, the intersecting point of the SNR plot between the EMCCD and CIS steadily moves closer to the left side of the figure. This indicates very interesting consequence: for very low-light level imaging, for instance, as shown in Figure 4-2, at 0.6 input photons, the CIS with 64 CMS samples taken has a better SNR than the EMCCD.

From the SNR calculation and comparison, it can be concluded that the use of a CMS technique will indeed offer a very positive impact on the

SNR of the CIS for low-light level imaging: the well-improved SNR is better than that of the EMCCD for low-light imaging. Yet how should this technique be implemented in a CIS? In the next section, two different approaches to implement the CMS technique will be presented and discussed.

4.2 CMS Technique Implementation

In recent years, researchers have put in a great deal of effort with regard to sensor design to implement the CMS technique in the readout circuits of CISs for low-light level imaging [4.1-4.6]. In general, there are two main approaches to implement the CMS technique in CMOS imagers: using column-parallel analog integrators or column-parallel ADCs, both of which are introduced and discussed as follows.

4.2.1 CMS Using Column-Parallel Analog Integrators

Figure 4-3 shows the redrawn schematic diagram of the column-parallel switched-capacitor (SC) integrator with two sample-and-hold (S/H) capacitors for the CMS configuration and readout [4.4]. The CMS is implemented as follows: firstly, the circuits start with the initialization of the feedback capacitor C_{fb} by closing the switches S_r. During this phase, the pixel reset level is also sampled on C_{in} by closing switches S_1, with switches S_{sr} also closed until the end of the pixel reset level samplings; secondly, by closing switches S_2 and opening S_1, the charge stored in C_{in} is transferred to C_{fb} and stored on C_{sr}. Then, the output of the sampled voltage is given by:

$$V_{sc}(1) = \frac{C_{in}}{C_{fd}} \cdot (V_{rst}(1) - V_{ref}) \tag{4-5}$$

The second sampling of the pixel reset level is done by closing switches S_1 and opening switches S_2 again while the charge from the previous sampling is stored on C_{sr}. This operation can be repeated for m-times; then the final output sampled on C_{sr}, which represents m-times pixel reset level sampling, can be expressed as:

$$V_{sc}(m) = \frac{C_{in}}{C_{fd}} \cdot \sum_{i=1}^{m} (V_{rst}(i) - V_{ref}) \tag{4-6}$$

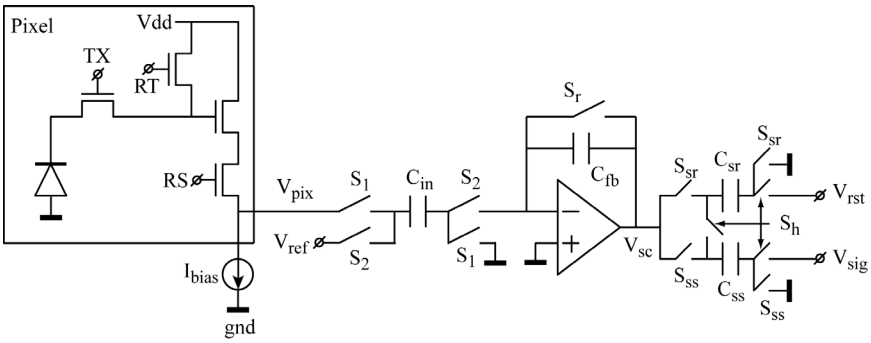

Figure 4-3: *Schematic diagram of the column-parallel integrator for CMS, redrawn from [4.4]*

The same configuration is done for *m*-times pixel signal level samplings and the output is sampled on the capacitor C_{ss} by closing switches S_{ss} and opening S_{sr} throughout this *m*-times pixel-signal level samplings phase. Then, when C_{in} equals C_{fb}, the final video signal of the pixels is taken by the averaged differential voltage sampled on C_{sr} and C_{ss}, and given by:

$$V_{out} = \frac{1}{m} \sum_{i=1}^{m} (V_{sig}(i) - V_{rst}(i)) \tag{4-7}$$

The advantage of this design is the effectiveness of the noise reduction and the flexible sampling-times setting [4.4]. However, for the *m*-times CMS configuration, the maximum output voltage swing of the SC integrator ($V_{sc\text{-}max}$) limits its maximum input range (V_{pix}) to $V_{sc\text{-}max}/m$, thus leading to a reduction in the pixel dynamic range. One solution is the folding integration CMS (FI-CMS) technique proposed in [4.4]. However, it needs extra circuits in the columns and also introduces some extra digital coupling noise [4.4]. A cost-effective design for implementing the CMS technique is thus necessary for low-light level imaging.

4.2.2 CMS Using Column-Parallel ADCs

Recently, column-parallel A/D converters (ADCs) with low bandwidth readout have been presented [4.9-4.11]. These ADCs do not use analog output buffers, the noise of which is significant in the overall noise of the signal readout path in a CIS. Thus the use of a low-noise, high-resolution column parallel ADC would improve the low-noise performance of the image sensors. Due to its simple circuit topology, good linearity and noise performance, the single-slope ADC (SS-ADC) is nowadays widely used [4.5-4.9] as column-parallel ADCs for CISs. Moreover, with these column-parallel SS-ADCs, the digital CMS approach, which performs both the multiple sampling and processing (generally averaging) in the digital domain, can be implemented [4.5]. This further helps the noise reduction and SNR enhancement for CISs to meet the requirements for low-light level imaging. A design example is shown in Figure 4-4. As shown in Figure 4-4, the simplified schematic diagram consists of the 4T pixel with a pinned-photodiode and a column-parallel SS-ADC. The column SS-ADC consists of a comparator driven by a ramp voltage V_{ramp} and a bit-wise inversion (BWI) counter [4.12].

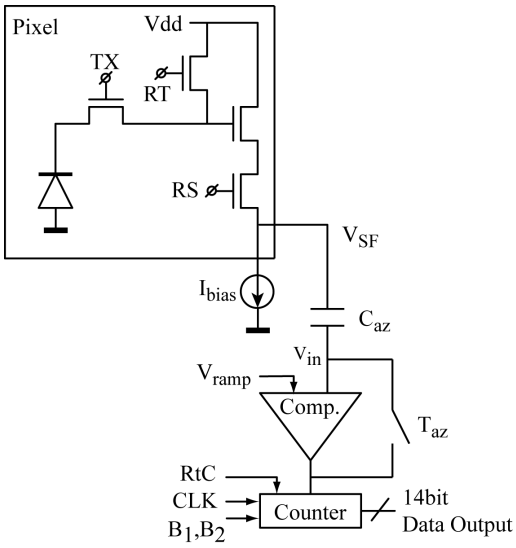

Figure 4-4: *Schematic diagram of pixel and the proposed column readout circuits*

Figure 4-5 shows the timing chart for the sensor operation with a digital CMS process of 4 times. First, the reset signal resets the pixel sensing node causing the reset level output to appear in the pixel output. After the pixel sensing node reset, the comparator reset switch T_{az} is closed to eliminate the offset of the comparators and the pixel output. The reset level is then compared with the ramp voltage V_{ramp}, and the BWI counter is set to count up synchronously. Whenever the reset level is higher than V_{ramp}, the comparator output toggles its output status to stop the BWI counter from counting. V_{ramp} ramps up and down for 4-times to configure the 4-times sampling. After the signal charges are transferred, V_{SF} adjusts itself to the pixel signal level. During the charge transfer period, every bit of the BWI counter is inverted by the control signals B_1 and B_2. The BWI counter is then set to up-count again from this negative ADC result for the pixel signal level sampling. V_{ramp} is configured in the same manner as the 4-times pixel reset level sampling. Finally the counter digitally subtracts the conversion of the 4-times sampling of the reset signal from the sensor signal, and then averages the ADC output in the digital domain.

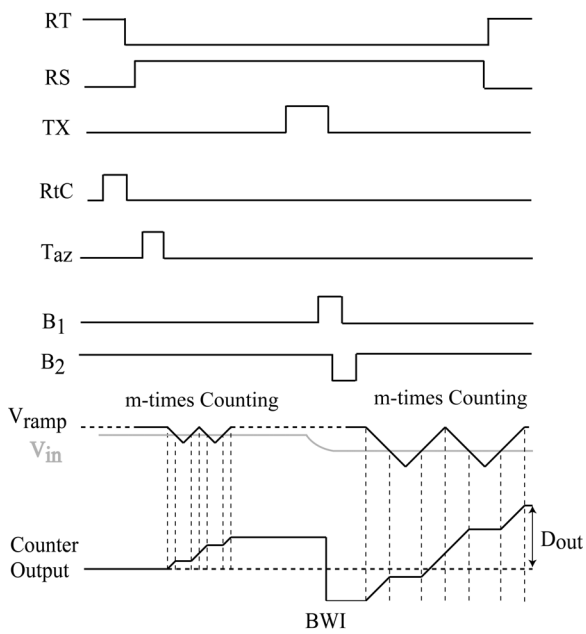

Figure 4-5: *Timing diagram of the column readout chain for the digital CMS*

In implementing the CMS technique, the main drawback of using column-parallel ADCs is the maximum sampling time limited by the highest resolution of the ADCs. However, the biggest benefit, as shown in [4.5], is the noise reduction in the pixel readout circuits without any additional circuits, power consumption and column areas. Moreover, compared to the design shown in [4.4], the architectural simplicity of these circuits also makes it much easier to implement the design and adapt it to other process technologies. More details about the implementation of column-parallel circuits using the column-parallel ADCs with the digital CMS approach to provide the CIS with low-noise and an enhanced SNR is presented and discussed in Chapter 5.

4.3 Modelling and Simulation of Noise Reduction Effects

To analyze the noise reduction effects by CMS technique, the transfer function-based noise analysis method [4.13][4.14] is used. Thus, together with the noise power spectrum and system transfer function, the noise reduction effects of different noise components, such as thermal noise and *1/f* noise by the CMS technique, can be calculated and analyzed in the frequency domain.

4.3.1 Effect on Thermal Noise

Due to the averaging operation in the CMS configuration, the CMS readout can be characterized in the frequency domain as a 1st-order low-pass filtering or band-narrowing operation. Because of this characteristic, for m-times sampling, the CMS technique can reduce the thermal noise by a factor of $\sqrt{m}$. More information about the thermal noise reduction effects by the column-parallel circuits with the CMS technique is presented and analyzed in Chapter 5.

4.3.2 Effect on *1/f* Noise

With the transfer function-based noise analysis method, the *1/f* noise reduction effect by the CMS technique using column-parallel analog integrators is well calculated and discussed in [4.1][4.4]. According to the calculations and simulations in [4.1][4.4], it was revealed that as the

sampling number increases, the more effectively the CMS technique can suppress the *1/f* noise than CDS.

However, as shown in Figure 4-4, if the CMS is configured with the column-parallel ADCs in the digital domain, then how will the *1/f* noise be affected? Actually, this can be solved by modifying the sampling diagram and system transfer function described in [4.4] as shown in Figure 4-6(a).

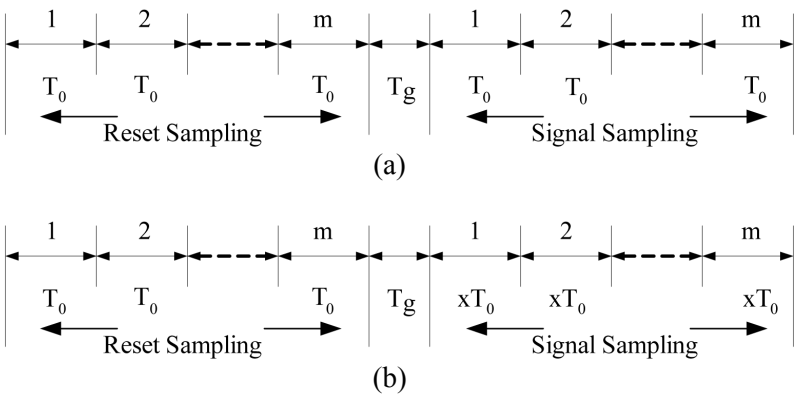

Figure 4-6: *(a) Sampling diagram of the CMS operation in [4.4]; (b) Sampling diagram of the digital CMS operation*

The sampling diagram for the digital CMS operation shown in Figure 4-5 is illustrated in Figure 4-6(b). In Figure 4-6(b), T_0 is the sampling period; T_g is the interval between two groups of multiple samplings, which is defined as $T_g = M_g T_0$, where M_g is an integer. As shown in Figure 4-5, the reset and signal level sampling periods are actually unequal, so during the signal level sampling period, a factor of x is introduced into each sampling phase. Then the final output voltage, $\Delta V(nT_0)$, before averaging as a function of discrete time, is written as:

$$\Delta V(nT_0) = \sum_{k=0}^{m-1} \{ V_p[(n-k)T_0] - V_p[(n-k-m-M_g+1-k(x-1))T_0] \} \quad (4\text{-}8)$$

where $x \geq 1$ and k represents the k-th sample during CMS configuration. Then, following the same calculating method described in [4.4], the transfer function of CMS configuration before averaging is obtained with

a z-transform, which converts a discrete time-domain signal into a frequency-domain representation, and is expressed in the z domain as:

$$H_x(z) = \frac{(1-z^{-m})}{1-z^{-1}} - \frac{(1-z^{-xm}) \cdot z^{-(m+M_g-1)}}{1-z^{-x}} \tag{4-9}$$

If $z = \exp(j\omega T_0)$, and then the *1/f* noise power after m-times CMS is given as follows:

$$\overline{V_{n,cms}^2} = \frac{1}{m^2}\int_0^{\infty}\left(\frac{k_f}{f} \cdot \frac{1}{1+(\omega/\omega_c)^2}\right)\left|H(e^{j\omega T_0})\right|^2 df \tag{4-10}$$

where ω_c is the cut-off angular frequency of the sampling circuits for CMS and k_f is the flicker noise coefficient [4.1].

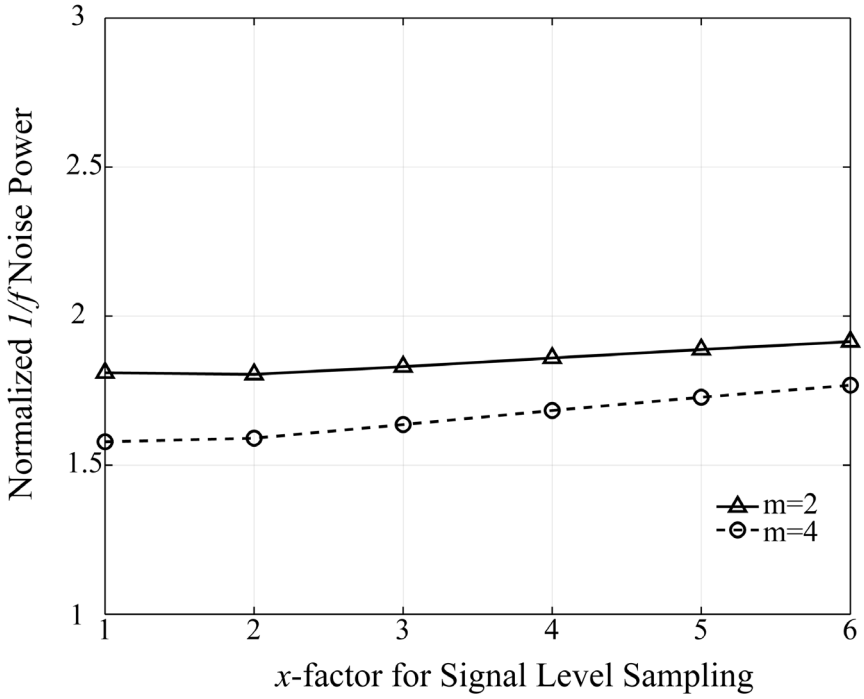

Figure 4-7: *1/f noise as a function of x*

By using Eq. (4-9) and Eq. (4-10), and assuming M_g=1, the *1/f* noise power after CMS configuration as a function of x can be simulated, as is shown in Figure 4-7. The noise power is normalized by a factor of k_f. As shown in Figure 4-7, as the factor of x increases, the normalized *1/f* noise power increases as well, but this increase is rather insignificant as long as the value of x is kept small. Thus, it can be concluded that for effective noise reduction with the digital CMS technique, each signal level sampling period should be minimized.

4.4 Conclusions

The CMS technique for CIS read noise reduction and SNR enhancement was introduced and discussed in this chapter. From the SNR simulation results, it was shown that with the use of the CMS technique, the SNR of CMOS imagers in the low-light level region can be well improved and even exceed that of EMCCDs. Compared to the design shown in [4.4] for CMS technique implementation, the digital CMS using column-parallel ADCs does not need additional circuits in the columns, and its architectural simplicity makes implementing the design much easier.

4.5 Acknowledgement

The author would like to thank Dr. S. Suh from Shizuoka University, Hamamatsu, Japan, for his kind help in the numerical simulation of the *1/f* noise reduction effect for CMS operation.

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5

Digital Correlated Multiple Sampling for Low-Noise CMOS Imagers

This chapter will be published as: Y. Chen, Y. Xu, A. J. Mierop and A. J. P. Theuwissen, "Column-Parallel Digital Correlated Multiple Sampling for Low Noise CMOS Image Sensors", in IEEE Sensors Journal

This chapter presents a low-noise CMOS image sensor using column-parallel high-gain signal readout and digital correlated multiple sampling (CMS). The sensor used is a conventional 4T active pixel with a pinned-photodiode as the detector. The test sensor was fabricated in a 0.18μm CMOS image sensor process from TSMC. The input-referred random noise from the pixel readout chain is reduced in two stages, first using a high gain column-parallel amplifier and second by using the digital CMS technique. The dark random noise measurement results show that the proposed column-parallel circuits with the digital CMS technique are able to achieve $127\mu V_{rms}$ input-referred noise. The significant reduction in the sensor read noise enhances the sensor's SNR by 10.4dB. Such sensors are very attractive for low-light imaging applications, which demand high SNR values.

This chapter starts with Section 5.1, which introduces and provides the background on a new topology of column-parallel circuits. This new topology can provide CMOS imagers with further reduced low-noise and

thus an enhanced SNR. The concept, design and measurement results are presented in the following subsections. In Section 5.2, the image sensor, the topology of the low-noise column-parallel circuits, and their operation principles are described. In Section 5.3, a detailed noise analysis is provided and the noise reduction obtained using the proposed column-parallel circuits is discussed. The noise measurement results from the test chip are shown in Section 5.4. Finally, the conclusions are outlined in Section 5.5.

5.1 Introduction

Generally, CMOS image sensors (CISs) for low-light level imaging require a low-noise performance. To achieve very low-noise performance at low-light levels, preamplifiers are often used. Preamplifiers usually have very high analog gains and are thus useful to suppress the noise contribution from the subsequent readout electronics [5.1-5.7]. Another approach is to use the correlated multiple sampling (CMS) technique to reduce the random noise from the pixels and the readout circuits [5.8-5.11]. However, both approaches fall short in applications such as scientific imaging, medical imaging, etc., where usually a very high signal-to-noise ratio (SNR) is desired. Therefore, in order to enhance the SNR of CMOS imagers to meet the requirements for low-light imaging application, certain readout chain circuits with a further reduced read noise floor and high-gain amplification are necessary.

Recently, column-parallel single slope analog-to-digital converters (SS-ADCs) with low bandwidth readout have been presented [5.11-5.13]. As mention in Chapter 4, the use of these single slope SS-ADCs would improve the overall noise performance of the imagers. Also, with these column-parallel ADCs, the digital CMS approach can be implemented, which further helps in noise reduction. As just mentioned, for low-light levels a column amplifier with high-analog gain can effectively reduce the random noise contribution of the subsequent electronic circuitry, thus effectively increasing the SNR [5.1-5.7]. Therefore, in this chapter, a new topology of column-parallel circuits that uses not only a column gain amplifier but also a column ADC for the digital CMS approach is presented. The proposed design is able to provide the CMOS imager with further reduced low-noise, thus enhancing its SNR.

5.2 Design and Principle of Operation

5.2.1 Sensor Column Architecture

Figure 5-1 shows a simplified schematic diagram of the 4T pixel with a pinned-photodiode and the proposed column readout circuits, including a gain amplifier and an SS-ADC. The pixel operation requires three control signals: a sensing node reset (RT), photodiode charge transfer (TX) and row select switch (RS), which can be controlled by row decoders. Besides the pixel, the sensor readout chain and the external components also contribute to the overall noise of the sensor. The noise from the readout chain usually dominates the pixel read noise over a wide bandwidth. The use of the column gain amplifier can reduce this large noise contribution by amplifying the signal, which narrows the bandwidth resulting from the conservation product of the gain and bandwidth, before the rest of the read noise is added. The gain here is defined by the capacitance ratio of C_{in}/C_{fb}, where C_{in} is the input capacitor, and C_{fb} is the feedback capacitor of the column gain amplifier, respectively. C_p is the column parasitic capacitor. The output of the column gain amplifier is connected to the column SS-ADC using an auto-zero capacitor C_{az}. The column SS-ADC consists of a comparator driven by a ramp voltage and a bit-wise inversion (BWI) counter [5.14]. The BWI is composed of a ripple counter and BWI cells to perform the A/D conversion by counting the number of clocks until the comparator output changes.

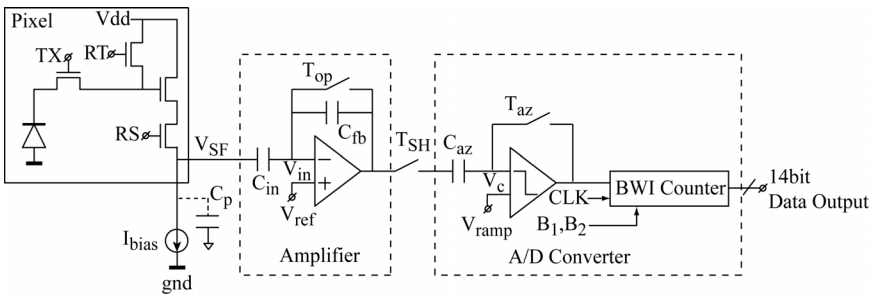


Figure 5-1: *Schematic diagram of the pixel and the proposed column readout circuits*

The advantage of using a ripple counter is that it does not need to be synchronized while using a high speed clock. The BWI counter shows a

32% reduction in power consumption and 2.4 times improvement in the maximum speed over the conventional up/down counter [5.14]. After the ADC, the digital output of the sensor is ready to be readout.

5.2.2 Principle of Operation

Figure 5-2 shows the readout timing diagram of the pixel and column readout chain. Initially, the floating diffusion (FD) node of the pixel is reset, and then the column gain amplifier and the comparator are reset sequentially. The pixel reset transistor (RT), the amplifier reset switch T_{op}, and the comparator reset switch T_{az} are closed sequentially. This sequential closing of the reset switches produces a "cascaded noise cancelling" process [5.6] which isolates the reset noise and offset noise of the preceding stage by storing it in a subsequent capacitor and cancels it by analog correlated double sampling (CDS) [5.6][5.12]. The digital CMS sequence is as follows. After the FD node is reset, the reset level is available in the column. The reset level is compared with the ramp voltage V_{ramp} generated by a digital-to-analog converter (DAC) and the BWI counter is set to count up simultaneously. When V_{ramp} is equal to the reset level, the comparator output toggles from digital "high" to digital "low", which stops the BWI counter from counting. The BWI counter value directly corresponds to the reset level in the column. For *m*-times sampling of the reset level, the reference ramp voltage V_{ramp} for the comparator is up- and down-ramped for *m*-times while the BWI counter counts *m*-times up. The latched counter output thus corresponds to the *m*-times sampling of the reset level available on the column. It should be noticed that if the ramp voltage is configured only in one ramping direction for *m*-times sampling, a high transient noise will be generated each time the ramp voltage flips back to its starting voltage level. This transient noise will consequently degrade the noise reduction effect of CMS, because it cannot be suppressed by CMS. This problem can be solved by configuring the ramp voltage, as shown in Figure 5-2.

After the signal charge from the photodiode is transferred to the FD node, V_C, as the input voltage of the comparator, rises to the amplified signal level voltage accordingly. During the signal charge transferred from the photodiode to the FD node, every bit of the BWI counter is inverted to perform 1's complement operation by applying the control pulses B_1 and B_2. Then after this inversion, the BWI counter holds the negative digital value corresponding to the count of the *m*-times pixel reset-level sampling. From this negative digital value, the BWI counter is then set to

up count *m*-times again during the pixel signal-level sampling. The ramp voltage is configured in the same manner as in the case of the pixel reset level sampling. Eventually the counters will digitally subtract the *m*-times sampling sum conversation of the reset signal from the sensor signal, and then average the output in the digital domain. When *m* is 1, only the digital CDS is performed by the column readout chain. During the whole conversion, the switch T_{SH} is always closed in order to monitor the column voltage of the source follower, V_{SF}.

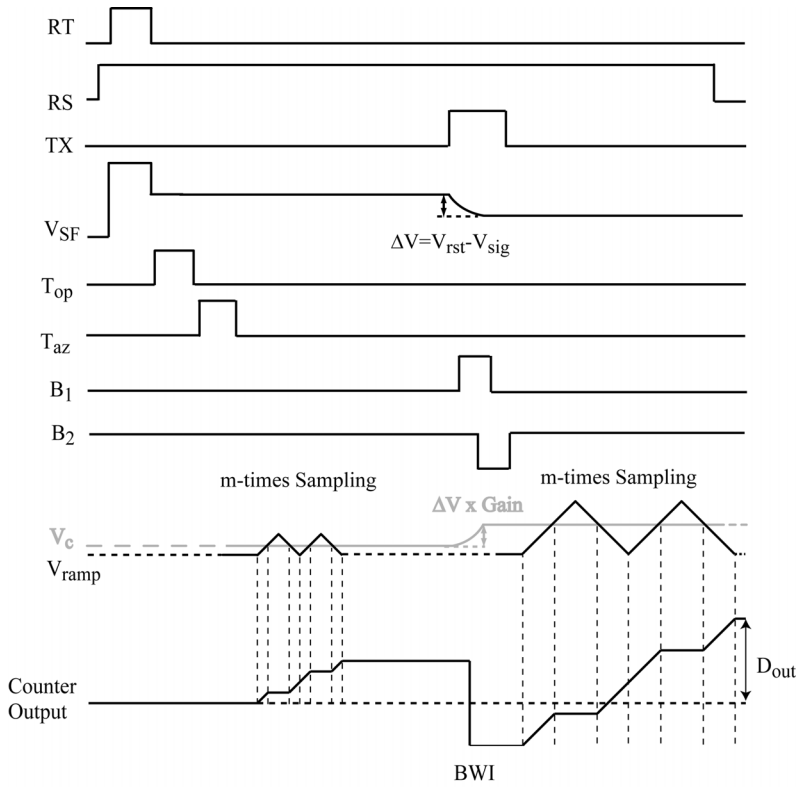


Figure 5-2: *Timing diagram of the column readout chain for digital CMS*

The advantage of this CMS technique is the high thermal-noise suppression capability in the readout chain circuits, which can be reduced by a factor of $\sqrt{m}$, where *m* is the number of samples. Also, the hardware complexity of the ADC is independent from the exact value of *m*, since

only a change in the clocking pattern determines *m*, thus making the ADC easy to reconfigure. According to [5.8-5.10], the CMS technique is also useful in reducing the random telegraph signal (RTS) noise, which is the dominating random noise source for noisy pixels in CISs, when a large value for *m* is applied. The RTS limits the imaging quality under low-light conditions for CISs in deep-submicron technologies [5.15][5.16].

5.2.3 Column-Parallel Gain Amplifier

A column-parallel gain amplifier is used to amplify the voltage difference between its inverting and non-inverting input nodes. Figure 5-3 shows the schematic of the column-parallel gain amplifier used in Figure 5-1, in which *Vin+* and *Vin-* are the non-inverting and inverting input nodes, V_{out} is the output node, and vp_1, vp_2, v_n and v_b are the bias signals of the amplifier, respectively. The amplifier is implemented using a folded-cascode architecture which gives high open-loop gain at a 3.3V power supply. The closed-loop gain of the amplifier is set by the ratio of the input capacitor C_{in} and the feedback capacitor C_{fb}, as shown in Figure 5-1. The specifications and simulated performance of the column-parallel gain amplifier are summarized in Table 5-1.

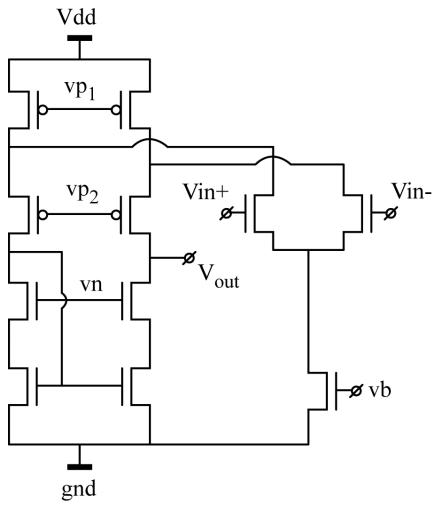


Figure 5-3: *Schematic of the folded-cascode column gain amplifier*

Table 5-1. *Simulated Column-Parallel Gain Amplifier Specifications*

Parameters	Value
Power supply	3.3V
Gain stage	x2, x4, x8, x12
Output swing	1.35V
Open-loop gain	81.6dB
-3dB Bandwidth	3Hz ~ 11MHz (Gain=12)
Phase margin	>62.68° (Gain=2)
SNR	65~70dB
Total noise	129μV_{rms} (Gain=1)
Power dissipation	0.39mW
Settling time	<160ns (Gain=12)
Slew rate	>25V/μs (Gain=12)

5.3 Noise Analysis

The noise reduction effect by the proposed column readout chain is mainly stems from the column-parallel gain amplifier and subsequent digital CMS. To estimate the noise performance, after the reset noise and offset of each stage are cancelled, the thermal noise through the readout chain is analyzed as follows.

The total noise contributed by the pixel source follower usually has 3 main components: the thermal noise in the reset phase, the thermal noise in the amplification phase [5.7], and the frequency-related *1/f* and RTS noise. The thermal noise of the pixel source follower at the output of the column gain amplifier, $\overline{V_{ns}^2}$, is given as [5.18]:

$$\overline{V_{ns}^2} = \frac{kTG^2 N_{sf}\xi_{sf}}{C_p + C_{in}} + \frac{kTG^2 N_{sf}^2 \xi_{sf}}{g_{ms}}\omega_a \tag{5-1}$$

where G is the amplifier closed-loop gain, defined by C_{in}/C_{fb}, k is Boltzmann's constant, T is the absolute temperature, C_p is the column parasitic capacitor shown in Figure 5-1, g_{ms} is the transconductance of the source follower, ω_a is the cutoff angular frequency of the column gain amplifier, and N_{sf}, ξ_{sf} are the noise gain factor and excess noise factor of the source follower, respectively [5.17][5.18].

The first and second terms of Eq. (5-1) represent the source follower thermal noise component in the reset phase and the amplification phase, respectively. During the reset phase, the column gain amplifier is in unity-gain configuration mode; the first term in Eq. (5-1) represents the source-follower thermal noise in this phase which is sampled on the amplifier's input capacitor. The input capacitor of the amplifier consists of the input capacitor C_{in} and column parasitic capacitor C_p. This thermal noise, which is also referred to as the sample-and-transfer noise component in [5.7], is transferred to the feedback capacitor C_{fb} in the amplification phase and eventually sampled in the comparator auto-zero capacitor C_{az} in Figure 5-1. Because this noise component stays unchanged during the amplification phase, it is sampled as a fixed charge on the capacitor and can be cancelled by the digital CMS later.

Figure 5-4 shows an equivalent schematic for deriving the noise of the column gain amplifier during the amplification phase. The noise of the column gain amplifier is represented by the noise voltage source at the input ($\overline{V_n^2}$). The output noise of the column-gain amplifier during the amplification phase, $\overline{V_{na}^2}$, is given as [5.6][5.18]:

$$\overline{V_{na}^2} = \frac{kT\xi_a(1+G)^2}{g_m}\omega_a \tag{5-2}$$

where g_m and ξ_a are the transconductance and excess noise factor of the gain amplifier, respectively, and ω_a is approximately equal to $g_m/[(1+G)C_L]$ [5.6][5.18], in which C_L is the load capacitance of the gain amplifier.

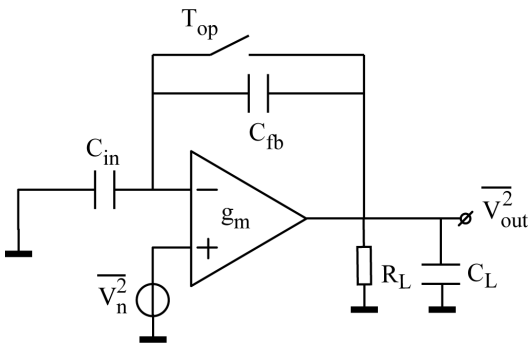
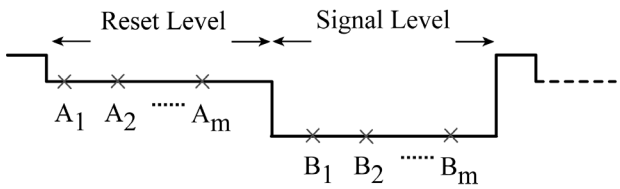


Figure 5-4: *Equivalent schematic diagram for column-parallel gain amplifier noise analysis in the amplification phase*

Figure 5-5 shows the sampling diagram and the sensor output using digital CMS. The thermal noise from the readout chain is reduced by a factor of $\sqrt{m}$ using m-times digital CMS. Therefore, for G >>1, the resulting input-referred noise from the proposed readout chain with CMS, $\overline{V_n^2}$, is given as:

$$\overline{V_n^2} = \frac{2}{m}\left(\frac{kTg_m N_{sf}^2 \xi_{sf}}{g_{ms} C_L (1+G) G_{sf}^2} + \frac{kT\xi_a}{C_L(1+G)G_{sf}^2} + \frac{\overline{V_{no}^2}}{G^2}\right) \tag{5-3}$$

where G_{sf} is the gain of the pixel source follower, and $\overline{V_{no}^2}$ represents the other thermal noise source in the readout chain. Eq. (5-3) shows the reduction in the input-referred thermal noise of the gain amplifier and the pixel source follower by a factor of $\sqrt{G}$, where G is the closed-loop gain of the column amplifier. The other thermal noise is reduced by a factor of G. Through the CMS and averaging process, the overall thermal noise is further reduced by $\sqrt{m}$, where m is the number of sampling times.



$$V_{out} = \frac{1}{m}\sum_{i=1}^{m}(A_i - B_i)$$

Figure 5-5: *Sampling diagram and the sensor output with CMS*

5.4 Measurement Results

A prototype test sensor with the proposed column-parallel readout circuits was designed and fabricated in a 0.18μm 1P4M CIS process from TSMC. The specifications of the test sensor are summarized in Table 5-2. Figure 5-6 shows the test chip microphotograph. To test the functionality and to better understand the proposed column-parallel readout circuits, a small array of pixels was implemented. Due to the limited chip area and wire bonding conditions, the column gain amplifier array was implemented on the right side of the chip layout, rather than underneath

the pixel array. The test setup for the sensor characterization included a PCB board and a frame grabber board which was installed in a desktop computer. The sensor output data was collected by the frame grabber board, then analyzed and recorded in real time by Labview for the measurements. The phase-lock loop (PLL) and DAC circuits, which are needed to generate the ramp voltage, were implemented externally. The sensor's configuration timing is supplied by an external FPGA. The system clock frequency driving the sensor is 10MHz, and a 120MHz clock is used to drive the column-parallel SS-ADC during the sensor performance characterization. By varying the configuration of the ramp voltage, the sensor can provide 10bit or 12bit output resolution.

Table 5-2. *The Prototype Test Chip Specifications Summary*

Specification	**Value**
Process	TSMC 0.18μm 1P4M CIS
Chip size	2.34mm (H) x 1.46mm (V)
Pixel type	4T APS with pinned-photodiode
Pixel size	10μm (H) x 10μm (V)
Number of effective pixels	7 (H) x 2 (V)
Power supply	3.3V (A) / 1.8V (D)
Output	10/12-bit digital resolution
Column-parallel amplifier gain	x2, x4, x8, x12
Digital CMS mode	1, 2, 4, 8, 16 in 10bit resolution 1, 2, 4 in 12bit resolution

The 14bit column-parallel SS-ADC has an n-bit resolution margin for the m-times sampling of pixel outputs, where $n= log_2(m)$. A successive configuration of the digital CMS with m-times sampling in a k-bit ADC resolution has a total equivalent data resolution of $k+n$ bits, where k is 10 or 12 for the test chip. Therefore, for the dark random noise characterization, the digital CMS is able to continue up to 16-times oversampling in a 10bit ADC resolution mode; if the ADC is in a 12bit resolution mode, the digital CMS is continued up to 4-times oversampling.

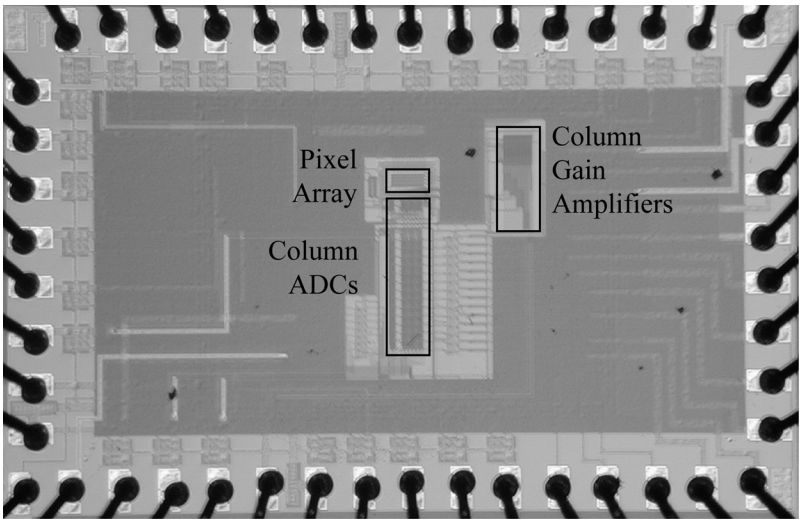


Figure 5-6: *Test chip microphotograph*

Figure 5-7 shows the output of the column readout chain with different column amplifier gains. The measurement is done with limited amount of light to prevent the pixels from becoming saturated at the amplifier output in the column, and only digital CDS, i.e. a digital CMS with $m = 1$. There are two types of gain error associated with the column gain amplifier: the gain amplification error and the gain deviation error among the columns. The results show that the maximum gain error from the column gain amplification is about 0.8%, which is defined by the ratio of the measured amplified output codes over the ideal ones. The maximum column gain deviation error is about 5%, which is defined by the ratio of the output standard deviation among the columns over their averaged values after amplification. The gain-deviation errors within columns cause a residual fixed pattern noise (FPN) at the column level. The column-based digital correction technique proposed in [5.4][5.5] can be useful to reduce the effects of the column FPN.

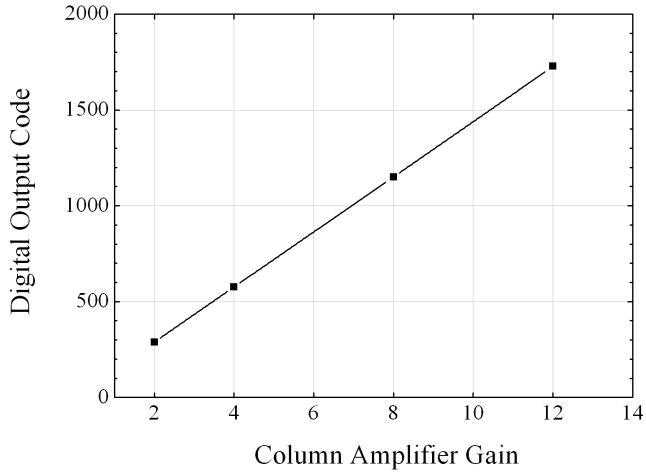
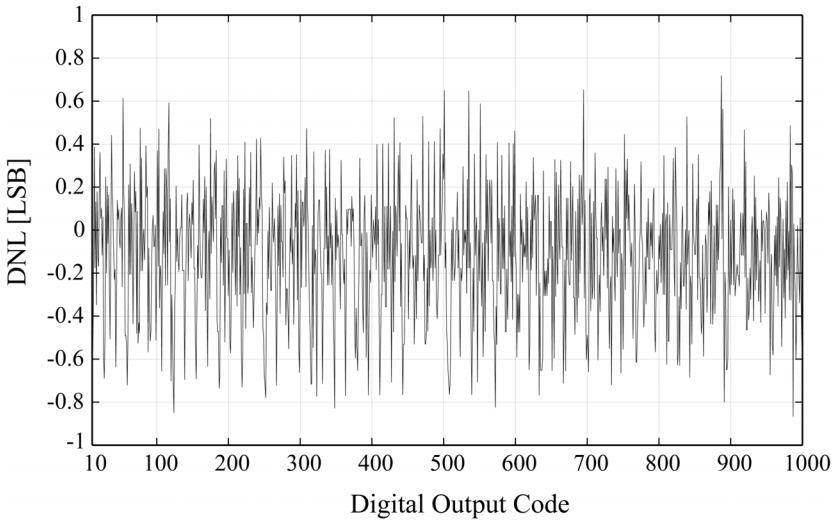


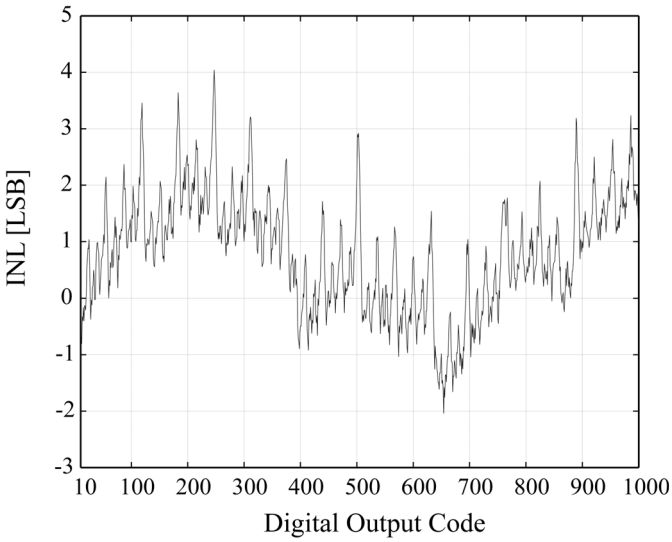
Figure 5-7: *Output characterization of the column readout chain*

Figure 5-8(a) & (b) show the measured differential nonlinearity (DNL) and integral nonlinearity (INL) plot of the column-parallel SS-ADC. The histogram test approach [5.19] is used to measure the non-linearity of the SS-ADC. A 1.5Hz sinusoidal wave signal was applied to the ADC after low-pass filtering. From the measured results, the worst DNL is within -0.8/+0.6 least significant bit (LSB) and the worst INL is within -2.0/+4.0 LSB, which corresponds to a 0.58% nonlinearity. The non-linearity of the ADC is well below the nonlinearity of the pixel (pinned-photodiode and source follower), which is at least 1% and thus can be neglected [5.20]. The parasitic capacitance from the input to the output of the comparator may be the probable cause of this nonlinearity; it can be further improved by the layout optimizations.

Figure 5-9 shows the measured random noise of the sensor versus the column amplifier gain in the 12bit ADC resolution mode. Only digital CDS (m=1) was applied to this measurement. It is shown that when the column amplifier gain G increases, the noise first decreases by a factor of G and then by a factor of $\sqrt{G}$, which corresponds to the tendency indicated in Eq. (5-3).



(a)



(b)

Figure 5-8: *Measured column ADC nonlinearity in 10bit resolution mode: (a) DNL; (b) INL*

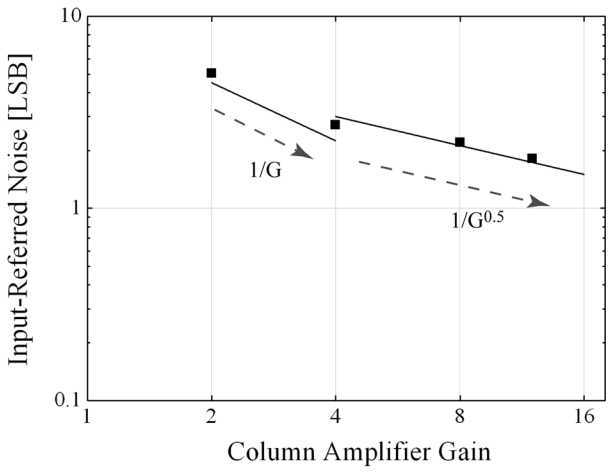
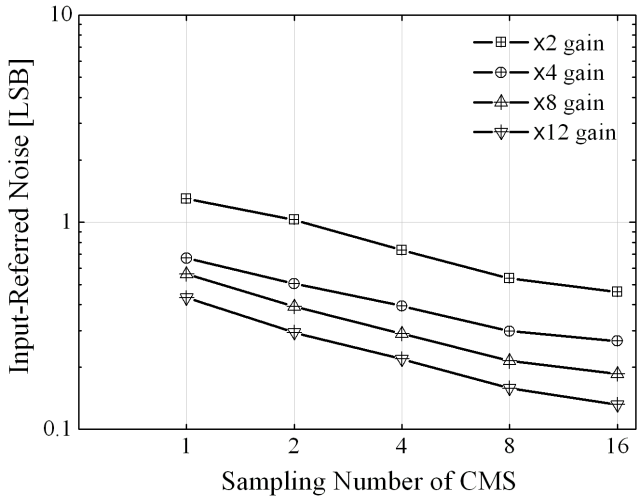
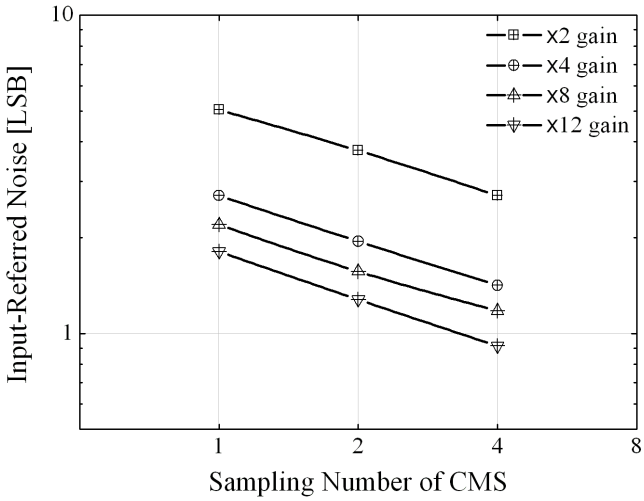


Figure 5-9: *Measured random noise versus the column amplifier gain*

Figure 5-10(a) & (b) show the input-referred dark random noise measurement results of the test sensor in 10bit and 12bit ADC resolution mode. While in 10bit ADC resolution, the complete configuration time from the pixels to the column readout chain is 5.7µs for digital CDS, and it is up to 65µs for 16-times digital CMS. While in 12bit ADC resolution mode, it is 23.8µs for digital CDS, and then up to 62µs for 4-times digital CMS. Compared to the noise after a x12 column amplifier gain and CDS, the dark random noise reduction in the proposed readout chain with digital CMS is about 70% in 10bit ADC resolution mode, where the gain of the column amplifier is 12 with 16-times digital CMS. This noise reduction results in a 10.4dB increase in the SNR. Furthermore, the dark random noise reduction is about 50% in 12bit ADC resolution, where the gain of the column amplifier is 12 with 4-times digital CMS. This noise reduction increases the SNR by 6dB. The input-referred dark random noise is $127\mu V_{rms}$ with a column amplifier gain of 12 when 16-times digital CMS is used in 10bit ADC resolution mode, a noise of $219\mu V_{rms}$ is obtained with a column amplifier gain of 12 with 4-times digital CMS in 12bit ADC resolution mode. It is also observed that the noise reduction effect of digital CMS is limited by the noise in the frequency domain, i.e. *1/f* noise from the pixel source follower, as the number of sampling times increases.



(a)



(b)

Figure 5-10:*Measured input-referred dark random noise of the sensor in: (a) 10bit ADC resolution mode; (b) 12bit ADC resolution mode*

Table 5-3. *Performance Comparison with State-of-the-Art*

Reference	Technology	ADC Type	ADC Resolution	CG[1] [μV/e⁻]	Noise[2] [μV_{rms}]
[5.2]	0.13μm CMOS	SAR	14bit	45	131[3]
[5.11]	90nm CMOS	SS	10/12bit	110	121[4]
[5.12]	0.18μm CMOS	SS	10/12bit	40	284
[5.21]	0.13μm CMOS	ΔΣ	13bit	80	152
[5.22]	0.18μm CMOS	Cyclic	13bit	61	299
[5.23]	0.18μm CMOS	Folding integration/ Cyclic	13bit-19bit	67	80
[5.24]	0.35μm CMOS	MRSS	10bit	46	490
This work	**0.18μm CMOS**	**SS**	**10/12bit**	**45**	**127**[5]

[1]: conversion gain
[2]: input-referred random noise
[3]: at x8 analog gain
[4]: at x16 analog gain
[5]: at x12 analog gain

A comparison of this work with the state-of-the-art is listed in Table 5-3. As is shown, compared with [5.11], [5.12] and [5.24], which also use column-parallel SS-ADCs, this work achieves the state-of-the-art random noise performance.

5.5 Conclusions

A prototype CMOS image sensor with a new type of column readout chain was presented. The test sensor achieves a low-noise performance by using the column-parallel gain amplifier together with a digital CMS algorithm. Contrary to the other approaches that implement the CMS technique such as the folding integration (FI) CMS technique in [5.10],

our proposed design does not need extra circuits in the columns. Because the CMS technique in our design is configured in the digital domain, it makes the sensor readout scheme very straightforward. What is more, compared to [5.10] and [5.23], the architectural simplicity of our proposed circuits makes it much easier to implement the design and adapt it to other process technologies. The measurement results show that the proposed column-parallel circuits achieve about a gain amplification error of about 0.8% and 0.58% nonlinearity. Due to the limited chip area, using a large number of pixels for the noise characterization with detailed information is not an option with this of prototype test sensor. However, even with a limited number of pixels, the dark random noise measurement results show that the use of the proposed column-parallel circuit with the digital CMS technique is still able to achieve a drastic reduction in the random noise, i.e. a nearly 70% reduction. This is an attractive benefit when using this proposed column-parallel circuit to enhance the SNR of imagers with 10.4dB for low-light imaging applications. For a further improvement using the proposed column-parallel circuit with a large number of pixels, the residual column level FPN introduced by the high-gain column amplifier has to be constrained. The column-based digital correction techniques proposed in [5.4][5.5] or off-chip FPN cancellation techniques can minimize this noise source.

5.6 Acknowledgement

The author would like to thank Yang Xu for her kind help and support in the column gain amplifier design and layout.

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6

A Low-Noise CMOS Imager for Radio-Molecular Imaging

As presented in Chapter 3 and Chapter 5, two different approaches to reduce the pixel random noise level - buried-channel source follower and digital correlated multiple sampling - were introduced and discussed. In this chapter, a low-noise CMOS image sensor that utilizes these approaches for low-noise imaging is presented. The pixel random noise can be efficiently reduced by using a high-gain column-parallel amplifier together with the digital correlated multiple sampling technique. Although pixel *1/f* and RTS noise limit the noise reduction effect [6.1] for a given sampling frequency when the signals are well settled, the use of an in-pixel buried-channel source follower can drastically minimize this noise. Therefore, the proposed CMOS imager can provide very low random noise. Also, compared to a conventional CIS without any noise suppression techniques, this work demonstrates a 40-times input-referred random noise reduction, which corresponds to a 32dB SNR improvement. As emphasized in Chapter 1, such an significant improvement in SNR is very attractive for low-light level imaging, such as the radio-molecular imaging, for which a high SNR is always required.

This chapter starts with Section 6.1 which is an introduction to the low-noise designs used in this CMOS imager. Next, in Section 6.2, the

architecture of the prototype sensor is briefly described. Then in Section 6.3, the noise measurement results as well as the captured sample images in very low-light conditions are presented. Finally, some conclusions and discussions are presented.

6.1 Introduction

As presented in Chapter 5, using a column-parallel amplifier with a high analog gain and the digital correlated multiple sampling (CMS) approach can largely improve the read noise floor of CMOS imagers. This design can efficiently suppress the random noise in a flat spectrum, e.g. the thermal noise. When the random noise in the flat spectrum is suppressed to the level at which it no longer dominates the read noise floor, the low frequency random noise, i.e. *1/f* and RTS noise, will start to dominate the read noise floor. This phenomenon limits the noise-reduction effect of our proposed design in Chapter 5. On the other hand, as introduced in Chapter 3, the in-pixel buried-channel source follower (BSF) technique has shown decent capability of pixel RTS noise minimization [6.2][6.3]. Therefore, by combining these three techniques together, i.e. using a high-gain column-parallel amplifier together with the digital CMS technique and an in-pixel buried-channel source follower, the read-noise floor of the CMOS imagers can be reduced to a very low level, for example, below $1e^-$. The noise and SNR of such CMOS imagers, especially for very low-light conditions, can be drastically improved so that they can reach the required low-noise level and high SNR [6.4] for radio-molecular imaging, as emphasized in Chapter 1.

Based on the proposed techniques, a prototype CMOS imager was designed and fabricated. More information about the chip as well as the noise characterization results are presented and discussed in following sections of this chapter.

6.2 Sensor Design Overview

A prototype test sensor was designed and fabricated in a 0.18μm 1P4M CIS process from TSMC. The specifications of the test sensor are summarized in Table 6-1. The sensor design is based on the test sensor presented in Chapter 5. The column-parallel circuit structure as shown in Figure 5-1 is used. It consists of column-parallel gain amplifiers offering

x1, x4 or x16 selectable analog gains by capacitive switching and single slope ADCs (SS-ADCs) for digital CMS mode configuration. All the pixels are pinned-photodiode 4T structures with 10µm pitch. In the pixel array, 60-column pixels are implemented with the conventional surface-channel source follower (SSF), and the 60-column pixels are implemented with BSF. The source follower transistor dimension for both the SSF and BSF pixels are the same, i.e. W/L= 0.42µm/0.5µm. A shift register structure is used for the row and column addressing circuitry.

Table 6-1. *The Prototype Test Chip Specifications Summary*

Specification	Value
Process	TSMC 0.18µm 1P4M CIS
Chip size	2.5mm (H) x 5mm (V)
Pixel type	4T APS with pinned-photodiode
Pixel size	10µm (H) x 10µm (V)
Number of effective pixels	128 (H) x 198(V)
Power supply	3.3V (A) / 1.8V (D)
Output	10/12 bit digital resolution
Column-parallel amplifier gain	x1, x4, x16
Digital CMS mode	1, 2, 4 (x4 ramp voltage gain available) 1, 2, 4, 8 (x4 ramp voltage gain not available)

Figure 6-1 shows the chip microphotograph. The phase-lock loop (PLL) and digital-to-analog converter (DAC) circuits needed to generate the ramp voltage were implemented externally. The sensor configuration timing is supplied by an external FPGA.

6.3 Measurement Results

The prototype CMOS image sensor was successfully designed and fabricated. The random noise measurement is thus the main focus for the chip characterization. In order to verify the lowest random noise level, all the noise measurements were done in the dark. During the measurements, the dark random noise was always measured at room temperature at 3 frames per second (fps). The system clock frequency to drive the sensor is 10MHz and a 120MHz clock was used to drive the column-parallel

SS-ADCs in 12bit mode. The pixel transfer gate was grounded to verify the results from the dark shot noise. All the pixels were biased with 12μA current. The random noise was calculated over 20 continuous frames.

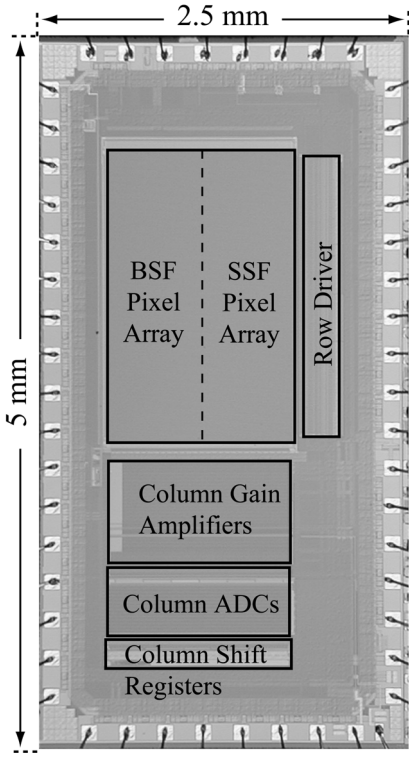

Figure 6-1: *Test chip microphotograph*

6.3.1 Random Noise vs. Analog Gain

Figure 6-2 shows the measurement results of the input-referred random noise as a function of the column-parallel amplifier gain. During the measurement, only digital CDS was implemented. The random noise was reduced to follow the tendency of *1/G* closely, where *G* is the closed-loop analog gain of the column amplifiers. As analyzed from Eq. (5-3) in Chapter 5, this tendency indicates that the dominant thermal noise is from the circuits and systems in the back-end of the column amplifiers.

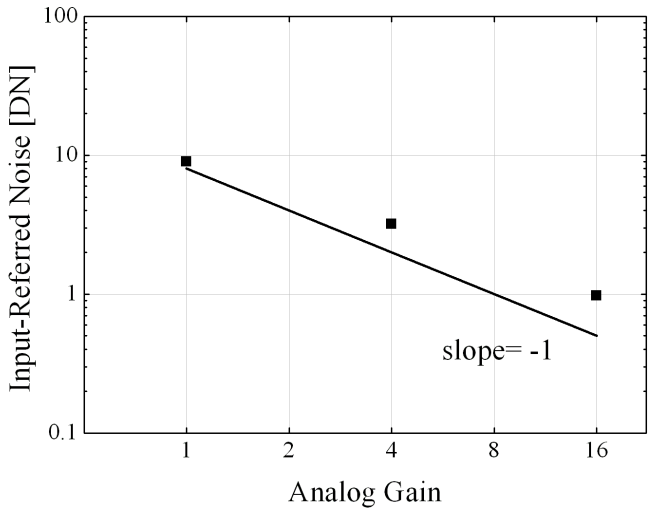

Figure 6-2: *Measured input-referred random noise as a function of the analog gain*

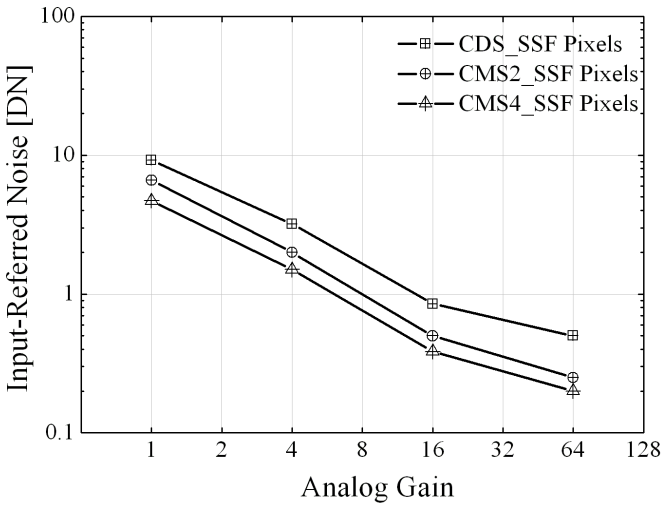

Figure 6-3: *Measured input-referred random noise of SSF pixels as a function of the analog gain*

6.3.2 Random Noise of SSF Pixels

Figure 6-3 shows the measured input-referred random noise, in which CMS2 and CMS4 signify the results after 2- and 4-times CMS, respectively. For the measurements, although the column-parallel amplifier only has a x1, x4 or x16 selectable gain, an additional gain could be supplied by lowering the range of the ADC ramp voltage [6.5]. Therefore, the analog gain of 64 shown in Figure 6-3 actually includes the x16 column-amplifier gain and x4 ramp voltage gain. Figure 6-3 shows the noise reduction tendency as the applied gain increases, but also the same tendency as the number of CMS sampling times increases. The measurement results show that with a conversion gain of 45μV/e^- and 244μV/DN, the lowest input-referred random noise of SSF pixels is about 1.1e^-.

6.3.3 Random Noise of BSF Pixels

Figure 6-4 shows the measured input-referred random noise and Figure 6-5 shows the input-referred random noise histogram of the BSF and SSF pixels, respectively. For the measurements, the reset voltage at the pixel floating diffusion (FD) node, V_{rt}, was set at 2.5V, and different gain configurations with 4-times CMS were implemented. The measurement results in Figure 6-4 show that while a x64 gain is applied, the random noise of the BSF pixels can be reduced down to 0.14DN - under a 2.5V reset voltage at the pixel FD node - which is about 0.76e^-. Furthermore, according to [6.2], lowering the reset voltage at the FD node can also help to improve the pixel random noise. Thus, as shown in Figure 6-4, the random noise achieves 0.13DN, which is 0.70e^- under the 1.6V reset voltage at the FD node. Also because of the use of the BSF, as previously reported in [6.2][6.3], the noise spread of the BSF pixels in the random noise histogram shown in Figure 6-5 is significantly improved. For the histogram shown in Figure 6-5, both the SSF and BSF pixels are under the 2.5V reset voltage at the FD node configuration. From the results shown in Figure 6-4, it also can be found that when a x64 gain and 4-times CMS are implemented, the noise reduction effect of the BSF pixels is also limited. The noise from the externally generated ramp voltage signal and the residual *1/f* noise source from the column readout circuits can be the remaining noise sources that cause this limitation.

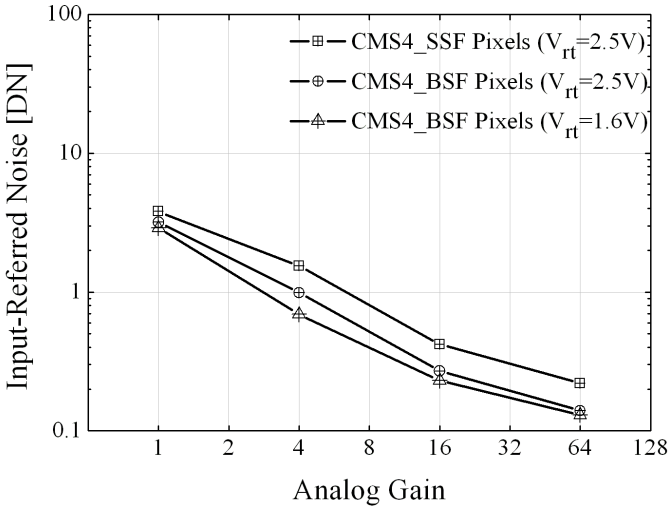

Figure 6-4: *Measured input-referred random noise of SSF and BSF pixels as a function of the analog gain*

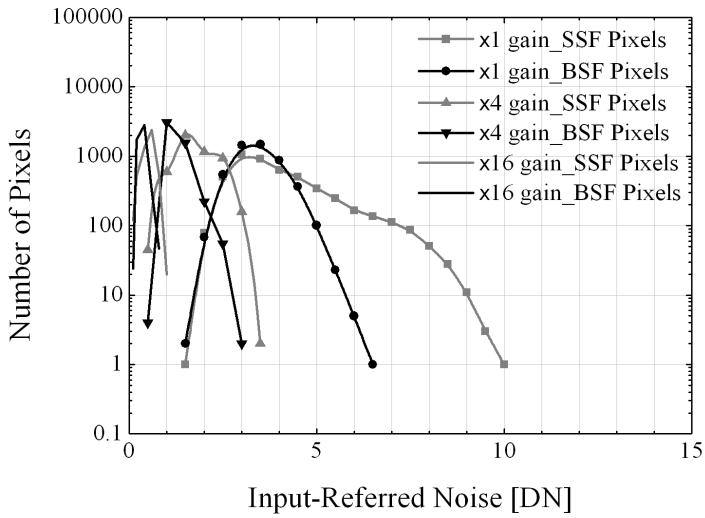

Figure 6-5: *Input-referred random noise histogram of SSF and BSF pixels with 4-times CMS and different gain settings*

As mentioned in Chapter 5, the low-frequency random noise of the pixel source follower, i.e. the *1/f* and RTS noise, limit the noise reduction effect as the number of correlated multiple sampling times increases [6.1]. Figure 6-6 shows a comparison of the CMS noise reduction effect for the SSF and BSF pixels, respectively. For this comparison, a x16 column amplifier gain was used to sufficiently suppress the thermal noise. As shown in Figure 6-6, compared to the BSF pixel, the SSF pixel shows a limited noise improvement from the 4-times CMS because of *1/f* and RTS noise from the in-pixel source follower. However, the buried-channel technique [6.2][6.3] prevents this limitation up to 8-times CMS in BSF pixels. Comparing the input-referred random noise with only-digital CDS (1-time CMS) shows that the noise reduction of CMS is about 36% for SSF pixels but about 55% for BSF pixels where 8-times CMS is applied. Because of the limited configurable range and slope of the ramp voltage, 8-times CMS is the maximum available value with a x16 amplifier gain.

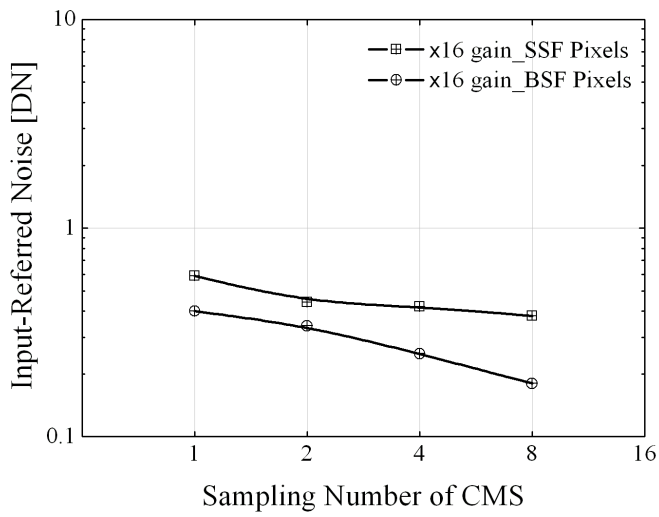

Figure 6-6: *Comparison of CMS noise reduction effect for SSF and BSF pixels*

Figure 6-7 shows the image lag measurements with different reset voltages at the pixel FD node, V_{rt}. For the measurements, the imager was at 3fps, the flash light duration was 0.1s, the charge transfer time was 0.1μs, and CDS with unit-gain was implemented. The results were based

on BSF pixels. Figure 6-7 shows that when V_{rt} was set at 2.5V, the saturation level-referred image lag is about 1%.

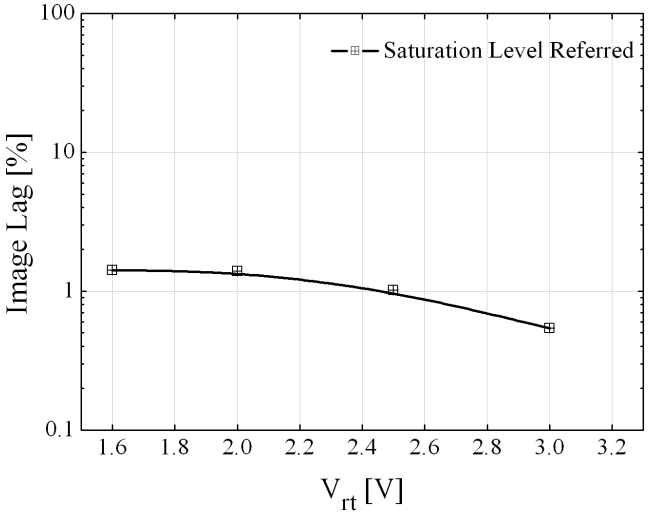

Figure 6-7: *Image lag measurements with different FD reset voltages*

Figure 6-8 shows the captured sample images from a prototype imager at a low-light illumination level. The images were captured in 3fps and 0.06Lux illuminations at room temperature. The F-number was F4.0, and a x16 column amplifier gain with 4-times CMS was configured. During the measurement, an infrared cutoff filter (CM500S) and a green optical filter (VG9) were placed in front of the lens. As shown in Figure 6-8, the prototype imager shows very good performance in low-light conditions, which makes its application for radio-molecular imaging promising.

(a) (b)

Figure 6-8: *Captured sample images from the prototype imager in 0.06 Lux illuminations: (a) raw image; (b) image after hot pixels removal*

Finally, the performance of the prototype CMOS imager is summarized in Table 6-2.

Table 6-2. *The Prototype Chip Performance Summary*

Specification	Value
Conversion Gain	45μV/e^-
Fill Factor	45%
Quantum Efficiency	56% @550nm[1]
Random Noise[2]	0.70e^-
Random Noise Improvement[3]	1/40 @V_{rt}=2.5V 1/44 @V_{rt}=1.6V
Dark Current	27pA/cm^2 @room temperature
Dark FPN	7%[4] @room temperature

[1]: the result without microlens; fill factor not included

[2]: measured with V_{rt}=1.6V and the pixel charge transfer gate grounded

[3]: compared with the conventional CIS without any noise suppression techniques

[4]: the result is the same for SSF and BSF pixels

6.4 Conclusions

A prototype imager for radio-molecular imaging was presented. The noise measurement results as well as the sampled images in very low-light conditions were also shown and discussed. By using the in-pixel BSF, column-parallel high gain amplifiers, and digital CMS technique, the prototype imager is able to achieve a random noise level as low as 0.70e^-. Compared to a conventional CIS without any noise suppression techniques, this work demonstrates a 40-times input-referred random noise reduction. However because of the implementation of the digital CMS technique, the frame rate is limited to 3fps for the measurement. This is a major drawback for the current design. To further improve the performance, there are several approaches to shorten the sampling period of the digital CMS so that the frame rate can be increased as well. More introduction and discussion regarding future improvement are given in Chapter 7.

6.5 Acknowledgement

The author would like to especially thank Dr. S. G. Wu's team at TSMC for their support in modifying the process flow.

6.6 References

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7 Conclusions and Future Work

In this thesis, new technology and designs to reduce the read noise floor of a CMOS image sensor have been presented. A new low-noise CMOS image sensor (CIS) that uses an in-pixel buried-channel source follower (BSF) and high-gain column-parallel amplifiers together with the digital correlated multiple sampling (CMS) technique was proposed. In this final chapter, the main findings of this thesis are summarized, and an overview of possible future work is discussed.

7.1 Main Findings

Regarding CMOS image sensors with an in-pixel BSF and optimized row selector

- The lattice defects at the Si-SiO_2 interface of the in-pixel source follower (SF) cause interface trap-induced pixel *1/f* and RTS noise. The use of the in-pixel BSF transistor moves the conducting channel away from the Si-SiO_2 interface. As the conducting carriers flow deeper and further away from the interface, the probability of the carriers getting trapped in the interface traps decreases. This helps in minimizing the in-pixel RTS noise.

- The buried-channel implantation decreases the threshold voltage of an nMOS transistors. This helps to increase the pixel output swing. However, this improvement is limited by the row select switch, which is normally realized by a standard nMOS transistor. One solution is to use optimized row select switches, i.e. the transmission gate switches.
- A newly designed CMOS image sensor using an in-pixel buried-channel source follower with an optimized row selector (RS) was presented. It achieved the same dark random noise performance as [7.1] - 250μV_{rms} - and moreover it is able to improve the trade-off between the noise reduction and the improvement in the pixel output swing.
- The pixel quantum efficiency (QE) decreases due to the optimized RS. The optimized RS contains an additional pMOS transistor inside of the pixel. Inside the pixel, the n-well of this pMOS transistor is always biased to a high voltage, i.e. the power supply. This makes it an additional photon-generated-electron sink during exposure, thus lowering the QE of the pinned-photodiode, especially for longer wavelengths of light. However, according to the measurement results shown in Figure 3-7 in Section 3.4, the QE for a 550-600nm wavelength, at which the pixels are most sensitive, only decreases by about 10% due to the optimized RS. This QE decrease does not have much negative impact on the SNR of BSF pixels, as the random noise improves over 50%. This causes the overall SNR to increase x1.8 times.

Regarding the noise reduction technique using CMS

- A CMS technique can reduce the read noise in the flat part of the spectrum (for example the thermal noise) by a factor of $\sqrt{m}$, where m is the number of CMS samples.
- Based on the SNR calculation and comparison, it can be shown that by using the CMS technique, the SNR of CISs can exceed that of EMCCDs for very low-light level imaging. As shown in Figure 4-2 in Section 4.1.2, compared to CISs without CMS implementing, with one single photon electron input, the SNR of CISs is increased by 14dB when 64-times CMS is implemented. With a 0.6 photon electrons input, the CIS implemented with 64-times CMS has a better SNR than an EMCCD.

- There are two main approaches to implement the CMS technique in CMOS imagers: using column-parallel analog integrators [7.2] or ADCs [7.3]. The effectiveness of noise reduction and the flexible sampling times setting are the advantages of using column-parallel analog integrators. However, for *m*-times CMS configuration, the maximum output voltage swing of the integrator limits its maximum input range to *1/m* of its initial full output swing, thus leading to a reduction in the pixel dynamic range. An improved design called the folding integration CMS (FI-CMS) technique [7.2] can solve this problem, but it needs extra circuits in the columns and it also introduces some extra digital coupling noise. Compared to using column-parallel analog integrators to implement a CMS, the biggest benefit of using column-parallel ADCs is the noise reduction in the pixel readout circuits without the need for any additional circuits, power consumption or silicon area. Moreover, the architectural simplicity of the circuits also makes it much easier to implement its design and to adapt it to other process technologies.
- Based on the transfer function analysis method, it is revealed that the digital CMS technique using column-parallel ADCs has noise reduction effects on *1/f* noise. Shortening the signal level sampling period would help to improve the *1/f* noise reduction effect by CMS.

Regarding the low-noise CMOS image sensor for radio-molecular imaging

- Due to the bandwidth limiting effect, the thermal noise from the pixel readout chain can be largely reduced by the column gain amplifier. As the column amplifier gain G is increased, the random noise firstly decreases by a factor of G, which indicates that the thermal noise from the circuits and system in the backend of the column amplifiers is dominant. Later the random noise decreases by a factor of $\sqrt{G}$, indicating that the thermal noise from the gain amplifier and the pixel source follower is dominant.
- The random noise can be efficiently reduced by using a high-gain column-parallel amplifier together with the digital CMS technique. When the random noise in flat spectrum is suppressed to a

certain level at which is no longer dominates the read noise floor, the *1/f* and RTS noise start to dominate the read noise floor. This phenomenon limits the noise reduction effect of the design.

- The use of an in-pixel BSF can drastically minimize the pixel RTS noise. Thus the proposed CMOS imager with all these techniques can provide a very low random noise level. A random noise of $0.70e^-$ random noise was measured from the phototype chip at 3 frames per second (fps) at room temperature. This work therefore demonstrates a 40-times input-referred random noise reduction, which corresponds to a 32dB SNR improvement for low-light level imaging.

A comparison of this work with state-of-the-art techniques is listed in Table 7-1. As is shown, compared to [7.1][7.4-7.8], this work achieves the lowest random noise level and the best noise reduction results. As mentioned in Chapter 1, compared to EMCCDs which can be used in the gamma-ray detectors for SPECT imaging [7.9], the low SNR in low-light conditions is the main barrier with using CMOS imagers for such detectors, in which the imager normally has to work with the illumination level of a single photon per pixel on average [7.10]. In other words, in order to adapt to SPECT imaging, the SNR of CMOS imagers needs to be at least better than the SNR of EMCCDs for single photon detection. Furthermore, the noise level of the CMOS imager needs to be less than $0.3e^-$/pixel/frame at room temperature [7.10].

Therefore, as this thesis draws to a close, the SNR of EMCCD and the proposed low-noise CMOS imager are calculated and compared again based on the Eq. (4-2) and Eq. (4-4), which are shown as follows:

$$SNR = 20\log\left(\frac{QE \cdot P}{\sqrt{n_{SN}^2 + n_{DN}^2 + n_{RN}^2}}\right)[dB] \tag{7-1}$$

$$SNR = 20\log\left(\frac{QE \cdot P}{\sqrt{F^2 \cdot (n_{SN}^2 + n_{DN}^2) + \frac{n_{RN}^2}{g^2}}}\right)[dB] \tag{7-2}$$

where QE is the quantum efficiency of the pixels, P is the number of input photons on the pixel area in electrons, n_{SN} is the photon shot noise, which equals $\sqrt{QE \cdot P}$, n_{DN} is the dark current shot noise, n_{RN} is the read noise, F is the excess noise factor contribution from the noise in the electron multiplication process [7.11], and g is the electron multiplication gain in EMCCDs.

Table 7-1. *Performance Comparison with State-of-the-Art*

Reference	Noise Reduction Technique	CG[1] [μV/e⁻]	Initial Random Noise [e⁻]	Final Random Noise [e⁻]
[7.1]	In-pixel BSF	73	6.8 (@gain x10)	3.4 (@BSF pixels with gain x10)
[7.4]	High-gain column amplifier and optimized STI process	75	4.6 (@gain x4)	3.5 (@gain x16)
[7.5]	Oversampling using ΔΣ ADC	80	3.5	1.9 (@130-times oversampling)
[7.6]	Pseudo-multiple sampling using SS-ADC	110	1.8	1.1 (@gain x16)
[7.7]	Pixel-level open-loop voltage amplifier	300	-	0.86 (@gain x10)
[7.8]	CMS using folding integration/cyclic ADC	67	13.9	1.2 (@64-times CMS)
This work	**In-pixel BSF, high-gain column amplifier and CMS using SS-ADC**	**45**	**30.9**	**0.7[2] (@BSF pixels with gain x64 & 4-times CMS)**

[1]: conversion gain

[2]: measured with 1.6V reset voltage and the pixel charge transfer gate grounded

Figure 7-1 and Figure 7-2 show the plot of the SNR comparison between the EMCCD and the proposed low-noise CMOS imager (CIS). For the plot, a number of assumptions are made. QE is assumed to be

70%, g is assumed to be 1000, and the read noise of CISs is 0.7e$^-$. F and the read noise of EMCCD are set at 1.41 [7.11] and 10e$^-$, respectively. For Figure 7-1, very low temperature is assumed so that dark current shot noise (n_{DN}) can be ignored, and for Figure 7-2, 1e$^-$ dark current shot noise is assumed for both EMCCD and CIS. It shows that since 0.7e$^-$ input photons, the proposed low-noise CIS has a better SNR than the EMCCD, if dark current shot noise is ignored. However, as shown in Figure 7-2, if the dark current shot noise is taken into account, the SNR of the CIS surpasses that of the EMCCD. This is because in the EMCCD the dark current is also amplified along with the signal in its electron multiplication stages. This dark current amplification in the EMCCD is higher compared to the dark current amplification in the CIS. Thus the CIS will exhibit a better SNR.

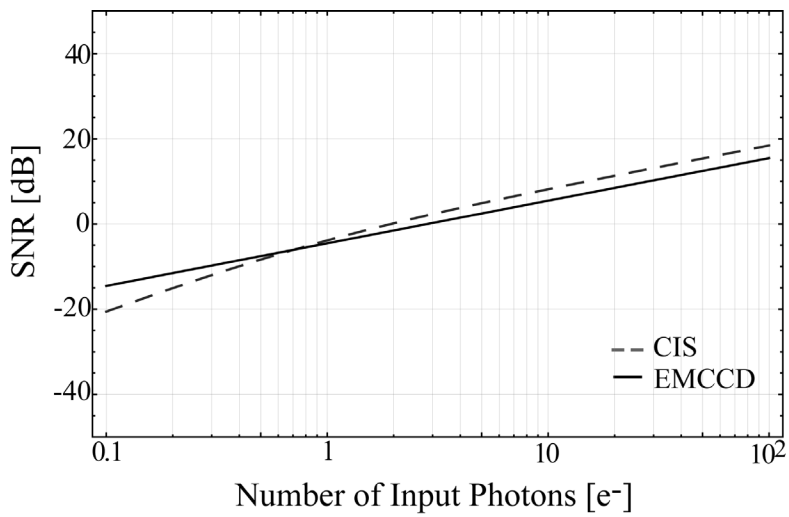

Figure 7-1: *SNR comparison between EMCCD and the low-noise CIS, with n_{DN} ignored*

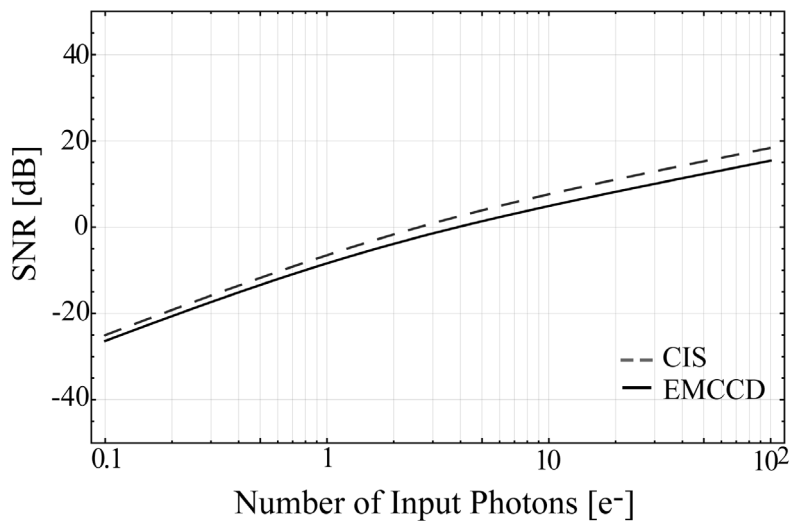

Figure 7-2: *SNR comparison between EMCCD and the low-noise CIS, with 1e⁻ n_{DN} assumed*

In conclusion, the proposed low-noise CMOS imager achieves a random noise level of 0.7e⁻ at 3fps and at room temperature. In fact, this random noise number is the averaged value of the measured random noise of pixels in the imager. Therefore, for each frame, the proposed CMOS imager reaches a random noise level of 0.7e⁻/pixel/frame. The EMCCDs used in the gamma-ray detectors in the studies of [7.9] is the CCD97 [7.12], which is a backside-illuminated EMCCD from E2V Technologies. According to the sensor datasheet [7.12], the input-referred readout noise of the CCD97 is 8e⁻/pixel/frame at a temperature of 293K with an EM gain of 1000. This readout noise level is much higher than that of the proposed low-noise CMOS imager. Therefore, with respect to the SNR and readout noise, the proposed low-noise CMOS imager is suitable for the new gamma-ray detector for SPECT imaging.

However, in this work, the dark current shot noise is not taken into account. At room temperature (300K), the dark current of the proposed CMOS image sensor is 27pA/cm^2, which is too high to reach the desired noise level of 0.3e⁻/pixel/frame for all the noise sources combined [7.10]. Furthermore, according to [7.10], the new gamma-ray detector requires the image sensor with higher frame rates of up to 50fps. These challenges

can be addressed in a future study in order to develop new gamma-ray detectors for SPECT imaging based on CMOS imagers.

7.2 Future Work

As presented in this thesis, the prototype low-noise CMOS imager has already shown very good random readout noise performance for low-light level imaging, such as SPECT imaging. However, there is still some work which can be done in the future to obtain an even lower noise level and better performance for SPECT imaging.

7.2.1 Further Investigation and Optimization on Pixels

To reach the total noise requirement for the gamma-ray detector for SPECT imaging, the pixel dark current must be reduced. This also significantly reduces the sensor's total read noise floor. Dark current is caused by process imperfections and leakage currents. Nowadays, the process imperfections are continuously being improved by increasingly better process control. The diffusion-based leakage current can be reduced by using holes instead of electrons, for example by operating the sensor in hole-accumulation mode [7.13] or using hole-based detectors [7.14].

To achieve a minimized random noise level, the pixel conversion gain (CG) should be further increased as much as possible. This can be done with two approaches:

- Decreasing the area of the floating diffusion (FD) node inside the pixels so that the FD node capacitance is decreased and the pixel CG is increased. However, by doing so, there is also a risk of a charge sharing problem if the capacitance of the FD node is reduced too much to make the resulting signal-level potential on the FD node higher than the pinned-photodiode (PPD) pinning potential. The optimized values for the FD node area can be investigated and designed by means of device simulation and calculation.
- Implementing an in-pixel open-loop amplifier, as illustrated in [7.7], so that the pixel CG can be effectively increased to more than 200μV/e^-. The column amplifier is then not necessary. However, for the conventional p-well based pixels, the use of pMOS transistors for the in-pixel amplifier hurt the pixel fill factor and the quantum efficiency. This problem can be avoided in the n-well

based pixels. In addition, the variation in the open-loop gain from pixel to pixel introduces additional pixel non-uniformity. This non-uniformity has to be corrected on a pixel-by-pixel basis.

The source follower in the BSF pixel was initially designed solely for the noise behavior investigation and comparison, but it was not optimized for noise performance. Generally, increasing the W/L ratio of the SF transistor helps to decrease the thermal noise of the SF. For example, if the W/L ratio is increased by 100%, the thermal noise of the SF can be reduced by 50%. However, if the W/L ratio of the SF transistor is increased, the pixel fill factor might be decreased. Therefore, the W/L ratio of the SF transistor can be increased while the pixel fill factor is being optimized.

7.2.2 Further Optimization on the Column-Parallel Amplifiers

From the simulation results, the column-parallel amplifier had a $129\mu V_{rms}$ closed-loop noise. However, this noise value is about $480\mu V_{rms}$ from the measurement results. The column-parallel amplifier used in the prototype sensor is actually an nMOS transistor-based folded-cascode amplifier. The column-parallel amplifier can obtain a lower noise level by using a pMOS transistor-based structure so that the sensor noise level can be further reduced as well. Yet by doing so, the design has to be properly adjusted to keep enough open-loop gain and output swing, for instance >80dB and >1V.

7.2.3 Further Optimization on the Column-Parallel ADCs

In the current design, the ramp voltage and the counter clocks are generated externally, which brings some additional noise and limits the speed of the ADC. As the results shown in Figure 6-4, the noise from the ramp voltage signal limits the noise reduction effect on the BSF pixels as a x64 gain and 4-times CMS are implemented. The relatively long sampling period for the digital CMS configuration limits the frame rate of the imager, which is a drawback of the current design. There are several approaches for future improvement:

- First of all, the most straightforward approach is to implement the on-chip digital-to-analog convertor (DAC), phase-lock loop (PLL) cells. By doing so, not only can the noise performance be improved but also can the sampling period for the digital CMS be

shortened. This will consequently help to achieve higher frame rates and noise improvements. For instance, if the clock frequency can be doubled, the signal level sampling period can be reduced by 50%, which means the *x*-factor introduced in Section 4.3.2 is reduced by 50%. Then according to the calculation shown in Figure 4-6, for 4-times CMS, the normalized *1/f* noise power can be improved by at least 12.5%.

- Another approach is to introduce an additional low-light-level-imaging mode to the ramp voltage (V_{ramp}), in which a reduced V_{ramp} voltage range is used. Because the pixel signal does not actually reach the full 12bit resolution in low-light conditions, the full range of V_{ramp} is not necessary. If 50% of the full range of V_{ramp} is used, then for 4-times CMS, the sampling period is reduced by 50%, or with the same sampling period, 8-times CMS can now be configured.
- A more advanced approach is to implement the digital CMS with the multiple ramp single-slope (MRSS) ADC architecture [7.15]. The MRSS-ADC converts the signal into a coarse phase and a fine phase; the CMS can be implemented in the fine phase. Firstly, the coarse analog-to-digital (A/D) conversion is performed by a coarse V_{ramp}, and the result of the coarse conversion is stored in the memory and subsequently used to choose the correct fine sub-ramps and in which range the input signal is. Next, the fine A/D conversion is performed with the fine sub-ramps corresponding to the input signal. The correct fine sub-ramp then does *m*-times up- and down-ramping for CMS implementation. The final digital output is a combination of the coarse and averaged fine conversion results. If *j* sub-ramps are used, because the sub-ramps only have to span *1/j* times the full range of V_{ramp}, the sampling time can be much faster. For example, if j=8 [7.15], for 4-times CMS with 12bit resolution, theoretically the sampling time can be reduced to about 1/8.
- To increase the SS-ADC conversion speed, the DLL-based SS-ADC can be implemented [7.16]. During the digital CMS configuration, as in the MRSS ADC concept, the conversion is divided into two modes: the coarse conversion and fine conversion. The coarse conversion and the fine conversion are processed concurrently during the CMS conversion. Within each column, the ripple counter is implemented to obtain the averaged coarse bits

after CMS. The delay lines from the DLL cell are distributed over the columns to obtain the averaged fine bits after CMS. The final output is a summation of the averaged coarse and fine codes.

In conclusion, with further optimizations, the starting point of random noise level can be reduced while the frame rate can be increased; thus, after the high gain and digital CMS configuration, a much lower random noise can be expected. For instance, if the initial random noise level can be reduced by 50%, following the same noise reduction tendency, eventually a random noise level well below $0.5e^-$ can be expected and achievable.

7.3 References

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Summary

This thesis presents the development of low-noise CMOS image sensors for radio-molecular imaging. The development is described in two directions: firstly, from the technology point of view to reduce the pixel noise level, and secondly from the design point of view to reduce the pixel readout circuits noise level.

Chapter 1 provides an introduction to the background and the motivation of this thesis. It starts with a brief introduction to the medical imaging technique. Medical imaging techniques can be roughly divided into two categories: anatomical and molecular imaging. Nowadays, molecular imaging is widely used not only for diagnosis of metabolic diseases and lesions on the cellular level, but also for building brain-computer interfaces. In particular, the imaging of molecules in patients and experimental animals is of strategic importance to biomedicine. Compared to other molecular imaging technologies, such as MRI which uses targeted activatable contrast agents and PET, Single-Photon Emission Computed Tomography (SPECT) is among the most sensitive of the molecular *in vivo* imaging technologies with its spatial scale covering the resolution required for imaging small laboratory animals and humans. Small-animal SPECT is a key tool used to study and understand human models of diseases. For small-animal SPECT, pinhole imaging has the most appeal because of the relatively small fields-of-view, which allow large numbers of pinholes to be placed close to the object. Pinhole imaging in small animals can lead to ultra-high resolutions, as has been demonstrated with the U-SPECT-I [1.19] and U-SPECT-II [1.20] systems. These U-SPECT systems developed at the University Medical Center in Utrecht, the Netherlands are capable of sub-half-mm resolution imaging despite the use of large clinical detectors that have a relatively low intrinsic spatial resolution of approximately 3.5mm.

A high intrinsic detector resolution combined with energy discrimination capabilities is essential for the improvement of future (pinhole) SPECT systems. One of the novel ways to obtain a very high spatial resolution (<100μm) with a gamma-ray detector is to use a scintillation layer composed of a bundle of parallel micro-columnar crystals, which is read out by a CCD suitable for operating at high frame rates. In most CCDs, readout noise becomes a serious problem at high frame rates. This degrades the SNR of the CCDs and thus also the performance of the gamma-ray detector for such application. To overcome this adverse effect, electron-multiplying CCDs (EMCCDs) are used, which allow a compact photon-counting CCD-based gamma camera to be constructed that in some cases resulted in spatial resolutions of about 60μm. However, the EMCCD-based gamma-ray detectors have several specific limitations. Therefore, developing a new type of CMOS image sensor with a better performance and an adaptive noise level required for radio-molecular imaging ($0.3e^-$/pixel/frame), but without the disadvantages of EMCCDs, becomes very challenging. This leads to the motivation of this thesis.

Chapter 2 gives an overview of the concepts and the performance of CMOS image sensors. The purpose is to briefly introduce the background of CMOS imagers. The chapter starts with the explanation of some crucial characteristics used to evaluate the performance of CMOS image sensors, such as the signal-to-noise ratio (SNR), quantum efficiency, dynamic range, and pixel conversion gain. A brief overview of spatial noise sources and temporal (random) noise sources in CMOS image sensors is also summarized in this chapter.

Chapter 3 presents a technological approach to reduce the pixel random noise level. As CMOS processes scale down, the gate area of the transistors becomes so small that it can easily only have one active interface trap underneath the transistor's gate, which will induce the quantization of the *1/f* noise, which is the RTS noise. Because of this single electron trapping and de-trapping during transistor operation, the RTS appears in pixels, which have only one active interface defect, and dominates the pixel temporal noise. As long as a perfectly clean gate interface cannot be guaranteed, the *1/f* or RTS noise will remain one of the dominant random noise sources in pixels and limit the performance of the pixels for low-light level imaging such as radio-molecular imaging. In this

chapter, a buried-channel source follower (BSF) is illustrated and evaluated as a replacement for the standard surface-mode source follower as the in-pixel amplifier. The buried channel requires only one extra implantation, which pushes the highest potential in the channel away from the Si-SiO_2 interface. Thus, the possibility of carriers being trapped by lattice defects can be minimized and the *1/f* and RTS noise can be reduced.

However, because of the buried-channel implantation, the threshold voltage of the nMOS transistor is shifted towards a negative value. This causes the pixel row select switch to work improperly while reading out the pixel reset level voltage. Therefore, a test sensor using BSF pixels with optimized row selectors is introduced in Section 3.3. The measurement results show that compared to a conventional surface-mode source follower design, the BSF can achieve a reduction of more than 50% in dark random noise, an improvement in the noise spread, and a significant reduction in the *1/f* and RTS noise component, with a cost of quantum efficiency attenuation. However, thanks to the noise reduction capability of the BSF technique, this penalty on QE will not hurt the SNR of the BSF pixels. After this chapter, the focus of this thesis is shifted from the technology point of view to design.

Chapter 4 introduces and discusses an effective noise reduction technique, i.e. the correlated multiple sampling (CMS) technique in CMOS image sensors. For CMOS image sensors, correlated double sampling (CDS) is an indispensable noise reduction technique, because it can effectively cancel reset noise and pixel output offset. However, for low-light level imaging, an extremely low noise floor is a must-have property for the CMOS imagers, and CDS is not sufficient enough to achieve such a requirement. Therefore a more advanced noise reduction technique, i.e. correlated multiple sampling (CMS), is developed and used in the column-parallel noise reduction circuits for low-noise CMOS imagers. The concept of CMS for a 4-transistor (4T) pixel structure is quite straightforward. The reset level of the pixels is firstly sampled m-times, and then after the charge transfer, the signal level is also sampled m-times. In the end, the m-times sampling sum of the reset and signal levels are subtracted from each other and then averaged. This approach can effectively reduce the readout noise in a flat spectrum, e.g. thermal noise, by a factor of $\sqrt{m}$, where m is the number of sampling times of CMS. From the SNR calculation and a comparison between EMCCDs and

CMOS image sensors, it is also concluded that the use of the CMS technique will indeed have a very positive impact on the SNR of CMOS image sensors for low-light level imaging: a well-improved SNR which is better than that of EMCCDs for low-light imaging.

In general, there are two main approaches to implement the CMS technique in CMOS imagers: using column-parallel analog integrators or column-parallel ADCs. Section 4.2 discusses and compares these two approaches. Compared to using column-parallel analog integrators for CMS, the biggest benefit of using column-parallel ADCs is the noise reduction of the pixel readout circuits without any additional circuits, power consumption or column areas. The hardware complexity of the ADCs is independent from the exact sampling times of CMS that only a change in the clocking pattern determines, which makes the ADC easy to reconfigure. The transfer function-based analysis also reveals that for effective noise reduction with CMS using column-parallel ADCs, each sampling period for the signal level sampling should be minimized.

Chapter 5 presents a low-noise CMOS image sensor which uses column-parallel high-gain signal readout and digital correlated multiple sampling (CMS). The sensor used is a conventional 4T active pixel with a pinned-photodiode as the detector. The test sensor was fabricated in a 0.18μm CMOS image sensor process from TSMC. The input-referred random noise from the pixel readout chain is reduced in two stages, first using a high gain column-parallel amplifier and second by using the digital CMS technique. The noise analysis based on the proposed circuits shows a reduction in the input-referred thermal noise of the column-parallel amplifier and the pixel source follower by a factor of $\sqrt{G}$, where G is the closed-loop gain of the column amplifier. The other thermal noise from the backend of the column-parallel amplifier is reduced by a factor of G. With CMS and the averaging process, the overall thermal noise is further reduced by $\sqrt{m}$, where m is the number of sampling times of the CMS. The dark random noise measurement results show that the proposed column-parallel circuits with a digital CMS technique is able to achieve $127\mu V_{rms}$ input-referred noise. The significant reduction in the sensor readout noise enhances the SNR of the sensor by 10.4dB.

Chapter 6 presents the realization of a low-noise CMOS imager using the buried-channel source follower, column-parallel high-gain signal readout, and digital CMS. The pixel random noise can be efficiently reduced by using a high gain column parallel amplifier together with the digital correlated multiple sampling technique, but the pixel *1/f* and RTS noise limit the noise reduction effect. On the other hand, the use of an in-pixel buried-channel source follower can drastically minimize the pixel *1/f* and RTS noise. Therefore, the proposed CMOS imager can provide a very low random noise. The prototype sensor was fabricated in TSMC's 0.18μm CIS technology. Standard 4T pixels with a pinned-photodiode are used and both SSF and BSF pixels are implemented in the pixel array of 128 (H) x 198 (V) with 10μm pixel pitch. The column readout circuits consist of the column-parallel gain amplifiers with x1, x4 or x16 variable analog gains and SS-ADCs for digital CMS implementing. The noise measurement results show that the prototype imager is able to reach a random noise level as low as $0.70e^-$ in 3fps at room temperature and with the pixel transfer gate grounded. Compared to a conventional CMOS image sensor without any noise suppression techniques, this work also demonstrates a 40-fold reduction in input-referred random noise, which corresponds to a 32dB SNR improvement. As emphasized in Chapter 1, such an improvement in SNR is very attractive for low-light level imaging, such as radio-molecular imaging, for which a high SNR is always required. In conclusion, with respect to the SNR and readout noise, the low-noise CMOS imager proposed in this thesis shows a promising performance for the new gamma-ray detector for SPECT imaging.

Samenvatting

Dit proefschrift presenteert de ontwikkeling van een ruisarme CMOS beeldsensor voor radiomoleculaire imaging. De ontwikkeling is beschreven vanuit twee invalshoeken: ten eerste, vanuit het technologische oogpunt om het pixel ruisniveau te verminderen, en anderzijds vanuit het oogpunt van het ontwerp om het circuit ruisniveau van de pixel uitlezing te beperken.

Hoofdstuk 1 geeft een inleiding met achtergrond en de motivatie van dit proefschrift. Het begint met een korte inleiding tot de medische imaging techniek. Medische imaging technieken kunnen grofweg worden onderverdeeld in twee categorieën: anatomische en moleculaire imaging. Tegenwoordig wordt moleculaire imaging veel gebruikt, niet alleen voor de diagnose van metabole ziekten en letsels op cellulair niveau, maar ook voor het bouwen van brein-computer interfaces. Voornamelijk de imaging van moleculen in patiënten en proefdieren is van strategisch belang voor de biogeneeskunde. In vergelijking met andere moleculaire imaging-technologieën, zoals MRI, die gebruikt activeerbare contrastmiddelen en PET, Single-Photon Emission Computer Tomografie (SPECT) is één van de gevoeligste van de moleculaire *in vivo* imaging-technologieën met een ruimtelijke omvang voor de resolutie nodig voor de imaging van kleine proefdieren en mensen. Kleine-dieren SPECT is een belangrijk instrument dat gebruikt wordt om menselijke modellen van ziekten te bestuderen en te begrijpen. Voor kleine-dieren SPECT, pin-hole imaging krijgt de meeste aandacht vanwege de relatief kleine gezichtsvelden, die het mogelijk maken om grote aantallen gaatjes te laten plaatsen dichtbij het object. Pin-hole imaging in kleine dieren kan leiden tot ultra-hoge resoluties, zoals aangetoond is door de U-SPECT-I [1.19] en U-SPECT-II [1.20] systemen. Deze U-SPECT systemen die ontwikkeld zijn aan het Universitair Medisch Centrum in Utrecht,

Nederland zijn geschikt voor sub-half-mm resolutie imaging ondanks het gebruik van grote klinische detectoren die een relatief lage intrinsieke ruimtelijke resolutie hebben van ongeveer 3.5mm.

Een hoge intrinsieke detector resolutie in combinatie met energie-discriminatie mogelijkheden is essentieel voor de verbetering van de toekomstige (pin-hole) SPECT-systemen. Een van de nieuwe manieren om een zeer hoge ruimtelijke resolutie (<100μm) te verkrijgen met een gamma-ray detector is gebruik te maken van een scintillatie laag die bestaat uit een bundel van parallelle micro-zuilvormige kristallen, die wordt uitgelezen door een CCD die geschikt is voor het functioneren op hoge frame snelheden. In de meeste CCD's, wordt de ruis uitlezing een ernstig probleem bij hoge frame snelheden. Dit degradeert de SNR van de CCD's en dus ook de prestaties van de gamma-ray detector voor deze toepassing. Om dit negatieve effect te overwinnen, worden elektronvermenigvuldigende CCD's (EMCCD's) gebruikt, die het mogelijk maken om een compacte foton-tellende CCD-gebaseerde gammacamera te bouwen dat in sommige gevallen leidde tot ruimtelijke resolutie van ongeveer 60μm. De op EMCCD gebaseerde gamma-ray detectoren hebben echter een aantal specifieke beperkingen. Het ontwikkelen van een nieuw type CMOS-beeldsensor met een betere prestatie en het adaptieve ruisniveau vereist voor radio-moleculaire imaging ($0.3e^-$/pixel/frame), maar zonder de nadelen van EMCCD's, wordt daarom zeer uitdagend. Dit leidt tot de motivatie van dit proefschrift.

Hoofdstuk 2 geeft een overzicht van concepten en de prestaties van de CMOS-beeldsensoren. Het doel is om een korte inleiding te geven van de achtergrond van CMOS-beeldsensoren. Het hoofdstuk begint met een uitleg van een aantal cruciale kenmerken die gebruikt worden om de prestaties van CMOS-beeldsensoren, zoals de signaal-ruisverhouding (SNR), kwantum efficiëntie (QE), dynamisch bereik, en pixel-conversie gain te evalueren. Een kort overzicht van de ruimtelijke ruisbronnen (FPN) en temporele (willekeurige) ruisbronnen in CMOS-beeldsensoren is ook samengevat in dit hoofdstuk.

Hoofdstuk 3 presenteert een technologische aanpak om het niveau van willekeurige pixel ruis te verminderen. Naarmate de CMOS-processen naar beneden schalen, wordt het gate-gebied van de transistoren zo klein dat het gemakkelijk slechts één actieve interface trap kan hebben onder de

transistor gate, die de quantisatie van de *1/f* ruis opwerkt, die gelijk is aan het RTS-ruis. Door een enkel elektron te vangen en los te laten tijdens de transistor operatie, verschijnt de RTS in pixels, die slechts één actieve interface defect hebben, waardoor de RTS de temporele pixel ruis domineert. Zolang een perfect schone gate-interface niet kan worden gegarandeerd, zal de *1/f* of RTS ruis één van de dominante willekeurige ruisbronnen blijven in de pixels en de prestatie van de pixels voor imaging bij lage lichtintensiteit beperken, zoals radiomoleculaire imaging. In dit hoofdstuk wordt een begraven-kanaal bronvolger (BSF) geïllustreerd en geëvalueerd als een vervanging voor de standaard oppervlak-mode bronvolger als de in-pixel versterker. De begraven-kanaal vergt slechts één extra implantatie, die de hoogste potentiaal in het kanaal duwt weg van de Si-SiO_2 interface. Zo kan de mogelijkheid worden verminderd van het vast komen te zitten van ladingen door roosterdefecten en de *1/f* en RTS ruis kan worden gereduceerd.

Echter, vanwege de begraven-kanaal implantatie, is de drempel spanning van de nMOS transistor verschoven naar een negatieve waarde. Dit zorgt ervoor dat de pixel-rij keuzeschakelaar niet goed werkt tijdens het uitlezen van het pixel reset niveau voltage. Daarom is een test sensor met BSF pixels met geoptimaliseerde rij kiezers geïntroduceerd in paragraaf 3.3. De meetresultaten tonen aan dat in vergelijking met een conventionele oppervlak-mode bronvolger ontwerp, de BSF het kan volgende bereiken: een vermindering van meer dan 50% van ruis in donker, een verbetering van de ruisspreiding, en een significante vermindering van de *1/f* en RTS ruiscomponent, met een kostprijs van kwantum efficiëntie demping. Maar dankzij de ruisonderdrukkingsvermogen van de BSF techniek, zal deze boete op de QE niet schadelijk zijn voor de SNR van de BSF pixels. Na dit hoofdstuk wordt de focus van dit proefschrift verschoven van het technologie oogpunt naar het ontwerp.

Hoofdstuk 4 introduceert en bespreekt een effectieve ruisonderdrukkingstechniek, d.w.z. de gecorreleerde multi-sampling (CMS) techniek in CMOS-beeldsensoren. Voor de CMOS-beeldsensoren, gecorreleerde dubbele sampling (CDS) is een onmisbare ruisonderdrukkingstechniek, want het kan effectief reset-ruis en pixel-offset verschuiving verminderen. Voor imaging bij lage lichtintensiteit is echter een extreem lage ruisondergrens een vereiste

eigenschap voor de CMOS-beeldsensoren, en CDS is niet voldoende om een dergelijke eis te bereiken. Daarom wordt een meer geavanceerde ruisonderdrukkingstechnieken, d.w.z. gecorreleerd multi-sampling (CMS), ontwikkeld en gebruikt in de kolom-parallelle ruisonderdrukkingscircuits voor ruisarme CMOS-beeldsensoren. Het concept van CMS voor een 4-transistor (4T) pixel structuur is vrij eenvoudig. Het reset niveau van de pixels wordt eerst m-maal bemonsterd, en dan na de ladingoverdracht, wordt het signaal niveau ook m-maal bemonsterd. Aan het einde worden de m-maal bemonsterd som van de reset en signaal niveaus van elkaar afgetrokken en dan gemiddeld. Deze aanpak kan de uitlezingruis effectief verminderen in een vlak spectrum, b.v. thermische ruis, met een factor van $\sqrt{m}$, waarbij m het aantal monsternames is van CMS. Van de SNR berekening en een vergelijking tussen EMCCD's en CMOS-beeldsensoren, wordt ook geconcludeerd dat het gebruik van de CMS-techniek inderdaad een zeer positief effect heeft op de signaal-ruisverhouding van CMOS-beeldsensoren imaging bij lage lichtintensiteit: een sterk verbeterde SNR, die beter is dan die van EMCCD's voor imaging bij lage lichtintentisteit.

In het algemeen, zijn er twee belangrijke benaderingen om de CMS-techniek te implementeren in CMOS-beeldsensoren: met behulp van kolom-parallelle analoge integrators of kolom-parallelle ADC's. Paragraaf 4.2 bespreekt en vergelijkt deze twee benaderingen. In vergelijking met kolom-parallelle analoge integrators voor CMS is het grootste voordeel van kolom-parallel ADC's de ruisreductie van de pixeluitlezingcircuits zonder extra circuits, energieverbruik of silicium oppervlakte. De hardware complexiteit van de ADC's is onafhankelijk van het exacte aantal bemonsteringen van CMS dat alleen door een verandering in het klokken patroon bepaald wordt, waardoor het gemakkelijk wordt om de ADC opnieuw te configureren. De transfer functie-gebaseerde analyse toont ook aan dat voor een effectieve ruisonderdrukking met CMS met behulp van kolom-parallel ADC's, elk bemonsteringsperiode voor het signaal niveau van bemonstering moet worden geminimaliseerd.

Hoofdstuk 5 presenteert een ruisarme CMOS beeldsensor die gebruikt maakt van kolom-parallel high-gain signaal uitlezing en digitale gecorreleerd multi-ampling (CMS). De gebruikte sensor is een conventionele 4T actieve pixel met een pinned-fotodiode als de detector.

De test sensor werd gefabriceerd in een 0.18µm CMOS-beeldsensor proces van TSMC. De input-gerelateerde ruis van de pixel uitlezingsketen wordt verlaagd in twee fasen: eerst met behulp van een high gain kolom-parallelle versterker en ten tweede door de digitale CMS techniek. De ruisanalyse op basis van de voorgestelde circuits toont een vermindering van de input-gerelateerde thermische ruis van de kolom-parallelle versterker en de pixel bron volger met een factor van $\sqrt{G}$, waarbij *G* de closed-loop versterking is van de kolom versterker. De andere thermische ruis geïntroduceerd na de kolom-parallelle versterker wordt verminderd met een factor van *G*. Met CMS, wordt de totale thermische ruis verder verminderd door $\sqrt{m}$, waarbij *m* het aantal monsternames is van de CMS. De meetresultaten van de ruis in donker tonen aan dat de voorgestelde kolom-parallelle circuits met een digitale CMS-techniek in staat zijn om 127µV_{rms} input-gerelateerde ruis te verkrijgen. De aanzienlijke vermindering van de sensor uitlezingruis verbetert de SNR van de sensor met 10.4dB.

Hoofdstuk 6 presenteert de realisatie van een ruisarme CMOS beeldsensor met behulp van de begraven-kanaal bronvolger, kolom-parallelle high-gain signaal uitlezing, en digitale CMS. De pixel ruis kan efficiënt worden verminderd door het gebruik van een high-gain kolom-parallelle versterker samen met de digitale gecorreleerde multi-sampling (CMS) techniek, maar de pixel *1/f* en RTS ruis beperken het effect op ruisvermindering. Aan de andere kant, kan het gebruik van een in-pixel begraven-kanaal bronvolger de pixel *1/f* en RTS ruis drastisch minimaliseren. Daarom kan de voorgestelde CMOS beeldsensor zorgen voor een zeer lage ruis. De prototype sensor is gefabriceerd in de 0.18µm CIS-technologie van TSMC. Standaard 4T pixels met een pinned-fotodiode worden gebruikt en zowel SSF als BSF pixels worden uitgevoerd in de pixel array van 128 (H) x 198 (V) met 10µm pixel steek. De kolom uitlezing circuits bestaan uit de kolom-parallelle gain versterkers met x1, x4 or x16 variabele analoge gains en SS-ADC's voor de digitale CMS implementatie. De ruis meetresultaten tonen aan dat het prototype imager in staat is om een ruisniveau te bereiken zo laag als 0.70e^- bij 3fps op kamertemperatuur met de pixel transfer gate geaard. In vergelijking met een conventionele CMOS-beeldsensor zonder ruisonderdrukking technieken, toont dit werk ook een 40-voudige reductie aan van de input-gerelateerde ruis, wat overeenkomt met een 32dB SNR verbetering. Zoals wordt benadrukt in hoofdstuk 1, deze verbetering van

de SNR is zeer aantrekkelijk voor imaging bij lage lichtintensiteit, zoals radio-moleculaire imaging, waarvoor een hoge SNR altijd vereist is. Tot slot, met betrekking tot de SNR en de uitlees ruis, de ruissarme CMOS imager voorgesteld in dit proefschrift laat een veelbelovende prestatie zien voor de nieuwe gamma-ray detector voor SPECT-imaging.

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In August 2007, when I started to work towards my Ph.D. degree, the project just seemed to be a mission-impossible for a student who had no clue about CMOS image sensors or even circuit design. Now, all of my four-year effort has finally resulted in this thesis. However, this never would have happened without the support and help of my supervisor, colleagues and friends, who I would like to acknowledge here.

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Yue Chen

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List of Publications

Journal Papers

Y. Chen, X. Wang, A. J. Mierop and A. J. P. Theuwissen, "A CMOS Image Sensor with In-Pixel Buried-Channel Source Follower and Optimized Row Selector", in *IEEE Transactions on Electron Devices*, vol.56, no.11, pp.2390-2397, Nov. 2009

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Y. Chen, Y. Xu, Y. Chae, A. J. Mierop, X. Wang and A. J. P. Theuwissen, "A $0.7e^{-}_{rms}$-Temporal-Readout-Noise CMOS Image Sensor for Low-Light-Level Imaging", to be submitted to *IEEE Journal of Solid-State Circuits* (in preparation)

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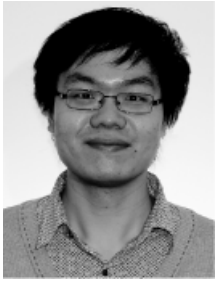
About the Author



Yue CHEN was born in Zibo, Shandong province, China, and had been living in Huaiyin (now called Huai'an), Jiangsu province, China since he was 8 years old. He received his the B.Sc. degree in Physics from Nanjing University (NJU), Nanjing, China in June 2004. The title of his B.Sc. thesis was "Physical Property Analysis for Zn-Co-O and Zn-Fe-O Powders Prepared by Sol-Gel Method".

In September 2005, thanks to the Philips Semiconductor Scholarship and Top Talent Loan sponsoring, he began his Electrical Engineering studies at Delft University of Technology (TU Delft), Delft, the Netherlands, where he received his M.Sc. degree in August 2007. The title of his M.Sc. thesis was "A Novel SiC/Polymer Based Bio-Inspired Surface-Micromachining MEMS Vibratory Gyroscope". Since August 2007, he has worked towards his Ph.D. degree at the Electronic Instrumentation Laboratory (EI Lab), TU Delft, with prof. dr. ir. Albert J. P. Theuwissen. The subject of his research was low-noise CMOS image sensors for radio-molecular imaging, which resulted in this thesis.

From June 2004 to June 2005, he did a research assistantship at NJU, where he worked on the research of diluted magnetic semiconductor materials. From March to September 2006, he completed a research project on theoretical modeling for a biomimetic strain-sensing Membrane-in-Recess microstructure at the EI Lab, TU Delft. In his spare time, he once acted as the treasurer of Promood (the independent representative body of Ph.D. candidates at TU Delft), the vice president of the Delft branch of Association of Chinese Students and Scholars in Netherlands (ACSSNL), and is the vice president of the 13th general board of ACSSNL.

為天地立心
為生民立命
為往聖繼絕學
為萬世開太平

宋　張載

To ordain conscience for the universe.
To secure life and fortune for the people.
To continue lost teachings for past sages.
To establish peace and prosperity for all future generations.

Zai ZHANG
(A.D. 1020-1077 in Song Dynasty)