Wideband High Power Doherty Amplifiers

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Abstract

Currently the Doherty Power Amplifier (DPA) is replacing the traditional Class B amplifier in base-station and broadcast applications, as such becoming the preferred choice of industry due to its simplicity and high efficiency performance. In spite of its success, so far practical DPA implementations can provide only a very limited RF bandwidth, which tends to narrow down even more at higher power levels. This narrowband behavior of the DPA is mostly caused by the use of traditional operating classes for the active devices and bandwidth restrictions related to use of a conventional impedance inverter.

In this work, the bandwidth of different DPA topologies has been analyzed, followed by a discussion of recent techniques that can help to improve the DPA bandwidth. To overcome the remaining bandwidth limitations in a DPA design, a novel differential configuration was proposed. In this approach, transmission line based baluns are used to implement the desired wideband 2nd harmonic terminations of the active devices. By combining this technique with a novel wideband impedance inverter, excellent DPA wideband performance can be achieved. Unfortunately, when going to practical balun implementations, various imperfections come to light, which trouble the achievable DPA bandwidth performance. For this reason, three practical balun structures are investigated in detail, namely, the coaxial cable based balun, the vertically installed planar balun and suspended planar stripline balun. To explore the proposed DPA concept when using practical baluns, two DPAs featuring mixed-signal driven inputs are presented. A dedicated design procedure for these DPAs is also given. The first prototype is implemented using NXP GaN devices and coaxial cable based baluns. Simulation results show a maximum output power of 52dBm, but in 6dB power back-off we only reach 40% efficiency from 530MHz to 700MHz, which is significantly less than the intend bandwidth (450MHz-810MHz). Using the lessons learned of this first amplifier, a second design with NXP LDMOS devices and suspended planar stripline balun has been developed. According to simulation this later design provides a maximum output power of 59dBm with the efficiency above 55% at both full power and 6dB power back-off. According the simulations this second design can even achieve 50% efficiency at 8dB back-off. The related center frequency is 650MHz with a high-efficiency bandwidth at 6dB power back-off (efficiency within 10% of its maximum) from 460MHz to 790MHz.
Acknowledgement

This project is a summary of my work in the past year. It is challenging but very interesting. I have not only gained a lot of professional knowledge but also learnt how to overcome the challenges. It is no doubt that this would not have been possible without the support of numerous people.

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Introduction

1.1 Background

Next generation base stations need to be efficient and wideband in nature to support multiple communication standards/bands (like the third generation mobile network, and the upcoming fourth generation standards) in an energy and cost effective manner. Currently, the overall efficiency of a base station, which relates to the conversion of DC power to the RF power, lies between only 12% to 15% [1] [2]. A large part of the efficiency is set by the performance of RF power amplifiers. A power amplifier (PA) is used to convert a low power level RF signal into a signal of much higher power to drive the antenna. In Figure 1.1 the block diagram of a modern high power base-station is given. As the last stage in the transmit chain, the PA is typically the most power hungry component and needs to handle the highest power level. It also requires the most attention with respect to the power efficiency, linearity power dissipation and cost.

![Figure 1.1 Wireless base station](image)

Many techniques have been proposed to enhance the performance of PAs over the years, such as Doherty, outphasing, dynamic load line, envelope tracking and
envelope elimination and restoration (EER). All these techniques increase the efficiency at the back-off power levels by improving the ratio of output power versus DC power over the transistors of the output stage. Among those methods, the Doherty power amplifier (DPA) technique is quite popular in the recent base station market due to its simplicity, low cost and high efficiency in power back-off operation.

1.2 Design Challenges and Project Goals

Although Doherty amplifiers are widely used, their increased efficiency performance is typically at the cost of their linearity and operating bandwidth. The Class C biased peaking device causes AM-PM distortion which limits the overall amplifier linearity. The output power combiner network is often indicated as the constraining factor for the RF bandwidth. For high power level DPA, the optimum load impedance is very low, resulting in an even narrower bandwidth. Therefore, Doherty PAs are typically narrowband and always accompanied by pre-distorters. The current improvement in the digital signal processing (DSP) technology enables the digital pre-distortion hardware to be directly embedded in the transmitter to improve linearity, consequently, research in DPA technology is recently more focused on achieving wider bandwidth [4] and increasing efficiency in power back-off operation rather than improving linearity. Within this thesis, we aim to explore a new design method that can extend the RF bandwidth of DPAs up to one octave without any degradation in peak and power back-off efficiency for a 2-way symmetrical DPA. For this purpose, first the background theory is given followed by a review of currently known wideband DPA design techniques. Starting from that, we introduce differential DPA structure with related matching strategies, resulting in a novel wideband power combiner scheme, which form the key contributions of this work. Using the concepts introduced high performance wideband DPA seem to become feasible.

1.3 Thesis Structure

The outline of the thesis is summarized as follows.

Chapter 2 briefly discusses the conventional PA operating classes. Then the basic theory of DPA is provided. After that, the bandwidth analysis with different existing DPA structure is performed, following the work of [5].
Chapter 3 gives innovative solutions to enhance RF operating bandwidth of the DPA. Several bandwidth improvement techniques are introduced, e.g. through using a frequency compensated impedance inverter the bandwidth behavior can be improved \[6\] \[7\]. Moreover, adding an offset line after the peak device will help to boost load at the power back-off in a wideband fashion \[8\]. To obtain more design freedom to implement the harmonic terminations, a differential topology is introduced in the DPA design, which is one of the key contributions of this work.

In Chapter 4 it describes a critical part of a differential DPA which is the balun. The behavior of an ideal balun is analyzed first. After that, two already existed structures are discussed. One is coaxial cable based balun and the other is vertically installed planar (VIP) balun. Both of these two structures have their drawbacks in practical high power implementations. Therefore a suspended planar stripline balun is proposed. A detailed discussion in complementing this balun is given later in this chapter.

Chapter 5 gives the design details of a 200W DPA using GaN transistors and coaxial cable based baluns. In this design many of the techniques introduced in Chapter 3 are utilized. The simulation results of the overall DPA show that the RF operation bandwidth can be indeed improved through these techniques but not good enough.

A practical coaxial cable balun will have some limitations such as low power handling capability, unpredictable behavior introduced by the transitions at the coax connection points. Therefore, in Chapter 6, an even higher power DPA (\(P_{\text{max}}=1\text{kW}\)) is designed using the novel suspended planar baluns described at the end of Chapter 4 and LDMOS (laterally diffused metal oxide semiconductor) transistors. This structure can offer lower impedance levels than coaxial cable based baluns and it is more suitable for mass production. Details on how to reach the desired balun performance are given.

Finally the overall conclusions are given in Chapter 7.
Before exploring any new matching strategies for the Doherty power amplifier, it’s useful to have a quick review on the classic power amplifier operations, like Class A, AB, B, C, F, J and their inverse counterparts. By adjusting the biasing point of the devices and/or controlling their harmonics, power devices can work at different operating classes and offer enhanced efficiency. It is the requirement on the harmonic conditions that will determine the efficiency bandwidth constrain in their final application. In this section, firstly, the principles of conventional PA are introduced. Next, DPA operation is discussed followed by an efficiency-bandwidth analysis.

2.1 Conventional Power Amplifiers

2.1.1 Class A, AB, B and C Power Amplifiers

These four types of power amplifiers are mainly distinguished by their bias conditions. This may be understood by the model sketched in Figure 2.1. In this section, the transistor in this category of power amplifiers can be regarded as a voltage controlled current source. The resulting amplifier class is mainly set by the gate biasing and by the impedances offered to the drain at the fundamental frequency and its harmonics. Different bias conditions will result in a different conduction angle $\alpha$. The conduction angle is defined as the portion of the RF cycle in which the device stays in saturation. For the analysis of all these classes, a sinusoidal signal is being assumed at the input of the active device. Class AB, Class B and Class C use short circuited conditions for all their harmonics. For Class A, due to the assumption that it is perfectly linear, no harmonic current will flow, therefore in this particular case the termination of the harmonics is less relevant and can be both shorted or assumed to be equal to the fundamental load.
Class A

In class A, the conduction angle is 360°. The biasing level is chosen to enable the transistor to operate in linear mode at all times, which means that the transistor remains conducting and stays in the saturation region during the entire input cycle. Theoretically, this type of power amplifier can achieve a 50% efficiency [9].

Class B

In class B, the conduction angle is 180°. The biasing level is set at the active device’s threshold voltage. The transistor conducts for half the cycle of the input RF signal. Linearity of class B is typically worse than class A. However, if proper 2\textsuperscript{nd} harmonic termination is used, class B can be very linear. By doing so, the memory effects can be reduced due to shorts in both baseband and harmonic termination. The theoretical maximum drain efficiency (DE) of an amplifier in class B mode is 78.5% [9].

Class AB

The conduction angle of this type is between 180° and 360°, depending on the bias levels. As a result, the efficiency and linearity are somewhat intermediate between class A and class B. The efficiency for this class of operation is between 50% and 78.5% [9].

Class C

In class C operation, the conduction angle is somewhere between 0° and 180°. Theoretically, a drain efficiency of 100% can be achieved [9], however in this specific
condition, the output power is basically reduced to zero. So, trade-off between efficiency and output power must be made. Moreover, linearity of this type is poor compared to class A and class B operation.

The various classes comprising the transconductance power amplifiers are summarized in Table 2.1.

<table>
<thead>
<tr>
<th>Operating Class</th>
<th>Conduction Angle $\alpha$</th>
<th>Drain Efficiency in %</th>
</tr>
</thead>
<tbody>
<tr>
<td>A</td>
<td>$2\pi$</td>
<td>50</td>
</tr>
<tr>
<td>B</td>
<td>$\pi$</td>
<td>78.5</td>
</tr>
<tr>
<td>AB</td>
<td>$\pi$ ~ $2\pi$</td>
<td>50~78.5</td>
</tr>
<tr>
<td>C</td>
<td>$0$ ~ $\pi$</td>
<td>78.5~100</td>
</tr>
</tbody>
</table>

**Mathematical analysis of transconductance based power amplifier**

A generalized current waveform incorporating all classes is shown in Figure 2.2 with varying conduction angle $\alpha$ and quiescent bias current $I_q$.

The drain current waveform ($i_d(\theta)$ in Figure 2.1) of the transistor can be expressed as

$$i_d(\theta) = \begin{cases} 
I_q + I_{pk} \cos \theta & \text{for } -\frac{\alpha}{2} \leq \theta \leq \frac{\alpha}{2} \\
0 & \text{for } -\pi < \theta < -\frac{\alpha}{2} \text{ or } \frac{\alpha}{2} < \theta < \pi 
\end{cases} \quad (2.1)$$

Where:
\( \alpha \) is the conduction angle,

let \( \theta = \frac{\alpha}{2} \), \( \cos \theta = -\frac{I_q}{I_{pk}} \),

\( i_d \) = drain current,

\( I_q \) = quiescent current,

\( I_{pk} = I_{max} - I_q \), amplitude of drain current,

\( I_{max} \) = the peak value of drain current.

Solving (2.1):

\[
i_d(\theta) = \frac{I_{max}}{1 - \cos\left(\frac{\alpha}{2}\right)} \left(\cos \theta - \cos\left(\frac{\alpha}{2}\right)\right), \text{for } -\frac{\alpha}{2} < \theta < \frac{\alpha}{2}
\]

(2.2)

The related DC current can be calculated through using Fourier decomposition as well as the fundamental and harmonic current components.

The Fourier expression of the waveform is:

\[
i_d(\theta) = I_{dc} + \sum_{n=1}^{\infty} I_n \cos(n\theta)
\]

(2.3)

Where the DC component is given by:

\[
I_{dc} = \frac{I_{max}}{2\pi} \cdot \frac{2\sin\left(\frac{\alpha}{2}\right) - \alpha \cos\left(\frac{\alpha}{2}\right)}{1 - \cos\left(\frac{\alpha}{2}\right)}
\]

(2.4)

The fundamental component is given by:

\[
I_1 = \frac{I_{max}}{2\pi} \cdot \frac{\alpha - \sin \alpha}{1 - \cos\left(\frac{\alpha}{2}\right)}
\]

(2.5)

The magnitude of \( n^{th} \) harmonic is:

\[
I_n = \frac{1}{\pi} \int_{\frac{\alpha}{2}}^{\frac{\alpha}{2}} \frac{I_{max}}{1 - \cos\left(\frac{\alpha}{2}\right)} \cdot \left(\cos \theta - \cos\left(\frac{\theta}{2}\right)\right) \cdot \cos(n\theta) \, d\theta
\]

(2.6)

where \( n \geq 2 \) and \( n \in \mathbb{N} \).

If the fundamental loading impedance is set to make the drain voltage of the device have a maximum \( 2V_{dc} \) peak to peak value, a maximum output power can be obtained
in this condition. This matching is called load line matching and the optimum load impedance is:

\[ R_{\text{opt}} = \frac{V_1}{I_1} = \frac{V_{\text{dc}}}{I_1} = V_{\text{dc}} \cdot \frac{2\pi}{I_{\text{max}}} \cdot \frac{1 - \cos\left(\frac{\alpha}{2}\right)}{\alpha - \sin \alpha} \]  

(2.7)

Figure 2.3 shows the load line for different classes of conventional PAs.

![Figure 2.3 Load line of different classes of conventional PAs](image)

The RF fundamental output power is given by:

\[ P_{\text{out}} = V_{\text{dc}} I_1 = V_{\text{dc}} I_{\text{max}} \cdot \frac{\alpha - \sin \alpha}{2 \sin \left(\frac{\alpha}{2}\right) - \alpha \cos \left(\frac{\alpha}{2}\right)} \]  

(2.8)

and the DC power supply is given by:

\[ P_{\text{dc}} = V_{\text{dc}} I_{\text{dc}} \]  

(2.9)

Where \( I_{\text{dc}} \) is from (2.4).

Then the drain efficiency is defined by:

\[ \eta = \frac{P_{\text{out}}}{P_{\text{dc}}} = \frac{1}{2} \cdot \frac{V_{\text{dc}} I_1}{V_{\text{dc}} I_{\text{dc}}} = \frac{1}{2} \cdot \frac{\alpha - \sin \alpha}{\sin \left(\frac{\alpha}{2}\right) - \alpha \cos \left(\frac{\alpha}{2}\right)} \]  

(2.10)

From (2.4) (2.10), the output power and efficiency can be plotted as a function of conduction angle, as shown in Figure 2.4.
It is obvious that when the conduction angle is smaller than $\pi$, although the efficiency goes higher, the output power is dropped dramatically. Therefore, in a conventional PA design, there is always a trade-off between output power and efficiency.

![Figure 2.4 Efficiency and output power (normalized to Class A operation) versus conduction angle of drain current](image)

2.1.2 Class F

The main difference between Class B and Class F operation is the open condition for the odd higher harmonics, which yields squaring of the output voltage wave. Figure 2.5 shows the typical textbook topology of a Class F amplifier and its drain voltage/current waveforms. In practical situations, more than three harmonics are difficult to control, resulting in a reduction of the maximum obtainable efficiency from 100%. Realization typically involves the use of many transmission lines for controlling harmonic impedances. The control of more harmonics tends to make the design narrowband. At RF, the parasites of the device become significant and they must therefore be resonated out to present the required impedances at the internal current generator plane [10]. In traditional Class F amplifier implementations the frequency sensitive harmonic resonators will result in a narrowband operation as well. The inherent narrowband performance of these traditional Class F amplifiers restricts their potential for integration within wideband or multiband transceivers.
2.1.3 The Continuous Class J*-B-J

While using capacitive 2\textsuperscript{nd} harmonic terminations in Class AB or Class B operation, the circuit can be tuned to Class J operation. The capacitive load seen by the device will reduce the precise harmonic shorting requirements of the Class B amplifier. Now the reactive loading condition of Class J is becoming:

\[ Z_{\text{fund,J}} = R_{\text{fund,B}}(1 \pm j) \quad (2.11) \]
\[ Z_{2\text{nd,J}} = \mp j \frac{3\pi}{8} R_{\text{fund,B}} \quad (2.12) \]

Where \( R_{\text{fund,B}} = R_{\text{opt}} = 2 \frac{V_{\text{dc}}}{I_{\text{max}}} \), \( R_{\text{opt}} \) is the optimum loading condition for an ideal Class B operation.

The loading condition of Class J- B- J* is depicted in Figure 2.6.
The red curve shows the fundamental impedance is changing from $F_c - \delta F$ to $F_c - \delta F$ where the operation classes is continuous, $F_c$ represents the center frequency. As can be seen in Figure 2.7, there appears to be a continuum of high efficiency operation from Class J through Class B to Class J* as long as the ratio of the reactance of the fundamental load to optimum load resistance is less than 1. In this circuit, the maximum bandwidth occurs when the final point lying in the fundamental frequency range is the starting point of the 2nd harmonic range [11]. The maximum bandwidth $BW$ can be calculated by:

$$2 \left( F_c - \frac{BW}{2} \right) = F_c + \frac{BW}{2}$$  \hspace{1cm} (2.13)

$$BW = \frac{2}{3} F_c$$  \hspace{1cm} (2.14)

Recently the Class J principle is extended to the Class F amplifier to overcome the intrinsic narrowband behavior of traditional Class F amplifiers, and termed the continuous Class F amplifier [12]. The continuous Class F amplifier offers a wide
range of voltage waveform that can be dynamically exploited across a desired bandwidth. The need for perfectly harmonic short is significantly relaxed, as such reducing the necessity for narrowband harmonic resonators. In [13] the author successfully implemented a continuous Class F amplifier, however, at both the input and output matching, there still have many stages transmission line based low-pass matching network. Every stage needs to be precisely tuned to properly align the impedance trajectory to the target impedances at both the fundamental and harmonic frequencies, which complicates the design.

![Figure 2.7 Efficiency contours for different fundamental and 2nd harmonic loading conditions](image)

**Figure 2.7 Efficiency contours for different fundamental and 2nd harmonic loading conditions**

(X is the reactance load; $R_{opt}$ is the optimum resistive load)

### 2.1.4 The Inverse Classes

For the inverse classes, voltage and current waveforms are interchanged. Consequently, the inverse Class B uses harmonic open conditions, while the inverse Class F amplifier uses open conditions at even harmonics and short circuited conditions at the odd harmonics. Once again, the non-overlap of voltage and current waveforms enable a high theoretical efficiency of this architecture.

However, the linearity of these inverse classes is not so good. To get the devices into inverse classes, one should drive the devices very hard, which will limit the linearity and puts a lot of voltage stress on the devices. Moreover, in practical design, the present of device’s output capacitance makes it very difficult to implement a wideband open termination.
2.1.5 Conclusion

In this section, to support the discussion on DPAs, several PA operation classes are briefly discussed. For these basic operation classes, there is always a trade-off between linearity and efficiency. Also, continuous operating classes are briefly reviewed. These concepts are very important for a wideband operation and as such they form the foundation of later discussions.

2.2 Doherty Power Amplifier

![Basic configuration of DPA](image)

Figure 2.8 Basic configuration of DPA

In power back-off level, a conventional PA drops in efficiency since for the given output power level the output voltage swing with respect to the supply voltage is reduced. For high efficiency amplifier, there are two basic concepts which can maximize the voltage swing with respect to the supply voltage in power back-off. One is changing the load line; the other is by modulating the supply voltage. The Doherty amplifier, invented by W. H. Doherty in 1936 [14], is directly based on the idea of changing the load impedance. Traditionally, the DPA is implemented with two identical devices, as depict in Figure 2.8. In this section, the theory of the DPA will be discussed in detail.

2.2.1 The Principle of DPA

The diagram of a two-way DPA in its elementary form is given in Figure 2.9. Typically, the DPA consists of two devices, which can be modeled as two current
sources. The main and peak devices are connected by a quarter wavelength transmission line (QWTL). At low power level, only the main amplifier is active. The impedance inverter inverts the load impedance to a higher value to boost the voltage swing across the drain of the main amplifier, thus yielding a higher efficiency. At higher power level, the peak amplifier starts to work which will increase the voltage swing across the load impedance. Consequently, the impedance seen at the output of the impedance inverter is effectively larger than its component value. Through the impedance inverter, the impedance seen by the main amplifier will be pulled down and its output power can continue to increase with increasing input power. This is what we call load-pulling. As input power further increases, the output power increases until it reaches the peak power capability of the amplifier.

In Figure 2.9, $Z_0$ is the characteristic impedance of the QWTL impedance inverter. $V_m$ and $I_m$ are the fundamental drain voltage and current of the main amplifier, while $V_p$ and $I_p$ are the fundamental drain voltage and current of the peak amplifier, respectively. Note that the current flowing out the main amplifier is delayed by the QWTL therefore a phase lag of $90^\circ$ should be introduced into $I_p$ to compensate the phase shift. Substitute $I_p$ with $-jI_p$ and the two-port network of the impedance inverter in chain matrix notation can be expressed as (note $V_p = V_o$):

$$\begin{bmatrix} V_m \\ I_m \end{bmatrix} = \begin{bmatrix} 0 & jZ_0 \\ \frac{1}{Z_0} & 0 \end{bmatrix} \begin{bmatrix} 1 \\ -jI_p \end{bmatrix} \begin{bmatrix} V_o \\ 0 \end{bmatrix}$$

(2.15)

Derive from (2.15), the $Z$ matrix can be obtained:
\[
\begin{bmatrix}
V_m \\
V_p
\end{bmatrix} = \begin{bmatrix}
\frac{Z_0^2}{R_L} & -jZ_0 \\
-jZ_0 & 0
\end{bmatrix} \begin{bmatrix}
I_m \\
-jI_p
\end{bmatrix}
\]  \hspace{1cm} (2.16)

Solving (2.16) the impedance seen from the drain of the main and peak device can be expressed as:

\[
Z_m = \frac{V_m}{I_m} = \frac{Z_0^2}{R_L} - jZ_0 \frac{I_p}{I_m}
\]  \hspace{1cm} (2.17)

\[
Z_p = \frac{V_p}{I_p} = Z_0 \frac{I_m}{I_p}
\]  \hspace{1cm} (2.18)

Clearly, (2.17) and (2.18) show that the impedance of the devices is modulated by the current ratio of main and peak device.

Next a back-off factor \( \alpha \) is defined. \( V_{\text{in}} \) is the gate drive for both devices and \( V_{\text{in,max}} \) is the maximum value that \( V_{\text{in}} \) can achieve. When \( V_{\text{in}} \geq \alpha V_{\text{in,max}} \) the peak device will be turned on. \( G_m \) and \( G_p \) are the transconductance of the main and peak amplifier. Since the current of both devices are controlled by their driving voltage, here both main and peak device are assumed to have the following transfer characteristics.

\[
I_m = \begin{cases}
0 & \text{if } V_{\text{in}} < 0 \\
G_m V_{\text{in}} & \text{if } 0 \leq V_{\text{in}} \leq V_{\text{in,max}} \\
G_m V_{\text{in,max}} & \text{if } V_{\text{in}} > V_{\text{in,max}}
\end{cases}
\]  \hspace{1cm} (2.19)

\[
I_p = \begin{cases}
0 & \text{if } V_{\text{in}} < \alpha V_{\text{in,max}} \\
G_p (V_{\text{in}} - \alpha V_{\text{in,max}}) & \text{if } \alpha V_{\text{in,max}} \leq V_{\text{in}} \leq V_{\text{in,max}} \\
G_p (1 - \alpha) V_{\text{in,max}} & \text{if } V_{\text{in}} > V_{\text{in,max}}
\end{cases}
\]  \hspace{1cm} (2.20)

Consequently the two devices work as follows:

Below the back-off point, that is \( V_{\text{in}} < \alpha V_{\text{in,max}} \), the peak device does not turn on and hence \( I_p = 0 \). From (2.17):

\[
Z_m = \frac{Z_0^2}{R_L}
\]  \hspace{1cm} (2.21)

\[
V_m = I_m \frac{Z_0^2}{R_L}
\]  \hspace{1cm} (2.22)

At the back-off point, or say \( V_{\text{in}} = \alpha V_{\text{in,max}} \), the main device becomes saturated. The drain voltage of main device reaches its peak amplitude, which are:
\[ V_m = G_m V_{in} \frac{Z_0^2}{R_L} = G_m \cdot \alpha V_{in,\text{max}} \frac{Z_0^2}{R_L} = V_{dc} \]  

(2.23)

After the back-off point, the peak amplifier starts to operate. Then:

\[ V_m = I_m Z_m = I_m \left( \frac{Z_0^2}{R_L} - Z_0 \frac{I_p}{I_m} \right) = V_{dc} \]  

(2.24)

\[ V_p = I_p Z_p = I_p Z_0 \frac{I_m}{I_p} = I_m Z_0 \]  

(2.25)

At full power level, both amplifiers show full swing at drain. As such both amplifiers reach their maximum voltage swing which is equal to the supply voltage. According to (2.16), (2.17) and (2.18):

\[ V_{m,\text{full}} = G_m V_{in,\text{max}} \left( \frac{Z_0^2}{R_L} - Z_0 \frac{G_p}{G_m} \right) = V_{dc} \]  

(2.26)

\[ V_{p,\text{full}} = G_p (1 - \alpha) V_{in,\text{max}} Z_0 \frac{G_m}{G_p (1 - \alpha)} = V_{dc} \]  

(2.27)

Solving (2.19), (2.20), (2.24), (2.26) and (2.27), the current and transconductance ratio of the main and peak device can be derived.

\[ \frac{Z_0}{R_L} = \frac{G_p}{G_m} = \frac{1}{\alpha} \]  

(2.28)

\[ \frac{I_{\text{max},m}}{I_{\text{max},p}} = \frac{\alpha}{1 - \alpha} \]  

(2.29)

### 2.2.2 Ideal DPA Performance

The analysis in the previous section shows that in the DPA operation, the effective transconductance ratio of the main and peak amplifier is \( \alpha \) when both devices are on. This can be done through controlling the amplitude of the input. This is called as mixed-signal drive. In order to get the same output maximum current, the input signal should meet the following equations:

\[ V_{in,m} = V_{in} \]  

(2.30)

\[ V_{in,p} = \begin{cases} 
0 & \text{if } V_{in} \leq \alpha V_{in,\text{max}} \\
\frac{1}{\alpha} (V_{in} - \alpha V_{in,\text{max}}) & \text{if } \alpha V_{in,\text{max}} \leq V_{in} \leq V_{in,\text{max}} 
\end{cases} \]  

(2.31)
Here assume that all the models are linear, the biasing point is also set at the value that the main device is working in linear region. Therefore, the characteristics of DPA can be described by the following equations.

**Fundamental device current**

When the main device is on, from (2.15), and (2.28):

\[ I_m = \frac{\alpha V_{out}}{R_L} \]  

(2.32)

When the peak device is turned on, from (2.15), (2.24) and (2.28):

\[ I_p = \frac{I_m}{\alpha} - \frac{\alpha V_m}{R_L} = \frac{V_{out} - \alpha V_{dc}}{R_L} \]  

(2.33)

**Fundamental device voltage**

When the main device is on, from (2.15) and (2.32):

\[ V_m = \frac{V_{out}}{\alpha} \]  

(2.34)

When the peak device is turned on, we have \( V_m = V_{dc} \) and:

\[ V_p = \frac{\alpha Z_0 V_{out}}{R_L} = V_{out} \]  

(2.35)

**Output power**

Assume that the devices are working at Class B mode (conduction angle is \( \pi \)); from the previous subsection we know that:

\[ I_{dc} = \frac{2}{\pi} I_{fund} \]  

(2.36)

When only the main device is on, \( I_p = 0 \),

\[ P_{out} = P_{main} = \frac{1}{2} I_m^2 \text{Re}(Z_m) = \frac{1}{2} \frac{V_{out}^2}{R_L} \]  

(2.37)

\[ P_{dc} = V_{dc} I_{dc} = \frac{2 \alpha V_{dc} V_{out}}{\pi R_L} \]  

(2.38)

After the back-off point, the peak device is turned on,
\[ P_{out} = P_{\text{main}} + P_{\text{peak}} \]
\[ = \frac{1}{2} I_m^2 \left( \frac{Z_0^2}{R_L} - Z_0 \frac{I_p}{I_m} \right) + \frac{1}{2} I_p^2 \left( Z_0 \frac{I_m}{I_p} \right) \]
\[ = \frac{1}{2} I_m^2 \frac{Z_0^2}{R_L} \]
\[ P_{dc} = \frac{2}{\pi} V_{dc} (I_m + I_p) = \frac{2 V_{dc}}{\pi R_L} (\alpha V_{out} + V_{out} - \alpha V_{dc}) \]

**Efficiency**

When the main device is on,
\[ \eta = \frac{\pi V_{out}}{4 \alpha V_{dc}} \]

When the peak device is turned on,
\[ \eta = \frac{\pi}{4} \left( \frac{V_{out}}{V_{dc}} \right)^2 \left( \frac{V_{out}}{V_{dc}} \right) (\alpha + 1) - \alpha \]

With all the information included, an ideal 2-way symmetrical DPA (\( \alpha=0.5 \)) is simulated using ideal components. All PA devices are biased at Class B working condition, thus the maximum efficiency is 78.5%. The driving conditions are specified according to (2.30) and (2.31). The output power is normalized to 1W. Its characteristics are shown in Figure 2.10.

### 2.2.3 Conclusion

The DPA shows an improvement in the efficiency over a large range of output power level as shown in Figure 2.10. Compared with Class B power amplifier, there are two efficiency peaks in the simulated DPA and both deliver 78.5% maximum efficiency. The main amplifier maintains maximum efficiency over the upper \(-20 \log(\alpha)\)dB power range, and the peak amplifier delivers efficiency from the back-off point to the maximum power level. Figure 2.10 also shows the loading condition of both amplifiers. Due to the QWTL, the load modulation effect will be inherently frequency selective. In optimum designed implementations this will be the main bandwidth limiting factor in the DPA. In the next section, we will discuss the frequency behavior of this DPA. Other limitations with be further discussed in the following chapter.
2.3 Bandwidth Discussions of DPA

To investigate the bandwidth constraints of the various known DPA configurations, some assumptions are first made before discussion. First, the same as previous subsection, all devices are operated ideally, which means the active device acts like a perfect current source in linear region and as a voltage source in the saturated region with zero knee voltage and zero output capacitance. Second, assume that all the harmonic shorts are perfect Class B terminations, i.e. all harmonics are perfectly...
shorted independent of operating frequency. Last but not least, assume that there is perfect phase tracking between main and peak device versus frequency, e.g. in the case of a two-way DPA, the phase of the peak amplifier is only \(-90^\circ\) relative to that of the main amplifier at the design center frequency and at all other frequencies it tracks the phase rotation offered by the impedance inverter, which is frequency dependent. For the efficiency bandwidth (BW$_{10\%}$), take the point where the efficiency is within 10% of its maximum value. For the power bandwidth (BW$_{0.5\text{dB}}$), usually take 0.5dB power reduction as limiting conditions. However, there are also some works refer to 3% efficiency bandwidth (BW$_{3\%}$) as a limit. This is more a tightened condition but it better represents the market demands.

### 2.3.1 Symmetrical and Asymmetrical Two-way DPA

A comparison of the bandwidth performance for symmetrical and asymmetrical two-way DPA is illustrated in Figure 2.11. Figure 2.11(a) shows the bandwidth performance of a typical symmetrical two-way DPA which is depicted in Figure 2.8 in section 2.2. As can be seen in the figure, at full power level the impedance remain the same (all devices are loaded with $Z_0$). As a consequence, there is no bandwidth limitation at full power level, which is the blue curve in Figure 2.11(a). However, in power back-off level, due to the frequency dependent impedance caused by the QWTL, a narrowband behavior is observed by red curve. Consequently, in the idealized case at 6dB back-off the relative bandwidth (BW$_{10\%}$) for efficiency is restricted to 28% and for BW$_{3\%}$ the number is 14%. When considering practical implementations of the Doherty power amplifier, often there is an additional impedance transformation incorporated in the output to match to the 50\$\Omega$ impedance level, which will also have impact on the bandwidth as depict in Figure 2.11(b). In this example the transformation is made by a single section QWTL. The difference between a symmetrical and asymmetrical DPA lies in the ratio of the maximum output power of the peaking amplifier with respect to that of the main amplifier [15], or say the back-off factor $\alpha$ that is defined before. Figure 2.11(c) shows an asymmetrical DPA with a back-off factor of 0.25 (or say a power ratio of 1:3) for its main and peaking device, the efficiency at 12dB back-off is dropped to 16% for the BW$_{10\%}$ and the number is 8% for BW$_{3\%}$.
Figure 2.11 Simulated efficiency and output power vs. frequency of ideal Class B operated DPAs normalized to 1W output power using a 1 GHz design frequency
(a) Symmetrical two-way DPA;
(b) Symmetrical two-way DPA with single QWTL output transformer;
(c) Asymmetrical two-way DPA

2.3.2 3-way and 4-way DPA

According to the theory, a three-way DPA (Figure 2.12(a)) provides an additional third high-efficiency peak in their efficiency curve versus power back-off compared to a two-way DPA. However, these amplifiers will provide higher average efficiency for signals with a large peak-to-average ratio at the cost of an increased complexity or really complicated driving profile.
For example, [16] provides a mixed-signal driving technique to control the three-way DPA and proved that the three-way DPA can provide an excellent efficiency performance versus power back-off. The use of mixed-signal techniques, however, yields a significant increase in complexity, which in many situations is undesired. To overcome these difficulties a new three-way DPA configuration is introduced in [17]. This later design, in Figure 2.12(b), uses a more sophisticated power combiner, which allows more relaxed drive profiles for its main and peaking devices. Efficiency and output power of both three-way DPA configurations have been plotted in Figure 2.13. From these results it can be concluded that both configurations have an improvement in terms of bandwidth and efficiency versus power back-off compared with the two-way DPA. Among this topology, the novel three-way DPA provides the best relative bandwidth for BW_{3%}, namely 32% at 9.5dB back-off and 39.8% for the BW_{0.5dB},
which is respectively 6% to 14% higher than that of a traditional three-way DPA for BW3%.

Recently, there is an exploration of a novel four-way DPA which is depicted in Figure 2.14(a) on the following page. In [18], the method provides an additional fourth high-efficiency peak in the efficiency curve versus power at 12dB back-off. As such it can provide theoretically even higher average efficiencies than the novel three-way DPA. However, the related higher complexity does not result in a larger bandwidth, as shown in Figure 2.14(b).
2.3.3 Performance Comparison

An overview of the bandwidth performances of the various Doherty amplifier configurations is given in Table 2.2. It works out that the asymmetric two-way DPA is the most limited in its efficiency bandwidth in power back-off, while the novel 3-way DPA provides clear bandwidth benefits over the other configurations at both peak output power (BW_{0.5dB}=39.8%) as well as in efficiency at power back-off operation (BW_{3dB}=32%). But this performance is at the cost of circuit complexity. For the two-way DPA, either symmetrical or asymmetrical configuration, there still have possibilities to improve.
### Table 2.2 Bandwidth comparison of different DPA topologies

<table>
<thead>
<tr>
<th>Doherty type</th>
<th>Efficiency %</th>
<th>Peak Power %</th>
</tr>
</thead>
<tbody>
<tr>
<td>(main device : peak device(s))</td>
<td>BW₃%</td>
<td>BW₀.₅dB</td>
</tr>
<tr>
<td>2-way Sym (1:1)</td>
<td>10.4</td>
<td>25.8</td>
</tr>
<tr>
<td>2-way Asym (1:2)</td>
<td>7.4</td>
<td>23.4</td>
</tr>
<tr>
<td>3-way Classical (1:2:2) [16]</td>
<td>26.0</td>
<td>25.2</td>
</tr>
<tr>
<td>3-way Novel (1:1:1) [17]</td>
<td>32.0</td>
<td>39.8</td>
</tr>
<tr>
<td>4-way Novel (1:1:1:1) [18]</td>
<td>24</td>
<td>24</td>
</tr>
</tbody>
</table>

#### 2.4 Conclusion

Compared to conventional single line-up Class B PAs, Doherty Power amplifiers provide higher efficiency at power back-off operation. However, the load modulation principle utilized in the DPA is frequency dependent in nature. This effect becomes more obvious in asymmetrical DPAs when including the additional impedance transformation to 50Ω. An overview on bandwidth performance of various DPA configurations including N-way DPAs has been given in this chapter. Although the novel four-way or three-way DPA can theoretically provide better efficiency performance in terms of power back-off operation, the improvement is at the cost of circuitry complexity. Note that in all the discussions above, ideal operation is assumed for the active devices, e.g. no output parasitics and perfect harmonic terminations versus frequency. In the next chapter, in addition to the DPA topology itself, analysis will show that other factors may influence the achievable RF operation bandwidth in practical situations.
In Chapter 2, the analysis is based on ideal devices and the assumption of perfect harmonic short-circuited conditions that are independent of frequency. However, in real life, these conditions are often no longer satisfied, yielding significant constraints on the actual realizable bandwidth. To study these effects, a two-way DPA design is analyzed in this chapter. The analysis includes the impact of output capacitance and the inductive bondwire connections on the power dies. To overcome the RF bandwidth restrictions related to a classical 2-way DPA impedance inverter, in section 3.2, a novel output power combiner is given [1], which has the potential to enhance the achievable efficiency bandwidth of the overall two-way DPA architecture. Finally, to fully utilize this bandwidth potential, a differential DPA design approach is introduced, which can provide more design flexibility to implement the harmonic terminations.

3.1 Improving the Traditional Power Combiner

The maximum bandwidth of DPA can be achieved if the PA devices are matched using wideband impedance matching techniques, which is traditionally done by matching the output of the PA devices as a complex impedance [19]. Using this approach in DPA operation, because of the load modulation, it is better to simplify the output matching network as a shunt parallel RC network as shown in Figure 3.1. However, in this topology the efficiency is degraded. The degradation is determined by the equation [1]:

$$\eta_{\text{degrade}} = \cos\left(\tan^{-1}\left(2\pi C_{\text{dev}}R_{\text{opt}}(1 - f^2)\right)\right)$$  \hspace{1cm} (3.1)

From (3.1), it is obvious that the efficiency degradation depends on the output capacitance and optimum loading of the PA device which is characteristic for a given technology. The efficiency-frequency characteristics of the DPA with devices NXP’s
LDMOS Gen 7 and Cree Inc. GaN are plotted in Figure 3.2. Note that output capacitance of GaN from Cree is almost half the capacitance of the LDMOS devices for the same output power level. This reduced output capacitance offers a better starting point to achieve a large high-efficiency bandwidth.

The first step to improve the bandwidth of the DPA is to compensate the output capacitance for the devices in a wideband fashion in order to eliminate the resonance at output [6]. An effective method to do so, is to absorb the output capacitance along-with the connecting bondwire in the impedance inverter [7]. Figure 3.3 shows the related DPA schematic, which now includes the output capacitance and the connecting bondwires. Note that $C_{\text{dev}}$ along with the bondwire and QWTL will form the new impedance inverter, which is called the quasi-lumped TL. Consequently, if the length and characteristic impedance of the connecting transmission line in this quasi-lumped inverter are adjusted in a proper way, it will provide the desired impedance transformation at the center frequency.
A quick analysis of this quasi lumped transmission line is performed below [1] [4]:

For simplicity, first the inductance of the bondwires $L_B$ is neglected. Then we have the electrical length and characteristic impedance of the required connecting transmission line needed to absorb the output capacitance of the active devices in the quasi-lumped inverter:

$$\theta_t = \cos^{-1}(\omega C_{dev} Z_0)$$  \hspace{1cm} (3.2)

$$Z_t = \frac{Z_0}{\sin(\theta_t)}$$  \hspace{1cm} (3.3)

$Z_0$ is the characteristic impedance of the original full QWTL impedance inverter, $Z_t$ and $\theta_t$ are the calculated impedance and electrical length of the transmission line in the quasi-lumped TL. Since $\theta_t$ should be smaller than 90 degree, (3.2) also indicates the maximum output capacitance that this method can absorb, which for a particular frequency $\omega$ is given by:

$$C_{dev} < \frac{1}{\omega Z_0}$$  \hspace{1cm} (3.4)

Or,

$$\omega < \frac{1}{C_{dev} Z_0}$$  \hspace{1cm} (3.5)
After introducing the effect of bondwires inductance $L_B$, the electrical length and impedance in the final realization turn out to be:

$$\theta_{\text{final}} = \tan^{-1}\left(\frac{Z_t}{\omega L_B}\right)$$  \hspace{1cm} (3.6)

$$Z_{\text{final}} = Z_t \frac{\sin(\theta_{\text{t}})}{\sin(\theta_{\text{final}})}$$  \hspace{1cm} (3.7)

Another concern is the bias line. As known from Figure 3.3, there are two bias lines connecting to the drain of two devices. Traditionally QWTLs are used as drain bias line which also serves as 2\(^{nd}\) harmonic short termination. The bias lines in this design are not set to 90° at the design frequency but to a lower value, such that they behave inductive and resonate out the output capacitance in the fundamental band. The impedance of the bias lines should meet the condition to keep away the resonance between the bias line and output capacitance at the intended operating band of DPA. The impedance of the lines should meet the condition:

$$Z_{\text{bias}} < \frac{1}{2\pi f_{\text{res}} C_{\text{dev}} \tan\left(\frac{\pi f_{\text{res}}}{f_{\text{fund}}}\right)}$$  \hspace{1cm} (3.8)

Where $f_{\text{fund}}$ and $f_{\text{res}}$ are the central and the resonance frequency, respectively.

At the double of the fundamental band, the input impedances provided by these lines are highly capacitive, providing an effective 2\(^{nd}\) harmonic short for the DPA.

![Figure 3.4 Drain efficiency of a 20W DPA with output capacitance compensation [4]](image)

To evaluate the above mentioned technique, in [4], achieved efficiency bandwidth performance is given. In Figure 3.4, it can be seen that at full power, the efficiency is
maintained high. But there is no efficiency enhancement at the back-off region. If the efficiency at back-off region can be improved at lower frequency band, larger DPA efficiency bandwidth can be obtained.

3.2 A Wideband Doherty Power Combiner Technique

In the previous section, the analysis and measurement results of a two-way DPA show that although the output capacitance of the devices are compensated properly by absorbing them into the impedance inverter, the bandwidth of the DPA at the power back-off is not improved. In this section, a wideband output power combiner to extend the bandwidth at the back-off region is explored.

One idea [8] of improving the wideband behavior is by adding an additional $\lambda/2$ compensation line, illustrated in Figure 3.5.

![Figure 3.5 Simplified Wideband DPA with additional compensate line](image)

To investigate this later topology, the magnitude of the load impedance versus frequency is plotted in Figure 3.6 with ideal components. Note that the load impedance $R_L$ is set to be 0.5$\Omega$, and $Z_0$ is equal to 1$\Omega$, so the wideband impedance inverter will provide 2$\Omega$ at back-off point. With the additional $\lambda/2$ offset line, the impedance is boosted close to 2$\Omega$ over a much larger bandwidth than the conventional DPA configuration shown in Figure 3.6(a). The cosine phase changing in the figure should not below 0.9 to represent a wide bandwidth. Therefore the $BW_{0.1}$ in a conventional two-way DPA is 44% and in a novel DPA topology the number is 56%.
As result, the impedance offered to the main amplifier in power back-off vs. frequency is improved, yielding an improved efficiency bandwidth.

![Normalized magnitude of the load impedance seen by the main device](image)

Figure 3.6 Normalized magnitude of the load impedance seen by the main device
(a) Magnitude of impedance at the main device in a conventional DPA;
(b) Phase of impedance at the main device in a conventional DPA;
(c) Magnitude of impedance at the main device in novel wideband DPA structure;
(d) Phase of impedance at the main device in novel wideband DPA structure

However, without 2\textsuperscript{nd} harmonic control, the devices in DPA are no longer operated at Class B, yielding the efficiency performance vs. frequency shown in Figure 3.7(a). Note that using this configuration, at power back-off the main amplifier is (strongly) overdriven but yielding still acceptable efficiency numbers. However, at higher power level only 65\% is achieved. Therefore modified bias line (see section 3.1) at the drain of the device which will provide 2\textsuperscript{nd} harmonic short is still necessary. The bias line will replace the RF choke in Figure 3.5. Now with the harmonic control method, the frequency behavior of bandwidth is changing to Figure 3.7(b). Obviously, even with the offset line inserting in front of the peak device, the bandwidth is still significantly decreased due to the frequency-dependent harmonic short. Therefore more design freedom is needed for the harmonic control terminations.
3.3 Differential Operation

To implement both fundamental and second harmonic short in wideband fashion, more design freedom is needed. The previous discussions are based on single-ended topology. In the modern communication system, the input signal usually consists of a highly complex time-varying signal whose form has to be accurately preserved during the amplification process. A simple single-ended Class B/Class AB operated amplifier would be quite unacceptable in this case, since the negative waveform of the signal would be wiped out [9]. Therefore the push-pull design is considered in this situation. Figure 3.8 shows the basic push-pull configuration for a DPA.

In this configuration, the top two devices are the main devices while the rest two are the peak devices. The push and pull devices in either main branch or peak branch are
driven differentially so that the equivalent circuit shows the two devices being driven in antiphase and being biased to a Class B operation, or zero quiescent current. The load is connected differentially between the two drains through a balun. Due to the differential excitation, the positive part of current waveform is linearly amplified by push device and the negative part is amplified by the pull device. Each device is driven beyond its cutoff point whenever the other is conducting. These amplified upper and lower portions will be added back together again by the action of the balun, as such the amplified signal is reconstructed at the output load.

The push-pull structure has two important advantages over single-ended operation: reduction of common lead effects and impedance doubling [9]. First and foremost, the fundamental signal flowing through the push and pull devices appear as differential signals while the even harmonics appear as common-mode signals. So ideally, if there is a common lead connecting the sources to ground, for the fundamental component, cancellation will occur (virtual ground) and no feedback voltage will be developed across the lead inductance which is very beneficial when working with high power devices. The second benefit is, while working with high power devices and differential excitation is available, the composite impedance presented by the push-pull pair at both the output and input is a factor of two higher than that presented in the single-ended structure (Figure 3.9). This is in a dramatic contrast to the impedance of a parallel pair, where the impedances would be halved in comparison to a single device.

![Figure 3.9 The impedance transformation of a balun in push pull configuration](image-url)
Moreover, the push-pull topology in combination with an input and output balun attains an orthogonal relation between the fundamental and 2\textsuperscript{nd} harmonic path providing more freedom on the harmonic terminations[20]. For this reason, it is the preferred topology while design wideband power amplifier.

However, the balun structure employed in the push-pull design is really critical. Generally, the balun is based on either magnetic coupling or transmission line coupling. The use of transmission line baluns in the push-pull configuration will result in important differences when compared to the classical push-pull amplifier, in which two anti-phased half-wave rectified current waveforms are combined using a magnetically coupled balun transformer to form a complete sinusoid [21]. Classical theory uses magnetic coupling and assumes that the even voltages harmonics at each device are shorted by the action of a center-tapped output transformer, but with transmission line baluns, the even harmonics are open-circuit terminated. Moreover, the use of magnetic coupled transformer introduces two issues [7]:

1. The coupling factor of the primary and secondary winding factor will restrict the bandwidth of the structure.
2. Assuming that transformer is implemented in a bond-wires scheme, it is extremely difficult to locate the exact electrical center. If it is not connected at the exact center, the symmetry of the structure is destroyed causing some imbalance between the fundamental signals at the drain of the push and pull devices. This results in performance degradation and a reduction of the bandwidth.

The detailed description of these issues is discussed in [11]. To avoid the above mentioned issues, transmission line based balun will be used in DPA design and is discussed in detail in the next chapter.

3.4 Conclusion

In this chapter, techniques that can improve the bandwidth of efficiency are discussed. It can be concluded that the output capacitance needs to be first absorbed into the inverter in order to get a wideband behavior. After that, employing the novel DPA structure by adding an additional offset transmission line in the circuit along with the
proper harmonic short, the bandwidth can be enlarged at power back-off compared to
the original DPA configuration. To obtain more design freedom, differential structure
is studied. This structure has the advantage of doubling the power level for the same
impedance level than the single-ended structure. Moreover, note that the fundamental
signal here is out of phase and the even harmonic signal is in phase. This feature
enable us to develop a better balun structure which is wideband and more identical
than the bondwires formed balun. Details of the design will be discussed in the
following chapter.
In Chapter 3, it was explained that the transmission line based balun has more advantages than bond-wires coupling transformer. This chapter, we will continue to explore different wideband structures of transmission line based balun.

### 4.1 Ideal Wideband Balun

A simple transmission line balun based on a piece of coaxial cable can have the form as illustrated in Figure 4.1. Generally, one end of the outer conductor is connected to ground named the unbalanced port, on the other side, the inner and the outer conductor of the cable form the balanced port. In this structure the voltage at the balanced port will be forced to be differential with respect to ground. As a result, the differential (odd-mode) signal at the balanced port will be transferred to a single-ended signal at the unbalanced port. The common-mode signals (even-mode) e.g. even harmonics will not be able to propagate over this structure since ideally the capacitance per unit length to ground is zero, which effectively resulting in an open condition for even-mode at the balanced port.

![Figure 4.1 Simplified Transmission line based Structure](image)

Note that in a Class B operated Doherty PA, we need in fact a short termination for the even harmonics. By inserting a λ/8 transmission line with the characteristic impedance that is half of the balun in front of the balanced port, the open for
common-mode signals will be transformed to a short condition at the reference plane of the active device see Figure 4.2.

\[ Z_{\text{even}} = 0 \text{ for even harmonics} \]

Figure 4.2 A balun with even-harmonic control method

To test the resulting impedances for the even-odd operation mode, the setup in simulator is shown in Figure 4.3. As in DPA operation, the characteristic impedance of the impedance inverter should be \( Z_0 = 2 \cdot R_L \), therefore in the setup, the characteristic impedance for the balun is two times of the load resistance.

In this particular example the fundamental frequency has been swept from 450MHz to 850MHz representing a 50% relative fractional BW (fractional BW = \( \frac{f_{\text{high}} - f_{\text{low}}}{f_{\text{center}}} \)).

Note that this change in frequency results also in a rotation of the input reflection...
coefficient for the common-mode signals which located on the left edge of the smith chart. To appreciate the plotted result for its wideband properties one should compare this balun structure with traditional approach using $\lambda/4$ shunt stubs. This configuration and results are shown in Figure 4.4. Note that both fundamental and even harmonic impedances vary a lot versus frequency. Obviously, this method will limit the bandwidth of not only the balun but also that of the overall amplifier.

\[
Y = \frac{1}{\eta_0 S} \begin{bmatrix}
C & -\sqrt{1-S^2} \cdot C \\
-\sqrt{1-S^2} \cdot C & C
\end{bmatrix}
\]

(4.1)

Where:
\( C = \) the 2×2 normalized static capacitance matrix with elements \( c \),

\[
c = \frac{c'}{\varepsilon} = \text{ratio of the static capacitance between conductor per unit length to the permittivity of the medium (this ratio is independent of the dielectric medium and depends only on cross-section geometry).}
\]

This dimensionless ratio is convenient for practical use with available design data,

\[
\eta_0 = \sqrt{\frac{\mu_0}{\varepsilon_0}} = 376.6 \, \Omega, \text{ the impedance of free space,}
\]

\[
S = j \tan \theta,
\]

\[
\theta = \pi \omega / 2 \omega_0, \text{ where } \omega_0 \text{ is the center frequency for which the transmission line is a quarter wavelength.}
\]

The static capacitance matrix of an ideal balun with elements \( c \) is:

\[
C = \begin{bmatrix}
    c_1 + c_{12} & -c_{12} \\
    -c_{12} & c_2 + c_{12}
\end{bmatrix}
\]  

(4.2)

Where \( c_{12} \) is the mutual coupling between the coupled transmission lines, \( c_1 \) and \( c_2 \) are the coupling between each conductor and the ground. In an ideal balun, \( c_1 \) and \( c_2 \) should be zero. According to the Y matrix, \( c_{12} \) is therefore related to the characteristic impedance of the balun.

Study the static capacitance of the balun will help us to gain a better understanding on the behavior the balun. Through adjusting the capacitance \( c_1 \), \( c_2 \) and \( c_{12} \), the trajectories of the fundamental and second harmonic reflection coefficient are illustrated in Figure 4.5.

The coupling between inner and outer conductor \( c_{12} \) will affect characteristic impedance. Therefore in Figure 4.5(a), the fundamental impedance now is no longer in the right position as in Figure 4.3. According to the Y matrix depicted in (4.1), it can be concluded that increasing \( c_{12} \) means decreasing the characteristic impedance of the balun. Observing Figure 4.5(b) and (c), one can see that \( c_1 \) has less impact on the behavior of the impedance than \( c_2 \). In Figure 4.5 (b) fundamental impedance is getting smaller and the harmonic reflection coefficient is no long align on top of each other.
for the push and pull branch. However, in Figure 4.5(c), the harmonic reflection coefficient barely changes while the fundamental impedances for the balanced port change to unequal. This can be explained by structure of the balun: for the coaxial base structure or any other structure that is equivalent, the coupling between inner and ground is mostly shielded by the outer, therefore the existence of $c_2$ can be neglected.

Moreover, if adjust $c_1$ and $c_2$ equally at the same time, the response of this matching network is plotted in Figure 4.5(d). Now both fundamental and even harmonic impedances are not the same and separated due to the coupling capacitance to ground.

Figure 4.5 Reflection coefficient of admittance matrix based balun while changing $c_1$, $c_2$, $c_{12}$ separately.
4.2 Coaxial Cable Configuration

In the discussion of an ideal balun, the coaxial cable is used as the equivalent simplified structure. One important assumption is $c_1 = c_2 = 0$. However, it is not always the case in a practical design.

The Static Capacitance Matrix

For a coax, since the inner conductor is absolutely shield by the outer sheath, there is no capacitance between the inner conductor and the ground ($c_2 = 0$). While integrating the cable into a practical circuit, usually it is placed on top of the PCB which has a metal ground plane. This action may introduce capacitance $c_1$. As such, the static capacitance distribution of a coaxial cable is illustrated in Figure 4.6.

![Figure 4.6 Static capacitance distribution of a coaxial cable](image)

The capacitance matrix for this network is given by:

$$C = \begin{bmatrix} c_1 + c_{12} & -c_{12} \\ -c_{12} & c_{12} \end{bmatrix}$$  \hspace{1cm} (4.3)

Simulated Wideband Behavior

Compared to an ideal balun, the extra capacitance $c_1$ has a negative influence on the performance. Using HFSS (high frequency structural simulator, a 3D Elector Magnetic structure simulator) combined with ADS (advanced design system, a circuit simulator), the influence is shown below. As one can notice in this more practical case in Figure 4.7(a), the fundamental impedances are no longer equal in the two branches due to the existence of $c_1$. 2nd harmonic impedance now is not good at higher frequency.
4.3 Vertically Installed Planar Configuration

In the study of the admittance matrix based balun, it can be learned that the unequal coupling capacitance between different conductors and ground will kill the balanced performance. Therefore, a more symmetrical structure is considered. A VIP balun could solve this problem.

The Static Capacitance Matrix

This structure was first proposed by Y. Konishi in [23], it usually consist a broadside coupled line vertically installed on a microstrip line circuit. This VIP structure holds a strong coupling between the metals and less but symmetrical coupling to the ground. Figure 4.8 shows the structure that can be used as a balun.
Therefore, the capacitance matrix for this network is given by:

\[
C = \begin{bmatrix}
c_1 + c_{12} & -c_{12} \\
-c_{12} & c_2 + c_{12}
\end{bmatrix}
\]

(4.4)

Note the capacitance \(c_1\) and \(c_2\) here are equal and relatively small compared to \(c_{12}\).

**Simulated Wideband Behavior**

To make the VIP balun usable in a practical PA design, capacitance \(c_1\) and \(c_2\) should be reduced to minimum values. Figure 4.9(a) shows the improved structure, which takes out the ground plane underneath the VIP balun. Use the same setup as in Figure 4.7(a), the simulated behavior is in Figure 4.9(b):
Observing Figure 4.5(b) and comparing with Figure 4.9(b), it can be seen that the capacitance \( c_1 \) and \( c_2 \) in the VIP structure are small but still effective and they will cause unequal impedances at the balanced port. In a push-pull design, the unequal impedance in the two branches will degrade the high bandwidth performance and cause unknown resonance. Furthermore, in an even real design, the connection between matching network and the vertical balun is very critical. For example, in a low impedance level PA design, the \( \lambda/8 \) transmission line that provide even harmonic short could be very wide compared to the signal input of the VIP balun. The signal transition from the microstrip line to the VIP balun can be no longer ignored and will appear as a parasitic series inductance. Consequently, an overall “layout” optimization of the matching network and the balun is necessary which will complicate the design procedure.

### 4.4 Suspended Planar Stripline Configuration

Both coaxial cable based balun and VIP balun have the drawbacks of too many capacitances to ground. Therefore another structure is proposed.

#### The Static Capacitance Matrix

The balun is a broadside stripline-like balun as shown in Figure 4.10.

\[
\begin{bmatrix}
c_1 + c_{12} & -c_{12} \\
-c_{12} & c_2 + c_{12}
\end{bmatrix}
\]  

(4.5)

This structure basically is the planar equivalent of the coaxial cable balun. Here the top conductor capacitance to ground is shielded by the bottom conductor (\( c_2 \approx 0 \)). This structure has the advantage of a more straightforward connection pattern while connecting the balun to the matching network to provide even harmonic short
circuited conditions at the transistor reference plane. It is also compatible with mass production at low cost.

From previous section it is known that an ideal balun needs $c_1 = c_2 = 0$. To make the planar balun usable in a practical PA design we need to approximate this condition. This can be done by making ground as far as possible from the stripline in the balun to reduce their capacitance to ground (mainly $c_1$, since $c_2$ is shielded by the bottom conductor). In a real design, the balun is fabricated on a substrate that has a top layer and a bottom layer as the ground plane. On the ground plane, remove the part that is close to the bottom conductor of the balun so that the capacitance $c_1$ is reduced. The distance from the edge of the bottom conductor to the ground edge $d$ is inverse proportional to the capacitance $c_1$. Since the matching network is fabricated on the top layer, which means the signal that flowing into the bottom conductor need to be connected from the top layer through vias to the bottom ground plane. The connection pattern is illustrated in Figure 4.11.

![Figure 4.11 Practical implementation of a suspended planar stripline balun](image)
Simulated Wideband Behavior

Use the same simulation setup as before, the simulated behavior is obtained in Figure 4.12.

![Figure 4.12 Reflection coefficient of a planar balun at fundamental and 2\textsuperscript{nd} harmonic frequency](image)

Compare to the VIP balun, it is obvious that in Figure 4.12 the behavior of the even harmonic terminations has been significant improved. Note that the fundamental impedance is still not perfect, that is mainly due to the extra metal and vias which connect the top layer and the bottom ground plane. Such pattern will add extra inductance and cause the asymmetrical in each branch. Through simulation, we know that the balun is very sensitive to the connection layout. Therefore, later in the Doherty PA design, compensation is made to absorb this inductance into the matching network.

4.5 Conclusion

In this chapter, the behavior of ideal transmission line balun is explored. Through analysis, it is shown that wideband fundamental and even harmonic control is feasible. By inserting a $\lambda/8$ transmission line, such a balun can provide a 2\textsuperscript{nd} harmonic short at design frequency at very lower impedance levels. This structure is very attractive in higher power level PA design. Three practical balun structures were discussed. The coaxial cable has the advantage of less inner capacitance to ground, but it cannot handle higher power level due to its complicated and sensitive
connection with the matching networks. The connections will introduce unpredictable behavior in practical realizations. The VIP structure has balanced parasitic capacitances to the ground. However, these small capacitances will still corrupt the even harmonic short behavior. Another drawback of this structure is the inductive connection between the microstrip line and the vertical installed transmission line will cause a narrow band behavior. Next, a planar balun is proposed. This planar structure improves the even harmonic impedance short but introduces some asymmetry in the fundamental signal path due to the topology itself. A method that can compensate the asymmetry is introduced later in Chapter 6.
A practical DPA design using NXP’s GaN transistors will be performed based on the introduced efficiency and bandwidth enhancement techniques. In this chapter, several coaxial cables are employed in the DPA as power combiners. The DPA is designed for a broadband operation from 470MHz to 810MHz to support broadcasting applications. Simulation of the key performance will be shown later to demonstrate the improvements.

5.1 Device Model and Characterization

GaN HEMTs (high-electron-mobility transistor) have been offered commercially since 2006, and are finding their way into various wireless infrastructure applications due to their high efficiency and high voltage operation [24]. In this project, NXP GaN CLTC5010 is used. The typical supply voltage of this device is 50V. The gate width is 7.2mm for a power handling ability of 160W per device. The DC transfer characteristic of this device is shown in Figure 5.1.

![Figure 5.1 DC transfer characteristic of NXP GaN CLTC5010](image)

The DC transfer characteristic shows that if $V_{DD}=50V$, the threshold voltage is -2.2V. In this design, devices are chosen to be operated in Class B, therefore the gate voltage is selected as -2.2V when $I_{DQ}$ is around 68mA.
5.2 Design of DPA

This section discusses the design procedure of a differential DPA. Since a common characteristic impedance of a coax cable is 50Ω, this value will be the impedance for the inverter. As such a 200W DPA with 50V supply voltage will be designed with a fundamental load impedance of 25Ω. In this design, the center frequency is 650MHz. For the desired wideband behavior, the bandwidth should not be less than 350MHz. The actual circuit of the PA is fabricated on Roger RO4350B substrate with a thickness of 0.762mm.

5.2.1 Output Matching Network

The simplified output matching network with a combination of those bandwidth improve techniques is illustrated in Figure 5.2.

![Figure 5.2 Simplified differential DPA using coaxial cable based baluns](image)

In Figure 5.2, the balun and transmission line in the output matching network for the main device will form the λ/4 impedance inverter (green box). For the peak devices, the 50Ω QWTL, the coax together with the λ/8 TL (red box) will boost the load impedance close to 50Ω in a wideband fashion at power back-off as we discussed in Chapter 3. By doing so, as analyzed before, each device will still be loaded by a 25Ω resistor at fundamental frequency. At the 2nd harmonic frequency, the open termination at the balun’s balanced port will be transformed into a “wideband” short.

To make the design more realistic, technique mentioned in Section 3.1 are used. The output capacitance and bondwires will be absorbed into the inverter to extend the
achievable bandwidth with practical devices. The structure now becomes as in Figure 5.3:

\[
Z_{\text{new}}, E_{\text{new}} Z_0, \lambda/8
\]

\[
Z_0, \lambda/4
\]

\[
RL
\]

\[
\text{Main Device}
\]

\[
\text{Peak Device}
\]

Figure 5.3 A differential DPA output network which absorbs the output capacitance of the devices as well as the bond-wires into the quasi-lumped transmission line inverter

5.2.2 Input Matching Network

Traditionally, a QWTL is used in the input biasing network to provide a good second harmonic short termination. By doing so and without any further action, these bias lines will limit the achievable bandwidth performance (Figure 3.7(b)). To avoid this situation, the proposed wideband balun structure including 2nd harmonic control is going to replace this traditional technique. The resulting structure is shown in Figure 5.4.

Figure 5.4 A 200W GaN DPA with input and output matching networks
Note that the matching network at the input is a low-Q network, which provides a conjugate matched condition to the input of the device. To avoid bandwidth limitations and precisely control the amplitude and phase of the input signal, the power splitter that used in conventional design is abandoned and the multi-input amplifier is driven by a mixed-signal approach.

### 5.3 Coax Balun Design

For the ideal balun, the discussion is based on the assumption that the inner and the outer sheath of the cable are directly connected to the matching networks which are fabricated on the PCB. In a practical PA design, especially in the differential structure which is discussed in previous chapters, the inner conductor of the coax usually need to be extended and soldered on the pull device’s matching network, while the outer is soldered on the push device’s matching network. The extra wire lengths introduce a lot of inductance. Moreover, the connecting pattern of the solder may cause uncertainty. Even more important is the undesired capacitance from the outer conductor to ground which will yield asymmetry in the electrical loading. Therefore the impedance of the single coaxial cable is no longer the desired value as depicted in Figure 4.7(b). To reduce the asymmetrical impedance behavior at the fundamental frequency, a dummy coax is placed [25]. The related layout and its frequency response are in Figure 5.5.

Due to the dummy coax, the coupling capacitance between the sheath and the ground is becoming more symmetrical in the push-pull structure. Therefore, the fundamental impedance offered to the two branches is getting close as seen from Figure 5.5 (b) or (c). However, the characteristic impedance of the balun is almost two times larger than the intended value at center frequency (Figure 5.5(c)). This increased characteristic impedance of the inverter will cause the transformation of the load impedance increased to a larger value, which will reduce the output power. The phase variation in Figure 5.5(d) also shows a narrow band behavior (BW_{0.1}=23%).
5.4 Layout and Simulation Results

The overall layout of the 200W DPA is shown in Figure 5.6.

Figure 5.6 Overall Layout of the 200W DPA
**Drain Efficiency**

With all the matching networks, stabilization networks, all SMD components and substrate-dependent models employed the simulation is performed. As seen from Figure 5.7, the efficiency is 51.3 % at 6dB back-off from the maximum output power. The maximum output power is 51.5dBm with 62.7 % as the drain efficiency. The designed maximum output power should be 53dBm, so clearly there is 1.5dB loss of the output power. This loss is caused by the loss in the microstrip matching network and the improper behavior of the coax balun. Since the balun has larger characteristic impedance, as an impedance inverter, it will invert the load impedance to a higher value than intended, which will cause the drop in output power.

![Figure 5.7 Drain Efficiency of the 200W DPA at center frequency](image)

**Transducer Power Gain**

The transducer power gain of the DPA is simulated and plotted versus output power in Figure 5.8. Note that the gain variation versus the output power is flat when the DPA is operating below the power back-off level. The compressed characteristic of the gain with respect to the overall input power can be observed beyond the back-off point.

![Figure 5.8 Simulated gain vs. output power at center frequency](image)
Bandwidth performance

To explore the operating classes of each device in this design, recall the expressions of continuous classes in Chapter 2. A comparison of loading conditions between the Class J-B-J* continuous classes and this DPA design is illustrated in Figure 5.9. The load impedance for DPA is extract from the internal point of the PA devices. In this figure, it is obvious that the variation of real fundamental impedance doesn’t meet the condition of continuous wideband requirement especially at power back-off which is represented by red dashed line. The fundamental impedance will change the load modulation in the DPA operation although the 2\textsuperscript{nd} harmonic is very close to a continuous loading condition. Therefore the bandwidth is pretty narrow which can be concluded from Figure 5.10 as well.

![Figure 5.9 Comparison of continuous classes and a 200W DPA operation for fundamental and 2\textsuperscript{nd} harmonic impedance at both full power and power back-off level](image)
In Figure 5.10(a) the simulated efficiencies at full power and 6dB back-off level are plotted. Clearly, at full power level the bandwidth is relatively large, despite the drop at high frequency. The bandwidth limitation occurs at the power back-off level which is the same with the conclusion from Figure 5.9. At 6dB power back-off level, the bandwidth is 170MHz, the fractional bandwidth is $BW_{10\%} \approx \frac{170\text{MHz}}{650\text{MHz}} = 26\%$. The narrow band behavior is mainly caused by the coaxial cable based impedance inverter. It is already known from Figure 5.5 that the impedance response of the output matching network is higher than intended value, hence the fundamental loading condition seen by the PA devices through the coax is changed. Consequently, the output power will be reduced due to the dramatically increased fundamental load resistance. Hence in power back-off level, the efficiency, output power and gain all appeared as narrow-band behavior (Figure 5.10 (a), (b) and (c)). Observing Figure 5.10 (e) and (f) is another way to evaluate the wideband performance. In this case, the magnitude of loading impedance at full power should be $25\Omega$ and around $50\Omega$ at back-off. The phase variation should between 0.9 and 1 within the bandwidth from 450MHz to 800MHz.
Figure 5.10 Simulation results of the 200W DPA at full power and power back-off level

(a) Output power vs. frequency;
(b) Efficiency vs. frequency;
(c) Magnitude of impedance vs. frequency;
(d) Phase of the impedance vs. frequency;
(e) Transducer gain vs. frequency;
(f) Fundamental and 2nd harmonics reflection coefficient vs. frequency
5.5 Conclusion

In a wideband DPA design, the matching network should include the following techniques: absorbing the output parasitic, including a wideband combiner, having the balun structure which will provide the even harmonic short without affecting the bandwidth. In this chapter, a design example that integrated all of the above mentioned techniques is given. This 200W GaN differential DPA design uses coaxial cables as power combiner and balun. Although the simulation results are good at full power, there are some known drawbacks. Most of the problems are caused by the practical implementation of the coaxial cable, which imperfections have been included in the simulation. To be more specific, the use of coaxial cables introduces extra inductances and capacitances, which will cause asymmetrical and improper impedance transformation. Therefore, a new balun structure is desired in the DPA design.
A 1kW LDMOS DPA Using the Planar Balun

In Chapter 5, it is concluded that using coaxial cable as the power combiner has some serious drawbacks. As is already discussed in Chapter 4, a suspended planar balun can have some benefits over a coax implementation and for this reason will be used within this chapter for the design of a high power DPA. The novel planar balun introduced in this thesis has the advantage of easy adjustment to any desired characteristic impedance which is highly beneficial when aiming for very low impedance levels. In the DPA of this chapter, LDMOS devices provided by NXP are used which can provide 350W of output power at an optimum load impedance of 4.4\(\Omega\).

6.1 Device Model and Characterization

LDMOS (laterally diffused metal oxide semiconductor) technology is a high voltage version of the famous CMOS (complementary metal oxide semiconductor) technology. Its drain-source breakdown voltage can be above 60V, which makes it very suitable for building high power amplifiers. Its good performance and relatively low cost compared to other technologies making it the most popular technology for base station applications within the low Giga-Hertz frequency operation [26].

In support of this design, NXP has provided the LDMOS model in Agilent’s Advanced Design System. The model number is BLF884P. This type of devices is suitable for broadcast transmitter applications and industrial applications [27]. To verify the proposed wideband balun structure and conclude of better results are possible with this structure, again, a differential two-way symmetrical DPA will be designed and implemented for a broadband operation from 450MHz to 810MHz.

The DC transfer characteristic of this device is shown in Figure 6.1. It shows that if \(V_{\text{DD}}=50\text{V}\), the threshold voltage is around 2.6V. For a Class B operation, the gate
voltage is selected as 2.6V when $I_{DQ}$ is around 51.4mA. The output capacitance of the LDMOS is much larger than that of a GaN transistor. When using the equation based device model with $V_{GS} = 2.6V$ and $V_{DS} = 50V$, the output capacitance is 31pF.

![Figure 6.1 DC transfer characteristic of LDMOS BLF884P and output capacitance as a function of drain voltage](image)

6.2 Design of DPA

Because of the low impedance level in this design and the nature of the novel broadside coupled balun, a very thin substrate with higher dielectric constant will be used. Most parts of the design will be fabricated on Roger RO3006 with the thickness of 10mil.

Here we following the same procedure as depicted in section 5.2. The only problem is the large output capacitance, which is very difficult to be absorbed into the matching network. However, from equation (3.5), we know that the lower the impedance $Z_0$, the easier to absorb the $C_{dev}$. Since in this particular differential design, $Z_0 = 4.4\Omega$, the frequency limitation will achieve to $f = \frac{(C_{dev}Z_0)^{-1}}{2\pi} \approx 1$ GHz, which is beyond the bandwidth.

6.2.1 Output Matching Network

The balun is an important part of the output matching network. As has been discussed before, the planar balun itself has asymmetrical response at both fundamental and 2nd harmonic signal. Hence there are two steps to compensate the asymmetry.

The first step is using a modified metal block. From Chapter 4, it is known that the capacitance $c_1$ and $c_2$ should be as small as possible to get a good balun behavior. Therefore, the topology of the balun is described in Figure 4.11. The ground near the
balun is relatively far from the edge of the top and bottom metal. However, a PA is usually implemented on a heat sink and this heat sink will enlarge the capacitance $c_1$ and $c_2$. To reduce the effect of $c_1$ and $c_2$, a metal block is fabricated with a hole where the balun will be located on top. Figure 6.2 sketched the pattern of the metal block with a planar balun installed on top of it. With the hole, capacitance $c_2$ is reduced. It is a common knowledge that in first order approximation the coupling capacitance is inversely proportional to the distance between the metal layer and surface of metal block $d$: $C = \frac{\varepsilon_0 \varepsilon_r A}{d}$ where $d$ is the distance from the edge of the coupled line to ground, $A$ is the area of the top or the bottom metal layer in the balun. Through simulation, it is known that as long as the capacitance is smaller than 0.5 pF, the performance of the balun is acceptable. $A$ is impedance dependent and in this case, is fixed. Therefore, $d$ should be not smaller than $\frac{\varepsilon_0 \varepsilon_r A}{0.5 \times 10^{-12}} = 0.3$ mm. If we choose a simple number 5mm for $d$, the capacitance is very small and can be neglected.

The second step is to make the transmission line inserted before the balanced port asymmetrical in order to compensate the unbalanced response in the balun, which means the characteristic impedances of these lines ($Z_1$ and $Z_2$ in Figure 6.3) are not equal. Moreover, these transmission lines will be implemented in the fashion of a quasi-$\lambda/8$ TL as shown in Figure 6.3.
Since the output capacitance is so big, absorbing it into the transmission line is not enough, further compensation will be made using lumped components as shown in Figure 6.3. Also here $C_{\text{comp}1}$ and $C_{\text{comp}2}$ are not necessarily equal because of the intrinsic asymmetry in the planar balun. $C_{\text{comp}3}$ can be tunable since this has less impact on the performance. $L_{\text{comp}}$ is made to get the 2nd harmonic right. In the simulation, the $C_{\text{dev}}$ and package parasitic are extracted from the device model and approximated by a network with linear inductors and capacitors. Matching networks together with the planar balun are simulated in HFSS. The impedance versus frequency response before and after asymmetrical compensation is shown in Figure 6.4. Before compensation, the 2nd harmonic is not zero at the center frequency. Moreover, the magnitude of fundamental impedance is not symmetrical in the band. This will cause the bandwidth shift during load modulation. It can be concluded that after the compensation, in Figure 6.4(b), for the fundamental signal, the impedance is more balanced and equal. Furthermore, the second harmonic impedance is closer to the simulation with ideal balun.

The matching network for the peak device is the same. The complete networks at output can be designed the same as depicted in Figure 5.3.
Figure 6.4 Comparison of Impedance with ideal balun and HFSS simulated planar balun

(a) Before compensation

(b) After compensation
To match the optimum load impedance to an external 50Ω load, multi-section TL network will be chosen since it is broader in bandwidth than the single TL case. However, the thin substrate that is used in the balun to have better coupling here loses its advantage at higher impedance levels. At higher output power levels, the transmission lines close to the 50Ω termination become too thin to handle high power. As such the multi-section network becomes too lossy. Thus in the later sections of the multi-TL network, a substrate of 25mil thick is used to reduce the losses. To make the two different substrates easy to joint, the width of the microstrip line at the connection point is made equal. A performance comparison of two networks with different substrate is illustrated below in Figure 6.5. It is obvious that with thicker substrate, the insertion loss is lower.

![Figure 6.5 Multi-section quarter wavelength impedance transformer with their insertion loss when using a single thin substrate (10mil) or when using two different substrate thickness (10mil and 25mil)](image-url)
6.2.2 Input Matching Network

Here we use the same topology as in Figure 5.4. The driving profile here for the PA is also mixed-signal based to enhance the bandwidth by precise control of magnitude and phase. Note that there is no stub for implementing the 2\textsuperscript{nd} harmonic short or providing biasing voltage, therefore in this design all biasing will be supplied through choke inductors. The value of the choke should be chosen such that it does not resonate with the input or output capacitance of the device. Its current handling capability should be taken into consideration as well.

6.3 Layout and Simulation Results

In Figure 6.6, the yellow area is based on the substrate of 10mil thickness. The green part is with 25mil substrate.

![Figure 6.6 Overall layout of the 1kW DPA](image)

By following the aforementioned design procedure, initial design parameters are obtained. After that an optimization is done including all matching networks, SMD components and other substrate-dependent models. The balun has been simulated in HFSS due to its 3D nature, which the remainder of the circuit has been computed using Momentum. The results are listed below.
Drain Efficiency & Power Added Efficiency

The estimated drain efficiency is 64 % at 6dB back-off from the maximum output power in Figure 6.7. The maximum output power is 59.47dBm with 70% drain efficiency. The power added efficiency (PAE), which is a more realistic measure of this amplifier since it also includes the input power that is delivered into the amplifier is 63.3% at maximum output power and 56% at back-off. There is about 0.5dB loss of output power generated by the active devices mainly caused by the loss in the microstrip matching network.

![Figure 6.7 Efficiency of the 1kW DPA at center frequency](image)

(a) Drain efficiency; (b) PAE

Transducer Power Gain

The transducer power gain of the 1kW DPA is simulated and plotted versus output power in Figure 6.8. Note that the gain variation versus the output power is flat when the DPA is operating below the power back-off level. The gain compression can be observed when the peaking device is active.

![Figure 6.8 Simulated transducer power gain vs. output power](image)
Bandwidth performance

To better understand the wideband capabilities, a comparison of the loading conditions offered to the active devices with the continuous amplifier classes has been made. From Figure 6.9, it is clear that at both full power and power back-off, the DPA loading conditions indeed approximate the optimum loading trajectories for the continuous J-B-J* class operation.

The bandwidth performance of the total circuit is plotted in Figure 6.10. From Figure 6.10(a), it can be conclude that at full power level there are no real bandwidth limitations, $BW_{10\%}=50\%$. The bandwidth limitation is presented at two power back-off level. At 6dB power back-off, the bandwidth is $770\text{MHz}−450\text{MHz} = 320\text{MHz}$, $BW_{10\%}=49\%$. At 8dB power back-off, the bandwidth is $800\text{MHz}−500\text{MHz}=300\text{MHz}$, $BW_{10\%}=46\%$. At high frequency, the output power is dropped as in Figure 6.10(b). This is due to the impedance variation at high frequency as can be seen from
Figure 6.10 Simulation results of the 1kW DPA at full power and back-off level
(a) Output power vs. frequency;
(b) Efficiency vs. frequency;
(c) Magnitude of impedance vs. frequency;
(d) Phase of the impedance vs. frequency;
(e) Transducer gain vs. frequency;
(f) Fundamental and 2nd harmonics reflection coefficient vs. frequency
Figure 6.10(c). The planar balun provides unequal transformations for the impedance but it is still in an acceptable range. In Figure 6.10(f), the phase variation, however, shows a nice wideband behavior. The gain versus frequency is plotted in Figure 6.10(c). About 2dB compression occurs at full power level compared to back-off power operation. In Figure 6.10(d), the second harmonic at high frequency is shown close to a short termination. At the whole frequency band, the bandwidth shows a continuous Class J-B-J* operation since the 2nd harmonic load now is either inductive or capacitive.

6.4 Conclusion

This chapter introduces a wideband 1kW DPA which absorbs the output capacitance into the planar balun based impedance inverter. Based on the theory discussed previously, the quasi-$\lambda/8$ TL is modified to improve the efficiency bandwidth. In this DPA design, the drain of the push and pull devices do not experience an identical loading impedance. The main reason is the asymmetrical behavior of the planar balun itself. By introducing asymmetry in an opposite way, such as adding capacitors or inductors and making the connecting matching network asymmetrical, the performance can be improved. Simulation results show a notable bandwidth improvement at both full power and power back off.
Conclusion and Future Work

7.1 Conclusion

This project aims to develop wideband DPA design solutions for broadcast applications.

In this thesis, first the conventional Class A/AB/B/C/J amplifier operations with their inverse counter parts have been reviewed. Next a detailed analysis was given for ideal 2-way DPA operation, followed by a bandwidth analysis of all currently known DPA topologies of DPAs. From this analysis it was shown that the bandwidth is most restricted in power back-off operation when the peak amplifier is off. Moreover, it has been also concluded that higher bandwidths seems to be possible using 3-way and 4-way DPA topologies while (a)symmetrical two-way DPA configurations seems to be most restricted in their bandwidth performance.

Traditional (two-way) Doherty PAs are considered inherently narrowband due to the QWTL used in output power combing network, which provides only perfect impedance inversion at specific frequency. Although this impedance inverter is widely blamed as a limit factor for bandwidth, in Chapter 3, another factor that significantly constrains the achievable bandwidth has been discussed, namely the output capacitance of the PA devices. Therefore, theory / design methods that allow compensation of this capacitance in the DPA design are discussed. Using such an approach the impact of the output capacitance can be relaxed, pointing the attention back again on the frequency behavior of the impedance inverter. In view of this, a novel wideband power combiner/impedance inverter scheme has been introduced in [8]. This structure has the capability to keep the load impedance more or less constant in a wideband manner at power back-off operation. Close inspection revealed however, that the 2nd harmonic control is essential in the DPA operation to maintain
high efficiency over the frequency band of interest. Conventional design methods aiming for such a harmonic termination using a quarter wavelength transmission line are too much restricted in their bandwidth. To implement both fundamental and proper second harmonic termination in a wideband fashion, more design freedom is needed. Therefore a novel wideband DPA configuration has been introduced, which utilizes a push-pull structure. The push-pull topology in combination with proper input and output baluns can provide orthogonal design relations between the fundamental and 2nd harmonic path, as such providing the design flexibility to solve bandwidth limitation.

In Chapter 4 a very critical part of a differential DPA design is described, which is the balun. As such a wideband balun with 2nd harmonic control method is proposed firstly. After analyzing the DPA network with a model of an ideal balun, three practical balun structures are discussed. The classical coaxial cable based balun provides the advantage of an absolutely zero coupling capacitance from inner conductor to the ground. However, in a practical design, the always present capacitance of the outer conductor to the ground cannot be ignored, since it affects the balun performance a lot. This non-zero capacitance will allow common mode signals to flow, which superimposed on the differential signals causes unequal loading conditions, while the open circuit condition for the 2nd harmonic gets violated. In view of this a Vertical Installed Planar (VIP) balun structure with removed ground plane has less capacitance to ground and a more balanced response. However, the connection between the microstrip line and the 3D structure introduces large parasitic inductances, which destroy the desired performance. Finally, a suspended planar stripline-like configuration is proposed. This structure is more suitable for mass production and has a better response at fundamental and 2nd harmonic frequency, when properly compensated.

Based on aforementioned techniques and topologies, a step-by-step introduced wideband 200W GaN DPA using mixed-signal input drive is provided in Chapter 5. In this particular design the impedance inverter in the PA is realized with coaxial cable based balun. The simulated results show good efficiency performances at maximum output power level from 450MHz to 750MHz and a rather big efficiency
CONCLUSION

degradation from 750MHz to 810MHz. At power back-off, the performance is even worse and only has 26% fractional bandwidth at $\text{BW}_{10\%}$ seem to be achievable. Furthermore, since the mixed-signal input drive is still used in this DPA, it is not directly applicable for the commercial applications.

In Chapter 6, a DPA design using NXP’s Gen7 350W LDMOS devices and the novel planar balun is introduced. Analysis shows that this impedance inverter has a better performance than the coaxial cable. From simulations it is also known that the planar balun has asymmetrical response due to the connection pattern from the microstrip line matching network to the DPA core structure. Hence the compensation for asymmetry should be made in the matching network by adding capacitors, inductors and adjust the characteristic impedance and physical length of the TL at the appropriate places. The simulated performances of the two designs are summarized in Table 7.1.

<table>
<thead>
<tr>
<th>Parameters</th>
<th>Design I 200W GaN DPA</th>
<th>Design II 1kW LDMOS DPA</th>
</tr>
</thead>
<tbody>
<tr>
<td>Drain Efficiency@ $P_{\text{max}}$</td>
<td>&gt;60%</td>
<td>~70%</td>
</tr>
<tr>
<td>Drain Efficiency@ $P_{6\text{dB back-off}}$</td>
<td>~40%</td>
<td>&gt;60%</td>
</tr>
<tr>
<td>PAE@ $P_{6\text{dB back-off}}$</td>
<td>~40%</td>
<td>&gt;60%</td>
</tr>
<tr>
<td>PAE@ $P_{8\text{dB back-off}}$</td>
<td>~40%</td>
<td>~50%</td>
</tr>
<tr>
<td>Gain</td>
<td>18dB</td>
<td>15-18dB</td>
</tr>
<tr>
<td>$P_{\text{out, max}}$</td>
<td>51.5-52dBm</td>
<td>58-59dBm</td>
</tr>
<tr>
<td>Bandwidth @ $P_{\text{max}}$</td>
<td>450-750MHz</td>
<td>460-810MHz</td>
</tr>
<tr>
<td>Bandwidth @ $P_{6\text{dB back-off}}$</td>
<td>530-700MHz</td>
<td>460-790MHz</td>
</tr>
<tr>
<td>Bandwidth @ $P_{8\text{dB back-off}}$</td>
<td>N/A</td>
<td>470-800MHz</td>
</tr>
</tbody>
</table>

It should be noted that the second design was not optimized to its full potential. The designs now are still in the measurement phase. The simulated results are compared to the state-of-the-art Doherty power amplifiers published in the recent literatures. The comparison is given in Table 7.2. As can be seen from the table, the proposed design has the highest fractional $\text{BW}_{10\%}$ (50.7%) and gain (15-18dB) compared to others. However, considering certain losses in the real implementation, those numbers should be degraded. This design uses an LDMOS device which has lower mobility and
slightly higher losses compared to GaN device. The high gain of this amplifier helps to improve the PAE and bring it much closer to its competition.

<table>
<thead>
<tr>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>Technology</td>
<td>LDMOS</td>
<td>GaN</td>
<td>GaN</td>
<td>LDMOS</td>
</tr>
<tr>
<td>DE</td>
<td>&gt;60%</td>
<td>~55%</td>
<td>&gt;65%</td>
<td>45%</td>
</tr>
<tr>
<td>PAE</td>
<td>&gt;60%</td>
<td>~40%</td>
<td>&gt;50%</td>
<td>N/A</td>
</tr>
<tr>
<td>Bandwidth</td>
<td>460-810MHz</td>
<td>1.5-2.4GHz</td>
<td>1.7-2.25GHz</td>
<td>2.25-2.55GHz</td>
</tr>
<tr>
<td>Fractional BW_{10%}</td>
<td>50.7%</td>
<td>41.8%</td>
<td>25.6%</td>
<td>12.5%</td>
</tr>
<tr>
<td>Fractional BW_{3%}</td>
<td>50%</td>
<td>28%**</td>
<td>N/A</td>
<td>1%**</td>
</tr>
<tr>
<td>Gain</td>
<td>15-18dB</td>
<td>8-12dB</td>
<td>N/A</td>
<td>14dB</td>
</tr>
<tr>
<td>P_{max}</td>
<td>58-59dBm</td>
<td>42dBm</td>
<td>48.2-49.6dBm</td>
<td>50dBm</td>
</tr>
<tr>
<td>Topology</td>
<td>Differential 2-way</td>
<td>2-way Sym.</td>
<td>2-way</td>
<td>2-way</td>
</tr>
<tr>
<td>Level of implementation</td>
<td>Simulated*</td>
<td>Hardware</td>
<td>Hardware</td>
<td>Hardware</td>
</tr>
</tbody>
</table>

* Hardware implemented, measurement same in the process
** Read from the plot

7.2 Recommendation and Future Work

There are a few recommendations which can add further values to this design. They are as follows:

Optimization in the design of the planar balun

Since the second design was not optimized to its full potential, more work are need to integrate the output matching networks and the planar balun. The optimization could include the dimension of the broadsided structure and the structure of the metal block. It is also known that LDMOS has larger output capacitance than GaN which is very difficult to be absorbed. Therefore, the use of the planar balun in a GaN DPA design should be more straightforward.

Linearization and Mixed-Signal Input Drive

Efficiency and bandwidth is the first consideration in this thesis. The simulation results in Chapter 4 have shown the strong compression in the gain of the DPA. Therefore, linearization has to be applied to the DPA. For base-station applications
the digital pre-distortion (DPD) is becoming the most important linearization technique. Note that in both designs the amplitude and phase of the signal in main and peaking devices are important not only for efficiency but also for bandwidth. In the simulation the input of main and peak amplifier are driven with two separate input signals, as such each phase can be adjusted easily. For a complex wideband modulated RF signal it will be more difficult to optimize the phase shift [16]. So far, implementing an input power splitter that can provide the required power and phase relations while keeping the main and peaking devices isolated from each other is still a big design challenge, which gives new opportunities to future research.
Appendix

The Static Capacitance Matrix of a 2N-port Network

Figure A.1 2N-port network with admittance matrix $Y$

From[22], a $N \times N$ admittance matrix $Y$ can be defined to represent a 2N ports network in Figure A.1 that contains $N+1$ parallel coupled lines:

$$Y = \frac{1}{\eta_0 S} \begin{bmatrix} C & -\sqrt{1 - S^2} \cdot C \\ -\sqrt{1 - S^2} \cdot C & \frac{1}{C} \end{bmatrix}$$

Where:

- $C$ = the $2 \times 2$ normalized static capacitance matrix with elements $c$;
- $c = \frac{c^{'}}{\varepsilon}$ = ratio of the static capacitance between conductor per unit length to the permittivity of the medium (this ratio is independent of the dielectric medium and depends only on cross-section geometry). This dimensionless ratio is convenient for practical use with available design data;
- $\eta_0 = \sqrt{\frac{\mu_0}{\varepsilon_0}} = 376.6 \ \Omega$, the impedance of free space;
- $S = j \tan \theta$;
\[ \theta = \frac{\pi \omega}{2 \omega_0}, \text{ where } \omega_0 \text{ is the center frequency for which the transmission lines are a quarter wavelength.} \]

Where,

\[ C = \begin{bmatrix} c_1 + c_{12} & -c_{12} \\ -c_{12} & c_1 + c_{12} \end{bmatrix} \]

With the Y matrix, the ratio of the static capacitance between conductors per unit length to the permittivity of the medium can be easily adjusted in simulator. Since in ideal balun, \( c_1 \) and \( c_2 \) should be zero, only \( c_{12} \) will determine the characteristic impedance of the balun. By adjusting these ratios, it’s more convenient to study and mimic the balun’s behavior in simulation.

The static capacitance matrix of a four-port network with two parallel inductors can be represented by Figure A.2.

![Figure A.2 Capacitance distribution of a four-port network with two parallel conductors](image)

All the balun structures discussed in this thesis are the transformation of Figure A.2.

With this matrix, we can simulate the balun’s behavior with different capacitance ratios.

Assume a 10\( \Omega \) balun is needed, after a series of calculations, the \( c_{12} \) can be obtained by:

\[ c_{12, \text{normalized}} = \eta_0 \frac{10 \Omega}{10 \Omega} = \frac{376.7 \Omega}{10 \Omega} = 37.67 \]

Or a 2\( \Omega \) balun is wanted,

\[ c_{12, \text{normalized}} = \eta_0 \frac{2 \Omega}{2 \Omega} = \frac{376.7 \Omega}{2 \Omega} = 188.35 \]
After having the dimensionless ratio, use linecalc in ADS to get the dimensions of two metal layers. Slightly adjust the dimension to have the proper coupling capacitance or compensate the asymmetry in the future optimization.
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