Stellingen

behorende bij het proefschrift

Non-linear A/D Converters for
Integrated Silicon Smart Sensors

doors

K. M. Mahmoud
1. Notatie in modulus en argument sluit het dichtst aan bij niet-lineaire conversie in "smart" sensor toepassingen.

2. De collector-basis sperspanning, welke het laag-gedoteerde deel van de collector (de epitaxiale laag) depleteert, is een belangrijke parameter voor de beoordeling van de bipolaire transistor in analoge circuits.

3. Een uitgebreide kennis van zowel de sensorwerking als de analoge parameters en het schakelgedrag van de bipolaire transistor is noodzakelijk om de prestaties van een "smart" sensor, welke is gefabriceerd in een (gemodificeerd) bipolaar proces, te optimaliseren.

4. Een Analoog-Digitaal omzetter met redelijke resolutie (8 bit) en een groot dynamisch bereik (13 bit) is mogelijk op basis van een standaard bipolaar proces.

5. Doordat digitale circuits relatief ongevoelig zijn voor ruis, verdient het de voorkeur de quantisatie zo dicht mogelijk bij de sensor plaats te doen vinden.

6. De dotering van de epitaxiale laag beperkt de compatibiliteit van een analoge schakeling met een sensor in hogere mate dan de post-processing temperatuur.

7. Het omgeven zijn door water is een belangrijke factor bij de ontwikkeling van een land.

8. Het is een grote misvatting om het gebruik van natuurlijke bronnen te baseren op de huidige omvang in plaats van op de hersteltijd.

9. De negatieve diffusiecoëfficiënt van geld is een van de grootste problemen ooit.

10. Het aantal fouten in een manuscript neemt exponentieel af met de correctietijd; een goede auteur dient over een kleine tijdconstante te beschikken.

11. Door de werkdag vroeg te beginnen en een rust pauze in de middag te nemen, creëert men anderhalve werkdag in 24 uur.

12. Een hoge belastingdruk gecombineerd met voorzieningen voor jongeren en bejaarden beïnvloedt familierelaties negatief.
1. Floating-point representation is the most suitable non-linear conversion for smart sensor applications.

2. For transistors designed for analogue circuits the collector-base reverse voltage, which fully depletes the low doped collector region (epilayer), is an important transistor parameter.

3. An extensive knowledge of both the sensor functioning as well as the bipolar transistor characteristics is essential for the smart sensor designer in order to optimize the total sensor performance.

4. Using a standard bipolar process, it is possible to realize a medium resolution (8-bit) and a wide dynamic range (13-bit) analogue to digital converter.

5. Because of the immunity of digital circuits to noise, it is very important to digitize information as close as possible to the sensor.

6. The doping concentration of the epitaxial layer limits the compatibility between analogue circuits and sensors more than the post-processing annealing.

7. The surrounding of a country by water is one of the most important factors that help in the development of that country.

8. It is a big mistake to use natural resources based on their existing quantity rather than their recovery time.

9. The negative diffusion coefficient of money is one of the biggest problems ever to have existed.

10. The amount of errors in a manuscript decreases exponentially with correction time, the best author has the shortest time constant.

11. By starting the working day early in the morning and taking a rest at midday one can have one and a half working day in 24 hours.

12. High tax combined with the governmental financial support to the young and old has a detrimental effect on family relations.
NON-LINEAR A/D CONVERTERS FOR INTEGRATED SILICON SMART SENSORS

K. M. Mahmoud
NON-LINEAR A/D CONVERTERS FOR INTEGRATED SILICON SMART SENSORS

Niet-lineaire A/D omzetters voor smart geïntegreerde silicium sensoren

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PRINTED IN THE NETHERLANDS
To my wife

To my mother
Leden van de promotiecommissie:

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Chapter 1

Introduction

Our senses play an important role in our daily life. For this reason many
artificial counterparts to our organs of sense have been developed, and are
generally referred to as sensors.

Senses and sensors can be grouped into three main categories. The most
important use of senses and sensors, which is common to human and animals
as well as machines and instruments, is the need to detect a coming danger, so
as to be able to avoid it. For example, an engine detects that it is over-heated
and switches itself off to avoid bursting into flame.

The second use of the senses and sensors is the need to collect more in-
formation about the surrounding environment so that tasks can be accom-
plished, and in the most efficient way. When a machine or an instrument
makes use of various sensors, more information can be taken into account,
and, therefore, the performance of the machine or the instrument can be im-
proved. Two examples of sensor implementations can be found in industrial
robots and in cameras. An industrial robot can manipulate a fragile object
in an uncertain environment when equipped with a wide-range vision system,
a medium-range proximity system and a tactile imaging system. A fully au-
tomated camera gives, on average, better results than a manually adjusted
camera.

The third use of our senses is for enjoyment. Many people enjoy, for
instance, watching a football match or listening to music. In the first two
groups many sensors have been developed, and still many research projects are
focused on developing new sensors. However, there is no artificial counterpart
to the third group, the use of the senses for enjoyment.

In the sensor groups discussed above, the main function of a sensor is to
convert a physical or chemical quantity, such as light intensity, temperature,
gas flow, magnetic field intensity or pressure into another physical or chemical
quantity that is recognizable by the sensing object. Therefore, in this context, the sensor is referred to as an input transducer. Signals of interest can be grouped into six energy domains [1]. The six energy domains are electrical, thermal, mechanical, optical, chemical, and magnetic. Electrical signals are currently the most preferred signal form. Therefore, sensor research is focused on developing transducers that convert signals from one of the five other energy domains into a quantity in the electrical domain.

1.1 Advantages of Integrated Smart Sensors

An automated process consists of three functional blocks; smart sensor, computer, and actuator, as shown in Figure 1.1. [2]. Recent advances in integrated circuit fabrication technology have resulted in an improved component performance as well as the reduction of the minimum reliable component size. This made the fabrication of highly sophisticated signal processing chips possible, which led to the production of low cost small-size products.

![Figure 1.1. The three blocks of an automated process.](image)

In the last two decades, the price-performance ratio of the sensor, computer and actuator has dropped down to one-third, one-thousandth and one-tenth, respectively [2]. Therefore, recently many research projects have been focused on the sensor area. The aim is to use the well-developed micro-electronic integrated circuit technology, which made microelectronic chips inexpensive, in sensor manufacturing. Thus, mass-production of inexpensive sensors can be achieved. More important, if the sensor is fabricated by the same technology as microelectronic circuits, the sensor and the required electronics can be integrated on the same chip yielding a smart sensor.

The first block in Figure 1.1, the smart sensor (sensory system), can itself be sub-divided into four parts as is depicted in Figure 1.2. The first block represents the sensing element, which can be a resistor, capacitor, transistor, piezo-electric material, etc. The signal produced from the sensor is often influenced by noise or interference, or is of such a magnitude that it is likely to be corrupted during transmission from the sensor to the external signal processor. Therefore, signal-processing techniques such as amplification, linearization and filtering are necessary, implemented as shown in the second
1.2. Silicon as a Sensor Material

block in Figure 1.2. As mentioned above, in many cases, such as automated processes, the signal from the sensor is required in a digital format. An analogue-to-digital converter is necessary to perform this function. The last block in Figure 1.2 is a sensor-bus interface. In many applications, when a large number of sensors are required by the system [2], the number of wires required for all sensors is a problem, and therefore a sensor-bus interface is necessary.

![Diagram of sensor system]

Figure 1.2. The four parts of the smart sensor.

It is a great advantage to integrate all four parts of the sensory system in a single chip, thus obtaining a smart sensor. By the integration, the size and cost of the system can potentially be reduced. What is more important is that the quality of the signal produced from the sensor can be improved. The sensitivity to the measurand can be increased and the linearity of response, accuracy and interference immunity can be improved. This can be achieved by using on-chip amplification, linearization and compensation.

When sensors are integrated with an A/D converter and a sensor-bus interface, the amount of wiring required can be reduced. For example, an 8×8 two-dimensional tactile sensor needs about 65 wires if each sensing element has to be connected separately to an external signal processor. The number of wires can be reduced to 17 when on-chip multiplexing is implemented. By adding an A/D converter and a sensor-bus interface, the number of wires can be reduced to a simple twisted pair when a serial-bus interface is implemented [3]. Moreover, standardization of the sensor output-signal format can be achieved, which makes the maintenance of the system and replacing the smart sensor much more reliable.

1.2 Silicon as a Sensor Material

The well-established electronic properties and the good physical and mechanical properties of silicon [4] make it the most common semiconductor material.

Signal conversion in a sensor is based on energy conversion. Silicon shows many physical effects that can be used to convert a quantity from a non-electrical energy domain into the electrical domain [5]. Some examples of
physical effects that exist in silicon are: photovoltaic effect, photoconductivity, photoelectric effect, piezoresistivity, the Seebeck effect, thermoresistive effect, the Hall effect, and magnetoresistance. In the case that silicon does not show a required effect, such as piezoelectricity and magnetism, a piezoelectric or magnetic [6, 7] material can be deposited on top of the silicon to construct the required transducer.

The good mechanical properties of silicon and the advances achieved in lithography and etching made the fabrication of micro-structures in silicon possible. This opened up a new field in many microelectromechanical sensors and actuators [8, 9, 10], which find applications in fields such as accelerometers [11], tactile imaging sensors [12], and pressure sensors [13].

However, silicon is not the optimum semiconductor in every respect. The electron and hole drift mobilities at 300 K in pure, defect-free germanium (Ge) (9300 and 1900 cm$^2$/Vs, respectively) and in gallium arsenide (GaAs) (8500 and 400 cm$^2$/Vs, respectively) are equal to or higher than those values in pure, defect-free silicon (1450 and 450 cm$^2$/Vs, respectively) [14]. This permits the fabrication of Ge and GaAs semiconductor devices with better frequency responses. Gallium arsenide is a direct band-gap semiconductor material, permitting the fabrication of many electro-optical devices that cannot be made with silicon technology [15]. Devices fabricated in Ge display high junction-leakage currents due to the relatively narrow band-gap of germanium (0.67 eV).

As gallium arsenide is a compound semiconductor, GaAs purification and growth technologies are more complicated than those of silicon. The technology of pure silicon wafers production is easier than that of compound semiconductors. This has made silicon wafers available at lower price. Silicon is, therefore, the principle material used in the fabrication of most semiconductor integrated circuits, sensors and actuators.

The use of silicon in the sensor field not only makes it possible to apply the highly developed and sophisticated batch-production method of integrated circuits to the sensor field, but also makes it feasible to combine sensors and integrated circuits on a single chip. Of course, this is not without its own set of problems. These problems are discussed in Section 1.4 and chapter 5.

1.3 Non-Linear A/D Converters

In instrumentation applications, many data acquisition systems are equipped with input transducers that feature a dynamic range exceeding four decades and an inaccuracy of about 1% [16, 17, 18]. This inaccuracy does not require an A/D converter with more than 7 or 8 bits. To cover the sensor dynamic
range, a 14-bit linear A/D converter is required. The linear A/D converter requires a differential nonlinearity less than 1 LSB to maintain monotonicity. For the 14-bit fixed-point representation, the maximum absolute quantization error is about 0.006 %. This accuracy exceeds by far the sensor accuracy, and, therefore, when the signal level is represented by more than 8 bits, the least significant bits will represent an error because of the limited sensor accuracy.

Available high-resolution and fast linear A/D converters are based on precision thin-film resistor networks [19]. Laser trimming has to be used to obtain the high resolution and the wide dynamic range. Both the thin-film deposition and the laser trimming add to the complexity of the fabrication, and, therefore, to the costs. However, integrating type A/D converters, such as the dual-slope type and the charge-balance type, do not require component matching, but they are rather slow [20], especially when a high resolution and large dynamic range are the requirements. Sigma-delta converters have bandwidths that are narrower than those of a successive-approximation converter but much wider than those of a dual-slope integrator. The resolution of sigma-delta converters is higher than that of successive-approximation converters and less than that of the integrating type converters. Because of the complex digital filtering, the monolithic chips tend to be large and their power requirements high [20].

Many sensors have a wide dynamic range and limited accuracy. These sensors do not require the high-resolution linear A/D converters, which would merely add to the system’s cost. For this type of sensor, non-linear A/D conversion offers an optimal solution [21].

Many techniques have been developed to realize the non-linear relations in a non-linear A/D converter. These techniques are discussed in more detail in chapter 2.

In instrumentation applications, the most suitable non-linear A/D converter technique is based on floating-point A/D conversion. In the simplest floating-point system, the number $N$ is represented as

$$N = S \times F \times B^E$$

where $S$ is the sign of the number $N$, $F$ is the fraction (mantissa) of the number, $E$ is the exponent, and $B$ is the base of the exponent.

In digital systems, the most often used system is the binary system, therefore, the value of $B$ is chosen to be 2. The total word length, $n$, required to represent the signed number $N$ is given by

$$n = f + e + 1$$
where \( f \) is the number of bits to represent the fraction, and \( e \) is the number of bits needed to represent the exponent.

The most important parameters of the floating-point A/D converters are the dynamic range and the relative error. If the fraction is normalized to values below 1 with a maximum of \((1 - 2^{-f})\), the smallest, \( N_{\text{min}} \), and largest, \( N_{\text{max}} \), numbers are

\[
|N_{\text{min}}| = (1/2^f) \times 2^0
\]

and

\[
|N_{\text{max}}| = (1 - \frac{1}{2^f}) \times 2^{2^e-1}
\]

so the dynamic range \( D \) is

\[
D = \frac{|N_{\text{max}}|}{|N_{\text{min}}|} = (2^f - 1)2^{(2^e-1)} \approx 2^{(f+2^e-1)}.
\]

The maximum relative error \( \epsilon(N)_{\text{max}} \) is

\[
\epsilon(N)_{\text{max}} = (2^f + 1)^{-1} \approx 2^{-f}.
\]

The inaccuracy of the floating-point A/D converter is determined by the number of bits in the fraction. The dynamic range of the floating-point converter is determined mainly by the number of bits in the exponent. If we take \( f \) to be 8 bits and \( e \) to be 3 bits, the dynamic range will be about \( 2^{15} \) and the maximum relative error about \( 2^{-8} \). Therefore, floating-point A/D converters are useful in the case of sensors with a wide dynamic range and limited accuracy since the A/D converter specifications can be adjusted to match the sensor specifications.

A typical example of a smart sensor implementing the floating-point A/D converter is the smart optical sensor [3], as shown in Figure 1.3. Photodiodes typically have a wide dynamic range and limited resolution [22]. The signal from the sensor is processed and converted to a binary floating-point number.

![Figure 1.3. An optical smart sensor.](image-url)
1.4 Sensors and ICs Compatibility

In standard bipolar integrated circuits used for analogue and digital signal processing, the technological process parameters, such as the doping levels, temperature, and epitaxial layer thickness, are optimized to give high performance components for the specific function required by the integrated circuit, such as frequency range or operating reverse voltage. Since the n-p-n bipolar transistor is the most important element in bipolar integrated circuits, basically because of the higher mobility of electrons than of holes, most of the processing parameters are mainly designed to yield a high performance n-p-n transistor, with a reasonable performance of the other components such as the lateral p-n-p and JFET transistors.

The fabrication of silicon-based sensors usually follows, in some form, non-standard processing sequences [23, 24, 25]. In many cases, the standard processing steps, which are to be merged with the sensor process, may remain the same, but the impurity level, temperature, dose or energy may need to be altered to achieve an optimum sensor performance. Additional compatible processing steps must often be added during the fabrication of many sensor types [26], such as the post-processing annealing for the removal of the residual stress in surface micromachined beams and membranes [27, 28], or the deposition of piezoelectric or magnetic thin or thick [7, 29] films [30, 31, 32]. The additional processing steps required by the sensor processing can lead to a change in the parameters of the original active bipolar components and to a reduction of their performance. However, the processing constraints that are imposed by the circuit should not conflict with the operation of the sensing element.

As a part of this research, the changes in some of the low frequency parameters of the vertical n-p-n and the lateral p-n-p transistors are studied as a function of some of the technological process parameters as required by various typical sensor process [8, 25, 33]. A given initial process is assumed. The transistor parameters are studied as a function of the epitaxial layer thickness and doping concentration, as well as to an additional high temperature post-processing annealing step.

Recently, micro-machining has become an important technology in sensors and actuators. Therefore, emphasis is put on micro-mechanical devices in silicon. Two micromachining techniques are frequently employed: bulk micromachining [34, 35], and surface micromachining. In bulk micromachining, the bulk of the silicon is etched to form the desired structures [36]. Figure 1.4(a) shows a membrane formed using an electro-chemical etch-stop technique in KOH [37]. The substrate is removed over the complete wafer thickness in
the desired location which is defined by a nitride mask on the back of the wafer to form the membrane. The thickness of the membrane is equal to the epitaxial layer thickness and therefore determines the mechanical properties of the micromechanical structure such as the sensitivity and the resonance frequency [13, 35].

![Piezoresistors and Capacitance Microbridge](image)

Figure 1.4. (a) A membrane formed using electro-chemical etch-stop technique, (b) A capacitive element fabricated with surface micromachining.

Surface micromachining is based on the deposition of thin layers on the silicon substrate and the selective removal of some of these layers (the sacrificial layers) in order to obtain free-standing structural layers. Figure 1.4(b) shows schematically a capacitive element fabricated using this technique. The poly-silicon structural layers fabricated using surface micromachining usually reveal high compressive stress after deposition. These stresses can be reduced or converted into low-tensile stress by a high (≈ 1000°C for 30 min.) temperature annealing step [27, 28, 38]. This annealing step affects the bipolar elements fabricated in the same wafer.

Another typical post-processing sensor step that greatly affects the thermal budget is direct wafer-to-wafer bonding at 1100°C [39] In the research reported in this thesis, theoretical, simulation, and measurement results of some DC SPICE transistor parameters are shown as a function of the epitaxial layer thickness and doping concentration. Moreover, the changes of some of the parameters caused by high-temperature post-processing steps are investigated.
1.5 Aim of the Research

Available large dynamic range linear A/D converters are realized based on thin-film resistors [19]. The required matching accuracy is obtained by using laser trimming. Both the film deposition and the laser trimming contributes to the A/D converter cost. Another problem arises from the complexity of the process. If the A/D has to be integrated with the sensor on the same chip, the process will be more complex, if we keep in mind that the sensor might require a few extra processing steps in addition to the basic standard electronic circuit process required for the signal processing. This entails a decrease in the yield and an increase in the cost. When taking advantage of the common sensor property of wide dynamic range along with moderate accuracy, floating-point A/D converters can be combined with those sensors to reduce the total cost. The aim of this research was to design a non-linear A/D converter for smart sensor applications with a dynamic range of about 15 bits and an accuracy of 8 bits and to investigate the effect of the post-processing annealing and the epilayer thickness and doping concentration on the DC parameters of the bipolar transistor. The A/D converter should only make use of a standard bipolar process (such as DIMES-01\textsuperscript{1} [40]), and should not require any additional processing steps in order to make it simple enough for integration with many sensors based on silicon, and to reduce the total cost of the smart sensor. Additional sensor processing steps discussed above should not significantly affect the operation of the non-linear A/D converter.

1.6 Organization of the Thesis

Several techniques are used to obtain a well-defined non-linear relation required for the realization of a non-linear A/D converter. In chapter 2 an overview of non-linear A/D conversion techniques is given.

Floating-point A/D conversion is the most suitable for sensors with a wide dynamic range and limited accuracy. The relevant specifications of the floating-point A/D converters are outlined in chapter 3.

The architecture of the floating-point A/D converter built during the course of the research is based on the Successive Approximation Technique. An accurate digitally programmable current source using binary-weighted current mirrors with emitter area scaling is used as the basic D/A converter in the Successive Approximation A/D converter. The successive approximation

\textsuperscript{1}A standard bipolar process at Delft Institute of Microelectronics and Submicron Technology (DIMES).
logic was built using bipolar non-saturating gates based on Emitter Function Logic (EFL). The architecture and the different parts of the floating-point A/D converter are described in chapter 4.

Chapter 5 deals with the compatibility between integrated circuits and sensor technologies. Since the aim of many smart sensor research projects is to integrate the sensor and the required electronics on the same chip, the technologies that are used to fabricate the sensor and the electronics must be compatible. The effect of some processing parameters that are required by the sensor and that affect the bipolar transistor parameters are discussed in this chapter.

In chapter 6 the measurement results of the DC bipolar transistor characteristics are presented and compared to the simulation results. Moreover, the experimental and measurement results of the floating-point A/D converter are discussed.

Some concluding remarks, recommendations and suggestions for future research related to the work presented in this thesis are given in chapter 7.
Chapter 2

Non-Linear A/D Conversion Techniques

2.1 Introduction

Data acquisition subsystems are usually composed of an input transducer and electronic circuits which both demonstrate some degree of non-linearity. When the non-linearity is small over the required dynamic range, the sensor or circuit is referred to as linear. The deviation from the straight line is considered as a non-linearity error. However, when the non-linearity is large and originates from a well-defined relation, the sensor or circuit is referred to as non-linear. The deviations from the theoretical characteristic is referred to as the non-conformity error. Although linear circuits are widely employed, non-linear circuits find application in areas such as instrumentation [41, 42], communications [43], nuclear science [44], and control systems.

In instrumentation applications, the output of a sensor may be of a non-linear form; therefore, a non-linear circuit is required to compensate for the undesired non-linearity [13]. For example, a spectrophotometer produces an output signal [45]:

\[ e = A \exp(-\xi dc), \]

(2.1)

where \( A \) is a constant, \( \xi \) the extinction coefficient, \( d \) the optical path, and \( c \) the concentration of the unknown. If the output of the sensor, \( e \), is applied to a logarithmic circuit with the transfer function:

\[ V_o = \ln(V_i), \]

(2.2)

the measurement can be linearized for the concentration, \( c \), and is given by:
\[ c = \frac{\ln(A) - V_o}{\xi d}. \] (2.3)

A second example of non-linear circuit application in instrumentation can be found in data acquisition modules. Many data acquisition modules are equipped with input transducers with a wide dynamic range and limited accuracy. By implementing a non-linear A/D converter with those sensors, moderate accuracy requirements are imposed on the critical components in the A/D converter and, thus, a better price/performance ratio can be obtained compared to linear A/D converters.

Audio signals generally require a system with a large dynamic range (12-bit or 72dB). However, this system would not be satisfactory for telephone voice transmission because of its excessive bandwidth requirements. The ear demonstrates a logarithmic sensitivity rather than a linear sensitivity [46]; therefore, the SNR can be kept constant for optimum adaptation to human perception. The main objective in telephone systems is to obtain a satisfactory S/N ratio of about 24dB. This can be accomplished by the use of two non-linear circuits in speech communications. One for the compression of the wide dynamic range of the voice signals at the transmitter, and the other for expansion, to reconstruct the original signal at the receiver.

The compression of the voice signal dynamic range can be implemented at the source by using a logarithmic A/D converter or by first compressing the analogue signal dynamic range, and a subsequent conversion into a digital code using a linear A/D converter. The circuit performing the analogue compression is known as a compressor.

At the receiving side of the channel, the digital code can be converted into its analogue equivalent by an exponential D/A converter or by converting the digital code into an analogue signal by a linear D/A converter, and a subsequent expansion using a non-linear analogue circuit, to reconstruct the original signal. The non-linear circuit performing this function is known as an expander.

The combined operation of compressing and expanding is abbreviated as companding [46]. Figure 2.1 shows a block diagram of a companding system. In this case only 8 bits are sufficient to provide the required S/N ratio, compared to the 12 bits when no compression/expansion is implemented.

Several techniques are available to realize non-linear A/D conversion. These techniques can be classified into four groups depending on how the non-linear relation is obtained. The first group makes use of the exponential relation between the collector current and the base-emitter voltage in a bipolar transistor. The second group utilizes the time-voltage relation when
2.2. NLADC Based on $I_C - V_{BE}$

charging or discharging a capacitor. The third technique, which in practice is extensively used in A/D converters, is based on the components geometry such as resistors, capacitors, or the emitter area of bipolar transistors. The fourth group utilizes look-up tables that are stored in ROMs. Of course, it is possible to use a high resolution A/D converter to digitize the signal first and then convert the digital output to any non-linear form. But this method is not convenient since it requires the expensive high-resolution linear A/D converter which have to be avoided. The basic theory and the limitations of each of the four techniques are presented in the following sections.

2.2 Non-Linear A/D Conversion Based on $I_C - V_{BE}$

The implementation of a bipolar transistor as a logarithmic or exponential converter seems to be best suited for extremely wide dynamic range applications (about 8 decades) [47]. But, because many error sources exist, the useful dynamic range is rather limited.

The simple ideal relation can be expressed as:

$$V_{be} = \left( \frac{kT}{q} \right) \ln \left( \frac{I_c}{I_s} \right),$$

where $k$ is the Boltzmann constant, $T$ the absolute temperature in Kelvin, $q$ the elementary charge, and $I_s$ the saturation current.

Even though this relation is considered to be ideal, it shows two undesired error source terms. The first is the temperature dependence due to the term $T$, and the second is due to the saturation current, $I_s$. The saturation current has a temperature dependence, and is process dependent. This means that its value will differ from one device to the other, leading to different values of base-emitter voltages from one device to another, at the same collector current.

Apart from the temperature dependence and the errors caused by the saturation current, mentioned above, the collector current depends on the collector-base voltage (Early effect and leakage currents). Moreover, the bulk
resistances, high level injection and heating up caused by internal power dissipation lead to errors at high collector currents. These errors limits the accuracy when the bipolar transistor is used as an exponential/logarithmic converter, in wide-dynamic range applications. Several techniques have been developed to compensate for these non-ideal characteristics [41, 47, 48].

The bipolar transistor can be configured to function as an exponential converter as well as a logarithmic converter. When an input current is supplied at its collector and the base-emitter voltage is monitored, a logarithmic conversion is obtained. Alternatively, when the base-emitter voltage is the input and the collector current is the output, an exponential conversion is obtained.

In this type of non-linear A/D conversion, the non-linear conversion is accomplished in the analogue form. A logarithmic/exponential A/D converter can be constructed by cascading the analogue logarithmic/logarithmic converter with a linear A/D converter as shown in Figure 2.2.

Figure 2.2. A block diagram of a logarithmic/exponential A/D converter.

In the following, the basic logarithmic/exponential circuits are briefly discussed.

2.2.1 Logarithmic conversion

The basic circuit for a logarithmic conversion can be constructed from a bipolar transistor in a feedback loop of an operational amplifier, as shown in Figure 2.3(a). The input current \( I_i \) is compensated by an equal collector current. Because of the exponential relation between the collector and the base-emitter voltage and the virtual ground at the inverting input, an output voltage, \( V_o \), is generated equal to:

\[
V_o = -V_{be} = -\left(\frac{kT}{q}\right) \ln \left(\frac{I_i}{I_s}\right).
\]  \hspace{1cm} (2.5)

The temperature dependence of the saturation current, \( I_s \), can be compensated for by doubling the circuit as shown in Figure 2.3(b). The output voltage is given by:
\[ V_o = -V_{be1} + V_{be2} = -\left(\frac{kT}{q}\right) \ln \left(\frac{I_i}{I_R}\right). \] (2.6)

\begin{center}
(a)
\end{center}

\begin{center}
(b)
\end{center}

Figure 2.3. Basic logarithmic converter circuits.

The combination of the analogue logarithmic converter with a dual slope A/D converter is demonstrated to be a good solution for the reduction of the error due to the temperature dependence of the gain factor, \( kT/q \) [41]. In a dual slope A/D converter a capacitor is charged with the unknown input current, \( I_i \), for a fixed time, \( T_s \), and discharged with a reference current, \( I_R \). Because of the charge balance the next relation is valid

\[ I_i \times T_s = I_R \times T_m, \] (2.7)

where \( T_m \) is the discharge period of the dual-slope A/D converter capacitor. Solving for \( T_m \) yields:

\[ T_m = T_s \times \ln \left(\frac{I_i}{I_R}\right). \] (2.8)

In this method, the maximum capacitor voltage is affected by the temperature dependence, but if both the input current and the reference current are subject to the same temperature-dependent operations, the effect is cancelled out in the ratio \( T_m/T_s \).
Figure 2.4 shows a block diagram of a dual-slope A/D converter implementing this technique. The two logarithmic converter blocks both represent the analogue logarithmic converter shown in Figure 2.3(b). The inverting input of the integrator is at virtual ground potential, which results in a current

\[ I_{o1} = -\frac{kT}{qR} \ln \left( \frac{I_i}{I_R} \right) \quad \text{or} \quad I_{o2} = -\frac{kT}{qR} \ln \left( \frac{I_{ref}}{I_R} \right), \]  

(2.9)

when operating the switch to the proper position. During the sample time the capacitor is charged with \( I_{o1} \) and during the measure time discharged with \( I_{o2} \).

![Block Diagram](image)

Figure 2.4. A block diagram showing how the analogue logarithmic converter can be combined with a dual-slope A/D converter.

The dual-slope operation ensures

\[ \frac{T_s}{C} \times \frac{kT}{qR} \ln \left( \frac{I_i}{I_R} \right) = \frac{T_m}{C} \times \frac{kT}{qR} \ln \left( \frac{I_{ref}}{I_R} \right), \]  

(2.10)

which yields a measurement period of:

\[ T_m = T_s \times \ln \left( \frac{I_{ref}}{I_i} \right). \]  

(2.11)

### 2.2.2 Exponential conversion

Figure 2.5 shows a simple analogue exponential converter circuit. The transfer function is defined as:
2.3. Non-Linear A/D Conversion Based on V-T of a Capacitor

Basically two types of relations can be obtained which originate from the time-voltage relation when charging or discharging of a capacitor. The first type is based on an RC network [42, 43, 49, 50]. In this type, the capacitor \( C \) is charged or discharged through a resistor \( R \). Upon charging or discharging, the voltage and time are related exponentially. The function obtained follows the natural logarithm and can be defined as \( t = \ln[\frac{V_i}{V_C(t)}] \), where \( V_i \) is the initial voltage (i.e. at \( t = 0 \)) across the capacitor, and \( V_C(t) \) is the voltage across the capacitor at the time \( t \). In the second type, the capacitor is charged by an ideal current source, \( I_R \), or is placed in a feedback path of an operational amplifier [49, 51], to integrate an input reference voltage, \( V_R \). In this case, the voltage-time relation obtained is \( V_C(t) = Kt \), where \( K \) is a constant. Of course, this is a linear relation, but by cascading \( n \) circuits of this type, the voltage-time relation \( t = \frac{[V_C(t)]^{-n}}{K_n} \) can be obtained.

Non-linear A/D converters based on this technique can be built by cascading the non-linear analogue circuit by a linear A/D converter as shown.

\[
I_o = I_i \times \exp \left( \frac{qV_o}{kT} \right).
\] (2.12)

From this equation it can be concluded that the saturation current, \( I_s \), is already compensated for. The temperature dependence due to the term \( T \) can be cancelled out by the cascading of a temperature-dependent circuit at the input [48].

Figure 2.5. Basic exponential converter circuit.
in Figure 2.6. As the signal to be digitized is a time interval, the A/D conversion implementation is very simple. Counting a high frequency clock during the period $T$ is sufficient.

Figure 2.6. Block diagram of a non-linear A/D converter.

2.3.1 RC network

The basic circuit and the voltage outputs of the $RC$ network type are shown in Figure 2.7. In this circuit the capacitor is first charged to the unknown voltage, $V_i$, then it is discharged through the resistor $R$ and the voltage across the capacitor, $V_C(t)$, is compared to a reference voltage, $V_R$. The time from the starting of the discharge until the capacitor voltage, $V_C(t)$, equal to the reference voltage, $V_R$, is a measure of the unknown input voltage.

Figure 2.7. (a) A basic circuit of the $RC$-based non-linear converter, (b) Output voltages.
The equation of the capacitive discharge is:

\[ V_C(t) = V_i \times \exp \left( -\frac{t}{RC} \right), \]  
\[ (2.13) \]
solved for \( T \), where \( V_C(T) = V_R \), gives:

\[ T = RC \times \ln \left( \frac{V_i}{V_R} \right). \]  
\[ (2.14) \]

### 2.3.2 The integrator

The basic integrator circuit is shown in Figure 2.8. Initially the capacitor is reset. A reference voltage, \( V_R \), is applied to the integrator. The output of the integrator, \( V_A \), is equal to:

\[ V_A(t) = -\frac{1}{RC} \int_0^t (-V_R)dt = \left( \frac{V_R}{RC} \right) t = K_1 t. \]  
\[ (2.15) \]

Where \( K_1 \) is a constant. This output is compared to the unknown voltage, \( V_i \). The pulse width, \( T \), at \( V_A(T) = V_i \) is given by:

\[ T = \frac{V_i}{K_1}. \]  
\[ (2.16) \]

![Figure 2.8](image)

**Figure 2.8. A basic integrator circuit.**

This is basically the single-slope linear A/D converter. An extension, the dual-slope A/D converter, is frequently used in digital multimeters. In the circuit shown in Figure 2.8 the integrator basically operates as a ramp waveform generator. By cascading \( n \) integrators of this type, the first, square, cube, fourth, \( \cdots \), \( n \)th root of the input voltage can be obtained. The period \( T \) for \( n \) integrators is given by:

\[ T = \frac{(V_i)^{-n}}{K_n}. \]  
\[ (2.17) \]
2.4 Non-Linear A/D Conversion Based on Component Geometry Scaling

Analogue to digital conversion based on component geometry is the most widely used approach in practical A/D converters. This technique is based on division and/or multiplication of a voltage, current, or charge. The multiplication or division is done by using component scaling, such as resistors, capacitors, the emitter areas of bipolar transistors, or the channel dimensions of a MOS transistor. For example, a current can be divided into two equal parts at a node connected to branch into two equal resistors. Basically, any non-linear relation can be obtained by using the proper geometrical ratios. Since digital electronics is based on binary numbers, binary weighted scaling is often used. The major error in this technique is caused by the mismatch of component values, which is present even when the components are fabricated close to each other on the same chip. Mismatch errors are caused by geometrical errors resulting from lithography and/or processing parameters variations, such as doping concentrations and temperature variation during processing. It is possible to reduce the errors caused by linear gradient variations in the processing parameters by using symmetrically distributed geometries [52, 53]. Errors caused by temperature variations are significantly reduced if the components are thermally well coupled.

Most of the non-linear A/D converters based on component geometry scaling are implemented using the Successive Approximation Technique. Figure 2.9 shows a simplified block diagram of an A/D converter using this technique. The major components are a non-linear D/A converter, a comparator, a Successive Approximation Logic (SAL) and a clock generator. In the following, several techniques for realizing non-linear A/D converters based on component geometry are addressed.

![Block Diagram](image)

**Figure 2.9. A block diagram of a Successive Approximation A/D converter.**
2.4.1 Non-linear A/D converters based on programmable gain amplifiers (PGA)

One way to realize non-linear A/D converters based on component geometry scaling is to cascade a linear A/D converter with a Programmable Gain Amplifier (PGA), as shown in Figure 2.10. This technique is used for piece-wise linear approximation. The gain of the PGA is determined by the input voltage level [54]. The output usually takes the floating-point format of the form

\[ F \times B^E \]

where \( F \) is the fraction, \( B \) is the base and \( E \) is the exponent of the base. In binary systems \( B \) takes the value 2. Depending upon the input voltage range, the gain of the PGA is set to the highest possible value that is required to bring the input voltage level into the upper half of the A/D converter range, except for very small input signals, \( (< V_{FS}/2^e \) where \( e \) is the number of bits in the exponent). This amplified input signal is then digitized into an \( f \)-bit fraction. The circuit with this configuration normally has two conversion cycles. First, the programmable gain amplifier is set to the lowest possible gain. The signal is linearly converted to digital. From this value, the value of the exponent, \( E \), and the suitable gain of the PGA are determined. In the second cycle, the input voltage, \( V_i \), is converted at this gain setting to determine the fraction value \( F \).

![Figure 2.10. A block diagram of a non-linear A/D converter implementing a PGA.](image)

Several methods are available to realize a digitally controlled PGA with a gain varying as a power of 2. The simplest way is to use an operational amplifier in which one of the gain determining resistors is tapped over a set of resistors with the proper ratios [55], using a multiplexer as shown in Figure 2.11. An other realization of a PGA is by using a multiplying type D/A converter which incorporates an R-2R resistive ladder [56].
2.4.2 Non-linear A/D converters implementing the Successive Approximation Technique

The technique discussed in the previous section uses a linear A/D converter to accomplish the non-linear conversion. A more efficient method is to use a non-linear D/A converter in the conventional Successive Approximation configuration as shown schematically in Figure 2.12. The conversion cycle in this case is also composed of two modes. In the first, a course approximation in the power of two is used to determine the exponent, and, in the second, the fraction is determined using linear refining. The key element in this technique is the non-linear D/A converter, which is usually a Floating-Point D/A Converter (FPDAC).

Figure 2.11. A PGA utilizes an operational amplifier with multiplexing resistors.

Figure 2.12. A block diagram of a non-linear A/D converter using a floating-point D/A converter in a Successive Approximation Technique.
Several techniques based on ladder networks or binary-weighted resistors have been developed to realise FPDACs [57]. In its simplest form it can be a Binary Floating-Point Resistor (BFPR), which consists of a network of resistors and analogue switches. The network is designed such that the value of $R$ as seen at the output port is related to the Fraction $F$ and the Exponent $E$ as:

$$R = R_0 F 2^E.$$  
(2.18)

Figure 2.13 shows a realization of the BFPR for $f = 4$ and $e = 2$. The fraction is first loaded in the fraction register, least significant bit to the left, and then are circulated as shown in the figure. Figure 2.14 shows two possible implementation of such a resistor as a floating-point D/A converter.

![Diagram of BFPR implementation for $f = 4$ and $e = 2$.](image)

Figure 2.13. BFPR implementation for $f = 4$ and $e = 2$.

A second method for realizing a FPDAC is based on using two ladder networks and an operational amplifier, as shown in Figure 2.15. The $F$ ladder operates normally, giving an output voltage

$$V_o = \frac{F}{2^f} \times V_R.$$  
(2.19)

The $E$ ladder receives $2^e$ digital inputs. The analogue input to it is the output of the $F$ ladder, through a buffer amplifier. Therefore, the output voltage is given by:

$$V_F = \frac{V_R}{2^f 2^e} \times F \times 2^E.$$  
(2.20)
2.4.3 Non-linear A/D converters using switched capacitors

Charge is a quantity that can easily be manipulated using capacitors as charge storage elements. A non-linear voltage-time relation can be obtained using charge manipulation. In practice, many non-linear A/D converters based on this technique have been designed [49, 50]. Assume two capacitors $C_1$ and $C_2$ which are charged initially to $V_{C_1}$ and $V_{C_2}$, respectively. When they are connected in parallel, charge redistribution takes place, and the voltage across both capacitors, $V_C$, becomes:

$$V_C = \frac{V_{C_1}C_1}{(C_1 + C_2)} + \frac{V_{C_2}C_2}{(C_1 + C_2)}. \quad (2.21)$$

If $V_{C_2}$ is initially equal to zero, then
\[ V_C = \frac{C_1}{(C_1 + C_2)} V_{C1}. \] (2.22)

This means that connecting a discharged capacitor, \( C_2 \), across a charged capacitor, \( C_1 \), results in the multiplication of the voltage of the charged capacitor by a factor \( D \), \( D = C1/(C1 + C2) < 1 \). By repeating this process each clock cycle, an exponentially decreasing staircase output voltage, \( V_F \) results, as shown in Figure 2.16. For \( n \) clocks the output voltage, \( V_F(n) \) is given by:

\[ V_F(n) = \left( \frac{C_1}{C_1 - C_2} \right)^n V_{C1} = D^n V_R. \] (2.23)

![Diagram showing the output voltage of a staircase generator.](image)

*Figure 2.16. The output voltage of a staircase generator.*

This method can be implemented as shown schematically in Figure 2.17 to realize a non-linear A/D converter. The advantage of this method is that only two capacitors are required, therefore reducing the necessary wafer area and the total cost. A disadvantage is that the number of bits is limited to about 8, because of the conversion time, parasitic capacitances and capacitor mismatch [50].
2.5 Non-Linear A/D Conversion Using a ROM

Recent advances in integrated circuit technology have made it possible to fabricate large memories on small wafer area. This creates the possibility of storing functions as tables in a ROM to be implemented in a non-linear A/D conversion applications [44, 58]. A block diagram of a look-up table based non-linear A/D converter is shown in Figure 2.18. This method is basically the same as the integrator or the switched capacitors based non-linear A/D converter discussed previously, apart from the fact that the reference signal, \( V_F \), is generated by a binary address counter, a ROM and a linear D/A converter.

The operation of the circuit is as follows. A high frequency clock is applied to the address counter whose outputs drives the \( r \) lower-order address lines of the ROM with \( m \) address lines in total (\( m > r \)). The remaining \( m - r = M \) address lines are used as characteristic selection inputs to select the required function out of \( 2^M \). The digital output of the ROM is converted by a linear D/A converter into the output voltage \( V_F \). This voltage is compared with the input signal, \( V_i \). The contents of the main counter is incremented as long as \( V_F < V_i \). When the voltage \( V_F \) exceeds the input voltage, the output of the comparator disables the main counter. The contents of the main counter at this moment is the digital representation of the input.

This method can be used to cover a wide spectrum of non-linear characteristics. The technique can be used to select any one of a set of \( 2^M \) different prestored conversion characteristics. Any monotonically increasing function can be sampled, quantized, coded and stored in binary form in a specific re-
gion of the ROM, in the form of $2^r$ binary numbers, $k$-bit each. These binary numbers represent $2^r$ samples of the original analogue quantizing characteristic used for the non-linear function quantized in $2^k$ levels. These samples can be read when a specific characteristic is to be used by simply selecting its address in the characteristic selection input of the memory. A disadvantage of this method is the high cost arising from the several parts required.

### 2.6 Conclusions

Four different techniques that can be used in non-linear A/D converters have been discussed. This classification is based on how the non-linear relation is obtained. Several non-linear relation based on these four techniques are shown to be possible.

The logarithmic/exponential relation in a bipolar junction transistor is most suitable for large dynamic ranges, about 8 decades [47], but the accuracy is limited because there are some non-idealities in the transfer characteristics.

Two non-linear relations can be obtained when charging or discharging a capacitor. One follows the natural logarithm and is based on a simple $RC$ network. The other is obtained by cascading $n$ integrator circuits. The relation obtained in the integrator case is defined by: $T = K_n V^{-n}$. The capacitor-based non-linear A/D converter has a small dynamic range and a limited obtainable resolution compared to the circuit based on the bipolar junction transistor. Some limiting factors are: stray capacitances and charge injection of analogue switches.

The third technique for building non-linear A/D converters discussed in
this chapter is based on the geometrical scaling of component, such as resistors and capacitors, or the active area of a transistor. This technique is the most widely used in A/D converters. The limiting factor is the mismatch errors and the required chip area. The mismatch error can largely be reduced when applying laser trimming at the expense of processing complexity and consequently to the cost.

The fourth method that can be used to realize non-linear A/D conversion is based on ROMs. A disadvantage of this method is the high cost as a factor of the structural complexity.
Chapter 3
Specifications and Errors

3.1 Introduction

Some relevant specifications and error sources in the floating-point A/D converter are discussed in this chapter.

In sensor applications the static specifications such as differential and integral non-linearity, gain and offset errors and conversion time, are more important than the dynamic specifications. Dynamic specifications such as distortion and aperture jitter are important in AC applications such as audio and video and are, therefore, not addressed here. Moreover, in the discussion given in this chapter, a unipolar operation is assumed, which is the case in sensor applications.

In the various D/A converter realizations discussed in section 4.4, different values of the reference current \( I_R \) are required to produce the same output current range. This is because in some circuits the reference current is scaled up, while in others a combination of scaling up and down is implemented. In the following discussion the reference current is assumed to be equal to the lowest resolution of the converter, i.e. only scaling up of the reference current, \( I_R \), is considered.

3.2 The Ideal Transfer Function

The floating-point D/A converter, which is implemented in the feedback loop of the A/D, can be regarded as a multiplying D/A converter. As will be discussed in section 4.4, the floating-point D/A converter consists of two parts, the exponent and the fraction (see Figure 3.1). The exponent part generates a variable reference current, \( I_{o1} \), which is fed to the fraction part.
The variable reference current, $I_{o1}$, is proportional to the exponent, $E$, and is equal to:

$$I_{o1} = 2^E I_R.$$  (3.1)

![Figure 3.1. A block diagram of the floating-point D/A converter.](image)

The variable reference current, $I_{o1}$, is equal to the quantization of the floating-point D/A converter. In this respect, the floating-point D/A converter can be considered as a linear D/A with variable magnitude quantizing step of $\text{LSB}_E$. The magnitude of the $\text{LSB}_E$ varies as the power of 2, and can be written as:

$$\text{LSB}_E = 2^E I_R,$$  (3.2)

where $E$ ($= 0, 1, 2, \cdots, 2^e$) is the exponent, and $e$ is the number of bits of which it is composed.

From the above definitions, the ideal transfer function of a floating-point A/D converter, when used to approximate the input signal, $I_i$, can be written as:

$$2^E I_R \times F = I_i \pm 2^{(E-1)} I_R \quad \text{or} \quad \text{LSB}_E \times F = I_i \pm \frac{1}{2} \text{LSB}_E,$$  (3.3)

where the $f$-bit fraction, $F$, is given by:

$$F = 2^{f-1} b_f + 2^{f-2} b_{f-1} + \cdots + 2^2 b_3 + 2^1 b_2 + 2^0 b_1$$  (3.4)

In floating-point converters, the converter is always operated in the upper half of its range, unless for very small input signals. Thus, an important condition that must be satisfied by equations (3.3) and (3.4), is that $b_f$ (the MSB) should take the value "1" for $E = 1$ to 7, and takes the value "0" only when $I_i$ is less than $2^{(f-1)} I_R$. 

3.3 Resolution

Resolution can be defined as the minimum change in the input that can cause a change in the output. In A/D and D/A converters it is usually expressed in number of bits. A linear converter of $n$-bits is said to have a resolution of $n$ bits. In the case of floating-point converters the resolution is equal to the number of bits in the fraction.

3.4 Dynamic Range

The dynamic range of a converter is defined as the ratio of the maximum output (full scale) to the minimum output (resolution). For a linear converter of $n$-bit, the dynamic range is equal to $2^n$. In the case of a floating-point A/D converter, the dynamic range is determined by the number of bits in the fraction, $f$, as well as in the exponent, $e$, and is given by equation (1.5) as:

$$D = (2^f - 1)2^{(2^e - 1)} \approx 2^{(f + 2^e - 1)}.$$

3.5 Absolute Accuracy

The error of an A/D converter at a given output code is the difference between the theoretical (standard) and the actual analogue input required to produce that code. Since the code can be produced by any analogue input in a finite range, the input required to produce that code is defined as the midpoint of the range. Absolute error comprises gain error, offset error, quantization, non-linearity and noise.

3.6 Integral Non-Linearity

The locus of the centre points of the actual steps forms a curve that generally deviates from the straight line that would result from perfect uniform steps. This is a result of the step size nonuniformity, see Figure 3.2. The maximum deviation is called the integral non-linearity. Also referred to as relative accuracy. This deviation is usually expressed in percent, parts per million, or fraction of 1 LSB. The straight line can either be drawn as the best-fit line, or obtained by joining the endpoints of the characteristic after the offset and gain errors have been trimmed out.
In a D/A converter, the non-linearity error results from the sum of errors in all bits. Suppose an absolute error of $\epsilon_m$ in the $m^{th}$ bit, $b_m$. The non-ideal weighting of the $m^{th}$ bit is:

$$b_m = 2^m + \epsilon_m. \tag{3.6}$$

This results in a total absolute error, $\epsilon_T$, in an $n$-bit converter of:

$$\epsilon_T = \sum_{m=0}^{m=n-1} \epsilon_m. \tag{3.7}$$

![Diagram showing non-linearity in a D/A converter with a theoretical and best fit line.](image)

**Figure 3.2. Errors in an A/D converter.**

The bit errors $\epsilon_m$ normally are of a random nature, and can have a positive or negative sign. The converter can be calibrated so that the total error, $\epsilon_T$, is zero. The worst-case non-linearity error results when only all bits which have a positive (negative) error are selected. The absolute value of the sum of all errors with a positive sign, $|\epsilon_+|$ (negative sign $|\epsilon_-|$) should not exceed 1/2 LSB.

In the floating-point D/A converter, an error in the exponent produces an offset error in the transfer function. Suppose a relative error of $\epsilon_{\alpha,k}$ in the $k^{th}$
bit of the exponent, and that the exponent current is generated by selecting only one current mirror branch at a time (refer to section 4.2). The output current, which is proportional to the exponent, is:

\[ I_{o1} = 2^k I_R \pm \epsilon_{e,k}. \]  

(3.8)

And, therefore, the output current of the D/A converter will be:

\[ I_o = I_{o1} F = \left(2^k I_R + \epsilon_{e,k}\right) \left(F + \epsilon_f\right), \]  

(3.9)

where \( \epsilon_f \) is the relative error in the fraction \( F \).

Equation (3.9) can be approximated as:

\[ I_o \approx 2^k I_R F + \left(\epsilon_{e,k} + \epsilon_f\right), \]  

(3.10)

where \( \left(\epsilon_{e,k} + \epsilon_f\right) \) is the relative error in the output current \( I_o \).

For an \( f \) bit resolution the maximum relative error \( \left(\epsilon_{e,k} + \epsilon_f\right) \) should be less than \( \pm 2^{-\left(f+1\right)} \) (\( \pm 1/2 \) LSB).

If the relative error \( \epsilon_{e,k} \) in the \( k^{th} \) bit of the exponent is larger than \( \pm 1/2 \) LSB, it will cause an offset in the corresponding segment at the output. And, therefore, that segment will be shifted outside the required specifications. Figure 3.3 shows the transfer function for the first two segments, i.e. for \( E = 0 \) and \( 1 \). The dotted line shows the ideal transfer function and the solid line shows the actual output with a relative error of \(-1/4 \) LSB\(_0\) (LSB\(_0\) = \( I_R \)) and of \(+1 \) LSB\(_1\) (LSB\(_1\) = 2\( I_R \)) for \( E = 1 \) in the exponent, where the error in the fraction assume to be zero. The large bit error in the exponent for \( E = 1 \) causes a shift of the segment and, therefore, a jump in the transition between the two segments. Therefore, the maximum relative error in each bit of the programmable current source used for the exponent should be less than \( \pm 1/2 \) LSB, for the proper operation of the floating-point A/D converter.

### 3.7 Differential Non-Linearity

The maximum deviation of the actual step size from the ideal step size of 1 LSB is called the differential non-linearity, which is also expressed in a fraction of 1 LSB. Thus in ideal D/A converter, all steps are exactly 1 LSB and the differential non-linearity is zero.

A differential non-linearity error larger than \( \pm 1/2 \) LSB can lead to non-monotonic response in a D/A converter and missing codes in an A/D converter.
3.8 Settling Time

The settling time in a D/A converter represents the time it takes for the output to settle within a specified band, usually ±1/2 LSB, of its final value following a code change at the input (usually a full-scale change).

3.9 Conversion Time and Rate

The conversion time is the total time required by a converter to perform a complete conversion. For example, in the case of the floating-point presented in this thesis, the conversion time includes the time required to determine the exponent and the fraction as well as the initialization period.

The conversion rate corresponds to the maximum number of conversions that can effectively be carried out in one second. In the case of the floating-point A/D converter described in this thesis, the conversion rate is simply the inverse of the conversion time. However, in some high-speed sampling converters, because of pipelining, new conversion are initiated before conversion has been completed, and therefore, the conversion rate is not the inverse of the conversion time.
3.10 Quantization Error

For an $n$-bit linear A/D converter, all analogue values within a given range are represented by the same digital code, which is assigned to the nominal mid-range value. There is, therefore, an inherent quantization uncertainty of $\pm 1/2$ LSB, in addition to the actual conversion errors. In the floating-point A/D converter, the value of the LSB is a function of the input signal level, and is related to the exponent by:

$$\text{LSB}_E = 2^E I_R,$$

therefore, the quantization error increases (as power of 2) with increasing the magnitude of the input signal as shown in Figure 3.4 for $E = 0, 1$ and 2.

![Quantization error in a floating-point converter.](image)

3.11 Gain Error

The gain error in linear A/D converters is the deviation of the actual difference between the first and last code transitions (or the best fit) from the ideal
difference between the first and the last code transitions. In other words, this error indicates whether the average of the LSB of a converter is larger or smaller than the theoretical value. The effect of the gain error is to rotate the characteristic about the origin. The gain error factor, \( k \), is defined as a positive coefficient greater or smaller than one. When \( k = 1 \), there is no gain error.

In the floating-point D/A converter, if the exponent and the fraction have a gain error factors of \( k_e \) and \( k_f \), respectively, the floating-point D/A converter will have a gain error factor which is equal to their product, i.e. \( k_e k_f \).

### 3.12 Offset Error

The offset error is defined as the difference between the value of the input signal which sets the LSB into state "1" and the theoretical value of the input signal which set the LSB (note that the LSB is not a constant in the case of the floating-point converter, but is given by equation (3.11)). The effect of the offset is to transfer the characteristic left or right, as shown in Figure 3.2.

### 3.13 Monotonicity and Missing Codes

A D/A converter is said to be monotonic if the output either increases or remains constant (but never decreases) as the digital input code increases. When a non-monotonic D/A converter is implemented in the feedback loop to realize an A/D converter, a missing code condition could result.

### 3.14 Conclusions

In floating-point converters, non-linearity error in the exponent produces an offset error in the transfer function of the converter. Therefore, it is necessary to keep the relative error in the exponent within \( \pm 1/2 \) LSB. The requirements in the fraction are similar to those imposed on conventional linear converter.
Chapter 4

Architecture of the Floating-Point A/D Converter

4.1 Introduction

In high speed linear A/D converters, such as flash converters, all bits are generated simultaneously, thus completing the conversion in just one clock cycle. This high speed operation requires a large number of components, which makes it difficult to realize them in a monolithic form [20]. Beyond 10-bit of resolution the limitations are die area, comparator matching, or device cost.

The hardware required for the realization of an integrating-type A/D converter is much less than that required for a flash converter, but the conversion time is rather long. The two most widely used integrating-type converters are the charge-balancing A/D converters and the dual-slope A/D converters. Charge-balancing A/D converters convert the input signal to a frequency, which is then measured by a counter and converted to an output code proportional to the analogue input. In dual-slope A/D converters, the conversion period consists of two phases. The signal integration phase, where the unknown input signal is integrated for $2^n$ cycles, and the deintegrate phase, which takes $N$ cycles, where $N$ is the digital output. Thus the total conversion time is $N + 2^n$ cycles.

Sigma-delta converters have a flexibility in the interchange between conversion time and resolution. The resolution of sigma-delta converters is higher than that of successive-approximation converters and lower than that of the integrating type of converters. Because of the complex digital filtering, the monolithic chips tend to be large and their power requirements high [20]. At present, hybrid realization is often implemented to reduce the coupling of the
noise between the analogue and the digital parts and to allow for different processes in the fabrication of the two parts [59].

Successive approximation technique offers a good compromise between circuit complexity and speed of operation. An n-bit successive approximation converter, requires \( n \) clock cycles to complete the conversion. The resolution largely depends on the technology employed. By using standard processing, the obtainable resolution is less than 10-bit [60, 61]. To achieve a higher resolution (12 to 16-bit), laser-trimmed thin-film resistors are implemented [19, 62].

From the several A/D conversion techniques, the Successive Approximation technique is chosen for the realization of the non-linear A/D converter, which is the main aim of the research reported here. The choice for the successive approximation is because of its good compromise between circuit complexity and speed of operation, and further, because of its ease of implementation in floating-point conversion based on component geometry scaling. It has been discussed previously, in section 2.4.

Figure 4.1 shows a simplified block diagram of the Successive Approximation floating-point A/D converter. It consists of a floating-point D/A converter, a Successive Approximation logic (SAL), and a comparator. This chapter discusses the design and realization of the three parts. The three parts have been realized in a standard bipolar process (DIMES-01).

![Block Diagram](image)

Figure 4.1. A block diagram of a successive approximation floating-point A/D converter.

The floating-point D/A converter is essentially a digitally programmable current source. Therefore, the following section discusses the design and realization of accurate digitally programmable current sources. Section 4.3
discusses the errors in the programmable current sources. The realization of floating-point D/A converters is presented in section 4.4. Section 4.5 gives an outline of the successive approximation technique implemented in the floating-point A/D converter. Section 4.6 discusses the design and realization of the successive approximation logic. The current comparator is presented in section 4.7 and the complete bipolar A/D converter in section 4.8.

A 3-bit exponent and an 8-bit fraction are satisfactory for most sensor applications. Using equations (1.5) and (1.6), would result in a 15-bit dynamic range and 8-bit accuracy.

4.2 Digitally Programmable Current Sources

The floating-point D/A converter, which is the key element in the A/D converter, is essentially a non-linear digitally programmable current source. Therefore, this section is devoted to discussing the design of digitally programmable current sources, the implementation of which to realize the floating-point D/A converters is discussed in the section thereafter.

A digitally programmable current source can be built using a current mirror circuit as shown in Figure 4.2. Each of the current mirror branches can be switched either to the output node or to the power supply. The output current is equal to the sum of the currents in the branches that were switched to the output node. For n-bit \( b_0b_1b_2 \cdots b_{n-1} \), the output current is given by:

\[
I_o = \sum_{i=0}^{n-1} b_i I_R \times 2^i. \tag{4.1}
\]

The binary scaling can be achieved by using emitter resistors or binary-weighted emitter areas. When using emitter resistors, as shown in the simplified circuit of Figure 4.3(a), and neglecting the base current, the output current, \( I_o \), is related to the input current, \( I_i \), by:

\[
I_o = \frac{kT}{qR_o} \ln \frac{I_i}{I_o} + \frac{I_i R_i}{R_o}. \tag{4.2}
\]

As it is evident from equation (4.2), the output current is temperature dependent. Moreover, the relation between \( I_o \) and the resistor values is not linear, which makes the realization of binary-weighted current sources more complicated.
Figure 4.2. A digitally programmable current source using current mirrors.

Figure 4.3. Simple current mirror circuits.
4.2 Digitally Programmable Current Source

By using emitter area scaling, the output current is related to the input current by:

\[ I_o = I_i \frac{I_{s2}}{I_{s1}}. \]  \hspace{1cm} (4.3)

where \( I_{s1} \) and \( I_{s2} \) are the saturation currents of \( Q_1 \) and \( Q_2 \), respectively, which are directly proportional to emitter areas.

The saturation current is temperature dependent, but if both junctions are at the same temperature, the ratio \( I_{s2}/I_{s1} \) is independent of temperature.

Accounting for the base current in the circuit of Figure 4.3(b) [63], the output current is given by:

\[ I_o = I_i \left( 1 - \frac{2}{\beta_F + 2} \right). \]  \hspace{1cm} (4.4)

where \( \beta_F \) is the forward common-emitter current gain.

If \( \beta_F \) is constant, the error attributable to the base current given by equation (4.4) will be constant, and can be considered as an offset. Unfortunately, \( \beta_F \) depends on the current density, and, therefore, the error is current dependent. In some realizations of the binary-weighted current sources, the input current is constant, \( (I_i = I_R) \), and, therefore, the current density is constant. This in turn will result in a constant \( \beta_F \), and therefore, a constant error due to the base current.

Another source of error in the simple current mirror circuit shown in Figure 4.3(b) is from the Early effect. The collector current of the bipolar transistor is proportional to \( 1 + V_{CE}/V_A \), where \( V_A \) is the Early voltage. The output current of the current mirror, including the error caused by the Early effect only is given by:

\[ I_o = I_i \left( \frac{1 + V_{CE}(Q_2)/V_A}{1 + V_{CE}(Q_1)/V_A} \right). \]  \hspace{1cm} (4.5)

A better transfer accuracy of the current mirror can be obtained by the cascoding of the mirror transistors \( Q_1 \) and \( Q_2 \) and using a Darlington configuration to supply the base current externally as shown in Figure 4.4 [63]. In this case, the error caused by the Early voltage of \( Q_1 \) and \( Q_2 \) is minimized, since \( V_{BC}(Q_1) \approx V_{BC}(Q_2) \approx 0 \).

An accurate binary-weighted current source based on the improved current mirror shown in Figure 4.4, can be realized using emitter area scaling as shown in Figure 4.5. The main source of error in this circuit is attributable to the mismatch of the transistor parameters caused by the technological process parameter variations such as temperature and doping levels. The voltage
Figure 4.4. *Improved current mirror."

Figure 4.5. *Accurate binary-weighted current sources using emitter area scaling."

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4.2 Digitally Programmable Current Source

drop due to the aluminum interconnect results in similar deviations in the bias conditions of the transistors. In the realized programmable current source circuit, the effect of the mismatch of the transistor parameters is reduced by using a symmetrical layout design [52, 64], which is discussed in more detail in section 4.3.3.

Using a single-collector transistor with multi-emitters as a binary-weighted current source would have a major advantage. In this realization, the required die area would be minimized, since no isolation lands are required between the collectors. Unfortunately, this circuit was for this application is not practically possible. The main problem when using a single-collector multi-emitter transistor is that the switching of the current mirror branches has to be done at the emitter side. The output current of the current mirror depends exponentially on the emitter-base voltage drop. The transfer accuracy of the current mirror will be disturbed by inserting any type of switch in the loop. Therefore, the choice is taken for current switching at the collector side.

The current switching at the collector is implemented as shown in Figure 4.6. Each collector is connected by a diode connected transistor, \((Q_{D0}, Q_{D1}, \ldots, Q_{D(n-1)})\), to the output node and by a switching transistor, \((Q_{S0}, Q_{S1}, \ldots, Q_{S(n-1)})\), to the power supply as shown in the figure. An advantage of using the diode connection at the output node is that no errors arise from the base currents of the switches.

Figure 4.6. Current switching.
Chapter 4. Architecture of the Floating-Point A/D Converter

The operation of the current switching is as follows: when a low logic level, $V_{SL}, (\approx 0\text{V})$ is applied at the selected switch, for example $S0$, the emitter base junction of $Q_{S0}$ is reverse biased, and $Q_{S0}$ is therefore switched OFF. The diode connected transistor $Q_{D0}$ is switched ON, because the voltage level at the collector of $Q_4$ is less than the voltage level at the output node, $V_o$. When $Q_{D0}$ is ON and $Q_{S0}$ is OFF, the voltage level at the collector of $Q_4$ is at its minimum value, $V_{XL}$, and is given by:

$$V_{XL} = V_o - V_{BE}(Q_{D0}).$$

(4.6)

This minimum voltage level at the collector of $Q_4$ is larger than zero (twice the $V_{BE}$ voltage drop). This ensures that $Q_{S0}$ remains OFF. The current flowing to the current mirror branch flows from the output node through the diode connected transistor.

When a relatively high voltage level, $V_{SH}(\approx 5\text{V})$, is applied at the base of $Q_{S0}$, its emitter-base junction is forward biased, and $Q_{S0}$, therefore, conducts. The voltage level at its emitter, $V_{XH}$, is given by:

$$V_{XH} = V_{SH} - V_{BE}(Q_{S0}).$$

(4.7)

If this voltage is higher than the voltage level at the output node, $V_o$, the diode connected transistor, $Q_{D0}$, is switched OFF. The current flowing to the current mirror branch flows from the power supply through the switching transistor $Q_{S0}$.

In this manner none, one, or more than one binary-weighted current branches can be switched either to the output node or to the positive power supply. The output current, $I_o$ is equal to the sum of the currents in the branches that are switched to the output node.

An $n$-bit digitally programmable current source can be built using this technique as shown in Figure 4.7. By switching more than one current mirror branch at the same time, an $n$-bit linear D/A converter is obtained. This operation is the same as that of ordinary linear D/A converters, which is required in the determination of the fraction in the floating-point A/D converter, as shown in section 4.4. By selecting only one current mirror branch at a time, a binary-weighted current source results, which is required for determination of the exponent.

An alternative method to reduce the die area required by the programmable current source is shown in Figure 4.8. For a $2n$-bit current source, the $n$ MSBs are generated by scaling the input reference current up and the $n$ LSBs are generated by scaling down. This is accomplished by subdividing one current mirror branch with a unity emitter area into the $n$ LSBs as shown in
the figure. Thus, the total die area required by the mirror transistors is reduced. This reduction of the required dynamic range of emitter areas is at the expense of the minimum supply voltage level.

4.3 Errors in the Programmable Current Sources

4.3.1 Errors caused by base currents

As mentioned in section 4.2, there are no errors caused by the base currents of the switching transistors because of the diode connection. The base currents in the mirror transistors, \((Q_{Mr}, Q_{M0}, Q_{M1}, Q_{M2}, \ldots)\), and the cascode transistors, \((Q_{Cr}, Q_{C0}, Q_{C1}, Q_{C2}, \ldots)\), are supplied externally using the Darlington pair \(Q_5\) and \(Q_6\) (see Figure 4.7). Since the emitter areas of the mirror transistors are binary scaled, the current density is constant and \(\beta_F\) and the base-emitter voltage drops of all transistors are about the same; all transistors operate under the same conditions, which ensures that the base currents of the mirror transistors are also binary scaled. Therefore, the error caused by the base currents is cancelled out to a first approximation. Only a second-order effect due to mismatches remains.
Figure 4.8. A programmable current source with minimum die area.
The emitter area of the cascode transistors is binary scaled. Since the mismatch errors of those transistors are less critical, their unity emitter area is designed to be much smaller than that of the mirror transistors, so as to minimize the die area. The binary scaling of the cascode transistors is for two reasons. First, their base-emitter voltage drop is about the same. This ensures that the collector-base voltage drop of the mirror transistors are the same, which therefore reduces the errors due to the Early effect in the mirror transistors. The second reason for scaling the emitter areas of the cascode transistors is for the reduction of the error caused by their base currents, in the same manner as that for the mirror transistors discussed above.

### 4.3.2 Errors caused by parasitic resistances

The parasitic emitter and base resistances of the bipolar transistor contribute to the error in most circuits. Fortunately, in current mirror circuits this error is cancelled out by using symmetry in the layout.

Assume a relative emitter area of $A_{Ei}$ and $A_{Eo}$ at the input and output side, respectively, and an emitter resistance of $R_{Ei}$ and $R_{Eo}$, respectively, at the input and the output side, as shown in the simplified circuit of Figure 4.9. Summing the voltage drops in the closed loop, we obtain:

$$V_{BEi} + I_i R_{Ei} = V_{BEo} + I_o R_{Eo}.$$  \hfill (4.8)

Algebraic manipulation yields:

$$I_o = I_i \frac{I_{so}}{I_{si}} \exp \left[ \frac{q}{kT} (I_i R_{Ei} - I_o R_{Eo}) \right],$$ \hfill (4.9)
where $I_{si}$ and $I_{so}$ are the saturation currents of the input and the output transistors, respectively. The term $I_i (I_{so}/I_{si})$ is the ideal output component. The exponential term shows the error factor caused by the emitter resistances.

If the current mirror has a scaling factor of $m$, the output current is related to the input current by:

$$I_o = m I_i. \quad (4.10)$$

Further, when assuming contact resistance to be predominantly proportional to the metal silicon contact area, the emitter resistance of the transistor at the output side, $R_{Eo}$, is related to that of the transistor at the input side, $R_{Ei}$, by:

$$R_{Eo} = \frac{R_{Ei}}{m}. \quad (4.11)$$

Substituting equations (4.10) and (4.11) into equation (4.9) yields:

$$I_o = I_i \frac{I_{so}}{I_{si}} \exp \left[ \frac{q}{kT} \left( I_i R_{Ei} - m I_i \frac{R_{Ei}}{m} \right) \right] = I_i \frac{I_{so}}{I_{si}}. \quad (4.12)$$

The exponential term vanishes, meaning that there are no errors caused by the emitter resistance of the mirror transistors if the transistors are well matched. The mismatch in the emitter resistance and the emitter areas causes a second-order error.

The effect of base resistance of the bipolar transistor is equivalent to an emitter resistance of the value $R_B / \beta_F$. Substituting $R_B / \beta_F$ for of $R_E$ in equation (4.9), we obtain:

$$I_o = I_i \frac{I_{so}}{I_{si}} \exp \left[ \frac{q}{kT} \beta \left( I_i R_{Bi} - I_o R_{Bo} \right) \right]. \quad (4.13)$$

Similarly, if the base resistance of the output transistor is related to that of the input transistor by:

$$R_{Bo} = \frac{R_{Bi}}{m}, \quad (4.14)$$

the errors caused by the base resistance in the two sides of the circuit is cancelled out. SPICE simulation confirm that, if the transistors are well matched, there will be no errors from the parasitic emitter or base resistance, in the current source circuit.
4.3 Errors in the Programmable Current Sources

4.3.3 Errors caused by transistor mismatch

Transistor parameters may differ from one transistor to another, even when the transistors are placed close to each other on the same chip. These differences are due to tolerance in process parameters, such as temperature gradients, doping concentration, masks misalignment, etc. In a small area of the wafer, the effect of the process parameters variation is assumed to produce a linear change in the transistor parameters.

In the following, the effect of linear changes in the common-emitter current gain and base and emitter resistances on the current source circuit performance is analyzed. These errors are minimized in the current source circuit by using a symmetrical layout design. The effect of each of $\beta_F$, the parasitic base and emitter resistances is studied separately. The total effect can be approximated by the superposition theorem [65].

In a small part of the wafer, it is assumed that a transistor parameter, such as $\beta_F$, can be approximated by linear dependence with position. For an array of $2n+1$ transistors, we denote the common-emitter current gain of the transistor at the centre of the array by $\beta_{F0}$. For constant gradient $\beta_F$ of any two neighbouring transistors differs by a constant amount, $\Delta \beta$. The current gain of any transistor in the array can be expressed by:

$$\beta_{Fi} = \beta_{F0} \pm i \Delta \beta,$$

(4.15)

where $i (= -n, \ldots, -1, 0, 1, 2, \ldots, n)$ denotes the index of the transistor in the array. If all transistors in the array have equal emitter areas, $A_E$, and are connected in parallel, the resulting transistor is equivalent to a transistor with an emitter area of $(2n + 1)A_E$ and $\beta_F$ of $\beta_{F0}$. The same is applicable to all other transistor parameters such as the base resistance, the emitter resistance, and the Early voltage.

The layout of the mirror transistors ($Q_{Mr}, Q_{M0}, Q_{M1}, Q_{M2}, \ldots$, see Figure 4.7) is designed as shown in Figure 4.10. Each square indicates a unity emitter area. The number indicates the total emitter area of the composite transistor of which this unity transistor is a part. The two smallest transistors (i.e. with a unity emitter area) are placed at the centre. Each of the other transistors is divided into two equal halves. Each two halves of a single transistor are placed in symmetry about the central point defined by the two smallest transistors. Thus, the effect of mismatch errors due to constant gradient in any of the process parameters over the wafer is reduced. This is true in the horizontal, vertical or any other direction. The net transistor parameter of the two halves of a single transistor can be approximated by the transistor parameter at the central point.
SPICE simulation of the programmable current source with $\Delta \beta = 2$ in the x-direction, and $\beta_{P0} = 100$ confirms that the error caused by constant gradient in $\beta_F$ would be cancelled out. A similar study for a gradient in the base (emitter) resistance in the mirror transistor of a nominal value of 100Ω (20Ω) and a difference of 2Ω (0.4Ω) between each two neighbouring transistors in the x-direction reveals the same results as when all transistors have a base (emitter) resistance of the nominal value. This means that a linear gradient in transistor parameters is cancelled out, for a first-order approximation, by using a symmetrical layout design.

### 4.4 Floating-Point D/A Converters

Two programmable current sources based on emitter area scaling were presented in the previous section. In this section we report on the realization of floating-point D/A converters using these programmable current sources. The main difference between the floating-point D/A converter realizations lies in the trade-off between the die area and the minimum power supply voltage level. In some implementations, a PNP current mirror is required, which might degrade the accuracy of the floating-point D/A converter by 1 bit. In a later section an improved method for designing a floating-point D/A converter is introduced. The advantage of this method is the low voltage operation ($\approx 3.5V$ power supply).

The floating-point D/A converter accepts two digital words $F$ (Fraction) and $E$ (Exponent) as input, and produces an analogue output current, $I_o$. The required transfer characteristics of the floating-point D/A converter can be expressed as: 

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Figure 4.10. The layout of the mirror transistors ($Q_{M1}$, $Q_{M0}$, $Q_{M1}$, $\cdots$).
\[ I_o = I_R \times F \times 2^E. \] (4.16)

For 3-bit exponent and 8-bit fraction, this relation can be plotted as shown in Figure 4.11. Note that only the lowest quarter of the relation is shown. For \( E = 1 \) to 7 only the upper half of the relation is used.

The most obvious way to realize a floating-point D/A converter is by using two programmable current sources as shown in the block diagram of Figure 4.12. The output current of one current source is proportional to the exponent, while the output current of the other is proportional to the fraction.

A 3-bit exponent means 8 distinct values, therefore an 8-bit current source is required for the exponent. A similar 8-bit current source is used for the fraction. Figure 4.13 shows the circuit diagram. The reference current, \( I_R \) is the input to the left current source. The output of this current source doubles for each increment in the exponent value. This is implemented by selecting only one current mirror branch at a time. The output current from the exponent current source, \( I_{o1} \), is given by:

\[ I_{o1} = I_R \times 2^E. \] (4.17)

The output current from the first programmable current source is used as the input to the second programmable current source using a PNP current mirror. The output of the second current source is proportional to the fraction and is given by:

\[ I_o = I_{o1} \times F = I_R \times F \times 2^E. \] (4.18)

The minimum voltage level of the power supply is about 6 times the \( V_{BE} \) voltage drop. The poor characteristics of the lateral PNP transistors might degrade the accuracy of this circuit by 1 bit. It is an advantageous to avoid the use of the PNP current mirror.

In the current source used for the exponent, only one current mirror branch is needed at a time. Therefore, the required die area can be reduced by replacing the transistor with the relative emitter area of 128 by one with a unity emitter area. A binary-weighted current can be generated in such an approach by adding current mirror branches rather than by selecting only one at a time. The largest current of the value \( 128I_R \) is generated by adding all current mirror branches at the output node.

A second floating-point D/A converter design, in which use of the lateral PNP current mirror is avoided, is shown in Figure 4.14. The two programmable current sources are cascaded. The penalty for avoiding the use
Figure 4.11. The transfer characteristics of the floating-point D/A converter.
4.4. Floating-Point D/A Converters

Figure 4.12. A block diagram of a floating-point D/A converter.

Figure 4.13. A circuit diagram of a floating-point D/A converter.
of the PNP current mirror is an increase in the minimum required voltage supply by about three base-emitter voltage drops.

![Diagram of a PNP current mirror](image)

**Figure 4.14. A floating-point D/A converter by cascading two current sources.**

By using two programmable current sources of the type shown in Figure 4.8, the required die area is further reduced. Figure 4.15 shows a block diagram of a floating-point D/A converter using two programmable current sources of the type shown in Figure 4.8. In this case, a minimum die area is achieved with an increase in the power supply voltage level requirements.

In the floating-point D/A converter circuits discussed above, the input reference current, $I_R$, is essentially converted into a base-emitter voltage drop.
which is further converted into an output current, $I_{o1}$. The output current is used as the input for the fraction current source. In this case, the base-emitter voltage drop in the current mirror transistors is kept constant and the output current varies as a function of the input digital word. A novel approach that can be implemented is based on a series of binary-scaled current mirror branches at the input side of the current mirror as well. The resulting current mirror circuit is shown in Figure 4.16. By forcing the input reference current, $I_R$, to flow into one or more current mirror branches at the input side, the resulting base-emitter voltage drop, $V_{BEi}$, is no longer constant, but a is function of the input reference current, $I_R$. The base-emitter voltage drop, $V_{BEi}$, is related to the sum of the relative emitter areas, $A_{Ei}$, of the transistors through which the reference current flows by:

$$V_{BEi} = \frac{kT}{q} \ln \left( \frac{I_R}{A_{Ei}I_s} \right).$$

By selecting only one current mirror branch at a time, the selected emitter area at the input side, $A_{Ei}$, is related to the exponent, $E$, by:

$$A_{Ei} = 2^E A_E,$$
where $A_E$ is the unity emitter area.

The output current, $I_o$ is related to $V_{BEi}$ by:

$$I_o = A_{Eo} I_s \exp \left( \frac{qV_{BEi}}{kT} \right), \quad (4.21)$$

where $A_{Eo}$ is the sum of the relative emitter areas of the selected branches at the output side by switching them to the output node.

Substituting equation (4.19) into equation (4.21), the output current is given by:

$$I_o = \frac{A_{Eo}}{A_{Ei}} I_R. \quad (4.22)$$

The total emitter area on the output side, $A_{Eo}$ is related to the fraction, $F$, by:

$$A_{Eo} = FA_E. \quad (4.23)$$

Combining equations (4.20), (4.22) and (4.23) the output current, $I_o$ is given by:
\[ I_o = I_R \times F \times 2^{-E}. \] (4.24)

An advantage of the circuit given in Figure 4.16 is that it can operate with a voltage supply as low as 3.5 Volts.

For 3-bit exponent and 8-bit fraction, the minimum output current \( I_R/128 \) is obtained when selecting the relative emitter area 128 on the input side and 1 on the output side, whereas the maximum output current, \( 255I_R \), is generated when selecting area 1 on the input side and all transistors that are on the output side. By switching the proper current mirror branches on the input and the output sides, any current in this range can be generated (with an 8-bit resolution).

In the realized circuit, the reference current \( I_R \) is chosen to be 12.8\(\mu\)A, the minimum output current, \( I_{o,min} \), is:

\[ I_{o,\text{min}} = 2^{-7} \times I_R = 0.1\mu\text{A}, \] (4.25)

and the maximum output current, \( I_{o,max} \), is:

\[ I_{o,\text{max}} = (2^8 - 1) \times I_R = 3.264\text{mA}. \] (4.26)

### 4.5 The Successive Approximation Technique

The successive approximation procedure in a floating-point A/D converter consists of two modes of operation. In the first mode (the exponent mode), a search operation is performed to determine the exponent, whereas in the second mode (the fraction mode), a similar search operation is used to determine the fraction. For the \( e \)-bit exponent, \( N_e \) clock cycles are required to determine the exponent, where \( N_e \) can take any value between 1 and \( 2^e \), depending on the level of the input signal. For the \( f \)-bit fraction, the fraction mode requires \( f \) clocks. The initialization process requires 2 clock cycles. Therefore, the total conversion time is \( (f + N_e + 2) \) clocks. The worst-case conversion time is equal to \( f + 2^e + 2 \) clock cycles, and is equal to 18 for 3-bit exponent and 8-bit fraction.

Figure 4.17 shows a flow-chart of the conversion procedure. When the Start Conversion (\( \text{SC} \)) command is applied, all fraction bits are set to high logic level "1", and the exponent is set to its lowest value, i.e. zero. At the same time the End-of-Conversion (\( \text{EC} \)) bit is set to a high logic level. After initialization, a search operation is performed, in which the converter is set to
the lowest possible range that is just larger than or equal to the input signal. This is done by comparing the output current from the D/A converter, \( I_o \), with the unknown input current, \( I_i \). If the input current, \( I_i \), is larger than the output current of the D/A converter, \( I_o \), the exponent is increased by one and the comparison procedure is repeated again. This process is repeated until the \( I_o \) exceeds \( I_i \). When this condition is satisfied, the exponent is found, and, therefore, the exponent mode is terminated. After the termination of the exponent mode, the fraction mode starts.

![Flow-chart of the A/D conversion procedure](image)

Figure 4.17. A flow-chart of the A/D conversion procedure.

The fraction mode is similar to that of linear A/D converters. When the converter enters the fraction mode, the MSB is reset and all other bits are kept at their high logic level values. The output current from the D/A converter is compared with the input current. If the input current is smaller than \( I_o \), and,
therefore, the comparator output, \( D_C \), is low, the MSB preserves its low logic value and the next MSB is reset. Otherwise, the MSB is set to a high logic level, and the next MSB is reset. These two steps are simply implemented in the hardware by latching the comparator output in the MSB and resetting the next MSB. This process is repeated for each bit, starting from the MSB, until the decision is taken for the LSB. Once the decision is taken for the LSB, the End-of-Conversion (\( \overline{E_C} \)) signal goes to low logic level indicating the completion of the conversion process.

### 4.6 The Successive Approximation Logic

Figure 4.18 shows a block diagram of the successive approximation logic (SAL). It consists of four parts, the exponent and the fraction registers, the control logic and an 8-line to 3-bit encoder.

![Block Diagram of the Successive Approximation Logic](image)

**Figure 4.18. A block diagram of the successive approximation logic.**

As a single block, the SAL has three signal inputs and 20 outputs. The three inputs are the comparator output, \( D_C \), the start conversion signal, \( \overline{S_C} \) and the clock, \( \text{clk} \). The outputs are the 16 lines to the D/A converter switches (from which 8 represent the fraction \( F \) and 8 the non-encoded exponent \( E \)), a 3-bit exponent and the End-of-Conversion line, \( \overline{E_C} \).

Figure 4.19 shows the state diagram of the successive approximation algorithm. Four stable states are required to define the operation of the converter.
The four states are; the Start State, (SS), the Exponent State (ES), the Fraction State (FS), and the Wait State (WS). Whenever a start conversion signal is applied, the converter enters the SS state, where initialization takes place. In the ES state a search operation is performed to determine the exponent. Once the exponent is determined, the converter enters the Fraction State, FS. A similar search operation is performed to determine the fraction. After the fraction is determined the converter enters the wait state, WS.

The inputs/outputs signals are defined as follows:

- $S_C$: Start Conversion,
- $D_C$: The comparator output,
- $E_C$: End-of-Conversion,
- $D_1$ and $D_2$: The inputs to the internal flip-flops,
- $Q_1$ and $Q_2$: The outputs of the internal flip-flops,
- $F_M$: Start Conversion,

![State Diagram](image)

Figure 4.19. The state diagram of the SAL.
4.6. The Successive Approximation Logic

\( \overline{E_M} \) : The comparator output,
\( D_o \) : A data input to the Exponent register,
\( S/P \) : Serial/Parallel load.

The successive approximation logic is realized using a modified version of the Emitter Function Logic (EFL) [17]. In this implementation a non-linear load is used instead of the ordinary resistive load. The choice for the EFL is because of its fast speed of operation and the LSI capability [66].

Before discussing the four parts of the successive approximation logic, it is important to introduce some basic EFL building blocks that are used for the realization.

### 4.6.1 EFL Building Blocks

The basic EFL cell that uses a non-linear load [17, 67] is shown in Figure 4.20. The main idea used in EFL is the implementation of multi-emitter transistors for the realization of logic AND and wired-OR functions. The logic AND function is realized by connecting logic inputs to the emitters of a multi-emitter transistor, where the AND function is obtained at the collector. The OR operation is obtained by the wired-OR function utilizing the open-emitter outputs.

![Figure 4.20. The basic EFL cell that uses a non-linear load.](image)

Figure 4.21(a) shows the circuits and the logic symbols of an AND gate. When the voltage level at the input \( B \) is higher than \( V_{rr} \), the current flows through the output transistor, and, therefore, the output is low. When the voltage level at \( B \) is lower than \( V_{rr} \), the logic output depends on \( A \) and will be
HIGH only if the voltage level at A is HIGH. Figure 4.21(b) shows the circuit and the logic symbol of an INHIBIT gate. Its operation is similar to that of the AND gate except that the inverse effect of the input B is seen, since the A input is connected to the right-hand transistor of the differential pair. The NOR gate requires two additional transistors although the multi-emitter transistor is not required as shown in Figure 4.21(c). If either of the inputs (or both) is HIGH, a current flows in the diode connected transistor, and, therefore, the output is LOW. Only when the two inputs are LOW, there is no current through the diode connected transistor, and the output is HIGH.

A SELECT gate is shown in Figure 4.22(a). Depending on the S input, one of the A and the B inputs is activated (selected) and the output have the same value as the activated input. A BUFFER gate is shown in Figure 4.22(b). A sample/halt (S/H) gate is shown in Figure 4.22(c). The circuit is similar to that of the SELECT gate shown previously in Figure 4.22(a). The output is fed to one of the inputs. When the (S/H) input is LOW, the D input appears at the output. However, when the (S/H) input goes to HIGH, the circuit output is locked in the state in which it was before.

The EFL gate uses two voltage references, which are referred to as the upper voltage reference, $V_{ru}$, and the lower voltage reference, $V_{rl}$. The circuit that is designed to generate the two voltage references is shown in Figure 4.23. A non-linear load ($Q_1$ to $Q_3$) biased by the collector current of $Q_3$ is used to generate a bias dependent reference voltage. This voltage is fed to a voltage follower, consisting of $Q_5$ to $Q_{16}$. The output from the voltage follower is divided into two equal parts using $R_1$ and $R_2$, where the mid point is the upper voltage level, $V_{ru}$, $Q_{17}$, which is biased with the same current as $Q_{13}$, is used to generate the lower voltage reference, $V_{rl}$.

In logic circuit design, it is always necessary to have a memory element. Figure 4.24 shows the circuit diagram of a positive edge triggered master-slave D-type flip-flop, its logic symbol and its state table.

In many register applications, it is desirable to have a dual input flip-flop, one input to be used for a shift operation while the other is to be used for parallel load. Figure 4.25 shows a dual input master-slave flip-flop. The two inputs are referred to as the Parallel Input, $PI$, and the Serial Input, $SI$.

The selection of the serial or parallel input is done in an indirect way using three clocks (X, Y, and Z) to the flip-flop. Thus, a smaller layout area can be achieved since no physical gate is required for the selection operation. Only two extra transistors are required for the second input (see Figure 4.25). The Z clock is a buffered version of the input clock, clk. The X clock is generated by a NOR operation and the Y clock is generated by an INHIBIT operation as shown in Figure 4.26(a). Figure 4.26(b) shows the X, Y and Z wave forms.
Figure 4.21. The circuits and the logic symbols of: (a) AND, (b) INHIBIT and (c) NOR.
Figure 4.22. The circuits and the logic symbols of: (a) SELECT, (b) BUFFER and (c) SAMPLE/HOLD.
4.6. The Successive Approximation Logic

Figure 4.23. The voltage references generator.

Figure 4.24. The circuit diagram of a master-slave D-type flip-flop and its state table.
Figure 4.25. A dual input master-slave flip-flop.

Figure 4.26. The X, Y and Z wave forms.
in relation to the clk and the Serial/Parallel \((S/P)\) selection signal. Either the serial input or the parallel input is latched in the flip-flop, depending on whether \((S/P)\) is high or low, respectively.

### 4.6.2 The Control Unit

As shown previously in Figure 4.19, four stable states are required. Two flip-flops are used to decode the four internal states of the converter. The state table in Table 4.1 is obtained from Figure 4.19. After converting to Karnaugh maps, the following set of equations is obtained;

\[
D_O = S_C
\]  
(4.27)

\[
D_1 = Q_2 S_C \overline{D_C} + Q_1 S_C
\]  
(4.28)

\[
D_2 = Q_2 S_C D_C + Q_1 Q_2 S_C + Q_1 S_C \overline{E_C} + \overline{Q_1 \overline{Q_2} S_C}
\]  
(4.29)

\[
E_M = D_1 = Q_2 S_C \overline{D_C} + Q_1 S_C
\]  
(4.30)

\[
F_M = Q_2 S_C D_C + Q_1 Q_2 S_C + Q_1 S_C \overline{E_C}
\]  
(4.31)

\[
S/P = Q_2 S_C + Q_1 S_C
\]  
(4.32)

where \(D_1\) and \(D_2\) are the inputs to the flip-flops used to define the internal state, \(Q_1\) and \(Q_2\) are their outputs.

The wired-OR capability of the EFL it is a great advantage. No physical gates are required to perform the OR operations in realizing the above six equations. This makes the circuit much simpler. Figure 4.27 shows the implementation of the above equations.

### 4.6.3 The Exponent Register

The exponent register composed of an 8-bit shift/load register, a clock generator, and a sample/hold circuit, as shown in the logic diagram of Figure 4.28. The operation of the circuit is as follows: on the receipt of a start conversion command, \(S_C\), the converter initialization take place. In the initialization period, the control unit enables the exponent register, and sets it to the parallel mode. This is done by setting both the \(E_M\) and the \(S/P\) to low logic levels. In the first positive edge of the clock, the most left flip-flop is set and all other
<table>
<thead>
<tr>
<th>Inputs</th>
<th>Outputs</th>
</tr>
</thead>
<tbody>
<tr>
<td>$Q_1$</td>
<td>$Q_2$</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
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</tbody>
</table>

Table 4.1. The state table of the A/D converter
4.6. The Successive Approximation Logic

Figure 4.27. The logic diagram of the control logic.

Figure 4.28. The logic diagram of the exponent register.
flip-flops are reset. This is accomplished by connecting the parallel inputs, \( P_I \), to the flip-flops as shown in the figure. This process is repeated for two clocks. The repetition is because the initialization of the fraction register requires two clock cycles.

After initialization, the exponent mode starts. In this mode the exponent register is enabled and is set to the shift mode. With each clock the data in the register is shifted to the right. The length of this mode is determined by the control unit depending on the comparator output. While the comparator output, \( D_C \), is LOW, the shift operation is continued. Once the comparator output goes high, the exponent register is disabled. The present value of the exponent is the required value. Therefore, the exponent mode is terminated. The control unit sets the \( \overline{E_M} \) line to HIGH disabling the register. The exponent register freezes in this condition until another \( \overline{SC} \) command is applied. By the end of the exponent mode the fraction mode starts.

### 4.6.4 The 8-line to 3-bit encoder

In the search operation of the exponent, each clock a current mirror branch is added by the shift-right operation. The 8-line to 3-bit binary encoder converts the 8-outputs of the flip-flops to the 3-bit exponent according to Table 4.2.

<table>
<thead>
<tr>
<th>Inputs</th>
<th>Outputs</th>
</tr>
</thead>
<tbody>
<tr>
<td>( b_0 ) ( b_1 ) ( b_2 ) ( b_3 ) ( b_4 ) ( b_5 ) ( b_6 ) ( b_7 )</td>
<td>( b_2 ) ( b_1 ) ( b_0 )</td>
</tr>
<tr>
<td>1 0 0 0 0 0 0 0</td>
<td>0 0 0</td>
</tr>
<tr>
<td>1 1 0 0 0 0 0 0</td>
<td>0 0 1</td>
</tr>
<tr>
<td>1 1 1 0 0 0 0 0</td>
<td>0 1 0</td>
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<td>1 1 1 1 0 0 0 0</td>
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<td>1 0 1</td>
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<tr>
<td>1 1 1 1 1 1 1 0</td>
<td>1 1 0</td>
</tr>
<tr>
<td>1 1 1 1 1 1 1 1</td>
<td>1 1 1</td>
</tr>
</tbody>
</table>

*Table 4.2. The function table of the 8-line to 3-bit encoder*

### 4.6.5 The Fraction Register

The logic diagram of the fraction register is shown in Figure 4.29. It consists of a 10-bit shift/load register, a SELECT, an INHIBIT gate, a sample and hold circuit, a clock generator, eight flip-flops and eight AND gates. The inputs are the clock, \( clk \), the serial/parallel control, \( S/F \), the comparator
output, $D_C$, a data input, $D_O$, and the enable/disable input, $\overline{F_M}$. The data line $D_O$ is generated by the control unit. The outputs are the 8-bit fraction and the $\overline{E_C}$ signal.

![Fraction Register Diagram](image)

Figure 4.29. The logic diagram of the fraction register.

In the initialization period, the $\overline{F_M}$ line is low thus activating the fraction register, the $S/\overline{P}$ is low thus setting the register in the parallel mode, and the output from the SELECT gate is "1". At the first positive going edge of the clock, the 10-bit shift/load register is reset. In the second positive edge of the clock, nine of the flip-flops are set. This is because the date line, $D_O$, is at logic "0" in the first clock and at logic "1" in the second clock. The resetting and setting action of this register result in a positive going edge at its output. This positive going edge triggers the upper eight flip-flops and causes the latching of the "1" from the SELECT gate. After initialization, the resulting conditions of the fraction register are as shown in Figure 4.29. After initialization is completed, the converter enters the exponent mode. In this mode the fraction register is disabled.

After completion of the exponent mode, the fraction mode starts. In this mode the 10-bit shift/load register is set in the shift mode by the control logic. Each clock the "0" in the most left flip-flop of the shift register is shifted to the right, and at the same time the comparator output, $D_C$, is latched in the corresponding flip-flop of the upper 8 flip-flops. After 8 clocks the "0"
in the shift register is latched in the most right flip-flop. The output of this
flip-flop represents the End-of-Conversion signal, $E_C$. When $E_C$ goes LOW,
the converter enters the wait state. In this state, all parts of the converter
are disabled. The E and the F outputs represent the digital equivalent of the
analogue input.

## 4.7 The Comparator

For dynamic ranges up to about 10 bits, the conventional voltage comparators
implemented in A/D converters are satisfactory. When the dynamic range
is higher than 10 bits, the limitation of the dynamic range of voltage com-
parators that are fabricated in standard processes excludes their use in these
applications.

The dynamic range of the D/A converter is 15 bits. If a linear load is
implemented to convert the current output to a voltage of 5V maximum, the
resulting LSB is equivalent to 0.15mV. In standard bipolar processes it is
difficult to achieve this resolution. If a non-linear load is used, there will be
loss in resolution at low current levels. Therefore, a current comparator is
implemented in this converter.

The current comparator circuit is composed of a resistive network and
three stages of differential amplifiers, as shown in Figure 4.30. The currents
to be compared are $I_{i1}$ and $I_{i2}$. For small values of $\Delta I_i$ ($\Delta I_i = I_{i1} - I_{i2}$), the
current $\Delta I_i$ flows in $R_b$ and $R_i$. $Q_N$ and $Q_P$ remains OFF for small values of
$\Delta I_i$, since the voltage drop across their emitter base is low ($V_{BE} = \Delta I_i R_b < 0.2V$). If $I_{i1}$ is slightly greater than $I_{i2}$, the current $\Delta I_i$ flows in the direction
indicated in the figure, and vice versa.

The voltage level at point B (see Figure 4.30) is about $V_{cc}/2$, because of
the equal values of $R_1$ and $R_2$. The voltage level at point A is higher or lower
than that at point B, depending on the direction of the current flowing in $R_i$.
Since the value of $R_i$ can be very high ($\geq 50k\Omega$), a small value of $\Delta I_i$, in the
range of a few tens of nano amperes produces a voltage difference between
points A and B in the order of few milli volts.

Since the output of a comparator can take only one of two possible states,
the amount of the current flowing in $R_i$, for the proper operation of the circuit,
is not critical. Only the direction of the current flowing in $R_i$ is important for
the comparison operation. A minimum value of $\Delta I_i$ of about $50nA$ is found
to be satisfactory for the proper operation, which is equal to $\frac{1}{2}$ LSB.

When the difference current, $\Delta I_i$ is more than a few micro amperes, the
voltage drop developed across $R_b$ switches one of the transistors $Q_N$ and $Q_P$
ON, depending on the polarity of $\Delta I_i$. When $\Delta I_i$ is in the direction indicated
in Figure 4.30, \( Q_P \) is switched ON and \( Q_N \) remains OFF. The remainder of \( \Delta I_i \) (in excess of few micro amperes flowing in \( R_i \)) sinks to the GND. However, when \( I_{i2} \) is larger than \( I_{i1} \), \( Q_N \) is switched ON and \( Q_P \) is OFF. The excess current is supplied by the power supply through \( Q_N \). The effect of \( Q_N \) and \( Q_P \) is an increase in the transit time of the comparator caused by their parasitic capacitances.

The performance of this circuit is not sensitive to mismatch of the resistive network or the absolute value of the resistors. For example, if there is a mismatch between \( R_1 \) and \( R_2 \) as high as 10%, it has no effect on the circuit’s performance.

The implementation of the Darlington pair in the differential stage is necessary to increase the input resistance of the differential stage, and, therefore, the input current to this stage remains small. If this is not the case, the base current to this stage largely influences the current flowing in \( R_i \). The intermediate stage consisting of \( Q_5 \) to \( Q_7 \), \( R_6 \) and \( R_7 \) is used for further amplification of the signal.

The final stage, consists of \( Q_{11} \) to \( Q_{18} \) offers more gain and converts the output voltage to the required EFL logic levels.

Figure 4.31 shows the comparator output voltage as a function \( \Delta I_i \). Only a 50nA input current at the input is sufficient to produce a full voltage swing at the output. From the figure, it can be seen that there is an offset of about 23nA, which is caused by the base currents of \( Q_1 \) and \( Q_2 \). Therefore, the Darlington configuration is implemented in this stage to minimize this offset. Moreover, this stage is also biased at low currents for the same reason.

For a good comparison of the transit time of voltage comparators, the
output voltage is plotted for a step input voltage of 100mV plus a small amount (overdrive). In this respect, the response time of this comparator is characterized for a step input current of 1mA plus an overdrive. Figure 4.32 shows the response time for various input overdrives of 50nA, 200nA, 1µA and 5µA. The worst-case response time is less than 200ns for 50nA overdrive.

Figure 4.31. The comparator output voltage as a function of $\Delta I_i$.

Figure 4.32. The comparator response time for various input overdrives of 50nA, 200nA, 1µA and 5µA.
4.8 A Bipolar Floating-Point A/D Converter

Figure 4.33 shows the block diagram of the complete floating-point A/D converter. The converter was fabricated in a standard bipolar process (DIMES-01). The die area is $3.4 \times 4.8$ mm. Figure 4.34 shows the chip photograph of the complete A/D converter.

Figure 4.33. The block diagram of the complete floating-point A/D converter.
Chapter 4. Architecture of the Floating-Point A/D Converter

Figure 4.34. The chip photograph of the floating-point A/D converter.

4.9 Conclusions

In this chapter several methods for realizing an accurate binary-weighted digitally-programmable current source have been discussed. These programmable current sources are implemented as a linear or non-linear current source.

The base current error in the mirror and the cascode transistors is cancelled to first approximation due to the binary scaling of the transistors. The most significant error in the programmable current sources is caused by mismatch of transistors, and due to variation in processing parameters and variations in the bias conditions due to the aluminium interconnect. This error was reduced by using a relatively large emitter area for the mirror transistors, and using symmetrical layout.
Chapter 5

Compatibility Between ICs and Sensors

5.1 Introduction

In standard bipolar integrated circuits, used for analogue and digital signal processing, the process parameters, such as the doping levels, temperature, and epitaxial layer thickness, are optimized to give high performance components for the specific function required by the integrated circuits. Since the n-p-n bipolar transistor is the most important element in bipolar integrated circuits, mainly because of the higher electron mobility than holes, most processing parameters are designed mainly to yield a high performance n-p-n transistor. Other components, such as the lateral p-n-p, although less critical, should have a reasonable performance.

The fabrication of silicon-based sensors usually follows a non-standard processing sequence [24, 33, 25]. In many cases the standard processing steps may remain the same, but the impurity level, temperature, dose or energy may need to be altered for optimum sensor performance. Additional compatible processing steps must often be added during the fabrication of many sensor types, such as the post-processing annealing for the removal of the residual stress [27, 28], deposition of piezoelectric or magnetic thin or thick films [30, 31, 32]. The additional processing steps required by the sensor processing may lead to changes in the structure of active bipolar components and in a reduction of their performance.

As was discussed in section 1.4, in bulk micromachining, the thickness of the free-standing membrane is equal to the epitaxial layer thickness and, therefore, the epilayer thickness determines the mechanical properties of the micromechanical structure, such as the sensitivity and the resonance fre-
frequency. However, the epilayer width and doping concentrations also affect the performance of the integrated transistors. In surface micromachining, stresses are present in the free-standing structural layers. These stresses are reduced by a high (≈ 1000°C) temperature annealing step [27, 28], which affects the bipolar elements fabricated in the same wafer.

In this chapter theoretical and simulation results of the changes in some of the DC parameters of the n-p-n and the lateral p-n-p transistors are presented. The base width, the common emitter current gain and the Early voltage are discussed in sections 5.2, 5.3 and 5.4, respectively. Sections 5.5, 5.6 and 5.7 discuss the breakdown voltages, the knee current, and the collector-base reverse leakage current, respectively. Section 5.8 presents the changes in $\beta_F$ and the Early voltage that result from a high-temperature post-processing annealing step.

5.2 The Base Width

n-p-n

The base width of the bipolar transistor is one of the most important parameters in transistor design. Figure 5.1 shows a typical vertical doping profile of an integrated n$^+$-p-n bipolar junction transistor. The base width is defined as the distance between the two junctions. As can be seen from the figure, the base width largely depends on the epitaxial layer doping concentration. Table 5.1 summarizes the most important steps of the process used to fabricate the test transistors. A one-dimensional simulation of the processing steps, carried out using SUPREM-3 [68], results in the net active doping profile shown in Figure 5.2. To be able to determine the base width as a function of the epilayer doping concentration, the simulation was repeated for several epilayer doping concentrations. The resulting base width is shown in Figure 5.3. From the base width dependence on the epitaxial layer doping concentration, several transistor parameters can be related to the epilayer doping concentration.

Lateral p-n-p

The lateral p-n-p transistor normally has a larger base width than the vertical n-p-n transistor. The base width of the p-n-p is determined by the distance between the emitter and collector masks, $W_M$, minus the lateral diffusion in the two sides, as shown in Figure 5.4. In this type of lateral p-n-p transistor the base region is formed in the unmodified epitaxial layer. Figure 5.5 shows TSUPREM-4 [69] results of the equi-doping concentration
5.2. The Base Width

<table>
<thead>
<tr>
<th>Step</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>Initialization: silicon p-type substrate, &lt;100&gt;, 3.5 Ωcm.</td>
</tr>
<tr>
<td>2</td>
<td>Buried-n implantation and annealing, (antimony).</td>
</tr>
<tr>
<td>3</td>
<td>Epitaxial layer growth, (arsenic), The epilayer thickness and doping concentration are used as variables.</td>
</tr>
<tr>
<td>4</td>
<td>Deep-p deposition and drive-in (boron).</td>
</tr>
<tr>
<td>5</td>
<td>Deep-n deposition and drive-in: (phosphorus).</td>
</tr>
<tr>
<td>6</td>
<td>Base implantation annealing, (boron).</td>
</tr>
<tr>
<td>7</td>
<td>Emitter implantation and annealing, (arsenic).</td>
</tr>
<tr>
<td>8</td>
<td>Post-processing annealing, one of the following (1) for 30 min. at 1000°C (2) for 60 min. at 1000°C (3) for 30 min. at 1100°C (4) for 60 min. at 1100°C.</td>
</tr>
</tbody>
</table>

Table 5.1. Outline of the bipolar processing steps.

![Doping Profile Diagram](image_url)

Figure 5.1. A typical doping profile of an integrated $n^+$-p-n bipolar transistor.
Figure 5.2. The net-active doping profile of an n-p-n.

Figure 5.3. The base width versus the epilayer doping concentration.
5.2. The Base Width

contours of the emitter or collector boron implantation.

![Diagram of epitaxial layer](image)

epitaxial layer

Figure 5.4. *Cross-section of the lateral p-n-p transistor.*

![Graph of equi-doping concentration](image)

Figure 5.5. *Equi-doping concentration of the emitter or collector implantation.*

The base width as a function of the epitaxial layer doping concentration can be obtained from this result. Assuming an initial emitter-to-collector mask separation, $W_M$, of 4 microns, the base width is plotted versus the epilayer doping concentration shown in Figure 5.6.

The base width shown in Figures 5.3 and 5.6 is the distance between the collector-base and the emitter-base junction. The effective base width is decreased by the depletion regions at the two sides.
5.3 The Current Gain

The common emitter forward current gain is defined as $\beta_F = I_C / I_B$. The expression for $\beta_F$ can be derived using a simplified model in which a constant emitter and base doping levels are assumed and can be written as [52]:

$$\beta_F = \frac{1}{\frac{W_B^2}{2L_B^2} + \frac{D_B W_B N_B}{D_B L_E N_E}} \quad (5.1)$$

where $W_B$ is the base width, $L_B$ ($D_B$) and $L_E$ ($D_E$) are the minority carriers diffusion lengths (coefficients) in the base and emitter, respectively, and $N_B$ and $N_E$ are the base and emitter doping concentrations, respectively.

n-p-n

For the vertical n-p-n, equation (5.1) can be modified as:

$$\beta_{F,npn} = \frac{1}{\frac{W_B^2}{2L_n^2} + \frac{D_n W_B N_B}{D_n L_p N_E}} \quad (5.2)$$

where $L_n$ and $L_p$ are the diffusion lengths of the electron and holes minority carriers in the base and emitter, respectively, and $D_n$ and $D_p$ are the electron and holes diffusion coefficients.
Figure 5.7 shows a plot of the common emitter current gain versus the epitaxial layer doping concentration. Equation (5.2) is used in plotting the figure with \( L_p = 1 \mu m \), \( L_n = 4 \mu m \) [70], \( N_E/N_B = 60 \), \( D_n/D_p = \mu_n/\mu_p = 1100/470 \), and the data for the base width is obtained from the simulation results in Figure 5.3. The values of the mobilities used are approximated from the concentration-dependent mobility curves [71].

![Graph showing \( \beta_F \) of the n-p-n versus \( N_{epi} \).](image)

From Figures 5.3 and 5.7, we see that by lowering the epitaxial layer doping concentration a larger base width results, which in turns lowers the current gain of the transistor.

Lateral p-n-p

Using the proper notation in equation (5.1), the common emitter current gain of the lateral p-n-p can be written as:

\[
\beta_{F, pnp} = \frac{1}{\frac{W_p^2}{2L_p^2} + \frac{D_nW_pN_{epi}}{D_pL_nN_E}}.
\]  

(5.3)
Figure 5.8 shows a plot of the common emitter current gain as a function of the epitaxial layer doping concentration. In plotting the figure the following values were used: \( L_p = 10\mu m \), \( L_n = 5\mu m \), \( N_E = 1 \times 10^{18} \text{cm}^{-3} \), \( D_n/D_p = \mu_n/\mu_p = 400/470 \). The values of the mobilities are approximated from the concentration-dependent curves [71].

![Figure 5.8. \( \beta_F \) of the lateral p-n-p versus \( N_{epi} \).](image)

For the lateral p-n-p, the common emitter current gain decreases with an increase in the epilayer doping for two reasons. Firstly, the base transport factor decreases due to the increase in the base width, and secondly, the emitter efficiency decreases because of the increase in the base-to-emitter doping concentration ratio, \( N_B/N_E \). Note that \( N_B = N_{epi} \) in this case.

### 5.4 The Early Voltage

**n-p-n**

The Early voltage, \( V_A \), of the bipolar transistor indicates how the collector-base voltage drop, \( V_{CB} \), affect the collector current and is defined as:

\[
V_A = -\left. \frac{I_C}{\partial V_{CB}} \right|_{V_BE}.
\]  

(5.4)
Equation (5.4) does not indicate a direct relation between $I_C$ and $V_{CB}$. However, the base width $W_B$ is modulated by $V_{CB}$ [72], thus:

$$I_C = \frac{qAD_n n_{p0}}{W_B} \exp\left(\frac{qV_{EB}}{kT}\right) = \frac{qAD_n n_{p0}}{W_B(V_{CB})} \exp\left(\frac{qV_{EB}}{kT}\right).$$  \hspace{1cm} (5.5)

An expression for the collector-base depletion layer width at the base is given in a later section (equation (5.19)) and yields:

$$W_B(V_{CB}) = W_{B0} - \sqrt{\frac{2\varepsilon_s N_{epi}}{qN_B(N_B + N_{epi})}} V_{CB},$$  \hspace{1cm} (5.6)

where $W_{B0}$ is the base width at $V_{CB} = 0$.

The differential change in $I_C$ with respect to $V_{CB}$ is given by:

$$\frac{\partial I_C}{\partial V_{CB}} = \frac{\partial I_C}{\partial W_B} \times \frac{\partial W_B}{\partial V_{CB}}$$

$$= -\frac{qAD_n n_{p0}}{W_B(V_{CB})} \exp\left(\frac{qV_{EB}}{kT}\right) \times -\sqrt{\frac{2\varepsilon_s N_{epi}}{qN_B(N_B + N_{epi})}} \frac{1}{2\sqrt{V_{CB}}}. $$  \hspace{1cm} (5.7)

Substituting equation (5.5) and (5.7) into (5.4) we obtain:

$$V_A = -\frac{I_C}{\partial I_C/\partial V_{CB}} = \frac{qAD_n n_{p0}}{W_B(V_{CB})} \exp\left(\frac{qV_{EB}}{kT}\right) \sqrt{\frac{\varepsilon_s N_{epi}}{2qN_B(N_B + N_{epi}) V_{CB}}}$$

$$= \frac{W_{B0} - \sqrt{\frac{2\varepsilon_s N_{epi}}{qN_B(N_B + N_{epi})}} V_{CB}}{\sqrt{\frac{\varepsilon_s N_{epi}}{2qN_B(N_B + N_{epi}) V_{CB}}}}. $$  \hspace{1cm} (5.8)

At this stage it is important to calculate the amount of charge per unit area of the majority charge carriers in the base, and the small-signal junction capacitance per unit area. The majority charge carrier per unit area in the base is given by:

$$Q_B = qN_B W_B(V_{CB}) \approx qN_A(W_{B0} - \Delta W_B).$$  \hspace{1cm} (5.9)

The small-signal junction capacitance per unit area is equal to:

$$C_{ch} = \frac{dQ_B}{dV_{CB}} = -qN_B d(\Delta W_B) = -qN_B d\left(\sqrt{\frac{2\varepsilon_s N_{epi}}{qN_B(N_B + N_{epi}) V_{CB}}}\right)$$

$$= -qN_B \sqrt{\frac{\varepsilon_s N_{epi}}{2qN_B(N_B + N_{epi}) V_{CB}}}. $$  \hspace{1cm} (5.10)
Combining equations (5.8) and (5.9) into (5.10) yields:

\[ V_A = \frac{Q_B}{C_{cb}}. \]  

(5.11)

The values of \( Q_B \) and \( C_{cb} \) depend on \( V_{CB} \), and therefore on \( V_A \). In the following analysis, the base-collector voltage dependence of \( V_A \) itself is neglected and the Early voltage is approximated by its value at \( V_{BC} = 0 \). The small-signal junction capacitance at \( V_{CB} = 0 \) is:

\[ C_{cb} = \sqrt{\frac{q \varepsilon_s N_B N_{epi}}{2(N_B + N_{epi}) V_{bi}}} \frac{1}{V_{bi}}, \]  

(5.12)

where

\[ V_{bi} = \frac{kT}{q} \ln \left( \frac{N_B N_{epi}}{n_i^2} \right). \]  

(5.13)

For a uniformly doped base

\[ Q_B = q N_B W_B. \]  

(5.14)

Substituting equations (5.12) and (5.14) into (5.11) yields:

\[ V_{A,npn} = \sqrt{\frac{2q N_B W_B^2 (N_B + N_{epi})}{\varepsilon_s N_{epi}}} V_{bi}. \]  

(5.15)

Figure 5.9 shows the Early voltage as a function of the epilayer doping concentration, which in this case is the collector region, \( (N_C = N_{epi}) \). The value of \( W_B \) used in plotting this figure is obtained from the SUPREM-3 simulation results given in Figure 5.3.

For a good transistor performance, the value of \( V_A \) should be as large as possible. To increase \( V_A \) the base region should be highly doped with respect to the collector and a large base width is required. These two requirements oppose the requirements of high current gain and high cut-off frequency of the transistor. Therefore, a compromise should be implemented for optimum transistor performance.
5.4. The Early Voltage

Figure 5.9. The Early voltage for the n-p-n versus $N_{epi}$.

**Lateral p-n-p**

Modifying equation (5.15) for the lateral p-n-p transistor results in:

$$V_{A_{pnp}} = \sqrt{\frac{2qN_{epi}W_B^2(N_{epi} + N_C)}{\epsilon_s N_C}} V_{bi}.$$  \hspace{1cm} (5.16)

Figure 5.10 shows the Early voltage for the p-n-p transistor as a function of the epilayer doping concentration with the collector-to-emitter mask separation, $W_M$, as a parameter. The conclusion already drawn for the n-p-n transistor is also valid for the lateral p-n-p transistor.
Figure 5.10. *The Early voltage for the p-n-p versus $N_{\text{epi}}$.\*

### 5.5 Transistor Breakdown

Breakdown of the bipolar junction transistor can be due to the breakdown of either of the two junctions or due to the punch-through (or reach-through). The punch-through breakdown occurs when the quasi-neutral base region is fully depleted. The breakdown of the emitter-base or the collector-base junction is due to Avalanche multiplication or tunnelling in junctions doped with concentrations of about $10^{18}$ atoms/cm$^3$ and higher.

In the normal forward operation of the bipolar transistor, the emitter-base junction is forward biased, while the collector-base junction is reversed biased. In this mode of operation, the transistor can breakdown due to either the collector-base junction breakdown or the full depletion of the quasi-neutral base region. These two processes are independent and the region in which the collector current becomes highly dependent on the reverse collector-base voltage will occur whenever one of them occurs.

In the following subsections a brief introduction to the breakdown processes is given, followed by discussion of the integrated vertical n$^+$-p-n-n$^+$ and lateral p-n-p transistor breakdown voltages.
5.5. Transistor Breakdown

5.5.1 Avalanche Breakdown

When the applied reverse voltage of a p-n junction is increased, the depletion layer width increases as well as the resulting electric field. The free carriers in the depletion region are accelerated by the electric field; holes are drifted to the p side and electrons to the n side of the junction. Above a certain threshold in the field (known as the critical electric field), the charge carriers gain enough energy to ionize atoms and, therefore, generate electron-hole pairs giving rise to a large current amplification. This process is known as avalanche multiplication.

The breakdown voltage of a single-sided abrupt junction is given by [14]:

\[ BV_{CB0} = \frac{\epsilon_e \varepsilon_c^2}{2qN_L}, \]  

(5.17)

where \( \varepsilon_c \) is the critical electric field at breakdown voltage, \( \epsilon_e \) the permittivity of the semiconductor material, \( q \) the elementary charge, and \( N_L \) the concentration of the lower doped side of the junction. The dashed curve in Figure 5.11 shows the junction breakdown voltage versus the concentration of the lightly doped layer, which in this case is the epilayer. The other curves show the breakdown due to other mechanisms, and will be discussed later.

For junctions with doping concentrations of \( 10^{18} \) atoms/cm\(^3\) and higher, the breakdown is mainly due to the tunnelling process. The collector region of the integrated n-p-n transistor is normally doped with concentrations less than \( 10^{17} \) atoms/cm\(^3\). Therefore, the tunnelling process at the collector-base junction is insignificant. The tunnelling process can be important in the emitter-base junction, but this junction is forward biased in the normal mode of operation of the transistor.

5.5.2 Punch-through

When a bipolar transistor is operated in the normal forward mode, the collector-base depletion region width is expected to increase with increasing the collector-base voltage. When the collector-base voltage is increased so that the emitter-base and the collector-base depletion regions touch each other, any further increase in the reverse collector-base voltage causes the potential barrier at the emitter-base junction to decrease, allowing a large injection of the minority carriers from the emitter directly to the collector-base depletion region. Therefore, only a slight increase in the collector-base voltage causes a large increase in the collector current.
5.5.3 Breakdown Voltages of the Integrated Transistor

n-p-n

For a transistor in the common-emitter configuration with the collector-base junction reverse biased, electron-hole pairs are produced by the avalanche process at the collector-base junction. In the case of an n-p-n transistor, holes are drifted to the base and electrons to the collector. This avalanche hole current injected into the base is amplified by the transistor action. The value of the collector-to-emitter voltage, $BV_{CEO}$, at which the transistor breakdown
occurs is less than the collector-base junction breakdown given previously by equation (5.17), and can be expressed in terms of the junction breakdown as [52]:

\[ BV_{CE0} = \frac{BV_{CB0}}{\sqrt{\beta_F}}. \]  

(5.18)

The dotted curve in Figure 5.11 shows \( BV_{CE0} \) with \( \beta_F = 100 \) and \( n = 6 \).

In the practical integrated n^+-p-n-n^+ bipolar transistor, the base is highly doped with respect to the collector region (see Figure 5.2). The buried-n layer is normally highly doped with respect to the base region. Initially, the collector-base depletion region extends almost entirely into the lightly-doped collector region. When the collector-base reverse voltage increases, this region becomes fully depleted and any further increase in the collector-base voltage causes a significant increase in the depletion region to the base side. Figure 5.12 shows the four regions of a uniformly-doped n^+-p-n-n^+ transistor, namely, the emitter, the base, the lightly doped collector (epilayer) and the highly doped collector region (buried-n layer). Using the abrupt junction approximation, the depletion layer width in the base region, \( W_{CB1} \), when the collector-base voltage is less than the voltage, \( V_{CBF} \), required to deplete the entire lightly doped collector region, \( W_C \), is given by:

\[ W_{CB1} = \frac{2\varepsilon_s(V_{CB} + V_{bi})}{qN_B \left(1 + \frac{N_B}{N_{epi}}\right)}. \]  

(5.19)

\[ \text{emitter} \quad \text{base} \quad \text{epilayer} \quad \text{buried-n} \]

\[
\begin{array}{c}
N_E \\
N_B \\
N_{epi} \\
N_{n+}
\end{array}
\]

\[ W_{CB1} \quad W_C \]

Figure 5.12. *The four regions of the integrated n^+-n-p transistor.*

Taking the derivative with respect to the collector-base voltage, and neglecting the built-in voltage yields:

\[ \frac{dW_{CB1}}{dV_{CB}} = \frac{\varepsilon_s}{2qN_B \left(1 + \frac{N_B}{N_{epi}}\right) V_{CB}}. \]  

(5.20)
However, when \( V_{CB} \) is larger than \( V_{CBF} \), i.e. the lightly doped collector region is fully depleted, the differential change in the depletion region in the base side, \( W_{CB2} \), with respect to \( V_{CB} \), is given by the same formula, only \( N_{epi} \) should be replaced by \( N_{n+} \).

\[
\frac{dW_{CB2}}{dV_{CB}} = \frac{\varepsilon_s}{\sqrt{2qN_B \left( 1 + \frac{N_{n+}}{N_{epi}} \right)V_{CB}}}.
\]  (5.21)

From equations (5.20) and (5.21) above, the ratio of the differential change in the collector-base depletion region to the base side when the lightly doped collector region is fully depleted \( (V_{CB} > V_{CBF}) \) to that when it is partially depleted \( (V_{CB} < V_{CBF}) \) is:

\[
\frac{dW_{CB2}}{dV_{CB}} = \frac{1 + \frac{N_B}{N_{epi}}}{1 + \frac{N_B}{N_{n+}}}.
\]  (5.22)

Substituting \( N_B = 1 \times 10^{17}, N_{epi} = 1 \times 10^{15} \), and \( N_{n+} = 1 \times 10^{19} \) in the above equation, gives a value of 10. This means that the base-width mod-ulation, when the low doped collector region is fully depleted, is about 10 times higher than that when it is not fully depleted. This sudden increase in the base width modulation causes a significant change in all of the transistor parameters that depend on the base width. Therefore, the collector-base voltage which causes full depletion of the lightly doped collector region, \( V_{CBF} \), is an important parameter, since most of the transistor parameters suffer from a large collector-base voltage dependence beyond this voltage. Using the single-sided abrupt junction approximation, the collector-base junction voltage, \( V_{CBF} \), required to deplete the entire low doped collector region, \( W_C \), of the \( n^+\)-\( p\)-\( n\)-\( n^+ \) transistor is:

\[
V_{CBF,npn} = V_{CB} + V_{bi} = \frac{qN_{epi}W_C^2}{2\varepsilon_s}.
\]  (5.23)

Figure 5.11 include plots of \( V_{CBF} \) as a function of \( N_{epi} \) and the initial epilayer thickness, \( W_{epi} \), as a parameter. The initial epilayer thickness is the thickness of the epilayer that is grown at the beginning of the process after the buried-\( n \) formation. The value of \( W_C \) is much less than \( W_{epi} \) because of the up-diffusion of the buried-\( n \), the part of the epilayer forming the emitter and the base regions and lastly the part of the epilayer that is etched away during processing. The values of \( W_C \) are obtained from SUPREME-3 simulations assuming an initial epitaxial layers thickness equals to \( W_{epi} \). From this figure it can be see that if high breakdown voltage for transistors manufactured
5.5. Transistor Breakdown

in lightly doped epitaxial layers is required, a large epitaxial layer thickness must be used.

The breakdown of the integrated n-p-n transistor can also occur because of punch-through, especially if the base width is very short compared to the thickness of the low-doped collector region, \( W_C \). The width of the depletion region in the base at the emitter junction is given by:

\[
W_{EB} = \frac{2\varepsilon_s V_F}{q N_B \left( 1 + \frac{N_B}{N_E} \right)},
\]

(5.24)

where \( V_F \) is the forward emitter-base junction voltage.

Similarly, the depletion layer width in the base at the collector junction is given by:

\[
W_{CB} = \frac{2\varepsilon_s V_j}{q N_B \left( 1 + \frac{N_B}{N_C} \right)},
\]

(5.25)

where \( V_j = V_{CB} + V_{bi} \).

The punch-through condition occurs when the sum of the two depletion regions is equal to the base width, i.e.

\[
W_B = W_{EB} + W_{CB} = \sqrt{\frac{2\varepsilon_s V_F}{q N_B \left( 1 + \frac{N_B}{N_E} \right)}} + \sqrt{\frac{2\varepsilon_s V_{jp}}{q N_B \left( 1 + \frac{N_B}{N_C} \right)}},
\]

(5.26)

where \( V_{jp} \) is the collector-base junction voltage at punch-through condition. After algebraic manipulation and substituting \( N_{epi} \) for \( N_C \) equation (5.26) yields:

\[
V_{jp,npn} = \frac{q N_B \left( 1 + \frac{N_B}{N_{epi}} \right)}{2\varepsilon_s} \times \left( W_B - \frac{2\varepsilon_s V_F}{q N_B \left( 1 + \frac{N_B}{N_E} \right)} \right)^2.
\]

(5.27)

The dot-dashed curve in Figure 5.11 shows the plot of \( V_{jp} \) as a function of \( N_{epi} \) for the n-p-n. The value of \( V_F \) is taken to be equal to 0.8 Volt. For such a transistor with a relatively large base width (see Figure 5.3), the collector-base voltage which causes punch-through is always larger than the junction breakdown voltage when the epilayer doping concentration is less than about 4x10^{16} atoms/cm^{3}.
Lateral p-n-p

In the simple, integrated lateral p-n-p transistors, the entire collector region is normally doped with a concentration higher than that used for the base region. The base region in this case is the unmodified epitaxial layer. For this reason, the base-width modulation in the p-n-p transistor is much larger than that of the n-p-n transistor. The depletion region in the base at the emitter and the collector junctions are given by the same equations as that for the n-p-n transistor. Therefore, the condition for the punch-through is given by equation (5.26). Taking into account that \( N_E = N_C = N \) and \( N_B = N_{epi} \) for the p-n-p, the collector-base voltage required to deplete the entire base region, \( V_{jp,pnp} \), is:

\[
V_{jp,pnp} = V_{CB} + V_{bi} = \left( \frac{\sqrt{qN_{epi}W_B^2 (1 + \frac{N_{epi}}{N})}}{2\epsilon_s} + \sqrt{V_F} \right)^2.
\]  \hspace{1cm} (5.28)

Using the values of \( W_B \) obtained from TSUPREM-4 simulation and shown in Figure 5.6, the punch-through voltage versus the epitaxial layer doping concentration is shown in Figure 5.13, with the emitter-to-collector mask separation, \( W_M \), as a parameter. The dashed curve shows the junction breakdown. The value of \( V_F \) is taken to be 0.8 V. As can be seen from the figure, a large base width is required for transistors made in lightly doped epitaxial layers in order to obtain acceptable breakdown voltage. This automatically implies poor transistor parameters such as current gain and cut-off frequency.

5.6 High-level Injection

When bipolar transistors are operated at increased current levels, violation of the low-level injection assumption takes place, which usually first becomes apparent either at locations where there is a high density of injected minority carriers or else where there is a low density of dopant atoms available. Since the simple bipolar junction transistor consists of two junctions, the increase in the collector current can lead to two independent high-level effects. The first caused by the injection of the charge carrier from the highly doped emitter into the base, while the second is due to the injection from the base into the low-doped collector region (in the case of the n-p-n transistor).
Figure 5.13. Breakdown voltages of the p-n-p versus \( N_{\text{epi}} \); the dashed curve shows the junction breakdown and the solid curves show the punch-through with \( W_M \) as a parameter.

5.6.1 High-level Injection at the Base

n-p-n

The collector current density of an \( n^+\)-p-n transistor in the active forward operation is given by [52]:

\[
J_C = q D_n \frac{n_p(0)}{W_B}.
\] (5.29)

Therefore, the amount of charge carriers injected from the emitter to the base as a function of the collector current is equal to:

\[
n_p(0) = \frac{J_C W_B}{q D_n}.
\] (5.30)

As long as the concentration of the injected charge, \( n_p(0) \), is much less than the majority-carrier density in the base, low-level injection conditions are satisfied and the base minority-carrier lifetime remains constant. However,
when the minority-carrier density becomes comparable with the majoritycarrier density, the majority-carrier density is locally increased to maintain charge neutrality in the base. This causes a decrease in the current gain for two reasons. The first reason is that the base transport factor given by:

$$\alpha_T = \frac{1}{1 + \left( \frac{W_B^2}{2r_B D_B} \right) \tau_B},$$  

(5.31)

will decrease due to the decrease in the effective minority carrier lifetime, $\tau_B$, in the base. Secondly, the increase in the majority-carrier density represents an effective increase in the base doping density. This causes a decrease in the emitter injection efficiency given by:

$$\gamma = \frac{1}{1 + \left( \frac{D_B W_B N_E}{D_B L_E N_B} \right)}.$$  

(5.32)

The collector current level at which these effects become significant can be obtained by equating equation (5.30) to the base doping density. Therefore, the collector current density at which high injection effects in the base become significant is given by:

$$J_{C,B} = \frac{q N_B D_n}{W_B}.$$  

(5.33)

For collector current densities above $J_{C,B}$, the current gain reduces because of the decrease in the base transport factor and the emitter injection efficiency as discussed above.

The solid curve in Figure 5.14 shows $J_{C,B}$ versus $N_{epi}$. Note that $J_{C,B}$ is indirectly related to $N_{epi}$ via $W_B$. The dashed line shows the collector current density at which high-level injection occurs at the collector-base junction, this is discussed in section 5.6.2.

**Lateral p-n-p**

For the integrated lateral p-n-p transistor, however, the base region is the most lightly doped region in the transistor. Therefore, the maximum collector current density is limited by the high-level injection in the base. Figure 5.15 shows plots of the collector current density at which the density of the injected charge is equal to the majority carrier concentration in the base versus the epilayer (base) doping concentration. The emitter-to-collector mask separation, $W_M$, is used as the parameter. Note that the base region, in this case, is the unmodified epilayer concentration.
5.6. High-level Injection

![Graph showing high-level injection vs. N_{epi} for the n-p-n, J_{C,B} solid line, J_{C,C} dashed line.]

Figure 5.14. High-level injection versus N_{epi} for the n-p-n, J_{C,B} solid line, J_{C,C} dashed line.

5.6.2 High-level Injection Effects at the Collector

Lateral n-p-n

In a typical n-p-n amplifying integrated transistor, the minimum doped region occurs in the collector, close to the base (see Figure 5.2). This region is essential for several reasons. It allows for a significant increase in the breakdown voltage of the collector-base junction, it reduces the collector capacitance, and it reduces the Early effect. The maximum collector current that can flow in the transistor without the occurrence of a significant drop of the current gain is limited by this low doped collector region. When a collector current density of J_C is flowing through the collector-base space-charge region, the maximum drift velocity of the charge carrier is limited to v_t, where v_t is the scattering-limited velocity \(v_t = 1.07 \times 10^7 \text{ and } 8.34 \times 10^6 \text{ cm/s at } 300^\circ \text{K for electrons and holes, respectively [72]}\). Therefore, the charge density present in the collector-base depletion region from the flowing collector current, \(N_{JC}\), is given by:

\[
N_{JC} = \frac{J_C}{q v_t}.
\]  

(5.34)
When this charge density becomes comparable to the low doped collector region concentration (epilayer), the quasi-neutral base region starts to widen. As the collector current is increased above this level, a significant change in transistor parameters occurs. By equating equation (5.34) to the epitaxial layer doping concentration, \( N_{epi} \), the collector current density at which the transistor parameters start to change significantly due to high level injection at the collector is given by:

\[
J_{C,C} = qN_{epi}v_l.
\]  

(5.35)

From this equation, it can be concluded that the maximum collector current density, beyond which the transistor parameter starts to degrade, is linearly proportional to the dopant concentration of the epitaxial layer doping concentration. The dashed line in Figure 5.14 shows the critical collector current density, \( J_{C,C} \), versus \( N_{epi} \) for the \( n^+-p-n \) transistor.

In the \( n^+-p-n \) transistors made in epitaxial layers with doping concentra-
tions of less than about $9 \times 10^{18}$ atoms/cm$^3$, the maximum collector current is limited by the high-level effects at the collector-base junction, while for transistors made in epitaxial layers doped with higher concentrations, the maximum collector current is limited by the high-level injection at the emitter-base junction.

**Lateral p-n-p**

In the case of the lateral p-n-p transistor, usually the emitter and the collector are made by the same diffusion or implantation process, and, therefore, have the same doping concentration. In this case, the doping concentration of the collector is higher than the base dopant concentration. Therefore, high-level injection at the collector is irrelevant in this case. The maximum allowed collector current is only limited by high-level injection at the emitter-base junction as discussed previously.

The effect of high-injection phenomena is usually extracted from measurements using the Gummel plots ($I_C$, $I_B$ versus $V_{EB}$) and using the deviation from the $\exp(qV_{EB}/kT)$ curve on a log scale.

## 5.7 Reverse Leakage Current

When a p-n junction is reverse biased, three current components contribute to the reverse leakage current. One component is due to the charge carrier generated in the depletion region, the other two components are due to thermally generated charge carriers in the neutral regions in the vicinity of the depletion region that diffuse to the edge of the depletion region. Since the collector-base junction of the bipolar transistor is reverse biased in the normal mode of operation, the three current component contribute to the collector-base reverse leakage current.

When electron-hole pairs are generated in the depletion region, electrons are swept by the electric field present in the depletion region to the n-side, and holes to the p-side. This process gives rise to a current density of $J_g$, which is shown [73] to be equal to:

$$J_g = \frac{qn_t W}{2\tau_g},$$  \hspace{1cm} (5.36)

where $\tau_g$ is the effective lifetime within the reverse biased depletion region, and $W$ the width of the depletion region and is given by:

$$W = \sqrt{\frac{2eV_{CB}}{qN_{epi}}},$$  \hspace{1cm} (5.37)
for a single-sided abrupt junction. By substituting equation (5.37) into equation (5.36), the generation current density in the n$^+$-p-n-n$^+$ transistor is given by:

$$J_g = \frac{n_i}{\tau_g} \sqrt{\frac{q\epsilon V_{CB}}{2N_{epi}}}.$$  

(5.38)

Figure 5.16 shows the generation current density versus the epilayer doping concentration and the reverse collector-base voltage as a parameter, $\tau_g$ is taken to be $10\mu$s [74, 75]. From the figure it can be seen that the generation current in the depletion region increases exponentially when the epilayer doping concentration is decreased.

![Figure 5.16. $J_g$ versus $N_{epi}$.](image)

In the neutral n-side of the junction, electron-hole pairs are generated in the vicinity of the depletion region. It is possible for these carriers to arrive to the edge of the depletion region. The parts of the generated holes that reach the edge of the depletion region will then be swept by the electric field to the p-side thus giving rise to a current component $I_{diff,p}$. The resulting current density is shown [73] to be equal to:

$$J_{diff,p} = qD_p \left( \frac{n_i^2}{N_C L_C} \right) = qD_p \left( \frac{n_i^2}{N_{epi} L_C} \right).$$  

(5.39)
Similarly, the current density due to thermally generated electrons in the p-side (base) and drift to the n-side (collector) is given by:

\[ J_{\text{diff},n} = qD_n \left( \frac{n_i^2}{N_B L_B} \right). \]  \hspace{1cm} (5.40)

Figure 5.17 shows the current density due to the holes that are generated in the epitaxial layer and diffused to the neutral base region, as a function of the epitaxial layer doping concentration.

![Graph showing \( J_{\text{diff},p} \) versus \( N_{\text{epi}} \).](image)

\[ J_{\text{diff},p} \text{ [nA/cm}^2\text{]} \]

\( N_{\text{epi}} \text{ [cm}^{-3}\text{]} \)

**Figure 5.17.** \( J_{\text{diff},p} \) versus \( N_{\text{epi}} \).

The total reverse leakage current across the collector base junction is the sum of the three components. For the integrated n\(^{+}\)-p-n transistor, the collector region is normally lightly doped with respect to the base. In this case the electron current component generated in the base is negligible compared to the hole current component generated in the collector region. Therefore, the reverse leakage current density for the n-p-n transistor is given by:

\[ J_{\text{leakage,npn}} = \frac{n_i}{\tau_g} \sqrt{\frac{q\varepsilon_s (V_{CB} + V_{bi})}{2N_{\text{epi}}}} + qD_p \left( \frac{n_i^2}{N_{\text{epi}} L_C} \right). \]  \hspace{1cm} (5.41)

The results presented above can also be applied to the lateral p-n-p transistor, in which the base is lightly doped compared to the collector. In this
case the diffusion current component due to the electrons generated in the collector is small compared to the hole-current component generated in the base. Therefore, the collector-base reverse leakage current density is given by:

\[ J_{\text{leakage},\text{pnp}} = \frac{n_i}{\tau_g} \sqrt{\frac{q \varepsilon_s (V_{CB} + V_{bi})}{2 N_{\text{epi}}}} + q D_p \left( \frac{n_i^2}{N_B L_B} \right). \]  

(5.42)

Note that the base of the lateral p-n-p is formed in the unmodified doping concentration of the epitaxial layer i.e. \( N_B = N_{\text{epi}} \). Therefore, the reverse leakage current density is the same as that for the n-p-n as shown in Figures 5.16 and 5.17.

5.8 The Effect of Post-processing Annealing on the Transistor Characteristics

In some sensor processing it is necessary to subject the die to a high temperature for some minutes [76]. This processing step is essential for the removal of the residual stress on the micromechanical elements [27, 28]. In the following, the effect of this high temperature annealing step on the transistor characteristics is discussed.

The base width is one of the most important transistor parameters that is affected by high-temperature annealing during manufacturing. A one-dimensional simulation of the complete processing sequences required by a typical integrated bipolar transistor is performed using SUPREM-3. To account for the effect of the post-processing annealing, an additional annealing step at 1000°C for 30 or 60 minutes or at 1100°C for 30 or for 60 minutes is added at the end of the standard process.

Figure 5.18 shows the resulting base width of the n-p-n transistor versus \( N_{\text{epi}} \), curve (1) represents the standard process and curves (2) through (5), the standard process with a post-processing annealing step at 1000°C for 30 and 60 minutes, and at 1100°C for 30 and 60 minutes, respectively. From the figure it can be concluded that, for epilayers doped with concentrations of more than \( 2 \times 10^{15} \) atoms/cm\(^3\), the base width decreases when the annealing time and/or temperature is increased, while for low doped epilayers the base width starts to decrease at a relatively low annealing time and temperature, and increases with excessive annealing time and/or temperature.

At high epilayer doping concentrations the decrease of the base is because of the low ratio between the boron and the epilayer doping concentrations.
At low epilayer doping concentrations, at first, the advance of the emitter-base junction is faster than the collector-base junction, but with increasing the annealing time and/or temperature, the advance of the collector-base junction exceeds that of the emitter-base junction mainly because of the high boron to epilayer doping concentration ratio.

![Graph showing the base width as a function of epilayer doping concentration](image)

**Figure 5.18.** The base width of the n-p-n versus $N_{\text{epi}}$, curve (1): standard process and curves (2) and (5), the standard process with a post-processing annealing step at $1000^\circ$C for 30 and 60 minutes, and at $1100^\circ$C for 30 and 60 minutes, respectively.

Figure 5.19 shows plots of the common-emitter current gain of the n-p-n versus $N_{\text{epi}}$. Curve (1) represents the standard process and curves (2) and (5), the standard process with a post-processing annealing step at $1000^\circ$C for 30 and 60 minutes, and at $1100^\circ$C for 30 and 60 minutes, respectively. It can be seen from the figure that there is an improvement in the current gain at high epilayer doping concentrations, but at low doping concentrations, the current gain starts to fall when the annealing temperature and/or time is increasing.

The Early voltage resulting from the effect of the post-processing annealing is plotted in Figure 5.20. The effect of the post-processing annealing is
to decrease the Early voltage, especially at low doped epilayers.

Figure 5.19. $\beta_F$ versus $N_{\text{epi}}$ for the n-p-n, curve (1) for the standard process and curves (2) and (5), the standard process with a post-processing annealing step at 1000°C for 30 and 60 minutes, and at 1100°C for 30 and 60 minutes, respectively.

Figure 5.21 shows the base width of the lateral p-n-p transistor for the standard process and the four cases with the additional annealing step versus the epilayer doping concentration. The base width decreases with increasing the annealing time and/or temperature because of the lateral diffusion of the collector and emitter region. Figure 5.22 shows the resulting common-emitter current gain versus the epilayer doping concentration. From the figure, it can be seen that at high annealing temperatures the current gain is very large due to the resulting short base. Figure 5.23 shows the Early voltage for the p-n-p which decreases with increasing the time and/or the temperature of the annealing step.
Figure 5.20. The Early voltage of the n-p-n versus $N_{\text{epi}}$.

Figure 5.21. The base width of the p-n-p versus $N_{\text{epi}}$. 
Figure 5.22. $\beta_F$ versus $N_{\text{epi}}$ for the p-n-p.

Figure 5.23. The Early voltage versus $N_{\text{epi}}$ for the p-n-p.
5.9 Conclusions

The base width of the n-p-n transistor increases with decreasing the epitaxial layer doping concentration, this in turn lowers the current gain of the transistor, while for the lateral p-n-p, the base width decreases with decreasing the epilayer doping concentration.

For the lateral p-n-p, the common-emitter current gain decreases with increasing the epilayer for two reasons. Firstly, the base transport factor decreases due to the increase in the base with, and secondly, the emitter efficiency decreases due to the increase in the base-to-emitter doping concentration ratio, $N_B/N_E$.

The collector-base voltage, which causes full depletion of the lightly doped collector region, $V_{CBF}$, is an important parameter, since most of the transistor parameters suffer from a large collector-base voltage dependence beyond this voltage.

When an n-p-n transistor is fabricated in a thin epilayer, the resulting low doped collector region is thin, which results in a low breakdown voltage. A large epilayer thickness is required for an acceptable breakdown voltage of the transistor, especially for transistors made in low doped epilayers.

For the lateral p-n-p transistors fabricated in lightly doped epilayers, a large base width is required for an acceptable breakdown voltage, therefore, poor transistor parameters such as the current gain and the cut-off frequency result.

The maximum collector current is limited by the high-level effects at the collector-base junction for n-p-n transistors fabricated in epilayers with doping concentrations of less than about $9 \times 10^{15}$ atoms/cm$^3$, while the maximum collector current is limited by high-level injection effects at the emitter-base junction for transistors made in epitaxial layers doped with higher concentrations.

With the additional post-processing annealing step, at low epilayer doping concentrations, the base width of the n-p-n transistor tends to increase, and, therefore, the current gain decreases, while at higher concentrations the base width decreases and the current gain increases.

The Early voltage of the n-p-n transistor tends to decrease in general with increasing the temperature and/or the annealing time. This is mainly because of the reduction in the base doping concentration.

For the lateral p-n-p transistors the base width decreases with increasing time and/or the temperature of the post-processing annealing step. Therefore, the current gain increases and the Early voltage decreases.
Chapter 5. Compatibility Between ICs and Sensors
Chapter 6

Measurements

This chapter is divided into two main parts. In the first part, the measurement results of the DC parameters of the bipolar transistor in relation to process modifications are presented and are compared to the simulation results discussed in chapter 5. In the second part, the functionality of the several parts of the floating-point A/D converter is verified.

6.1 Measurement of the DC Transistor Parameters

As discussed in chapter 5, two processing parameters are of interest in micromechanical sensor design, they are the epitaxial layer doping concentrations and the post-processing annealing. The effect of these two parameters on the bipolar transistor characteristics is discussed below.

To be able to measure the transistor parameters as a function of process modification (epilayer doping concentration and the post-processing thermal cycles), several wafers were processed in a standard process (DIMES-01) and a non-standard processes. In the standard process a 4μm epilayer with a dopant (arsenic) concentration of $1 \times 10^{16} \text{ cm}^{-3}$ is used and a final annealing step at 1000°C for 35 minutes is used after the emitter implantation to activate the implanted ions. In the non-standard processes, a final annealing of 45 and 60 minutes was used to account for the post-processing annealing required by many micromechanical sensor designs [27, 28]. Further, to study the transistor parameters as a function of the epilayer doping concentration, three other dopant concentrations were chosen for the non-standard processes.

A batch of 11 wafers was successfully processed with different epilayer doping concentration and different final annealing times as shown in Table 6.1.
<table>
<thead>
<tr>
<th>Wafer group</th>
<th>Standard process with a final annealing</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
</tr>
<tr>
<td>$N_{epi}$</td>
<td></td>
</tr>
<tr>
<td>1.5$\times$10$^{15}$</td>
<td>wafer # 1</td>
</tr>
<tr>
<td>4.5$\times$10$^{15}$</td>
<td>wafer # 2</td>
</tr>
<tr>
<td>1$\times$10$^{16}$</td>
<td>wafer # 3</td>
</tr>
<tr>
<td>2$\times$10$^{16}$</td>
<td>wafer # 4</td>
</tr>
</tbody>
</table>

Table 6.1. Processing scheme for the wafers prepared for measurement.

6.1.1 Measurement set-up

The measurement on the transistor parameters was performed by a set-up consisting of an $hp$ work station, a DC parameter measurement unit ($hp4042B$ Modular DC Source/Monitor) and a probe station. IC-CAP$^1$ was used to extract the DC transistor parameters from the basic measurements such as the Gummel plot and $I_C$ versus $V_{CB}$ at constant $V_{EB}$.

6.1.2 The common-emitter current gain

The forward common-emitter current gain, $\beta_F$, is defined as $I_C/I_B$. The value of $\beta_F$ largely depends on the collector current level. Figure 6.1 shows a typical measurement result of $\beta_F$ versus $I_C$ for an n-p-n transistor.

The SPICE forward common emitter current gain is obtained from a mathematical formula [77] that includes many parameters in order to obtain the best fit to the measured characteristics. We will denote the SPICE forward common-emitter current gain by $\beta_{FS}$. The value of $\beta_{FS}$ is somewhat higher than the maximum value of $\beta_F$ that can be obtained from a measurement of $\beta_F$ versus $I_C$ such as the one shown in Figure 6.1. We will refer to the maximum value of $\beta_F$ as $\beta_{FM}$. When the maximum is not peaked, but rather flat and wide, the value of SPICE $\beta$ does not differ too much from $\beta_{FM}$. The difference is typically less than 20%. Table 6.2 shows some measured values of $\beta_{FS}$ and $\beta_{FM}$ for the n-p-n transistor.

When $\beta_F$ shows a sharp peak as in the case of the lateral p-n-p transistor shown in Figure 6.2, $\beta_{FS}$ can be more than three times $\beta_{FM}$. Table 6.3 shows some measured values of $\beta_{FS}$ and $\beta_{FM}$ for the lateral p-n-p transistor. In the

$^1$A software package for semiconductor characterization and modelling system.
Figure 6.1. A typical measurement result of $\beta_F$ versus $I_C$ for an n-p-n transistor.

<table>
<thead>
<tr>
<th>Wafer #</th>
<th>$\beta_{FS}$</th>
<th>$\beta_{FM}$</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>98</td>
<td>88</td>
</tr>
<tr>
<td>4</td>
<td>109</td>
<td>95</td>
</tr>
<tr>
<td>7</td>
<td>108</td>
<td>94</td>
</tr>
<tr>
<td>10</td>
<td>144</td>
<td>122</td>
</tr>
</tbody>
</table>

Table 6.2. $\beta_{FS}$ and $\beta_{FM}$ for an n-p-n transistor.
following sections, $\beta_{FM}$ is plotted for the lateral p-n-p transistor rather than $\beta_{FS}$, since $\beta_{FS}$ does not have a physical meaning.

<table>
<thead>
<tr>
<th>Wafer #</th>
<th>$\beta_{FS}$</th>
<th>$\beta_{FM}$</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>2152</td>
<td>1121</td>
</tr>
<tr>
<td>4</td>
<td>462</td>
<td>189</td>
</tr>
<tr>
<td>7</td>
<td>308</td>
<td>90</td>
</tr>
<tr>
<td>10</td>
<td>64</td>
<td>34</td>
</tr>
</tbody>
</table>

Table 6.3. $\beta_{FS}$ and $\beta_{FM}$ for lateral p-n-p with $W_M$ of 4$\mu$m.

![Graph](image)

**Figure 6.2. A typical measurement result of $\beta_F$ versus $I_C$ for the lateral p-n-p.**

Figure 6.3 shows the measurement result of $\beta_{FS}$ versus $N_{epi}$ for the n-p-n. Curve (1) is for the standard process (wafer group A), and curves (2) and (3) are for the standard process, with a final annealing step at 1000°C for 45 or 60 minutes (wafer B and C), respectively.

If the additional annealing step is relatively short, its effect on the lateral p-n-p is less significant than it is for the n-p-n. Figure 6.4 shows the measured (points) and simulated (curves) of the common-emitter current gain for the lateral p-n-p versus $N_{epi}$. The solid curve is for the standard process (wafer
Figure 6.3. Simulated and measured $\beta_F$ versus $N_{epi}$ for the n-p-n.

Figure 6.4. Simulated and measured $\beta_F$ versus $N_{epi}$ for the lateral p-n-p with a post-processing step.
group A) and the dashed curve is for the non-standard process (wafer group C).

Figure 6.5 shows the simulation and measurement results of $\beta_{FM}$ versus $N_{epi}$ for the p-n-p, with the emitter to collector mask separation, $W_M$, as a parameter. This result is for the standard process (wafer group A). $\beta_{FM}$ increases with decreasing the $N_{epi}$ and, of course, decreases with increasing the base width. Note that the base width is equal to $W_M$ minus the lateral diffusion at the two sides (refer to Figure 5.4).

![Graph showing $\beta_F$ versus $N_{epi}$ with $W_M$ as a parameter for the lateral p-n-p.]

Figure 6.5. Simulated and measured $\beta_F$ versus $N_{epi}$ with $W_M$ as a parameter for the lateral p-n-p.

### 6.1.3 The Early voltage

The Early voltage is extracted from the plot of the collector current versus the collector-base voltage at constant emitter-base voltage. Figure 6.6 shows the simulated (curves) and measured (points) Early voltage for the n-p-n versus $N_{epi}$ for the standard and the non-standard processes. Curve (1) is for the standard process (group A) and curves (2) and (3) are for wafer groups B
and C, respectively. There is a good agreement between the measured and the simulated results.

![Graph showing $V_A$ versus $N_{epi}$ for the n-p-n](image)

**Figure 6.6.** Simulated and measured $V_A$ versus $N_{epi}$ for the n-p-n.

In the case of the p-n-p, the base width is a parameter that can be modified by the layout designer. Figure 6.7 shows the simulated and measured Early voltage for the p-n-p versus $N_{epi}$ and the emitter-to-collector mask separation, $W_M$, as a parameter.

With decreasing the epilayer doping concentration, the common-emitter current gain of the lateral p-n-p transistor increases very rapidly and the Early voltage decreases. At low epilayer doping concentrations, the performance of the transistor with a base width of about 4μm is not satisfactory. In this region a transistor with a large base width ($\approx 10μm$) will give a better performance.

Figure 6.8 shows a measurement and a simulation result of the Early voltage for the p-n-p as a function of $N_{epi}$ with different annealing times. Curve (1) is for the standard process and curve (2) is for the non-standard process (wafer group C). As in the case of $\beta_F$, for such relatively short annealing time, the effect of the post-processing annealing step is insignificant, only with excessive annealing time and temperature will a significant change in the Early voltage result (refer to Figure 5.23).
Figure 6.7. Simulated and measured $V_A$ versus $N_{epi}$ for the lateral p-n-p.

Figure 6.8. Simulated and measured $V_A$ versus $N_{epi}$ for the lateral p-n-p.
6.1.4 Collector series resistance

The parasitic collector series resistance $R_C$ of the integrated n-p-n transistor is composed of three components: the resistance of the epitaxial collector under the intrinsic base, the resistance of the buried-n layer, and the resistance from the buried-n layer to the contact, including the collector contact resistor. The collector resistance strongly depends on the device-operating point. Therefore, an approximation value will be used in the measurement.

One method to measure the collector series resistor is from a plot of $I_C$ versus $V_{CE}$. Figure 6.9 shows a typical measurement result of $I_C$ versus $V_{CE}$ for the n-p-n transistor. The slope of the plot is equal to $1/R_C$.

![Graph of $I_C$ versus $V_{CE}$](image)

Figure 6.9. A typical measurement result of $I_C$ versus $V_{CE}$ for the n-p-n.

Figure 6.10 shows the measurement results of the collector series resistance versus $N_{epi}$, for the n-p-n. The solid curve is for the standard process, and the dashed curve is for the standard process with a final post-processing annealing at 1000°C for 60 minutes (wafer group C). The collector resistance decreases with increasing epilayer doping concentration, this is because the low doped collector region under the base is the unmodified epilayer. Further, the collector resistance tends to decrease with increasing the post-processing annealing time and/or temperature, this is due to the up-diffusion of the buried-n, as well as the down diffusion of the base and the deep-n regions.
Figure 6.10. Measured $R_C$ versus $N_{epi}$ for the n-p-n.

### 6.1.5 Emitter resistance

The parasitic emitter resistance $R_E$ is primarily determined by the emitter contact resistance. One method to measure $R_E$ is based on the measurement of the collector-emitter voltage given by [78]

$$V_{CE} = \frac{kT}{q} \ln \left[ \frac{I_B + I_C(1 - \alpha_R)}{\alpha_R[I_B - I_C(1 - \alpha_F)/\alpha_F]} \right] + R_E(I_B + I_C) + R_CI_C. \quad (6.1)$$

where $\alpha_F$ and $\alpha_R$ are the large-signal forward and reverse common base current gain, respectively. With $I_C = 0$, equation (6.1) reduces to:

$$V_{CE} = \frac{kT}{q} \ln \left[ \frac{1}{\alpha_R} \right] + R_EI_B. \quad (6.2)$$

A plot of $V_{CE}$ as a function of $I_B$ reveals a slope of $R_E$ and an intercept at $(kT/q)\ln(1/\alpha_R)$. Figure 6.11 shows a typical measurement result of $V_{CE}$ versus $I_B$ for an n-p-n transistor.

The value of the emitter resistor for the n-p-n transistor is found to be independent of the epilayer doping concentration and is about 15 ± 2 $\Omega$, for a transistor with an emitter area of $2\times4 \mu m^2$. 

6.2.1 Programable current source

In section 4.4, four non-linear D/A converters that can be implemented in the feedback loop to realize the Successive Approximation floating-point A/D converter are discussed. The first three realizations are based on two types (shown in Figures 4.7 and 4.8) of an n-bit programmable current source (n-bit D/A converters). Each floating-point D/A converter realization requires two 8-bit programmable current sources, one is used to determine the exponent, while the other is used to determine the fraction. In the following, the verification of the performance of these two programmable current sources, which are realized as 8-bit versions is presented.

Figure 6.12 shows the realized circuit of the programmable current source shown previously in Figure 4.7. Note that each current mirror branch is divided into two branches. Figure 6.13 shows the chip photograph, which has an active die area of 0.8×1.2 mm².

Equation (3.10) shows that, if the relative error in the fraction is assumed to be zero (i.e. \( \epsilon_f = 0 \)), the relative error in the exponent, \( \epsilon_e, k \), should not exceed \( \pm 1/2 \) LSB. Since an error in the exponent produces an offset error in the transfer function of the floating-point D/A converter. Therefore, the relative error is of more importance than the absolute error in the programmable current sources used to determine the exponent. Figure 6.14 shows the rela-
Figure 6.12. Circuit diagram of the 8 bits programmable current source.

Figure 6.13. Chip photograph of the 8 bits programmable current source shown in Figure 6.12 (0.8x1.2 mm²).

tive error in each bit in two programmable current sources on the same wafer, where the relative error is defined as:

$$\text{Relative Error} = \frac{I_{\text{measured}} - I_{\text{theoretical}}}{I_{\text{theoretical}}}.$$  \hspace{1cm} (6.3)

It is found that except for the two LSBs, the relative error is within the required specification, which is ±0.2% (±1/2 LSB), for an 8-bit resolution. This performance limits the dynamic range of the A/D converter to 13 bits rather than the intended 15 bits. From Figure 6.14 it can be seen that the error in the two LSBs is of a systematic type. This error can be reduced by further optimization of the circuit layout.

![Figure 6.14. Measured relative error in the 8-bit of the programmable current source shown in Figure 6.12.](image)

In the programmable current source used to determine the fraction, the relative error is allowed to increase towards the LSBs, i.e. the LSB can have a relative error higher than ±0.2% for an 8-bit resolution. Therefore, in the fraction the absolute error is of more importance than the relative error. The absolute error should not exceed ±1/2 LSB in the programmable current source used for the fraction.

Figure 6.15 shows the absolute error in each of the 8 bits for two circuits on the same wafer, for the programmable current source shown in Figure 6.12.
The maximum absolute error in each bit is found to be less than \( \pm 1/8 \) LSB. Figure 6.16 shows the Integral Non-linearity (INL) versus the input code. The integral non-linearity is found to be less than \( \pm 1/4 \) LSB, which means that a 9-bit resolution can easily be obtained by adding a current mirror branch with a value of 1/2 LSB. But this high degree of accuracy is required in the fraction, since the total error in the floating-point D/A converter is a combination of the errors in the fraction as well as in the exponent. Moreover, the two designs of the floating-point D/A converters discussed previously in section 4.4 make use of a PNP current mirror. In this case the error caused by the PNP current mirror should also be taken into account.

![Figure 6.15. Measured absolute error in the 8 bits of the programmable current source shown in Figure 6.12.](image)

Figure 6.17 shows the chip photograph of the programmable current source shown in Figure 4.8. The active die area is about 0.7\times1.4 \text{ mm}^2. The unity emitter area of the mirror transistors in this circuit is twice that used in the previous design, i.e. Figure 6.13. Figure 6.18 shows the measured relative error in each of the 8 bits for two circuits on the same wafer. The relative error is found to be less than \( \pm 0.2\% \) in the remaining 5 MSBs. Which means, only five segments for the exponent can be achieved when using this programmable current source for the exponent. Figure 6.19 shows the absolute error in the 8 bits. It is less than \( \pm 1/8 \) LSB in one chip and less than \( \pm 1/4 \) LSB in the other. Figure 6.20 shows the integral non-linearity in the first chip and is found to be less than \( \pm 1/4 \) LSB.
Figure 6.16. *Integral non-linearity in the programmable current source.*

Figure 6.17. *Chip photograph of the 8 bits of the programmable current source shown in Figure 4.8 (0.7x1.4 mm²).*
Figure 6.18. Measured relative error in the 8 bits of the programmable current source shown in Figure 6.17.

Figure 6.19. Measured absolute error in the 8 bits of the programmable current source shown in Figure 6.17.

Figure 6.20. Integral non-linearity in the programmable current source shown in Figure 6.17.

Figure 6.21 depicts the circuit diagram of the floating-point D/A converter shown previously in Figure 4.16, and Figure 6.22 shows the chip photograph. The required die area is 1.1×1.5 mm². The circuit was tested and its performance is similar to the two discussed above.

6.2.2 The Successive Approximation Logic

As discussed in section 4.6, the realization of the Successive Approximation logic is based on EFL with a non-linear load [17]. The basic element in the realization of the Exponent and the Fraction registers is a D-type flip-flop. The D-type flip-flop is realized in a standard bipolar process (DIMES-01), with conservative design rules and requires only 334×445μm². Figure 6.23 shows the chip photograph and Figure 6.24 shows the measurement results in a binary divider configuration for different bias currents. A bias current of 20μA is sufficient for proper operation at 1MHz. With a power supply of 5 V, the power consumption is about 0.2 mW per flip-flop, which allows the integration of 5000 flip-flops in a 1 W encapsulation.

Figures 6.25 and 6.26 show the die photograph of the Exponent and the Fraction registers which have an active die area of 0.7×3.1 mm² and 1.0×3.8 mm², respectively. Figure 6.27 shows the die photograph of the control logic
Figure 6.21. Circuit diagram of the 8 bits D/A converter.

Figure 6.22. Chip photograph of the 8 bits D/A converter shown in Figure 6.21 (1.1x1.5 mm²).

Figure 6.23. Chip photograph of the D-type flip-flop (334×445μm²).

Figure 6.24. Measurement result of the D-type flip-flop.
and which has a die area of 0.5×2.6 mm². The power consumption of the Successive approximation is about 120 mW.

Figure 6.25. *Chip photograph of the Exponent register (0.7×3.1 mm²).*

Figure 6.26. *Chip photograph of the Fraction register (1.0×3.8 mm²).*

Figure 6.27. *Chip photograph of the control logic (0.5×2.6 mm²).*
6.2.3 PNP current mirror

The accuracy problem in current mirrors is not only due to the static error, which causes a shift of the relative error. More important is that the error value must be constant with the current level. In many applications the first type of error can be trimmed out. Figure 6.28 shows a typical measurement results of the relative error versus the input current. It can be seen that the error increases at high current levels, which is mainly due to the drop in the current gain.

![Graph showing relative error vs. input current](image)

Figure 6.28. The relative error in a current mirror.

To achieve good accuracy, an improved current mirror circuit was used [63]. Figure 6.29 shows the circuit diagram and Figure 6.30 shows the chip photograph. Relatively large transistors were used for the mirror transistors, $Q_1$ and $Q_2$, to reduce the mismatch error and to obtain a higher knee current value. Figure 6.31 shows the measured relative error versus the input current for three current mirror circuits. From the figure, it can be seen that there is a similarity in the three plots, which indicates that the measurement system contributes to most of the noise in the measurement. A relative error of less than ±0.1% was obtained in the dynamic range required by the floating-point A/D converter which is 0.1 – 200µA.
Figure 6.29. The circuit diagram of the PNP current mirror.

Figure 6.30. Die photograph of the PNP current mirror.

Figure 6.31. Measured relative error in the PNP current mirror.

6.2.4 Comparator

The chip photograph of the realized current comparator is shown in Figure 6.32. The comparator has an active die area of 210×540 µm² and a power consumption of 60 mW, and it requires a single supply of 5 V. The measured transit time is shown in Figure 6.33 and it is about 1.3µs.
Figure 6.32. *Die photograph of the current comparator (210×540 μm²).*

Figure 6.33. *Measured transit time in the current comparator.*
6.3 Floating-Point A/D Converter

Figure 6.34 shows the chip photograph of the complete A/D converter. The die area is $4.2 \times 4.8$ mm$^2$ and consumes a power of 205 mW.

Figure 6.34. The chip photograph of the floating-point A/D converter ($3.4 \times 4.8$ mm$^2$).

6.4 Conclusions

The common-emitter current gain of the lateral p-n-p transistor increases very rapidly and the Early voltage decreases, with reducing the epitaxial layer doping concentration. The performance of the lateral p-n-p transistor with a base width of about 4μm in low doped epilayer is not satisfactory. To obtain a satisfactory performance of the lateral p-n-p a large base width ($\approx 10\mu$m) should be used.
The error in the two LSBs of the realized programmable current source of Figure 6.12 is of a systematic type. This error can be reduced by further optimization of the circuit layout.
Chapter 7

Conclusions

In smart sensor design, it is essential to know about the influence of processing parameters on the performance of the sensor as well as on the circuit components. By knowing of the bipolar transistor characteristics on a non-standard process, the sensor and the on-chip read-out electronics can be simulated and the smart sensor performance can be optimized.

The effect of the epilayer doping concentration and post-processing annealing on the n-p-n and the lateral p-n-p bipolar transistors characteristics have been studied theoretically and experimentally.

In sensors with a wide dynamic range and limited accuracy, floating-point A/D conversion is more suitable than linear A/D conversion.

A floating-point A/D converter is fabricated in a standard bipolar process. No special additional processing sequences are required, which makes the converter attractive in terms of simplicity, cost and integrability with many sensors.

Although BiCMOS might seem to be more suitable for such a realization, the complexity of the process adds to the system's cost, specially bearing in mind that the fabrication of the sensor might also require some additional fabrication sequences. This makes the process more complex, and, therefore, decreases the yield and increases the system's cost.

An 8-bit resolution and 13-bit dynamic range is obtained using a standard bipolar process. By further optimization of the layout, the dynamic range can be increased to 15 bits.

The converter has an operating frequency of 20KHz which is equivalent to a conversion time of 50μs. The converter requires a single supply of 5 V and consumes a power of 205 mW. Table 7.1 lists the power consumption of the different parts of the converter.
<table>
<thead>
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<th>Part</th>
<th>Power consumption in mW</th>
</tr>
</thead>
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<tr>
<td>D/A converter</td>
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</tr>
<tr>
<td>SAL</td>
<td>120</td>
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<tr>
<td>Comparator</td>
<td>60</td>
</tr>
<tr>
<td>Total</td>
<td>205</td>
</tr>
</tbody>
</table>

Table 7.1. Power consumption of the FPADC.
Bibliography


List of Publications and Presentations

Publications


Presentations


Summary

Many sensors have a wide dynamic range and a limited accuracy. The use of a high-resolution A/D converter to cover the sensor dynamic range adds to the cost of the system without any benefit being derived from the high resolution in respect to the system overall accuracy. A non-linear A/D converter offers an optimal solution for digitizing the output of these sensors. The aim of this research was to develop a non-linear A/D converter that features a wide dynamic range ($\approx10^{15}$) and a resolution of about 8 bits. Further, in this research, the effect of the post-processing annealing and the epilayer thickness and doping concentrations on the DC bipolar characteristics were investigated.

Chapter 1

This chapter highlights the importance of sensors in our life and the advantages derived from integrated smart sensors. The benefits from using silicon as a sensor material are mentioned. The most important characteristics of the floating-point A/D converters, their dynamic range and resolution are formulated. A brief introduction to the problem of compatibility between sensors and standard bipolar IC technologies is given.

Chapter 2

An overview of existing techniques used in non-linear A/D converters is given. The existing techniques are grouped into four categories. The first group makes use of the exponential relation between the collector current and the emitter-base voltage drop. The second group uses the voltage-time relation when charging or discharging a capacitor. The third group utilizes the geometrical area of components. The final group implements ROMs for the storage of the pre-digitized non-linear characteristics. The basic theory and limitations of each group are briefly discussed.
Chapter 3

This chapter discusses the specifications and errors in the floating-point D/A and A/D converters. Most of the specifications have a similarity to those of linear converters.

Chapter 4

In this chapter, the realization of the several parts of the non-linear converter are discussed. The Successive Approximation technique was chosen for the realization of the floating-point A/D converter. Several methods for realizing the floating-point D/A converter that are based on current mirrors using emitter area scaling of a bipolar transistor are presented. The realized Successive Approximation logic is based on the EFL with a non-linear load.

Chapter 5

Many sensors require a slightly modified version of the standard process. Three of the most important processing parameters that need to be modified are the post-processing annealing and the epilayer doping concentration and thickness. The DC parameters of the n-p-n and the lateral p-n-p bipolar transistor are presented as a function of the epilayer doping concentrations, thickness and the post-processing annealing time and temperature.

Chapter 6

The measurement of the DC transistor characteristics as a function of the epilayer doping concentration and thickness, as well as the post-processing annealing time and temperature, are presented and compared to simulation results. The functionality of the several parts of the floating-point A/D converters is verified. An 8-bit resolution with a 13-bit dynamic range is verified to be possible using standard bipolar process. The chip area (3.4×4.8 mm²) is comparable to commercial products.

Chapter 7

Some conclusions and suggestions for future research are given in this chapter.
Samenvatting

Veel sensoren hebben een groot dynamisch bereik gecombineerd met een beperkte nauwkeurigheid. Een analoog naar digitaal omzetter (ADC) met een hoog oplossend vermogen is voor deze sensoren niet effectief. Ze verhogen de kosten van het sensor systeem zonder dat wordt geprofiteerd van het hoge oplossende vermogen, de nauwkeurigheid van de sensor zelf is immers de beperkende factor. Niet-lineaire ADC’s, voor het omzetten van het sensor signaal naar een digitaal signaal, zijn voor deze sensoren veel beter geschikt. Het doel van dit onderzoek is het ontwikkelen van een niet-lineaire ADC met een groot dynamisch bereik (ongeveer 10^15) en een oplossend vermogen van 8 bits. Verder worden verschillende proces-invloeden op de DC karakteristieken van bipolaire transitors onderzocht. Er is gekeken naar invloed van "post-processing annealing", de dikte van de epi-laag en de doterings concentraties.

Hoofdstuk 1

In dit hoofdstuk wordt aangegeven hoe belangrijk sensoren zijn in ons leven en de voordelen van geïntegreerde "smart" sensors worden besproken. De voordelen van silicium als sensor materiaal worden besproken. Het dynamisch bereik en het oplossend vermogen van "floating-point" ADCs, een speciaal soort niet-lineaire ADCs, wordt geformuleerd. Het hoofdstuk eindigt met een korte inleiding over het compatibiliteitsprobleem tussen sensoren en standaard bipolaire technologie.

Hoofdstuk 2

Er wordt een overzicht gegeven van bekende technieken die in niet-lineaire ADC’s worden gebruikt. Deze technieken worden gegroepeerd in vier categorieen. De eerste groep maakt gebruik van de exponentiële relatie tussen de collectorstroom en de basis-emittor spanning in een bipolaire transistor. De tweede groep gebruikt de spanning-tijd relatie van het op- of ontladen van een capaciteit. De derde groep maakt gebruik van componenten met verschillende
afmetingen. De vierde groep tenslotte bevat ROM's waarin de niet-lineaire overdracht van de ADC is opgeslagen. De basisstheorie en de beperkingen van ieder van deze groepen wordt kort besproken.

Hoofdstuk 3

In dit hoofdstuk worden de specificaties en fouten van de "floating-point" ADC's en DAC's (Digitaal naar Analoog omzetters) op een rijtje gezet. De meeste eigenschappen blijken hetzelfde als de eigenschappen van lineaire omzetters.

Hoofdstuk 4

De realisatie van de verschillende onderdelen van niet-lineaire omzetters wordt beschreven. De "Successive Approximation" techniek is gekozen om de "floating-point" ADC in te realiseren. DAC's vormen de bouwstenen van een ADC in deze techniek. Verschillende methoden om "floating point" ADC's te realiseren worden gepresenteerd. Deze ADCs zijn gebaseerd op stroomspiegels die gerealiseerd worden m.b.v. geschaalde emitters van bipolaire transistoren. Om de "successive approximation" functie te realiseren wordt gebruik gemaakt van EFL technieken met een niet-lineaire belasting.

Hoofdstuk 5

Voor veel sensoren is het noodzakelijk het standaard IC proces iets te veranderen. De drie belangrijkste proces parameters die aangepast moeten worden zijn: "post-processing annealing", epi-laag doping concentratie en epi-laag dikte. De DC eigenschappen van de npn en laterale pnp transistors worden gegeven als functie van deze drie parameters.

Hoofdstuk 6

De gemeten DC transistor karakteristieken worden voor diverse waarden van de technologieparameters vergeleken met de simulatie resultaten. De functionaliteit van de verschillende onderdelen van de "floating-point" ADC's wordt gecontroleerd. Een oplossend vermogen van 8 bit en een dynamische bereik van 13 bit blijkt mogelijk bij gebruik van een standaard bipolair proces. De oppervlakte van de ADC (3.4x4.8 mm²) is vergelijkbaar met die van commercieel verkrijgbare produkten.
Hoofdstuk 7

Dit laatste hoofdstuk geeft de conclusies van het becreven onderzoek en tevens worden suggesties aangedragen voor verder onderzoek.
## List of Abbreviations

<table>
<thead>
<tr>
<th>Abbreviation</th>
<th>Description</th>
</tr>
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<tbody>
<tr>
<td>BFPR</td>
<td>Binary Floating-Point Resistor</td>
</tr>
<tr>
<td>DNL</td>
<td>Differential Non-linearity</td>
</tr>
<tr>
<td>INL</td>
<td>Integral Non-linearity</td>
</tr>
<tr>
<td>EFL</td>
<td>Emitter Function Logic</td>
</tr>
<tr>
<td>FPADC</td>
<td>Floating-Point A/D Converter</td>
</tr>
<tr>
<td>FPDAC</td>
<td>Floating-Point D/A Converter</td>
</tr>
<tr>
<td>LSB</td>
<td>Least Significant Bit</td>
</tr>
<tr>
<td>MSB</td>
<td>Most Significant Bit</td>
</tr>
<tr>
<td>NLADC</td>
<td>Non-Linear A/D Converter</td>
</tr>
<tr>
<td>PGA</td>
<td>Programmable Gain Amplifier</td>
</tr>
<tr>
<td>SAL</td>
<td>Successive Approximation Logic</td>
</tr>
<tr>
<td>S/N</td>
<td>Signal-to-noise ratio</td>
</tr>
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</table>
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Biography

Kamal-Eldin Mohamed Mahmoud was born in Atbara, Sudan in 1958. He received his B.Sc. (honours) from the University of Gezira, Wad Medani, Sudan in 1984. After graduation he worked for two years in the Applied Physics, Electronics and Instrumentation Department of the same university. In the period from March to August 1986 he was with the Signals and Systems Laboratory, the Applied Physics Department, Delft University of Technology, the Netherlands. In September 1986 he joined the Laboratory for Electronic Instrumentation, Electrical Engineering Department, of the same university, where he received his M.Sc. in electrical engineering in 1988. Subsequently he joined the Electronic Instrumentation Laboratory, where he worked on nonlinear Analogue to Digital converters as described in this thesis. Most of his work has been published in several technical papers and presented at many international conferences.