Power Balance Control of DC Microgrids

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Power Balance Control of DC Microgrids

MASTER OF SCIENCE THESIS

For the degree of Master of Science in Electrical Power Engineering at Delft University of Technology

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Faculty of Electrical Engineering, Mathematics and Computer Science (EEMCS)
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Abstract

DC systems, Energy conversion, and Storage (DCE&S) is a new emerging ambitious group. For decades power system and power electronics have been sailing in separate boats. DCE&S group tries to bridge the two. With introduction of concept of smartgrids, many techniques and systems have been developed for their integration. Further research into these techniques, and development of novel systems are also progressing at a quick pace worldwide.

With increasing adaptation of distributed generation in everyday energy landscape, it becomes essential to have a control that compliments the distributed nature of generation. Intelligent DC microgrids have the capability to house the locally-generated energy, its end-utilizers, and the mechanism to cope with the issues of having smaller systems.

Distributed generation suffer from great invariance, thus a strong control system is required. The development of Power balance control with relevant hardware tested under rigorous testing could alleviate the problem and provide a new dimension to grid contributors.

The aim of this MSc Thesis was to achieve power balance control in decentralised way. First, a control algorithm was developed to provide stable robust operation for the grid incorporating features from different control techniques; second, was implementing this algorithm to already present technology and perform real life analysis; third, was to develop a hardware specifically for the ease of using this and many other techniques. In the end the algorithm was tested under multiple scenario and experiments were carried out to asses the viability.
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'May all our relationship age like fine wine'

Delft, University of Technology

September 25, 2015

Subhronil Chaudhuri
"The embodied soul is eternal in existence, indestructible, and infinite, only the material body is factually perishable – therefore fight, o Arjuna!"

———The Bhagavad Gita (Chapter 2, Verse 3)
Chapter 1

Introduction

Electricity is the set of physical phenomena associated with the presence and flow of electric charge (electrons). Movement of electric charge is known as electric current. The rate at which electric energy is transferred by an electric circuit is Electric power. The SI unit of electric power is Watt or one Joule per second. Electric power (International System for Units (SI) unit: Watt, W) is produced by an electric current I consisting of a charge of Q (SI unit: Coulombs, C) every t seconds passing through an electric potential difference of V is:

\[ P = \frac{VQ}{t} = VI \]  

(1-1)

Where,
- Q is electric charge in coulombs.
- t is time in seconds.
- I is electric current in amperes.
- V is electric potential or voltage in volts.

From the standpoint of electric power, components in an electric circuit can be divided into two categories [7]:

- **Passive devices** or **loads**: They consume electric power from the circuit converting it to other forms of energy such as mechanical energy, chemical energy, heat, light, etc. Examples are electrical appliances, bulbs, motors, heaters, etc.

- **Active devices** or **sources**: Any type of circuit component with the ability to electrically control electron flow. They generate electric power from converting other forms of energy such as mechanical energy, chemical energy, heat, light, etc. into electric power. Examples are generators, batteries, fuel cells, etc.

Some devices can be either source or load, depending on the voltage and the current through them. For example, a rechargeable battery acts as a source when it provides power to a circuit, but as a load when it is connected to a charger and is being recharged.
The basic relation between voltage (V) and current (I) is given by Ohm’s law \[ V = I \times R \] which states that: "The potential difference (voltage) across an ideal conductor is proportional to the current through it." The constant of proportionality is called the resistance, 'R', which has the unit of Ohm (\(\Omega\)), named after German physicist Georg Ohm.

1-1 AC vs DC

The operation of electrical systems can be based on two different kinds of currents, namely alternating current (Alternate Current (AC)) and direct current (Direct Current (DC)).

- **Alternating current (AC):** Flow of electric charge that periodically reverses direction; the usual waveform is a sine wave. Alternate current is produced by generators (AC ones), windmills, etc. [9]. Cables ratings are based upon the peak voltages of the system, and the power delivered is based on RMS value, i.e. RMS value = (Peak voltage/\(\sqrt{2}\)) [10].

AC systems have plenty of standards regarding fault elimination and protection.

- **Direct current (DC):** Flow of electric charge is unidirectional, usual waveform is a straight line (ideally). Direct current is produced by batteries, solar-cell, etc. [11]

Cables rating are based upon constant peak voltage of the system same for the power delivered, thus DC system can deliver peak voltage [10], which is \(\sqrt{2}\) times that of AC RMS voltage for a similar cable.

DC systems do not experience the same luxury as AC systems in the protection department.

1-1-1 War of Currents

"Where did the Australian rock band AC/DC get their name from? Why, Alternating Current and Direct Current, of course!" [12] With respect to the operational difference between AC and DC, a commercial war broke out between the American born Thomas A. Edison and George Westinghouse backed Croatian born Nikola Tesla in the late 1800s. While Edison was an inventor and entrepreneur (founded the General Electric), Tesla teamed up with Westinghouse, an industrialist and founder of Westinghouse Electric based in Pittsburgh, Pennsylvania, which acquired many of Tesla’s patents Edison was a developer and supporter of a DC distribution network, but DC system generated and distributed at the same voltage as used by customer’s lamps and motors. This resulted in large, costly distribution wires and thus generation plants near the loads. Nikola Tesla immigrated to the United States in 1884 to work for Thomas Edison at Edison Machine Works in New York City. Tesla was offered the task of redesigning the Edison’s inefficient dc motor and generator. Edison remarked, ‘There’s fifty thousand dollars in it for you—if you can do it’. After accomplishing the feat, Edison remarked 'Tesla, you don’t understand our American humour', Tesla immediately resigned [13].
For feasible long distance, cost efficient transmission, the voltage levels had to be stepped up, creating the high voltage transmission. The lack of technology at that time, limited the AC voltage to be stepped up, transmitted over long distance and stepped-down for customer use, by means of a newly developed Z.B.D. transformer by the Hungarians, in 1884. In the North America, Westinghouse was one of the strong believers in the new technology. In 1888, he licensed Nikola Tesla’s US patents for poly phase AC induction motor and transformer design and in turn hired him at his Westinghouse Electric and Manufacturing Company’s Pittsburgh lab [14]. This contention came to an end on November 20th, 1928. Since around 1920, most companies on both sides of the Atlantic ocean had abandoned the DC system for AC system. Edison kept pushing for DC system, but then GE President Coffin with the GE board of director had muted Edison. It only took couple of years for GE to catch up with AC, mainly due to Charles Proteus Steinmetz, a Prussian mathematician who was first to understand AC power from a solid mathematical standpoint [15]. The history and technology have conferred the victory of this war to AC distribution.

1-2 Electric Power Distribution

The electrical power distribution system is the final stage delivery of the electric power to the consumer. Transmission system is split into distribution system through an electric substation, which brings the voltage level down to low-voltage level (50V-1.5kV) with the use of transformers or power electronic converters.

1-3 DC Distribution

Due to the lack of technology to step-up/step-down (DC-DC conversion) the voltage value, AC beat DC in the war of currents as stated in previous century 1-1-1. With increasing efficiency, reduction in price and increasing compactness of the power electronics, currently DC solution has started to become viable. DC system can be classified into two categories based on the voltage level:

- **High Voltage Direct Current (HVDC)**
- **Low Voltage Direct Current (LVDC)**
1-3-1 HVDC

In the initial part of last century, DC transmission was a part of science fiction in itself. But with the development of the mercury-arc valve, power transmission became available during the period 1920-1940. The first complete system was put into service by the Soviet Union between Moscow-Kashira HVDC system was implemented in 1954. It was rated at ±200kv, 60MW. Today over 100 HVDC links are active all around the world. Further developments in the power electronic switches such as, thyristors, integrated gate-commuted thyristors (IGCTs), MOSFETs, insulated-gate bipolar transistors (IGBT), etc. made DC transmission much more promising in the late 1990s. One of the motivations to go HVDC is monetary. With the increase in transmission distance, the expenses for HVAC exceed that of HVDC. But in HVDC power has to be converted from AC to DC and vice versa at the other end. Power electronics interfaces are comparatively expensive. Thus, there is a minimum transmission distance for the HVDC lines, for it to be more feasible than HVAC. This minimum distance keeps reducing with the advancements in power electronics. Other considerations for DC, are due to the skin effect losses in AC, which in turn leads to the transmission of the same amount of DC power with much thinner wire [16]. the voltage level is defined with respect to a common line. In the [17] the author explains in detail about HVDC over HVAC, challenges, and the demands.

The voltage level is defined with respect to the common line. And there are several configuration[18]:

- **Monopole**: One of the terminals of the rectifier is connected to Earth ground while the other at a potential above/below ground.

- **Monopole and Earth return**: If no metallic conductor is installed, current flows in the Earth and/or sea between two specially designed earth electrodes.
• **Monopole and metallic return**: Metallic conductor is installed, return current flows through this conductor.

• **Symmetrical monopole**: Two high-voltage conductors, operating at ±half of the DC voltage, with only a single converter at each end.

• **Bipolar**: In bipolar transmission a pair of conductors is used, each at a high potential with respect to ground, in opposite polarity.

• **Back to back**: A plant in which both the converters are in the same area. The length of the DC line is kept as short as possible.

• **Multi-terminal systems**: Most common configuration of an HVDC link, consists of two converter stations connected by an overhead power line or underwater cable.

• **Tripole**: Intended for conversion of existing AC transmission lines to HVDC. Two of the three circuit conductors are operated as a bipole, the third conductor is used as a parallel monopole.

### 1-3-2 LVDC

Low voltage is a relative term, in electrical power systems low voltage mostly refers to the customer/consumer level voltage as used by lighting. The International Electrotechnical Commission (IEC) defines supply system low voltage in the range 120-1500V DC. The local grid has come a long way since the war of currents. Elision’s light bulb has been substituted by Light Emitting Diodes (LED), cause of being monochromatic, efficient and effective. Solar panels have been gaining a lot popularity, ever since Fukoshimo incident in Japan, PV panel market in Europe has exploded, thus increasing the presence of DC in the distribution level (Low/Medium Voltage) [20, 21].

LVDC can be implemented at the distribution level, substituting the medium voltage AC (MVAC) lines. The demand for undistributed power supply is growing when society depends more and more on electricity. This increases the chances of outages, which affects the customers in a negative way and produces increase in the outage cost. Thus upgrade to a more reliable network compared to traditional 3-phase MVAC becomes a necessity. Studies have shown that a LVAC system (office building, apartments, etc.) lose about 13% of their...
Introduction

(a) Monopolar HVDC link with ground return path.  

(b) Monopolar HVDC link with metallic return path.

(c) Bipolar HVDC link with ground return optional path.  

(d) Bipolar HVDC link with the options of ground return and metallic return with converter outage.

(e) Bipolar HVDC link with metallic return path.  

(f) Bipolar HVDC link without return path.

Figure 1-3: Topologies of HVDC link, from [19].
electrical power every year simply by distributing and converting power from utility meter
down to the point where it can power the equipment. The percentage of loss is even higher
for automated and optimised system (compared to similar DC based system) [21]. The LVDC
system concept responds to this challenge in the field of distribution of electricity.

It has been well established that HVDC is more efficient and cost effective (after the point)
compared to HVAC. Most of today’s utilization of DC technology concentrates mainly on
HVDC transmission system, industrial distribution, and electric drives. From a technological
point of view the DC distribution system is a new concept in electrical distribution [19].

The LVDC transmission system has higher transmission capacity than a traditional 400V AC
system resulting from the voltage difference between the systems. The transmission capacity
can be over 16 times at the voltage drop limit and over 4 times at thermal limit compared to
tradition 400V AC system. The transmission capacity on the used DC voltage level is much
higher than that of its AC counterpart, thus leading to either smaller cross-section of cables
or higher power delivery capacity.

The number of different kind of variations can present in LVDC topologies, which are as
follows [20]:

- **Monopole:** AC/DC conversion is always located near medium voltage (MV) or high
  voltage (HV) line. The DC/AC and/or DC/DC conversion can instead be located at
different location
  - a: HVDC link type solution, where the link between AC/DC and DC/AC or
    DC/DC is high voltage link (HV) which is then stepped down and distributed
    among various costumer. It constructs of one DC link between two separate AC
    network or AC-DC network. Customers are connected to a common 3-phase AC
    or common DC link.
  - b: Wide LVDC distribution district, where DC/AC or DC/DC conversion is made
    at every individual customer end. The network consists of a number of branches
equal to the number of customers.

- **Bipolar:** In bipolar system two unipolar systems are connected in series. Multiple ways
can be achieved using bipolar system.
  - 1: Between a positive pole and common.
  - 2: Between a negative pole and common.
  - 3: Between a positive and a negative pole.
  - 4: Between a positive and a negative pole with common connection.

### 1-4 Electric Grid

The term *Grid* usually refers to a network

An **electric grid** is an interconnected network for delivering electricity from producers/-
suppliers to consumers, consists of generating station, high voltage (HV) transmission lines
<table>
<thead>
<tr>
<th></th>
<th>Advantages</th>
<th>Disadvantages</th>
</tr>
</thead>
<tbody>
<tr>
<td>Monopolar link</td>
<td>Less cable material</td>
<td>Limited use of midpoint grounding</td>
</tr>
<tr>
<td></td>
<td>Faults more easily detected</td>
<td>Adequate protection requested</td>
</tr>
<tr>
<td>Bipolar link</td>
<td>Midpoint high resistance allowed</td>
<td>Higher costs and material used</td>
</tr>
<tr>
<td></td>
<td>Higher flexibility</td>
<td>Fault detection more complicated</td>
</tr>
</tbody>
</table>

Table 1-1: Advantages and disadvantages of the two topologies of LVDC, adapted from [11].

that carry power from distant sources to demand centres, and distribution lines that connect
dividual customers [22].

Generating/power stations, that produce electrical power are generally coal/gas stations, hydro
stations, wind farms, solar farms, and various other conventional & unconventional energy
sources. The generated electric power is then stepped up to a higher voltage at which it
connects to the bulk power transmission network. Transmission networks will move power to long
distances, sometimes across international boundaries, until it reaches its wholesale customer.
On arrival at a substation, the power will be stepped down from the transmission level voltage
to distribution level voltage, after which it enters the distribution ring, finally the power is
stepped down again to the required service voltage (customer/consumer end).

The traditional grid is generally unidirectional, that is the power flows only from the producer
to consumer, which inherently means fewer degree of control, fewer degree of adaptability
(to sudden changes), and thus fewer redundancy measures. the electric grid has existed
since the inception of the industrial age in the 19th century, battling against gas, steam,
hydraulics, etc. . The electric grid is expected to evolve to a new grid paradigm in the 21st
century [21]. The new grid needs to have greater degree of adaptability, controllability, needs
to be bidirectional; so that the consumer has a greater influence, not just as a consumer but
as a producer (distributed generation) too [24]. Thus the following different concept came into
existence:

- Super Grid
- Smart Grid
- Micro Grid

1-4-1 Super Grid

Also referred to as "Mega Grid".

A super grid is a wide area transmission network that makes it possible to trade high volumes
of electricity across great distances. In current usage, super grid has two senses - one of being
a superstructure layer overlaid or super-imposed upon existing regional transmission grid or
grids, and the second of having some set of superior abilities exceeding those of even the most
advanced grids.

In the overlay or superstructure meaning, a super grid is a very long distance equivalent of
a wide area synchronous network capable of large-scale transmission of renewable electricity.
Figure 1-5: General layout of electric grid, with hierarchical separation from Extra high generation to consumers, from [23].
(a) Present unidirectional power distribution system.

(b) Near future bidirectional power distribution system.

**Figure 1-6:** Present and future of the power distribution systems, from [25].
In some conceptions, a transmission grid of HVDC transmission lines forms a layer that is distinctly separate in the way that a superhighway system is separate from the system of city streets and regional highways. In the second sense of an advanced grid, the super grid is superior not only because it is wide area mega grid, but also because it is highly coordinated from a macro level spanning nations and continents, all the way down to the micro level scheduling low priority loads like water heaters and refrigeration.

"This is similar to how the internet bound together small network into single ubiquitous network." [27]

One advantage of such a geographically dispersed and dynamically balanced system is that the need for baseload generation is significantly reduced since intermittency of some sources such as ocean, solar, and wind can be smoothed. [28]

Example; The synchronous grid of continent Europe with an installed generation capacity of 667 GW, IPS/UPS with an installed generation capacity of 300 GW, etc.

Studies for such continental sized systems report there are scaling problems as a result of network complexity, transmission congestion, and the need for rapid diagnostic, coordination and control systems. Such studies observe that transmission capacity would need to be significantly higher than current transmission systems in order to promote unimpeded energy trading across distances unbounded by state, regional or national, or even continental borders.
1-4-2 Smart Grid

A smart grid is a modernized electric grid that uses analog or digital information and communication technology to gather and act on information - such as information about the behaviours of suppliers and consumers - in an automated fashion to improve the efficiency, reliability, economics, and sustainability of the production and distribution of electricity [29]. A common element to most definitions is the application of digital processing and communication to power grid, making data flow and information management central to smart grid [30].

The story goes like this: If Dr. Who were to somehow transport Alexander Graham Bell to the 21st century, he would not begin to recognise the components of modern telephony - cellphones, texting, mms, smartphones, etc. while Thomas Edison, one of the grid’s key early architects, would be totally familiar with the grid. While this is far from the whole story, Edison would be quite familiar with the present grids basic infrastructure. After the first grid establishment in 1886, there hasn’t been much change; most of the existing grids are over 5 to 6 decades old.

Since the early 21st century, opportunities to take advantage of the improvements in electronic communication technology to resolve the limitations and costs of the electrical grid have become apparent. Technological limitations on metering no longer force peak power prices to be averaged out and passed on to all consumer equally. Renewable energy such as Wind power and solar power are highly erratic and need more sophisticated control system to facilitate the connection of sources to the otherwise highly controllable equally. The rapidly falling costs point to change from centralized grid topology to one that is highly distributed, with power being both generated and consumed right at the limits of the grid. The move to a smarter grid promises to change the industry’s entire business model and its relationship with all stakeholders, involving and affecting utilities, regulator, energy service providers, technology and automation vendors and all consumer of electric power [31].

some of the features of the smart grid are:

- **Intelligent:** Capable of sensing system malfunction/faults and re-routing power to prevent or minimize blackout; working autonomously under dire situation, when response faster than human is required, and cooperatively in aligning the goals of utilities, consumer and regulator [31].

- **Reliability:** the smart grid will make use of technologies, such as state estimation [32], that improve fault detection and allow self-healing of the network without the intervention of technicians, reducing vulnerability to natural disasters or attack [33].

- **Accommodating:** Accepting energy from virtually any fuel source including conventional and un-conventional; capable of integrating any or all better ideas and technologies [31].

- **Motivating:** Enabling real-time communication between the consumer and utility so consumers can tailor their energy consumption based on individual preferences, like price and/or environmental concerns [31].

- **Opportunistic:** Creating new opportunities and markets by means of its ability to capitalize on plug-and-play innovation wherever and whenever appropriate [31].
• **Flexibility:** Next generation transmission and distribution infrastructure will be better able to handle possible bidirectional energy flows, allowing for distributed generation [34].

• **Efficiency:** Overall improvement of efficiency of energy infrastructure are anticipated from the deployment of smart grid technology. In particular including demand-side management, for example turning of an appliance during short time spikes in electricity price through optimization, eliminating truck-rolls for meter reading [35, 31].

• **Sustainability:** The improved flexibility of the smart grid permits greater penetration of highly variable renewable energy sources such as Solar and Wind power, even without addition of energy storage. Smart grid is a necessity for very large amount of renewable electricity on the grid for this reason [30].

All of the advancement in the smart grid is a result of technological advancements, and some of the technologies are noted below:

• **Integrated Communication:** Most communication are non uniform because they have been developed in an incremental fashion and not fully integrated. In integrated communication, a standard protocol is built into the the converter; allows for real time control, information and data exchange to optimize system reliability, asset utilization, and security [36, 37].

• **Sensing and Measurement:** Core duties are evaluating congestion and grid stability, monitoring equipment health, energy theft prevention, and control strategies support. Includes advanced microprocessor based meter (smart meter)and meter reading equipment, microprocessor based measuring circuit, wide-area monitoring system, dynamic line rating, digital protective circuits, etc. [38].

• **Advanced Control:** Power System Automation enables rapid diagnosis of and precise solutions to specific grid disruptions or outages [39]. Technology categories for advanced control methods are:
  
  – Distributed intelligent agents (Control System)
  
  – Analytical tools (software algorithms and high-speed computers)

  – Operational Application (SCADA, substation automation, demand response, etc.)

### 1-4-3 MicroGrid

Centralised generating facilities are giving way to smaller, more distributed generation partially due to loss of traditional economies of scale.

A microgrid is an integrated local energy grid consisting of distributed energy resources such as fuel cells, solar cells, wind turbine, micro-turbine, etc. with power electronic converters, energy storage devices (i.e. batteries, super-capacitor and flywheels), customer load, and possibility of control, which can be disconnected from a traditional grid and operate autonomously: island mode of operation[10, 40]. A microgrid can be based on either DC or AC system. The DC-Microgrid has the potential to overcome AC microgrid’s popularity, due to
fewer control parameters (DC: Voltage and Current, AC: voltage, current, frequency, phase, and reactive power), and DC being more efficient by elimination of last rectification stage (AC/DC) as majority of the device’s end utilization is DC power [41]. Further advantages of DC over AC has been discussed extensively in the previous section 1-1.

According to [42], due to distributed nature of the microgrid approach, the connection to the central grid can be removed or minimised so that the power quality to sensitive loads can be enhanced. Generally, they have two operation modes:

- **Stand-alone (island) mode**: in this mode of operation, a microgrid operates on its own with its distributed energy sources fulfilling the load demand.
- **Grid-connected mode**: microgrid is connected to the main grid, which satisfies the load demand. Since we are concerned with DCMG, this mode requires AC/DC conversion at the grid interface (in-case of legacy grid)

A microgrids needs to have a reliable and versatile protection. AC systems have plenty of experience and standards when it comes to protection. DC systems do not have either of these advantages. The protection devices commercially available for low-voltage DC-bus systems are fuses and Circuit breakers.

Because microgrid systems need to be multi-terminal, voltage-source converters (VSCs) must be used to interface different subsystems to the bus. Fault current must be detected and extinguished very quickly as converter’s fault withstand rating is generally only twice the full-load rating [10].

**Smart Microgrid**: It is a term used to differentiate the technological sophistication of a microgrid. Generally the term Microgrid alone is used to refer smart-microgrid. In truth, not every DCMG is smart in itself; this quality is given by its control systems, and in general by how the grid can serve, protect and check loads and sources; reference [43] summarizes this concept in

"the advanced communications overlay that makes a grid a Smart Grid."

### 1-4-4 LVDC Standard

Since LVDC is very young in the development phase, The standard operating voltage has to be set, keeping in mind couple of facts:

- Transferring the same power at higher voltage results in lower transfer loss in cable.
- Voltage level and electrocution risk increase together.
- A higher voltage level forces to improve the switches rating.

The upper voltage limit of LVDC is set at 1500V or 1.5KV by IEC 60634, although standardised, the nominal voltage is far from it, thus unstandardised safety measures.

As of today, multiple voltage standard are being used, for example [21].:
• 380V DC: Building services, data centres, variable speed drive (Washer, Driver, Air Cond.).
• 5-100V DC: Computer power delivery, Laptop and tablet charger, flash-drives, etc..
• 48V DC: Lighting, consumer electronics (TVs, PCs, Projectors.), telecom central offices.
• 5-20V DC: USB type C power delivery, external hard-disk, flash-drives, smart phone chargers, etc.
• Other: 1000V DC, 900V DC, 750V DC, 600V DC, 400V DC, 350V DC, 260V DC, etc.

And then there is bipolar link with midpoint grounding offer additional voltage option; for instance a system with 350V DC on positive to neutral or negative to neutral side and offers a 700V DC link over positive and negative polarity.

According to [21] the draft standard is pushing for 380V DC as distribution level and industrial level and 48V DC as consumer level. Why? 380V:

• Higher reliability
• Higher efficiency
• Smaller size
• Better power quality
• Easier integration of Renewable Energy

48V DC:

• Majority of household application are rated at 48V DC maximum.
• Lower concern of accidental electrocution.

1-5 Power Electronics in DC Microgrid

DCMG would not be possible if it weren’t for advancement in research and development of power electronic converters. What a transformer is for an AC system, a power electronic converter is for a DC system. Converters are the medium to regulate the voltage levels, and can be classified into 3 different types on the basis of conversion:

• Inverter: Converts DC voltage to AC voltage.
• Rectifier: Converts AC voltage to DC voltage.
• DC-DC converter: Converts DC voltage from one level to another, i.e. either step-up, step-down or both.
The output of the converter is never an ideal DC or AC waveform, the inverter output is plagued with DC component and the rectifier’s output with AC component, additionally every power electronic converter output is full of ripples (rather than constant DC or smooth AC, we have fast changing voltage), which is undesirable, thus filters are employed to get rid of ripples and the addition components discussed earlier. The filter (low-pass)is made up of an inductor and a capacitor, L-C filter [44].

Since we are concerned with DCMG, we will only go in depth with DC-DC converters. In this section, the basic DC-DC converters are explained [44]:

1-5-1 Basics of DC-DC Converter

Power electronic converter were made possible only due to the recent advancement in research and development of semiconductor-based switches, usually called the transistors. Transistors can be either current (BJTs) or voltage (FETs) driven switches. Voltage driven switches are preferred due to their adherent advantages, widely used ones are MOSFETs and IGBTs. Power MOSFETs can switch(change state from on to off or vice versa) with frequency of 100s of KHz, and carry current in hundreds of amperes or block up to 1 KV. An IGBT is comparatively slower, it switches with frequency of 10s of KHz, but can carry current in thousands of amperes or block up to couple of KV.

Switch on or off state is achieved by comparing a control signal with a repetitive waveform, usually a sawtooth-shaped; the control signal can be varied in order to modify the DC output. The frequency of repetitive waveform gives the switching frequency $f_s$, inverse of which is $T_s$. During a single switching cycle, switch is either on (Conducts current at low voltage) or off (blocks current at high voltage). The ratio between on-time interval and the switching time interval is the duty cycle $D$. All the above discussed concepts are illustrated in the Figure, this makes up the constant frequency Pulse Width Modulation control.

The DC-DC converter can have two distinct mode of operation:

- Continuous Current conduction Mode (CCM): Inductor current flows continuously, i.e. current through the inductor increases to max during the switch on-interval , and the current value does not decrease to zero during the switch off-interval.

- Discontinuous Current conduction Mode (DCM):Inductor current flows discontinuously, the current value becomes zero for a finite amount of time, i.e. current through inductor increases to max during the switch on-interval , and the current value does decrease to zero during the switch off-interval.

There are multiple different types of DC-DC converters, but we only look into the three basic topologies, and they are as follows:

- Buck Converter: Step-down converter.

- Boost Converter: Step-up converter.

- Buck-Boost Converter: Step-down and Step-up converter.
1-5-2 DC-DC Buck Converter

Also known as Step-Down converter, a DC-DC buck converter produces lower average voltage than the DC input voltage $V_d$, the main application is in regulated DC power supplies and DC motor speed control.

![Buck converter schematic.](image)

**Figure 1-8:** Buck converter schematic.

The basic circuit is depicted in the Figure, 1-8; it constitutes of a step-down converter with the switch and freewheeling diode (used to define the power transfer direction, and to provide a path to the inductor current if the switch is off), L-C filter and the resistive load. It is assumed that all the components are ideal [45].

For a buck converter, the relationship between input and output voltage can be deduced through a voltage-time ($s$) relation on the inductor. The concept underlying is the following: in steady state, the waveforms have to be periodic, that is, the current of the inductor at the beginning has to be equal to the end of the switching period. Moreover, in an inductor, current and voltage are related by:

$$v_L = L \frac{\partial i}{\partial t} \iff i(t) = i(0) + \int_0^t \frac{v_L}{L} dt$$

(1-3)

Over a period, in CCM and neglecting the voltage drop over diode and parasitic resistances of the inductor (ideal), $v_L = V_i - V_o$ if the switch is conducting, or else $v_L = -V_o$. Integrating Equation 1-3, over the boundary of the voltage-time($s$) balance, gives:

$$(v_i - v_o)DT_s = -v_o(1 - D)T_s \implies \frac{v_o}{v_i} = D$$

(1-4)

An ideal buck converter follows the law of power conservation in steady state; i.e, no energy is stored in the passive components when the steady state is reached. The ratio between input and output currents is given by $1/D$. Equation 1-4 (and its consequence) shows the similarity between this DC-DC converter and an AC transformer; for the latter, an analogous relation
holds, where $D$ is substituted by the turns ratio of the transformer.

The same result obtained in equation 1-4 can be derived by averaging the output of the buck converter:

$$v_o = \frac{1}{T} \int_0^{T_s} v_i dt \implies \frac{1}{T} \int_0^{DT_s} v_i dt + 0 \implies \frac{v_o}{v_i} = D$$  \hspace{1cm} (1-5)$$

In DCM the same relationship does hold, but a different result is obtained, because of the finite period where the inductor current is zero. In order to study this behaviour, it is interesting to have a look at the boundary between Continuous Conduction Mode (CCM) and Discontinuous Conduction Mode (DCM). There, the average inductor current, supposed the output voltage is constant, is given by:

$$i_{L,B} = \frac{V_o}{2f_s L} (1 - D) \implies I_{L,B,max} = \frac{V_o}{2f_s L}$$  \hspace{1cm} (1-6)$$

Note that $i_{L,B}$ with a finite $V_o$ and $D = 0$ is a purely-theoretical case, since the input voltage should be infinite. $I_{L,B,max}$, together with the output current $i_o$, gives a relation for the duty cycle in DCM:

$$D = \frac{v_o}{v_i} \sqrt{\frac{i_o/I_{L,B,max}}{1 - v_o/v_i}}$$  \hspace{1cm} (1-7)$$

Equation 1-7 is plotted, for various values of $D$, in Figure 1-9. Considering this graph, and what expressed by Equation 1-6, it can be derived as rule of thumb that a smaller inductor will make it easier for a converter to be in DCM. Being the purpose of the buck converter to control the output voltage, the ripple in this quantity has to be determined. It is defined as the difference between the maximum and the minimum voltages of the output capacitor, which appear because of its ability in absorbing the DC part of $i_o$. This can be explained
with the fact that, if the switch is off, all of the output power has to come only from the capacitor. This ripple is usually expressed as percentage of $v_o$, and calculated as:

$$\Delta v_{\text{ripple}, \%} = 100 \frac{\Delta v_o}{v_o} = \frac{12.5}{f_s^2 LC} (1 - D)$$  \hspace{1cm} (1-8)$$

In can also be related to a constant input voltage, in CCM, with a small modification of Equation 1-8:

$$\Delta v_{\text{ripple}, \%} = \frac{12.5v_i}{f_s^2 LC} D(1 - D)$$  \hspace{1cm} (1-9)$$

Equation 1-9 shows how the maximum ripple with respect to the input is obtained at 50% duty cycle. With respect to the efficiency, a buck converter performs better if operated at high duty cycle, since the diode has higher conduction losses with respect to a switch. Other losses are given by the parasitic resistances of the passive components.

### 1-5-3 DC-DC Boost Converter

A boost converter is the reverse topology with respect to buck converter, presented in the previous section; the output voltage is always equal to or higher than the input voltage. Its schematic is depicted in Figure 1-10.

![Boost converter schematic](image)

**Figure 1-10:** Boost converter schematic.

From the relation presented in Equation 1-5, the relationship between duty cycle and voltage at the terminals can be derived. Moreover, using the already-presented steady-state power conservation hypothesis, the two currents at input and output can be related. For CCM:
It should be noted that, in this case, the inductor current \( i_L \) is always equal to the input current. \( i_o \), for power conservation, will be smaller of a factor depending on the duty cycle. This, intuitively, can be derived from the fact that this current is routed alternatively through the switch or through the diode, and only the diode’s one contributes to the output power. As it was done for the buck topology, an average current can be defined for the boundary between CCM and DCM; this time, it will be the output current. Moreover, this current will present a maximum value, as shown in Equation 1-11:

\[
 i_{o,B} = \frac{v_o}{2f_sL}D(1-D)^2 \implies \frac{I_{o,B,\text{max}}}{I_{o,B}} = \frac{2v_o}{27f_sL} \quad (1-11)
\]

Analogously, \( I_{o,B,\text{max}} \) can be used to determine the relationship between the voltage at the two terminals and the duty cycle:

\[
 D = \sqrt{\frac{4}{27f_sL}} \frac{v_o(v_o - v_i)}{i_o} \quad (1-12)
\]

A graph similar to the one of Figure 1-9 can be plotted for a boost converter as well. The outcome does not qualitatively vary too much. Conversely, with respect to the buck topology, the highest efficiencies will be attained if the duty cycle remains on low values. If it increases beyond a certain threshold, the behaviour of the converter will deviate considerably from that predicted by the Equation 1-10, and the output voltage will start to decrease.

The output voltage ripple, in CCM, is given by

\[
 \Delta v_{\text{ripple,\%}} = 100 \frac{\Delta v_o}{v_o} = 100 \frac{i_o(v_o - v_i)}{v_o^2Cf_s} \quad (1-13)
\]

### 1.5.4 DC- DC Buck-Boost Converter

the converter is depicted in the Figure 1-11.

The peculiarity of the buck-boost converter, with respect to the previous two topologies, is the inversion of the output voltage with respect to the input, needed for the voltage-time (s) balance. Keeping this in mind, on applying Equation 1-5 to CCM, the usual relations between duty cycle and currents or voltages could be found as:

\[
 \frac{v_o}{v_i} = \frac{D}{1-D} \implies \frac{i_o}{i_i} = \frac{1}{D} - 1 \quad (1-14)
\]

It appears that a buck-boost converter can perform the operations of both buck and boost converters, one at a time. As before, the average output current can be found for constant \( v_o \), along with its maximum; these can enter the expression for the duty cycle in DCM.
Figure 1-11: Inverting buck-boost schematic.

\[ i_{o,B} = \frac{v_o}{2f_s L} (1 - D)^2 \implies I_{o,B,\text{max}} = \frac{v_o}{2f_s L} \]  

(1-15)

\[ D = \frac{v_o}{v_i} \sqrt{\frac{i_o}{I_{o,B,\text{max}}}} \]  

(1-16)

The CCM and DCM regions, as functions of \( D \) and \( i_o/I_{o,B,\text{max}} \), acquire a rather different shape with respect to the previous cases; this is reported in Figure 1-12. With respect to losses, a buck-boost converter behaves as a boost converter. The ripple in the CCM output voltage is expressed by Equation 1-17.

\[ \Delta v_{\text{ripple},\%} = 100 \frac{\Delta v_o}{v_o} = 100 \frac{i_o}{(v_o + v_i)Cf_s} \]  

(1-17)

The switch utilization is in general rather poor, so buck-boost converters should be used only if a full control of the output is necessary. A buck-boost converter can be isolated through a high-frequency transformer, as already mentioned for the buck topology.

**Non-Inverting Buckboost Converter**

This converter, described in [46] and depicted in Figure 1-13, is made up by a quasi-series of buck and boost converters: they can be considered to be cascaded, but they share the passive components of the L-C filter. There are one more diode and two switches. The switches of this converter can act almost independently, with a single condition to be met: the buck switch should be always on when the boost switch is. This avoids the appearance of a low-impedance current loop within the converter [47]. Although this configuration increases the switches utilization in both modes, more components...
Figure 1-12: CCM and DCM areas of operation for a buckboost converter. The dashed line refers to the boundary between CCM and DCM (from [44]).

Figure 1-13: Non inverting buck-boost schematic.

are needed and their losses should be taken into account; as an example, in the buck mode there will always be an extra diode on the path. This converter is granted to work linearly at least for $v_o \leq 2v_i$ [46].
1-6 Concept of Power Balance and Control

As the name suggests, power balance is the equilibrium between source and load. It refers to the use of various techniques by electrical power stations to store excess electrical power during low demand periods for release as demand rises. The goal would be for the power supply system to see a load factor of 1.

\[
\text{Load Factor} = \frac{\text{Average Load}}{\text{Maximum load in given time period}}
\]  
(1-18)

Grid energy storage stores electricity within the transmission grid beyond the customer. Alternatively, the storage can be distributed and involve the customer, for instance in storage heaters running demand-response tariffs, or in a vehicle-to-grid system to use storage from electric vehicle during peak times and then replenish it during off-peak times. These require incentives for consumer to participate, usually by offering cheaper rates off-peak electricity.

The above discussed concept with load factor holds for standard legacy and smart grids mostly due to the sheer vastness of the grid, standard load pattern, a microgrid is something small, it could be as small as a community to a single home which can operate on its own (Island). Anatomy of microgrid is very different from that of a legacy grid, i.e., it’s difficult to devise a standard load pattern. Every variation in load or source affects the stability of the grid. Since we are focusing on DC microgrid, the control parameters are only voltage (V) and current (I). Any increase in source output or decrease in load input increases the grid voltage and decrease in source output or increase in load input decreases the grid voltage, both of which could destabilize the grid. Control scheme has to be devised for healthy operation of the grid, hence the power balance control. The majority of renewable sources in DCMG are solar panel and wind mill, micro-turbines and fuel cells are also a possibility but are rare and difficult to maintain. These source’s output are dependent on weather and season, whereas a load is more or less constant or has a defined range of power consumption. Thus, power balancing suddenly becomes very critical for longer period of healthy grid operation. At any given moment of time, combined sources should satisfy the combined loads and the losses. As a buffer, grid and battery connections are employed to take care of the difference, where the battery or any other form of storage is given the preference. Even then if the combined loads and losses overwhelm the combined sources, load shedding is employed, where the load with least priority is shut down when the grid voltage level drops below a critical level (CL1) and then turned on when the grid voltage level increase another critical level (CL2), where CL2 ≥ CL1. In other case where the sources overpowers the loads, the excess is used to store and put back into grid. All of this ensures the equilibrium of the grid, where the source power is equal to load and loss power at a nominal voltage level.

To ensure all this plus additional redundancy, a proper control scheme has to be developed. This control scheme is employed into the power electronic interface between each component and the DCMG.

1-7 Problem Definition: the Power Balance control

Every research begins with the very fundamental question; The Why? Why is this necessary? Why isn’t the present technology good enough? These are the question that drives any
research.

The current system environment is at the verge of saturation and needs evolving, with more and more renewable energy integration as distributed sources, it’s only evident that a new system environment has to be developed to accommodate and optimise the evolution process into more efficient, safe, hassle free, reliable, ecosystem.

The problem today is that the legacy system is bulky, and introduction of any new technology leads to developing new interface which adds into inefficiency and unoptimised operation of the system. It’s like having an old computer and trying to use thunderbolt accessory with it, even though the old PC has no interface, their are adapters for it, but this doesn’t allow for the maximum use of the thunderbolt’s super high speed bandwidth (10MbPS).

Integration of renewable energy is the new technology refereed in the previous paragraph. The main source of renewable source, directly/indirectly is our star, the Sun. Due to rotation and revolution of Earth, being tilted at an axis of 23.50, and being on an elliptical path around the Sun, makes the solar energy a varying factor, over which we have no control. But since this energy is free, the hassle of integrating is worth the trouble, due to all the abrupt climatic changes.

1-8 Objectives

The objective of this MSc Thesis is to come up with a control scheme that doesn’t rely on communication for control operations. The integration of communication would make the system smarter but would provide the station with another point of failure, which raises reliability problems. The microgrid has to occasionally operate in island mode, separated from the main grid, which has to be accommodated in the controller design. Further, the controller should be as simple as to provide plug-and-play operation.

1-9 Research Questions

Based on everything discussed in the previous chapters and will elaborated in further chapters, especially on the definition of the problem and the objective, following research questions had to be answered at the end of this MSc Thesis:

- Is it possible to maintain power balance in a dynamic system, if yes, then how robust and reliable would the system be?
- Software simulation and real life tests are poles apart, so how would this control strategy perform in a real life experiment and what would be difficulties encountered during the implementation?
- How versatile is the power balance control scheme and explain with some possible scenarios?
- Does ‘Current pricing’ work with the changing dynamics of a real system?
- What are the hardware requirements to allow the control scheme to work optimally?
1-10 Contribution

Over the period of the thesis, various goals were achieved and the contribute to the current research process in the control of microgrids.

- **Power balance control:** The power balance control scheme is designed with the goal of utilising every possible power for the sake of stability of the grid. The control strategy is strong enough to support black start of grid and sustained operation of microgrid with changing dynamics.

- **Dynamic Current pricing:** The concept of dynamic pricing based on voltage was introduced by Mr. Laurens Mackay, but the analysis was done in steady state. This concept has been improved upon with current based pricing and the analysis is done in the dynamic system.

- **Hardware:** Even though the design of hardware may not be considered as a scientific contribution but it most certainly contribute to testing of other scientific contribution, such as hysteresis control, demand response, power balance control, and various safety techniques. The current assortment of hardware are limited in terms of testing capability of control schemes and security features.
Chapter 2

Modelling and Comparison of Power Electronic Converter

Computational modelling is the analysis of a power electronic converter schematic via a simulation so as to study its characteristics without the use of physical components, which reduce the expense of the components and time invested behind it. Various different modelling methods are there to reckon with, some use the ideal switches, close to real switch parameter, switch emulator techniques, etc [1, 48, 49, 50, 51]. Important parameter in computational modelling is the the computational time, a sophisticated model is likely to take longer time to finish the simulation. Thus depending on the analysis, a suitable modelling method is chosen with some trade-off in the low priority field [52].

For all intent and purposes of this thesis, control part of the analysis is prioritised thus the switch emulation technique is chosen, and PWM switching due it’s constant frequency operation is studied. Pulse-Width-Modulation (PWM) techniques are most popular in the application of switching power supplies. The power switches On-Off using PWM where the duty ratio (D) determines the average load voltage [53]. Feedback loop methodologies are an integral part of DC-DC converters to regulate the load voltage, compensating for load variations and irregularities in the source voltage [54]. The converter in our discussion is the DC-DC buck converter and three different modelling has been studied, and they are:

- Switching Model
- General Model
- Simplified Model

2-1 Switching Model

The schematic of the switching model for buck converter is presented in the Figure 2-1.
Figure 2-1: Schematic for Switching Model. Green highlighted area is the outer voltage control loop. Yellow highlighted area is the inner current control loop. In the schematic $e^*$ represents the error; i.e. the difference between the desired value and the current value, $d^*$ represents the duty cycle, generated from the current control loop, which is fed into the PWM generator which is then multiplied with the input voltage to obtain the output voltage.
The desired voltage value (Nominal voltage, $V_{\text{nom}}$ or reference voltage, $V_{\text{ref}}$) from the converter is compared to the previous output voltage, for the black start its zero. The error signal is fed into a controller, preferably a PID (Proportional, Integral and Differential) controller. The output of the controller is the reference current value, which is compared to the previous output current value of the converter. The error signal is then again fed into a controller, the output is the new duty cycle ($D$) which is fed into a PWM-Generator. The PWM-generator emulates the action of a switch constantly switching from on to off to on. The PWM-Generator output is the carrier signal for the duty cycle which is multiplied to the input voltage ($V_{\text{nom}}$) which gives the output voltage 1-4 [44].

But this output voltage is plagued ripples, which is filtered out using L-C filter and the smoothed waveform is fed into to the load. The figure below shows the output waveform for the switching model, where the duty cycle ($D$), PWM-switching, current filtered and un-filtered, voltage filtered and un-filtered.

From the waveform it can be seen that the average value increases linearly, with the increment being gradual from the output to the nominal/desired value. The rate of rise of output dependent on the parameters of the controller, for PID controller its the $K_p$ (proportionality constant), $K_i$ (integral constant), and $K_d$ (differential constant). The waveform in the switching circuit is in the form of undulation, where the wave changes it’s value from a minimum to a maximum value around the desired output. Now the average of the undulation gives the desired output. And for analysis and control, it’s the average value that is of importance, thus with some further simplification, we arrive at the average model, which will be discussed in the next section.

### 2-2 Average Model

The schematic of the average model for buck converter is presented in the Figure 2-3.

The desired voltage value (Nominal voltage, $V_{\text{nom}}$ or reference voltage, $V_{\text{ref}}$) from the converter is compared to the previous output voltage, for the black start its zero. The error signal is
Figure 2-3: Schematic for Average Model. Green highlighted area is the outer voltage control loop. Yellow highlighted area is the inner current control loop. In the schematic, $e^*$ represents the error; i.e., the difference between the desired value and the current value, $d^*$ represents the duty cycle, generated from the current control loop, which is multiplied with the input voltage to obtain the output voltage.
fed into a controller, preferably a PID (Proportional, Integral and Differential) controller. The output of the controller is the reference current value, which is compared to the previous output current value of the converter. The error signal is then again fed into a controller, the output, duty cycle (D) is multiplied with the input voltage ($V_{IN}$), which gives the output voltage 1-4. This schematic has two control loop, the inner loop is the current loop and the outer loop is the voltage loop. From the control point of view, the inner loop has to be much, much faster than the outer loop for it to be ready to catch in the data from the outer loop. The output of this schematic is smooth non-undulating waveform which represents the average output value, i.e the desired value. This makes analysis and control much easier

From the waveform it can seen that the values increase lineally, with gradual increment for the output towards the nominal value. The rate of rise of output dependent on the parameters of the controller, for PID controller its the Kp (proportionality constant), Ki (integral constant), and Kd (differential constant). The waveform from the average model is smooth curve representing the average value of the converter. Average model takes much less computational power and time than the switching model, which can further be reduced with out adversely affecting the operation of the converter.

2-3 Simplified Model

The schematic of the simplified model for buck converter is presented in the Figure 2-5.

The desired voltage value(Nominal voltage, $V_{nom}$ or reference voltage, $V_{ref}$) from the converter is compared to the previous output voltage, for black start its zero. The error signal is fed into a controller, preferably a PID (Proportional, Integral and Differential) controller. The output of the controller is the reference current value, which is compared to the previous output current value of the converter. The error signal is then which is fed into a low-pass filter. The low-pass filter replaces the inner current loop in the average model. Filtered value gives the current set point, which gives the output voltage 1-4 through the capacitor of the system. This schematic has only one control loop, the inner loop, the current loop is replaced
by a low-pass filter and the outer loop is the voltage loop. From the control point of view, the low pass filter has to be much, much faster than the outer loop, around 10-15 times [1].

The output of this schematic is smooth non-undulating waveform which represents the average output value, i.e. the desired value. This makes analysis and control much easier.

From the Figure 2-3 it can be seen that the values increase linearly, with gradual increment for the output towards the nominal value. The rate of rise of output dependent on the parameters of the controller, for PID controller its the Kp (proportionality constant), Ki (integral constant), and Kd (differential constant). The waveform from the average model is smooth curve representing the average value of the converter. Simplified model takes much less computational power and time than the average model, and even then the output waveform of the simplified and average model are close enough, thus the simplified model is chosen for our control purpose and further analysis.

### 2-3-1 Filter Time Constant

The low-pass filter’s time constant as stated above should be 10-15 times of that of the sampling time, stated by the research from [1]. But this necessarily is not the perfect solution, if the converter link capacitors are to be sized to realistic value. In the literature [1] system, the capacitor is rather sized quite large, which helps with ripple and makes for ideal simulations.

![Schematic for Simplified Model](image_url)
The filter time constant in our system is calculated using the rise time. Initially the afore-
mentioned time constant is implemented, then the output ripple is analysed. The time for
the current ripple to rise to 63.5% of its maximum current value should be the minimum time
constant for the low-pass filter.

The comparison is shown in the Figure 2-7.

2-4 Comparison Results

The Figure 2-4 shows the comparison of voltage and current in all of the three models. All
the controllers are tuned to work optimally. For this analysis a step response was chosen. The
buck converter has an input of 30V and output of 10V initially, at a finite time, the output
was changed to 15V. The figure plots the dynamics of individual converter at and around the
step signal. It can be seen that the average model’s output voltage and current is exactly
at the average of the output from the switching model, which should be case. The thing to
analyse is the response of simplified model versus that of the average model, at steady state
both the models have the same output current and voltage, which could be noticed as one
overlaps the other. When the step signal is introduced, the output rises to the new value
within a fraction of seconds delay. The simplified model due to a faster response, responds
quickier, but due to an appropriately sized filter, doesn’t increase in a rapid manner, rather the
rate of increase is slowed down and starts to fall behind that of the average model. But within
a short time simplified model catches up to the average model and both achieve stability at
the same time.

The Figure 2-4 shows the comparison of voltage and current in all of the three models with
incorrect tuning. All the controller have the same tuning parameters. As always, average
model output exactly overlaps the output of the switching model. It’s the simplified model
which fails to follow the average model closely. Due to the filter instead of a controller the
response is slow, so in steady state the simplified and average model overlap each other, but
in a dynamics, the response of simplified model falls behind to average model.
Figure 2-7: The oscillations in blue are in the case of filtered design suggested by [1], and the oscillations in orange are due to the filter design by calculating the rise time. The oscillations in latter is comparatively much lower than in that of the former.

Figure 2-8: Simplified modelling circuit’s output voltage and current.
Dynamics at initial start of the system

The figure 2-4 shows the start of a converter from 0 current and 0 voltage. The dynamics

Conclusions: The simplified model, if tuned properly could very closely replicate the average model. The simplified model is no-way perfect, as explained earlier, but one trades accuracy for faster computation time and simplicity and ease in use. In our case the trade-off was considered to be worth the while and finally the simplified model with the parameters in figure 2-4 was chosen to be the base for the modelling.
Control Topology

Control ensures optimum operation of the microgrid, under constant varying load and source, stability of a DCMG becomes an issue. Stability of DCMGs is influenced under high penetration of tightly regulated power converters used to interface distributed resources and loads[55]. In these systems, load converters and batteries during regulated charging mode behave as constant power load (CPL), thus extracting constant power from the DCMG[56]. CPLs introduce a negative incremental resistance feature, which reduces the system stability[50, 57, 55, 58]. Moreover, interconnecting DCMGs together in order to create multiple microgrid (DCMMG), intended to improve the operational stability could destabilize the system, depending on the line impedance between the DCMGs. To overcome the negative impedance instability problems of CPLs, two methods could be formed:

- **Passive Methods:** These are basic ones that employ damping passive elements in the (L-C filter of) source converter to reshape its impedance.

- **Active Methods:** These use active damping strategies [57, 55, 58, 59] and use virtual control loops to improve the stability, offering higher efficiency and reliability.

The ultimate goal is to design an active stabilization loop, with a combination of different types of control strategies in order to improve the stability of DCMG and DCMMG in the presence of constant power load/source, variable loads, and connection of MGs.

Due to transient response of sources, and the fact that they cannot be always available (in the case of RESs), storage becomes essential in the DCMG. Furthermore, they can be used for used for the ancillary services like voltage regulation, power quality improvement, and emergency power supply. Normally secondary battery, super capacitor, and flywheels are used as the storage system. It is desired to connect the storage system to a DC bus through converters in order to supply high reliable power to the loads.
3-1 Hierarchy of Control

Control scheme for a DCMG can be classified into three different types on the basis of type of control[1]:

- **Centralised Control**: Bundling of various power generators in combination with storage and load creates a virtual power point, which is controlled from a single point or centrally, like human brain controlling the entire body. Communication between different controllers is the integral part of this control.

- **Decentralised Control**: Sources, loads, and storage are individually controlled based on the key information of terminal voltage, reference voltage. Control is done locally, based on local information. Communication is not an integral part of this control, but with addition of low-bandwidth communication, wonders could be achieved.

Control scheme for a DCMG can be classified into three different types on the basis of level of control:

- **Primary Control**: It’s employed locally for every source inside the MG in order to regulate the current injection into the common bus automatically. This introduces the deviation of the common DC bus voltage, due to imbalance between power consumption and production.

- **Secondary Control**: It’s employed to restore the voltage of DCMG bus to nominal value. It removes the voltage deviations inside the DCMG by sending appropriate set point.

- **Tertiary Control**: It’s employed to restore the voltage of DCMMG to a nominal voltage value, facilitate current sharing. It requires low-bandwidth communication to transfer the set point data between different DCMGs.

As a goal of my thesis, the primary control of DCMG is addressed. The power balance controller consists of individual control strategies stitched together to form a hybrid controller, which is general enough to be used with all the operations, be it source, load, or bidirectional source load operation. The individual control strategies are described below:

- **Droop Control**: Voltage droop is the intentional loss in the output voltage from a device as it drives a load. A series resistor is included between the regulator output and the load. The resistance needs to be chosen so that at maximum output current, the output voltage at load is the minimum acceptable. Conversely when the output current is (near) zero, the voltage is near the maximum. This simply follows the Ohm’s law.

  In a controller not employing droop, when the load is increased in rapid succession, the output voltage will momentarily sag. Conversely when a heavy load is suddenly taken off, the voltage will show a peak. The output link capacitor have to absorb these transients before the loop has a chance to compensate. The Figure below shows the transient. The maximum allowed voltage regulation is $V_{\text{max}} - V_{\text{nom}}$. Now the controller with droop, the maximum voltage regulation has doubled; $V_{\text{max}} - V_{\text{min}}$. This increase in tolerance to transients allows decrease in the capacitor value, or get better voltage regulation with same number of capacitor [60].
Why Droop? In order to connect number of voltage source converter (VSC) based sources in parallel, this control loop shares current between the units accordingly, and reduces the circulating current when the DCMG units voltages are different. Moreover, it improves the dynamic performance of the source output voltage[61]. This control creates appropriate voltage references for the voltage inner loop:

\[ v_{\text{ref}} = v_{\text{MG}}^* - R_d \times i_0 \]  \hspace{1cm} (3-1)

with \( v_{\text{MG}}^* \) being the MG voltage reference, \( i_0 \) is the output current and \( R_d \) is the virtual resistance. To ensure low voltage deviation, low value of droop gain \( R_d \) is used. Larger droop gains, more voltage deviation of the DCMG and better load sharing.

Although Droop control has been proven as an efficient method for parallel operation of sources inside DCMG, it still has its fair share of problems. In DCMG, power sharing is realised by linearly reducing the voltage reference as the output current increases [62, 61]. The output current sharing accuracy is degraded due to effect of the voltage drop across the line impedance. This effect is similar to the reactive power sharing of AC microgrids with inductive line impedances. To overcome the mismatch of line impedances, the concept of virtual impedance was proposed to match the unequal line impedances [63]. In addition to the problem of current sharing accuracy in a DCMG, a voltage deviation is produced since droop control is realised by reducing the DC output voltage. To solve this problem, a centralised controller can eliminate the voltage deviation [61].

- **Constant Power Control:** The idea is simple, to supply a fixed power level to the load. But it’s simple only if load impedance is known, and the impedance doesn’t change [50, 55, 58, 59]. Simply apply a constant voltage based on the formula for power in a resistive load:

\[ \text{Power}(P) = \frac{V^2}{R} = V \times I \]  \hspace{1cm} (3-2)
But, the question arises, how to deliver constant power when load isn’t constant? As the load and the source varies, impedance and the current changes as well, complicating the the delivery of constant power.

To maintain constant power, power into feedback network is incorporated. The error amplifier then compares a sample of output power against the reference, and drives the output stage to maintain them equal [64].

When load increases, it draws more current, which from the above equation gives a reference voltage. This reference voltage is fed into the amplifier, to set as the bus voltage. Unlike droop control, constant power control waveform is non-linear, it is hyperbolic. Constant power control generally sets in when any of the connected element reaches its maximum power capacity.

- **Constant current Control:** Or maximum current control, is a limit imposed on every source and load to protect it against over current. The waveform is a straight line with zero or infinite slope depending on the X-Y axis position of current.

### 3-2 The Hybrid Power Balance Controller

This section describes in elaborate about the controller designed as per my MSc thesis. It’s an amalgamation of all the former discussed primary control strategies. The final controller is shown in figure 3-3. The curve in the figure gives a general overview of the converter operation. The curve is supposed to serve as a guide, such that at any given grid voltage the converter always has an operating point. This in general is really useful, under the situation when the grid voltage is either too high or too low, cause the controller then stops the load/source respectively from dropping out and aggravating the condition. This general power balance curve is calculated from the equations based on the converter’s local parameters (Maximum/minimum power, maximum/minimum current, droop coefficient, local current and voltage measurements, and nominal voltage), hence each converter has its individual unique curve to follow.

Thus the power balance controller is bidirectional, easy to implement and can even facilitate plug and play. Another important feature is the introduction of dead-band, which is elaborated in later sections, along with the equations and their explanations.
Figure 3-3: Control characteristic of a bidirectional power source. The negative-current hemiplane corresponds to the operation as load, while in the positive-current hemiplane the device acts as source. The current maximum and minimum are denoted by vertical lines, while the operations at constant power retain the shape of a hyperbole. The dead-band can be seen as delimited by two dashed and parallel lines; it truly only affects the operations if the current is null. Last, the droop characteristics are straight lines of slope $-1/R_D$.

Note how, for both hemiplanes, the conditions on power, current and droop should be defined for a totally-controlled functionality.
3-2-1 Operation of The Controller

The controller switches between different modes of operation depending on converters local parameters, terminal voltage, local current, local power, maximum and minimum voltage, maximum and minimum current, and the local droop coefficient. All these parameters are used to calculate the set point for the converter output, which is carried on again and again with the resolution depending on the sampling time. The intersection point between different control strategy is fixed for a converter depending upon its parameters, i.e., the curve in the figure is fixed and unique with unique intersection for every converter depending on the parameters.

3-2-2 Controller Equations

As discussed in the previous chapter, the intersection points are unique in every converter. These intersection points need to be flexible enough so as to be used in plethora of converters with diverse characteristics, allowing the capability of plug and play. The equation to calculate the intersection points had to be derived, and are as follows:

### Source Side

Voltage intersection point $V_0$:

$$V_0 = 0V$$  \hspace{1cm} (3-3)

This point of intersection is the lowest value of the voltage that can be allowed by the converter or the grid (which ever is higher). This necessarily need not be zero, zero here is used to show the dynamic characteristics of control topology. For any voltage value higher than this, the converter falls into maximum current mode of operation. This is the maximum value of the current that the converter, grid, or the device (dictated by the lowest among three) can handle.

Voltage intersection point $V_1$, between maximum current and constant power source:

$$V_1 = \frac{P_{\text{max},S}}{I_{\text{max},S}}$$  \hspace{1cm} (3-4)

where $P_{\text{max},S}$ is the maximum power rating of the converter, device, or the grid (lowest among the three), and $I_{\text{max},S}$ is the maximum current rating of the converter, device, or the grid (lowest among the three) for source mode operation. This point of intersection gives the transitional point from constant power operation to maximum current and vice versa. Voltage higher than $V_1$, and we have constant power mode of operation and voltage lower than $V_1$, and we have maximum current mode of operation. At certain times the voltage fluctuates between the two modes of operation, which causes fast switching and thus can induce ripples in the grid. This situation could be eliminated by a good filter or importing the features of hysteresis control or smoothing the intersection point by introducing an arc with a finite radius.

Voltage intersection point $V_2$, between constant power source and Droop:

$$V_2 = \frac{V_{\text{ref},s} + \sqrt{V_{\text{ref},s}^2 - 4P_{\text{max},S} \cdot D_s}}{2}$$  \hspace{1cm} (3-5)
where $V_{ref_s}$ is desired nominal voltage for source side, $P_{max_s}$ is the maximum power rating of the converter, device, or the grid (lowest among the three), and $D_P_s$ is the droop coefficient for source mode of operation. This voltage value is the intersection point between constant power mode of operation and droop mode of operation. Voltage higher than $V_2$, and we have Droop mode of operation and voltage lower than $V_2$, and we have constant power mode of operation. The transition is rather gradual hence the switching ripples are less likely to occur at and around the point of intersection, which could be reduced further by using good filters and importing features of hysteresis control or smoothing the intersection point by introducing an arc with a finite radius.

Voltage intersection point $V_3$, between Droop and dead-band:

$$V_3 = V_{nom} - \frac{V_{dead-band}}{2}$$  \hspace{1cm} (3-6)

where $V_{nom}$ is the nominal voltage for the grid where current is zero, $V_{dead-band}$ is the range of dead-band voltage. Dead-band voltage is a range, corresponding to which the current is zero. This is there to eliminate constant switching between source and load mode of operation for a bidirectional converter. $V_3$ is the voltage where the droop begins, the current at this voltage value is zero.

Under certain circumstances the converter directly falls into maximum current current operation from Droop, the voltage intersection point $V_{21}$ is given by:

$$V_{21} = V_{ref_s} - I_{max_s} \times D_P_s$$  \hspace{1cm} (3-7)

where $V_{ref_s}$ is desired nominal voltage for source side, $I_{max_s}$ is the maximum current rating of the converter, device, or the grid (lowest among the three), and $D_P_s$ is the droop coefficient for source mode of operation. This is circumstance is where the controller transitions from Droop mode to maximum current mode, cause the maximum power is never reached.

**Dead-Band Voltage**

This is defined as a range of voltage for which current stays at zero.

$$V_{DB} = V_{nom} \pm \frac{V_{dead-band}}{2}$$  \hspace{1cm} (3-8)

where $V_{DB}$ is the higher and the lower end of the dead-band voltage, $V_{nom}$ is the nominal voltage and, and $V_{dead-band}$ is the dead-band voltage range. In general the $V_{DB}$ is the range of voltage for which the current stays zero. The converter operates in load mode, if the voltage is higher than the upper range of dead-band and in source mode if lower than the lower range of dead-band voltage. This is there to prevent the converter from simultaneously switching between load and source mode of operation.

**Load Side**

Voltage intersection point $V_4$, between Droop and dead-band:

$$V_{ref_l} = V_{nom} + \frac{V_{dead-band}}{2}$$  \hspace{1cm} (3-9)
where $V_{\text{ref}, \text{l}}$ represents the voltage point from which the load side droop begins which is given by the nominal voltage $V_{\text{nom}}$ plus half of the dead-band voltage $V_{\text{dead-band}}$.

Under load side of operation two conditions could appear:

- **Standard condition**: The controller switches from droop control to constant power, same as in the source converter side operation. The voltage intersection point is given by $V_{65}$.

- **Maximum current condition**: The condition for maximum current is reached before constant power, as the voltage keeps increasing, the converter then starts to operate in constant power operation. The voltage intersection point is given by $V_{5}$.

Voltage intersection point $V_{5}$, between Droop and maximum current is:

$$V_{5} = V_{\text{ref}, \text{l}} - I_{\text{min}} \ast D_{P_{\text{l}}}(3-10)$$

where $V_{5}$ represents the voltage point at which the controller switches from droop to maximum current mode of operation. This is the case where the maximum current is reached before the maximum power boundary was reached.

Voltage intersection point $V_{65}$, between Droop and constant power load:

$$V_{65} = V_{\text{ref}, \text{l}} + \sqrt{V_{\text{ref}, \text{l}}^{2} - 4P_{\text{min}} \ast D_{P_{\text{l}}}}(3-11)$$

where $V_{65}$ represents the voltage point at which the controller switches from droop to constant power mode of operation. This is the case where the constant power is reached before the maximum current boundary was reached. Voltage intersection point $V_{6}$, between maximum current and constant power load is:

$$V_{6} = \frac{P_{\text{min}}}{I_{\text{min}}}(3-12)$$

In the load side of operation, things happen quite differently, loads generally are constant power loads. So the loads have maximum current mode of operation after droop and then once the voltage raises beyond the setpoint, it falls into constant power mode of operation. This point is given by $V_{6}$.

### 3-2-3 Classification of Operation of Controller

The operation of converter can be further classified into multiple orthodox and un-orthodox operation. Orthodox as in unidirectional mode of operation, i.e. pure source or pure load. Un-orthodox as in bidirectional mode of operation, i.e bidirectional power grid, storage, etc. But the controller operation will be elaborated using these three classifications, on the basis of mode of operation:

- **Pure Source mode of Operation**
- **Pure Load mode of Operation**
- **Source and Load mode of Operation**
Pure Source Mode of Operation

Under this operation the converter acts as a pure source, once the voltage increases beyond the dead-band intersection, the converter stops; it automatically stops sharing current due to droop. The entire process is illustrated in the figure 5-5. This in general could be illustrated by renewable energy sources (other than fuel cell, and some hydro-plants), fossil fuel generators, CHPs (Combined Heat and Power), legacy grid. The source operates between the nominal voltage $V_{nom}$ and the lowest permissible voltage $V_0$ level. In this range the current value is only positive (Source current convention), thus can only provide power cannot accept it. Different sources operate at different mode of operation at the same voltage level. Generally in centralised model, it’s quite easy to assign each converter their mode of operation, like solar PV should always be at maximum power, only should it droop to avoid over voltage. But in decentralised control without communication, each controller is assigned a different nominal voltage, such that at grid nominal voltage, the solar PV (other free sources) is at maximum power, and the non-renewable sources at droop. This is done in order to extract every possible free energy, only when this is not enough, non-renewable sources act, and when they both aren’t enough is when the grid contributes. The nominal voltage for renewable ($V_{nom_R}$) is higher than the nominal voltage of non-renewable energy ($V_{nom_N R}$), which in turn is higher than that of grids ($V_{nom_G}$).

$$V_{nom_R} > V_{nom_N R} > V_{nom_G}$$ (3-13)

Pure Load Mode of Operation

Under this operation the converter acts as a pure load, once the voltage decreases beyond the dead-band intersection, the converter stops; it automatically stops taking current due to droop. The entire process is illustrated in the figure 3-5. This in general could be illustrated by loads such as computers, washing machine, lighting, air condition etc.. The load operates between the nominal voltage $V_{nom}$ and the highest permissible voltage $V_H$ level. In this range the current value is only negative (Load current convention), thus can only take power cannot give it. Different loads operate at different mode of operation at the same voltage level. Generally in centralised model, it’s quite easy to assign each converter their mode of operation, like load 1 could be operating at maximum power, while some are at droop and others at maximum current. But in decentralised control without communication, each controller is assigned a different nominal voltage, such that at grid nominal voltage, the high priority loads are at maximum power, and the loads that can be throttled operate at droop, and some loads at maximum current. Loads in general are constant power devices. This is done in order to stabilize the grid, when the voltage falls below a certain level, non-essential loads could be turned off, while the loads which can be throttled (lighting system fans) could operate at droop or be turned off. The nominal voltage is has to be lower than that of the pure source.

Source and Load Mode of Operation

Under this operation the converter acts as a source and load, once the voltage increases beyond the dead-band intersection, the converter becomes load; it reverses the flow of current. The
Figure 3-4: Source mode of operation, here all the three modes of operation are shown, initially it starts with droop at around 400V, then to the constant power at 380V and finally into maximum current at 302V.
(a) With maximum current operation in play. At around 1.4A, the maximum current limit is hit, the voltage keeps increasing, at around 360V the constant power operation begins.

(b) Without maximum current operation in play. At around 320V constant power operation begins, and the maximum current limit is never reached.

**Figure 3-5:** Pure Load mode of operation. With the reference voltage at around 300V, the droop begins.

(a) With constant power operation in play. At around 335V constant power operation begins, and at around 280V/1.8A maximum current operation begins, for source side. Same is the case at higher voltage for load side of operation.

(b) Without constant power in play. At around 320V/1.5A maximum current operation begins, without encountering constant power operation for Source side. Same is the case at higher voltage for load side of operation.

**Figure 3-6:** Source and Load mode of operation. Source side voltage reference is at around 330V and the load side voltage reference is at around 350V.
entire process is illustrated in the figure 3-6. This in general could be illustrated by bidirectional grids and storage elements, such as battery, fuel cell, hydro storage etc. The converter operates between the lowest permissible voltage $V_0$ and the highest permissible voltage $V_H$ level. In this range the current value is not only positive (Source current conversion) but is also negative (Load current convention), thus can take and give power. Different converters operate in different modes of operation, some could be in source mode, load mode, or even could be in off state. In an individual mode of operation some could be in droop, maximum power, or maximum current. Storage and grid operation principle varies a lot, since they could have emphasis on price, stability, backup, or island operation. Nominal voltage level could be higher than that of load, but most certainly lower than that of the renewable sources.

The same control algorithm is used in all of the above conditions, by varying the parameters, one or the other condition could be obtained. Thus the converter algorithm is abstract enough, that it could be used under any scenario and could very well work without communication or central controller. Loss or gain of any source or load is automatically adjusted due to their contribution in stabilizing/destabilizing grid voltage.
Electric power system is very sensitive in nature, it balances on a needle point between sources and loads, so any change could disrupt this balance, now one way to cope with this is to use huge storage systems; which are cost intense. Another possibility is to use the energy when it is available. This is called demand side participation, which can be done directly by the grid operators, switching off specific loads, or by using variable energy prices. However doing this manually is too expensive, compared to the savings achieved, and therefore demand shift should be done more or less autonomously [65].

One possibility is that devices know the current price and react on it. Internet connection to fridges is one example for smart grids and how the load can be controlled [66]. While it sounds interesting, it would involve enormous costs and system complexity to connect every single device. One has to think of the millions of small devices, that would need an internet connection. However, a fully bidirectional communication is not necessary to implement demand response with variable prices. Only the price has to be communicated to the devices. Devices can determine the price in a DC grid using the local current value. The additional costs are limited as more and more devices use DC internally.

The emergence of the decentralised generation suggests a more abstract market model. The market model is based on the concept of "prosumers" that can produce and consume energy [67]. They are connected by DC grids managed by their system operators. Those grids can be connected to higher level grids where they act as aggregated prosumers. The energy price can be different at every node in the grid, known as nodal pricing. Power fed into grid has the same price as the power taken out of at the same place and time. The only trading partner of prosumers is the local system operator. Prices are based on supply and demand and additional congestion costs, in case of insufficient grid capacity, and are determined according to the system operator. The construction and maintenance cost of the grid are charged to the prosumers independently of the effective energy consumed or produced. However, the grid connection price can be based on the maximum power capacity of the connection.
4-1 The Why?

Parameters governing transfer of electric power are current (I) and voltage (V), where the load dictates a constant amount of current under a small range of voltage. Then again transmitting power over large distance cause voltage drops across parasitic passive elements. The power loss is given by the voltage difference between two ends of the cable. The power line loss is given by:

\[ P_l = U_{12} \cdot I \]  \hspace{1cm} (4-1)  
\[ P_l = (U_1 - U_2) \cdot I \]  \hspace{1cm} (4-2)  
\[ P_l = U_1 \cdot I - U_2 \cdot I \]  \hspace{1cm} (4-3)

Power sent at the one end of transmission is given by \( U_1 \cdot I \) and the power received at the other end is given by \( U_2 \cdot I \). The voltage varies according to the passive element of the transmission line, but the current value remains the same. Thus pricing based on current makes more sense. Moreover to keep the voltage at the required level, the current value is pushed up, thus all the cost incurred due to losses are covered up in the current based pricing.

4-2 Steady State analysis

For steady state analysis a simple setup is chosen with a single source, \( P_1 \); a single load, \( P_2 \); which is given by [65]. The only passive element would be the resistance substituting the line resistance. The loss across the line resistance would be \( P_l \):
\[ P_l = P_1 - P_2 = V_1 I_1 - V_2 I_2 \] (4-4)

In this system the source current should be equal to load current since a resistor only introduces a drop in voltage, hence:

\[ I_1 = I_2 = I \] (4-5)

Thus the loss becomes:

\[ P_l = (V_1 - V_2) I \] (4-6)

And the current remains the same at both the ends, source or load. If the pricing were to be done based on current, it would be as:

\[ \int (\kappa I_1) dt = \int (\kappa I_2) dt \] (4-7)

where \( \kappa \) is the nominal price for the current at a given moment of time. We assume that the the price per unit paid by the consumer is the same received by producer. Any administrative charges are assumed to be null.

Integral of current over time \( t \) gives total amount of charge \( (Q) \) in Coulombs. Thus after integrating the above equation we get:

\[ \kappa Q_1 = \kappa Q_2 \] (4-8)

The equation 4-2 seems simple and obvious, but in reality we don’t have any pure resistive element in nature. A passive component always accompanies some finite value of resistance \( (R) \), inductance \( (L) \), and capacitance \( (C) \). This is not the same as a pure resistive circuit, hence a dynamic analysis was performed.

### 4-3 Dynamic State analysis

A circuit with resistance \( (R) \), inductance \( (L) \), and capacitance \( (C) \) elements have power dissipative, current storing, and voltage storing elements respectively. Combination of these elements causes the circuit to resist the changes in the current and voltage value which causes the delay.

By Kichoff’s current law:

\[ I_1 = I_S + I_{CS} \] (4-9)

Where \( I_1 \) is the current from the source converter: interface

\[ I_2 = I_L + I_{CL} \] (4-10)
Figure 4-2: Setup for dynamic analysis.

Where $I_2$ is the current from the Load converter: interface

$$I_2 = I_1 - I_C$$  \hspace{1cm} (4-11)

Where $I_C$ is the current through the line capacitance

For current pricing we need to have:

$$\int (\kappa I_1) dt = \int (\kappa I_2) dt$$  \hspace{1cm} (4-12)

For this to hold true at any given moment of time:

$$I_1 = I_2$$  \hspace{1cm} (4-13)

but in a realistic circuit, this can't be true; so the current based pricing becomes:

$$\int (\kappa I_1) dt = \int (\kappa I_2) dt + \int (\kappa I_C) dt$$  \hspace{1cm} (4-14)

This equation would hold true for any moment of time as the difference in the current is satisfied by the capacitor, which could be seen in the figures later.

Now over a complete period of time:

$$\int I_C dt = 0$$  \hspace{1cm} (4-15)

Integrating the equation 4-3 and from the 4-3 we get:
Thus over a period of time, the steady state equation (4-2) holds true for the dynamic state. This is due to the fact that law of *conversation of charge* should exist, thus pricing done on the basis of charge, hence all the losses in the circuit can be counted for. Both the consumer and producer share the expenses for the the loss in transmission. At the instance of a increase or decrease in load, the grid operator acts as a buffer, the grid capacitor in combination with the converter capacitor fulfil the shortage/excess current in the grid. So overall from starting a grid to turning it off, complete charge is accounted for and the final price at consumer and produces end will be the same.

### 4-4 Realisation in DC Grid

#### 4-4-1 Transmission and Distribution Grid

Current pricing can be used to account for the line losses in transmission and distribution grids. The nominal price is in general unique in a subgrid and can be broadcast. If need be, congestion management could be done by setting differing nominal prices on both sides of overloaded lines. The power control is done indirectly by the prosumers and the grid operator earns a congestion rent.

Different grid levels can be connected by DC/DC converters shifting power from lower to higher price areas. As long as the conversion capacity is not fully utilised prices just differ by the conversion loss. Connections to AC systems with other pricing systems can be done similarly with voltage source converters. They could even stabilize the AC grid with reactive power.

#### 4-4-2 Households

At the prosumer side smart meters calculate the price from the local current values and the nominal price communicated separately. A DC/DC converter converts a preferably higher grid voltage to an internal voltage reflecting the determined price with linear price curve. From DC voltage alone, devices know the price and can react autonomously according to their importance. Energy storage could be connected internally for interruptible power supply, where the DC/DC converter disconnects the grid in case of fault and unimportant generation can be connected internally to increase reliability.

#### 4-4-3 Setup

A simulation framework has been built to verify the introduced concept. The generators and loads in the grid are represented by positive and negative current sources. The setup is shown in Figure 4-2. The source along with its capacitor form the source side converter, and the current value through it is $I_1$. The load along with its capacitor form the load side converter,
and the current value through it is $I_2$. The line between them is assumed to be a T-line, with the line capacitance is given by $C$ and the current through it is, $\pm I_C$.

Renewable energy sources have very low marginal costs and would always produce power, therefore they have to ramp down their power as the maximum voltage is approached. The maximum power is limited by given climatic conditions.

### 4-5 Simulation and Results

The simulations were carried out for the setup explained in the previous section. The following waveform and observations were observed:

The first Figure plotted 4-3 shows the source and load current in a dynamic situation. Initially the grid starts from zero, goes then rises towards the first set point ($S_1$) then stabilizes, after sometime the load goes to the next set point ($S_1$) then again it stabilizes, after sometime load goes back to the first set point and stabilizes, then the grid finally turns-off. At this point the current drops to zero. The source current follows the load current.

Even though the source and load current may seem exactly the same, that’s not the case in reality. In reality the inductor and capacitor resist the change in current and voltage, respectively. Hence there will be some delay in rise and fall of voltage and current value. Which is a very small percentage, but it adds up as the system size and operation time increases. Thus this difference in current is plotted against the the line capacitor current in Figure 4-4. According to the equation derived in the previous section both the plot should be identical. In the Figure they look exactly the same which was verified in simulation by displaying the real values.

The Figure plotted 4-5 shows the source and load voltage in a dynamic situation. Initially the grid starts from zero, goes then rises towards the first set point ($S_1$) then stabilizes, after sometime load goes to the next set point ($S_1$) then again it stabilizes, after sometime load
Difference between source current and load current.

Current through the line capacitor.

Figure 4-4: Current flowing into the Load is shown in the Figure; according to the convention load current is negative.

goes back to the first set point and stabilizes, then the grid finally turns-off. At this point the current drops to zero. The source voltage responds to that of the load voltage.

The Figure 4-6 shows the integrated current over the complete time, i.e. charge over the time period of the simulation. Since we are mostly concerned for the discrepancy between source and load current, hence the charge difference between them was plotted and the charge in the capacitor. They have exactly the same plot, as should be, more importantly the charge stored starts from zero and once the grid is switched off, the charge goes to zero again. Thus confirming the hypothesis of using current as medium for pricing.

Finally the electricity could be priced for current; i.e. X Euros for Y Coulombs of charge or X Euros for Y ampere-hour.
Figure 4-5: Current flowing into the Load is shown in the Figure; according to the convention load current is negative.

(a) Voltage across source.

(b) Voltage across load.

Figure 4-6: Current flowing into the Load is shown in the Figure; according to the convention load current is negative.

(a) Difference in charge between source and load.

(b) Charge in the line capacitor.
Chapter 5

DC Microgrid

In traditional electrical power systems, the dynamic operation of each source, distribution system, and load are all coupled together. The system stability must then be passively assured by imposing overwhelmingly slow dynamics of the sources: electro-mechanically anchored constant frequency of the rotating synchronous generators in AC systems or electro-chemically anchored constant voltage of the batteries or fuel cells in DC systems. Availability of energy to the loads is only ensured through redundancy, over-design, complicated networks, and electro-mechanical switchgear controlled system configuration and protection. These switchgear systems are inherently slow, inefficient, and unreliable [68]. Recently, due to a boom in power electronics industry, it is being employed in power systems and power electronic converters and have started to decouple the dynamic coupling between sources, distribution system, and loads. These systems have multiple levels, which include multiple primary and secondary energy sources, several levels of energy storage and back-up, and numerous active loads, all interfaced through electronic power converters [69, 70].

Thus, it could be envisioned that in future electronic power distribution systems (EPDS), the dynamics of electric energy generation, distribution, and delivery will be fully dynamically decoupled by using separate source converters, load converters, and power distribution converters. In the literature of [71], this approach has been explained with an anatomy of PC power management system. Instead of forcing all components inside a computer to use a single voltage supply (as was the case with 5V) most of the loads are now fed from a their own dedicated power supply with a voltage (e.g. 0.7, 1.8, 3.3, -8, 800 V) and dynamic behaviour, that enable optimum design of the respective loads, such as processor, memory, I/O, disks, display, etc. [71]. The energy is supplied by two different source converters: the adapter that interfaces to DC outlets in cars and air-planes, and the charger/discharger that assures optimum battery utilization. Although this may seem overly complex, but the benefits outweigh the drawbacks.

For the concept to flourish beyond small and autonomous power systems, future advancements in power electronics must go beyond components and converters themselves, addressing also the system-level integration of EPDS. Currently their is the lack of of standardized architectures and consistent system synthesis and integration methodologies, as well as the
insufficient understanding and inability to quantify complex interactions and trade-offs in these new power systems, this represents major barriers to the widespread usage of power electronics converters. Thus the Future research in systems integration in power electronics should be focused on the following aspects as per [71]:

- System architecture design and optimization;
- Energy balance control, and protection;
- System-oriented modelling of power converters.

5-0-1 Benefits

The aforementioned benefits that outweigh the drawback of this conceptual approach are:

- The overall energy consumption is reduced;
- The battery runtime and life time are increased, because of optimization based on battery SOC;
- The overall system weight and expense is fewer;
- And, all the protection provided in the system are consolidated, faster, and smaller without thermo-mechanical breakers or fuses. Proof can be seen in the hardware section.

5-1 Operating Point

In the previous chapter the equations for operating point of an individual converter were derived, while operating in a microgrid configuration, the operating point between source and load dictates the stable point of operation and theoretically can be derived. Each time the current in the grid changes a new stable operating point has to be achieved, which the converters achieve using iterative process of the controller. For deeper understanding of the grid interaction the theoretical approach had to be studied. To theoretically derive the stable point the control strategy has to be linear, where droop and constant current current are linear in nature, constant-power load is non-linear, hence had to be removed for this intent:

- \( i \): counter for the loads in droop.
- \( V_i \): reference voltage for sources in droop.
- \( n \): total number of loads in droop.
- \( j \): counter for the loads in constant power.
- \( P_j \): Constant power for constant power loads.
- \( m \): total number of loads in constant power.
• k: counter for the loads in current cap. A load switched off counts as a constant zero current load.

• l: total number of loads in current cap.

• \( V_s \): reference voltage for sources in droop.

• s: counter for sources in droop.

• p: total number of sources in droop.

• \( P_t \): Constant power for constant power sources.

• r: counter for sources in current cap.

• q: total number of sources in current cap.

• t: counter for the source in constant power.

• o: total number of sources in constant power.

The known parameters:

• Every \( I_k \)

• Every \( I_r \)

• Every \( R_i \)

• Every \( V_i \)

• Every \( P_j \)

• Every \( P_t \)

• \( V_s \)

• \( R_s \)

The unknown parameters:

• The final voltage \( V \).

• The final currents of sources and loads.

Equations involved:

• Droop characteristic of the sources

\[
V = V_s - R_s \times I_s \Rightarrow I_s = \frac{V}{R_s}
\]  

(5-1)
• Droop characteristic of the loads

\[ V = V_i - R_i \cdot I_i \Rightarrow I_i = \frac{V}{R_i} \quad (5-2) \]

• Constant power characteristic of sources

\[ V = \frac{P_t}{I_t} \Rightarrow I_t = \frac{P_t}{V} \quad (5-3) \]

• Constant power characteristic of loads

\[ V = \frac{P_j}{I_j} \Rightarrow I_j = \frac{P_j}{V} \quad (5-4) \]

• Constant current characteristic of sources

\[ I_r = I_{Source\text{max}} \quad (5-5) \]

• Constant current characteristic of loads

\[ I_k = I_{Load\text{max}} \quad (5-6) \]

By the law of power conservation:

\[ \sum_{s=1}^{p} I_s + \sum_{r=1}^{q} I_r + \sum_{t=1}^{o} I_t = \sum_{i=1}^{n} I_i + \sum_{j=1}^{m} I_j + \sum_{k=1}^{l} I_k \quad (5-7) \]

from the 5-1, 5-2, 5-3, 5-4, 5-5, and 5-6, we get:

\[ \left( \sum_{s=1}^{p} \frac{V}{R_s} - \sum_{s=1}^{p} \frac{V_i}{R_s} \right) + \left( \sum_{r=1}^{q} I_r \right) + \left( \sum_{t=1}^{o} \frac{P_t}{V} \right) = \left( \sum_{i=1}^{n} \frac{V}{R_i} - \sum_{i=1}^{n} \frac{V_i}{R_i} \right) + \left( \sum_{j=1}^{m} I_j \right) + \left( \sum_{k=1}^{l} I_k \right) + \left( \sum_{j=1}^{m} \frac{P_j}{V} \right) \quad (5-8) \]

Multiplying both the sides with V and rearranging the equation:

\[ V^2 \left( \sum_{s=1}^{p} \frac{1}{R_s} - \sum_{i=1}^{n} \frac{1}{R_i} \right) + V \left( \sum_{i=1}^{n} \frac{V_i}{R_i} + \sum_{r=1}^{q} I_r - \sum_{k=1}^{l} I_k - \sum_{s=1}^{p} \frac{V}{R_s} \right) + \left( \sum_{t=1}^{o} P_t - \sum_{j=1}^{m} P_j \right) \quad (5-9) \]

This gives a quadratic equation which can be solved for V using Sridhar Acharya formula.
\[ V = \frac{-B \pm \sqrt{B^2 - 4AC}}{2A} \]  

(5-10)

Where:

\[ A = \sum_{s=1}^{p} \frac{1}{R_s} - \sum_{i=1}^{n} \frac{1}{R_i} \]  

(5-11)

\[ B = \sum_{i=1}^{n} \frac{V_i}{R_i} + \sum_{r=1}^{q} I_r - \sum_{k=1}^{l} I_k - \sum_{s=1}^{p} \frac{V}{R_s} \]  

(5-12)

\[ C = \sum_{t=1}^{o} P_t - \sum_{j=1}^{m} P_j \]  

(5-13)

5-10 should be solved remembering that it must be comprehended between the minimum \( V_i \) and the maximum \( V_s \). Moreover, the current of the loads should not exceed the maximum current of the two sources. All the equations hold in steady state.

## 5-2 DC Microgrid Architecture

The architecture of the DCMG’s system, including the individual component’s voltage and current ratings, is a major determinant for the system structural and thermal feasibility, safety, availability, size, weight, power and energy efficiency, reliability, and ultimately the cost of energy utilization.

As earlier stated, integration of power electronics makes the system more complex, however, if judiciously used, power converters on the contrary can enable simplification of the design problem by separating the one-time complex system into a number of smaller, well-defined, and easily optimized subsystems.

The presence of distributed generation with its associated power electronic converter, which are not controlled by the electric power utility operator has provided fresh thinking about how the electric grid is built and operated, at least at the distribution level. The microgrid concept that comprises energy storage and a larger number of generating units in order to get the most from the naturally available renewable energy sources while minimizing architectural changes and operational disruptions of the existing power grid [72, 73].

## 5-3 DC Microgrid Setup

For various analysis purposes in DCMG, the setup had to be kept simple, and to save time on the computational time, simplified model for converters had to be used. The setup consists of two sources, a bidirectional infinite grid converter and a solar PV converter, and two generic load converters. For further simplification, all system wiring is represented with a single RLC circuit placed between the sources and the loads. The dynamic behaviour of the system is then analysed by using simplified models of the converters.
The grid interface is two-stage bidirectional converter: a single-phase full-bridge AC-DC PWM rectifier/inverter in series with a DC-DC PWM converter. Such converter can achieve bidirectional power flow control and DC-bus voltage regulation in addition to the substantial reduction of the DC-link capacitor for higher power density [74]. For the purposes of the simulation here, the grid interface converter is modelled in MATLAB using detailed average model, including input and output current, voltage control loops, and constant maximum power control. The selected parameters are:

- Max current = +1.65A
- Droop coefficient = 8
- Min current = -1.65A
- Maximum power = +500W
- Minimum power = -500W

The other representative source converter for the dynamic analysis is solar converter. It is a unidirectional two-stage converter comprising the front-end boost in series with a DC-DC buck
converter, which provides for good energy efficiency as well as excellent bus regulation and system protection. Average models are used for the analysis, including an MPPT controller in the boost stage, and the output current and voltage control in the buck stage to implement the static behaviour. The selected parameters are:

- Maximum current = +1.65A
- Minimum current = 0A
- Droop coefficient = 8
- Maximum power = +500W
- Minimum power = 0W

5-3-3 Load Converter Setup

The load converters are represented using simple average models of unidirectional buck converters with output current and voltage control. The load converter behaves like a constant power loads (CPLs) on the DC bus side. To simulate the load the, current is with negative amplitude value, due to general conventions. The selected parameters are:

- Maximum current = 0A
- Minimum current = -1.65A
- Droop coefficient = 8
- Maximum power = 0W
- Minimum power = -500W

5-4 Simulation and Result

The simulation were carried out in MATLAB’s Simulink, where the relevant system is shown in the figure 5-1. It consists of two sources, the bidirectional DC grid converter interface and the solar PV converter interface and two loads; with one of them at a higher priority then other. It is assumed that the loads rather than only being constant power loads, they can droop, so as to have a gradual and smooth charging of the grid. The dynamic behaviour of the systems is then analysed under different scenarios and then the grid voltage with the output currents are plotted against time.

The results after the simulation are as follows:
5-4-1 Scenario 1: General Conditions

In this scenario a general condition is considered to begin with, all the components are assumed to operate without any problems. The capacitor, inductor, and resistance are sized as realistic as possible (from real cable data-sheet and our own converter design parameter). In the Figure 5-4-1 the current and the voltage output of the simulation are plotted. The grid has a cold start from 0 volts, so initially both the sources contribute in pushing the grid to the nominal voltage level. Once a certain lower voltage level is achieved, the load with the highest priority starts operating, and so on. The PV initially is more than enough to maintain the grid voltage while the loads gradually increase. The remaining power is being fed to the grid, which initially contributed in black-starting the grid. Once the loads start operating at full potential the solar PV is overwhelmed and is unable to satisfy the loads, which results in drop of DC grid voltage. After a certain amount of grid voltage regulation, the bidirectional grid starts sharing the load. This occurs at around 5.7s. The solar PV operates at it’s full potential and at around 2.5s, it hits its maximum current rating, this is when the bidirectional grid starts to contribute by reducing its power intake, meanwhile the loads were operating unhindered without destabilizing the grid. All of this is achieved without any sort of communication.

5-4-2 Scenario 2: Sudden load Drop Out

This is a special scenario, where one of the load is abruptly tripped while in operation. This condition causes the DC grid voltage to spike thus leading to over voltage fault which trips all the sources and loads. In centralised control, the central controller would send the signal to switch or regulate some or all of the sources to stabilize the grid. In decentralized control the individual converters have to react to the over voltage. The control topology drawn is such that, their is always an operating point at any voltage level. In the figure 5-4-2, the DC grid voltage starts from zero and attains a stable grid voltage. At around 5s, the variable load 1 is disconnected, due to small capacitor value across the converter, the charge is discharged instantaneously, and the current falls to zero, this cause a spike in the DC grid voltage (5-4-2 b), meanwhile the other load demands continues to rise and operate without any fault.
sudden drop in load is being fulfilled by the bidirectional grid converter, which instantaneously carries the excess power to the grid and within a fraction of time the DC grid voltage stabilises to safe value. The second load remains unhindered from the over voltage.

5-4-3 Scenario 3: Sudden Source Drop Out

This is another special scenario, where one of the source is abruptly turned off while in operation. This could be due to cloud cover over the PV solar or any catastrophic fault at any of the source. This condition causes the DC grid voltage to dip abruptly thus leading to under voltage fault which trips all the sources and loads. In centralised control, the central controller would send the signal to switch some or all the loads for the voltage to stabilize. The idea is to achieve the same feat in decentralised control, thus the developed control topology is such that it provides an operating point for the converter at any voltage level. The Figure 5-4-3 shows the output simulation of this scenario. The grid starts from zero volts, and stabilizes at around 350 V. At around 5s solar PV drops out, the capacitor discharges instantly, and due to line inductance and discharged capacitor, some power is transferred to the solar PV converter’s capacitor to bring it to DC grid voltage. At the same time the grid changes from taking power to supplying power. The DC grid voltage dips beyond the stable point for low priority load, hence this load (Variable load 1) ramps down and eventually turns off. The system is starved of power, and a new stable point is achieved at a lower voltage value compared to previous stable point. The high priority loads keeps operating unhindered by this scenario, the grid is almost operating at the maximum current, and thus the stability is maintained.

This might not be the optimal solution, but compared to the trade-off of a centralised control, the results are very much acceptable. In various scenarios the grid stabilizes very quickly and maintains power balance. This system could very well be complimented by the dynamic pricing, which forms a higher level control utilising low-bandwidth communication for control.
5-5 Experimental Analysis

As of now the entire analysis for "Power balance control of DC microgrids" has been done on MATLAB simulation. As much detailed as the computational analysis is, it is no where close to real life analysis. Additionally to answer some of the research question, the control scheme was implemented on an off the shelf commercial power electronic converter. The results and the experience have been discussed here.

5-5-1 Setup

The experiment was performed on a setup developed by Ir Tsegay. It consists of two converters in parallel connection with a load. One converter is a pure source, which operates at constant power, this was used to emulate the solar PV, the other converter is a programmable bidirectional DC/DC-DC/AC converter, which emulated the bidirectional grid converter. The load was emulated by a variable resistor. The developed control scheme was programmed into the converter emulating the programmable bidirectional DC/DC-DC/AC grid interface converter. A power diode was used to eliminate the flow of power to the converter emulating the solar PV. For measurement the grid was probed to the oscilloscope. The grid voltage and the current dynamics from both the sources were plotted.

Process: The grid was black started from the grid converter, which brings the the DC link voltage to the nominal value. At this moment the entire load is supported by the grid converter, after a finite time the solar PV emulating converter was turned on to its minimum current value at the DC link voltage. Now both the sources start sharing the load, gradually the solar PV source current value is increased. This leads to reduction in the current sharing from the grid converter, at some point the grid current sharing drops to zero, this is where the entire load is supported by the solar PV converter. Upon further increasing the solar PV converter’s share, the current value exceeds the load current value, and the excess current is
Figure 5-5: The setup used in the lab. Where $S1$ is the programmable bidirectional power electronic converter in which the power balance controller was programmed, this acts as the grid converter; $S2$ is a constant power source, which acts as the solar PV converter interface power electronic converter; $load$ is a variable resistance, with two rheostats of $75\Omega$ in series; $M$ is the measurement, the one on the left is for voltage, the one on the right is for current; $O$ is the oscilloscope, for recording the measurements, $PC$ is the computer for programming the programmable converter.
fed back to the grid. The developed power balance controller scheme was programmed into the Grid converter.

5-5-2 Results

the figure5-6 shows the snap shot of the experiment’s waveform. The total range is for 10s, where the grid converter is turned on, starts supplying current from a finite value (green), after some finite amount of time Solar PV begins to conduct (Magenta) as it ramps up and increases its share of power the grid sharing is reduced autonomously. Once the solar PV overwhelms the load, grid starts taking power and becomes negative. the other two lines are the voltage between each of the probe,i.e the grid voltage is difference of voltage probe 1 and voltage probe 2. The measurements is plagued with oscillations, which were to be expected as the programmable converter has delay of 1ms. And the measurements were taken at less than adequate locations. Even then t could be said that the Power balance control algorithm work in real life scenario, albeit it is very difficult to implement in off the shelf converters and requires a faster controller. This prompted us to develop our own converter, which is focussed around the implementation of several novel control and protection techniques.

Further the measurements taken through oscilloscope were plotted in MATLAB, unhindered in figure 5-5-2 and 5-8.
Figure 5-7: Voltage and current plot against time.

Figure 5-8 shows the voltage vs current waveform for the experimented setup, for the simplicity of understanding, the steady state waveform for the same parameter has been overlayed. It can be deduced, that the experimental setup follows the steady state waveform from Power balance controller. But the measurement is plagued with oscillations, which was even seen in the measurement equipments. Using external measurement is another adding factor to inaccuracy, but the converter only transmits one measurement at a time, i.e either voltage or current. The oscillations are most likely caused due to converters own delay in measurement transmission, which is around 1ms.
Figure 5-8: The Voltage versus Current plot for the experiment and steady state.
Chapter 6

Hardware

In this part of this MSc thesis the procedure that was followed to design and construct a non-inverting buck-boost converter will be presented. This is done based on design and concept from Laurens Mackay which was verified and simulated by Ir Emanuele Marafante [45]. The final use of the non-inverting buck-boost converters that has been designed is to act as the DC/DC interface between loads/sources and grid of a DC microgrid that will be constructed in the lab for simulation and testing of various topics, among which Fancy controller, current pricing that has been discussed in previous chapters of this Master Thesis.

Apart from the non-inverting buck-boost converter, a Dual Active Bridge (DAB)(emulating load/source) and communication module will also be designed, which will be responsible for the centralized control of the converters. In other words, it will act as the master of the entire system.

6-1 Non-Inverting Buck-Boost Converter

This converter, described in [46] and depicted in Figure 1-13, is made up by a quasi-series of buck and boost converters: they can be considered to be cascaded, but they share the passive components of the L-C filter. There are one more diode and two switches. The switches of this converter can act almost independently, with a single condition to be met: the buck switch should be always on when the boost switch is. This avoids the appearance of a low-impedance current loop within the converter [47].

Although this configuration increases the switches utilization in both modes, more components are needed and their losses should be taken into account; as an example, in the buck mode there will always be an extra diode on the path. This converter is granted to work linearly at least for \( v_o \leq 2v_i \) [46].

Filter

In signal processing, a filter is a device or process that removes from a signal some unwanted component or feature. Filtering is a class of signal processing, the defining feature of filters
being the complete or partial suppression of some aspect of the signal. Most often, this means removing some frequencies and not others in order to suppress interfering signals and reduce background noise. Filters could be classified on different bases, which include; linear or non-linear, time-invariant or time-variant, causal or not-causal, analog or digital, discrete-time (sampled) or continuous-time, and many other. The one used in our application is a Linear-continuous-time variant low-pass filter.

**Low-pass Filter**

A low-pass filter is a filter that passes signals with a frequency lower than a certain cutoff frequency \( f_c \) and attenuates signals with frequencies higher than the cutoff frequency \( f_c \). The amount of attenuation for each frequency depends on the filter design. There are many different types of filter circuits, with different responses to changing frequency. The frequency response of a filter is generally represented using a Bode plot, and the filter is characterized by its cutoff frequency. In all cases, at the cutoff frequency, the filter attenuates the input power by half or 3 dB. So the order of the filter determines the amount of additional attenuation for frequencies higher than the cutoff frequency.

- **First-order filter:** Reduces the signal amplitude by half (so power reduces by a factor of 4, or 6 dB), every time the frequency doubles (goes up one octave); more precisely, the power rolloff approaches 20 dB per decade in the limit of high frequency. Example R-C filter, R-L filter

- **Second-order filter:** the Bode plot for this type of filter resembles that of a first-order filter, except that it falls off more quickly. Every time the frequency doubles (goes up one octave); more precisely, the power rolloff approaches 40 dB per decade in the limit of high frequency. Example: RLC-filter.
LC-filter

An LC circuit, also called a resonant circuit, tank circuit, or tuned circuit, is an electric circuit consisting of an inductor, connected together with capacitor. The circuit can act as an electrical resonator, an electrical analogue of a tuning fork, storing energy oscillating at the circuit’s resonant frequency. Generally used as low-pass filter and as resonant tanks in resonant converter for zero power switching. The cut-off frequency is given as:

\[ f_c = \frac{1}{2\pi\sqrt{LC}} \] (6-1)

For the voltage ripple to be minimized, the cutoff frequency \( f_c \) of the low-pass filter has to be much less than the switching frequency \( f_s \), \( f_c \ll f_s \). Thus the inductor and capacitor has to be sized accordingly for the condition to be satisfied. From the previous equation we know that the inductor and capacitor value has to be sized accordingly so as to absorb the excess energy in case of a fault, which is mostly peak current at short circuit and peak voltage at over voltage. The fault trip time determines the net rise in the current value, hence keeping all this into account the inductor and capacitor were designed and the procedure is discussed in the following sections.

6-1-1 Inductor and sizing

An inductor, coil or reactor, resists changes in electric current passing through it. When current flows through an inductor, energy is stored temporarily in magnetic field in the coil. When the current flowing through an inductor changes, the time-varying magnetic field induces a voltage in the conductor, according to Faraday’s law of electromagnetic induction, According to Lenz’s law the direction of induced e.m.f is always such that it opposes the change in current that created it. As a result, inductors always oppose a change in current.

Design calculation for Buck-Boost converter’s inductor and capacitor can be from [75] A converter generally has two mode of operation, namely DCM and CCM between them is the boundary condition, for which the inductance value is such that, anything greater gives CCM and anything lower gives DCM [44]. Thus the equations are such that the maximum inductance current is given at \( D=0 \):

\[ I_{L,\text{max}} = \frac{T_s V_o}{2L} \] (6-2)

with the parameters \( I_{L,\text{max}} = 5\text{A}, T_s = 10\mu\text{s}, V_o = 100\text{V} \) we get the inductance value as, \( L = 100\mu\text{H} \)

The inductance of this small value is of reasonable small size for the PCB and is readily available in the market. Now the solid state protection, which will be elaborated in the following section has a trip time of under 200\(\eta\)s, which is extremely fast and gives an inductance value of \( L = 2\mu\text{H} \). But for reliability and redundancy purpose, inductance value of \( L = 100\mu\text{H} \) was chosen.
6-1-2 Capacitor and sizing

A capacitor (originally known as a condenser) is an electrical component used to store electrical energy temporarily in an electric field. Capacitor is made up of two electrical conductors (plates) separated by a dielectric (i.e. an insulator that can store energy by becoming polarized). A capacitor stores energy in the form of an electrostatic field between its plates. When there is a potential difference across the conductors, an electric field develops across the dielectric, causing positive charge +Q to collect on one plate and negative charge -Q to collect on the other plate. Capacitors are widely used in electronic circuits for blocking direct current while allowing alternating current to pass. In analog filter networks, they smooth the output of power supplies. In resonant circuits they tune radios to particular frequencies. In electric power transmission systems, they stabilize voltage and power flow [76]

The Capacitor ideally should be as large as possible, which improves the stability but also the bulk of the converter, but a realistic trade-off was carried off and thus a capacitance of 30µC was chosen [75].

For the filter cutoff frequency we get a value of 3kHz.

6-2 PCB Layout

The entire PCB has three different isolated zones, one for the power electronics and its periphery, one as common ground for all the PCB to be connected, and the last one for USB-JTAG necessary for flashing the micro-controller (MCU). For data transfer between the isolated zones, opto-couplers are implemented. All the measurement, protection, driving circuit are present on the power electronic side, along with MCU, power switches, and various logical circuits necessary for proof of concept experimentation. The common side has been chosen for powering the whole PCB and providing interface with DAB, and communication module.

In Figure 6-2 a general overview of how different zones and components are placed in the PCB. The Figure below only serves as a compact view of different isolated zones. The individual layers and their tracing are available in the Figure below.

Individual components used in the PCB are explained in detail below:

6-2-1 Power Supplies

The power supplies of the integrated circuits used in the non-inverting buck-boost PCB are designed in such a way that they will be powered from the control and communication module, which will have a 12V DC power supply directly from a separate power supply module. Using the appropriate integrated circuit modules converter, the 12V power supply is converted to ±15V, 5V, and ±3.3V, which are the necessary voltage levels required to drive the plethora of integrated circuits used in the PCB.
Figure 6-2: PCB Diagram.
Figure 6-3: Exploded view of the PCB, with individual relevant layers
6-2-2 Measurement Circuits

The measurement circuit is based on combination of op-amp logics [77] and voltage division, and shunt resistor. The fundamental logic is to take a small proportion of the real value and feed it into the op-amp circuit, which either shifts the value or adds gain to match the actual current/voltage value. This is either pushed to a logical Integrated Circuits (IC), Micro-controller (MCU), or both for further processing. General measurement circuit could be obtained from [78], and further sophisticated current measurements circuits could be analysed from [79].

Bidirectional Low-Side Current Measurement

For the current measurement, a simple shunt resistor based measurement is chosen, it is inexpensive and accurate enough to fulfill the needs in our purpose. The principle is based on use of op-amps. Its main disadvantage is that it adds a small, but undesirable resistance to the ground path, the shunt resistance [80]. The shunt resistance value is chosen to be as small as possible, without the resulted voltage dropping below the minimum offset voltage of the operational amplifier. The voltage drop across the shunt resistor is shifted up by 1.65V (half of 3.3V, which is the maximum for MCU, so that 1.65V correspond to zero current) then fed to an op-amp. The op-amp is powered by 3.3V and by appropriately setting the resistances appropriate gain is achieved. The first op-amp circuit of the current measurement circuit is a differential amplifier and the second op-amp provides the gain. This is better illustrated in Figure 6-4. Its output voltage is calculated with the following equation:

\[ V_{out} = \frac{R_1 + R_f}{R_1} \frac{R_g}{R_g + R_2} V_2 - \frac{R_f}{R_1} V_1 \]  

(6-3)

If \( R_1 = R_2 \) and \( R_f = R_g \), then this equations can be simplified to:

\[ V_{out} = \frac{R_f}{R_1} (V_2 - V_1) \]  

(6-4)

After this the voltage is fed to the second op-amp for amplification with a particular gain value, the output of which is sent to an ADC (Analog to Digital) port of the MCU.
\[ V_{\text{out}} = -R_f \left( \frac{V_1}{R_1} + \frac{V_2}{R_2} + \ldots + \frac{V_n}{R_n} \right) \]  

(6-5)

If \( R_1 = R_2 = \ldots = R_n = R_f \) this equations can be simplified to:

\[ V_{\text{out}} = -(V_1 + V_2 + \ldots + V_n) \]  

(6-6)

This means that an output voltage higher than 1.65V corresponds to a positive current, while an output voltage lower than 1.65V corresponds to a negative current. The current measurement circuitry and the actual values of the resistors and capacitors are schematically represented in Figure 6-6.

**Voltage Measurements**

The voltage measurement circuit is very straightforward, it uses the differential op-amp configuration to compare the measured voltage ratio with a set voltage value. Both these voltage are stepped down value with same voltage divider ratio [6]. The circuit that was used for the voltage measurements is presented in Figure 6-7.

In addition to the circuit in Figure 6-7, for the voltage measurement of the secondary side, an additional module that provided voltage isolation was added.

**6-2-3 Buffer and R/S Latch for Tripping the Switches**

After an overcurrent fault is detected from the comparator described in 6-2-6, the switches have to be tripped so as to protect the switches in the Buck-boost Printed Circuit Board (PCB) remains unharmed. This is achieved using a latch circuit, namely with the use of a
Figure 6-7: Differential op-amp circuit for voltage measurement, from [4].

R/S latch and a buffer. It’s the comparator’s job to provide the trip signal, but due to being continuous is nature, the comparator can not hold the trip; as it will go to low as soon as the circuit is tripped, which will cause another fault and another trip, thus leading to an infinite loop. Thus the output of the comparator circuit is fed to a R/S latch integrated circuit, which produces and holds a high output, when a high input is fed to its set pin, only way to set it low is through reset pin. The the trip signal from latch could keep the switch off, until a reset high is provided by the MCU. This provided complete control over the switches, and they can be turned on once the fault is cleared.

The circuit diagram of a R/S latch is presented in Figure 6-8. In more detail, a R/S latch operates as follows. When high signal is applied to the set pin (S) its output (Q) goes to high and remains high, even if the input (S) goes to low. Only a high input on the reset pin (R) can drive the output (Q) to low. If both (S) and (R) are at low, the output (Q) latches, meaning that it maintains its previous state. A problem occurs when both (S) and (R) are at high at the same moment since, the output (Q) takes the value of the pin that is set initially. This situation has to be avoided. The enable pin serves as a condition for latch, when it can or cannot latch. When the enable input is low (Q) remains latched to the previous data. Only when the enable input is high can the state of the latch change. In Table 6-1 the characteristic table of an R/S latch is summarized.

An active-low 3-state buffer [82] is used for tripping of the pulses from the MCU. In such a buffer when a low input is applied to its enable control pin, then data can flow from its input to its output. When the enable pin is high, the buffer output is disabled and a high impedance condition Z, is present at the output. These information are summarized in Figure 6-9 and Table 6-2.

The combination of the comparator, the R/S latch and the buffer allows for the switches to turn-off when a problem is detected. It is important to notice that the fact the R/S latch has to be physically reset through its (R) pin, by driving it high, if the switches are to be turned-on again. This feature of the R/S latch provides an extra layer of safety [82].
Table 6-1: Operation of R/S Latch

<table>
<thead>
<tr>
<th>E</th>
<th>S</th>
<th>R</th>
<th>Q</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>Latch</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>1</td>
<td>Latch</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>0</td>
<td>Latch</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>1</td>
<td>Latch</td>
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<tr>
<td>1</td>
<td>0</td>
<td>0</td>
<td>Latch</td>
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<tr>
<td>1</td>
<td>0</td>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>1</td>
<td>X</td>
</tr>
</tbody>
</table>

Table 6-2: Operation of Active Low 3-State Buffer

<table>
<thead>
<tr>
<th>Enable</th>
<th>A</th>
<th>Y</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>Z</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>Z</td>
</tr>
</tbody>
</table>

6-2-4 Power Switches

The MOSFET switches and their respective drivers were selected for their optimum performance capability. The switches selected have an on drain to source resistance of 45m$\Omega$ which is second least in its class. Other advantages include low gate charge $Q_g$, reduced energy stored in output capacitance ($E_{oss}$), low switching losses, increased power density are few to name [83]. The driver [84] avails fast switching which in our case is 100KHz, with high and low side driving capability in the same chip, by bootstrap diode. Due to the target of maximum flexibility in terms of switching, charge pump circuit rather than bootstrap is used, Thus high side could be switched without switching the low side.

6-2-5 USB type C and JTAG Boot

The choice to boot the MCU from a USB device was also implemented in the Buck-Boost converter PCB, in the exact same way that it is done in the LAUNCHXL-F28069 C2000 Piccolo LaunchPad. This increased the size of the PCB by a small factor, but provided more choices for booting and powering the MCU, while also making it easier to flash program the MCU with the use of the Universal Serial Bus (USB) port. The USB port used is the new USB-C, first of its kind to be implemented in such an application. USB-C provides the ease of reversible cable plugin, with option of high power transfer, upto 100W and high speed USB3.0 (5GbPS) or USB3.1 (10GbPS) data transfer. This new connector ensures endless future expandability option. The versatility USB-C causes other issues, since it can be used for HDMI, Thunderbolt, Displayport, USB, and power connector, special arrangement has
to be employed for it to select the operation of USB 2.0 (this is only one supported by the JTAG). Typically, a pull-up resistor in the device is used to detect the presence or absence of an ID connection [85]. The USB host is required to have Pull-Up resistors (Rp) on CC1 and CC2. The USB Type-C specification allows Rp to be implemented as current source and voltage clamp. Actual function is the same.

The host identifies a device is connected by detecting one of the device Pull-Down resistors. Both host and device can determine the cable orientation, as only one of the CC pins is wired in the cable [2].

![Figure 6-10: Pull-up CC model for connection and orientation- [2].](image)

### 6-2-6 Indication LEDs

LEDs are placed on the PCB to indicate when a predefined event has occurred, for instance over-current, over-voltage, MCU operation status, flashing, etc. For the indication to occur the event has to happen, thus the measurement circuits measure the relevant parameters. Once the event has occurred, this information is relayed to the MCU, which in turn sets the particular Light Emitting Diode (LED) to high. The state of this LED remains high until the issue is resolved or the converter is turned off. This serves as the first layer of diagnostics for the user.

### 6-2-7 Overview of the Components of the PCB

In Table 6-3 the components selected for the PCB are presented. The operational amplifiers selected are dual, minimizing their total footprint on the PCB. The buffer selected are not inverting. The LAUNCHXL-F28027 C2000 Piccolo launchpad was replaced by TI-F28069 MCU and some of the launchpad’s features were also added on the PCB.
6-3 Charge-Pump

Charge pumps are for driving a high-side gate drive power supply that features high voltage capabilities for switching a power switch. The transformer less topology uses a small capacitor to transfer energy to the high-side switch from a single power supply referred to the negative rail. Unlike conventional bootstrap power supplies, no switching of the main phase-leg switches is required to provide power continuously to the high-side gate drive, even if the high-side switch is permanently on.

![Charge pump schematic](image)

Figure 6-11: Charge pump schematic.

Bootstrap circuits are widely used in bridge inverters to provide the floating power supply for high-side switch gate drives [86]. They are often preferred over high-frequency transformer circuits due to their simplicity and basic compatibility with integrated circuit implementation, making them well suited for achieving low cost and high reliability. However, the bootstrap technique imposes significant limitations due to its periodic charging time requirements that can interfere with the desired gate drive operation under some important operating conditions [1 of charge pump]. In particular, the high-side gate drive can become starved of energy if the inverter switching algorithm calls for either switch to be on for long intervals. Under such circumstances, the main phase-leg switch may be forced to perform a brief switching cycle in order to refresh the depleted capacitor charge for the high-side gate drive [87].

In our application we would like to have the freedom of switching high-side gate drive without interfering with the desired phase-leg switching sequence, thus the use of charge pump.
6-3-1 Operating Principles

Operation could be divided into three different modes which could be seen in Figure 6-12:

- Charging mode: The boost capacitor $CL$ in Figure 1 is charged by the single low-side power supply $VCC$ through $D1$ and $D2$ when the switch turns on as shown in Figure 2. $S2$ and $D2$ remain in their off-states since the gate $VGS2$ source voltage $VD3$ is forced to during this charging mode. $D1$, $D2$, $S1$, and $S2$ must all be high voltage devices rated at the DC link voltage $VDC$.

- Boost mode: When $S1$ turns off, the voltage $VL$ on the boost capacitor $CL$ starts to charge the gate capacitance of $S2$, $CGate$ through $R3$. Assuming that $CL$ is much bigger than $CGate$, the decrease in the $CL$ voltage is negligible. The value of $R3$ determines the turn-on time of $S2$, but does not affect the magnitude of the final $S2$ gate voltage. Once $CGate$ is charged, there is no additional current flow or loss in $R3$. The voltage at the negative (lower) terminal of $CL$ rises from ground level to $VDC$ (the output node voltage) as switch $S1$ turns off and the drain-source voltage of $S2$ decreases.

- Pumping mode: After $S2$ fully turns on, the charge in the boost capacitor $CL$ is transferred to the high-side capacitor $CH$ that serves as the local supply for the high-side switch gate. This pumping mode ends when $S1$ is turned on again by the external control. Continuous switching of $S1$ insures that gate drive charge is available at all times to the high-side switch without any interference with the desired phase-leg switching sequence.

6-3-2 Simulation and Results

The schematic was simulated in SPICE software with the models of the real switches with realistic parameters. The output waveform can be seen in the Figure 6-11:

The Figure 6-13 shows the output voltage of the charge pump, it charges up from 400V to 412V in 1ms. The charging time depends on the combination of resistances and capacitances. The output voltage fluctuates from 411.5V to 410.5, which is well above the minimum $VGS$ to gate the Power MOSFET.

The Figure 6-14 shows the output current of the charge pump. The current through the MOSFET switch of charge pump has to be under the safe limit in order to sustain prolonged operation of the switch. By regulating the resistance values in the circuit the continuous and pulsed drain current are kept well under the maximum permissible limit. In the end the maximum pulsed current value is 21mA and continuous drain current is 5mA.

6-4 Inrush-Current limiting

*Developed by Ir. Emanuele Marafante.*

DC components are plagued with high starting currents, due to capacitacnes present between the power lines and in the converters. One of the goal of MSc thesis for Ir. Emanuele Marafante was to develop a hardware architecture to address the issue [45].
Figure 6-12: Three different modes of operating principle of charge pump.
6-4 Inrush-Current limiting

DC components and power lines/buses are characterised by the need for passive components that prevent the voltage level from abrupt changes. Voltage-source converters bear input capacitors for their own characteristic, while in general L-C filters are used to turn the on-off behaviour of the switches into a smooth output signal. Since larger capacitors can handle wider fluctuations in voltage, the control of the steady-state operation will be made much easier.

The drawback of such a setting is given by the behaviour of the system as it starts: if uncontrolled, large capacitive currents are pulled into the circuit according to equation 6-7.

\[ i = C \frac{\partial v}{\partial t} \]  

(6-7)

The application of a step voltage to a converter or DC bus theoretically results into infinite current, which in practice is limited by the external circuit, its stray resistances, and its stray inductances.

What happens is that a system, sized for certain maximum current value, ends up experiencing another value which is much larger, albeit for very short time. This leads to premature ageing and failure of the Component. Moreover, the current could be as large as to cause the tripping of short circuit protection devices.

When the equipment had to withstand a much higher power, this problem had to be somehow faced. Various solutions have been found in literature, and the ones used the most are reported.

Figure 6-13: Charge Pump SPICE simulation results. The plot shows the output voltage waveform of the charge pump.

6-4-1 Inrush current limiting in DC equipment

DC components and power lines/buses are characterised by the need for passive components that prevent the voltage level from abrupt changes. Voltage-source converters bear input capacitors for their own characteristic, while in general L-C filters are used to turn the on-off behaviour of the switches into a smooth output signal. Since larger capacitors can handle wider fluctuations in voltage, the control of the steady-state operation will be made much easier.

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(6-7)

The application of a step voltage to a converter or DC bus theoretically results into infinite current, which in practice is limited by the external circuit, its stray resistances, and its stray inductances.

What happens is that a system, sized for certain maximum current value, ends up experiencing another value which is much larger, albeit for very short time. This leads to premature ageing and failure of the Component. Moreover, the current could be as large as to cause the tripping of short circuit protection devices.

When the equipment had to withstand a much higher power, this problem had to be somehow faced. Various solutions have been found in literature, and the ones used the most are reported.
Figure 6-14: Charge Pump SPICE simulation results. The plot shows the current through the switch of charge pump.

in the MSc thesis of Ir Emanuele Marafante. These solutions can also be applied to AC-DC converters (rectifiers): if their output capacitor had to be charged, high inrush current can be experienced especially if the input voltage is around its crest ($\sqrt{2}V_{LL}$) [44].

6-4-2 Simulation and Results

The simulated setup, built in the lab, is depicted in Figure 6-29. The PCB with the two OpAmps (OPA2350 and LM833) and the MOSFET (C7CoolMOS) was directly connected to a power supply giving $V_i = 15$ V. The same power supply had the possibility of limiting the current to a designated value; this feature was taken as safety measure. The PCB also bore the contacts for the connection of the OpAmps alimentation ($\pm 15$ V for the LM833 and +3.3 V for the OPA2350), and a cable for the application of the Pulse Width Modulation (PWM) signal from the microcontroller.

6-5 Over-current Protection

The system under study is depicted in Figure

DC voltage is connected to a constant resistance load ($R_{load}$) via a 100 $\mu$H inductance. The current flowing through 0.01 $\Omega$ resistance $R_{cm}$ is to be measured using a difference op-amp of appropriate gain in order to have appropriate over-current protection. When a ground fault occurs at the load side, the short circuit current present in the circuit must be disconnected.
Figure 6-15: Op Amp-based inrush current limiter circuit schematic.

(a) Complete setup used to simulate the inrush current limiter
(b) Particular of the PCB bearing the inrush current limiter circuit. The C2000 microcontroller is also visible.

Figure 6-16: Hardware realization of the OpAmp based inrush current limiter.
Figure 6-17: Measured $v_f$ as function of $\delta$. The circles’ blue line represents the measurements, the red one the plot of the approximation function developed. The yellow line reproposes the results of the simulation.

Figure 6-18: Measured $i_{DS}$ as function of $\delta$. The circles’ blue line represents the measurements, the red one the plot of the approximation function developed. The yellow line reproposes the results of the simulation.
Figure 6-19: $P_{\text{Loss},\text{MOS}}$ as function of $\delta$. The circles’ blue line represents the measurements, the red one the plot of the approximation function developed. The yellow line reproposes the results of the simulation.

Figure 6-20: Measured $G_i$ as function of $\delta$. The circles’ blue line represents the measurements, the red one the plot of the approximation function developed. The yellow line reproposes the results of the simulation.
Figure 6-21: Proportionality between $v_f$ (yellow) and $i_{DS}$ (cyan): the two quantities follow the same pattern, albeit it should be noted how the scale is different and so it is the origin line. To generate this pattern, $\delta$ has been varied from 0.05 to 1.00 in steps of 0.05, every 10 ms.

Figure 6-22: Equivalent Circuit of System

using a solid state switch $S_{on}$, which is normally closed. For this purpose a faster response than over-current protection is required (which needs to be coordinated accordingly with the protection scheme). Simultaneously, the switch $S_{off}$ is switched on to ensure the discharge of inductor current [3].
6-5-1 Circuit Schematic

The LTSpice schematic prepared along these lines is shown in Figure 2.2. All variable values are indicated. M1 and M2 are the MOSFET IPB65R045C7 used as switches $S_{off}$ and $S_{on}$ respectively. The gates of these switches are controlled according to the protection scheme wherein M1 remains open and M2 closed in normal operation and the flip states as soon as the protection circuit sends a trigger signal. Switch S1 simulates a short circuit in the load side at 5 $\mu$s.

![Schematic Diagram]

Figure 6-23: LTSpice schematic of the system from [3].

6-5-2 Protection Scheme

The voltage across inductor is measured using V3 and V2 and feeding it into a difference op-amp of type OPA350 via a 550/3.3 V voltage divider built using 50 k$\Omega$ and 330 $\Omega$ resistances in series. This is the part of the short circuit protection scheme as shown in Figure 6-23. Output of Opamp U1 is fed into the comparator (TLV3501) U4 which gives high signal when input is greater than reference voltage of 1.5 V indicating a high voltage drop across the inductor. The response time for this comparator is 4.5 ns. The output of comparator is then fed into the SR latch A1 which then triggers the MOSFET switches to flip their normal states.

6-5-3 Simulation and Results

Figure 6-25 shows the behaviour of the system during short circuit without any protection and Figure 6-26 shows the behaviour when protection scheme is in place. As observed, The protection scheme is able detect the fault in 77 ns. The step size used is 1 ns.
Figure 6-24: Schematic for fast short circuit protection scheme, from [3].

Figure 6-25: Short circuit behaviour without protection in place, from [3].

Figure 6-27 shows the corresponding signals of the Opamp, comparator and SR latch of the protection scheme. By reducing the reference voltage value, the protection speed can be increased, however this must be done after ascertaining the voltage swing across the inductor expected during normal operation.

It is also of consequence to decide the variation in detection time based on the inductance value across which the voltages are measured. With greater inductance, the time constant $L/R$ will increase thereby increasing the trigger time taken to reach the set reference voltage of the comparator. $R$ is very low here due to a short circuit so this increase may have marginal
impact. Further, with larger inductance, the increase in current will be slower. It is hence, these varying conditions that should be looked into while determining the reference voltage for the protection scheme.
6-6 Circuit Combining, Current Limiting and Protection

The converter designed, is a bidirectional DC-DC converter which dictates it having several protection scheme in both the direction. The hardware is being designed for research purpose and the ease of implementation of above mentioned features. Which include black starting the grid with inrush current limiting, but should protect the converter in case of over-current. This could very well be done by MCU, which is rather slow, thus a logical circuit was devised and Experimentally proven to switch between inrush current limiting and over-current protection.

The system is shown in the Figure 6-27:

6-6-1 Circuit Schematic

The Figure 6-28 below shows the schematic of the circuit for the logical selector.

The MOSFET used is a high voltage low current switch and the transistor is a NPN Bi-Junction transistor (BJT). The MOSFET is connected in series with the inrush-current limiting circuit which drives the main power MOSFET. The BJT is in series connection with over-current protection circuit and then this arrangement is in parallel connection with the MOSFET and inrush connection. The driving voltage for the Inrush current limiting comparator is reduced than that of the over-current protection using two diodes in series.
6-6 Circuit Combining, Current Limiting and Protection

(a) Under normal operation, with in rush current limiting.

(b) Under fault, with active over current protection.

Figure 6-29: Two different stages of operation of logical selector. Red line indicates open circuit region, black line indicates closed circuit region

Low current MOSFET is there to drive the main Power MOSFET and BJT is there to drain the gate capacitance of Power MOSFET.

6-6-2 Operating Principle

Over-current Protection in combination with BJT is there to trip the main Power MOSFET under over-current fault. The over-current protection has higher priority over the inrush current limiting in terms of driving. When the over-current protection gives a high, i.e the their is no over current detected; low current MOSFET is turned on, thus gating the main power MOSFET(CoolMOS C7). At this instance the base and emitter of the BJT are at the same potential thus the BJT stays off. The gate of the low current MOSFET is at the potential as that of base of BJT, this where the two diodes come into play, they make sure the potential at the source is lower than that of the gate of the low current MOSFET.

When the over-current protection gives a low, i.e the their is over current detected; Base-Emitter of the BJT is positively biased, which starts conducting. This removes the gate signal from the low current MOSFET, which in-turn removes the gate signal from Power MOSFET (CoolMOS C7); thus tripping the switch. The Power MOSFET gate capacitor has enough charge left to sustain conduction for longer period. The BJT drains the gate capacitor to ground, thus eliminating any chance of false switching.

6-6-3 Simulation and Results

The Figure below shows the output voltage and current waveform for various switches present in the logical selector.

In the Figure 6-30 (a) shows gate voltage to the the main power MOSFET (CoolMOS C7)at 0.5 ms the gate signal is removed and the gate voltage drops to 7V, but at 7V the MOSFET can maintain power flow, this voltage is present due gate capacitance. The charge stored in the gate capacitor is discharged to the ground using the BJT circuit. In Figure6-30 (b)
Figure 6-30: Voltage and current curves at gate and base terminals.
shows the flow of current through the Power MOSFET, during the gated period, current is positive, after the removal of gate, current becomes negative, but due to gate capacitance the MOSFET starts to change current to a positive value, this is where the BJT starts to conduct and the current value increases in the negative side, until the entire charge is dissipated to ground. And the power MOSFET is completely turned off and ready to be fired again.

In the Figure 6-30 (c) and (d) shows voltage across Base-Emitter and current through the BJT. Initially when the Power MOSFET is conducting, base-emitter voltage in BJT is zero. When the Power MOSFET is tripped, the voltage across base-emitter in BJT becomes positive and higher than the minimum $V_{BE}$, due to the power diodes between the the comparator and the power supply. The BJT starts conducting and the entire gate capacitance’s charge of Power MOSFET is discharged to the ground, thus maintaining the $V_{GS}$ of the power MOSFET to zero. Once the OCP gives a high (high is equal to no fault), the $V_{BE}$ gets zero and the main power MOSFET starts conducting.

This helps in attaining two safety features through one switch. The propagation delay for the tripping circuit is well below our target of 200ns, which enables for reduction in size of the components and faster recovery time.

6-7 Protection Scheme Explained

In the above sections, individual parts and features of the hardware are explained. In this section all the parts will be combined and elaborated. For the ease of understanding a comprehensive schematic is presented in the Figure 6-31

To start with we have the power electronic side, which comprises of all the power switches for the Buck-Boost arrangement, inrush current limiting switch, over-current protection switch, discharge circuits, inductors, capacitors, and the power connectors. The power switches are arranged as per the schematic. The discharge circuits are simple dissipative circuits, controlled by MOSFET, once triggered the charges stored in the capacitor and inductor are drained to the ground while being dissipated through the resistances.

Next we have the measurements, which tap into points of power electronics regions which needs to be measured. For voltage, their is a voltage divider, which steps down the voltage to a level that is safe for the integrated circuits. For current measurement, a resistive shunt method is used, the voltage drop across the shunt gives a voltage value relative to the real current, based on Ohms law. This voltage is directly fed to the amplifier, but the current value has to be pushed by 1.65V (half of the full voltage range) so as to accommodate bidirectional measurement, such that 0V = negative maximum current ($I_{\text{min}}$), 1.65V = 0 current, and 3.3V = positive maximum current ($I_{\text{max}}$). The amplified values are then fed into the microcontroller for further processing and for flexible protection regimes.

The protection and its logic is quite sophisticated, so to understand it, lets start from the very beginning. One switch is dedicated for inrush current limiting, another one for combination of over-current protection and inrush current limiting. All the integrated converter power switches will open if protection is tripped. The protection is enabled using the local measurement explained above. The short circuit protection and the over current protection
converge at the R/S latch, this where the common protection logic begins. The short circuit protection; the positive and negative voltage divider value at the two ends of the inductor is fed into an op-amp, OP-Amp 1, which is in differential mode of operation. The output is fed into a comparator, COMP 1. The differential output is compared, COMP 2 to a filtered adjustable value (filtered through an amplifier, Op-Amp 2) from the microcontroller, which is fed into the first port of R/S latch, Quad R/S latch. The comparator is dual input, COMP Pac 1 hence the current flowing through the Over Current Protection (OCP) switch is fed into second input of the comparator COMP 2, which is compared with a reference value generated by a voltage divider. The output is fed into second port of the R/S latch Quad R/S latch. The former protection is to protect the circuit from short circuit in the grid, and the latter is to protect the grid from the short circuit in the load side of the converter. The over current protection; The bidirectional current through the integrated switches is compared, COMP Pac 2 against the references for either direction of flow of current (COMP 3 for negative current and COMP 4 for positive current ). The compared outputs are fed into OR gate (OR 1), the output of which goes to the fourth port of R/S latch, Quad R/S latch. The R/S latch is a quad R/S chip, hence one port, Port 3 is given an input through the microcontroller, just to have an additional degree of control. The output of R/S latch port 1, 2, and 3 are fed into an OR gate (Quad Input OR Gate), so if any of the logic detects a fault, the OCP switch has to be tripped. The output of OR gate (Quad Input OR Gate) is inverted through a NOT gate, Inverter or NOT Gate and pushed into the logical operator. The output of R/S latch port 3 is fed into the AND gate quad AND gate which is ANDed with microcontroller ports. All of the outputs of the AND gate are pushed into the gate drivers. This is an additional layer of safety for the main power switches. So, the switches to switches, both the microcontroller

Figure 6-31: hardware protection logic.
output and the over current should be within the limits.

6-8 Communication

6-8-1 Isolation Optocouplers for I\textsubscript{2}C, SPI and SCI Communication Interfaces

The entire converter is being designed in layers, so addition functionalities could be added as layers. The heart of this capability is the communication. The TMS320F28069 MCU, that is being used, supports I\textsubscript{2}C!, SPI, and SCI communication protocols. For maximum comparability and for all research intents and purposes, all the protocols are being made available in the converter. In order to interface the respective pins of the MCU with the control and communication module, optocouplers for isolation purposes are used. In this case it is important to consider the direction in which data flows. All the communication protocols are serial communication, and a brief explanation in provided in the following sections.

Serial port and issues:

A common serial port, the kind with TX and RX lines, is called asynchronous (not synchronous) because there is no control over when data is sent or any guarantee that both sides are running at precisely the same rate. Since computers normally rely on everything being synchronized to a single clock (the main crystal attached to a computer that drives everything), this can be a problem when two systems with slightly different clocks try to communicate with each other [88].

6-8-2 SCI

A serial communications interface (SCI) is a device that enables the serial (one bit at a time) exchange of data between a microprocessor and peripherals such as printers, external drives, scanners, or mice. The SCI enables serial communications with another microprocessor or with an external network, and more info could be found in [4].

6-8-3 SPI

Serial Peripheral Interface (SPI) is an interface bus commonly used to send data between microcontrollers and small peripherals such as shift registers, sensors, and SD cards. It uses separate clock and data lines, along with a select line to choose the device you wish to talk to [5].

Figure 6-32: Serial communication protocol and will often send the least significant bits first, so the smallest bit is on the far left. [88].
Figure 6-33: Interfacing of a single master - single slave with SCI protocol. The transmit pin of the master is connected to the receive pin of the slave and vice versa, from [4].

Figure 6-34: SPI uses separate lines for data and a clock that keeps both sides in perfect sync. [5].

6-8-4 \( I^2C \)

The Inter-integrated Circuit (\( I^2C \)) Protocol is a protocol intended to allow multiple slave digital integrated circuits (chips) to communicate with one or more master chips. Like the Serial Peripheral Interface (SPI), it is only intended for short distance communications within a single device. Like Asynchronous Serial Interfaces (such as RS-232 or UARTs), it only requires two signal wires to exchange information \[89\].

Each \( I^2C \) bus consists of two signals: SCL and SDA. SCL is the clock signal, and SDA is the data signal. The clock signal is always generated by the current bus master; some slave devices may force the clock low at times to delay the master sending more data (or to require more time to prepare data before the master attempts to clock it out). This is called clock stretching and is described on the protocol page.

The original specification allowed for only 100kHz communications, and provided only for 7-bit addresses, limiting the number of devices on the bus to 112 (there are several reserved addresses, which will never be used for valid \( I^2C \) addresses). Which was later expanded to 10-bit address space.
Figure 6-35: Interfacing of a single master - single slave with $I^2C$ protocol [90]. Both wires are bidirectional.

6-9 PCB Prototype

The Figure 6-36, shows the real PCB after production.

Figure 6-36: The back and the front view of the PCB.
Figure 6-37: The stencil for the PCB, for easy and efficient soldering.
### Table 6-3: List of Buck-Boost converter PCB Components

<table>
<thead>
<tr>
<th>Function</th>
<th>Name</th>
<th>Manufacturer</th>
</tr>
</thead>
<tbody>
<tr>
<td>12V to +/-15V</td>
<td>NMA1215DC</td>
<td>Murata Power Solutions</td>
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<tr>
<td>Power Supply</td>
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<td></td>
</tr>
<tr>
<td>15V to 5V</td>
<td>R-78E5.0-0.5</td>
<td>Recom Power</td>
</tr>
<tr>
<td>Power Supply</td>
<td></td>
<td></td>
</tr>
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<td>TLV1117-33CDCY</td>
<td>Texas Instruments</td>
</tr>
<tr>
<td>Power Supply</td>
<td></td>
<td></td>
</tr>
<tr>
<td>-15V to -3.3V</td>
<td>LT1964ES5-BYP#TRMPBF</td>
<td>Linear Technology</td>
</tr>
<tr>
<td>Power Supply</td>
<td></td>
<td></td>
</tr>
<tr>
<td>MCU</td>
<td>TMS320F28069MPZT</td>
<td>Texas Instruments</td>
</tr>
<tr>
<td>Operational</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Amplifier</td>
<td>OPA2350UA</td>
<td>Texas Instruments</td>
</tr>
<tr>
<td>Comparator</td>
<td>LMV762MA</td>
<td>Texas Instruments</td>
</tr>
<tr>
<td>MOSFET</td>
<td>2N7002,215</td>
<td>NXP</td>
</tr>
<tr>
<td>Buffer</td>
<td>74AC540SC</td>
<td>Fairchild Semiconductor</td>
</tr>
<tr>
<td>R/S Latch</td>
<td>CD4043BD</td>
<td>Texas Instruments</td>
</tr>
<tr>
<td>Optocoupler</td>
<td>ISO7240CDW</td>
<td>Texas Instruments</td>
</tr>
<tr>
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</tr>
<tr>
<td>I²C! Optocoupler</td>
<td>ISO1540DR</td>
<td>Texas Instruments</td>
</tr>
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<td>Infenion</td>
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<td>93LC46BT-I/OT</td>
<td>Microchip</td>
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<tr>
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<td></td>
<td></td>
</tr>
<tr>
<td>UART/FIFO</td>
<td>FT2232H</td>
<td>FTDI Chip</td>
</tr>
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</table>
In this chapter, a holistic Eagle’s view is taken over the entire spectrum of results presented in this research work. Multiple questions were posed at the onset of this project, and the aim of this MSc thesis was to answer these questions:

- **Is it possible to maintain power balance in a dynamic system, if yes, then how robust and reliable would the system be?**
  - Yes, the power balance controller is a hybrid control technique that can stabilize the grid in a dynamic system. The power balance controller creates a graph with their setpoints for every load and source based on their individual parameters. Each source and load has a different graph, which provides a current setpoint for the terminal voltage. This technique ensures stable grid operation without the aid of communication. Having decentralised controller is already a plus for robustness and reliability. Additionally, a number of scenarios were simulated as an attempt to disrupt the grid’s stability. The disturbances were easily counteracted within a fraction of seconds by the controllers and appropriate action, like shedding low priority loads were performed. So in a sense it could be said that the controller is quite robust and reliable to handle disturbances while in operation.

- **Software simulation and real life tests are poles apart, so how would this control strategy perform in a real life experiment and what would be difficulties encountered during the implementation?**
  - Thanks to Ir. Tsegay Gebremedhin the power balance controller algorithm had been tested on his DC microgrid setup. The setup and the result has been elaborated in the previous chapters. The overall experience of incorporating the controller algorithm on to this particular programmable controller was rather uncomfortable. Several work around had to be used to get the desired result, even then maximum current limit could not be implemented. This was mostly due to the lack of versatility of the current power electronic converter technology in implementing algorithms. Once implemented, The converter performs as expected from the simulations. This proves that the power
balance controller algorithm would perform equally as well as that in the simulations. In the setup the programmable converter is much slower than the other converter, then their is a delay between the PC and the converter. This was the major driving force behind developing our own converter.

- **How versatile is the power balance control scheme and explain it with some possible scenarios?**

  By performing multiple simulations under various different scenarios and the experimental tests, it could be established that the Hybrid power balance controller is versatile enough to handle the unexpected. And since it’s a common algorithm capable of adapting to any mode of operation, say source, load, or source/load; it could be said that the hybrid power balance converter is versatile enough to be used in most of the situations.

- **Does "Current pricing" work with the changing dynamics of a real system?**

  Current pricing in steady state is pretty straight forward, it was the dynamic state that raises concern. From the derivations and the simulations, current pricing can be used to eliminate loss-based market distortion in DC grids regardless of the grid structure. Cause the integration of current over a time period accommodates for all the storage elements, this is due to fact of law of conservation charge, which has to be satisfied under any condition.

- **What are the hardware requirements to allow the control scheme to work optimally?**

  After performing the simulation and the experiment the hardware required to achieve perfect real life experiment would need to have a faster response time. The converter used for experiment had delay of 1ms, which in turn plagued the results with oscillations. This invariance in result could cause the converter to switch between various modes of operation; which is undesirable. In case of fault, the converter need to act quickly and trip the circuit. hence our converter was designed around these ideas, the switches switch at much faster rate of 100KHz, i.e 10µs, and the fault detection and tripping time is somewhere around 200ms.

The goal with which we set were to have a decentralised primary controller with advantages of various individual control techniques mixed together, which would easy to use and yet elegant. The control algorithm delivers stable operation of the grid even under multiple abnormal scenarios, without any communication. The control has even shown to work under black start, albeit their are some transient, but it recovers within fraction of a second, thus the maximum value of the oscillation stays within limits.

The control algorithm seemed to hold up upon testing in areal life scenario. Although the equipment was less than optimal for proper testing. Even then it can be seen that for a converter which could compliment the software, would perform quite well to stabilize the grid.

The current pricing works optimally in a dynamic setup, which accounts for all the losses encountered while distribution of power. Currently the grid operator has to bear the expense for any transmission and distribution loss, which the current pricing would shift to the prosumers. This could be further improved upon to encourage use of power from the closest of
sources so as to reduce the losses encountered in distribution loss. Thus reducing the overall expense and increasing power delivery efficiency. The developed theory’s holds even in the rigorous of the simulations, thus proving the concept feasible.

The experiment performed proved that the present hardware technology is not suited for research and experiment of hybrid power balance controller or other control techniques. Hence with the necessary specification we the non-inverting buck-boost converter was designed and built from ground up. Theoretically all and experimentally some of the features were tested and finally the converter was successfully built.

7-1 Outlook and Future Work

There is only so much one can achieve during the short tenure of a MSc thesis, but further research and experimental work is necessary. To name some:

- Hardware testing remains to be seen, designing is something, but testing is all together different thing. The intended features remain to be tested, which in turn will lead to future enhancements in design and operation of the converter. Currently the converter is rated at 400v at 1A steady operation, which has to be increased with future iterations. With more and more research in the field of protection, it only stands to further enhancements in the capability of the converter.

- The power balance controller has only been proven in simulation with a fundamental experiment to back it up, but further experiments and advancements would be necessary for the controller algorithm to be used in real life.

- Implementation of storage, the controller is designed in such a way that it can be used under any kind of operation, but with storage things change a bit. Storage, other than acting as a grid has another parameter; state-of-charge, which determines the amount of energy left in the battery. State-of-charge also influences the battery life to a great extent, hence while using the power balance controller for battery, an additional parameter of state-of-charge is to be inducted which will influence battery’s performance. This itself could form a broad research topic on its own

Once the hardware operation is well within the satisfactory limit, more experimental based research could be performed. A real life grid with real solar PV, wind turbine, micro-hydro, CHP, etc. could be built based on the hardware and thus extensive experiments under real elements would be feasible.
Included here are the schematic for the non-inverting buck-boost converter developed for our research and experiment.
Inrush Current Limiting

LM833D

3.3V

12K

12K

12K

12K

20

2.7K

1K

100n

U14G$1

V+
+IN_A
3
OUT_A
1
V-
4
-IN_A
2

U7

VCC+
8
POS_1
3
NEG_1
2
NEG_2
6
POS_2
5
VCC-
4

U29G$1

V+
8
+IN_A
3
OUT_A
1
V-
4
-IN_A
2

U29G$2

+IN_B
5
-IN_B
6
OUT_B
7

R88

R62

R63

R65

R66

R68

R69

R71

R72

R67

R73

R64

C33

C34

C38

C39

C40

C53

C54

C55

C60

C95

C96

P$1

P$2

P$1

C

P$2

D

GND

GND

GND

GND

GND

GND

GND

A

B

C

D

E

Inrush current limiting

TITLE: BuckBoostThesis
Document Number: BuckBoostThesis
Date: 25-09-2015 07:30:16
Sheet: 6/11
A-1 PCB

The figures show the final manufactured PCB.

Figure A-1: The top view of the naked PCB. The golden parts are to solder the components.
Figure A-2: The bottom view of the naked PCB. The golden parts are to solder the components.
Appendix B

Hardware Communication in Detail

The MCU f28069 from TI supports multiple communication protocols, and a further comprehensive view is presented in this chapter.

Serial port and issues:

A common serial port, the kind with TX and RX lines, is called asynchronous (not synchronous) because there is no control over when data is sent or any guarantee that both sides are running at precisely the same rate. Since computers normally rely on everything being synchronized to a single clock (the main crystal attached to a computer that drives everything), this can be a problem when two systems with slightly different clocks try to communicate with each other [88].

B-0-1 SCI

A serial communications interface (SCI) is a device that enables the serial (one bit at a time) exchange of data between a microprocessor and peripherals such as printers, external drives, scanners, or mice. The SCI enables serial communications with another microprocessor or with an external network, and more info could be found in [4].

The SCI contains a parallel-to-serial converter that serves as a data transmitter, and

Figure B-1: Serial communication protocol and will often send the least significant bits first, so the smallest bit is on the far left. [88].
a serial-to-parallel converter that serves as a data receiver. The two devices are clocked separately, and use independent enable and interrupt signals. The SCI operates in a nonreturn-to-zero (NRZ) format, and can function in half-duplex mode (using only the receiver or only the transmitter) or in full duplex (using the receiver and the transmitter simultaneously). The data speed is programmable. Serial interfaces have certain advantages over parallel interfaces. The most significant advantage is simpler wiring. In addition, serial interface cables can be longer than parallel interface cables, because there is much less interaction (crosstalk) among the conductors in the cable.

![Figure B-2](image.png)

A universal asynchronous receiver/transmitter, abbreviated UART, is a computer hardware device that translates data between parallel and serial forms. UARTs are commonly used in conjunction with communication standards such as TIA (formerly EIA) RS-232, RS-422 or RS-485. The universal designation indicates that the data format and transmission speeds are configurable. The electric signaling levels and methods (such as differential signalling etc.) are handled by a driver circuit external to the UART.

### B-0-2 SPI

Serial Peripheral Interface (SPI) is an interface bus usually used to send data between microcontrollers and small peripherals such as shift registers, sensors, and SD cards. It uses separate clock and data lines, along with a select line to choose the device you wish to talk to [5].

#### Synchronous Solution

SPI works in a slightly different manner. It’s a synchronous data bus, that means that it uses separate lines for data and a clock that keeps both sides in perfect sync. The clock is an oscillating signal that tells the receiver exactly when to sample the bits on the data line. This could be the either low to high, raising or high to low, falling edge of the clock signal; the datasheet will specify which one to use. When the receiver detects that edge, it will immediately look at the data line to read the next bit (see the arrows in the below Figure B-5) Because the clock is sent along with the data, specifying the speed isn’t important, although devices will have a top speed at which they can operate.
Receiving Data

In SPI, only one side generates the clock signal (usually called CLK or SCK for Serial Clock). The side that generates the clock is called the master, and the other side is called the slave. There is always only one master (which is almost always your microcontroller), but there can be multiple slaves (more on this in a bit).

When data is sent from the master to a slave, it’s sent on a data line called MOSI, Master Out / Slave In. If the slave needs to send a response to the master, the master will continue to generate a prearranged number of clock cycles, and the slave will put the data onto a third data line called MISO, Master In / Slave Out.

Slave Select

This tells the slave that it should wake up and receive or send the data and also can be used when multiple slaves are present to select the one to talk to. The Fig. B-4 shows how the slave select (SS) works, which is generally used for multiple slave communication.

The SS line is normally held high, which disconnects the slave from the SPI bus. (This type of logic is known as active low, and one would often see it used for enable and reset lines.) Just before data is sent to the slave, the line is brought low, which activates the slave. When done using the slave, the line is made high again. In a shift register, this corresponds to the latch input, which transfers the received data to the output lines [5].

B-0-3  I2C

The Inter-integrated Circuit (I2C) Protocol is a protocol intended to allow multiple slave digital integrated circuits (chips) to communicate with one or more master chips. Like the Serial Peripheral Interface (SPI), it is only intended for short distance communications within
Figure B-4: Master always generates the clock signal, it must know in advance when a slave needs to return data and how much data will be returned. SPI uses separate lines for data and a clock that keeps both sides in perfect sync. [6].

a single device. Like Asynchronous Serial Interfaces (such as RS-232 or UARTs), it only requires two signal wires to exchange information [89].

Each I2C bus consists of two signals: SCL and SDA. SCL is the clock signal, and SDA is the data signal. The clock signal is always generated by the current bus master; some slave devices may force the clock low at times to delay the master sending more data (or to require more time to prepare data before the master attempts to clock it out). This is called clock stretching and is described on the protocol page.

The original specification allowed for only 100kHz communications, and provided only for 7-bit addresses, limiting the number of devices on the bus to 112 (there are several reserved addresses, which will never be used for valid I2C addresses). Which was later expanded to 10-bit address space.

Protocol

Communication via I2C is more complex than with a UART or SPI solution. The signalling must adhere to a certain protocol for the devices on the bus to recognize it as valid I2C communications.

Messages are broken up into two types of frame: an address frame, where the master indicates
Figure B-5: SPI uses separate lines for data and a clock that keeps both sides in perfect sync. [5].

Figure B-6: Interfacing of a single master - single slave with I²C! protocol [90]. Both wires are bidirectional.

The slave to which the message is being sent, and one or more data frames, which are 8-bit data messages passed from master to slave or vice versa. Data is placed on the SDA line after SCL goes low, and is sampled after the SCL line goes high. The time between clock edge and data read/write is defined by the devices on the bus and will vary from chip to chip [89].

The Fig. B-6, B-5, B-2 shows the information on the communication protocols. Based on these figures the pins of the optocouplers are connected to the Micro-controller (MCU) and to the...
**Figure B-7:** Interfacing of a single master - single slave with \( I^{2}C \) protocol [89]. Both wires are bidirectional.

common header, which will be then connected to the control and communication module, for controlling all the MCU from a central point.


[18] Siemens, “Long-distance power transmission,”


[26] D. foundation, “DESERTEC.”


[90] Wikipedia, “Sample Inter-Integrated Circuit (I2C) schematic with one master (a microcontroller) and three slave nodes (an analog-to-digital converter (ADC), a digital-to-analog converter (DAC), and a microcontroller),” 2006.
# Glossary

## List of Acronyms

<table>
<thead>
<tr>
<th>Acronym</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>DC</td>
<td>Direct Current</td>
</tr>
<tr>
<td>AC</td>
<td>Alternate Current</td>
</tr>
<tr>
<td>LVDC</td>
<td>Low Voltage Direct Current</td>
</tr>
<tr>
<td>LED</td>
<td>Light Emitting Diode</td>
</tr>
<tr>
<td>CCM</td>
<td>Continuous Conduction Mode</td>
</tr>
<tr>
<td>DCM</td>
<td>Discontinuous Conduction Mode</td>
</tr>
<tr>
<td>PWM</td>
<td>Pulse Width Modulation</td>
</tr>
<tr>
<td>DAB</td>
<td>Dual Active Bridge</td>
</tr>
<tr>
<td>PCB</td>
<td>Printed Circuit Board</td>
</tr>
<tr>
<td>MCU</td>
<td>Micro-controller</td>
</tr>
<tr>
<td>SI</td>
<td>International System for Units</td>
</tr>
<tr>
<td>USB</td>
<td>Universal Serial Bus</td>
</tr>
<tr>
<td>IC</td>
<td>Integrated Circuits</td>
</tr>
<tr>
<td>OCP</td>
<td>Over Current Protection</td>
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