Material-inversion solid-phase epitaxy of p⁺ Si for elevated junctions

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Recently, we presented a solid-phase epitaxy (SPE) process based on material inversion of an aluminum/amorphous-silicon stack that offers a new solution to ultra-shallow p-type junction formation [1]. It was shown that the size and high quality of the SPE c-Si island could be well-controlled by the stack thickness and lateral dimensions. In the present study, we demonstrate the controllability of the whole process when the junction area is reduced to the sub-100 nm range and the processing temperature is reduced to 400 °C. The SPE-Si/Si-substrate interface, analyzed locally by transmission electron microscopy (Fig. 1) and more systematically by the fabrication and electrical characterization of p⁺-n diodes, was found to be practically defect-free. It is remarkable that even for junction areas as small as 200×200 nm², the diodes have very low ideality factors without resorting to any form of extra perimeter doping as is mainly necessary in conventional selective CVD epitaxy processes used for elevated S/D formation. The presented SPE process is moreover processed at such low temperatures that all transient-enhanced diffusion of dopants is avoided and the SPE p⁺-island to n-substrate transition is ideally abrupt.

The SPE process renders an Al-doped c-Si island in a fully CMOS compatible manner. Here the growth is induced in windows to the <100> Si substrate that are defined by optical lithography and the lateral dimensions are brought down to the 100 nm range by using SiN spacers. As seen in Fig. 2, the I-V characteristics of the as-fabricated p⁺-n diodes are near ideal (n = 1.02) over the whole wafer. Since the metallurgic junction lies at the substrate to island interface, it can be concluded that the epitaxial process is characterized by a very low density of defects that can lead to generation/recombination centers in the depletion region. The contact resistance to both p⁻ and p⁺-bulk-Si regions was found to be low ohmic and the total contact resistivity of the elevated p⁺ Si was measured to be at most 10⁻⁷ Ω×cm². The measured resistance, that includes the island to contact-metallization contact resistance as well as the resistance through the SPE island itself, increases when the deposition temperature is decreased (Fig. 3). This is presumably due to a decrease of dopant incorporation during epitaxy for lower temperatures. The abruptness of the doping transition has been verified by an in-house capacitance-voltage (C-V) doping profiling technique that uses an abrupt n⁺ buried layer to profile the tail of high-gradient B-doped layers at the wafer surface (Fig. 4). The height of the SPE-island has been fabricated down to 20 nm. In summary, it has been demonstrated that the presented technique can be reliably used to form high-quality nanoscale p⁺-n junctions that may be attractive for elevated S/D formation.

REFERENCES

1. Y. Civalé *et al.*, *IEEE Electron Device Lett.*, pp. 341-343, vol.27, no. 5, May 2006.

Fig. 1. (a) SEM micrographs of the contact window before and after silicon SPE. The inset shows the original contact window (dark center region) that is less than 100 nm in size. A crystal preferably grows at the interface with the Si substrate rather than on the surrounding oxide, and overgrows the contact windows. (b) HRTEM image of the growth interface.

Fig. 2. Over the wafer current-voltage characteristics of 200×200 nm² junctions fabricated on an n-type substrate. When SPE is performed, a p⁺-n diode characteristics is measured. Without SPE, Al/Si(1%) metallization to n-doped silicon gives Schottky diode characteristics.

Fig. 3. Contact resistance of SPE p⁺ filled contacts measured on special Kelvin test structures with low-ohmic p⁺ diffusion taps as a function of SPE temperature.

Fig. 4. Doping profiles extracted from C-V measurements from a buried n⁺ layer to the contact window surface.