HF Silicon ICs for Wide-Band Communication Systems

- Technology characterization
- Modelling
- Design

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PROEFSCHRIFT

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Leonardus Cornelis Nicolaas de VREEDE

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geboren te Delft
Dit proefschrift is goedgekeurd door de promotor:

Prof. dr. ir. R.G. Baets

en de toegevoegd promotor:

Dr. ir. H.C. de Graaff

J.L. Tauritz, M.Sc. heeft als begeleider in belangrijke mate aan het totstandkomen van het proefschrift bijgedragen.

Samenstelling promotiecommissie

Rector Magnificus
Prof. dr. ir. R.G. Baets
Dr. ir. H.C. de Graaff
Prof. dr. ir. J.W. Slotboom
J.L. Tauritz, M.Sc.
Prof. dr. ir. R.J. van de Plassche
Prof. ir. A.J.M. van Tuijl
Prof. dr. ing. H. Schumacher

Technische Universiteit Delft, voorzitter
Technische Universiteit Delft, Universiteit Gent, promotor
Technische Universiteit Delft, toegevoegd promotor
Technische Universiteit Delft
Technische Universiteit Delft
Technische Universiteit Eindhoven
Universiteit Twente
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Stellingen
behorende bij het proefschrift

"HF Silicon ICs for Wide-band Communication Systems"


1. Het door Perna geïntroduceerde opgevolgen-transmissielijnmodel\(^1\) voor keramische multilaagscondensatoren mist een fysische basis. Hierdoor zijn Ingalls en Kent's uitbreidingen\(^2\) niet zinvol en is het resultaat onbruikbaar. Juister is de "multiconductor" aanpak\(^3\).


2. Het gebruik van de unilaterale vermogensversterking voor de bepaling van \(f_{\text{Max}}\) leidt tot een overschatting van de transistoreigenschappen (zie hoofdstuk 2).

3. Correct gebruik van kwaliteitsgetallen voor bipolare technologie is moeilijk blijkens de vaak vrije interpretatie van "Figures of Merit"\(^4\) om proces technologie te karakteriseren\(^5\).


4. Het VBIC95 epilaagmodel\(^7\) omzeilt de singulariteit in de epilaagweerstand die optreed bij de kritische stroomdichtheid van het Kull model,\(^6\) maar is incorrect wanneer de transistor dieper in quasi-saturatie wordt gedreven (zie hoofdstuk 4).


5. De waarde van een model wordt in belangrijke mate bepaald door zijn geschiktheid voor parameterextractie.

6. Hoe groter de signaaluitstoring, hoe onbelangrijker de vorm van de devicekarakteristieken\(^8\) is voor distorsie.

7. Het controleren van de modelvergelijkingen voor transistoren d.m.v. de niet-lineaire signaalvervorming vertoont veel overeenkomsten met het bestuderen van olifanten m.b.v. een elektronenmicroscoop.

8. De wens tot integratie van passieve circuitelementen met een hoge kwaliteitsfactor zal één van de belangrijkste drijfveren worden in de ontwikkeling van IC-technologie voor de telecommunicatie.

9. Dat het opstellen van een contract tussen TU en bedrijfsleven meer tijd vergt dan het in het contract vastgestelde project, blijkt uit het toenemende aantal contracten dat getekend wordt nadat het project is afgelopen.

10. Een proefschrift vertoont veel gelijkenis met een fotoalbum in die zin dat alleen de geslaagde momenten worden vastgelegd.

11. Gemeten naar de medische klachten is promoveren eerder een lichamelijke dan een geestelijke inspanning.

12. Het voor- en nadeel van een coalitieregering is dat niemand krijgt waar hij voor gestemd heeft.

13. Natuurontwikkeling in Nederland vindt meestal plaats in die gebieden die door een uitzonderlijk hoog geluidsniveau ongeschikt zijn voor woningbouw.

14. Microwave-techniek is geen ambacht, doch ook niet beperkt tot de aaneensluiting van los gekarakteriseerde "black boxes", maar een samensmelting van wiskunde, fysica en electronica, m.a.w. een moeilijk verteerbare "cheese burger".


Chapter 1  Introduction to HF silicon

1.1 Introduction

This thesis is on the realization of application-specific radio frequency integrated circuits (MMICs) for use in modern telecommunication systems. There are generic circuit requirements for wide-band systems featuring high bit rates (fibre optic links) and, more recently, (early nineties) for narrow-band systems for mobile telecommunication services in densely populated frequency bands. Circuits operating in the low GHz region place stringent requirements on the high-frequency behaviour of the process technology used.

GaAs has since the 1970s been the material of choice for the realization of MMICs. It is only in the last decade that silicon process technology became sufficiently developed for functionality above 1 GHz to be achieved. Progress booked in the development of discrete silicon process technology and the promise of extending this success to IC processes was the reason for the Microwave Component Group (MCG) to concentrate on the design and characterization of silicon MMICs. Concomitantly, the Dutch Ministry of Education chose to place major emphasis on silicon process technology and design in Delft, while GaAs activities were concentrated in Eindhoven. In March 1991, Philips Research invited the MCG to participate in a study on the design and application of silicon integrated circuits for use in broadband telecommunication systems at frequencies to 4 GHz and above.
Historical background

Initially, it was unclear to what extent silicon process technology would develop and whether circuit specifications in respect to bandwidth, noise and distortion were realizable. Today, there are few who would deny that silicon is the technology of the present and the future. Characteristic are: high performance double poly bipolar transistors with 2 GHz noise factors below 0.8 dB with cut-off frequencies up to 60 GHz (see Figure 1.1), high-speed digital CMOS circuits operating with clock speeds in excess of 500 MHz, very well-defined model libraries, an extraordinary degree of integrability and exceptional reliability. These advantages and the relatively low cost of silicon process technology make silicon the logical choice for most HF circuits.

![Graph showing evolution of silicon process technology](image)

**Figure 1.1.** Evolution of silicon process technology (source [1.27])

Is GaAs going out of business? For the time being, the answer is, "No". Two aspects of GaAs have not as yet been beaten by silicon. These are the very low noise performance of high electron mobility transistors (HEMTs) and the availability of low-loss transmission lines. Their combination facilitates the realization of high Q low noise circuitry. Conventional silicon realizations suffer from relatively high base resistance and poor transmission-line and inductor properties. In wide-band design, the advantages of GaAs are less evident since resonant circuitry is normally not used.
Future perspectives of silicon

The double polysilicon emitter transistor is representative of the present state of the art in bipolar technology. Although transition frequencies in excess of 60 GHz have been reported (see Figure 1.1), these devices suffer, in general, from excessive base resistance. Introduction of SiGe technology is a breakthrough of great potential, due to its inherent band-gap advantage, it allows higher doping in a thinner base thus yielding higher $f_T$'s with lowered base resistance. The noise level as well as the maximum operating frequency are, thereby, significantly improved.

When SiGe transistors are grown on semi-insulating substrates, the main shortcomings of Si-based technology in respect to GaAs are eliminated. An alternative to the realization of high Q circuit components is the application of locally under-etched lines, capacitors and inductors [1.35]. High line losses in inductors may be mitigated by the use of stacked metallization layers [1.32].

GaAs is, therefore, at some risk of remaining a “niche component technology” [1.28] of residual interest in some low-noise high Q applications above 10 GHz. The introduction of SiGe with on-chip high Q elements will significantly erode this remaining domain as well.

1.2 The Development of Silicon HF ICs

The development of silicon HF ICs makes high demands on process technology, simulation tools, component models and circuit architecture. It is for this reason that this study is not limited to the realization of HF circuits, but also considers other aspects of the design flow, such as the selection of process technology and modelling. Further, there was a demonstrable need for a design environment suitable for the development of HF silicon ICs. Covering the complete design trajectory of HF ICs in detail is beyond the scope of this thesis. We have chosen to treat selected issues in HF silicon design in more detail rather than to attempt completeness.

This thesis is anchored in the context of the standard design flow for silicon HF ICs as depicted in Figure 1.2. The following three areas are treated, namely:

- technology characterization
- modelling
- design

The programs used within the design trajectory are: HP's Microwave Design System (MDS) (a design program with powerful simulator tools), HP's ICCAP (a model parameter extraction program) and CHIPGRAPH (a Mentor Graphics layout tool for silicon ICs). The programs MDS and ICCAP have been developed for use in GaAs IC and discrete HF circuit design. The customizing of these programs and the addition of accurate Philips' models has led to a design environment dedicated to HF silicon ICs. This environment incorporates powerful simulator tools with accurate models and libraries of silicon devices, thus enabling the designer to fully explore the possibilities of the available silicon process technology.
Figure 1.2. Cross-section of the context of this thesis with the design flow of silicon HF ICs and the programs used

1.3 HF Silicon Technology Characterization

Starting from system specifications (see Figure 1.2), a circuit is often specified in terms of bandwidth, noise level and dynamic behaviour. Meeting the specification on bandwidth and noise is strongly dependent on the available process technology. In the past, the chance of success was often estimated by using the widely known transition frequency $f_T$ (see also Figure 1.1). Unfortunately, $f_T$ includes only limited information on the process technology, and ignores important parameters such as the base resistance, so that its predictive validity is limited. There is a clear and evident need for Figures of Merit that are more precise in respect to specific circuit performance, i.e. switching speed [1.36] and noise [1.5]. Ideally, the influence of biasing and emitter length scaling should be excluded so that these Figures of Merit are a primary measure of process technology. With their aid, designers should be
able to select the process technology that meets their circuit specifications. However, for process developers, it is useful to know to what extent their process noise and switching performance can be improved without the need of extensive circuit simulations. This subject is treated in Chapters 2 and 3.

1.4 HF Silicon Modelling

One of the most important components for the HF silicon designer is the bipolar transistor. Working on the premise that proper design is contingent on the availability of accurate models, significant effort was put into the development of transistor models. This has led to a number of compact models which have been placed in the public domain:

- Ebers-Moll [1.13]
- Gummel-Poon [1.15]
- Extended Gummel-Poon (Kull Extension [1.17]), VBIC95 [1.31]
- Mextram [1.18]

In order of their appearance, an increasing number of electrical effects have been included in the models, improving their accuracy, but also leading to increased model complexity and parameter count. In general, more advanced transistor models entail longer computation time and more difficult parameter extraction. Faster computers and the use of sophisticated parameter extraction software and measurement protocols [1.30] contribute to the viability of the sophisticated models. The current state of the most commonly used public domain models is given below.

![Transistor model diagram]

**Figure 1.3.** Current state of most commonly used public domain transistor models

For the past twenty years analogue designers have taken the Gummel-Poon model, which is widely available in the SPICE circuit simulator, to be the “standard”. Stringent constraints
on HF circuit specifications have, however, brought the adequacy of GP into question. The extended Gummel-Poon and Mextram models were developed to guarantee single-pass design flow and to obviate the need to redesign. Although there is a need for these more complicated models, it is difficult for the designer to have an overview. In order to increase the clarity in this area Chapter 4 addresses bipolar transistor models in the public domain. Their individual advantages and disadvantages are considered and a side-by-side comparison of the various models is provided in tabular form with emphasis on the formulation and the model parameters (see also [1.12]). The electrical characteristics are compared for DC, AC and large-signal conditions.

Our further study led to the conclusion that all these models were inaccurate under high-frequency large-signal conditions, particularly at the onset of quasi-saturation (q.s.). This problem was shared by the epilayer models Kull, VBIC95 and Mextram: Ebers-Moll and Gummel-Poon have no provision at all for dealing with q.s. [1.6, 1.11]. Specific experience gained with the Mextram model during this study has led to an extension of the collector charge description and improvement of the high current distortion behaviour at low and high frequencies [1.10]. This modified Mextram model, discussed in Chapter 6, is unmatched in accuracy in the presence of high current distortion when compared to the other models discussed and has been adopted as the official Mextram definition as implemented in Pstar and MDS.

The design trajectory requires accurate models not only for the active devices but for the passive components as well. In this context, work has been carried out on the implementation of a subset of the QUBIC library [1.19]. This complements the active device models Mextram and MOS9 [1.22] which have also been implemented in MDS by the author. MDS has thus been made compatible with the design environment used within Philips [1.20]

1.5 HF Silicon Design

Analogue circuit design for frequencies of 1 GHz and higher has traditionally been the domain of microwave practitioners. The methods developed by these practitioners are for the most part suitable for hybrid design in which individual semiconductor elements and other components are mounted on a suitable substrate. The use of transmission line concepts for modelling and characterization, most often in conjunction with GaAs devices, is characteristic of this work. Electronic designers, however, have developed elegant methods for the synthesis of more or less ideal components [1.14, 1.16, 1.23]. A synergistic blend of the analogue and microwave design worlds has in the case of wide-band discrete components proved profitable [1.26]. Amplifiers, in general, must meet requirements related to bandwidth, gain, stability, noise, group delay, linearity and dynamic range, among others. In the case of low-frequency amplifiers, specifications can often be simultaneously satisfied by using overall feedback. The application of overall feedback in high frequency design is often impractical because of the relatively high work frequency with respect to the $f_T$ or $f_{Max}$ of the active devices. The phase shift introduced by other circuit elements can further complicate the application of overall feedback. This is, for example, the case in very-wide-band amplifiers where overall feedback is replaced by local feedback [1.24, 1.25]. Unfortunately, the use of local feedback frequently results in poor noise performance.

In Chapter 8, a number of demonstrator circuits the design of which uses the HF Silicon design environment described above, namely, a series of pre-amplifiers [1.9] and an AGC
amplifier [1.4] intended for use in optical telecommunication systems are considered. The pre-amplifiers make use of local as well as overall feedback techniques, depending on individual bandwidth and noise requirements, while the AGC amplifier is based on the use of local feedback. The pre-amplifiers and the AGC amplifier were realized in Philips Research's experimental double poly process and Philips Semiconductors 1 μm Bipolar/CMOS process QUBiC, respectively.

In following the design path, it became apparent that a number of design aspects required additional attention. One of these was the stability of the balanced circuits. It was found that although of topical interest, most papers in the open literature concentrate on the amplifier response and are often vague, or consider only in a general way aspects related to stability. This has led us to study the stability conditions of balanced amplifiers in more detail.

1.5.1 Stability

Amplifiers designed for high bit-rate telecommunication systems have to combine wide-band transfer with substantial gain. This combination makes the amplifier prone to oscillation [1.21]. Mounting parasitics are the limiting factor in the full exploitation of the potential gain-bandwidth product (GB) of HF silicon process technology. Minimization of package related parasitics like bondwire inductance and pin to pin capacitance is highly desirable. In Chapter 7 reformulation of the problem in generic terms has facilitated the derivation of a set of explicit guidelines for the designer in respect to the IC mounting configuration and circuit topology in order to minimize the influence of parasitics. This empowers HF designers to increase the practical gain bandwidth product limit.

1.6 Overview

This thesis deals with the following topics:

- **Silicon process technology characterization**: Tools for assessing competing silicon process technologies based on Figures of Merit related to the maximum operating frequency \(f_{\text{max}}\), switching speed \(\tau_{\text{opt}}\) and noise performance \(F_{\text{f=2GHz}}\) are introduced (Chapters 2, 3 and [1.2,1.5]).

- **Transistor models**: The most commonly used transistor models in the public domain, Ebers-Moll, Gummel-Poon, VBIC95 and Mextram are evaluated and compared. Using a tabular approach, the current and charge functions combined with standardization in circuit representation, node numbering and parameters designation are presented in an easy to use side by side comparison that offers direct and detailed insight into the four models (Chapter 4 and [1.3,1.8,1.12]).

- **Distortion**: The distortion behaviour of bipolar transistor models at high current levels is compared. Based on these results, the Mextram base-collector charge description is extended, ensuring monotonic Early voltages and improved modelling of nonlinear distortion at high current levels and frequencies (Chapters 5, 6 and [1.6,1.10,1.11]).

- **Stability of wide-band amplifier configurations**: Stability problems often encountered in the development of high gain wide-band amplifiers are considered. A general method for improving stability through a systematic choice of the connection layout, bias line configuration and circuit architecture is introduced. (Chapter 7).

- **Design examples**: A series of pre-amplifiers and a 4 GHz AGC amplifier designed for application in optical transmission systems are discussed (Chapter 8 and [1.4,1.7,1.9]).
### 1.6.1 Publications resulting from this work


### 1.7 Other references


Other references


[1.33] H.C. de Graaff and W.J. Kloosterman, The Mextram Bipolar Transistor Model (level 503.2), 1995. (implementation guide available on request from Philips Research Laboratories P.O. Box 80000, 5600 JA Eindhoven, the Netherlands.)


Chapter 2  
*The HF behaviour of the bipolar transistor*

2.1 Introduction

When designing HF circuitry, it is clear that improved components facilitate the designer's task of satisfying circuit specifications and at the same time enlarge the design space with respect to topological choices. In principle, a Figure of Merit for the HF behaviour of the most important individual component in the design process namely the bipolar transistor should provide the designer with information as to the viability of a given process technology.

Unfortunately, there are many different circuit applications and specifications, each with its own requirements in respect to base resistance, depletion capacitance, delay time, bias operating points etc. This has led to the definition of a number of Figures of Merit for the HF behaviour of the bipolar transistor. Prior to the introduction of Figures of Merit we consider the influence of technological choices on the performance of the bipolar transistor. In general, we can distinguish the following three areas (see Figure 2.1):
Introduction

Planar layout

![Planar layout and doping profile of a vertical bipolar transistor](image)

**Figure 2.1.** Planer layout and doping profile of a vertical bipolar transistor

- **Process technology:** Proscribes the doping profile, which is fixed and normally not assessable to the designer. The process technology defines the depletion capacitances per unit area, the transit time, the current gain, the base sheet resistances and the current densities for high injection and quasi-saturation based on the emitter length $L_e$.

- **Geometrical layout:** Within the process design rules, the designer can modify the emitter width ($S_e$) and emitter length ($L_e$). Emitter width down-scaling leads, to a certain extent (e.g. 0.5 μm), to smaller lateral dimensions and lower parasitics (i.e. base resistance) thus yielding an improved high-frequency performance. In general, HF designers tend to take the smallest possible emitter width $S_e$ and modify the transistor properties by scaling the emitter length $L_e$ in order to obtain the optimum device performance for a given circuit configuration. Scaling up the emitter length $L_e$ leads to a proportional increase in the depletion capacitances and decrease of the series resistances.

- **Bias operating point:** In order to optimize the transistor for circuit operation with respect to speed, noise etc. the designer has to find the optimum bias conditions.

From the above it is clear that it is only the process technology that cannot be changed by the designer and is by definition a given quantity; the other two provide the designer with much greater latitude. For this reason, it is convenient to use Figures of Merit, which are a measure of quality for process technology rather than for a specific device. Consequently,
The HF behaviour of the bipolar transistor

The influence of scaling the emitter length and the bias operation point should be eliminated. In order to avoid confusion during our analysis and discussions we distinguish the following items:

- **Parameters**: These represent the transistor model parameters (e.g. Ebers-Moll, Gummel-Poon, or Mextram parameters, see Chapter 4).
- **Quantities**: These represent the circuit elements of a scaled and biased transistor (e.g. hybrid π).

With the aid of these definitions, we give a brief overview of the most commonly used high frequency Figures of Merit of a bipolar transistor, namely: the cut-off frequency \( f_T \) and the maximum oscillation frequency \( f_{\text{Max}} \). We give for these Figures of Merit their definition, use, advantages and shortcomings. It will become clear from this discussion that there is a need for better Figures of Merit which are closer to realistic modern integrated circuit design. To this end two other Figures of Merit are proposed, namely: \( \tau_{\text{opt}} \) which gives the minimum gate delay time for optimally scaled and biased MCL gates, and \( f_{\text{2dB}} \) which provides information about the high-frequency noise behaviour of an optimally biased and scaled first-stage transistor of a front-end.

In conclusion, a graph illustrating the progress made in HF silicon technology as a function of time is presented. By using process information from several silicon technologies, conclusions are drawn as to the extent to which the various Figures of Merit are correlated and what they mean in real circuit design.

### 2.2 The hybrid π circuit and its elements

Figures of Merit for the HF behaviour of a bipolar transistor are usually based on a limited number of process / transistor parameters. These parameters can be related to the hybrid π circuit as given in Figure 2.2.

![Figure 2.2. The hybrid π circuit](image)

The elements of the hybrid π circuit can be expressed as follows:

\[
C_{b'c} = g_e T_0 + C_{T_E} \quad C_{b'c} = C_{T_C} \quad C_s = C_{T_S}
\]

\[
g_e = \frac{\partial I_c}{\partial V_{b'e}} = \frac{kT}{qI_c} \quad r_{b'e} = \frac{\beta}{g_e}
\]

The following quantities\(^1\) are assumed to be only slightly dependent on the bias conditions.
The cut-off frequency \( f_T \)

and will be treated as constants in the rest of our analysis; for realistic modern circuit design we take as bias condition \( V_{bc} = 0 \) V

- \( c_{TE} \): Emitter depletion capacitance (in normal operation \( c_{TE} = 2C_{JE} \)).
- \( c_{TC} \): Zero bias base collector depletion capacitance (in normal operation \( c_{TC} = C_{JC} \)).
- \( c_{TS} \): Zero bias collector substrate depletion capacitance (in normal operation \( c_{TS} = 0.5C_{JS} \)).
- \( \tau_0 \): Transit time, which can be found by extrapolation from the \( f_T \)-characteristic at \( V_{bc} = 0 \) V.
- \( r_b \): Base resistance, assumed to be independent of the bias current but the width modulation of the neutral base is taken into account by lowering the base resistance under the emitter, using [2.13]:

\[
r_b = R_{BC} + \frac{R_{BV}}{1 + \frac{C_{JE}V_{DE}}{Q_{BO}}}
\]

- \( \beta \): Small signal current gain which equals the maximum DC current gain \( \beta_{FE_{\text{max}}} \).
- \( I_{c_{\text{max}}} \): Bias current at maximum \( f_T \) \( (f_{T_{\text{max}}}) \), the transconductance at this bias point is \( g_{e_{\text{max}}} \).

**Emitter length scaling**

The effect of emitter length scaling leads to the first-order approximation that the quantities \( c_{TE}, c_{TC}, I_{c_{\text{max}}}, g_{e_{\text{max}}} \) are linearly proportional to the emitter length, \( r_b \) is inversely proportional. Note that \( \beta \) and \( \tau_0 \) are independent of the emitter length.

### 2.3 The cut-off frequency \( f_T \)

The most commonly used Figure of Merit for the HF behaviour of a bipolar transistor is cut-off frequency \( f_T \). Which is defined as:

- **The cut-off or transition frequency \( (f_T) \) is the frequency for which the magnitude of the AC current gain \( |h_{21}| \) drops to unity for a transistor in common emitter configuration with an AC-shorted collector.**

In terms of the hybrid \( \pi \) circuit shown in Figure 2.2, the two-port parameter \( |h_{21}| \) is given by:

\[
|h_{21}| = \left| \frac{\beta(-j\omega \frac{C_{bc}}{g_e} + 1)}{j\omega \frac{\beta}{g_e} (C_{bc} + C_{bc'}) + 1} \right| \tag{2.4}
\]

Substitution of \( |h_{21}| = 1 \), assuming a large \( \beta \) and \( \omega C_{bc}/g_e \ll 1 \), yields the commonly used equation:

---

1. The parameters used in the definitions of these quantities are listed in Table B.1, "Mextram 503 input list," on page 85

**HF Silicon Technology Characterization**
The HF behaviour of the bipolar transistor

\[ f_T = \frac{g_e}{2\pi(C_{b'e} + g_{b'c})} = \frac{1}{2\pi \left( \tau_0 + \frac{c_{TE} + c_{TC}}{g_e} \right)} \]  \hspace{1cm} (2.5)

Note that (2.5) implies a single-pole device. The neglect of the zero \( C_{b'c}/g_e \) in the current gain caused will affect the value found for the cut-off frequency. This because the levelling-off in \( f_T \) is now ignored. This levelling of can clearly be noted by transistors with \( C_{b'c} \) and \( C_{b'e} \) in the same order. However, for the designer this \( f_T \)-levelling-off is of little importance as long as \( \beta >> 1 \), so from this point of view equation (2.5) is justified. The parameter \( |h_{21}|l \) of equation (2.4) is plotted as a function of the frequency in Figure 2.3.

![Figure 2.3. Extrapolation of the \( h_{21} \) for the calculation of the \( f_T \)](image)

Measurement of the \( f_T \)

In general, the \( f_T \) is calculated from s-parameter data (see "Calibration and error correction" on page 24), which can be obtained by using a vector network analyzer (e.g. an hp8510b see [2.8]). The use of parameter extraction programs and computer-controlled bias supplies, s-parameter measurements can be performed at a fixed frequency \( f_{\text{meas}} \) as a function of the DC collector current, while keeping the base-collector voltage constant. Thus insight is gained in the high-frequency behaviour of the device under test as a function of the bias current. Note that the fixed frequency \( f_{\text{meas}} \) should be located on the 6 dB/oct slope of the \( |h_{21}|l \) curve (see Figure 2.3). The \( f_T \) is now calculated by extrapolation, using:

\[ f_T = f_{\text{meas}} |h_{21}|_{\text{meas}} \]  \hspace{1cm} (2.6)

The frequency extrapolation again implicitly assumes a single-pole device. The measured \( f_T(l_c) \) characteristic is plotted in Figure 2.4.
Figure 2.4. Measured \( f_T(I_c) \) characteristic as function of the DC collector current of a DIMES 03 npn transistor

Dependency of bias current and emitter length

According to its definition, see equation (2.5), the \( f_T \) is bias \((g_e)\) dependent. Starting at low current levels \( f_T \) increases with the collector current up to the point where quasi-saturation, high injection in the base, or current crowding, sets in. These effects lead to an increase in the transit time and base-collector storage charge, and thus to a decrease of the \( f_T \) consequently, the \( f_T(I_c) \) characteristic has a maximum of \( f_{T_{\text{max}}} \).

When considering the scaling of the emitter length \((L_e)\), the maximum cut-off frequency \( f_{T_{\text{max}}} \) (which occurs at \( I_{c_{\text{max}}} \)) works out to be independent of the emitter length; this is explained by the fact that \( \tau_0 \) is independent of \( L_e \) and both \( g_{e_{\text{max}}} \) and \((c_{TE}+c_{TC})\) are linearly proportional to \( L_e \).

\[
\begin{align*}
f_{T_{\text{max}}} = \frac{g_{e_{\text{max}}}}{2\pi((c_{TE}+c_{TC}) + \tau_0 g_{e_{\text{max}}})}
\end{align*}
\]

(2.7)

Discussion

The main advantage of the \( f_T \) as Figure of Merit for the bipolar transistor’s HF behaviour is its simplicity, and this is probable the reason for its wide acceptance. However, its simplicity is also a disadvantage, because its definition represents a nonrealistic circuit configuration (short-circuited output and the use of a current source as input). However, at high current levels up to the point where high-level injection and base widening take place, the maximum cut-off frequency \( f_T \) is a measure of the intrinsic physical limit of the frequency at which the
transistor can operate. Consequently, it can be concluded that for $f > f_{T\text{max}}$ the device is useless and for $f < f_{T\text{max}}$ not necessarily useful.

2.4 The high-frequency power gain and the maximum oscillation frequency $f_{\text{Max}}$

One important property of a transistor is its capability to amplify power at high frequencies. Unfortunately, the definition of the maximum power gain is open to ambiguity since the transistor may oscillate when in- and output terminations consistent with maximum power gain are emplaced. The maximization of power gain for a given device should therefore take place within constraints that ensure stable operation. However, for a qualitative comparison of individual devices, the capability of power amplification is more interesting than the realization of the actual circuit itself. For this reason designers use different definitions of high-frequency power gain (see appendix B).

In order to qualify the high-frequency power gain of a transistor, the gain-bandwidth frequency $f_{\text{Max}}$ has been proposed in [2.1,2.2,2.3]. This frequency, where the power gain is reduced to 1, gives, in principle, the highest frequency at which a transistor can oscillate. Its definition is:

- $f_{\text{Max}}$ is the frequency where the magnitude of the power gain of a transistor becomes unity.

In terms of the hybrid $\pi$ circuit, an approximation can be found [2.1,2.3,2.5] in the following formulation:

$$f_{\text{Max}} = \sqrt[3]{\frac{f_T}{8\pi r_b C_{b'c}}}$$  \hspace{1cm} (2.8)

where $r_b$ is the series resistance of the base and $C_{b'c}$ is the base-collector capacitance. It should be noted that this expression is not generally valid but is only valid for a limited range of values of $r_b$ and $C_{bc}$ (e.g. if the base resistance $r_b$ goes to zero, $f_{\text{Max}}$ becomes infinite). An alternative method is the extrapolation of the maximum unilateral power gain (see Appendix B). The disadvantage of this method is that it can lead to an over-estimation of the device properties by the fact that $s_{12}$ is set to zero. The most objective method is, in our opinion, to shift up in frequency, up to the point where the device under test has become unconditionally stable, after which $f_{\text{Max}}$ can be found by the extrapolation of $G_{A\text{Max}}$ (2.19) (See “Definitions of high-frequency power gain” on page 26.). In Figure 2.5 $f_{\text{Max}}$ is plotted using equation (2.8), (2.19) and (2.23). As can be seen in this figure, the use of the unilateral power-gain when $K<1$ leads to an overestimation of $f_{\text{Max}}$. The hybrid $\pi$ approximation (2.8) gives a reasonable approximation of $f_{\text{Max}}$ at moderate current levels with deviations appearing at higher currents. When the device under test is measured at a significant higher frequency (up to $K>1$) the differences between the maximum in unilateral power-gain $G_{T\text{umax}}$ and maximum power-gain $G_{A\text{Max}}$ are small.
The high-frequency power gain and the maximum oscillation frequency $f_{\text{Max}}$

\[ f_{\text{meas}} = 1.5 \text{ GHz} \]
\[ f_T (K<1) \]
\[ 2 \times 10^{10} \]
\[ 1.5 \times 10^{10} \]
\[ 1 \times 10^{10} \]
\[ 5 \times 10^{9} \]
\[ 0 \]
\[ 0.0001 \]
\[ 0.001 \]
\[ 0.01 \]
\[ I_C (A) \]

\[ f_{\text{meas}} = 5 \text{ GHz} \]
\[ f_T (K>1) \]
\[ 2 \times 10^{10} \]
\[ 1.5 \times 10^{10} \]
\[ 1 \times 10^{10} \]
\[ 5 \times 10^{9} \]
\[ 0 \]
\[ 0.0001 \]
\[ 0.001 \]
\[ 0.01 \]
\[ I_C (A) \]

Figure 2.5. $f_{\text{Max}}$ as function of the DC collector current for the DIMES03 transistor using: A) hybrid $\pi$ approximation (2.8), B) unilateral power gain definition $G_{T\text{max}}$ of equation (2.23) when $K<1$ (at 1.5 GHz) and C) max. power gain $G_{A\text{max}}$ of equation (2.19) when $K>1$ (at 5 GHz)

Measurement of the $f_{\text{Max}}$

By using similar calibration and de-embedding technics as for the $f_T$ measurement, the unilateral power gain can be calculated from the s-parameters as given in equation (2.23). When measured at a fixed frequency, $f_{\text{meas}}$, as a function of the collector current $I_C$, $f_{\text{Max}}$ can be found using:

\[ f_{\text{Max}} = f_{\text{meas}} \sqrt{G_{T\text{max}}} \] (2.9)

Again it should be noted that a single-pole device is assumed.

Discussion

The advantage of $f_{\text{Max}}$ above $f_T$ is the additional information about the base resistance (see equation (2.8)). This base resistance is a very important parameter in circuit design with respect to speed and noise. The frequency $f_{\text{Max}}$ however is most useful in narrow-band design using discrete components, because its definition assumes that the feedback of base-collector capacitance can be compensated. In integrated design, this is a difficult task and can only be realized in a relative narrow frequency band, which yields the conclusion that this Figure of Merit is not suitable for wide-band design.

When using equation (2.8), the dependency of the bias current and the emitter length will be the same as that of the cut off frequency $f_T$. Considering equation (2.23), it can be con-
cluded that the maximum in $f_{Max}$ can shift away from the maximum in $f_T$.

2.5 The minimum CML propagation delay time $\tau_{opt}$

To overcome the shortcomings for integrated bipolar circuits of the previous Figures of Merits ($f_T$ and $f_{Max}$) and to provide a more suitable standard, the minimum delay time in CML circuits ($\tau_{opt}$) is introduced. Recently, a number of papers treating this subject have appeared [2.10,2.15,2.21]. However, they differ in their approximations and accuracy, their main principle is based on the minimum delay time per CML gate. Here, too, we use the minimum delay time following from a long CML ring oscillator. Note that CML is sometimes confused with ECL logic, which has an extra emitter-follower buffer added, see Figure 2.6.

![CML and ECL gate](image)

**Figure 2.6.** The CML and ECL gate

When a CML stage is connected in an N-stage ring oscillator structure (which consists of an odd number of stages or an even number with one crossed connection), no stable operating point exists and the circuit will oscillate. Note that in such a configuration each CML stage is loaded with the input impedance of the next stage (see Figure 2.7).
Figure 2.7. The CML ring oscillator

The behaviour of the CML ring oscillator shown in Figure 2.7 is characterized by its voltage swing and oscillation frequency. The oscillation frequency determinates the propagation delay per stage. By its nature, the CML ring oscillator exhibits large-signal behaviour. We can, using the oscillation conditions for the loop gain $G$,

$$|G| = 1 \quad \text{arg}[G] = \frac{\pi}{N} + \pi,$$  \hspace{1cm} (2.10)

obtain an expression which represents the delay per gate [2.24]. By optimizing for the load resistance $R_l$ we find the minimum delay time. Using this optimization, the bias current is automatically optimized ($R_l|_{\text{gate}=\text{constant}}$ for a given voltage swing). The resulting expression is independent of the emitter length and can be considered as a process-technology-related Figure of Merit

$$\tau_{opt} = \tau_0 + r_b(2c_{TC} + c_{TE}) + 2\sqrt{(3c_{TC} + c_{TS} + c_{TE})(r_b\tau_0)}$$  \hspace{1cm} (2.11)

Discussion

The minimum delay of the CML stage has proved to be a useful Figure of Merit for fast-switching bipolar circuit conditions [2.24]. The formulation of (2.11) is a measure for process technology and includes the influence of the substrate capacitance ($c_{TS}$), thus illustrating its suitability for integrated circuit design. The accuracy of (2.11) (about 10%) can be even further improved by taking into account the influence of the series resistances $r_b$ and $r_c$ (see [2.24]).

2.6 $f_{Fc(dB)}$ the maximum frequency for a given noise level

This Figure of Merit for the high-frequency noise behaviour of the bipolar transistor in small-signal operation gives the upper frequency limit for a given noise level (e.g. the noise factor $F$ equals 2 dB) when using a purely resistive source [2.23]. Optimization both for bias and emitter length of the transistor provides a Figure of Merit for the high-frequency noise
behaviour which again is rather a measure for a given process technology than for a single transistor. The full derivation of this figure of Merit is given in Chapter 3. The principle is illustrated in Figure 2.8

![Figure 2.8. Maximizing the upper frequency for a given noise level $F_c$ by varying the bias ($I_c$) and emitter length of the transistor](image)

By applying a fit function to simplify the equations involved, the Figure of Merit for the high-frequency noise behaviour can be expressed as:

$$f_{Fc(dB)} = \frac{0.01\tau - 0.05 - \frac{1}{\beta} + \frac{F_c(dB)}{0.842\tau + 10.53}}{\sqrt{4\pi^2\tau_0 r_b (c_{TE} + c_{TC})}}$$

(2.12)

In which $F_c(dB)$ is the chosen noise factor $F$ in dBs. The parameter $\tau$ gives the ratio between the transit time and the time constant given by the base resistance and the depletion capacitances:

$$\tau = \frac{\tau_0}{r_b (c_{TE} + c_{TC})}$$

(2.13)

Discussion

In contrast to the previous Figures of Merit treated in this chapter, which concentrates on the signal-handling itself, the Figure of Merit proposed here concentrates on the quality of the signal transfer (with respect to noise). This makes this Figure of Merit very interesting to the analogue designer when designing low-noise front-ends. With the aid of this Figure of Merit, the suitability of a process technology can be checked against system specifications for noise without the need to perform extensive computations. Due to the fact that for a purely ohmic source the noise factor is a monotonic rising function, we are able to specify the noise performance for a given constant level as a single frequency.
2.7 Overview Figures of Merit

To reduce the confusion about the different Figures of Merit and to obtain insight into their real meaning with respect to process technology and their mutual correlation, we have calculated and plotted the Figures of Merit for a number of processes. The processes with their most important parameters are listed in appendix C. The results given in Figure 2.9 can be interpreted as the evaluation of silicon process technologies in time. In Figure 2.9 it is easy to see that the different Figures of Merit are correlated.

![Figure 2.9](image)

**Figure 2.9.** Evaluation of silicon process technology by plotting $f_{(P_c=2dB)}$, $1/(2\pi \tau_{opt})$, $f_T$ and $f_{Max}$

In order to illustrate this correlation in a clear and unified way, we have performed a linear scaling of the traces of Figure 2.9 and normalized the resulting frequency to one for the
QUBiC1 process. From this figure, it is clear that \( f_{(F_c=2dB)} \) is strongly correlated with the quantity \( 1/(2\pi \tau_{opt}) \). This is not surprising if we consider the definitions of these Figures of Merit (see equation (2.11) and (2.12)). The larger fluctuation of \( f_T \) and \( f_{Max} \) can be explained by the fact that they are only dependent on a subset of the transistor parameters. The correlation factors are listed in Table 2.1.

\[
\begin{array}{|c|c|}
\hline
\text{Correlation between:} & \text{coefficient:} \\
\hline
f_T \text{ and } f_{Max} & 0.979 \\
f_T \text{ and } 1/(2\pi \tau_{opt}) & 0.905 \\
f_T \text{ and } f_{(F_c=2dB)} & 0.899 \\
f_{Max} \text{ and } 1/(2\pi \tau_{opt}) & 0.966 \\
f_{Max} \text{ and } f_{(F_c=2dB)} & 0.959 \\
f_{(F_c=2dB)} \text{ and } 1/(2\pi \tau_{opt}) & 0.999 \\
\hline
\end{array}
\]

**Figure 2.10.** The different Figures of Merit normalized for the Qubic process

The correlation coefficients between the Figures of Merit has been given in Table 2.1. From the graph given in Figure 2.10, it is not difficult to conclude that the quality of a given process technology can be expressed best in the Figures of Merit developed for the high-frequency noise behaviour \( f_{(F_c=2dB)} \) and the quantity for CML switching conditions \( 1/(2\pi \tau_{opt}) \), both representing realistic circuit conditions for integrated circuit design and taking a large number of transistor parameters into account.
**Appendix A) Calibration and error correction**

To measure the actual device properties at high frequencies, error correction must be applied to remove the influence of connection parasitics (cables, connectors, microstrip lines etc.). For some of the packaged devices, special purpose coaxial test fixtures can be used. After applying a standard calibration with the network analyzer, the reference planes can be shifted from the outer connectors up to the leads of the device under test by using de-embedding techniques (see references [2.9] and Figure 2.11). Devices with a nonstandard package can be mounted on a printed circuit board. By using a TRL calibration (True Reflect Line calibration see [2.9]), again the reference planes can be placed up to the device leads. The latest method has the advantage that the device is measured in exactly the same environment as that in which it will be used (see Figure 2.12).

![Diagram of test fixture with device under test](image-url)

**Figure 2.11.** Special purpose coaxial test fixture with device under test

![Diagram of microstrip calibration set and device under test](image-url)

**Figure 2.12.** Calibration on printed circuit board using a TRL calibration method
In order to measure unpacked devices, on-wafer measurements can be performed by making use of a microwave probe-station. Currently, microwave probes that allow accurate measurements up to tens of GHz are available. With these probes and the TRL calibration, or by using a variant of this method, e.g. the LRM (Line Reflect Match) method (reference [2.12]), accurate reproducible on-wafer microwave measurements are possible. An additional de-embedding step [2.16] for the elimination of the influence of the connection lines should be applied if one only wishes to measure the actual device properties.

**Figure 2.13.** Test and de-embedding structures for on-wafer measurements
Appendix B) Definitions of high-frequency power gain

The power gain of a transistor stage is determined by three factors

1. The efficiency of the power transfer from the input generator to the transistor.
2. The transistor’s power gain.
3. The efficiency of the power transfer from the transistor output to the load.

The power gain of a stage can now defined by a combination of the points above. In this thesis, we restrict ourselves to two definitions of power gain which are commonly mentioned in literature, namely the transducer gain and the available power gain.

The transducer power gain is defined by:

\[
G_T = \frac{\text{power delivered to load}}{\text{power available from source}}
\]  \hspace{1cm} (2.14)

In terms of the s-parameters [2.7]:

\[
G_T = \frac{|s_{21}|^2(1 - |\Gamma_s|^2)(1 - |\Gamma_L|^2)}{|(1 - s_{11}\Gamma_s)(1 - s_{22}\Gamma_L) - s_{11}s_{21}\Gamma_L\Gamma_s|^2}
\]  \hspace{1cm} (2.15)

in which: \(\Gamma_s\) and \(\Gamma_L\) are, respectively, the source and load reflection. The available power gain is defined as:

\[
G_A = \frac{\text{power available from network}}{\text{power available form source}}
\]  \hspace{1cm} (2.16)

Expressed in the s-parameters:

\[
G_A = \frac{|s_{21}|^2(1 - |\Gamma_s|^2)}{(1 - |s_{22}|^2) + |\Gamma_s|^2(|s_{11}|^2 - |\Delta|^2) - 2\text{Re}(\Gamma_s(s_{11} - \Delta s_{22}^*)})
\]  \hspace{1cm} (2.17)

with:

\[
\Delta = s_{11}s_{22} - s_{12}s_{21}
\]  \hspace{1cm} (2.18)

Note that the transducer power gain represents the effective power transfer, while the possible power transfer is given by the available power gain. In order to maximize the power gain of a transistor stage, a simultaneous conjugate match for input and output should be applied while maintaining a stable operation (see [2.7] or [2.14]). This can only be applied if the stability factors \(K>1\) and \(|\Delta|<1\). If \(K>1\) and a simultaneous conjugate match at in- and output is achieved, then we have:

\[
G_T = G_{T\text{max}} = G_A = G_{A\text{max}} = \frac{|s_{21}|}{s_{12}}(K \pm \sqrt{K^2 - 1})
\]  \hspace{1cm} (2.19)

With the condition \(|s_{12}s_{21}| \neq 0\), and the stability factor \(K\) given by:
The HF behaviour of the bipolar transistor

\[ K = \frac{1 - |s_{11}|^2 - |s_{22}|^2 + |\Delta|^2}{2s_{21}s_{12}} \]  \hspace{1cm} (2.20)

However, in many cases we find for modern transistors \( K<1 \) at moderate frequencies. In order to find \( f_{\text{Max}} \) for these transistors (which is extrapolated from the high-frequency power gain), one can shift up in frequency to the point were \( K \) becomes larger than 1. This method has the disadvantage that the correct measurement frequency is not known from the start (this can lead to the need of an extra calibration procedure), but it will give realistic information about the actual \( f_{\text{Max}} \) of the device under test. Another approach is the use of the unilateral power gain, achieved by setting \( s_{12} \) equal to zero. The unilateral transducer power gain in terms of the s-parameters is now given by:

\[ G_{T/u} = \frac{|s_{21}|^2(1 - |\Gamma_3|^2)(1 - |\Gamma_4|^2)}{|1 - s_{11}\Gamma_3|^2|1 - s_{22}\Gamma_4|^2} \]  \hspace{1cm} (2.21)

By matching the in- and output with the complex conjugate of \( s_{11} \) and \( s_{22} \), respectively, (note that this simple matching technique is only allowed due to fact that \( s_{12}=0 \)), the maximum unilateral power gain is obtained:

\[ \Gamma_3 = s_{11}^* \quad \Gamma_4 = s_{22}^* \]  \hspace{1cm} (2.22)

Equation (2.21) reduces to:

\[ G_{T/\text{uMax}} = \frac{|s_{21}|^2}{|1 - s_{11}\Gamma_3|^2|1 - s_{22}\Gamma_4|^2} \]  \hspace{1cm} (2.23)

With equation (2.23) we can define \( f_{\text{Max}} \) as the frequency where \( G_{T/\text{uMax}} \) reaches unity. Note that setting \( s_{12} \) to zero will, in general, lead to an overestimation of the power gain performance of the device. To avoid this overestimation for the figures in this chapter, we have chosen to shift the frequency to the point were unconditional stable behaviour is demonstrated \( (K>1) \).
Appendix C) Silicon process data

<table>
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<td>$c_{TF}$ (ff)</td>
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<td>930</td>
<td>40.0</td>
<td>11.0</td>
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<td>16.9</td>
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<td>67.5</td>
<td>25.8</td>
<td>28</td>
<td>3.5</td>
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<td>$\tau_y$ (ps)</td>
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<td>38.9</td>
<td>18.7</td>
<td>13.6</td>
<td>13.3</td>
<td>5.4</td>
<td>3.7</td>
<td>4.7</td>
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<td>$r_0$ (\Ohm)</td>
<td>588.4</td>
<td>43.6</td>
<td>167.0</td>
<td>444.0</td>
<td>40.0</td>
<td>52.8</td>
<td>380.0</td>
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<td>$\beta$ (V$_{CE}$=0V)</td>
<td>66.0</td>
<td>80.0</td>
<td>80.0</td>
<td>92.0</td>
<td>100.0</td>
<td>72.0</td>
<td>80.0</td>
<td>84.0</td>
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<td>$I_c$ ($I_{max}$) (mA)</td>
<td>1.7</td>
<td>10.0</td>
<td>8.0</td>
<td>0.24</td>
<td>2.3</td>
<td>2.5</td>
<td>4.0</td>
<td>0.63</td>
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Table 2.2. Various silicon processes with their parameters

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<tbody>
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<td>$f_{max}$ (GHz)</td>
<td>2.6</td>
<td>3.1</td>
<td>10.9</td>
<td>11.3</td>
<td>12.5</td>
<td>27</td>
<td>39.5</td>
<td>36.9</td>
</tr>
<tr>
<td>$f_T$ (GHz)</td>
<td>7.5</td>
<td>3.7</td>
<td>8.4</td>
<td>10.2</td>
<td>10.5</td>
<td>25.1</td>
<td>41.7</td>
<td>30.0</td>
</tr>
<tr>
<td>$1/(2\pi v_{opt})$ (GHz)</td>
<td>0.58</td>
<td>0.7</td>
<td>2.5</td>
<td>3.0</td>
<td>3.3</td>
<td>6.4</td>
<td>6.7</td>
<td>8.0</td>
</tr>
<tr>
<td>$f_{(f=20dB)}$ (GHz)</td>
<td>0.47</td>
<td>0.42</td>
<td>1.5</td>
<td>1.9</td>
<td>2.1</td>
<td>3.7</td>
<td>3.9</td>
<td>4.6</td>
</tr>
</tbody>
</table>

Table 2.3. Overview Figures of Merit for the process given in Table 2.2.

2.8 References

[2.10] G.W. Taylor and J.G. Simmons, "Figure of Merit for Integrated Bipolar transistors," *Solid-


Chapter 3  \textit{The HF noise behaviour of bipolar transistors}

3.1 Introduction

In analogue signal processing, the noise behaviour of the electronic circuits is of paramount importance, especially at higher frequencies, where the noise factor increases significantly. In this chapter, a new Figure of Merit (FOM) for the high-frequency noise behaviour of a bipolar transistor, driven by a purely resistive source, is defined. This FOM (which should not be confused with the noise factor, sometimes also called noise figure) is shown to be convenient for assessing silicon technological development with respect to high-frequency noise behaviour. In conclusion, a comparison with capacitive sources that illustrates the applicability of the FOM in practical situations where the applied sources are not ohmic is carried out.

We start from a simple Ebers-Moll model but take into account the base resistance and the influence of the emitter resistance and derive an expression for the noise factor as a function of frequency, bias current and device geometry [3.1]. The Figure of Merit proposed is defined as follows:

\[ f_{FC} \, (\text{dB}) = \text{the frequency at which the noise factor } F, \text{ optimized with respect to bias current and device geometry, has increased to a specified value (e.g. } F = 1.5 \text{ or } 2.0 \text{ dB).} \]

This optimization relates the proposed Figure of Merit to technological processes rather than to devices. By using the formulas shortly to be presented, insight can be gained in the high-frequency noise behaviour of a given process, thereby obviating the need for full transistor characterization and extensive computations.
3.2 The noise model of the first-stage transistor

As starting point for our noise study, we use the circuit shown in Figure 3.1. In this figure, the basic bipolar transistor equivalent circuit is given with its dominant noise sources and ohmic input circuit. The 1/f noise of the base current and the shot noise of the collector leakage current are neglected. All noise sources are assumed to be white and uncorrelated.

![Diagram of transistor noise model](image)

**Figure 3.1.** Ebers-Moll noise model of a bipolar transistor with base and emitter resistance

Power spectrum noise sources with their thermal equivalent

The resulting noise power spectral components are:

\[ S(i_c) = 2qI_c = 2kTg_e \]

(3.1)

\[ S(i_b) = 2qI_b = 2q\frac{I_c}{h_{FE}} = \frac{2kTg_e}{h_{FE}} \]

(3.2)

\[ S(u_b) = 4kTR_b \]

(3.3)

\[ S(u_e) = 4kTR_e \]

(3.4)

with:

\[ g_e = \frac{1}{r_e} = \frac{qI_c}{kT} \]

(3.5)
3.3 The derivation of the noise factor \( F \) for a purely ohmic source

The source impedance \( R_s \) is considered to be purely ohmic with its own noise source \( u_{n\,\text{source}} \). The calculation of the noise factor \( F \) is now straightforward and is defined as the ratio of the total available noise to the noise of the source impedance at room temperature (290 degrees Kelvin) [3.2].

\[
F = \frac{\frac{u_{n\,\text{source}}^2}{2} + u_{n\,\text{network}}^2}{u_{n\,\text{source}}^2}
\]  \hspace{1cm} (3.6)

For the calculation of \( u_{n\,\text{network}} \), the remaining noise sources of the transistor should be transformed to one single source using a Thévenin representation. A straightforward approach to calculate \( u_{n\,\text{network}} \) for the circuit shown in Figure 3.1, which uses noise correlation matrices [3.3], [3.4] produces very cumbersome equations which are difficult to handle and mask insight. A more fruitful approach is to simplify the circuit given in Figure 3.1 by eliminating the emitter resistance \( R_e \) while taking into account its noise contribution.

In effect, we neglect the influence of \( R_e \) on the AC signal transfer and transfer \( R_e \)'s associated thermal noise source to the input. The influence of the emitter resistor \( R_e \) can be investigated by studying a chain parameter description of the intrinsic transistor combined with the emitter resistance. The chain parameters, which relate the output directly to the input quantities, are defined as follows:

\[
\begin{bmatrix}
U_1 \\
I_1
\end{bmatrix} = \begin{bmatrix} A & B \\ C & D \end{bmatrix} \begin{bmatrix} U_2 \\
I_2
\end{bmatrix}
\]  \hspace{1cm} (3.7)

We conclude that the influence of the emitter resistor \( R_e \) on the AC signal transfer can be neglected as long as \( R_e g_e << 1 \). Based on the equivalent small-signal circuit of a bipolar transistor with its parasitic resistors \( r_b \) and \( R_e \) in Figure 3.1, we can (using Kirchof's Voltage Law) carry out a Blackwell transformation or e-shift [3.5] which leads us to the situation shown in Figure 3.2

![Figure 3.2. Blackwell or e-shift of the emitter resistance noise source](image-url)
The derivation of the noise factor $F$ for a purely ohmic source

The resulting voltage noise source in the collector branch can be neglected. The noise source resulting from the emitter in the base branch can be directly combined with the one resulting from the base resistance, by replacing it by one single source with the value $4kT(r_b+R_e)$. Consequently, for the remainder of this paper, the noise contribution of the emitter resistance is modelled simply by adding its numerical value to the base resistance $r_b$ and ignoring the existence of $R_e$ in the rest of our calculations. This simplifies our calculation considerably and (according to some numerical verification) gives a good approximation as long as $R_e g_e << 1$. Following this simplification, a chain matrix transformation [3.6], [3.7] for the collector shot noise source is applied, yielding the situation shown in Figure 3.3.

![Figure 3.3. Transformation of the noise sources to the input using a chain matrix representation](image)

The relevant chain matrix parameters of the intrinsic bipolar transistor are given below:

$$B_{tr} = \frac{-1}{g_e - j\omega C_{b’c}} \quad D_{tr} = \frac{1 + j\omega r_{b’e} C_{b’e}}{g_e - j\omega C_{b’c}}$$ \hspace{1cm} (3.8)

For the condition that $\omega r_{e} C_{b’c} << 1$ these expressions can be simplified to:

$$B_{tr} = -r_e \quad D_{tr} = -\left[\frac{1}{\beta} + j\frac{f}{f_T}\right]$$ \hspace{1cm} (3.9)

with current gain and cut-off frequency given by:

$$\beta = g_e r_{b’e} \quad f_T = \frac{g_e}{2\pi(C_{b’e} + C_{b’c})}$$ \hspace{1cm} (3.10)

$C_{b’e}$ is the sum of the emitter diffusion and depletion capacitances ($g_e \tau_0 + C_{T_E}$), in which $\tau_0$ is the base transit time. In forward operation, $C_{b’c}$ is equal to the collector depletion capacitance $c_{TC}$, so that the cut-off frequency may be written as:

$$f_T = \frac{1}{2\pi(r_e (c_{T_E} + c_{TC}) + \tau_0)}$$ \hspace{1cm} (3.11)
Based on Figure 3.3, the noise voltage \( u_{n\text{network}} \), expressed in terms of the chain parameters of the transistor, is, on inspection:

\[
u_{n\text{network}} = u_{bn} + (R_s + r_b)I_{bn} + (B_{tr} + D_{tr}(R_s + r_b))I_{cn}\tag{3.12}\]

Using the simplified expressions for the chain matrix parameters of (3.8), we obtain for the noise factor:

\[
F = 1 + \frac{1}{R_s} \left[ \frac{r_e}{2} + \frac{(r_b + R_s)(r_b + R_s + 2r_e)}{2r_e} + \frac{(r_b + R_s)^2}{2r_e^2} + \frac{(r_b + R_s)^2}{2r_e} \left( \frac{f}{f_T} \right)^2 \right] \tag{3.13}\]

In the DC limit when \( f \) approaches zero, it can be shown that this is exactly equivalent to the van der Ziel results [3.2]. If we assume \( B \gg 1 \) and \( \omega r_e C_{D\text{c}} \ll 1 \), we can further simplify our calculations without introducing serious error into the expression for the noise factor given in [3.7]:

\[
F = 1 + \frac{1}{R_s} \left[ \frac{r_e}{2} + \frac{(r_b + R_s)^2}{2r_e} + \frac{(r_b + R_s)^2}{2r_e} \left( \frac{f}{f_T} \right)^2 \right] \tag{3.14}\]

This expression for the noise factor takes into account the current gain \( B \), the base resistance \( r_b \), the delay time \( \tau_0 \) and the depletion capacitances \( c_{TE} \) and \( c_{TC} \). This is in contrast to Hawkins’ [3.8] and van der Ziel’s [3.2] noise analyses which neglect the base collector capacitance \( C_{b\text{c}}(= c_{TC}) \). In the analysis of [3.2], however, the correlation between collector and base shot noise sources (which occurs at high frequencies) has been included. This is an effect which manifests itself most clearly when determining the optimum noise reflection parameter (which is needed to achieve the minimum noise factor) for devices with an extremely low base resistance. This correlation is a second-order effect which would unnecessarily complicate our equations and it has, therefore, been ignored.

### 3.4 Introduction of normalization and scaling

To obtain a noise FOM that is independent of the source impedance level, normalization and scaling of the device under consideration has proved useful. In the remainder of this paper, we introduce a reference transistor that is representative of for a particular process. This reference transistor is described by the parameters \( \tau_0, \beta, r_b, c_{TE} \) and \( c_{TC} \); the parameters \( \tau_0 \) and \( \beta \) are mainly process dependent, \( r_b, c_{TE} \) and \( c_{TC} \) are also dependent on geometry. For optimization purposes, we introduce the emitter length multiplication factor \( L_e \) (see Figure 3.4), which is the ratio of the emitter length of the transistor under consideration and the reference transistor.
We assume that the depletion capacitances are linearly proportional to the multiplication factor $L_e$ and that the base resistance is inversely proportional to $L_e$. Thus for a transistor with an arbitrary multiplication factor equation (3.14) becomes:

$$F = 1 + \frac{1}{\frac{R_s}{L_e} + \frac{1}{2} + \frac{(\frac{r_b}{L_e} + R_s)^2}{2\beta r_e} + \frac{\left(\frac{r_b}{L_e} + R_s\right)^2}{2r_e} \left(\frac{f}{f'}\right)^2}$$

(3.15)

where $f'T$ is:

$$f'T = \frac{1}{2\pi r_e L_e (c_{TE} + c_{TC}) + t_0}$$

(3.16)

Normalization results in the following:

$$F = 1 + \frac{1}{s + \frac{1}{2}} + \frac{\left(1 + \frac{1}{s}\right)^2}{2\beta r} + \frac{\left(1 + \frac{1}{s}\right)^2}{2r} (\tau + sr)^2 \Omega^2$$

(3.17)

where:

$$r = \frac{r_e}{R_s} \quad s = \frac{R_s L_e}{r_b}$$

(3.18)

$$\tau = \frac{\tau_0}{r_b (c_{TE} + c_{TC})} \quad \Omega = 2\pi r_b (c_{TE} + c_{TC}) f$$

(3.19)

The normalized quantities $r$, $\tau$ and $\Omega$ are geometry independent; $\tau$ is the ratio of the time constant determined by $r_b(c_{TE} + c_{TC})$ and the transit time $\tau_0$. 

HF Silicon Technology Characterization
3.5 Optimization for bias and device geometry

Noting that $r_e$ and thus $r$ are current dependent, the noise factor can be optimized with respect to the bias condition. We assume that $\tau_0, c_{TE}$, $c_{TC}$ and $r_b$ are current independent. The optimization is carried out by solving for the minimum in the noise factor function:

$$\frac{dF}{dr} = 0 \rightarrow r_{opt} = \left(1 + \frac{1}{s}\right) \sqrt{\frac{1 + \Omega^2 \tau^2}{1 + (1 + s)^2 \Omega^2}}$$

(3.20)

Substituting in equation (3.17) yields:

$$F_{r_{opt}}(s) = 1 + \frac{1}{s} + \left(1 + \frac{1}{s}\right)^2 s\tau \Omega^2 + \left(1 + \frac{1}{s}\right)^2 \sqrt{\frac{1 + \Omega^2 \tau^2}{1 + (1 + s)^2 \Omega^2}}$$

(3.21)

This is a function of the normalized frequency $\Omega$ and the normalized scaling factor $s$. Determination of an optimum value for $s$ is not straightforward. In particular, at low frequencies ($F=F_0$) there is no distinct optimum for $s$. This problem may be circumvented by setting the noise factor to a constant arbitrary value $F_c > F_0$ (e.g., 2 or 3 dB) and maximizing the corresponding frequency (see Figure 3.5) by differentiating $\tau \Omega^2$ with respect to $s$.

![Figure 3.5. Maximization of the bandwidth by optimizing for the scale](image)

Replacing $F_{r_{opt}}(s)$ by the constant $F_c$ and writing the frequency-dependent parameters explicitly we obtain:

$$\tau \Omega^2 = \frac{(sF_c - 1)^2 - 1}{2s(F_c - 1) - 2 + \tau + \frac{1}{\beta \tau} (1 + s)^2}$$

(3.22)

Putting $d(\tau \Omega^2)/ds=0$ and neglecting minor terms (assuming large $\beta$) leads to:
Optimization for bias and device geometry

\[
s_{opt} = \frac{1}{2} \left( 2 + F_c + \sqrt{F_c} \sqrt{F_c + 4\tau} \right) \frac{1}{F_c - 1} \tag{3.23}
\]

Substituting \( s_{opt} \) in equation (3.22) and using the definitions of \( \Omega \) and \( \tau \) we solve for our Figure of Merit, namely, the frequency \( f_{FC} \) for which the noise factor reaches the value \( F_c \).

\[
f_{FC(dB)} = \sqrt{\frac{\max(\tau\Omega^2)}{4\pi^2\tau_0 r_b(c_{TE} + c_{TC})}} \tag{3.24}
\]

Here \( \max(\tau\Omega^2) \) is the right-hand side of eq. (3.22) for \( s = s_{opt} \).

This defines our Figure of Merit with respect to the high-frequency noise behaviour of the bipolar transistor. The function \( \sqrt{\max(\tau\Omega^2)} \) complicates the use of equation (3.24). We have found it expedient to replace the function \( \sqrt{\max(\tau\Omega^2)} \) by a fit function. In Figure 3.6, \( \sqrt{\max(\tau\Omega^2)} \) is plotted as function of \( F_c \) (in dBs) with \( \tau \) as parameter.

![Figure 3.6](image)

**Figure 3.6.** The function \( \sqrt{\max(\tau\Omega^2)} \) with its fit function for \( \beta = 100 \)

\[
f_{FC(dB)} = \frac{0.01\tau - 0.05 - \frac{1}{\beta} + \frac{F_c(dB)}{0.842\tau + 10.53}}{\sqrt{4\pi^2\tau_0 r_b(c_{TE} + c_{TC})}} \tag{3.25}
\]

Alternatively, the fit function may be used to compute the optimized noise factor corresponding to a given bandwidth and process parameters.
The HF noise behaviour of bipolar transistors

\[ F_{c(dB)} = (0.842 \tau + 10.53) \left( f_{F_{c(dB)}}^{4\pi^2\tau_0 r_b (c_{TE} + c_{TC}) - 0.011 \tau + 0.05 + \frac{1}{\beta}} \right) \] (3.26)

3.6 Choice of the parameter values.

The capacitances \( c_{TE} \) and \( c_{TC} \), although slightly bias dependent, have been treated as constant in the optimization process. Realistic values for \( c_{TE} \) and \( c_{TC} \), corresponding to the normal forward bias condition, must be employed. To prevent results from being overly optimistic we take \( c_{TE} = 2C_{j0} \) (twice the zero bias emitter-base depletion capacitance) and \( c_{TC} = C_{jc} \) (the zero bias collector-base depletion capacitance).

We also assume \( r_b \) to be independent of the bias current, but we take the width modulation of the neutral base into account by lowering the base resistance under the emitter, using:

\[ r_b = R_{BC} + \frac{R_{BV}}{1 + \frac{C_{je} V_{DE}}{Q_{BO}}} \] (3.27)

in which: \( R_{BC} \) = the constant part of the base resistance, \( R_{BV} \) = maximum of the variable part of the base resistance, \( V_{DE} \) = emitter-base diffusion voltage, \( Q_{BO} \) = the base charge at zero bias.

We have chosen \( \beta = h_{FE_{max}} \); \( \tau_0 \) is obtained by extrapolating from the \( f_T \) characteristic at \( V_{bc}=0 \).

3.7 Results

In order to test the validity of our calculations and approximations, the accurate compact transistor model Mextram [3.9] as implemented at the Delft University of Technology in Hewlett Packard’s Microwave Design System (MDS) has also been used to calculate the noise factor. The Mextram model combines the benefits of a compact circuit model with the accuracy and insight of a physical device model.

The transistors were optimized in scale and bias to maximize the frequency at which the noise factor reaches the value of 2 dB (\( F_o = 2 \) dB). The optimized multiplication factor for the length of the emitter becomes:

\[ L_{eopt} = S_{opt} \frac{r_b}{R} \] (3.28)

We have treated three different processes, namely: a conventional oxide-isolated process (A), a modern production process [3.10] (B) and an advanced experimental process [3.11] (C). The calculated noise factor as a function of frequency is plotted in figures 3.7, 3.8 and
3.9 for these three processes by using the previously developed equations and the complete Mextram model.

![Graph showing computed noise factor for process A](image)

**Figure 3.7.** The computed noise factor for the optimized device of process A

![Graph showing computed noise factor for process B](image)

**Figure 3.8.** The computed noise factor for the optimized device of process B
The HF noise behaviour of bipolar transistors

![Graph showing noise factor F vs. frequency f (Hz) with Fc = 2 dB and \( \omega r_e C_{bc} = 0.04 \). The graph includes two curves labeled 'calculated' and 'Measram' with a marked point at \( f_{(Fc=2 \text{ dB})} = 4.5 \text{ GHz} \).]

**Figure 3.9.** The computed noise factor for the optimized device of process C

It is clear from these figures that for frequencies where \( \omega r_e C_{bc} \ll 1 \) both curves fit tightly. The results are summarized in Table 3.1.

<table>
<thead>
<tr>
<th>Process</th>
<th>A</th>
<th>B</th>
<th>C</th>
</tr>
</thead>
<tbody>
<tr>
<td>( f_{Fc=2 \text{ dB}} \text{ num. optimized (GHz)} )</td>
<td>0.41</td>
<td>2.1</td>
<td>4.37</td>
</tr>
<tr>
<td>( f_{Fc=2 \text{ dB}} ) (eq. (3.24)) (GHz)</td>
<td>0.423</td>
<td>1.97</td>
<td>4.92</td>
</tr>
<tr>
<td>( f_{Fc=2 \text{ dB}} ) (eq. (3.25)) (GHz)</td>
<td>0.446</td>
<td>1.9</td>
<td>4.65</td>
</tr>
<tr>
<td>( L_e \text{ opt num. optimized} )</td>
<td>54.56</td>
<td>53.5</td>
<td>32.6</td>
</tr>
<tr>
<td>( s_{\text{opt (eq. (3.23))}} )</td>
<td>4.76</td>
<td>6.46</td>
<td>6.08</td>
</tr>
<tr>
<td>( L_e \text{ opt (eq. (3.28)) using } s_{\text{opt (eq. (3.23))}} )</td>
<td>60</td>
<td>57.3</td>
<td>30.4</td>
</tr>
</tbody>
</table>

In these figures, the analytical calculations neglect the emitter resistance \( R_e \). This can be noted in Figure 3.9 which is related to a modern device with a relatively high emitter resistance. Here, the constant difference in level between the two calculated noise factors is caused by the absence of \( R_e \) in our equations. If we, however, modify the value of the base resistance by adding the emitter resistance \( R_e \) to it, the resulting curve will coincide with the numerical simulation.
3.8 Further justification for the use of this Figure of Merit

It is interesting to know whether this Figure of Merit is also a measure of quality if the source impedance is not purely ohmic. We consider here a signal source that is purely capacitive (see Figure 3.10). This situation can be found in the case where a photodiode or capacitive sensor is the signal source.

\[ i_{tot} = u_{bn} Y_s + i_{bn}(r_b Y_s + 1) + i_{cn}(B_{ir} Y_s + D_{ir}(r_b Y_s + 1)) \]  \hspace{1cm} (3.29)

with:

\[ Y_s = j \omega C_s \]  \hspace{1cm} (3.30)

With a capacitive source, the use of the noise factor \( F \) is no longer convenient; it is more logical to transform the noise sources of the bipolar transistor to one single equivalent current noise source at the input. The value of this current noise source is given by:

\[ S(i_{tot}) = 4kT \left[ \left( \frac{r_b}{2} + \frac{r_e}{2} \right) + \frac{\omega^2 C_s^2}{\omega_T} + \frac{1}{2r_e} \left( \frac{1}{\beta} + \frac{\omega^2}{\omega_T^2} \right) \right] \]  \hspace{1cm} (3.31)

In wide-band amplifiers, one is interested in the equivalent noise current at the input for a given bandwidth \( f_2 \) and source capacitance \( C_s \). To obtain the equivalent noise current we integrate the noise spectrum over the bandwidth \( f_2 \) yielding:

\[ \overline{i_{tot}^2} = 4kT f_2 \left[ \frac{1}{3} \left( \frac{r_b}{2} + \frac{r_e}{2} \right) + \frac{\omega^2 C_s^2}{\omega_T} + \frac{1}{2} \frac{1}{2r_e} \left( 1 + \frac{1}{3} \omega^2 C_s^2 r_b^2 \right) + \frac{\omega^2}{2r_e^2} \frac{1}{5} \left( \frac{\omega^2 C_s^2 r_b^2}{3} \right) \right] \]  \hspace{1cm} (3.32)

The noise spectrum of equation (3.31) is plotted in Figure 3.11; the shaded area below the curve is a measure of \( \overline{i_{tot}^2} \).
The HF noise behaviour of bipolar transistors

![Figure 3.11. Spectrum of $S(i_{tot})$ of a bipolar transistor with a capacitive source](image)

Restricting ourselves to the dominant terms for the linear and quadratic region of the noise spectrum as depicted in Figure 3.11 (which is usually valid in the case of wide-band amplifiers) and scaling with respect to the emitter length using: $r_b \Rightarrow r_b / L_e$ and $\omega_T = 1 / (r_e L_e C_T + \tau_0)$ where $C_T = C_{TE} + C_{TC}$ we can reduce equation (3.32) to:

$$\frac{i_{tot}^2}{4kTf_2} = g_1 + g_2^2 r_e + \frac{h}{r_e}$$  \hspace{1cm} (3.33)

with:

$$g_1 = \frac{1}{3} \omega_s^2 C_s^2 \left[ \frac{r_b}{L_e} + \frac{\tau_0}{C_s} + \frac{L_e \tau_0 C_T}{C_s^2} \right]  \hspace{1cm} g_2^2 = \frac{1}{6} \omega_s^2 C_s^2 \left[ 1 + \frac{L_e C_T}{C_s} \right]^2  \hspace{1cm} h = \frac{1}{2} \left[ \frac{1}{\beta} + \frac{1}{3} \omega_s^2 \tau_0 \right]^2$$  \hspace{1cm} (3.34)

Optimizing $\frac{i_{tot}^2}{4kTf_2}$ with respect to the bias condition ($r_e$) and the scaling factor ($L_e$) we obtain (see appendix A):

$$\frac{i_{tot}^2}{4kTf_2} = \frac{1}{3} \omega_s^2 C_s^2 \left[ \tau_0 \left( 1 + \frac{1+3}{\beta \omega_s^2 \tau_0^2} \right) + 2 \sqrt{r_b C_T \tau_0 \left( 1 + \frac{1+3}{\beta \omega_s^2 \tau_0^2} \right)} \right]$$  \hspace{1cm} (3.35)

Equation (3.35) gives the equivalent noise current for a bipolar input stage with a capacitive source impedance optimized both for bias and geometry. Note that the expression found allows us to normalize for the capacitance, so that it is possible to define the equivalent noise current per pF for a given bandwidth. The equivalence noise current per pF for a bandwidth of 2 GHz has been calculated for a number of processes using equation (3.35), and plotted in relation to the results found for an ohmic source using equation (3.26) (see Figure 3.12). From this, we can conclude that the Figure of Merit as proposed is a real measure of quality for a given silicon process even when the source impedances are capacitive.

A similar approach can be used to inductive sources. In this case, however, optimization of the emitter length with respect to the noise behaviour tends to give a resonant solution for

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the input circuit, consisting of the source inductance and the depletion capacitances \(c_{TE}\) and \(c_{TC}\). This resonance, although useful in reducing the noise level will, in general, significantly deteriorate the transfer characteristic of the amplifier. For this reason, we find that a device optimized in bias and geometry for a purely inductive source is of limited interest in the wide-band amplifier case. A more detailed treatment is beyond the scope of this chapter.

**Noise Performance**
(bandwidth = 2 GHz)

![Noise Performance Graph](image)

Figure 3.12. Correlation in noise performance for optimized devices of different processes using a capacitive as well as an ohmic source impedance for a bandwidth of 2 GHz

### 3.9 Conclusions

A new Figure of Merit for the high-frequency noise behaviour of a bipolar transistor with optimum bias and emitter length has been presented. We have kept the expressions as compact as possible while taking into account all dominant parameters with respect to noise. When using the results, process technologies may be rated with respect to their high-frequency noise behaviour, without requiring full transistor parameter sets. This Figure of Merit for high-frequency noise behaviour can be useful to process developers and designers in assessing competing technologies.

As a final illustration, the progress in silicon process technology with respect to high-frequency noise behaviour is reviewed in Figure 3.13. \(F_{c 1=2 \text{ GHz}}\) has been plotted for processes from 1981 to the present. The introduction around 1982 of self-aligned bipolar process technology [3.15] resulted in a substantial decrease in the lowest achievable noise
factor for a given bandwidth. Self-aligning, which facilitates the use of smaller geometries in combination with other technological improvements, has led to considerable reductions in base resistance and depletion capacitances; the smaller lateral dimension and the availability of very shallow junctions facilitate the reduction of the delay time $\tau_0$. For the moment, performance is relatively stable, yielding a noise factor of below 1 dB at 2 GHz. Results for a number of recently described processes are listed in Table 3.2. We anticipate that the further maturation of silicon-germanium IC processes will lead to significant reductions in the noise factor.

The Figure of Merit for the high-frequency noise behaviour, as presented in [3.16] and extended in [3.17], has worked out to be an attractive measure for rating process technologies and is starting to be used by process developers. In [3.18] and [3.19], this Figure of Merit is used for rating the noise performance of a state-of-the art CMOS-compatible self-aligned double poly process technology (see Figure 3.13 process D), it yields a noise factor of only 0.8 dB at 2 GHz or, alternatively, a bandwidth of 7 GHz for a noise factor of 2 dB.

![Optimum noise factor](image)

**Figure 3.13.** High-frequency noise behaviour of silicon IC technology

<table>
<thead>
<tr>
<th>TABLE 3.2. Recent processes with their noise performance</th>
</tr>
</thead>
<tbody>
<tr>
<td>--------------------------------------</td>
</tr>
<tr>
<td>$F_{\text{c}(2\text{GHz})}$ (dB)</td>
</tr>
<tr>
<td></td>
</tr>
</tbody>
</table>
Appendix A) Optimization with respect to the bias condition and the scaling factor for a capacitive source impedance

Optimizing $\overline{i_{tot}^2}$ of equation (3.33) with respect to the bias condition ($r_b$) we find for $r_{eo opt}$:

$$r_{eo opt} = \frac{\sqrt{h}}{g_2}$$  \hspace{1cm} (3.36)

substitution of $r_{eo opt}$ in equation (3.33) yields:

$$\overline{i_{tot}^2} = \frac{1}{3} \omega \tau_0 C_s^2 \left[ \frac{\tau_0}{C_s} \left( 1 + \sqrt{1 + \frac{3}{\beta \omega \tau_0^2}} \right) + \frac{r_b}{C_T L_e} \frac{C_T}{C_s} \left( 1 + \frac{1}{\sqrt{1 + \frac{3}{\beta \omega \tau_0^2}}} \right) \right]$$  \hspace{1cm} (3.37)

which leads in turn to the following optimum for $L_{eo opt}$:

$$L_{eo opt} = C_s C_T \frac{r_b C_T}{\sqrt{\tau_0 \left( 1 + \sqrt{1 + \frac{3}{\beta \omega \tau_0^2}} \right)}}$$  \hspace{1cm} (3.38)

Substitution of $L_{eo opt}$ in equation (3.37) results in equation (3.35).

3.10 References


The HF noise behaviour of bipolar transistors


Chapter 4  Compact models for the bipolar transistor

4.1 Introduction

With the invention of the bipolar transistor at Bell Laboratories in 1947, one of the most important semiconductor devices was introduced. It triggered an endless chain of improvements in process technology and device performance, which ultimately led to today's integrated circuits with high-performance devices with respect to power and frequency handling. This level of development which makes possible complex circuits that operate at high frequencies, has resulted in a need for accurate compact models, to enable the designer to fully explore the possibilities of the available process technology. Historically, we can distinguish the following models:

- Ebers-Moll (EM),
- Gummel-Poon (GP),
- Extended Gummel-Poon (Kull extension), VBIC95,
- Mextram.

In the order of their appearance an increasing number of electrical effects were included in the above models, this improved their accuracy, but also led to an increase in model complexity and number of parameters. In general, a more advanced transistor model requires a longer computation time and parameter extraction is more difficult. However, faster computers and the use of sophisticated parameter extraction software and measurement protocols, alleviate the disadvantages of the use of sophisticated models. In high-frequency analog design, the engineer tends to choose the model that most accurately meets his circuit specifications without the necessity for redesign.

In this chapter at the time of writing we discuss the most commonly
used bipolar transistor models. For each model we give its main features and disadvantages. In order to facilitate a side-by-side comparison of the different models, we give a tabular overview of the formulation and the required parameters. It is beyond the scope of this thesis to give the full physical background of the electrical effects modelled; for those interested in this subject, we refer to [4.21].

4.2 Circuit representation, node numbering and parameters

In order to make a clear comparison between the various bipolar transistor models treated in this chapter, we need some standardization in the graphical circuit representation, node numbering and model parameters. All equivalent circuits of the transistor models are given with the emitter on the left, collector on the right and base at the bottom. Further, we use in this thesis the SPICE [4.16] implementation for the definition of the Ebers-Moll and Gu-mel-Poon models. The parameters of the EM, GP and extended GP (VBIC95) models are according to the SPICE 2G version and are listed in Table A.1. For the Mextram model we use the 503.2 version as given in the implementation guide [4.23]. The parameters for this model are listed in Table B.1.

Node numbering

In the figures and formulas of this chapter we use the following notation for the node numbering:

- External nodes: c, b, e, s for respectively the collector, base, emitter and substrate connection.
- Internal/intrinsic nodes: c1, b1, e1, and s1 are used for respectively the internal collector, base, emitter and substrate nodes. In the absence of an extended modelling of the base and collector regions (as in the Ebers-Moll model) these nodes can be considered to be connected to the intrinsic device.
- Intrinsic nodes: c2, b2 and b3 are connected to the intrinsic collector, the base and the base of the parasitic pnp when extended modelling of the base, collector and substrate regions is included in the transistor model (see e.g. VBIC95).

4.3 The Ebers-Moll model

The basic model for the bipolar transistor is the Ebers-Moll model [4.1]; it was originally only a static (DC) model. Extension of the basic Ebers-Moll (EM) model has resulted in a simple but fast compact model, suitable for the simulation of large digital circuits. The Ebers-Moll model treated in this thesis is based on the SPICE implementation (see Figure 4.1) and includes the following features:

**Characteristics of the Ebers-Moll model**

- Simple and fast.
- Network topology with 3 internal nodes (c1, b1 and e1).
- Constant emitter, base and collector series resistance (Rc, Rb and Re).
- Forward and reverse components of the main current modelled by ideal exponential functions; no high-injection effects.
- Only forward Early effect modelled, with a constant Early voltage (VAF).
- Only ideal base currents \( I_{be} \) and \( I_{bc} \) modelled with constant current gains \( B_F \) and \( B_R \).
- Diffusion capacitances with the stored minority carrier charges, given by the charge-control concept are modelled with constant forward and reverse delay times \( \tau_F \) and \( \tau_R \).

- The depletion charges \( Q_{te} \) and \( Q_{tc} \) are derived from the capacitance formula

\[
C = C_i \left(1 - \frac{V}{V_j}\right)^m
\]

the singularity at \( V=V_j \) is circumvented by a linear continuation at \( V=F_C V_j \) (with \( F_C<1 \)).

![Ebers-Moll model diagram](image)

**Figure 4.1.** The Ebers-Moll model according to the SPICE implementation

The formulations of the nonlinear current sources \( I_n \), \( I_{be} \) and \( I_{bc} \) are given in Table 4.1, “Overview current formulation intrinsic device and base-emitter sidewall component,” on page 60. The formulation of the diffusion charges \( Q_{de} \) and \( Q_{dc} \) and the depletion charges \( Q_{te}, Q_{tc} \) are given in Table 4.4 and 4.5.

**Shortcomings Ebers-Moll model**

Although it has the advantage of a very short calculation time, the Ebers-Moll model lacks a proper representation of a number of important second-order effects present in modern devices. Namely:

- No low and high-current \( \beta \) fall-off: At low current levels, the recombination in the emitter-base junction lowers the effective DC current gain. At high-current levels, current gain degradation can take place due to high-level injection (also called the Kirk effect [4.3]) or quasi-saturation (also called base push-out).
- Constant delay times \( \tau_F \) and \( \tau_R \)

**Conclusions Ebers-Moll model**

Because of its short calculation time and its low memory requirements, the Ebers-Moll model is perfectly suited to use for the simulation of large digital circuits which operate at low to medium switching speed in respect to the transistor cut-off frequency. It is assumed that the transistor is biased at moderate current conditions. For designs operating at high-current levels or frequencies, the model tends to be over-optimistic in its predictions of the performance.
4.4 The Gummel-Poon model

The Gummel-Poon model [4.8] is based on an extension of the Moll-Ross relation [4.2], which includes the integral charge-control concept. This concept uses the charge $Q_d$ which represents the total majority carriers in the neutral base region. By using the integral charge-control concept, a number of physical phenomena are naturally included in the model definition (e.g., high-level injection and the forward and reverse Early effect). The schematic diagram of the Gummel-Poon model is given in Figure 4.2. The characteristics of the Gummel-Poon model are listed below:

**Characteristics of the Gummel-Poon model**

- More complex than EM and somewhat slower.
- Network topology with 3 internal nodes.
- Constant emitter and collector resistance; the base resistance is current-dependent, modelling the emitter current crowding effect or the conductivity modulation.
- The exponential functions for the forward and reverse components of the main current have non-ideality factors ($N_F$ and $N_R$).
- Both forward and reverse Early effects modelled, with constant Early voltages ($V_{AF}$ and $V_{AR}$).
- The main current includes high-injection effects in the base.
- The base current has, besides the ideal, also nonideal components, with nonideality factors $N_E$ and $N_C$ and saturation leakage currents $I_{SE}$ and $I_{SC}$. The current gain is thus bias dependent.
- The reverse diffusion charge has a constant $\tau_R$ whereas the delay time $\tau_F$ for the forward diffusion charge is bias dependent.
- The depletion charges are modelled as in the EM model, but $C_{tc}$ is split up into an internal part $X_{CJC}.C_{JC}$ and an external part ($1-X_{CJC}).C_{JC}$. The substrate depletion capacitance is also modelled.
- The collector current has an additional excess phase shift term to account for the extra delay at high frequencies.

![Figure 4.2. The Gummel-Poon model](image-url)
The implementation of the current formulation of GP model is given in Table 4.1, "Overview current formulation intrinsic device and base-emitter sidewall component," on page 60. It can be seen that in comparison with the EM model, the nonideal base currents have been added and that the formulation of the normalized base charge \( q_b \) is extended to take into account the reverse Early and the high-level injection effects.

In the Gummel-Poon model, the \( f_T(I_C) \) characteristic is approximated by modifying the forward transit time. In the low and medium current range \( \tau_{for} \) is assumed to be constant, at the high-current region \( \tau \) becomes a function of the base-collector voltage and the collector current. There are three parameters affecting the increase in \( \tau_{for} \), namely: \( X_{TF} \) controls the total fall-off of the \( f_T \) characteristic, \( V_{TF} \) gives the dependency with respect to \( V_{BC} \) and \( I_{TF} \) deals with the dependency on the collector current. It must be noted that formulation of \( \tau_{for} \) in the GP model is more curve-fitting in nature than based on actual device physics. The formulation of \( \tau_{for} \) is given in Table 4.4 on page 64. Because the depletion and diffusion charge components are not used in the definition of the main current \( I_n \), one can say that in the GP model the DC and AC characteristics are more or less uncoupled. This gives greater freedom in the parameter extraction, but can result in a nonphysical parameter set which is not suitable for proper scaling of the transistor.

**Shortcomings Gummel-Poon model**

The main shortcomings in the Gummel-Poon model are:
- Early voltages constant.
- No quasi-saturation.
- Curve-fitting nature of \( f_T \) fall-off.
- Poor modelling of substrate effects.
- Poor scaling.
- No avalanche effects.
- Poor temperature scaling.

**Conclusions**

By using the integral charge control concept, a number of second-order effects like the forward and reverse Early effect, high injection etc. are naturally included in the Gummel-Poon model. Although the basic derivation of the Gummel-Poon model (like the Ebers-Moll model) assumes a one-dimensional transistor structure, it includes two-dimensional effects related to the distributed nature of the base. The implementation of these two-dimensional effects in the GP model yields an improved modelling of the base-resistance [4.4], high frequency current crowding effect and a distributed base-collector capacitance. In comparison with the EM model, the modelling of the base-resistance is greatly improved, but only current crowding or base conductivity modulation is taken into account. The combined effect is not modelled.

In spite of some shortcomings, it is clear why the GP model has long been the favourite of many designers, it includes many electrical effects in a relative simple manner. However, the increasing demands on telecommunications circuits, like highly efficient power output stages operating at low supply voltages, requires a more correct modelling of the collector epilayer.
4.5 Extended Gummel-Poon / Kull model / VBIC95

If we implement a voltage-dependent current source in the collector branch of the GP model for the modelling of the epilayer, by using, e.g., the epilayer formulation given by Kull, we obtain after the addition of the parasitic pnp transistor (nnp case) the Extended Gummel-Poon model (see Figure 4.3) which is in use in a number of circuit simulators. The main purpose of this model is for the analogue design of integrated circuits.

As can been seen from Figure 4.3, the extended GP model as proposed by Kull includes, in fact, two complete transistors, the active npn and the parasitic pnp modelling the substrate interface. Both transistors consist of a GP model itself, although there is some neglect of the parasitic pnp. This is illustrated by Figure 4.4, which gives the schematic of the VBIC95 model. The VBIC95, which is strongly based on the work of Kull [4.15], has been recently proposed as a new “standard” transistor model by a number of semiconductor industries. The characteristics of the VBIC95 model are:

Characteristics of the VBIC95 model

- More complex than GP and slower.
- Network topology with 7 internal nodes.
- Constant emitter resistance; the base resistance is current-dependent, modelling the base conductivity modulation; the emitter current crowding effect is modelled to a first-order approximation by the splitting of the base current into a side wall and a main component.
- Modelling of the collector epilayer resistance (according to [4.34]).
- The exponential functions for the forward and reverse components of the main current have non-ideality factors ($N_F$ and $N_R$).
- Dynamic forward and reverse Early voltages based on the junction charges [4.30].
- The main current includes high-injection effects in the base formulated as in GP.
- The base current has besides the ideal also nonideal components that are uncoupled from the collector current.
- The reverse diffusion charge has a constant $\tau_R$, whereas the delay time $\tau_F$ for the forward diffusion charge is bias dependent, formulation similar to that in GP but now also the dependency of the Early effect has been added.
- The depletion charges are default modelled as in the GP model, but can be replaced by a single piece model [4.26].
- Excess phase shift similar to GP by means of separate subcircuit.
- Parasitic substrate pnp.
- Weak avalanche.

---

1. Note that there is an extra substrate resistor added to the model as presented by Kull [4.15], this addition has be made to obtain the same node numbering as in the VBIC95 model (see Figure 4.4).
Figure 4.3. Circuit of the extended Gummel-Poon model (Kull extension)

The implementation of the current formulation of the VBIC95 model is given in Tables 4.1. to 4.7. It can be seen from Table 4.1 that in comparison to the GP model, the base currents are no longer directly related to the collector current and that an alternate formulation of the normalized base charge \( q_b \) has been used in order to obtain dynamic Early voltages.

Shortcomings VBIC95 model

- Complicated circuit structure that involves many (7) internal nodes and circuit elements.
- For the full model, a clear and unified parameter extraction will be impossible.
- Incorrect epilayer model.
- Limitations in the modelling of lightly doped epilayers resulting in nonmonotonic Early voltages and \( f_T(I_c) \) behaviour at the onset of \( q_s \).
- Incorrect modelling of the Early effect in the presence of high injection.
- No AC current crowding.
- Constant reverse delay time \( \tau_R \).
- Uncoupled DC and AC behaviour.
- Incorrect modelling of distortion at high frequency and current levels.
Figure 4.4. Circuit of the VBIC95 model

Conclusions

The VBIC95 model seems to be heavily supported, however, the model still looks unfinished. In its full definition with seven internal nodes, it demands considerable memory and computation time when applied in a harmonic balance simulation. The use of an almost complete GP model for the modelling of the parasitic pnp necessitates circuit elements with many parameters which purpose is unclear, e.g. the modulated nonlinear base resistance in the parasitic pnp. Although the benefits of including the modelling of the collector epilayer are clear, this should be done in a more careful way. The implementation as given in [4.34] results in a non-physical behaviour when going deeper in q.s. Furthermore the absence of an extra charge ($\Delta Q_C$) in the formulation of $Q_{bc}$ will lead to non-monotonic Early voltages and $f_T(I_C)$ behaviour at the onset of q.s. for transistors with a lightly doped epilayer (see Chapter 6). It has been shown [4.37] that the modelling of the Early effect under high current conditions is incorrect (see “Early effect” on page 59). The constant reverse delay time $\tau_{R_c}$ can lead to difficulties in modelling the fall-off of the $f_T(I_C)$ characteristic. Finally, the absence of the modelling of AC current crowding can lead to inaccurate results for the $y_{11}$ parameter [4.22].

The great advantage of this model is that it reduces to the basic Gummel-Poon model as parameters are left out, which makes the acceptance easier for a wider public. In this
respect it is a pity that compatibility with respect to the Early voltages $V_{AR}$ and $V_{AF}$ has been lost.

4.6 The Mextram Model

The Mextram model [4.23] was developed by de Graaff and Kloosterman and it incorporates a long list of modelled effects. This strongly physics-based transistor model has been recently placed in the public domain by Philips as candidate for the new standard bipolar transistor model, and it provides, for a compact model, an unmatched accuracy in the modelling of the bipolar transistor. This and the implementation of the model in HP's microwave design system (MDS), makes the model very interesting to the high-frequency designer. The circuit of the Mextram model is given in Figure 4.5. The characteristics of the Mextram model are:

Characteristics of the Mextram model

- More complex than GP and slower, but with reduced circuit complexity compared to the full VBIC95 model.
- Network topology with 5 internal nodes.
- Constant emitter resistance; the base resistance is current dependent, modelling the emitter current crowding effect and conductivity modulation.
- Modelling of the collector epilayer resistance by the physical formulation of [18], including hot carrier behaviour and current spreading.
- The exponential functions for the forward and reverse components of the main current have no nonideality factors.
- Monotonic bias-dependent forward and reverse Early effect.
- The main current includes high-injection effects in the base.
- The base current has, in addition to the ideal, also nonideal components, formulation [4.21] p. 57.
- Bias-dependent delay times $\tau_R$ and $\tau_F$
- The depletion charges are modelled by a non-segmented solution, the base-emitter capacitance is split up into an intrinsic part and a side wall component, the base-collector capacitance takes into account the finite thickness of the epilayer and current modulation.
- Excess phase shift by base-charge partitioning.
- High frequency current crowding.
- Parasitic substrate pnp.
- Weak avalanche.
- Built-in electric field in base region.
- Monotonic Early voltages and $f_T(I_B)$ behaviour [4.36] for lightly doped epilayer devices and, consequently, improved modelling of signal distortion when entering the quasi-saturation region.
- Extensive temperature modelling.
Figure 4.5. The Mextram model

The implementation of the current formulation of Mextram is given in Tables 4.1 to 4.7. It can be seen from Table 4.1 that the current formulation results in bias-dependent Early voltages which are related to the physical quantity $Q_{BO}$ (this in contrast to VBIC95).

Monotonic $f_T(I_C)$ behaviour and improved modelling of distortion

Improved bipolar models with an epilayer extension like Ext. GP and Mextram are particularly sensitive to their epilayer parameter values; slight deviations may produce erratic, non-monotonic Early voltages and $f_T(I_C)$ behaviour. In practice, their parameter sets, especially $V_{DC}$ are extracted so as to obviate this deleterious behaviour, but this results in improper modelling of nonlinear distortion [4.31] at high-current levels. We analyse this phenomena in Chapter 6 and solve this problem by adding an extra storage charge ($\Delta Q_C$) to the base-collector junction. This combined with a modification of the collector-base depletion capacitance leads to monotonic Early voltages and $f_T(I_C)$ behaviour and an improved modelling of nonlinear distortion when the transistor enters the q.s. region.

Shortcomings Mextram model

- Inflexible in base current definition.
- Parameters differ from the GP ones.
- Difficult to understand due to physical nature.
Conclusions

It must be noted that the Mextram model does not reduce to the standard GP model as parameters are omitted. In contradiction with GP, the Mextram formulation includes a direct coupling between the current and charge model which leads to a coupled DC and AC behaviour (see Table 4.1 and Table 4.4) This coupling makes the parameter extraction somewhat more complex because the different phenomena like $\beta$ roll-off and $f_T(l_c)$ roll-off cannot be treated separately. However, this has the advantage that when the correct parameter set is found, which can be done fully automatically as demonstrated in [4.33], a physical representation of the device is found which allows an accurate scaling [4.24].

4.7 Formulation of the standard transistor models

In order to make a side by side comparison of the formulation of the different transistor models possible, we have provided a tabular overview of the definitions of the currents in the intrinsic device, the diffusion and depletion charges, the extrinsic parts and the modelling of the epilayer. Where useful, a graphical representation of the different model functions is added. In a second stage, we compare the different models with the measured data of a real device. In this comparison, we concentrate on the $\beta$ trace, $I_C(V_{ce})$ and the $f_T(l_c)$ characteristics.

4.7.1 Definition of the currents in the intrinsic transistor

The definition of the collector and the base currents for the intrinsic transistor is given below in Table 4.1.

Early effect

From Table 4.1 it is clear that the collector current in all the models is based on Moll-Ross [4.2]. In both the GP and VBIC95 models, Moll-Ross is rewritten in the well-known integral charge formulation as proposed by [4.8]. Note that the Spice implementation of the GP model uses a simplification of the original definition of $q_0$, this simplification combined with the use of constant Early voltages separates the effect of $q_1$ and $q_2$. This separation contributes to slightly more $\beta$ roll-off at high collector current and ensures that the Early effect remains present at high-injection conditions. The inaccuracy introduced by static Early voltages, is circumvented in the VBIC95 model by using the depletion charges $Q_{te}$ and $Q_{tc}$ in the definition of $q_1$, leading to dynamic Early voltages [4.30]. VBIC95's use of the original integral charge formulation [4.8] neglects the Early effect for high-level injection. In this case $q_2$ will dominate the expression for $q_0$ completely. The Mextram model employs the original bias-dependent Early effect modelling as proposed by Moll-Ross. In contrast with the VBIC95 formulation the diffusion charges $Q_{de}$ and $Q_{dc}$ include $q_1$, so that the Early effect is also present under high injection conditions. The Mextram formulation uses the base charge at zero bias ($Q_{B0}$) instead of two independent parameters ($V_{EF}, V_{ER}$) for the modelling of the Early effect.

Note that modelling of the Early effect is limited to outside the q.s. region. The modelling of the Early effect within the q.s. region is discussed in Chapter 6.
<table>
<thead>
<tr>
<th>Ebers-Moll</th>
<th>Gummel-Poon</th>
<th>VBIC95</th>
<th>Mextram</th>
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<tbody>
<tr>
<td><strong>main current</strong></td>
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<tr>
<td>general current function: $I(I_{sat}, V_f, N) = I_{sat} \left(\exp\left(V_{IF}\right) - 1\right)$</td>
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<tr>
<td>$I_n = \frac{I_f - I_r}{q_b}$</td>
<td>$I_n = \frac{I_f - I_r}{q_b}$</td>
<td>$I_n = \frac{I_f - I_r}{q_b}$</td>
<td>$I_n = \frac{I_f - I_r}{q_b}$</td>
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<tr>
<td>$I_f = I(I_S, V_{b1e1}, 1)$</td>
<td>$I_f = I(I_S, V_{b1e1}, N_F)$</td>
<td>$I_f = I(I_S, V_{b2e1}, N_F)$</td>
<td>$I_f = I(I_S, V_{b2e1}, 1)$</td>
</tr>
<tr>
<td>$I_r = I(I_S, V_{b1c1}, 1)$</td>
<td>$I_r = I(I_S, V_{b1c1}, N_R)$</td>
<td>$I_r = I(I_S, V_{b2c1}, N_R)$</td>
<td>$I_r = I(I_S, V_{b2c1}, 1)$</td>
</tr>
<tr>
<td>$q_b = q_1$</td>
<td>$q_b = q_1 + \sqrt{1 + 4q_2}$</td>
<td>$q_b = q_1 + \sqrt{\frac{q_1^2 + 4q_2}{2}}$</td>
<td>$q_b = q_1 + q_2'$</td>
</tr>
<tr>
<td>$q_1 = \frac{1}{V_{b1c1} - V_{AF}}$</td>
<td>$q_1 = \frac{1}{1 - \frac{V_{b1c1}}{V_{AF}} - \frac{V_{b1c1}}{V_{AR}}}$</td>
<td>$q_1 = 1 + \frac{Q_{le}}{C_{JE}V_{EF}} + \frac{Q_{ic}}{C_{JC}V_{EF}}$</td>
<td>$q_1 = 1 + \frac{Q_{le} + Q_{ic}}{Q_{B0}}$</td>
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<tr>
<td>$q_2 = \frac{I_f}{I_{KF}} + \frac{I_r}{I_{KR}}$</td>
<td>$q_2 = \frac{I_f}{I_{KF}} + \frac{I_r}{I_{KR}}$</td>
<td>$q_2' = \frac{Q_{de} + Q_{dc}}{Q_{B0}}$</td>
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<tr>
<td><strong>base currents</strong></td>
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<tr>
<td>$I_{bei} = \frac{I_f}{B_F}$</td>
<td>$I_{bei} = \frac{I_f}{B_F} + I(I_{SE}, V_{b1e1}, N_E)$</td>
<td>$I_{bei} = W_{BE}(I(I_{BE}, V_{b2e1}, N_E) + I(I_{BEM}, V_{b2e1}, N_E))$</td>
<td>$I_{bei} = (1 - X_{BE})(\frac{I_f}{B_F}) + \frac{I(I_{BE}, V_{b2e1}, 1)}{\exp(V_{b2e1}/2V_F) + \exp(V_{IF}/2V_F)}$</td>
</tr>
<tr>
<td>$I_{bei} = (1 - W_{BE})(I(I_{BE}, V_{b1e1}, N_E) + I(I_{BEM}, V_{b1e1}, N_E))$</td>
<td></td>
<td></td>
<td>$I_{bes} = X_{BE}I(I_{BE}, V_{b1e1}, 1)$</td>
</tr>
<tr>
<td>$I_{bei} = \frac{I_r}{B_R}$</td>
<td>$I_{bei} = \frac{I_r}{B_R} + I(I_{SC}, V_{b1c1}, N_C)$</td>
<td>$I_{bei} = I(I_{BC}, V_{b2c1}, N_C) + I(I_{BCN}, V_{b2c1}, N_{CN}) + I_{AVL}$</td>
<td>$I_{bei} = I_{AVL}$</td>
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</table>
Base currents

In the EM and GP models, the ideal base currents are coupled to the collector current by their current gain parameters. This is the same for the base-emitter current in the Mextram model. In the VBIC95 model, however, the ideal base currents are decoupled from the collector current by the use of separate saturation currents constants \( I_{BEi} \) and \( I_{BCi} \) and non-ideality factors \( N_{EI} \) and \( N_{CI} \). This results in greater flexibility but also in four extra parameters.

Note that in the Mextram model, the reverse base current \( (l_{b3} + l_{ex}) \) is placed outside the intrinsic device; this is closer to reality when considering vertical npn's. Its formulation is given in Table 4.3 which considers the modelling of the extrinsic regions and the parasitic pnp.

4.7.2 Modelling of the extrinsic region

The extrinsic region is absent in the EM and the GP models, so only the VBIC95 and Mextram models are considered. In these two models, two different philosophies can be recognized, namely:

- The intention of the VBIC95 model is to use an almost complete separate transistor model for the modelling of the parasitic pnp. This results in two extra nodes and seven extra parameters when comparing with the Mextram model. The effects modelled in the VBIC95 model are: a main current affected by high injection, base currents for both junctions with ideal and nonideal components but without high-injection effects. Further, a modulated base resistance for the parasitic pnp and a substrate resistance have been added.

- The Mextram model is much more pragmatic in the modelling of the extrinsic regions. It concentrates on the desired, improved modelling of the extrinsic regions for devices under normal operation (collector-substrate junction reversed bias). With almost no increased circuit complexity and extra parameters, a great number of relevant effects are included. The Mextram model takes into account an ideal reverse base current \( (l_{ex}) \) which is affected by high injection and can be partitioned over two external base-collector branches. The nonideal reverse base current is given by \( l_{b3} \). The forward main current of the parasitic pnp also takes into account high injection and is the combination of the currents \( l_{sub} \) and \( l_{xsub} \). Also the diffusion and depletion charge functions are more sophisticated than those in the VBIC95 model (see Table 4.4 and Table 4.5), because they include the effects of high-current injection and the finite thickness of the epilayer. A simple diode current function is implemented \( (l_{df}) \) to indicate the situation that the collector-substrate junction becomes forward biased.
### TABLE 4.2. Useful functions for the Mextram model

<table>
<thead>
<tr>
<th>parameter-dependent constants</th>
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<tbody>
<tr>
<td>( a_{bl} = \exp(-\eta) ), ( a_{bh} = 2 \frac{1 - \exp(-\eta)}{\eta} ), ( b_{bh} = 1 \frac{1 - \exp(-\eta)}{\eta} ), ( b_{bl} = \frac{(1 - \eta)(1 - a_{bl})}{(1 - a_{bl})^2} ), ( b_{bl} = \frac{(1 - (\eta + 1))a_{bl}}{(1 - a_{bl})^2} )</td>
</tr>
</tbody>
</table>

(needed for the calculation of the currents in the parasitic pnp and diffusion charges see Tables 4.3 and 4.4)

| \( q_e = \frac{2 + \eta - (2 - \eta) \exp(\eta)}{2 - \eta - (1 - \eta) \exp(\eta) - \exp(-\eta)} \) |

(needed for the base-charge positioning see Table 4.6)

| \( Q_{Q_{NO}} = \tau_{NE}\exp(\gamma) \) |

(needed for the calculation of \( Q_{ne} \) see Table 4.4)

<table>
<thead>
<tr>
<th>useful functions</th>
</tr>
</thead>
<tbody>
<tr>
<td>( f_4(x) = 4I_{SP}^{1/2} \exp(\frac{V}{V_t}) ), ( f_3(x) = 4 \exp(\frac{x - V_{DC}}{V_t}) ), ( f_3 = \frac{R_{CV}I_{SP}}{V_{DC}} \exp(\frac{V_{DC}}{V_t}) )</td>
</tr>
<tr>
<td>( g(x) = \frac{x}{2(1 + \sqrt{1 + x})} ), ( h(x) = \frac{a_{bl} \cdot b_{bh} + x}{a_{bl} \cdot b_{bl} + x} ) ( h_{bh} = a_{bl} \cdot \frac{f_4(x)}{a_{bl}^2} )</td>
</tr>
</tbody>
</table>

### TABLE 4.3. Currents parasitic pnp

<table>
<thead>
<tr>
<th>VBIC95</th>
<th>Mextram</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Main currents extrinsic region</strong></td>
<td><strong>Main currents extrinsic region</strong></td>
</tr>
<tr>
<td>general current function: ( I_{sat}(V_p, N) = I_{sat}(\exp(\frac{V_p}{V_t}) - 1) )</td>
<td>( I_{np} = \frac{I_{fp} - I_{rp}}{q_{bp}} )</td>
</tr>
</tbody>
</table>
| \( I_{fp} = W_{sp}(I_{sp}, V_{h13}, N_{FP}) + I_{sp} \) | \( I_{np} = \frac{I_{sp}(V_{h13}, 1)}{q_{bp}}(1 - X_{EXT}), \)
| \( I_{sp} + (1 - W_{sp})(I_{sp}, V_{h2c}, N_{FP}) \) | \( I_{sat} = F_E(V_{sat}) \frac{I_{sp}(V_{h13}, 1)}{q_{bp}}X_{EXT} \)
| \( I_{rp} = I(I_{SP}, V_{h13}, N_{FP}) \) | \( F_E(V_{sat}) \) limits the conductivity of this branch to \( I/R_C \) |

| \( q_{bp} = \frac{1 + 4 \sqrt{1 + \frac{I_{fp}}{I_{KP}}}}{2} \) | \( q_{bp} = \frac{1 + 4 \sqrt{1 + \frac{I_{sp}(V_{h13}, 1)}{I_{sp}(V_{h13}, 1)}}}{2} \) |

---

HF Silicon Modelling
### TABLE 4.3. Currents parasitic pnp

<table>
<thead>
<tr>
<th>VBIC95</th>
<th>Mextram</th>
</tr>
</thead>
<tbody>
<tr>
<td>Reverse base current</td>
<td></td>
</tr>
<tr>
<td>$I_{bep} = I_{BEIP} \left( \exp \left( \frac{V_{bip}}{N_{CIP}V_{T}} \right) - 1 \right)$</td>
<td>$I_{ex} = \left( 1 - \frac{X_{EXT}}{B_{RI}} \right) \frac{I_{E}}{a_{h} \cdot n(V_{bcl})} \frac{I_{K}}{a_{h} \cdot n(V_{bcl})} - I_{S}$</td>
</tr>
<tr>
<td>$I_{BENP} \left( \exp \left( \frac{V_{bnp}}{N_{CNP}V_{T}} \right) - 1 \right)$</td>
<td>$I_{sec} = I_{ES} \left( \frac{X_{EXT}}{B_{RI}} \frac{I_{E}}{a_{h} \cdot n(V_{bcl})} a_{h} \cdot n(V_{bcl}) - I_{S} \right)$</td>
</tr>
<tr>
<td>Collector-substrate junction</td>
<td></td>
</tr>
<tr>
<td>$I_{bcp} = I_{BCIP} \left( \exp \left( \frac{V_{bic}}{N_{CIP}V_{T}} \right) - 1 \right)$</td>
<td>$I_{b3} = \frac{I_{BR} \left( \exp \left( \frac{V_{bic}}{V_{T}} \right) - 1 \right)}{\exp \left( \frac{V_{bic}}{2V_{T}} \right) + \exp \left( \frac{V_{BR}}{2V_{T}} \right)}$</td>
</tr>
<tr>
<td>$I_{BCNP} \left( \exp \left( \frac{V_{bic}}{N_{CNP}V_{T}} \right) - 1 \right)$</td>
<td></td>
</tr>
<tr>
<td>$I_{c1b3} = \frac{q_{b3}}{q_{B}}$</td>
<td>$I_{sf} = I_{SS} \left( \exp \left( \frac{V_{asc}}{V_{T}} \right) - 1 \right)$</td>
</tr>
</tbody>
</table>

#### 4.7.3 Diffusion charge formulation

The formulation of the diffusion charges is given in Table 4.4, but some of the functions used for the Mextram model are defined in Table 4.2. One of the major differences in the model definition between Mextram and GP / VBIC95 is the definition of the diffusion charges. The Mextram charge definitions are based on [4.14] which relates the current and charges to the injected minority carrier concentrations in the base. When using this formulation the transit time is no longer a parameter but is implicitly defined. As a consequence, bias-dependent current gain, current-dependent transit time and the effect of built-in electric field in the base are included. In Figure 4.6, the influence of the built-in electric field in the base is illustrated (for reasons of simplicity we ignore here the influence of the Early effect). If no built-in electric field is present $\eta = 0$, then $Q_{de}$ has the same junction voltage dependency as $Q_{dc}$. For $\eta > 0$ $Q_{de}$ lowers and $Q_{dc}$ rises in normal operation (base-collector junction reverse biased). This leads to an improvement of the high-frequency performance of the transistor. In Figure 4.6, also the high injection can clearly be noted from the change in slope of $Q_{de}$ and $Q_{dc}$.

The diffusion charge $Q_{dc}$ in the VBIC95 model, is calculated based on the product of the fixed delay time $\tau_{R}$ and the reverse current $I_{r}$. When the transistor enters q.s. this combination, which neglects high injection effects, significantly influences $Q_{dc}$ which can cause difficulties in modelling the $\tau_{R}(I_{r})$ roll-off [4.37].
### Table 4.4. Overview diffusion charge formulation compact bipolar models

<table>
<thead>
<tr>
<th>Ebers-Moll</th>
<th>Gummel-Poon</th>
<th>VBIC95</th>
<th>Mextram</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>base-emitter diffusion charges</strong></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$Q_{de} = \tau_f I_f$</td>
<td>$Q_{de} = \tau_{for} I_f$</td>
<td>$Q_{de} = \tau_{for} I_f$</td>
<td>$Q_{dc} = Q_{bo} q_{1} b h 0 \cdot g(f_1(V_{b2c2}))$</td>
</tr>
<tr>
<td>$\tau_{for} = \tau_f \left( 1 + X_T F \left( \frac{I_f}{I_f + I_{TP}} \right) \right)^2$</td>
<td>$\tau_{for} = \tau_f(1 + Q_{TP} q_{1}) \left( 1 + X_T F \left( \frac{I_f}{I_f + I_{TP}} \right) \right)^2$</td>
<td></td>
<td>$\frac{(1/2 + \frac{a h 0}{4} + g(f_1(V_{b2c1}))}{(1/2 + \frac{a h 0}{4} b h 0) + g(f_1(V_{b2c1}))}$</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>$Q_{dc} = Q_{bo} q_{1} b h 0 \cdot g(f_1(V_{b2c1}))$</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>$\cdot \exp \left( \frac{V_{b2c1}}{1.44V_{TP}} \right)$</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>$\cdot \exp \left( \frac{V_{b2c1}}{1.44V_{TP}} \right)$</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>$\left( \frac{1/2 + \frac{a h 0}{4} + g(f_1(V_{b2c1}))}{(1/2 + \frac{a h 0}{4} b h 0) + g(f_1(V_{b2c1}))}$</td>
</tr>
<tr>
<td><strong>base-collector diffusion charges</strong></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$Q_{dc} = \tau_R I_r$</td>
<td>$Q_{dc} = \tau_R I_r$</td>
<td>$Q_{dc} = \tau_R I_r$</td>
<td>$Q_{dc} = Q_{bo} q_{1} h \left( \frac{alb \cdot g(f_1(V_{b2c2}))}{alb^2} \right)$</td>
</tr>
<tr>
<td>$Q_{dep} = \tau_R I_{fp}$</td>
<td></td>
<td></td>
<td>$Q_{dc} = Q_{bo} q_{1} h \left( \frac{1 - X_{CJC}}{X_{CJC}} \right) f_{3} \cdot g(f_{2}(V_{b1c1})) + h(n(V_{b1c1}))$</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>$Q_{dc} = Q_{bo} q_{1} h \left( \frac{1 - X_{CJC}}{X_{CJC}} \right) f_{3} \cdot g(f_{2}(V_{b1c1})) + h(n(V_{b1c1}))$</td>
</tr>
<tr>
<td><strong>epilayer diffusion charges</strong></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$Q_{epi} = Q_{CO} K_0 (V_{b2c2})$</td>
<td></td>
<td>$Q_{epi} = I_s Q_{bo} \left( \frac{\exp \left( \frac{V_{b2c2}}{V_t} \right) - \exp \left( \frac{V_{b2c1}}{V_t} \right)}{I_{c1c2}} \right)$</td>
<td></td>
</tr>
<tr>
<td>$Q_{epix} = Q_{CO} K_0 (V_{b2c1})$</td>
<td>(see Table 4.7 for the formulation of $K_0$ and $K_W$)</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
Compact models for the bipolar transistor

\[ Q \text{ (f Coul.)} \]

\[ V_j \text{ (V)} \]

\[ Q_{dc} (\eta=0.01) \]
\[ Q_{dc} (\eta=5) \]
\[ Q_{dc} (\eta=0.01) \]
\[ Q_{dc} (\eta=5) \]

**Figure 4.6.** Mextram diffusion charges \( Q_{de} \) and \( Q_{dc} \) as function of the junction voltage \( V_j \) (\( V_{b2e1} \), resp. \( V_{b2e2} \)) for different gradings of the base

### 4.7.4 Depletion charge formulation

When the junction is reversely biased, all models use the classical approximation with a grading coefficient (see Figure 4.7). Under forward bias, the models differ in their formulation in order to avoid the singularity at the diffusion voltage \( V_d \).

The Ebers-Moll and the Gummel-Poon Spice implementation use a linear tangential continuation starting from 0 volt for the collector-substrate junction and from \( F_c \cdot V_d \) volt for the other junctions. Note that for the Ebers-Moll model the junction grading coefficient \( m \) is fixed at 0.33.

The VBIC95 depletion capacitances are formulated by default in accordance with the Gummel-Poon Spice implementation. A single-piece formulation that provides a constant capacitance after approaching \( F_c \cdot V_d \) is optional\(^1\) (see Table 4.5). The transition from the graded part to the linear part is ruled by a parameter \( a \). The VBIC95 model uses the same depletion model for all junctions.

---

1. The reference for this depletion capacitance model given in [4.34] refers to a formulation that does not fit with the graphs shown in [4.34].
Figure 4.7. Normalized depletion capacitance functions of the Ebers-Moll, Gummel-Poon, VBIC95 and the Mextram model

Figure 4.8. Normalized base-collector depletion capacitance by the Mextram model
Of the depletion models treated here, the Mextram formulation is closest to the physical Chawla-Gummel results. The Mextram depletion model has a symmetrical peaking around $V_d$ which depends on the grading coefficient and a fixed limiting constant ($K=0.01$) for the base-emitter junction (see Table 4.5 and Figure 4.7).

The base-collector junction capacitance peaks less ($K=0.1$) and is more complicated in its formulation. It takes into account the finite thickness of the epilayer and the modulation of the capacitance by the epilayer current. This results in a decreasing junction capacitance when the epilayer current approaches the critical current density $I_{HC}$. This is illustrated in Figure 4.8.a, where the normalized capacitance is plotted for different values of $I_{cap}$, the critical current density ($I_{HC}$) is set to one. By definition, the value of $I_{cap}$ is limited to $I_{HC}$ (see Table 4.5). Note that also the amount of peaking is controlled by the epilayer current. This is needed in order to obtain a well-behaved modelling of distortion at higher frequencies and current levels.

The modelling of the finite thickness of the epilayer is expressed by the parameter $X_P$ (see also Figure 4.8.b): $X_p = X_{d0}/(W_{epi})$, which represents the ratio of the zero-bias depletion layer and the epilayer thickness. With an increasing value of $X_P$ the base-collector depletion depends less on the base-collector voltage. The extrinsic base-collector charge omits current modulation but takes into account the finite thickness of the epilayer. Note that devices with only a difference in epilayer thickness require modification of the parameter $X_P$ as well the parameter $P_C$. 
### Table 4.5. Overview depletion charge formulation compact bipolar models

<table>
<thead>
<tr>
<th>Ebers-Moll</th>
<th>Gummel-Poon</th>
<th>VBIC95</th>
<th>Mextram</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Basic formulation depletion charge</strong></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>for $V_j &lt; F_C , V_d$:</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$Q_c(C, V_j, V_d, m, F_C) = \frac{C V_d}{1 - m \left( 1 - \frac{V_j}{V_d} \right)^{1-m}}$</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$Q_c(C, V_j, V_d, m, F_C) = \frac{1}{1 - m \left( 1 - \frac{V_j}{V_d} \right)^{1-m} + \frac{1}{(1 - F_C)^m} \cdot Y}$</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$Q_c(C, V_j, V_d, m, F_C) = \frac{CV_d}{1 - m + K}$</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>for $V_j \geq F_C , V_d$:</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$Q_c(C, V_j, V_d, m, F_C) = C \left( F_1 + \frac{(V_j - F_C V_d)(1 - F_C^1 + m(V_j - F_C V_d))}{(1 - F_C^1 + m(V_j - F_C V_d))} \right)$</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$\frac{V_j}{V_d} + F_C - \sqrt{\frac{V_j}{V_d} - F_C}^2 + A$</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$\left( 1 - \frac{1}{(1 - \frac{V_j}{V_d})^{m/2} + CKI} \right)^{m/2} \left( 1 - \frac{I_{cap}}{I_{HC}} \right)^M$</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>If $I_{cap} &gt; 0$ then:</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$CKI = CK + \frac{I_{CAP}}{I_{HC}}$</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>else:</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$CKI = CK$</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>Depletion charge base-emitter junction</strong></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$Q_{te} = Q_c(C_{JE}, V_{BE}, V_{BE}, m_{BE}, F_C)$</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$Q_{te} = Q_c(C_{BE}, V_{BE}, V_{BE}, m_{BE}, A_{BE})$</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$Q_{te} = (1 - X_{CJE})Q_{te}^{inf}$</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$Q_{te} = X_{CJE}Q_{te}^{inf}$</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>with:</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$Q_{te}^{inf} = Q_c(C_{BE}, V_{BE}, V_{BE}, P_{BE}, 0.01, 0)$</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Ebers-Moll</td>
<td>Gummel-Poon</td>
<td>VBIC95</td>
<td>Mextram</td>
</tr>
<tr>
<td>------------</td>
<td>-------------</td>
<td>--------</td>
<td>---------</td>
</tr>
<tr>
<td><strong>Depletion charge base-collector junction</strong></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$Q_{ic} = Q_i(1 - X_{JC})C_{JC} V_{b2c2} \cdot V_{JC} \cdot m_C \cdot F_C$</td>
<td>$Q_{ic} = Q_i(C_{JC}, V_{b2c2}, V_{JC}, m_C, A_{JC})$</td>
<td>$Q_{ic} = \Delta Q_c + (1 - X_p) \cdot Q_i(X_{JC}C_{JC} \cdot V_{b2c2} \cdot V_{DC} \cdot P_C, 0, 1, I_{sup})$ - $X_pX_{JC}C_{JC}(I_{sup} R_{CV} - V_{b2c2})$</td>
<td>If $V_{b2c2} \cdot V_{b2c2} &gt; 0$ then:</td>
</tr>
<tr>
<td>$Q_{ix} = Q_i((1 - X_{JC})C_{JC} V_{b2c2} \cdot V_{JC} \cdot m_C \cdot F_C)$</td>
<td></td>
<td></td>
<td>$I_{CAP} = \frac{I_{HC}(V_{b2c2} - V_{B2c1})}{V_{b2c2} - V_{B2c1} + I_{HC} R_{CV}}$</td>
</tr>
<tr>
<td></td>
<td></td>
<td>else: $I_{CAP} = \frac{V_{b2c2} - V_{B2c1}}{R_{CV}}$</td>
<td>The formulation of $\Delta Q_c$ is given in Chapter 6</td>
</tr>
</tbody>
</table>

| **Depletion charge extrinsic base-collector junction** | | | |
| $Q_{nep} = Q_i(C_{EP} V_{s2b1}, V_{JC} \cdot m_C, A_{JC})$ | $Q_{ite} = X_p C_{ite} V_{b1c1} + Q_i((1 - X_p)C_{ite} V_{b1c1}, V_{DC} \cdot P_C, 0, 1, 0)$ | with: $C_{ite} = (1 - X_{ite})(1 - X_{JC})C_{JC}$ |
| | | | $Q_{ite} = X_p C_{ite} V_{b1c1} + Q_i((1 - X_{ite})C_{ite} V_{b1c1}, V_{DC} \cdot P_C, 0, 1, 0)$ |
| | | | with: $C_{ite} = X_{ite}(1 - X_{JC})C_{JC}$ |

| **Depletion charge collector-substrate junction** | | | |
| $Q_{ix} = Q_i(C_{JS} V_{c1t}, V_{JS} m_S, 0)$ | $Q_{ix} = Q_i(C_{JS}, V_{c1t}, V_{JS} m_S, A_{JS})$ | $Q_{ix} = Q_i(C_{JS}, V_{c1t}, V_{DS} P_S, 0, 01, 0)$ |
4.7.5 Modelling of the base resistance

In vertical npn's the base resistance can be split up into two parts: an external part which consists of the contact resistance and the base resistance outside the emitter, and an intrinsic part which consists of the base resistance under the emitter. This intrinsic part causes a nonuniform biasing of the emitter region, known as current crowding. It can be modelled as a nonlinear resistance. Other effects that influence the base resistance are the base width modulation (Early effect) and the conductivity modulation by the injection of minority carriers. Both effects can be included by using the normalized base charge \( q_b \). Further, at high frequencies, the base structure of a vertical npn leads to distributed high-frequency effects.

Table 4.6 gives the formulation of the base resistance for all four models. In the EM model, the base resistance is taken to be constant. Using the Spice implementation of the GP model, the base resistance contains a constant part, which represents the external resistance and a variable part that represents the intrinsic base resistance. By using \( I_{RB} \), a choice can be made in the modelling of the variable part between current crowding \( (I_{RB} > 0) \) or conductivity modulation \( (I_{RB} = 0) \) by using the normalized base charge \( q_b \). In the VBIC95 and Mextram models there is a separate constant resistor for the modelling of the external base resistance. In the VBIC95 model, emitter crowding is modelled to a first-order approximation by the splitting of the base-emitter current and charge over the variable base resistance (between nodes b1 and b2). The base resistance itself is modulated by the normalized base charge \( q_b \). The Mextram model also has a splitting of the base-emitter current, but still takes into account the emitter current crowding for the base resistance itself \([4.9,4.17]\), without needing an extra parameter. Also the conductivity modulation by the normalized base charge is incorporated (see Table 4.6); this leads to the most refined base resistance modelling of all models presented here.

4.7.6 Excess phase

The time delay in the base combined with its distributed nature entails an extra phase shift in the collector current, the phase shift is larger than predicted by the poles of the equivalent circuit. In order to account for the extra phase shift, two methods can be applied:

The first method modifies the collector current by adding an extra phase shift (see Table 4.6). This method has been applied in the Gummel-Poon and VBIC95 model. Note that the delay time is approximated by a second-order Bessel function. In the GP model, this function is solved for the time domain by using a numerical integration step. In the VBIC95 model, this numerical integration is circumvented by using the node voltage of a separate second-order subcircuit as input voltage for the definition of \( I_f \). The parameter \( P_{TF} \) gives the extra phase shift at the frequency \( f=1/2\pi \tau_F \).

The second method is base-charge partitioning, which rearranges the base-emitter and base-collector charges (see Table 4.6). This method has been applied in the Mextram model. Within the Mextram model, high-frequency current crowding in the lateral direction has also been accounted for, yielding better accuracy in the modelling of \( y_{11} \) \([4.22]\).
### TABLE 4.6. Overview modelling distributed phenomena in the base

<table>
<thead>
<tr>
<th>EM</th>
<th>Gummel-Poon</th>
<th>VBIC95</th>
<th>Mextram</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>base current</strong></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>( I_{bb1} = \frac{V_{bb1}}{R_B} ) for ( I_{RB} = 0 )</td>
<td></td>
<td>( I_{b1b2} = V_{b1b2} \cdot \frac{q_b}{R_{BF}} )</td>
<td>( I_{b1b2} = \frac{q_b}{3R_{BV}} \left( 2V \left( \exp \left( \frac{V_{b1b2}}{V_t} \right) - 1 \right) + V_{b1b2} \right) )</td>
</tr>
<tr>
<td>( I_{bb1} = \frac{V_{bb1}}{R_{BM} + R_B - R_{BM}} ) for ( I_{GB} &gt; 0 )</td>
<td>( I_{b1b2} ) = ( \frac{V_{bb1}}{R_{BM} + 2(R_B - R_{BM})} \left( \frac{\tan(z) - z}{z \tan^2(z)} \right) ) - 1 + ( \frac{1 + \frac{144I_b}{\pi^2 I_{RB}}}{\pi^2 \frac{I_b}{\pi^2 I_{RB}}} ) ( I_{bb1} )</td>
<td>( I_{b1b2} ) as given above</td>
<td></td>
</tr>
<tr>
<td>with: ( z = \frac{24I_b}{\pi^2 I_{RB}} )</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>distributed high-frequency effects in the intrinsic base (excess phase)</strong></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>( I_C = I_{CC} = \omega_0 = I_C \cdot \frac{1}{\frac{\omega}{3 \omega_n^2} + \frac{1}{\omega_n}} )</td>
<td>( Q_{bb1b2} = V_{b1b2} \left( \frac{\partial Q_{TE}}{\partial V_{b2e1}} + \frac{\partial Q_{BE}}{\partial V_{b2e1}} + \frac{\partial Q_N}{\partial V_{b2e1}} \right) )</td>
<td>( Q_{dc'} = (1 - q_c)Q_{dc} )</td>
<td></td>
</tr>
<tr>
<td>with: ( \omega_0 = \frac{1}{\tau_P P_{TF}} )</td>
<td></td>
<td>( Q_{dc'} = q_c Q_{dc} + Q_{dc} )</td>
<td></td>
</tr>
<tr>
<td>( q_c ) is given in Table 4.2</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

### 4.7.7 Modelling of the collector epilayer resistance

At higher current levels or at a relatively low collector-emitter voltage, the voltage drop over the epilayer of the collector can lead to forward biasing of the internal base-collector junction. This effect is called quasi-saturation (q.s.) and has been the subject of several publications: [4.3,4.5,4.6,4.7,4.10,4.13,4.14,4.15,4.18,4.21,4.32]. Quasi-saturation leads to current gain \( \beta \) and cut-off frequency \( (f_T) \) fall-off at higher current levels.

When q.s. occurs, the internal base-collector junction becomes forward biased and injection of minority carriers in the epilayer leads to a strong reduction of the epilayer resistance and the build-up of storage charge. This reduction of the epilayer resistance has been described by Kull et al. in [4.15] and later, more completely, by the Graaff and Kloosterman [4.32]. Recently, in [4.34], an alternative to the Kull model has been proposed. In all cases [4.15,4.32,4.34], we can model the reduction of the epilayer resistance by a current source which is controlled by two voltages, namely the internal junction voltage \( V_{b2e} \) and the
external voltage $V_{b2c1}$ (see Figure 4.9).

The formulation of $I_{c1c2}$ depends on the chosen epilayer model. When ignoring hot carrier effects ($I_{HC} \rightarrow \infty$); all epilayer models reduce to the basic description of the Kull model when hot carriers are omitted. The formulations of the epilayer models are given in Table 4.7.
### TABLE 4.7. Formulation EpiLayer current \( I_{e1c2} \)

<table>
<thead>
<tr>
<th>Kull</th>
<th>VBIC95</th>
<th>Mextram</th>
</tr>
</thead>
<tbody>
<tr>
<td>The complete Kull model ([4.15]) including hot carrier effects:</td>
<td>( I_{e1c2} = \frac{E_e + V_{e1c2}}{R_{CV} + \frac{V_{e1c2}}{I_{HC}}} )</td>
<td>( I_{e1c2} = I_{low} + S_{FH} \left( \frac{V_{e1c2} - I_{low}R_{CV}(1 - \frac{X_i}{W_{epi}})}{S_{CRCV}(1 - \frac{X_i}{W_{epi}})} \right) )</td>
</tr>
<tr>
<td>( I_{e1c2} = I_{ep0} )</td>
<td>with ( X = 0.5 ) according ([4.34]) and ( I_{ep0} ) as the Kull model neglecting hot carriers</td>
<td>with:</td>
</tr>
<tr>
<td>with:</td>
<td>( R_{CV} = R_{CI} )</td>
<td>( I_{low} = \frac{I_{HC}V_{e1c2}}{V_{e1c2} + I_{HC}R_{CV}(1 - \frac{X_i}{W_{epi}})} )</td>
</tr>
<tr>
<td>( I_{ep0} = \frac{E_e + V_{e1c2}}{R_{CV}} )</td>
<td>( S_{CRCV} = R_{CR}H_{RCF} )</td>
<td>( X_i/W_{epi} ) representing the normalized thickness of the injected region of the epilayer.</td>
</tr>
<tr>
<td>( 4\exp\left[ -\frac{V_{DC}}{V_i} \right] = G_{AMM} )</td>
<td>( I_{HC} = V_0/R_{CI} )</td>
<td>Substitution of ( I_{low} ) and ( X_i/W_{epi} ) leads to a cubic equation for ( I_{e1c2} )</td>
</tr>
</tbody>
</table>

\( E_e \) is defined as: \( E_e = V_i(K_0 - K_w - \ln \frac{K_0 + 1}{K_w + 1}) \)

with: \( K_0(V_{b2c2}) = \sqrt{1 + 4\exp\left[ \frac{V_{b2c2} - V_{DC}}{V_i} \right]} \) and \( K_w(V_{b2c2}) = \sqrt{1 + 4\exp\left[ \frac{V_{b2c2} - V_{DC}}{V_i} \right]} \)

The epilayer models differ in their capability to model the epilayer resistance in combination with hot carrier effects. For example, the limitation of the Kull model appears at current levels approaching the critical current density \( I_{HC} \). This can be illustrated by plotting the DC epilayer resistance \((R_{e1c2}=V_{e1c2}/I_{ep0})\) according to the Kull Model (see Figure 4.10). As can be noted from this figure, the epilayer resistance is initially equal to \( R_{CV} \) and increases due to the space charge modulation (Kirk effect) until the internal junction voltage exceeds the built-in voltage \( V_{DC} \) and q.s. sets in. It can be seen that the Kull model becomes inaccurate for a collector current \( I_c \geq I_{HC} = qA\nu_{lim}N_c \).

Recently, an alternative epilayer model has been proposed \([4.34]\) for the VBIC95 model. This Kull-based epilayer has solved the difficulties around \( I_{HC} \) but is incorrect when the device is driven deeper into the q.s. (see Figure 4.10.b). Deeper in q.s., the epilayer resistance predicted by this model again rises. In \([4.34]\), an error has been made, namely \( X = 0.5 \) (see Table 4.7): this leads to the strange behaviour shown in Figure 4.10.b. Replacing \( X = 0.5 \) by \( X = 1 \) leads to more realistic results (see also Figure 4.10.b).
The epilayer formulation used in the Mextram model is given by de Graaff and Kloosterman [4.32] and represents the most realistic description of the epilayer models given here. It includes both the influence of space charge modulation due to hot carriers and current spreading. The formulation provides a more accurate description of the epilayer behaviour in all operating modes than the formulation given by Kull and [4.34]. The final equations of this epilayer model are given in Table 4.7. Figure 4.10.c shows the Mextram epilayer resistance $R_{c1c2}$ as function of the collector current for different external junction voltages $V_{b2c1}$. In this figure (compare with Figure 4.10.a and b), the epilayer resistance once again is initially equal to the value of $R_{CV}$, when the collector current reaches the hot carrier current, the epilayer resistance will increase to a maximum value. This maximum is given by the Mextram parameter $S_{CRCV}$ which represents the space-charge-limited epilayer resistance. Note that the epilayer resistance decreases when the internal junction voltage exceeds the built-in voltage $V_{DC}$. The parameters used in Figure 4.10 are the same for all epilayer models. Following from Figure 4.10, it is clear that the Mextram epilayer model is superior to the Kull and VBIC95 epilayer model.
4.8 Model parameters

It is beyond the scope of this thesis to discuss parameter extraction in full detail. The basics of the parameter extraction for the EM and GP model are well described in [4.12] and [4.16]. The parameter extraction of the Mextram model is given in [4.33], which gives an almost full automatic parameter extraction. The parameter extraction of the VBIC95 model is still under development. Despite all the effort, it must be remarked that an accurate extraction of the series resistances remains difficult. In this section, we concentrate on aspects of the parameter extraction of the compact bipolar epilayer models VBIC95 and Mextram.

The model parameters for the models treated in this chapter are given in appendices A and B. The model parameters are ordered with respect to the related physical effect in Table 4.8. Note that the number of parameters (ignoring temperature and noise parameters) for the EM, GP, VBIC95 and Mextram model are respectively 16, 35, 70 and 39. The very high number of parameters for the VBIC95 model is partly caused by some overlap in the parameter definitions. This overlap is needed in order to maintain compatibility with the GP model. The differences are in the implementation of the Early effect, the current gain and the base resistance, which give a total parameter overlap of seven. If we reduce the original number of parameters of the VBIC95 model for this overlap, still 63 parameters remain to be extracted.

For parameter extraction, the general strategy is to divide the parameters into small groups and extract the grouped parameters from measured data of the physical effects modelled by these parameters. It is obvious that with an increasing number of parameters, it becomes more difficult to define sets of small groups of parameters together with their specific measurements. These measurements should contain enough information to solve or to optimize for the unknown parameters, something that, due to the high correlation between some parameters, is not an easy task. For this reason it is wise to limit the number of parameters as much as possible. In the Mextram model, much emphasis is placed on limiting the number of parameters and relating them to physical quantities, which is in marked contrast to the VBIC95 model. The philosophy of the VBIC95 model, to use just the parts of the model that you want, relaxes the requirements on its parameter extraction. Basically, one could start with a GP model parameter extraction and extend it for the VBIC95 model. This is valid, except for the Early parameters which also depend on the depletion capacitances in the VBIC95 model. Thus, in contrast to the EM and GP model, where the Early parameters can be extracted purely from the DC characteristics, the VBIC95 and Mextram models require a combination of the capacitance and DC measurements.

With more powerful parameter extraction programs (like ICCAP) there is a general trend to combine DC and AC measurement data in order to find the optimum parameter values. This method is most effective when used for parameters that affect the high-current regions, like the delay time modulation parameters, the high-injection parameters and the series resistances in the base, emitter and epilayer. We have used a similar approach to the Mextram epilayer parameter extraction to obtain a parameter set that is capable of describing accurately the nonlinear distortion of the transistor. This set-up concentrates on a simultaneous fit of the transconductance at low and at high frequencies for different base-collector voltages and yields good results for the whole frequency range at all current levels.
TABLE 4.8. Physical effects and the related model parameters

<table>
<thead>
<tr>
<th>Modelled Effect</th>
<th>Ebers-Moll (Spice version)</th>
<th>n</th>
<th>Gummel-Poon (Spice version)</th>
<th>n</th>
<th>Ext. GP / VBIC95</th>
<th>n</th>
<th>Mextram</th>
<th>n</th>
</tr>
</thead>
<tbody>
<tr>
<td>main current</td>
<td>IS, VAF</td>
<td>2</td>
<td>IS, NF, NR, VAF, VAR, IKF, IKR</td>
<td>7</td>
<td>IS, NF, NR, VAF, VAR, VEE, VER, IKF, IKR</td>
<td>7</td>
<td>IS, QB0, XCI, XCIJC</td>
<td>4</td>
</tr>
<tr>
<td>base currents</td>
<td>BF, BR</td>
<td>2</td>
<td>BF, BR, ISE, ISC, NE, NC</td>
<td>6</td>
<td>BF, BR, ISE, ISC, NE, NC, IB, NEI, NCI, WBE</td>
<td>11</td>
<td>BF, BRI, IBF, IBR, VLF, VLR, XIBI</td>
<td>7</td>
</tr>
<tr>
<td>substrate currents</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>ISP, NFP, IBEI, IB, NEP, NCP, NCP, NC, ICP, IC, IB, ICP, NCP, NCP</td>
<td>10</td>
<td>ISS, IKS</td>
<td>2</td>
</tr>
<tr>
<td>avalanche current</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>AVC1, AVC2</td>
<td>2</td>
<td>AVL, EFI</td>
<td>2</td>
</tr>
<tr>
<td>collector resistance</td>
<td>RC</td>
<td>1</td>
<td>RC</td>
<td>1</td>
<td>RC</td>
<td>1</td>
<td>RCC</td>
<td>1</td>
</tr>
<tr>
<td>base resistance</td>
<td>RB</td>
<td>1</td>
<td>RB, IR, RMB</td>
<td>3</td>
<td>RB, IR, RMB, RBX, RBL</td>
<td>5</td>
<td>RBC, RBV</td>
<td>2</td>
</tr>
<tr>
<td>emitter resistance</td>
<td>RE</td>
<td>1</td>
<td>RE</td>
<td>1</td>
<td>RE</td>
<td>1</td>
<td>RE</td>
<td>1</td>
</tr>
<tr>
<td>substrate resistance</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>RS</td>
<td>1</td>
<td></td>
<td></td>
</tr>
<tr>
<td>epilayer</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>RCI, GAMM, V0, HRCC, QC0</td>
<td>5</td>
<td>RCV, IHC, VDC, SCRCV, SFH</td>
<td>5</td>
</tr>
<tr>
<td>storage charge</td>
<td>TF, TR</td>
<td>2</td>
<td>TF, TR, XTF, ITF, VTF</td>
<td>5</td>
<td>TF, TR, XTF, ITF, VTF, QTF</td>
<td>6</td>
<td>IK, ETA, TAU, MTAU</td>
<td>4</td>
</tr>
<tr>
<td>collector dep. charge</td>
<td>CJE, VJC, FC</td>
<td>3</td>
<td>CJC, VJC, MJC, XCIC, FC</td>
<td>5</td>
<td>CJC, VJC, MJC, XCIC, FC, AJ, CJE</td>
<td>7</td>
<td>CJC, PC, XP, MC, XEXT</td>
<td>5</td>
</tr>
<tr>
<td>emitter dep. charge</td>
<td>CJE, VJE</td>
<td>2</td>
<td>CJE, VJE, MJE, AJE</td>
<td>3</td>
<td>CJE, VJE, MJE, AJE</td>
<td>4</td>
<td>CJE, VDE, PE</td>
<td>3</td>
</tr>
<tr>
<td>substrate dep. charge</td>
<td>CJS, VJS</td>
<td>2</td>
<td>CJS, VJS, MJS, AJS</td>
<td>3</td>
<td>CJS, VJS, MJS, AJS</td>
<td>4</td>
<td>CJS, VDS, PS</td>
<td>3</td>
</tr>
<tr>
<td>fixed capacitances</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>CBE0, CBC0</td>
<td>2</td>
<td></td>
<td></td>
</tr>
<tr>
<td>excess phase</td>
<td>PTF</td>
<td>1</td>
<td>PTF, TD</td>
<td></td>
<td></td>
<td>2</td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>sub. total</strong></td>
<td>16</td>
<td>35</td>
<td></td>
<td>70</td>
<td></td>
<td>39</td>
<td></td>
<td></td>
</tr>
<tr>
<td>noise</td>
<td>KF, AF</td>
<td>2</td>
<td>KF, AF</td>
<td>2</td>
<td>KF, KNF, AF</td>
<td>2</td>
<td></td>
<td></td>
</tr>
<tr>
<td>temperature</td>
<td>EG, XTB, XTI</td>
<td>3</td>
<td>EG, XTB, XTI</td>
<td>3</td>
<td>EG, XTB, XTI, XII, XIN, XRE, XRB, XRC, XR, XVO, EAIE, EAIC, EAIS, EAAN, EANS, TF, TAVC</td>
<td>18</td>
<td>VGE, VGC, VGB, VGS, VGJ, AB, AEP, AEX, AC, VI, ER, NA</td>
<td>12</td>
</tr>
<tr>
<td><strong>total</strong></td>
<td>21</td>
<td>40</td>
<td></td>
<td>90</td>
<td></td>
<td>54</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

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4.9 Results

The Mextram and VBIC95 model calculations are compared with characteristics obtained from the 2D device simulator Medici [4.25]. (A comparison of the GP model with the Mextram model is given in Chapter 5, so the simulation results of this model are not treated here). The transistor structure used in the Medici simulations is described in [4.28], and is based on SIMS measurements, and it is representative of present-day bipolar transistor technology. The Mextram parameters are extracted as previously discussed, the GP parameters have been extracted using standard procedures [4.29]. Due to the fact that to date there is no pre-described parameter extraction method for the VBIC95 model, the parameter set of this model are calculated, based on a GP and Mextram parameter set for the same device. In the end, fine-tuning of the VBIC95 parameters was performed by comparing VBIC95 characteristics with Medici characteristics.

Using the calculated parameters (which are physically correct) we observed a strange behaviour in the high-current region of the $I_{C}(V_{CE})$ characteristics for the VBIC95 model (see Figure 4.11). This behaviour is caused by the incorrect epilayer model of the VBIC95 model as discussed in “Modelling of the collector epilayer resistance” on page 71. We can correct for this nonphysical behaviour by neglecting the hot carrier effect for the VBIC95 model ($I_{HC} \rightarrow \infty$) and reducing its epilayer model to the basic Kull epilayer model without hot carrier effects. Using this physically more correct simplification of the VBIC95 model, we have fine-tuned the VBIC95 parameter set and obtained a good overall fit of the $I_{C}(V_{CE})$ as well as reasonable $f_T(I_C)$ characteristics (see Figure 4.12 and Figure 4.13). As can be seen from Figure 4.12, both models fit the low current $I_{C}(V_{CE})$ characteristics well. At higher current levels and collector-emitter voltages, the fit becomes less perfect for both models. The greatest deviations are found for the VBIC95 model and this can be explained by the neglect of hot carrier effects. Generally speaking, one could improve the fit of the $I_{C}(V_{CE})$ characteristics for high-current levels by manipulation the high-injection parameter $I_K$. However, doing so would cause problems in the modelling of the maxima in the $f_T(I_C)$ characteristics. For the $f_T$ characteristics, the quality of the fit is in the same order for both models (see Figure 4.13). That the VBIC95 model is capable of achieving a good $f_T$ fit even when hot carriers are ignored is because of the considerable flexibility in the current and voltage modulation of the delay time $\tau_C$. Note that a correct fit of the $f_T$ characteristics at very high-current levels remains difficult.

The low and high frequency distortion behaviour of the VBIC95 and Mextram model are compared in Chapter 6. From these results, it works out that for this low-doped epilayer device, the Mextram model is far more accurate in its distortion behaviour than the VBIC95 model.
Figure 4.11. High-current region of the $I_c(V_{ce})$ characteristics using: Medici, Mextram and VBIC95 with physically correct parameters.

Figure 4.12. Low and high-current region of the $I_c(V_{ce})$ characteristics using: Medici, Mextram and VBIC95 ignoring hot carriers.
4.10 Conclusions

In this chapter, four of the most important public domain compact models have been given in a unified manner, complete with their schematic, parameters and their formulation in tabular form. Differences in the formulation have been discussed and supported by graphical illustrations. We summarize the following conclusions from this side-by-side model comparison:

- **The Ebers-Moll model:** Due to its short calculation time and its low requirements on memory, it is well suited to the simulation of large digital circuits, operating at low to medium switching speed in respect to the transistor cut-off frequency. For designs operating at high-current levels or frequencies, the model tends to be over-optimistic in its predictions.

- **The Gummel-Poon model:** This model has been the favourite of many designers for a long period of time, it includes many electrical effects in a relatively simple manner, such as the Early effect, high injection and the distributed nature of the base. Its biggest disadvantage is the absence of a real epilayer model.

- **The VBIC95 model:** This model still looks unfinished. In its full definition it demands the use of many parameters and much memory and computation time are required. The modelling of the collector epilayer should be done in a more careful way. The implementation as given in [4.34] results in nonphysical behaviour when going deeper into q,s. The advantage of this model is that it
Conclusions

is closely related to the Gummel-Poon model, making acceptance easier for a wider public. In this respect, it is pity that the compatibility with respect to the Early voltages $V_{AR}$ and $V_{AF}$ has been lost.

- **The Mextram model:** The formulation of this model includes a direct coupling between the current and charge model thus leading to coupled DC and AC behaviour. This coupling has the advantage that when the correct parameter set is found, which can be done fully automatically [4.33], a physical representation of the device is found, which facilitates accurate scaling [4.24]. The physically correct epilayer model, including hot carrier behaviour and improved formulation of the base-collector charge leads to monotonic Early voltage and $f_T(I_C)$ behaviour at the onset of q.s. and, consequently, to an improved simulation of distortion, even for transistors with a lightly doped epilayer (see also Chapter 6).

From the above we see that the most logical model choice for the RF designer is, at the moment, the Mextram model. From Table 4.9, it is clear that the Mextram model is the most complete of all the models presented here. The only point where Mextram could use some improvement is in the $f_T$ fall-off at very high-current levels. Note that the VBIC95 model has considerable flexibility in its $f_T$ fall-off but it does not necessarily yields better results. A model that is very concentrated on the $f_T$-fall-off and that could improve on this point is the HICUM model [4.19,4.20,4.27]. The reason that the HICUM model has not been compared here with the other models is that it is not in the public domain. It must be noted, however, that the HICUM model uses a completely different epilayer approach and that it would be interesting to compare the $y$-parameters as function of the bias current at several frequencies of HICUM and Mextram.
### TABLE 4.9. Various effects modelled in bipolar compact models

<table>
<thead>
<tr>
<th>Modelled Effect</th>
<th>Ebers-Moll (Spice version)</th>
<th>Gummel-Poon (Spice version)</th>
<th>Ext. GP / VBIC95</th>
<th>Mextram</th>
</tr>
</thead>
<tbody>
<tr>
<td>low current drop in $\beta$</td>
<td>-</td>
<td>implemented</td>
<td>implemented</td>
<td>implemented</td>
</tr>
<tr>
<td>high-injection effects</td>
<td>-</td>
<td>implemented</td>
<td>implemented</td>
<td>implemented</td>
</tr>
<tr>
<td>Early effect</td>
<td>only for forward operation using the constant voltage $V_a$</td>
<td>in forward and reverse operation using the constant voltages $V_a$ and $V_b$</td>
<td>bias-dependent Early voltages.</td>
<td>implemented, double split optional</td>
</tr>
<tr>
<td>split base-collector capacitance</td>
<td>-</td>
<td>implemented</td>
<td>implemented</td>
<td>modulated by the base width and current crowding by first-order approx.</td>
</tr>
<tr>
<td>base resistance</td>
<td>constant</td>
<td>function of $I_b$</td>
<td>modulated by the base width and current crowding by first-order approx.</td>
<td>modulated by the base width and current crowding by first-order approx.</td>
</tr>
<tr>
<td>built-in electric field in the base</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>implemented</td>
</tr>
<tr>
<td>substrate effects and parasitic pnp</td>
<td>-</td>
<td>only collector substrate capacitance</td>
<td>parasitic pnp</td>
<td>parasitic pnp and extrinsic region optional by flag</td>
</tr>
<tr>
<td>excess phase shift</td>
<td>-</td>
<td>direct addition of phase shift</td>
<td>same as GP.</td>
<td>partial shift of base diffusion charge to collector and addition of a shunt capacitance over the base resistance, (optional flag)</td>
</tr>
<tr>
<td>quasi-saturation</td>
<td>-</td>
<td>-</td>
<td>modelled separately</td>
<td>modelled separately</td>
</tr>
<tr>
<td>hot carrier effects in the collector epilayer</td>
<td>-</td>
<td>-</td>
<td>poorly</td>
<td>low and high field conditions continuously matched</td>
</tr>
<tr>
<td>current spreading in the epilayer</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>implemented</td>
</tr>
<tr>
<td>extra collector charge for onset q.s.</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>implemented</td>
</tr>
<tr>
<td>weak avalanche</td>
<td>-</td>
<td>-</td>
<td>same as Mextram</td>
<td>implemented, extended modelling (optional flag)</td>
</tr>
</tbody>
</table>
### Appendix A) Parameters of the Ebers-Moll, Gummel-Poon and Ext GP (VBIC95) model

In Table A.1 the input parameters of the Ebers-Moll, GP and Ext. GP / VBIC95 model are given according the SPICE 2G implementation and [4.34] notation. Note that some parameters are common parameters for more than one model. The notation used to indicate this is:

- **bold:** EM + GP + VBIC95
- **italic:** GP + VBIC95
- **regular:** VBIC95

<table>
<thead>
<tr>
<th>Symbol</th>
<th>SPICE 2G keyword</th>
<th>Parameter description</th>
<th>Default value</th>
</tr>
</thead>
<tbody>
<tr>
<td>$I_S$</td>
<td>IS</td>
<td>Saturation current</td>
<td>10.e-16</td>
</tr>
<tr>
<td>$B_F$</td>
<td>BF</td>
<td>Ideal maximum forward current gain</td>
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<tr>
<td>$B_R$</td>
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<tr>
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<td>Base-emitter saturation current</td>
<td>10.e-18</td>
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<tr>
<td>$I_{BCI}$</td>
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<td>Base-collector saturation current</td>
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<td>$I_{SE}$</td>
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<tr>
<td>$I_{SC}$</td>
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<td>Base-collector leakage saturation current</td>
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<td>$N_E$</td>
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<td>Forward Early voltage</td>
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<td>Emitter resistance</td>
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<td>Substrate resistance</td>
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<td>Minimum base resistance at high currents</td>
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<td>Constant external base resistance</td>
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<td>Modulated part of base resistance parasitic pnp</td>
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<td>Parameter description</td>
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<td>Excess phase at $f=1/2\pi\tau_F$</td>
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<td>Zero-bias base-emitter depletion capacitance</td>
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<td>$V_{JE}$</td>
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<td>Base-emitter built-in potential</td>
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<td>$m_E$</td>
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<td>Base-emitter junction grading coefficient</td>
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<td>Smoothing coefficient base-emitter depletion capacitance</td>
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<td>Zero-bias base-collector depletion capacitance</td>
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<td>Base-collector built-in potential</td>
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<tr>
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<tr>
<td>$C_{JEP}$</td>
<td>CJE P</td>
<td>Parasitic pnp zero-bias base-emitter depletion capacitance</td>
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<tr>
<td>$C_{JS}$</td>
<td>CJS,CJCP</td>
<td>Zero-bias collector-substrate depletion capacitance</td>
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<tr>
<td>$V_{JS}$</td>
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<td>Substrate-junction built-in potential</td>
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<td>Substrate-junction exponential factor</td>
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<td>Smoothing coefficient collector-substrate depletion capacitance</td>
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<tr>
<td>$X_{CJC}$</td>
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<td>Fraction of base-collector depletion capacitance connected to internal base node</td>
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<tr>
<td>$F_C$</td>
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<td>Coefficient for forward depletion capacitance formula</td>
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<td>$C_{BC0}$</td>
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<td>Fixed base-collector capacitance</td>
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<td>Weighting factor storage charge epilayer</td>
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<td>Saturation current parasitic pnp</td>
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<td>Base-emitter saturation current parasitic pnp</td>
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<td>$I_{BENP}$</td>
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<td>Base-emitter leakage saturation current parasitic pnp</td>
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<td>$I_{BCNP}$</td>
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<td>Base-collector leakage saturation current parasitic pnp</td>
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<td>Base-collector leakage saturation current parasitic pnp</td>
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<td>Base-collector leakage emission coefficient parasitic pnp</td>
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### TABLE A.1 Model parameters Ebers-Moll model (bold) and Gummel-Poon conform the SPICE 2G implementation

<table>
<thead>
<tr>
<th>Symbol</th>
<th>SPICE 2G keyword</th>
<th>Parameter description</th>
<th>Default value</th>
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<tr>
<td>$I_{KP}$</td>
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<td>Corner for forward high-current gain roll-off parasitic pnp</td>
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<td>$W_{EB}$</td>
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<td>Base current splitting ratio</td>
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<td>$W_{SP}$</td>
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<td>Current splitting ratio parasitic pnp</td>
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<td>Avalanche parameter one</td>
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<td>$A_{VC2}$</td>
<td>AVC2</td>
<td>Avalanche parameter two</td>
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<td>$R_{CI}$</td>
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<td>Low electric field epilayer resistance</td>
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<tr>
<td>$V_0$</td>
<td>V0</td>
<td>Critical electric field epilayer</td>
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<tr>
<td>$G_{AMM}$</td>
<td>GAMM</td>
<td>Measure for built-in voltage base-collector junction</td>
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<tr>
<td>$H_{FCR}$</td>
<td>HFCR</td>
<td>Ratio between low and high electric field epilayer resistance</td>
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#### Model temperature definition

- **$T$**
  - Nominal temperature for simulation and at which all input data is assumed to have been measured: $27.0$°C

#### Temperature parameters

<table>
<thead>
<tr>
<th>Symbol</th>
<th>SPICE 2G keyword</th>
<th>Parameter description</th>
<th>Default value</th>
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<tr>
<td>$X_{TB}$</td>
<td>XTB</td>
<td>Forward and reverse $\beta$ temperature coefficient</td>
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<td>$X_{II}$</td>
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<td>Base saturation current temperature exponent</td>
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<td>$X_{IN}$</td>
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<td>Base leakage saturation current temperature exponent</td>
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<td>Emitter resistance temperature exponent</td>
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<td>Base resistance temperature exponent</td>
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<td>Collector resistance temperature exponent</td>
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<td>$X_{RS}$</td>
<td>XRS</td>
<td>Substrate resistance temperature exponent</td>
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<td>Built-in base-collector voltage junction temperature exponent</td>
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<tr>
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<td>Energy gap for temperature effect on $I_{BEI}$</td>
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<tr>
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<td>Energy gap for temperature effect on $I_{BEN}$</td>
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<tr>
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<td>Energy gap for temperature effect on $I_{BCN}$</td>
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<td>$E_{ANS}$</td>
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#### Noise parameters

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<td>Flicker-noise exponent</td>
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Appendix B) Parameters of the Mextram model

The input list for the MEXTRAM model release 503 is listed below.

<table>
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<th>Symbol</th>
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<th>Parameter description</th>
<th>Default value</th>
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<td></td>
<td>simulation flags</td>
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<td>EXPHI</td>
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<td>Flag for distributed high-frequency effects</td>
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<td>Flag for extended modelling of avalanche currents</td>
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<td>model parameters</td>
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<td>Collector-emitter saturation current</td>
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<td>IK</td>
<td>IK</td>
<td>High-injection knee current</td>
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<td>Q_{BO}</td>
<td>QB0</td>
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<td>V_{DE}</td>
<td>VDE</td>
<td>Emitter-base diffusion voltage</td>
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<td>P_E</td>
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<td>Emitter-base grading coefficient</td>
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<td>X_{EXT}</td>
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<td>Cross-over voltage of the nonideal forward base current</td>
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HF Silicon Modelling
### TABLE B.1 Mextram 503 input list

<table>
<thead>
<tr>
<th>Symbol</th>
<th>MDS keyword</th>
<th>Parameter description</th>
<th>Default value</th>
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<td>Critical current for hot carriers</td>
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<td>Resistance of the unmodulated epilayer</td>
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<td>Space charge resistance of the epilayer</td>
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<td>Current spreading factor epilayer</td>
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<tr>
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<td>Emitter series resistance</td>
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<td>$R_{CC}$</td>
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<td>Constant part of the collector resistance</td>
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<td>Constant part of the base resistance</td>
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<tr>
<td>$R_{BV}$</td>
<td>RBV</td>
<td>Variable part of the base resistance at zero bias</td>
<td>300.0</td>
</tr>
<tr>
<td>$B_{RI}$</td>
<td>BRI</td>
<td>Ideal reverse current gain</td>
<td>6.5</td>
</tr>
<tr>
<td>$I_{SS}$</td>
<td>ISS</td>
<td>Base-substrate saturation current</td>
<td>5.0e-17</td>
</tr>
<tr>
<td>$I_{KS}$</td>
<td>IKS</td>
<td>Knee current of the substrate</td>
<td>6.0e-6</td>
</tr>
<tr>
<td>$A_{VL}$</td>
<td>AVL</td>
<td>Weak avalanche parameter</td>
<td>75.0</td>
</tr>
<tr>
<td>$E_{FI}$</td>
<td>EFI</td>
<td>Electric field intercept (with EXAVL=1)</td>
<td>0.73</td>
</tr>
</tbody>
</table>

### Model temperature definition

- $T_{REF}$: TREF, Reference temperature
- $D_{TA}$: DTA, Difference of the device temperature to the ambient

### Temperature scaling parameters

- $E_R$: ER, Temperature coefficient of VLF and VLR
- $A_B$: AB, Temperature coefficient resistivity base
- $A_{EX}$: AEX, Temperature coefficient resistivity of the extrinsic base
- $A_C$: AC, Temperature coefficient resistivity of the buried layer
- $A_S$: AS, For a closed buried layer: $A_S = A_C$
- $A_{EPI}$: AEPI, Temperature coefficient resistivity of the epilayer
- $N_A$: NA, Maximum base dope concentration
- $V_{GE}$: VGE, Band-gap voltage of the emitter
- $V_{GB}$: VGB, Band-gap voltage of the base
- $V_{GC}$: VGC, Band-gap voltage of the collector
- $V_{GS}$: VGS, Band-gap voltage of the substrate
- $V_{GI}$: VGI, Band-gap voltage recombination emitter-base junction
- $V_I$: VI, Ionization voltage base dope

### Noise parameters

- $K_F$: KF, Flicker-noise ideal base current
- $K_{FN}$: KFN, Flicker-noise coefficient nonideal base current
- $A_F$: AF, Flicker-noise exponent
4.11 References


Chapter 5  

High-current signal distortion 
in bipolar transistors

5.1 Introduction

In mobile telecommunication receivers and transmitters, there are several constraints on the output power, efficiency, and matching; there is the requirement for a low battery power consumption and supply voltage. These will, in general, limit the collector-emitter voltage. It is clear that at higher current levels, or at a relatively low collector emitter voltage, the voltage drop over the epilayer of the collector can lead to forward biasing of the internal junction. This effect is called quasi-saturation (q.s.) and has been discussed in Chapter 4. Quasi-saturation leads to current gain ($\beta$) and cut-off frequency ($f_T$) fall-off at higher current levels. Less well known to designers is the fact that the onset of q.s. also has a dominant influence on the distortion behaviour of the bipolar transistor [5.9]. In conventional transistor models like the Gummel-Poon model, the modelling of q.s. is limited to the voltage drop over the fixed internal collector resistance ($R_c$), which can lead to “unexpected” results when realized circuits are measured. Quasi-saturation effects are of particular interest under high drive conditions as in power stages or mixers. In this chapter, we consider the modelling of distortion effects in bipolar transistors which are due to the onset of quasi-saturation and compare computational results obtained by using the Mextram and Gummel-Poon model, with measured results.

5.2 The modelling of quasi-saturation in transistor models

In conventional transistor models such as the Gummel-Poon model, the voltage drop in the collector is modelled by a single ohmic resistor
$R_C$ (see Chapter 4, Figure 4.2). In the Mextram model, the voltage drop in the collector region is modelled by the ohmic buried layer resistor $R_{CC}$ and a voltage-controlled current source $I_{c1c2}$ (see Figure 4.5). The controlled source is used to account for the voltage drop across the epilayer resistance, it is modulated by the injected space charge in the collector region [5.14,5.18]. The extra voltage drop in the Mextram model leads to earlier forward biasing of the internal base collector junction than occurs in the Gummel-Poon model. This is best illustrated by considering the simulation results obtained with the Gummel-Poon and Mextram models for the same transistor. We have chosen the BFR520 transistor commonly employed in discrete RF circuits. The calculated $I_c(V_{ce})$ characteristics are compared with measurement data given in Figure 5.1. The q.s. region ($V_{b2c2} \geq 0.7V$) is much larger for Mextram than for GP. Both models give a reasonable fit of the $I_c(V_{ce})$ characteristic, but GP does so by manipulating the Early voltages; GP, however, fails to describe distortion behaviour at higher current levels or at low collector-emitter voltages, as explained in the next section.

![Figure 5.1. $I_c(V_{ce})$ characteristics of the BFR520 transistor, for $I_B=0.1$, 0.3, 0.5, 0.7 mA](image)

5.3 Low-frequency distortion effects at high-current levels

Distortion effects at low-current levels in bipolar transistors are well understood [5.2,5.3,5.8]. Conventional transistor models like Gummel-Poon [5.12] as well as the Mextram model can model most of the distortion effects for moderate drive conditions. At high-current levels or at lower collector-emitter voltages, q.s. will set in at a certain point for a given device. The onset of q.s. will lead to an increase in the third-order distortion component [5.9].
5.3.1 Distortion increase due to q.s.

This increase in distortion is caused by the internal base-collector junction becoming forward biased. When this happens, the injection of minority carriers in the epilayer (related to the built-in base-collector junction voltage) will lead to a considerable reduction of the epilayer resistance and the build-up of storage charge. This, combined with the increase of the reverse component of the main current, will lead to a significant change in the small-signal transfer of the device under consideration. The distortion behaviour can be understood by studying the small-signal transfer of the circuit shown in Figure 5.2. At sufficiently low frequencies, (ignoring reactive elements) the higher harmonics in the output of the transistor will be related to the input voltage by a Taylor series [5.12]. Consequently, the distortion behaviour of a device can be studied at low frequencies and low driving conditions by investigating the derivatives of the AC transfer characteristics with respect to the input voltage \( V_{b2e1} \).

![Circuit Diagram](image)

**Figure 5.2.** Simplified circuit model of a bipolar transistor with a lightly doped epilayer

The small-signal definitions of the epilayer current and the main current in the Mextram implementation are:

\[
i_n = g_x v_{b2e1} + g_y v_{b2c2} \tag{5.1}
\]

\[
i_{epi} = g_{epiy} v_{b2c2} + g_{epiz} v_{b2c1} \tag{5.2}
\]

where:

\[
\begin{align*}
g_x &= \frac{\delta I_n}{\delta V_{b2e1}} \\
g_y &= \frac{\delta I_n}{\delta V_{b2c2}} \\
g_{epiy} &= \frac{\delta I_{epi}}{\delta V_{b2c2}} \\
g_{epiz} &= \frac{\delta I_{epi}}{\delta V_{b2c1}}
\end{align*} \tag{5.3}
\]

AC short-circuiting the output of the given network topology yields: \( V_{b2c1} = V_{b2e1} \) and \( i_n = i_{epi} \). By using these conditions, we can solve for the small-signal transconductance \( i_{epi} / v_{b2e1} \), leading to:

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Low-frequency distortion effects at high-current levels

\[
\frac{i_{epi}}{v_{b2e1}} = g_x + g_y \left[ \frac{g_{epiz} - g_x}{g_y - g_{epiz}} \right] \tag{5.4}
\]

Although this appears simple in its representation, the conductances used in equation (5.4) represent very complicated functions. As we are interested in the influence of the epilayer parameters on the distortion behaviour at the onset of q.s, we ignore (for this analysis only) the influence of the normalized base-charge component (high injection, Early effect) and simplify the conductances to their first-order approximation:

**no saturation:** In this situation the main current is given by: \( I_n = I_f = I_s \exp(V_{b2e1}/V_t) \) consequently \( g_x = I_f/V_t \) (linear with the collector current) and \( g_y = 0 \).

**quasi-saturation:** \( (V_{b2e2} > 0) \) In this situation the main current is given by:
\[
I_n = I_f - I_r = I_s \left[ \exp(V_{b2e1}/V_t) - \exp(V_{b2e2}/V_t) \right],
\]
consequently \( g_x = I_f/V_t \), \( g_y = -I_r/V_t \) and \( g_x + g_y = I_n/V_t \).

When considering the transconductance of equation (5.4) as a function of the DC collector current, we note that \( i_{epi}/v_{b2e1} \) in the nonsaturated region equals \( g_x \) and is linear with the DC collector current. When entering q.s, \( g_y \) is no longer zero and the transconductance no longer increases linearly (see curves marked with "fund" (for fundamental) in figures 5.8 and 5.9). The higher harmonics (2nd and 3rd) can be determined from the derivatives of the transconductance with respect to \( V_{b2e1} \).

5.3.2 The influence of the parameters \( V_{DC} \) and \( R_{CV} \)

For reasons of simplicity, we use the Kull model [5.11] with a purely ohmic epilayer description, neglecting hot carrier effects (in any case, the Kull model becomes inaccurate when approaching \( I_{HC} \)). This simplified Kull model is equal to the Mextram model for low current values and has the advantage for this analysis that \( i_{epi} \) is only affected by two parameters (see Table 4.7 on page 73): \( R_{CV} \) which represents the epilayer resistance, and \( V_{DC} \) (the built-in base-collector junction voltage). \( R_{CV} \) will influence the value of the collector current at which the internal junction becomes forward biased for a given external base-collector voltage (see Figure 5.3). In contrast, the built-in voltage \( V_{DC} \) hardly affects the current at which the transistor enters q.s, but it will determine how much the internal base-collector junction will become forward biased and thus it directly determines \( g_y \). The value of \( g_y \) acts as a weighting factor for the term between brackets in equation (5.4), and it affects the slope of the decrease of the transconductance. This is of major importance for the increase in distortion when the device enters the q.s. region. In summary, we note that a device with a high built-in junction voltage will result in more distortion when it enters q.s. than a similar device with a lower built-in voltage. This is illustrated in Figure 5.4.
Figure 5.3. The influence of $R_{CV}$ on the fundamental frequency and third harmonic of $i_n$.

Figure 5.4. The influence of $V_{DC}$ on the fundamental frequency and the third harmonic when a transistor enters quasi-saturation.
Simulations and measurement results at low frequencies

In the standard Mextram parameter extraction, the epilayer parameters $R_{CV}$, $V_{DC}$, $I_{HC}$, $S_{FH}$ and $S_{CRCV}$ are found by fitting both the $f_t(I_c)$ fall-off and the q.s. region of the $I_c(V_{ce})$ characteristics (see shaded area Figure 5.1). This will give a good first-order approximation of the epilayer parameter values; fine tuning for accurate harmonic description can be performed by concentrating on the fit of the transconductance as a function of $I_c$ for several base-collector voltages in the frequency range of interest.

5.4 Simulations and measurement results at low frequencies

**simulations:** The calculated distortion data for the BFR520 have been obtained using our Mextram implementation in Hewlett Packard's harmonic balance simulator MDS. This has proved to be a particularly valuable tool in this investigation.

**measurements:** Although pulsed bias voltages are applied to minimize self-heating effects, the DUT will generally heat up within 0.1 ms, which leads to an increase in the collector current. To avoid corruption of the distortion data, the LF measurement should be short in duration and take place at exactly the same moment that the bias current $I_c$ is measured. At lower current levels, distortion measurements can be carried out using a spectrum analyzer (SPA). At higher current levels, self-heating of the device under test (DUT) will give temperature-related errors caused by the minimum sweep time (e.g. 20 ms) inherent to the instrument. In principle, faster measurements are possible by setting the SPA to zero bandwidth and locking the signal source to the SPA. In practice, SPA (hp8566A) firmware-related problems made it impossible to achieve the desired measurement time (e.g. $t < 0.1$ ms).

Alternatively, distortion measurements can be carried out using a 100 MHz, 500 megasamples/sec data acquisition scope to maintain the phase information. An illustration of this measurement set-up is given in Figure 5.5. The network analyzer is used as a 10 MHz signal source. At a constant $V_{ce}$, the $V_{be}$ of the transistor is pulsed for 1 ms. The amplified signal will stabilize at the output of the DUT within 50 µs and the sample scope triggered. Following a delay of approximately 0.7 ms, the DC collector current as well as the AC voltage over the 50 ohm load resistance during a time span of 0.1 ms are measured and read by HP's data acquisition program VEE TEST. For each bias point, a trace of the load resistance voltage is taken and a Fast Fourier Transformation (FFT) is performed to find the coefficients of the distortion components. Since a large number of periods are measured, the FFT functions as an averaging filter, thus improving the accuracy. A comparison of the measurement results obtained with an SPA and with a sample scope is given in Figure 5.6. The results of the SPA drift away at higher collector base voltages as the DUT consumes more power.
High-current signal distortion in bipolar transistors

Low-frequency distortion measurements

![Diagram showing experimental setup for low-frequency distortion measurements](image)

**Figure 5.5.** Low-frequency distortion measurement set-up using a 100 MHz / 500 megasamples / sec. oscilloscope

![Graph showing current vs. voltage](image)

**Figure 5.6.** Comparison of data obtained with an SPA (20 ms) and sampling scoop (1 ms)
results: In comparing the Mextram and the Gummel-Poon simulations, we note that the third-order distortion maximum is manifest when approaching the $V_{b2c2} = 0.7\, V$ lines of Figure 5.1. Since in the case of Gummel-Poon, this line is reached much later, bipolar transistor distortion at higher current levels is improperly modelled (see figures 5.7 to 5.9 for increasing driving voltages). In these figures, the amplitude of the fundamental frequency (10 MHz) as well as the second- and third-order distortion components of the collector voltage are plotted as a function of $I_c$ for $V_{bc} = 0, -1$ and $-3\, V$. (The AC collector voltage is directly related to the AC collector current via a 50 ohm load resistor). In general, the distortion of larger signals is more easily modelled because small details in the device characteristics are then of reduced significance.

![fundamental tone](image)

![second-order distortion](image)

**Figure 5.7.** Simulated and measured distortion components in the collector voltage of the BFR520 at a driving input voltage of 7 mV
Figure 5.8. Simulated and measured distortion components in the collector voltage of the BFR520 at a driving input voltage of 21 mV
Figure 5.9. Simulated and measured distortion components in the collector voltage of the BFR520 at an input voltage level of 62 mV
5.5 Discussion LF results

Comparison of the measured and simulated LF distortion results leads to the conclusion that Mextram is far more accurate than GP at all power levels. At higher power levels, the fit for GP seems to improve somewhat, because the transistor now enters hard saturation thus increasing the third-order distortion. In Figure 5.9, we note that although there is better fit for the third-order distortion, the minima are still dislocated with respect to the collector current. Second-order distortion products as predicted by the GP model also fail to describe the measured results.

5.6 Conclusions

Incorporation of the latest developments in the formulation of epilayer behaviour in Mextram has provided the first compact transistor model capable of accurately describing the LF distortion behaviour of a transistor when operation extends into the region of quasi-saturation. Implementation of Mextram in the simulator package MDS has resulted in a very powerful combination which facilitates the use of harmonic balance techniques in strongly nonlinear circuit design. The results of this chapter are valid for LF conditions. When considering RF excitation, the charge functions must also be taken into account. We treat this issue in the next chapter.

5.7 References


[5.10] L.J. Turgeon, J.R. Mathews, "A Bipolar Transistor Model of Quasi-Saturation for Use in


Chapter 6  

*Improvement of the high-current HF distortion of compact bipolar epilayer models*

---

### 6.1 Introduction

In this chapter, an extension to the collector charge description for compact bipolar epilayer models is presented. With this extension, monotonic $f_T$ and Early-voltage behaviour is ensured when transistor operation extends into the quasi-saturation region. The modification leads to a major improvement in the modelling of nonlinear distortion at high-current levels and high frequencies.

It was shown in Chapter 4 that compact bipolar epilayer models, like Mextram, give a significant improvement in the modelling of the high-current region of the DC characteristics. However, these improved epilayer models [6.1,6.2,6.5] are particularly sensitive to the parameter values with respect to their AC characteristics; slight deviations may produce erratic, nonmonotonic Early voltages and $f_T(I_C)$ behaviour (see e.g. figures 6.9 and 6.10). In practice, epilayer parameter sets, especially $V_{DC}$, are extracted to obviate nonmonotonic behaviour, but this may result in the improper modelling of nonlinear distortion at high-current levels as explained in Chapter 5. This chapter explores the underlying causes of these problems and proposes an improved formulation for the collector charge model. To this end, the Mextram model [6.3,6.5] has been modified by adding an extra charge $\Delta Q_c$, which yields better modelling of signal distortion at high-current levels and high frequencies and monotonicity in Early voltages and $f_T$ fall-off characteristics.

In order to make the problem more tractable and to help in finding a mathematical formulation for this extra charge $\Delta Q_c$, we consider the AC signal transfer of a bipolar transistor with a lightly doped epilayer.
6.2 Analysis of the low-frequency small-signal transfer

At low frequencies and low driving conditions, the distortion behaviour of a device can be studied by investigating the derivatives of the AC transfer characteristics with respect to the base-emitter input voltage. Carrying this out by using a strongly simplified circuit of a bipolar epilayer transistor model (see Figure 5.2) was discussed in the previous chapter. In this chapter, which treats the high-frequency distortion properties, we use the same circuit for our analysis, but now we take into account the internal base-collector charge $Q_c$ (see Figure 6.1). Note that for the very low frequencies used in the previous chapter $Q_c$ have no effect and can be set to zero.

![Circuit Diagram]

**Figure 6.1.** Simplified circuit model of a bipolar transistor with a lightly doped epilayer

As found in the previous chapter, the functions involved for the low-frequency small-signal transfer are the main current $I_n(V_{b2e1}, V_{b2c2})$ and the epilayer current $I_{epi}(V_{b2c2}, V_{b2c1})$. Solving for the small-signal transconductance, $i_{epi} / v_{b2e1}$ yields the original result of equation (5.4) (see page 94 of the previous chapter).

$$\left. \frac{i_{epi}}{v_{b2e1}} \right|_{v_{c2e1}} = g_x + g_y \left[ \frac{g_{epiz} - g_x}{g_y - g_{epiz}} \right]$$  \hspace{2cm} (6.1)

This result can be rewritten for later convenience, to:

$$\left. \frac{i_{epi}}{v_{b2e1}} \right|_{v_{c2e1}} = g_{epi} \left[ \frac{g_{epiz} - g_x}{g_y - g_{epiz}} \right] + g_{epiz}$$  \hspace{2cm} (6.2)

Plotting equation (6.1) or (6.2) as a function of the DC collector current ($I_{epi}$) yields information on the influence of the epilayer parameters on the distortion behaviour as given in Figures 5.3 and 5.4 of Chapter 5. Note that we end here with a slightly different notation for the transconductance. It will be seen in the next section that this notation is better suited for the transconductance found at high frequencies.
6.3 Analysis of the high-frequency small-signal transfer

At higher frequencies, the base-collector depletion charge \(Q_{bc}\) becomes one of the dominant factors in the AC signal transfer when the transistor enters quasi-saturation (note that the diffusion storage charge \(Q_{bc}\) will only have a significant value when the transistor is already in q.s.). The AC signal transfer is calculated using the circuit shown in Figure 6.1. The functions involved are now: \(I_n(V_{b2e1}, V_{b2e2}), I_{epi}(V_{b2e2}, V_{c1b2})\) and \(Q_{bc}(V_{b2e2}, V_{b2e1})\). Concentrating on the small-signal transfer we use \(i_n, i_{epi}\) as defined in equations (5.1) and (5.2). The small-signal collector charge \(q_c\) is defined below:

\[
q_c = c_y v_{b2e2} + c_z v_{b2e1}
\]  

with:

\[
c_y = \left. \frac{\delta Q_{bc}}{\delta V_{b2e2}} \right|_{v_{b2e1}} \quad c_z = \left. \frac{\delta Q_{bc}}{\delta V_{b2e1}} \right|_{v_{b2e2}}
\]

The physical significance of \(c_y\) and \(c_z\) is considered in Appendix A.

Due to the shorted output (\(v_{b2e1} = v_{b2e2}\)), we can again solve for the transconductance \((i_{epi}/v_{b2e1})\), and find in place of equation (6.1):

\[
\frac{i_{epi}}{v_{b2e1}} = (j\omega c_z + g_{epiz} - g_y) \left[ \frac{g_{epiy}}{g_y - (g_{epiy} - j\omega c_y)} \right] + g_{epiz} = f_1
\]

(6.5)

Plotting \(i_{epi}/v_{b2e1}\) as a function of the DC collector current for sufficiently high values of \(\omega c_y\), we find (given lower values of the built-in base-collector voltage \(V_{DC}\)) nonmonotonic behaviour at the onset of q.s. (see Figure 6.2). This is caused by the current-dependent behaviour of the multiplication term between square brackets in equation (6.5); rewriting:

\[
\left[ \frac{g_{epiy}}{g_y - (g_{epiy} - j\omega c_y)} \right] = \frac{1}{g_y - 1 + j\omega c_y} = f_2
\]

(6.6)

In Figure 6.3, \(f_2\) is plotted as a function of the DC collector current \(I_c(=i_{epi})\). For reasons of simplicity, Figures 6.2 and 6.3 have been computed at 1 GHz with \(c_y\) constant and hot carrier effects omitted. The values for \(R_{cv} = S_{CRCV} = 30\ \Omega\) and \(c_y = 4\ \text{pF}\) are chosen such that a clear graphical illustration of the nonmonotonic behaviour is obtained. For low values of \(V_{DC}\) (e.g. 0.7 V), \(g_y\) will have a negligible value and there will be a sudden rise when q.s. sets in \((V_{b2e2}=V_{DC})\). This can be suppressed by taking a higher value of \(V_{DC}\) (e.g. 0.8V), see Figure 6.3, but this will lead to incorrect modelling of distortion [6.7, 6.9]. The sudden rise in \(f_2\) is due to the decrease of the time constant \(c_y/g_{epiy}\) which falls to a low value when the epilayer resistance suddenly drops in q.s. The same nonmonotonic behaviour can be found in the \(f_T(I_c)\) characteristics (e.g. see Figure 6.10).
Analysis of the high-frequency small-signal transfer

![Figure 6.2](image1)  
**Figure 6.2.** Normalized transconductance \( f_l/g_x \) as function of the DC current using the Mextram epilayer model with \( I_{HC} \to \infty \) so that \( S_{CRCV} = R_{CV} \)

![Figure 6.3](image2)  
**Figure 6.3.** Function \( f_2 \) plotted as function of the DC current

The drop in epilayer resistance is best illustrated by plotting \( g_{epiy} \) as a function of \( l_{epi} \) (see Figure 6.4). It starts at a value of \( 1/R_{CV} \) and slowly decreases to \( 1/S_{CRCV} \) until at q.s. the \( g_{epiy} \) sharply rises (hot carrier effects are now included). For a given \( l_{epi} \), \( g_{epiy} \) can be split into a nonsaturated part \( g_{epi ns} \) and a q.s. part \( \Delta g_{epi} \).
We define:

\[
g_{\text{epi} \ ns} = \frac{\delta I_{\text{epi} \ ns}}{\delta V_{b2c1}} V_{b2c1} \quad \Delta g_{\text{epi}} = \frac{\delta \Delta I_{\text{epi}}}{\delta V_{b2c1}} V_{b2c1}
\]

(6.7)

with:

\[
\Delta I_{\text{epi}} = I_{\text{epi}} - I_{\text{epi} \ ns}
\]

(6.8)

The epilayer current \( I_{\text{epi}} \) is given for various epilayer models in Table 4.7 on page 73. \( I_{\text{epi} \ ns} \) represents the nonsaturated part of the epilayer current \( I_{\text{epi}(E_C=0)} \) (\( E_C \) set to zero). To ensure monotonic behaviour, we add an extra capacitance \( \Delta c \) such that the time constant:

\[
\frac{c_y}{g_{\text{epi}}} \Rightarrow \frac{c_y + \Delta c}{g_{\text{epi}}} = \frac{c_y + \Delta c}{g_{\text{epi} \ ns} + \Delta g_{\text{epi}}} = \frac{c_y}{g_{\text{epi} \ ns}} \left(1 + \frac{\Delta c}{c_y}ight)
\]

(6.9)

behaves properly. This is the case if:

\[
\left(\frac{\Delta c}{c_y} = \frac{\Delta g_{\text{epi}}}{g_{\text{epi} \ ns}}\right) \Rightarrow \Delta c = \frac{\Delta g_{\text{epi}}}{g_{\text{epi} \ ns}} c_y
\]

(6.10)

The required extra charge \( \Delta Q_c \), ensuring monotonic Early voltages and \( f_T(I_C) \) behaviour is now given by:
\[
\Delta Q_c(V_{b2c2}, V_{b2c1}) = \int_{0}^{V_{b2c2}} c_y \frac{\Delta g_{epi}}{g_{epi ns}} \bigg|_{V_{b2c1}} dV_{b2c2}
\]  

(6.11)

Physically speaking, \(\Delta Q_c\) represents charge stored in the space-charge region around the base-collector junction at high-current levels. This additional charge can, depending on the value of \(V_{DC}\), dominate over the base-collector diffusion charge (\(Q_{bc}\)) at the onset of q.s. Deeper in saturation, \(Q_{bc}\) will become dominant over \(\Delta Q_c\). This is illustrated in Figure 6.5 where \(\Delta Q_c\) and the \(Q_{bc}\) are plotted as a function of the DC collector current.

![Figure 6.5. The charge functions \(\Delta Q_c\) and \(Q_{bc}\) obtained with the improved Mextram model](image)

Finally, in order to ensure an analytical computation, the integral in equation (6.11) can be simplified into an analytical expression by noting that \(c_y(V_{b2c2}, V_{b2c1})\) and \(g_{epi ns}(V_{b2c2}, V_{b2c1})\) are slowly varying functions compared to \(\Delta g_{epi}(V_{b2c2}, V_{b2c1})\),

\[
\Delta Q_c(V_{b2c2}, V_{b2c1}) = c_y \frac{V_{b2c2}}{g_{epi ns}} \Delta g_{epi ns} \bigg|_{V_{b2c1}} dV_{b2c2}
\]

(6.12)

which is equal to:

\[
\Delta Q_c(V_{b2c2}, V_{b2c1}) = c_y \frac{\Delta I_{epi}(V_{b2c2}, V_{b2c1}) - \Delta I_{epi}(0, V_{b2c1})}{g_{epi ns}}
\]

(6.13)

The maximum difference between the \(\Delta Q_c\)'s from equations (6.11) and (6.13) is about 10%. Note that with the aid of (6.13), the charge function \(\Delta Q_c\) can, based on the functional description of the base-collector depletion capacitance (\(c_y\)) and the epilayer current (\(I_{epi}\)), be calculated analytically. Using this formulation, \(\Delta Q_c\) is not restricted to a specific epilayer model and can be calculated based on one of the models of [6.1,6.3,6.5]. The calculation of \(g_{epi ns}\) is explained in more detail in Appendix B).
6.4 The base-collector depletion capacitance

From the derivation of $\Delta Q_c$, it is clear that the new charge function depends strongly on the value of the base-collector depletion capacitance $c_y$ in q.s. Consequently, in order to obtain a realistic behaviour of the charge function $\Delta Q_c$, the base-collector depletion capacitance should be very well behaved at this point. To achieve an optimum behaviour of $\Delta Q_c$, we have modified the base-collector capacitance for its current dependency around ($V_{b2c2}=V_{DC}$). The base-collector function used in the previous Mextram model is normalized for the zero junction capacitance and shown in Figure 6.6, the modified function is shown in Figure 6.7.

![Figure 6.6. Original base-collector capacitance function of the Mextram Model](image1)

![Figure 6.7. Modified base-collector capacitance function of the Mextram Model](image2)
As can been seen in Figure 6.6 and Figure 6.7, the modified capacitance function exhibits a less pronounced peaking around \( V_{b_{2DC}}=V_{DC} \) for higher collector currents\(^1\). The final formulation of the modified base-collector depletion charge takes into account the finite thickness of the epilayer and the current modulation [6.3,6.5] and is given in Table 4.2, "Useful functions for the Mextram model," on page 62.

### 6.5 Results

The Mextram version 503.1 and the newly modified Mextram model calculations are compared with data obtained by using the 2D device simulator Medici [6.4]. The transistor structure in these simulations, described in [6.6], is based on SIMS measurements and is representative of present-day bipolar transistor technology. By using this method, we avoid the difficulty of performing a pulsed distortion measurement (in order to avoid self-heating) at high frequencies and high-current levels. The simulations with the Mextram model were performed with Hewlett Packard's Microwave Design System (MDS). To illustrate the effect of \( \Delta Q_c \), one parameter set has been used was optimized for the modified Mextram model. The Figures 6.4 to 6.12 all refer to the same transistor structure (1x1 \( \mu \)m emitter area) with the following epilayer parameters:

\[
\begin{align*}
R_{CV} & = 1.20e+4 \, \Omega \\
S_{CRCV} & = 4.17e+4 \, \Omega \\
I_{HC} & = 3.93e-5 \, A \\
V_{DC} & = 0.64 \, V \\
S_{FH} & = 0.53 
\end{align*}
\]

**DC characteristics**

The base-collector charge \( \Delta Q_c \) is present in the total majority base charge \( Q_b \) that controls the main current \( I_n \). This leads, when comparing the new version of Mextram with the previous version, to some reduction of the collector current \( (\Delta I_n) \) in the q.s. region (see Figure 6.8). Using the improved model, monotonous behaviour of the Early voltages is now ensured: see Figure 6.9.a and Figure 6.9.b.

---

\(^1\) Note that the current dependency of \( Q_{TC} \) is not realized by using the actual epilayer current \( (I_{ep}) \) but is replaced for reasons of simplicity by an approximating current function \( I_{CAP} \) which as upper limit that approaches the value of \( I_{HC} \) for very high values of the epilayer voltage.
Figure 6.8. $I_c(V_{ce})$ characteristic using the previous and the improved Mextram model, compared to Medici

Figure 6.9. Early-voltage characteristics
AC characteristics

At high frequencies, addition of $\Delta Q_C$ prevents the drop in the collector charging time ($c_y/g_{epiy}$) and leads, consequently, to monotonic $f_T$ characteristics (see Figure 6.10.b).

![Graphs showing AC characteristics](image)

**Figure 6.10.** $f_T(I_C)$ calculated using Medici for a device of 1 $\mu$m length and Mextram

Distortion

The monotonic $f_T$-characteristics result in improved modelling of distortion as is illustrated in Figure 6.12. In this figure, the second-order distortion component in the collector current is shown for a 10 mV 1 GHz input signal with the collector-base voltage maintained constant at 1 V. The circuit topology used for this simulation is given in Figure 6.11. In Figure 6.13, it may be seen that, using the previous Mextram, fitting the $f_T(I_C)$ characteristic by increasing the built-in base-collector voltage $V_{DC}$ leads to a better fit in the $f_T$-characteristics but to a too high level of distortion in the q.s. region (see Figure 6.14).

![Circuit diagram for distortion](image)

**Figure 6.11.** Configuration used for the distortion calculation with the Medici program

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Figure 6.12. The magnitude of the second-order component of the collector current compared to Medici using the previous and improved version of the Metram model with $V_{DC}$ set to 0.64 V.

Figure 6.13. $f_T(I_C)$ calculated using Medici and the previous version of Mextram (503.1) for $V_{DC}=0.64$V and $V_{DC}=0.69$V.
Figure 6.14. The magnitude of the second-order component of the collector current compared to Medici using the previous Mextram model for two different values of $V_{DC}$ (0.64 V and 0.69 V).

Finally, it can be stated that with this extension of the base-collector charge formulation, the physical nature of the Mextram model allows now an accurate fit of all the characteristics at low (1 MHz) as well as at high frequencies (1 GHz). This is illustrated in Figure 6.15 and Figure 6.16 by plotting the higher-order harmonics as a function of the DC collector current for the base-collector voltages: 0, -1 and -3 volt. If we consider for the sake of comparison the VBIC95 model, we note that, unless there is a reasonable fit of the $f_T(I_C)$ characteristics (see Figure 4.13), the VBIC95 fails to describe the higher-order harmonics (see Figure 6.15 and Figure 6.16). This is caused by the fact that for the VBIC95 model, the fit of the $f_T(I_C)$ characteristics is achieved by manipulating the delay time $\tau_F$ while the higher-order harmonics are strongly dependent on the epilayer behaviour.
Figure 6.15. Distortion components in the collector current, according to Medici, Mextram and VBIC95 at 1 MHz, as function of the DC collector current for the collector-base voltages 0, 1 and 3 V. The input signal voltage is 10 mV.
Figure 6.16. Distortion components in the collector current, according to Medici, Mextram and VBIC95 at 1 GHz, as function of the DC collector current for the collector-base voltages 0, 1 and 3 V. The input signal voltage is 10 mV.
6.6 Conclusions

Incorporation of $\Delta Q_c$ in the Mextram model yields, even for low values of $V_{DC}$, a compact transistor model with improved modelling of the Early voltages and the $f_T(l_c)$ fall-off. Without requiring any additional parameters, greater flexibility is obtained in the modelling of the high-current region of the bipolar transistor with lightly doped epilayer. This leads to an improved modelling of the distortion behaviour at high frequencies when the transistor operation extends into the quasi-saturation region. Implementation of this model in Hewlett Packard’s simulator package MDS has resulted in a very powerful combination, which facilitates the use of harmonic balance techniques in strongly nonlinear bipolar circuit design.

Appendix A) The physical meaning of $c_y$ and $c_z$

In nonquasi-saturation, the collector charge is a function of $v_{b2c2}$ and $i_{epi\ ns}$ (see equations (6.7) and (6.17)) and the small-signal value becomes:

$$q_c = c_T \cdot v_{b2c2} + \tau \cdot i_{epi\ ns} = (c_T + \tau \cdot g_{epi\ ns}) v_{b2c2} - (\tau \cdot g_{epi\ ns} \cdot v_{b2c1})$$  \hspace{1cm} (6.14)

With $i_{epi\ ns}$ given by,

$$i_{epi\ ns} = (v_{b2c2} - v_{b2c1}) g_{epi\ ns}$$  \hspace{1cm} (6.15)

It is easily shown that:

$$c_y = c_T + \tau \cdot g_{epi\ ns} \quad c_z = -\tau \cdot g_{epi\ ns}$$  \hspace{1cm} (6.16)

Here $c_T (=c_y+c_z)$ represents the collector depletion capacitance and $\tau$ ($=dQ_c/dl_{epi}$ at constant $V_{b2c2}$) is the delay of the mobile charge in the depletion region.
Appendix B) The formulation of $g_{epi\ ns}$

In our calculations, nonsaturated epilayer conductance $g_{epi\ ns}$ represents the derivative of the nonsaturated epilayer current ($E_c=0$) with respect to $V_{b2c2}$ (see equation (6.7)). Using the Kull model and omitting the hot carrier behaviour $g_{epi\ ns}$ is given simply by $1/R_{CV}$. However, when including hot carrier behaviour the formulation of $g_{epi\ ns}$ becomes more complicated. The nonsaturated epilayer current according the Mextram model is given by:

$$I_{epi\ ns} = I_{epi(E_c=0)} = \frac{I_{HC}S_{CRCV}V_{c1c2} + V_{c1c2}^2}{S_{CRCV}(I_{HC}R_{CV} + V_{c1c2})} \quad (6.17)$$

In which $V_{c1c2}$ represents the voltage drop over the epilayer:

$$V_{c1c2} = V_{b2c1} - V_{b2c2} \quad (6.18)$$

Calculating $g_{epi\ ns}$ using (6.7) and (6.17) and plotting it as a function of $V_{c1c2}$ yields the situation shown in Figure 6.17. As can be observed in this figure, $g_{epi\ ns}$ represents a continuously decreasing function in respect to the epilayer voltage drop ($V_{c1c2}$).

![Figure 6.17. The nonsaturated epilayer conductance as function of the voltage drop over the epilayer](image)

In Figure 6.18, the internal node voltages are plotted as function of the DC collector current while the external collector-emitter voltage is kept constant. As can be seen from this figure, the epilayer voltage drop ($V_{c1c2}$) increases up to the point were the internal base-collector junction becomes forward biased and q.s. sets in. At the onset of q.s., $V_{c1c2}$ will have its highest value, when going deeper in q.s. $V_{c1c2}$ will decrease yielding to an increase of $g_{epi\ ns}$ (see Figure 6.17). When $g_{epi\ ns}$ rises, $\Delta Q_c$ will decrease, this effect is undesired because it can lead, for devices with a large ratio between $S_{CRCV}$ and $R_{CV}$ to an unrealistic increase of the high-frequency transfer just before the device enters hard saturation.
In order to ensure a monotonic decreasing value for \( g_{epl \, ns} \) even when the transistor is in q.s., we have calculated the fictive epilayer voltage drop using the total epilayer current as if the transistor were not in q.s. Thus therefore solving \( V_{(E_c=0)} (=V_{c1c2} \text{ for } E_c=0) \) from the quadratic equation of (6.17) and using the total epilayer current gives us a monotonic decreasing function for \( g_{epl \, ns} \) given by:

\[
g_{epl \, ns} = \frac{S_{CRCV}(V_{(E_c=0)} + I_{HC}R_{CV})^2}{V_{(E_c=0)}^2 + 2V_{(E_c=0)}I_{HC}R_{CV} + S_{CRCV}(I_{HC}^2R_{CV})} \quad (6.19)
\]

The function (6.19) is used in the calculation of \( \Delta Q_c \) as given in (6.13).
6.7 References


Chapter 7  Stability of wide-band amplifier configurations

7.1 Introduction

Very high bit rates are required in present-day telecommunication system applications. This has led to a growing need for inexpensive circuits offering very wide-band signal handling capability. In this chapter we concentrate on one of the basic building blocks, the amplifier. The question of stability is central to any serious discussion of amplifier design, this is particularly relevant in the presence of frequency-dependent parasitics. Mounting parasitics limit the full exploitation of the potential gain-bandwidth product (GB) of modern HF silicon process technology. For this reason, minimization of package-related parasitics like bondwire inductance and pin-to-pin capacitance is highly desirable. Reformulation of the problem in generic terms has facilitated the derivation of a set of explicit guidelines for the designer in respect to the IC mounting configuration and circuit topology, thus minimizing the influence of parasitics.

7.2 The stability factor $K$

The stability of an amplifier or its resistance to oscillation can be determined from s-parameters, the matching networks, and the terminations. In a two-port network, oscillations are possible when either the input or output port presents a negative resistance. This occurs when the magnitude of the in- or output reflection coefficient is larger than one ($|\Gamma_{IN}| > 1$ or $|\Gamma_{OUT}| > 1$). In the case of an unilateral amplifier ($s_{12}=0$), or an amplifier connected with a perfect match, these conditions on the reflection coefficients can be replaced by: $|s_{11}| > 1$ and $|s_{22}| > 1$. 

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The stability factor $K$

![Two-port amplifier](image)

**Figure 7.1.** Two-port amplifier with in- and output ports

If one requires for an amplifier that $|\Gamma_{IN}| < 1$ or $|\Gamma_{OUT}| < 1$ for all possible passive in- and output terminations, the amplifier is said to be unconditionally stable, which can be expressed by the Rollett stability factor $K$ [7.1,7.2] which is equal to $1/C_L$ ($C_L$ is the Linvill stability factor). This factor is mostly expressed in the s-parameters with the following definition:

$$K = \frac{1 - |s_{11}|^2 - |s_{22}|^2 + |\Delta|^2}{2|s_{21}s_{12}|} \quad (7.1)$$

where

$$\Delta = s_{11}s_{22} - s_{21}s_{12} \quad (7.2)$$

If $K > 1$ and $|\Delta| < 1$ the amplifier will be stable for all possible passive in- and output terminations.

A graphical illustration of the relationship between the stability factor $K$, in- and output matching and the gain isolation product as proposed in [7.3] is illustrated in Figure 7.2. In this figure, it is assumed (for simplicity) that $s_{11}$ equals $s_{22}$ and all s-parameters have zero phase. The vertical axis represent the product of the magnitude of the forward gain ($s_{21}$) and the isolation ($s_{12}$). The use of this graph is simple, e.g., if the forward gain ($s_{21}$) is 60 dB and the return losses ($s_{11}$, $s_{22}$) are -10 dB, the isolation ($-20\log|s_{12}|$) should be larger than 67 dB. In practice, however, it is wise to maintain a safety margin. In [7.12] a margin of 20 dB between $s_{21}$ and $-s_{12}$ is proposed.
Figure 7.2. Conditions for absolute stability \((K>1)\) as function of the matching and isolation.

As can be observed in Figure 7.2, unconditionally stable circuit operation for high-gain amplifiers requires low return losses and high isolation between in- and output. In practice, the isolation \((-s_{12})\) will always be limited by mounting parasitics, which restricts the maximum achievable gain bandwidth product \((GB_{max})\) for stable operation. The influence of relatively small parasitics can limit \(GB_{max}\) seriously as illustrated in the following example:

- Assume an amplifier with \(K>1\) and an output-to-input mounting capacitance of only 10 fF. The isolation \((-20\log|s_{12}|)\) decreases with frequency and limits the \(GB_{max}\) to approximately 300 GHz (e.g. an amplifier with 40 dB gain \((s_{21}=100)\) and 3 GHz bandwidth).

Stable single-chip amplifiers with a much larger gain-bandwidth product have, however, been reported in the literature [7.12,7.13]. These remarkable results are attributable to the cancellation of the dominant mounting parasitics, through careful design which significantly improves the output-to-input isolation.

Although the design of high-performance wide-band amplifiers is of topical interest [7.3,7.4,7.7,7.8,7.9,7.12,7.13,7.14], most recent papers concentrate on the amplifier response and are often vague or consider only in a general way aspects related to stability. The graphical evaluation of Figure 7.2 and the example above are incomplete, in that they ignore the influence of s-parameter phase behaviour on the stability. This conclusion is even more valid when considering the stability of high-gain wide-band balanced amplifiers. In this chapter, a methodology is introduced for studying stability conditions of single-ended amplifiers, balanced amplifiers under differential operation as well as in nondifferential operation. The analysis uses an ideal amplifier block with arbitrary gain and phase. In studying the stability conditions in nondifferential operation, we consider a variety of inner amplifier topologies. In our approach, idealized amplifier blocks are placed in a network representa-
tive of an actual mounting situation on a printed circuit board. The value of the mounting parasitics and their equivalent circuit values were found by using Sonnet's program EM.

For the analytical derivations, we have used the MAPLE program, numerical verification was carried out with the MDS program.

7.3 The single-ended and balanced amplifier with their internal topologies

In our stability analysis, we consider the following three types of amplifier operation, namely:

- The single-ended amplifier (see Table 7.1.a).
- The balanced amplifier in differential operation (see Table 7.1.b). This situation represents the normal operational mode of an amplifier in a wide-band telecommunication system.
- The balanced amplifier in unbalanced operation (see Table 7.1.c). This situation is common in the traditional testing of wide-band amplifiers. Unbalanced testing is required since commercial two-port network analysers are defined in respect to ground. In order to make a balanced measurement using a conventional network analyser, power splitters and phase shifters can be applied (see [7.12]). An alternative approach is to perform a four-port characterization\(^1\) and reduce the matrix obtained to a two-port as indicated in Table 7.1.

In order to facilitate an analytical treatment of the stability problem and for reasons of convenience, a number of assumption are made, namely:

- The y-parameter representation is used for the definition of the amplifier configurations.
- The characteristic system admittance of the in- and output ports are equal ($y_0$).
- The port admittance of the single-ended amplifier equals the port admittance in unbalanced operation ($y_0 = y_{unb}$).
- The port admittance for an amplifier in differential (balanced) operation is half the port admittance of the unbalanced configuration ($Y_{bal} = y_0/2$).

---

\(^1\) With a set of six two-port s-parameter measurements, the complete four-port matrix can be determined. If symmetry with respect to ground is assumed only four two-port measurements are required. Note that the ports which are not connected to the network analyser should be terminated with the characteristic impedance.
### TABLE 7.1. Amplifier operation and two-port representation

<table>
<thead>
<tr>
<th>Amplifier operation</th>
<th>two-port representation (for symmetrical four-port)</th>
</tr>
</thead>
<tbody>
<tr>
<td>a) Single-ended amplifier</td>
<td>$\begin{bmatrix} s_{11} &amp; s_{12} \ s_{21} &amp; s_{22} \end{bmatrix}<em>{\text{single}}$ or $\begin{bmatrix} y</em>{11} &amp; y_{12} \ y_{21} &amp; y_{22} \end{bmatrix}_{\text{single}}$</td>
</tr>
<tr>
<td>b) Balanced amplifier in differential operation</td>
<td>$\begin{bmatrix} s_{11} &amp; s_{12} \ s_{21} &amp; s_{22} \end{bmatrix}<em>{\text{diff}} = \begin{bmatrix} (s</em>{11} - s_{12}) &amp; (s_{13} - s_{14}) \ (s_{23} - s_{24}) &amp; (s_{44} - s_{43}) \end{bmatrix}<em>{\text{4-port}}$ $\begin{bmatrix} y</em>{11} &amp; y_{12} \ y_{21} &amp; y_{22} \end{bmatrix}<em>{\text{diff}} = \begin{bmatrix} (y</em>{11} - y_{12}) &amp; (y_{13} - y_{14}) \ 2 &amp; 2 \ (y_{31} - y_{32}) &amp; (y_{33} - y_{34}) \ 2 &amp; 2 \end{bmatrix}_{\text{4-port}}$</td>
</tr>
<tr>
<td>c) Balanced amplifier in unbalanced operation (testing conditions)</td>
<td>$\begin{bmatrix} s_{11} &amp; s_{12} \ s_{21} &amp; s_{22} \end{bmatrix}<em>{\text{unbal}} = \begin{bmatrix} s</em>{11} &amp; s_{13} \ s_{31} &amp; s_{33} \end{bmatrix}_{\text{4-port}}$</td>
</tr>
</tbody>
</table>

Note that $Y_{\text{unb}} = 2Y_{\text{bal}} = y$

Further, we assume ideal amplifier blocks with a perfect output-to-input isolation. During the analysis, we consider four types of internal amplifier structure, namely, the ideal single-ended amplifier shown in Table 7.2.a, the internal floating structure of Table 7.2.b, the internal grounded amplifier given in Table 7.2.c and the amplifier block with grounded input and floating output (see Table 7.2.d). The gain of the ideal amplifier (A) is taken to be a complex number with arbitrary phase. This is required because, in realistic HF wide-band amplifiers, the phase of $s_{21}$, as a function of frequency, can pass 360 degrees several times. Note that the amplifiers with a floating output have a perfect common-mode rejection, this in contrast with the internal grounded amplifier which has no rejection of common-mode signals at all.
TABLE 7.2. Internal amplifier structures

<table>
<thead>
<tr>
<th>Schematics</th>
<th>([Y_{amp}])</th>
</tr>
</thead>
<tbody>
<tr>
<td>a) Two-port amplifier</td>
<td>([Y_{amp}]_{\text{single}} = \begin{bmatrix} \gamma_0 &amp; 0 \ -\gamma A &amp; \gamma_0 \end{bmatrix} )</td>
</tr>
<tr>
<td><img src="image" alt="Two-port amplifier diagram" /></td>
<td>(I = U_{in} A \gamma_0)</td>
</tr>
</tbody>
</table>

| b) Four-port amp. with floating structure | \([Y_{amp}]_{\text{float}} = \begin{bmatrix} \frac{\gamma_0}{2} & \frac{\gamma_0}{2} & 0 & 0 \\ -\frac{\gamma_0}{2} & -\frac{\gamma_0}{2} & 0 & 0 \\ \frac{A \gamma_0}{2} & \frac{A \gamma_0}{2} & \frac{\gamma_0}{2} & \frac{\gamma_0}{2} \\ \frac{A \gamma_0}{2} & \frac{A \gamma_0}{2} & -\frac{\gamma_0}{2} & -\frac{\gamma_0}{2} \end{bmatrix} \) |
| ![Four-port amplifier diagram](image) | \(I = (U_{\text{ina}} - U_{\text{inh}}) A \gamma_{\text{bal}}\) |

| c) Four-port amp. with internally grounded structure | \([Y_{amp}]_{\text{gnd}} = \begin{bmatrix} \gamma_0 & 0 & 0 & 0 \\ 0 & \gamma_0 & 0 & 0 \\ 0 & 0 & -A \gamma_0 & 0 \\ 0 & 0 & 0 & -A \gamma_0 \end{bmatrix} \) |
| ![Four-port amplifier diagram](image) | \(I_a = U_{\text{ina}} A \gamma_{\text{unb}}\) \(I_b = U_{\text{inh}} A \gamma_{\text{unb}}\) |

| d) Four-port amp. with grounded input and floating output | \([Y_{amp}]_{\text{gnd\&float}} = \begin{bmatrix} \gamma_0 & 0 & 0 & 0 \\ 0 & \gamma_0 & 0 & 0 \\ \frac{A \gamma_0}{2} & \frac{A \gamma_0}{2} & \frac{\gamma_0}{2} & \frac{\gamma_0}{2} \\ \frac{A \gamma_0}{2} & \frac{A \gamma_0}{2} & -\frac{\gamma_0}{2} & -\frac{\gamma_0}{2} \end{bmatrix} \) |
| ![Four-port amplifier diagram](image) | \(I = \frac{1}{2}(U_{\text{ina}} - U_{\text{inh}}) A \gamma_{\text{bal}}\) |
From Figure 7.2, it follows that it is important to match the input and output of the amplifier to its characteristic port admittance. For the single-ended amplifier, this matching admittance is simply \( y_0 \), in the case of a balanced design, however, two sorts of port admittance can be considered, namely, the balanced admittance \( (Y_{bal} = y_0 / 2) \) of Table 7.1.b and the unbalanced admittance \( (Y_{unb} = y_0) \) of Table 7.1.c. Whether these port admittances can be matched simultaneously depends on the internal topology of the amplifier blocks. Note, for example, that the circuit shown in Table 7.2.c can be matched both in differential mode and unbalanced mode simultaneously. This in contrast with the circuit given in Table 7.2.b, which can only be matched for balanced operation. Under the condition that \( Y_{unb} = 2Y_{bal} \), the in- and output match \( (s_{11} \text{ and } s_{22}) \) for the configuration depicted in Table 7.2.b will be \(-6 \text{ dB}\). The choice of a grounded or floating amplifier structure depends on the frequency range, the gain required and the mounting parasitics as discussed later in this chapter.

7.4 Interconnects and capacitive mounting parasitics

In the case of a properly designed chip amplifier, the reverse isolation \((-20 \log |s_{12}|)\) is limited in practice by mounting parasitics. The principle factors are the capacitive and inductive coupling between input and output, feedback via the bias lines and ground connections. In this section, parasitic coupling between in- and outputs is considered.

7.4.1 Capacitive coupling

Capacitive parasitics consist of the of air and substrate terms related to the bondwires and the open ends of the interconnects, respectively. The capacitive open ends of these lines are believed to be dominant over the capacitive coupling of the bondwires (not to be confused with the inductive coupling of the bonding wires). In order to make an estimation of the capacitances involved, we consider the bare chip mounting situations of Table 7.3. In Table 7.3.a, the two interconnects separated by a gap are shown for a single-ended amplifier. The equivalent circuit for the open end parasitics is given below. The situation for the interconnects of a balanced amplifier together with an accompanying equivalent circuit are given in Table 7.3.b. Note that these configurations are determined by the parameters \( W, s, G, H \) and \( \varepsilon_r \).
<table>
<thead>
<tr>
<th>a) single-ended</th>
<th>b) balanced</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Physical structure</strong></td>
<td><strong>Physical structure</strong></td>
</tr>
<tr>
<td>![Diagram A]</td>
<td>![Diagram B]</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th><strong>Single-ended equivalent circuit parasitic capacitances</strong></th>
<th><strong>Balanced equivalent circuit parasitic capacitances</strong></th>
</tr>
</thead>
<tbody>
<tr>
<td>![Diagram C]</td>
<td>![Diagram D]</td>
</tr>
</tbody>
</table>

The two-port $Y$-matrix

$$[Y_{cap}]_{\text{single}} = j\omega \begin{bmatrix} c_{\text{series}} & -c_{\text{series}} \\
-c_{\text{series}} & (c_{\text{series}} + c_{\text{shunt}}) \end{bmatrix}$$

The four-port $Y$-matrix

$$[Y_{cap}]_{\text{bal}} = j\omega \begin{bmatrix} c_{\text{diag}} & -c_{\text{par}} & -c_{\text{series}} & -c_{\text{cross}} \\
-c_{\text{par}} & c_{\text{diag}} & -c_{\text{cross}} & -c_{\text{series}} \\
-c_{\text{series}} & -c_{\text{cross}} & c_{\text{diag}} & -c_{\text{par}} \\
-c_{\text{cross}} & -c_{\text{series}} & -c_{\text{par}} & c_{\text{diag}} \end{bmatrix}$$

with: $c_{\text{diag}} = c_{\text{series}} + c_{\text{cross}} + c_{\text{shunt}} + c_{\text{par}}$

**Figure 7.3.** Parasitic capacitive networks due to the connection lines

Later in this chapter, we find that the stability of an balanced amplifier is greatly improved if the parasitic feedback capacitances $c_{\text{series}}$ and $c_{\text{cross}}$ are equal (see Figure 7.3.b). We define the difference between these two feedback capacitances as:

$$c_{\text{diff}} = c_{\text{series}} - c_{\text{cross}} \quad (7.3)$$

It will be demonstrated that for balanced amplifiers $c_{\text{diff}}$ should be as small as possible. This
can only be accomplished when the in- and output lines (and pins) are narrowly spaced (s is small) and there is a wide separation between in- and output (G is large). Following from the previous section, a simultaneous match for the balanced amplifier under differential as well as under unbalanced operation (assuming the internal structure\(^1\) of Table 7.2.c \((2.Y_{bas}=Y_{unbl})\) can only be reached, if the balanced connection lines should be almost uncoupled, resulting in a wide spacing (s). From the above, it is clear that people will have to compromise in the spacing of s. In practice, however, when using a thin substrate with a high dielectric constant, the coupling between the lines is a strong decreasing function of the spacing s. Thus for relatively small values of s, the lines will already be almost uncoupled (e.g: for a substrate with \(\varepsilon_r = 9.6\), and a thickness \(t = 10\) mil (=254 \(\mu\)m) suitable line dimensions are \(W = 0.251\) mm and \(s = 0.5\) mm). When using a substrate with a lower dielectric constant, the modified connection line configuration of Figure 7.4 can be used [7.12]. Note that the taped sections should be short with respect to the wavelengths involved.

![Diagram](diagram.png)

**Figure 7.4.** Modified interconnection lines for balanced circuitry

**Calculation of the capacitance values**

The capacitive coupling between the open ends is very dependent on the physical dimensions and the dielectric constant of the substrate. We have calculated the capacitances for a number of dimensions and substrates using the Sonnet's EM program, see Table 7.4 and Table 7.5. Due to specification of the reference planes at the very end of the microstrip, lines \(c_{par}\) will be zero. It will be seen later in our analysis that the values of \(c_{shunt}\) and \(c_{par}\) are of little influence on the stability.

As can be noted from this table the value of \(c_{series}\) is very small. The worst-case condition exists (a high value of \(c_{series}\)) when using a thick substrate with a low dielectric constant. Consequently, the use of a thin substrate with a high dielectric constant is highly recommended for wide-band amplifier circuits.

---

1. Due to the fact that the amplifier cell with the floating architecture cannot simultaneously be matched for balanced and unbalanced operation, there are no fixed relations for the coupling of the connection lines.
## TABLE 7.4. $c_{\text{shunt}}$, $c_{\text{series}}$ and $c_{\text{cross}}$ for different types of substrates (gaps 2, 3 and 4 mm)

<table>
<thead>
<tr>
<th>Substrate Type</th>
<th>$H$ (mm)</th>
<th>$W$ (mm) (50 Ω)</th>
<th>$G$</th>
<th>$c_{\text{shunt}}$ (pF)</th>
<th>$c_{\text{series}}$ (pF)</th>
<th>$c_{\text{cross}}$ (pF)</th>
<th>$c_{\text{diff}}$ (pF)</th>
<th>$Y_{\text{single}}$ (10GHz) (50 Ω)</th>
<th>$Y_{\text{diff}}$ (10GHz) (50 Ω)</th>
</tr>
</thead>
<tbody>
<tr>
<td>A) epoxy</td>
<td>0.8</td>
<td>1.29</td>
<td>2 mm</td>
<td>33.4</td>
<td>1.51</td>
<td>0.653</td>
<td>0.857</td>
<td>4.7e-3</td>
<td>2.7e-3</td>
</tr>
<tr>
<td>(ε=5.5)</td>
<td>3 mm</td>
<td>34.6</td>
<td>0.462</td>
<td>0.257</td>
<td>0.197</td>
<td>1.4e-3</td>
<td>6.4e-4</td>
<td></td>
<td></td>
</tr>
<tr>
<td>(s=1.0 mm)</td>
<td>4 mm</td>
<td>34.7</td>
<td>0.169</td>
<td>0.096</td>
<td>0.033</td>
<td>4e-4</td>
<td>1e-4</td>
<td></td>
<td></td>
</tr>
<tr>
<td>B) ceramic</td>
<td>0.635</td>
<td>0.629</td>
<td>2 mm</td>
<td>29.5</td>
<td>0.454</td>
<td>0.257</td>
<td>0.197</td>
<td>1.4e-3</td>
<td>6.2e-4</td>
</tr>
<tr>
<td>(ε=9.6)</td>
<td>3 mm</td>
<td>29.9</td>
<td>0.129</td>
<td>0.096</td>
<td>0.033</td>
<td>4e-4</td>
<td>1e-4</td>
<td></td>
<td></td>
</tr>
<tr>
<td>(s=1.0 mm)</td>
<td>4 mm</td>
<td>29.9</td>
<td>0.048</td>
<td>0.039</td>
<td>0.009</td>
<td>1.5e-4</td>
<td>2e-5</td>
<td></td>
<td></td>
</tr>
<tr>
<td>C) ceramic</td>
<td>0.254</td>
<td>0.251</td>
<td>2 mm</td>
<td>11.6</td>
<td>0.0359</td>
<td>0.0328</td>
<td>0.0031</td>
<td>1.1e-4</td>
<td>9.7e-6</td>
</tr>
<tr>
<td>(ε=9.6)</td>
<td>3 mm</td>
<td>11.6</td>
<td>0.0135</td>
<td>0.0128</td>
<td>0.0007</td>
<td>4.2e-5</td>
<td>2.2e-6</td>
<td></td>
<td></td>
</tr>
<tr>
<td>(s=0.5 mm)</td>
<td>4 mm</td>
<td>11.6</td>
<td>0.0055</td>
<td>0.0053</td>
<td>0.0002</td>
<td>1.7e-5</td>
<td>6.2e-7</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

## TABLE 7.5. $c_{\text{shunt}}$, $c_{\text{series}}$ and $c_{\text{cross}}$ for different types of substrates (gaps 2, 3 and 4 mm) using taped sections

<table>
<thead>
<tr>
<th>Substrate Type</th>
<th>$H$ (mm)</th>
<th>$W$ (mm) (strip)</th>
<th>$G$ (mm)</th>
<th>$c_{\text{shunt}}$ (pF)</th>
<th>$c_{\text{series}}$ (pF)</th>
<th>$c_{\text{cross}}$ (pF)</th>
<th>$c_{\text{diff}}$ (pF)</th>
<th>$Y_{\text{single}}$ (10GHz) (50 Ω)</th>
<th>$Y_{\text{diff}}$ (10GHz) (50 Ω)</th>
</tr>
</thead>
<tbody>
<tr>
<td>epoxy</td>
<td>0.8</td>
<td>0.25</td>
<td>2 mm</td>
<td>10.4</td>
<td>0.252</td>
<td>0.205</td>
<td>0.047</td>
<td>8e-4</td>
<td>1.5e-4</td>
</tr>
<tr>
<td>(ε=5.5)</td>
<td>3 mm</td>
<td>10.7</td>
<td>0.0758</td>
<td>0.0677</td>
<td>0.0081</td>
<td>2.4e-5</td>
<td>6e-6</td>
<td></td>
<td></td>
</tr>
<tr>
<td>(s=0.5 mm)</td>
<td>4 mm</td>
<td>10.7</td>
<td>0.0276</td>
<td>0.0257</td>
<td>0.0019</td>
<td>8.7e-5</td>
<td>3e-5</td>
<td></td>
<td></td>
</tr>
<tr>
<td>ceramic</td>
<td>0.635</td>
<td>0.25</td>
<td>2 mm</td>
<td>15.7</td>
<td>0.16</td>
<td>0.13</td>
<td>0.03</td>
<td>5e-4</td>
<td>9e-5</td>
</tr>
<tr>
<td>(ε=9.6)</td>
<td>3 mm</td>
<td>15.7</td>
<td>0.045</td>
<td>0.049</td>
<td>0.004</td>
<td>1.4e-4</td>
<td>3e-5</td>
<td></td>
<td></td>
</tr>
<tr>
<td>(s=0.5 mm)</td>
<td>4 mm</td>
<td>15.7</td>
<td>0.017</td>
<td>0.016</td>
<td>0.001</td>
<td>5.3e-5</td>
<td>3e-6</td>
<td></td>
<td></td>
</tr>
<tr>
<td>ceramic</td>
<td>0.254</td>
<td>0.25 (50 Ω)</td>
<td>2 mm</td>
<td>11.6</td>
<td>0.0359</td>
<td>0.0328</td>
<td>0.0031</td>
<td>1.1e-4</td>
<td>9.7e-6</td>
</tr>
<tr>
<td>(ε=9.6)</td>
<td>3 mm</td>
<td>11.6</td>
<td>0.0135</td>
<td>0.0128</td>
<td>0.0007</td>
<td>4.2e-5</td>
<td>2.2e-6</td>
<td></td>
<td></td>
</tr>
<tr>
<td>(s=0.5 mm)</td>
<td>4 mm</td>
<td>11.6</td>
<td>0.0055</td>
<td>0.0053</td>
<td>0.0002</td>
<td>1.7e-5</td>
<td>6.2e-7</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
7.4.2 Inductive coupling

When using bondwire technology for the connection of the amplifier chip to the test print, an inductive coupling between in and output is introduced. In order to estimate the introduced inductive coupling, we consider the situations depicted in Table 7.6.

<table>
<thead>
<tr>
<th>TABLE 7.6. Parasitic inductive networks due to the bondwires</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>a) single-ended</strong></td>
</tr>
<tr>
<td>Physical structure single-ended bondwire connection</td>
</tr>
<tr>
<td><img src="image1" alt="Single-ended bondwire connection" /></td>
</tr>
<tr>
<td>Equivalent circuit single-ended bondwire connection</td>
</tr>
<tr>
<td><img src="image3" alt="Equivalent single-ended bondwire" /></td>
</tr>
</tbody>
</table>

The inductance matrix for the single-ended connection is given by:

\[
[L]_{single} = \begin{bmatrix}
    l & -m_c \\
    -m_c & l
\end{bmatrix}
\]

The 4-port y connection is now defined as:

\[
[Y]_{ind, single} = \frac{1}{j\omega} \begin{bmatrix}
    [L]^{-1}_{single} & -[L]^{-1}_{single} \\
    -[L]^{-1}_{single} & [L]^{-1}_{single}
\end{bmatrix}
\]

The inductance matrix for the balanced connection is given by:

\[
[L]_{bal} = \begin{bmatrix}
    l & m_s & -m_{c1} & -m_{c2} \\
    m_s & l & -m_{c2} & -m_{c1} \\
    -m_{c1} & -m_{c2} & l & m_s \\
    -m_{c2} & -m_{c1} & m_s & l
\end{bmatrix}
\]

The 8-port y connection is now defined as:

\[
[Y]_{ind, bal} = \frac{1}{j\omega} \begin{bmatrix}
    [L]^{-1}_{bal} & -[L]^{-1}_{bal} \\
    -[L]^{-1}_{bal} & [L]^{-1}_{bal}
\end{bmatrix}
\]

Table 7.6 illustrates a chip bondwire connection for an unbalanced and a balanced amplifier IC. We have calculated the matrix components for the inductive network shown in Table 7.6b. For this calculation, we have assumed a substrate with zero thickness, which results in an almost closed loop of the bondwires with respect to ground. The closed loops are necessary to clearly define the integration path and bondwire excitation, this is needed to obtain a reliable result for the mutual inductance between the in- and output lines. Doing this, however, will lead to some deviation in the values of the inductances found, with this in

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mind, the values given in Table 7.7 should be considered as only an indication of the inductive coupling in reality.

The bondwire inductances are calculated by using a bondwire model implementation in MDS. This model has been compared for some special cases employing the SONNET’s EM program and is found to be in close agreement. The configuration calculated is given in Table 7.7 with \( s_1 \) (=0.5 mm) and the bond-patch pitch \( s_2 \) (200 \( \mu \)m). The maximum height of the bondwire is 400 \( \mu \)m. The inductances are calculated as a function of the gap size \( G \) with a bondwire length \( l_b \) of 0.5 and 1 mm (see Table 7.7).

**TABLE 7.7. Induction matrix coefficients for the configuration given in Table 7.6.**

<table>
<thead>
<tr>
<th>G (mm)</th>
<th>( l_b ) (mm)</th>
<th>( l ) (nH)</th>
<th>( m_2 ) (nH)</th>
<th>( m_{c1} ) (nH)</th>
<th>( m_{c2} ) (nH)</th>
<th>( m_{diff} = m_{c1} - m_{c2} ) (nH)</th>
<th>( X_{\text{single}} ) (10GHz) (50 ( \Omega ))</th>
<th>( X_{\text{diff}} ) (10GHz) (50 ( \Omega ))</th>
</tr>
</thead>
<tbody>
<tr>
<td>2</td>
<td>0.5</td>
<td>0.360</td>
<td>0.044</td>
<td>6.17e-4</td>
<td>4.85e-4</td>
<td>1.32e-4</td>
<td>7.75e-4</td>
<td>1.66e-4</td>
</tr>
<tr>
<td></td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>-</td>
</tr>
<tr>
<td>3</td>
<td>0.5</td>
<td>0.360</td>
<td>0.044</td>
<td>1.24e-4</td>
<td>9.24e-5</td>
<td>3.16e-5</td>
<td>1.56e-4</td>
<td>3.97e-5</td>
</tr>
<tr>
<td>1.0</td>
<td>0.571</td>
<td>0.113</td>
<td>1.55e-3</td>
<td>1.44e-3</td>
<td>1.1e-4</td>
<td>1.95e-3</td>
<td>1.38e-4</td>
<td></td>
</tr>
<tr>
<td>4</td>
<td>0.5</td>
<td>0.360</td>
<td>0.044</td>
<td>4.39e-5</td>
<td>3.11e-5</td>
<td>1.28e-5</td>
<td>5.52e-5</td>
<td>1.61e-5</td>
</tr>
<tr>
<td>1.0</td>
<td>0.571</td>
<td>0.113</td>
<td>3.93e-4</td>
<td>3.74e-4</td>
<td>1.9e-5</td>
<td>4.94e-4</td>
<td>2.39e-5</td>
<td></td>
</tr>
</tbody>
</table>
7.5 Single-ended and balanced amplifiers in differential operation

The balanced amplifiers given in Table 7.2 and the parasitic networks of Table 7.3.b and Table 7.6.b, are all symmetrical with respect to ground. By using this symmetry we can reduce, for differential operation, the balanced amplifier to a circuit structure whose topology is equivalent to that of the single-ended amplifier. The value of the port impedance and other circuit elements should be modified according the matrix reduction equations as given in Table 7.1. We start our analysis with single-ended amplifiers and extend it later for use with balanced amplifiers in differential operation. This facilitates the comparison of balanced and single-ended amplifiers with respect to stability.

7.5.1 Single-ended amplifiers loaded by capacitive mounting parasitics

We have studied the influence of capacitive parasitics on amplifier stability by calculating the stability factor $K$ using the circuit shown in Figure 7.5 with the single-ended amplifier given in Table 7.2.a.

![Diagram of single-ended amplifier loaded with capacitive mounting parasitics](image)

**Figure 7.5.** Single-ended amplifier loaded with capacitive mounting parasitics

The $y$-matrix of the single-ended capacitively loaded network is given by:

$$[Y]_{cap\, single} = [Y_{amp}]_{single} + [Y_{cap}]_{single} \tag{7.4}$$

yielding:

$$[Y]_{cap\, single} = y_0 \begin{bmatrix} j\omega \left( \frac{c_{series} + c_{shunt}}{y_0} \right) + 1 & -j\omega \frac{c_{series}}{y_0} \\ -j\omega \frac{c_{series}}{y_0} - A & j\omega \left( \frac{c_{series} + c_{shunt}}{y_0} \right) + 1 \end{bmatrix} \tag{7.5}$$

If we use the $y$-parameter representation of the stability factor $K[7.15]$:

$$K = \frac{2Re(y_{11})Re(y_{22}) - Re(y_{12}y_{21})}{|y_{12}y_{21}|} \tag{7.6}$$

we obtain:
Single-ended and balanced amplifiers in differential operation

\[
K_{\text{cap single}} = \frac{Y_{\text{single}}^2 + Y_{\text{single}}|A| \sin(\phi) + 2}{\sqrt{Y_{\text{single}}^2 (Y_{\text{single}}^2 + 2Y_{\text{single}}|A| \sin(\phi) + |A|^2)}} 
\]

(7.7)

with:

\[
Y_{\text{single}} = \frac{\omega C_{\text{series}}}{y_0} 
\]

(7.8)

Worst-case conditions in equation (7.7) occur for a phase shift \(\phi = -\pi/2\):

\[
K_{\text{cap single}} \left( \phi = -\frac{\pi}{2} \right) = \frac{Y_{\text{single}}^2 - Y_{\text{single}}|A| + 2}{\sqrt{Y_{\text{single}}^2 (|A| - Y_{\text{single}})^2}} 
\]

(7.9)

In equations (7.7) and (7.9) \(c_{\text{shunt}}\) has no influence on the amplifier stability, as implied by the formulation of (7.6). In Figure 7.6, \(K=1\) lines are plotted for phase shifts of \(-\pi/2\), 0 and \(\pi\) in the amplifying element. Note that for \(\phi = \pi/2\) equation (7.7) only has solutions for \(K>1\) and the system remains unconditionally stable and there is no solution for \(K=1\). The solutions for \(K=1\) can be approximated by their asymptotic lines with the relation \(|A|=1/Y\) (for \(\phi = -\pi/2\)) and \(|A| = 2/Y\) (for \(\phi = 0\)). The generality of Figure 7.6 becomes apparent when considering inductive parasitics.

![Diagram showing K=1 contours for a single-ended or differential mode symmetrically balanced amplifier loaded with dominant capacitive or inductive mounting parasitics.](image_url)

**Figure 7.6.** \(K=1\) contours for a single-ended or differential mode symmetrically balanced amplifier loaded with dominant capacitive or inductive mounting parasitics.
7.5.2 Single-ended amplifiers connected by inductive bondwires

In order to judge the influence of inductive coupling on the stability, we calculate the $K$ factor for the configuration given in Figure 7.7.

![Figure 7.7](image)

The four-port $\{Y_{ind}\}_{single}$ matrix which represents the inductive connection network is calculated as in Table 7.6a. Summation with the rearranged $y$-matrix of the amplifying element, using the node numbering of the circuit given in Figure 7.7, gives us a four port $y$-matrix for the complete network. Since we are only interested in the external node conditions, we can reduce this matrix to a two-port by conversion to the impedance matrix representation and eliminate the rows and columns 2 and 3, leaving only the external nodes. The resulting $y$-matrix is given in (7.10)

$$
\begin{bmatrix}
    \tilde{y}_{ind\ single} \\
    \end{bmatrix} = \frac{y_0}{T} \begin{bmatrix}
    -(jZ_{single} + 1) & jX_{single} \\
    jX_{single} + A & -(jZ_{single} + 1)
    \end{bmatrix}
$$

(7.10)

with:

$$
T = (Z_{single}^2 - X_{single}^2) + jX_{single}A - j2Z_{single} - 1
$$

(7.11)

and

$$
Z_{single} = y_0 \omega l, \quad X_{single} = y_0 \omega m
$$

(7.12)

The $K$ factor for a single-ended amplifier connected by inductive bondwires is now given by:

$$
K_{ind\ single} = \frac{X_{single}^2 + X_{single}|A|\sin(\phi) + 2}{\sqrt{X_{single}^2(2X_{single}|A|\sin(\phi) + |A|^2)}}
$$

(7.13)

Note that definition for the $K$ factor is similar to that of an amplifier loaded by capacitive parasitics see (7.7) and that the self-inductance $l$ of the bondwire has no influence on the stability. Based on the analogy with equation (7.7), the worst-case condition with respect to stability occurs for a phase shift in the amplifying element of $\phi = \pi/2$ yielding:

$$
K_{ind\ single}(\phi = \pi/2) = \frac{X_{single}^2 - X_{single}|A| + 2}{\sqrt{X_{single}^2(|A| - X_{single})^2}}
$$

(7.14)
This similarity in formulation of the $K$ factor for capacitive and inductive parasitics allows us to use the same graph (but now with an axis given by $X_{single}$) for the illustration of the stability behaviour with respect to the inductive output to input coupling (see Figure 7.6).

### 7.5.3 Single-ended amplifiers loaded by capacitive parasitics and connected by inductive bondwires

In the previous sections, we, in order to allow an analytical computation, assumed that either the capacitive or the inductive parasitics were dominant. In this section, we consider the influence of the combined parasitics. For this analysis we use the circuit shown in Figure 7.8

![Circuit diagram](image)

**Figure 7.8.** Single-ended amplifier loaded by capacitive parasitics and connected by inductive bondwires

The $y$-matrix of this circuit is found by the summation of $[Y]_{ind \ single}$ (see equation (7.10)) with $[Y]_{cap \ single}$ (see Table 7.3) yielding the combined $y$-matrix:

$$
[Y]_{comb \ single} = y_0 \begin{bmatrix}
\frac{-(jZ_{single} + 1)}{T} + jY_{single} + j\omega \frac{c_{sh}}{y_0} & \frac{jX_{single}}{T} - jY_{single} \\
\frac{jX_{single} + A}{T} - jY_{single} & \frac{-(jZ_{single} + 1)}{T} + jY_{single} + j\omega \frac{c_{sh}}{y_0}
\end{bmatrix}
$$

(7.15)

where $T$ is given by (7.11). If we calculate $K$ using (7.6), it leads to a lengthy expression for $K$ which depends on the following variables:

- $Y_{single}$: the normalized capacitive coupling between in- and output ($\omega c_{series} y$)
- $X_{single}$: the normalized inductive coupling between in- and output ($y_0 m_{c1}$)
- $Z_{single}$: the normalized self-inductance of the bondwires ($y_0 l$)
- $|A|$: the magnitude of the amplifier gain
- $\phi$: the phase of the amplifier

Note that $c_{sh}$ once again has no influence on the stability. The complete expression for $K$ is difficult to interpret. A graphical approach is potentially more useful provided the number of variables can be dealt with. We have solved this problem by considering two cases, namely:
• \(2Z_{\text{single}} < X_{\text{single}} |A|\) In this situation, we obtain the situation shown in Figure 7.9 which gives the \(K=1\) lines for \(\phi = -\pi/2, 0\) and \(\pi\) at different gain levels as a function of the capacitive and inductive coupling. In this figure, the unconditional stable region for a given gain level is at the lower left-hand corner. The worst-case conditions with respect to stability still occur for a phase shift of \(\phi = -\pi/2\). Cancelling effects are observed, at an amplifier phase shift of 0 and \(\pi\), when magnetic coupling equals capacitive coupling \((X = Y)\). For reasons of simplicity, only the \(K=1\) contours which are the first limitations of the unconditional stable region are plotted.

• \(2Z_{\text{single}} > X_{\text{single}} |A|\). In this situation, the worst-case condition is not at a phase shift of \(\phi = -\pi/2\). Further, the compensating effects found in Figure 7.9 are no longer present: in contrast, if \(X_{\text{single}}\) and \(Y_{\text{single}}\) are of the same order of magnitude, a reduction of the unconditionally stable region can be observed. To illustrate this phenomenon, we have calculated the \(K=1\) lines for different amplifier phase shifts at different ratios of \(Z_{\text{single}}\) to \(X_{\text{single}} |A|\) (see Figure 7.10). Please note the reduction of the unconditional stable region. Although Figure 7.10 has been calculated for a gain level \(|A|=1000\), the result is equivalent for other gain levels.

2. \(Z < X, |A|\)

\[\begin{align*}
\text{gain limited by inductive feedback} \\
\phi = 0, \pi \quad \cdots \cdots \\
\phi = -\pi/2
\end{align*}\]

Figure 7.9. Schematic representation of the \(K=1\) contours for \(\phi = -\pi/2, 0\) and \(\pi\) at various gain levels as a function of the capacitive and inductive coupling under the condition \(2Z < X, |A|\)
Figure 7.10. \( K=1 \) contours for \( \phi = 0, \pi/2, -\pi/2 \) and \( \pi \) at a gain level of \( |A|=1000 \) as a function of the capacitive and inductive coupling for the condition \( 2.Z > X.|A| \)
7.5.4 Balanced amplifier in differential operation

Differential operated balanced amplifiers which are symmetrical with respect to ground can be represented by a single-ended equivalent amplifier topology. This representation is found by applying the four-port to two-port matrix reduction as indicated in Table 7.1; it facilitates the clear comparison of single-ended and balanced amplifiers. The calculations needed for the overall four-port matrix are similar to those introduced for the single-ended amplifier. The schematic of the balanced amplifier in differential operation loaded by capacitive parasitics and connected by inductive bondwires is depicted in Figure 7.11.

![Diagram of balanced amplifier](image)

**Figure 7.11.** Balanced amplifier loaded by capacitive parasitics and connected by inductive bondwires for differential operation

The $y$-matrix of the configuration shown in Figure 7.11 is:

$$\begin{bmatrix}
y_{comb\text{diff}} &=& \\
\chi_0 & \frac{-(jZ_{\text{diff}} + 1)}{T_{\text{diff}}} + jY_{\text{diff}} + j \frac{\omega}{\gamma_0} (\frac{c_{\text{shunt}}}{c_{\text{par}}} + 2c_{\text{par}} + 2c_{\text{cross}}) & + \frac{jX_{\text{diff}} - jY_{\text{diff}}}{T_{\text{diff}}} \\
jX_{\text{diff}} + A & - jY_{\text{diff}} & - \frac{(jZ_{\text{diff}} + 1)}{T_{\text{diff}}} + jY_{\text{diff}} + j \frac{\omega}{\gamma_0} (\frac{c_{\text{shunt}}}{c_{\text{par}}} + 2c_{\text{par}} + 2c_{\text{cross}}) \\
\end{bmatrix}$$

(7.16)

with:

$$T_{\text{diff}} = (Z_{\text{diff}}^2 - X_{\text{diff}}^2) + jX_{\text{diff}} A - j2Z_{\text{diff}} - 1$$

(7.17)
and
\[ Y_{\text{diff}} = \frac{\omega (c_{\text{series}} - c_{\text{cross}})}{y_0}, \quad Z_{\text{diff}} = y_0 \omega (1 - m_3), \quad X_{\text{diff}} = y_0 \omega (m_{c1} - m_{c2}) \]  \hspace{1cm} (7.18)

Note that the formulation of equation (7.16) is similar to that of (7.15) and that the capacitances \( c_{\text{par}} \) and \( c_{\text{shunt}} \) play no role in the stability analysis for differential operation because they are only present in the imaginary part of \( y_{11} \) and \( y_{22} \).

Normally, one of the parasitic feedbacks will be dominant as individually described in the previous sections. The parasitic which is dominant can be found by determining the inductive and capacitive components \( X_{\text{diff}} \) and \( Y_{\text{diff}} \). The use of thin high dielectric constant substrates (resulting in narrow connection lines) will lead to dominant inductive parasitics. Similarly, the use of thick substrates with a low dielectric constant will lead to dominant capacitive parasitics. If capacitive parasitics are dominant, equation (7.7) can be used with \( Y_{\text{single}} \) replaced by \( Y_{\text{diff}} \); if inductive coupling is dominant equation (7.13) should be used with \( X_{\text{single}} \) replaced by \( X_{\text{diff}} \). This reasoning is also applicable when considering the \( K=1 \) lines of Figure 7.6. If \( Y_{\text{diff}} \) and \( X_{\text{diff}} \) are of the same order of magnitude, the theory of the previous section should be applied using \( Y_{\text{diff}}, X_{\text{diff}} \) and \( Z_{\text{diff}} \).

Based on the above, the advantage of balanced over single-ended circuitry with respect to stability is apparent. In contrast with the single-ended amplifier whose stability is dependent on the values of \( c_{\text{series}} \) and \( m_{c1} \), the stability of a balanced amplifier in differential operation is dependent on the difference in the parasitic feedback elements: \( c_{\text{diff}} = c_{\text{series}} - c_{\text{cross}} \) and \( m_{\text{diff}} = m_{c1} - m_{c2} \). Cancellation can be explored by employing narrowly spaced input and output pin/line pairs and a relatively large distance between in- and output, so that: \( c_{\text{series}} = c_{\text{cross}} \) and \( m_{c1} = m_{c2} \) eliminating parasitic feedback.

### 7.5.5 Stability conditions when \( K<1 \)

Absolutely stable behaviour is a rather heavy constraint for amplifier design. In most cases, the amplifier is connected to characteristic terminations, and it is sufficient when the in- and output of the amplifier does not present a negative resistance (\( |\Gamma_{\text{IN}}| < 1 \) or \( |\Gamma_{\text{OUT}}| < 1 \)). When connected to a characteristic termination, the conditions for \( |\Gamma_{\text{IN}}| \) and \( |\Gamma_{\text{OUT}}| \) can be replaced by \( |s_{11}| < 1 \) and \( |s_{22}| < 1 \). Consequently, stable behaviour can be studied by plotting \( |s_{11}| \) and \( |s_{22}| \) equal 1. We have plotted these lines for the situation that the amplifier is dominated by one of the feedback parasitics (capacitive or inductive) assuming \( c_{\text{shunt}} \) and \( c_{\text{par}} \) to be zero, representing the worst-case conditions with respect to stability (see Figure 7.12). Calculation of the reflection s-parameters indicates that the situation \( |s_{11}| = |s_{22}| > 1 \) only occurs for a phase shift of the amplifying element of: \(-\pi < \phi < 0\).
7.5.6 Stability conclusions for single-ended and balanced amplifiers in differential operation.

When a bare amplifier chip is mounted on a printed circuit board (see the illustrations in Table 7.3 and Table 7.6), one of the feedback parasitics (capacitive or inductive) will, in general, be dominant. Worst-case conditions with respect to stability occur when for a phase shift of the amplifying element of $\phi = \pi/2$. The maximum gain level $|A|$ for unconditionally stable behaviour is now approximated by $1/X$ or $1/Y$ (see Figure 7.10). If the feedback parasitics ($X$ and $Y$) are of the same order of magnitude and the condition $2Z < X \cdot |A|$ holds, the above remains valid. For the condition $2Z > X \cdot |A|$, one should consider the reduced stable region as indicated in Figure 7.10 in this situation, the maximum gain level can no longer be approximated by $1/X$ or $1/Y$.

- **Single-ended amplifier**: This amplifier configuration works out to be the most sensitive in respect to stability. This is mainly caused by the fact that no compensating effect between different mounting parasitics is present. Consequently, the gain bandwidth product will be seriously limited for unconditional behaviour as well as for the condition $|s_{11}|$ and $|s_{22}| < 1$ (see Figure 7.6).

- **Balanced amplifier in differential operation mode**: From a stability point of view, this is the preferred configuration for high-gain wide-band amplifiers. When properly connected, the feedback parasitics will partly compensate each other. In fact, only their differences are important ($c_{\text{diff}} = c_{\text{series}} - c_{\text{cross}}$ and $m_{\text{diff}} = m_{c1} - m_{c2}$). Note that for this operational mode all the balanced amplifier block configurations of Table 7.2 are identical.
7.6 Unbalanced operation of balanced circuitry (testing conditions)

When balanced circuitry is used in unbalanced operation, a different set of stability conditions becomes important. In this configuration, the balanced circuit cannot, independently of its internal structure (grounded or floating), be reduced to an equivalent single-ended configuration. This has as consequence that the internal structure of the amplifier must be taken into account during the stability analysis. A balanced amplifier in unbalanced operation loaded by dominant capacitive parasitics is illustrated in Figure 7.13. The uses of s-parameters facilitates the four to two-port reduction by using the characteristic match of port two and four, and the use of stability circles later in this section. The four-port s-parameters are calculated using:

\[
[S]_{4\text{port}} = \left(\begin{bmatrix} 1 \end{bmatrix} - \frac{1}{y_0} [Y]_{4\text{port}} \right) \cdot \left(\begin{bmatrix} 1 \end{bmatrix} + \frac{1}{y_0} [Y]_{4\text{port}}\right)^{-1}
\]

(7.19)

In which \(y_0\) is the system admittance and \(\begin{bmatrix} 1 \end{bmatrix}\) the diagonal unit matrix. The s-parameters for unbalanced operation are now given by:

\[
\begin{bmatrix}
S_{11} & S_{12} \\
S_{21} & S_{22}
\end{bmatrix}_{\text{unbal}} =
\begin{bmatrix}
S_{11} & S_{13} \\
S_{31} & S_{33}
\end{bmatrix}_{4\text{port}}
\]

(7.20)

In the following sections, the stability behaviour of balanced circuitry in unbalanced operation is be investigated for the amplifier structures given in Table 7.2. Capacitive mounting parasitics, inductive bondwire parasitics and combined parasitics are considered in turn.

7.6.1 Unbalanced operation of a balanced amplifier loaded with capacitive parasitics

A balanced amplifier loaded with capacitive parasitics is illustrated in Figure 7.13.

Figure 7.13. Amplifier loaded with capacitive parasitics in unbalanced operation
Direct calculation of the s-parameters leads to lengthy equations and a distinct lack of insight. One way to simplify this problem is to neglect the parasitic capacitances $c_{shunt}$ and $c_{par}$. It can be shown numerically that $c_{par}$ does not significantly influence the results and that sufficient $c_{shunt}$ tends to lower the gain, which improves the situation with respect to stability. In practice, worst-case conditions can be studied by considering the feedback capacitances over the amplifier ($c_{series}$ and $c_{cross}$). Further, if $c_{series} = c_{cross}$, (using narrow input and output lines / pins) one obtains rather simple expressions for the s-parameters.

**Internally grounded architecture**

Using the above, we obtain for the internally grounded amplifier block (see Table 7.2c). The following s-parameters:

$$s_{11} = s_{22} = \left(\frac{1}{2}\right) \frac{(-6Y + 2YA - 4 + A)}{(-4Y + YA - 2)} Y$$  \hspace{1cm} (7.21)

$$s_{12} = \frac{-Y}{-4Y + YA - 2}$$  \hspace{1cm} (7.22)

$$s_{21} = \left(\frac{1}{4}\right) \frac{(4A + 8YA + 4Y - YA^2 + 2YA + 8Y^2 + 4Y^3)}{(1 + Y)^2(-4Y + YA - 2)}$$  \hspace{1cm} (7.23)

with

$$Y = \frac{j\omega c_{series}}{y_0} = \frac{j\omega c_{cross}}{y_0}$$  \hspace{1cm} (7.24)

It can be seen by straightforward inspection of the s-parameters that the worst-case stability conditions occur for a phase shift of -90 degrees of the amplifying element. Plotting the $K=1$ lines (see Figure 7.14a) shows that the allowed maximum gain-bandwidth product for unconditional stable behaviour will be strongly limited by the parasitic mounting capacitances and is comparable to the situation of a single-ended amplifier. Note that in this case $Y$ is given by (7.24) and not by the normalized difference between $c_{series}$ and $c_{cross}$ (see equation (7.18)). In Figure 7.14a, it is clear that there are two unconditionally stable regions, one at the lower left-hand corner and one at the upper right-hand corner. Use of the upper right region is not really an option since any contribution that leads to a decrease in amplifier gain can cause unstable behaviour.

If unconditional stable behaviour is no longer required and a characteristic termination at the in- and output is assumed, the stability behaviour can be studied by plotting the contours where $|s_{11}|$ and $|s_{22}|$ equal 1. Assuming that $s_{11} = s_{22}$, the stability behaviour for this configuration is illustrated in Figure 7.14b. The gain-bandwidth product of the amplifier is seen to be seriously limited by the parasitic capacitances, even when we limit consideration to the case $|s_{11}| = |s_{22}| = 1$. 

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Floating architecture

Study of the s-parameters for unbalanced operation of an amplifier block with a floating architecture (see Table 7.2b for the schematic and y-matrix) shows that $K<1$ for high values of $|A|$ and $|Y|$ (see Figure 7.14a).

If unconditionally stable behavior is no longer required and the amplifier is characteristically terminated, the magnitude of the reflection parameters should be smaller than one. Depending on which of the parasitic capacitances is dominant, $|s_{11}|$ and $|s_{22}|$ will vary between 0 and 1. If $c_{par}$ is dominant, the two amplifier inputs will be short-circuited, thus yielding a direct connection from the input port to the input load (see Figure 7.13) thus resulting in a perfect match ($|s_{11}|=0$). If $c_{shunt}$ is dominant, the ports will become short-circuited, so that $|s_{11}|=|s_{22}|=1$ for very high frequencies. In all other cases we can write $s_{11}$ (assuming $c_{par}=c_{shunt}=c_{diff}=0$) as:

$$s_{11} = s_{22} = \left( \frac{1}{2} \right) \frac{(2Y-1)(2Y+1)}{(Y+1)(4Y+1)} = \frac{1}{2}$$  \hspace{1cm} (7.25)

and

$$s_{12} = 2 \frac{Y}{4Y+1}$$  \hspace{1cm} (7.26)
Stability of wide-band amplifier configurations

\[ S_{21} = \frac{(1}{4})(A + 4YA + 8Y + 8Y^3 + 16Y^2)}{(4Y + 1)(Y + 1)^2} \]  \hspace{1cm} (7.27)

with \( Y \) defined as in (7.24). Surprisingly enough, the gain \( A \) does not appear in the expressions for \( s_{11}, s_{22} \) and \( s_{12} \). Once again we find that \( s_{11} = s_{22} \). From (7.25) it follows that, when connected to a characteristic impedance at the in- and output, the magnitude of the overall circuit s-parameters \( |s_{11}| \) and \( |s_{22}| \) will be close to -6 dB. Consequently, it can be concluded that under the condition \( c_{\text{series}} = c_{\text{cross}} \) this floating amplifier circuit topology, independent of the gain-bandwidth product will remain stable for balanced as well as unbalanced operation.

Given a specific situation, the stability behaviour of a floating amplifier structure under unbalanced operation can be illustrated graphically by plotting the stability circles for phase shifts of \( \phi = \frac{\pi}{2}, \frac{\pi}{2} \) and \( \pi \). The stability circles give the \( \Gamma_L \) values for \( |\Gamma_{\text{IN}}| = 1 \) (output stability circle) or the \( \Gamma_S \) values for \( |\Gamma_{\text{OUT}}| = 1 \) (output stability circle), see Figure 7.1. Given that \( s_{11} = s_{22} \), we only have to consider the in- or output stability circles. For the plots shown in Figure 7.15, we have considered an amplifier mounted on a ceramic 0.254 mm alumina substrate using a gap of 4 mm (see Table 7.4). In Figure 7.15a, a narrow spacing for the connection lines (\( s = 0.5 \) mm) has been used and this results in the ratio \( c_{\text{cross}}/c_{\text{series}} \approx 1 \).

The stable region is indicated by the hatched area. If the ratio \( c_{\text{cross}}/c_{\text{series}} \) becomes significantly smaller than one, the hatched area shifts from the Smith chart centre to the left, yielding the situation that \( |s_{11}| > 1 \) for a characteristic match if the centre of the Smith chart is no longer enclosed. This tendency is illustrated by Figure 7.15b which gives the stability circles for much wider spacing (\( s = 4 \) mm), (now \( c_{\text{cross}}/c_{\text{series}} = 0.635 \)) Note that for reasons of simplicity we have assumed that the value of \( c_{\text{series}} \) is not affected by the spacing \( s \).

![Stability circles for an amplifier with a floating structure in unbalanced operation](image)

**Figure 7.15.** Stability circles for an amplifier with a floating structure in unbalanced operation

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Given a higher gain-bandwidth product or larger parasitic feedback capacitances, the stability circles will narrow around the centre of the Smith chart, and increase the requirements on the matching. The influence of the capacitors $c_{par}$ is neglected. The presence of $c_{par}$ decreases the gain bandwidth and improves the input match for this type of operation, so that its neglect represents, in fact, a worst-case condition.

**Amplifier block with grounded input and floating output**

Practical amplifiers are often built with an emitter-follower input and a balanced stage at the output. It is interesting to consider the stability conditions governing the amplifier block of Table 7.2d which combines an internally grounded structure and a floating architecture. The resulting s-parameters are ($c_{series} = c_{cross}$):

$$s_{11} = -Y \frac{(2Y + 1)}{(Y + 1)(3Y + 1)} \quad s_{22} = \frac{1}{2} \frac{4Y^2 + Y - 1}{(Y + 1)(3Y + 1)}$$

(7.28)

and

$$s_{21} = \frac{1}{4} \frac{A + 3YA + 4Y^2 + 4Y^3}{(3Y + 1)(Y + 1)^2} \quad s_{12} = \frac{Y}{3Y + 1}$$

(7.29)

The gain $A$ does not appear in the expressions for $s_{11}$, $s_{22}$, and $s_{12}$. Numerical study of the s-parameters for this type of operation shows that $K$ will become smaller than one at a sufficiently high level of gain and frequency. The input and output match ($s_{11}$ and $s_{22}$) are no longer equal to each other. As can be seen from these s-parameters, for low values of $Y$ the input will be perfectly matched and the output will be close to -6dB. Numerical study indicates that this configuration has approximately the same behaviour as that of the floating amplifier structure. With the added advantage of improved input match and, consequently, a larger unconditionally stable region (see Figure 7.14).

### 7.6.2 Amplifiers in unbalanced operation connected by inductive bondwires

When using an internally grounded amplifier, even when $m_{c1} = m_{c2}$ unconditionally stable behaviour cannot be guaranteed for very large gain-bandwidth products. This is in contrast to the amplifier block with a floating architecture, which for $m_{c1} = m_{c2}$ results in $s_{21} = 0$, and yields an unlimited gain-bandwidth product. The s-parameters for a floating amplifier connected by inductive bondwires are:

$$s_{11} = s_{22} = \frac{XA - 2 - 3Z - Z^2 + X^2}{XA - 4 - 4Z - Z^2 + X^2}$$

(7.30)

$$s_{12} = \frac{X}{XA - 4 - 4Z - Z^2 + X^2} \quad s_{21} = -\frac{X + A}{XA - 4 - 4Z - Z^2 + X^2}$$

(7.31)

with:

$$Z = j\omega(l - M_{sh}) \quad X = j\omega(m_{c1} - m_{c2})$$

(7.32)

When $X$ is unequal to zero, the unconditionally stable region is slightly larger than for the
same amplifier under differential operation. This is also true for an amplifier with grounded input and floating output.

It must be noted that a singularity exists in the analysis of the floating amplifier when computing the \([Z_{\text{tot}}]\) matrix. This problem can be circumvented by adding dummy variables in the \(Y\) matrix of the floating amplifier block. After the final transformation to the four-port \(S\)-matrix these dummy variables can be set to zero, so they no longer complicate the analysis.

### 7.6.3 Amplifiers in unbalanced operation loaded by capacitive mounting parasitics and connected by inductive bondwires

If an amplifier is mounted with narrow in- and output pin spacing (\(s\)) with a large gap (\(G\)), we find the conditions \(c_{\text{series}}=c_{\text{cross}}\) and \(m_{c1}=m_{c2}\) for the mounting parasitics. In the previous sections, it was shown that for these conditions, the internally grounded amplifier has stable behaviour which is significantly limited by capacitive and inductive parasitics. This is in contrast with an amplifier based on an internal floating architecture which is only limited by the capacitive parasitics for unconditionally stable behaviour. The \(s\)-parameters for the floating architecture, taking into account the capacitive as well the inductive parasitics (under the condition \(c_{\text{series}}=c_{\text{cross}}\) and \(m_{c1}=m_{c2}\)), are given below:

\[
\begin{align*}
    s_{11} &= s_{22} = \frac{(Z + 1)4Y^2 - 2YZ - Z - 1}{(1 + 4Y)((1 + Z)2Y + 2 + Z)} \quad (7.33) \\
    s_{12} &= 2\frac{Y}{1 + 4Y} \quad (7.34) \\
    s_{21} &= \frac{(2Z + Z^2 + 1)8Y^3 + (Z^2 + 3Z + 2)8Y^2 + (2A + 4 + Z^2 + 4Z)2Y + A}{(1 + 4Y)((1 + Z)2Y + 2 + Z)^2} \quad (7.35)
\end{align*}
\]

As can be seen from the \(s\)-parameter \(s_{12}\), the stability behaviour for the floating amplifier (under the condition \(c_{\text{series}}=c_{\text{cross}}\) and \(m_{c1}=m_{c2}\)) is only limited by the capacitive parasitics. This conclusion holds also for the amplifier with grounded input and floating output. Consequently, one could argue that for unbalanced operation, the stability behaviour of amplifiers with a floating output can be improved by the use of a larger gap with longer bondwires for the chip connection. One reduces the capacitive parasitics at the cost of higher inductive parasitics, which leads to improved stability behaviour.

### 7.7 Stability conclusions for balanced amplifiers in unbalanced operation

In this mode of operation, unconditionally stable behaviour cannot be ensured for large gain-bandwidth products, even when assuming \(c_{\text{series}}=c_{\text{cross}}\) and \(m_{c1}=m_{c2}\). Significant differences were found in the stability behaviour between internally grounded amplifier blocks and amplifier blocks with a floating output. Amplifiers with a floating output have limited values for their in- and output reflection parameters (\(|s_{11}|\) and \(|s_{22}| < 1\) when matched with the system impedance and are not affected (with respect to stability) by the inductive
parasitics. Consequently, for this type of amplifier, the stability behaviour in unbalanced operation can be improved by using a wider gap with longer bondwires.

An amplifier with grounded input and floating output has a lower return loss at the input than a completely floating amplifier.

When comparing these results with those found for an amplifier operated differentially, it becomes apparent that narrowly spaced inputs and outputs should, in general, be used. The floating output amplifier structure proved to be the most well behaved for both operational modes.

### 7.8 Off-chip matching

In the previous discussion, we assumed the use of on-chip termination. This type of termination has the advantage that no external components (such as SMD resistors) are required. However, the HF behaviour of the amplifier will often be affected deleteriously due to the inductance of the bondwires. This is especially true for the in- and output buffer, where the high bondwire reactance in combination with the relatively low on-chip characteristic impedance can lead to poor return loss and high sensitivity of the transfer characteristics with respect to uncertainty in bondwire inductance. A logical way to circumvent these problems is to use a low value off-chip resistor for impedance matching and a high ohmic on-chip resistance to reduce the effect of bondwire self-inductance (see Figure 7.16).

![Figure 7.16. Amplifier with off-chip termination](image)

For reasons of simplicity, we have considered a single-ended amplifier and ignored parasitic capacitances. We assume $y_{off}$ and $y_{on}$ to be purely ohmic and the sum $y_{off} + y_{on} = y_0$ to be perfectly matched at low frequencies. Further, we introduce factor $R$ given by:

$$R = \frac{y_{off}}{y_{on}}$$

(7.36)

We have calculated the influence of $R$ on the stability factor $K$. Note that the worst-case condition with respect to the amplifier phase shift once again occurs at $(\phi = -\pi/2)$. If $R=0$ we have the same situation as in section 7.5.2. For higher values of $R$, the stability behaviour can be illustrated as follows:

It has proved interesting to plot the behaviour of $K$ as function of $X_{id}$ which is perpendicular to the $K=1$ line of Figure 7.6. As shown in Figure 7.17, the unconditionally stable region increases with $R$ due to the concomitant decrease in current flow through the bondwires.
Stability of wide-band amplifier configurations

From the above, one might conclude that off-chip matching is an ideal way to enlarge the unconditionally stable region. In the case where the amplifier stability is strongly limited by inductive parasitics this will be true, however, adding external matching resistors (mostly SMDs) would mean that the capacitive parasitics would be greatly enlarged, which might well limit the stable region (see Figure 7.9).

\[ R = \frac{y_{off}}{y_{on}} \]

![Graph showing unconditional stable region and K=1 limit for an amplifier with only on-chip matching (X/A/ = 1)](image)

**Figure 7.17.** K=1 lines for an externally matched amplifier as a function of X/A/ and the ratio between the external and on-chip admittance

### 7.9 Asymmetry

The stability analysis of balanced amplifiers in differential operation, as discussed previously, is based on the assumption that amplifier and parasitic networks are symmetrical with respect to ground. If asymmetry in the connecting networks or in the amplifier is present, the stability behaviour will, in general, be negatively affected. In order to study this degradation of stability, we consider a number of asymmetrical balanced amplifier configurations under differential operation. The asymmetry in the amplifier circuit or parasitics will disturb the definition of the virtual ground, yielding to the fact that differential operation can no longer be represented by an equivalent, simple, single-ended amplifier. The disturbance of the virtual ground is why during our analysis we must take into account the internal amplifier structure. In Figure 7.18, the current paths are given for cascaded internally grounded and floating amplifiers if asymmetry is present. As can be seen in Figure 7.18, the use of an internally grounded amplifier with an asymmetry in the input match causes a compensating ground current because \( I_1 \) and \( I_2 \) do not cancel. The amplifier with the floating architecture forces \( I_1 = I_2 \) and is, therefore, relatively insensitive to gain fluctuations and impedance mismatch. We consider the avoidance of ground currents, which can complicate the correct operation of balanced amplifiers considerably, to be of primary importance and discuss, therefore, only the floating amplifier structure.
General four-to-two-port y-matrix reduction

An general four-port in its general y-matrix representation is given by:

\[
\begin{align*}
\begin{bmatrix}
    i_1 \\
    i_2 \\
    i_3 \\
    i_4 \\
\end{bmatrix} &= \begin{bmatrix}
    y_{11} & y_{12} & y_{13} & y_{14} \\
    y_{21} & y_{22} & y_{23} & y_{24} \\
    y_{31} & y_{32} & y_{33} & y_{34} \\
    y_{41} & y_{42} & y_{43} & y_{44} \\
\end{bmatrix} \begin{bmatrix}
    u_1 \\
    u_2 \\
    u_3 \\
    u_4 \\
\end{bmatrix} \\
\end{align*}
\]

If we assume a floating amplifier configuration, we can reduce to a two-port y-matrix by using the conditions:

\[
\begin{align*}
    i_2 &= -i_1 \\
    v_1 &= u_1 - u_2 \\
    i_4 &= -i_3 \\
    v_2 &= u_3 - u_4
\end{align*}
\]

yielding:
\[ i_1 = v_1 \cdot y_{11} + u_2(y_{11} + y_{12}) + v_2 \cdot y_{13} + u_4(y_{13} + y_{14}) \]
\[ -i_1 = v_1 \cdot y_{21} + u_2(y_{21} + y_{22}) + v_2 \cdot y_{23} + u_4(y_{23} + y_{24}) \]
\[ i_3 = v_1 \cdot y_{31} + u_2(y_{31} + y_{32}) + v_2 \cdot y_{33} + u_4(y_{33} + y_{34}) \]
\[ -i_3 = v_1 \cdot y_{41} + u_2(y_{41} + y_{42}) + v_2 \cdot y_{43} + u_4(y_{43} + y_{44}) \] (7.39)

By solving for \(i_1, i_3\) and elimination of \(u_2\) and \(u_4\) we obtain the general two-port \(y\)-matrix representation for the floating amplifier giving the relation between \(i_1, i_3, v_1\) and \(v_2\). The resulting two-port parameters are, in this very general case, lengthy and difficult to interpret. In order to address the effects of asymmetry on the amplifier in a more sensible way, we consider the output to input isolation expressed in the \(y_{12}\) parameter for a limited number of asymmetrical configurations (see Figure 7.19).

Asymmetry caused by capacitive mounting parasites

In Figure 7.19, the circuit of a floating amplifier with its capacitive connection parasitics is given. The capacitors \(c_{par}\) have been neglected because they cannot give a contribution to an asymmetry with respect to ground.

![Floating amplifier with capacitive asymmetric connection parasitics](image)

with the capacitance matrix:

\[ [Y_{cap}]_{bal} = j\omega \begin{bmatrix}
    c_{shunt1} + c_{cross} + c_{series1} & 0 & -c_{series1} & -c_{cross} \\
    0 & c_{shunt2} + c_{cross} + c_{series2} & -c_{cross} & -c_{series2} \\
    -c_{series1} & -c_{cross} & c_{shunt3} + c_{cross} + c_{series1} & 0 \\
    -c_{cross} & -c_{series2} & 0 & c_{shunt4} + c_{cross} + c_{series2}
\end{bmatrix} \]

**Figure 7.19.** Floating amplifier with capacitive asymmetric connection parasitics

The circuit shown in Figure 7.19. is symmetrical in respect to ground if:

\[ c_{shunt1} = c_{shunt2} \]
\[ c_{shunt3} = c_{shunt4} \]
\[ c_{series1} = c_{series2} \]
\[ c_{cross1} = c_{cross2} \] (7.40)

If one of the conditions above is not valid, then the amplifier configuration will be asymmetrical to ground. The parameter \(y_{12}\) which is a measure for the output to input isolation is
given in Table 7.8, for three different cases of asymmetry, namely:

- a) Unbalanced shunt capacitances in the input or output of the amplifier will not affect \( y_{12} \). This can clearly be seen by comparison with equations (7.16) and (7.18) for the symmetrical amplifier under differential operation.

- b) Unbalanced shunt capacitances at the output and input of the amplifier leads to an increase in the two-port parameter \( y_{12} \), thus decreasing the isolation (see Table 7.8b). This can clearly be seen if \( c_{\text{series}} = c_{\text{cross}} \) and \( c_{\text{series}} < c_A + c_B \) then \( y_{12} \) becomes:

\[
y_{12} = -j \omega c_{\text{series}} \frac{(c_A - c_B)^2}{(c_A + c_B)^2}
\]

(7.41)

From (7.41), it can be concluded that if \( c_A \) or \( c_B \) becomes very large, the isolation becomes totally dependent on \( c_{\text{series}} \) and, in fact, the configuration reduces to a single-ended amplifier.

- c) Unbalanced feedback capacitances (\( c_{\text{series1}} \neq c_{\text{series2}} \)) will also negatively affect the isolation (see Table 7.8c). Following from numerical calculations of the parameter \( y_{12} \) it can be concluded that it is more important that \( c_{\text{series1}} + c_{\text{series2}} = 2c_{\text{cross}} \) then \( c_{\text{series1}} = c_{\text{series2}} 

TABLE 7.8. Capacitive asymmetrical connection configurations

<table>
<thead>
<tr>
<th>asymmetry</th>
<th>( y_{12} )</th>
</tr>
</thead>
<tbody>
<tr>
<td>a) Asymmetry in the input shunt capacitances: ( c_{\text{shunt1}} \neq c_{\text{shunt2}} ) while: ( c_{\text{shunt2}} = c_{\text{shunt3}} = c_{\text{shunt4}} = c_{\text{shunt}} ) ( c_{\text{cross1}} = c_{\text{cross2}} = c_{\text{cross}} )</td>
<td>( y_{12} = \frac{1}{2} j \omega (c_{\text{cross}} - c_{\text{series}}) )</td>
</tr>
<tr>
<td>b) Asymmetry in the input and output shunt capacitances: ( c_{\text{shunt1}} = c_{\text{shunt3}} = c_A ) ( c_{\text{shunt2}} = c_{\text{shunt4}} = c_B ) ( c_A \neq c_B ) while: ( c_{\text{series1}} = c_{\text{series2}} = c_{\text{series}} ) ( c_{\text{cross1}} = c_{\text{cross2}} = c_{\text{cross}} )</td>
<td>( y_{12} = j \omega \left( \frac{2(c_A + c_B)(c_{\text{cross}}^2 - c_{\text{series}}^2) + 2c_{\text{cross}}c_A c_B - c_{\text{series}}(c_A^2 + c_B^2)}{(c_A + c_B + 4(c_{\text{series}} + c_{\text{cross}}))(c_A + c_B)} \right) )</td>
</tr>
<tr>
<td>c) Asymmetry in the feedback capacitances ( c_{\text{series1}} \neq c_{\text{series2}} ) while: ( c_{\text{shunt1}} = c_{\text{shunt2}} = c_{\text{shunt3}} = c_{\text{shunt4}} = c_{\text{shunt}} ) ( c_{\text{cross1}} = c_{\text{cross2}} = c_{\text{cross}} )</td>
<td>( y_{12} = \frac{1}{4} j \omega \left( \frac{2c_{\text{cross}} - (c_{\text{series1}} + c_{\text{series2}}) - (c_{\text{series1}} - c_{\text{series2}})^2}{2c_{\text{cross}} + c_{\text{shunt}} + c_{\text{series1}} + c_{\text{series2}}} \right) )</td>
</tr>
</tbody>
</table>
Asymmetry caused by inductive connection wires

In Figure 7.20, the circuit is given of a floating amplifier with its inductive connection wires.

![Diagram of floating amplifier with inductive connection wires]

with the L matrix:

$$[L]_{bal} = \begin{bmatrix}
    l_a & m_s & -m_{c1a} & -m_{c2} \\
    m_s & l_b & -m_{c2} & -m_{c1b} \\
    -m_{c1a} & -m_{c2} & l_c & m_s \\
    -m_{c2} & -m_{c1b} & m_s & l_d
\end{bmatrix}$$

Figure 7.20. Floating amplifier with inductive asymmetrical connection parasitics

The circuit shown in Figure 7.19. is symmetrical with respect to the ground if:

$$l_a = l_b$$
$$l_c = l_d$$
$$m_{c1a} = m_{c1b}$$

If one of the conditions above is not valid, then the inductive connection of the amplifier will be asymmetrical to ground. We have calculated the $y_{12}$ parameter for a number of asymmetrical configurations based on bondwire variations in self-inductance or mutual coupling. The general conclusion of these calculations is that the nominator of $y_{12}$ depends only on the difference given by: $m_{c1a} + m_{c1b} - 2m_{c2}$ which is closely related to the situation found for the symmetrical amplifier in differential operation (see (7.16)).

7.10 Other causes of instability

7.10.1 $s_{12}$ degradation due to bias lines and ground connects feedback

Degradation of $s_{12}$ due to the bias lines is manifest when the supply line impedance including bondwires becomes large at high frequencies. When a standard bias line connection is applied to a chip (see Figure 7.21), there is a direct feedback path between the output stage and the input stage. This is caused by the non-zero impedance of the bias connections.
Conclusions

Providing each amplifier stage with its own bias line significantly improves the $s_{12}$ (Figure 7.22). Note that in the situation of Figure 7.21, three bondwires are connected in parallel to facilitate an objective comparison with the situation of Figure 7.22. The inductance for a single bondwire is estimated to be 0.5 nH/mm. For a packaged IC, the bias line inductance is in the order of 3 to 10 nH.

![Figure 7.21. Feedback of signals by common bias lines will increase $s_{12}$](image)

![Figure 7.22. Separated bias lines for the amplifier blocks will lower $s_{12}$](image)

7.11 Conclusions

In this chapter, a general stability analysis which is not limited to a specific circuit, gain level, amplifier phase shift or mounting parasitic value has been introduced. The amplifier topologies treated are: the single-ended amplifier, the balanced amplifier in differential operation and the balanced amplifier in unbalanced operation. Although the stability analysis assumes on-chip termination, some attention is paid to the effect of off-chip matching. It has been found that worst-case conditions with respect to stability mainly occur for an amplifier phase shift of $\phi=-\pi/2$. The main conclusions are given below:
Stability of wide-band amplifier configurations

- **Single-ended amplifier:** This amplifier configuration is the most sensitive in respect to stability. This is mainly due to the fact that no compensating effect between different mounting parasitics is present. As a consequence, the gain-bandwidth product will be seriously limited in respect to unconditionally stable behaviour as well the condition \(|s_{11}| \) and \(|s_{22}| < 1\) (see Figure 7.6).

- **Balanced amplifier in differential operation:** From a stability point of view, this is the preferred configuration for high-gain wide-band amplifiers. When properly connected, the feedback parasitics will partly compensate each other. In fact, only the differences between the feedback parasitics are important. These are given by \(c_{\text{diff}}=c_{\text{series}} c_{\text{cross}}\) and \(m_{\text{diff}}=m_{c1} m_{c2}\). Note that for this operational mode, all amplifier block configurations shown in Table 7.2 are identical. When applying symmetrical narrow-spaced input and output lines, the fields of these lines will cancel in the far field for differential operation, which has two advantages. Firstly, the radiation from the output is reduced and, secondly the input will be less sensitive to disturbances since only differential signals will be amplified. Another positive effect is that the supply current will be almost constant as a function of time. Voltage fluctuations over the bias lines will manifest themselves as common-mode signals and will have almost no effect on the circuit operation. If asymmetry is present, the stability is, in general, negatively affected. For internally grounded amplifiers, asymmetry will cause compensating ground currents which are undesirable. In the case of a floating amplifier, asymmetry is less harmful, when asymmetry is present in the connection parasitics, degradation of stability is mainly caused by the fact that the cancelling of connection parasitics is less effective.

- **Balanced amplifiers in unbalanced operation:** For this operational mode, unconditionally stable behaviour cannot be ensured for large gain-bandwidth products, even under the assumption \(c_{\text{series}} = c_{\text{cross}}\) and \(m_{c1} = m_{c2}\). Significant differences were found in the stability behaviour between internally grounded amplifier blocks and amplifier blocks with a floating output. Amplifiers with a floating output have limited values for their in- and output reflection parameters \(|s_{11}|\) and \(|s_{22}| < 1\) when matched with the system impedance and they are not affected (in respect to stability) by the inductive parasitics.

From the above, it is clear that using conventional chip mounting techniques with narrowly spaced input and output amplifiers with very high gain and bandwidth can be realized. When amplifiers are used with a floating output, circuits which behave stably in unbalanced operation can be realized. This allows a simpler characterization by using a standard two-port network. Further it would appear that these circuits are relatively insensitive to asymmetry.

### 7.12 References


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Chapter 8  
*Wide-band amplifier design examples*

8.1 Introduction

Optical telecommunication systems are currently being designed for bit rates in excess of 10 GBits/s. Experimental systems have been demonstrated, at significantly higher bit rates. It is clear that the very large bandwidths needed for these systems can lead to difficulties in the realization of the RF circuitry. The data transmission capacity of an optical fibre link can be multiplied without further stressing the RF circuitry by applying Wavelength DeMultiplexing (WDM). The WDM concept avoids the inherent bandwidth limitation of the RF circuitry (determined in the main by the pre-amplifier photodiode combination) by paralleling multiple data channels. In Figure 8.1 a conceptual four channel wavelength demultiplexer is depicted. The multi-wavelength receiver separates spectral components of the incoming light signal based on colour (optical frequency) into one of the four channels terminated by a photo detector diode. The photodiode pre-amplifier combination is followed by the main amplifier, often in combination with an Automatic Gain Control (AGC) or limiter, matching the incoming signal to a level compatible with the decision circuitry. This circuitry is controlled by the clock extracted from the incoming bit-stream. Finally the demultiplexer converts the serial data to parallel binary form at a lower clock rate.
The RF silicon design environment created within MDS has been used to realize a number of the high frequency components for the system of Figure 8.1, namely: a hybrid configuration of a Si-pre-amplifier array with an optical WDM InP chip [8.19], a series of pre-amplifiers and an AGC amplifier [8.10]. The pre-amplifiers and the AGC amplifier were realized in Philips Research’s experimental double poly process [8.12] and Philips Semiconductors 1μm Bipolar/CMOS process QUBiC [8.6] respectively.

Wide-band amplifier performance is specified in terms of: bandwidth, gain, stability, noise, group delay, linearity and dynamic range. In low frequency design, these specifications can in general be simultaneously satisfied using overall feedback [8.2]. The application of overall feedback in high frequency design is often impractical due to the relatively high operating frequency with respect to the $f_T$ or $f_{Max}$ of the active devices. The phase shift introduced by other circuit elements can further complicate the application of overall feedback. It is, therefore common practice that in very-wide-band amplifier design overall feedback is replaced by local feedback [8.14,8.17]. Unfortunately, the use of local feedback often results in poor noise performance. The pre-amplifiers discussed in this chapter make use of local as well overall feedback techniques depending on individual bandwidth and noise requirements. The AGC amplifier is based on the use of local feedback.

### 8.2 Pre-amplifiers for optical telecommunication systems

Pre-amplifiers in optical receiver systems are most frequently of the transimpedance type (voltage out/current in). These amplifiers convert the light-modulated current of the photodiode into a signal compatible with the main amplifier. Requirements on the pre-amplifier are
severe, namely: low noise, large bandwidth, high gain and sufficiently damped transfer and phase characteristics. These requirements, when using a single silicon process technology for all RF system blocks, accounts the pre-amplifier, in combination with the photodiode, being the limiting component with respect to the bandwidth. This justifies the use of an optical pre-amplifier (see Figure 8.1), to compensate for losses in the fibre optic link and integrated optics circuitry, ensuring a significantly higher input signal to the photo diode. Increasing the signal level allows the designer to exchange some of the noise performance for greater bandwidth. Amplifiers designed for extremely wide bandwidths require, however, extra care in the realization of specific transfer and phase behaviour. In the following sections, the design of wide-band pre-amplifiers for optical systems is considered in some detail.

8.2.1 Feedback amplifiers that use a purely capacitive source

The information content of an optical signal may be transformed into current fluctuations using a photodiode. Since the simplest equivalent circuit of a photodiode is a current source in parallel with a capacitance, an amplifier with zero input impedance is required to preserve the integrity of the signal. Two feedback amplifier configurations are in general use: the current-to-current amplifier (see Table 8.1 a) and the transimpedance amplifier (see Table 8.1 b). In circuit solutions based on discrete components, the current-to-current amplifier has some advantages over the transimpedance amplifier, since parasitic elements in the feedback path \( C_{pan} \) (see Table 8.1a), can be compensated in the other feedback branch by adding a compensation capacitance \( C_c \). In integrated circuit design, this advantage is less pronounced because the parasitics of the feedback components can often be neglected. In this section we address the realization of sufficiently damped transfer and phase characteristics for integrated feedback amplifiers employing a purely capacitive source.

Compensation of the transfer characteristics using one feedback loop

An optical transimpedance amplifier is depicted in Table 8.1b. Using a nullor with constant voltage gain \( A_{DC} \), the transfer of this configuration is limited in bandwidth by a single pole whose position is defined by the external time constant \( \tau_E = R_f C_s \) and the constant voltage gain \( A_{DC} \) of the amplifying component, yielding \( P_1 = (1 - A_{DC})/(R_f C_s) \).

In actual circuit design, however, the amplifying component has its own internal time constant \( \tau_A \) which affects the behaviour of the transfer characteristic and can cause a undesired peaking (see also [8.9]). Replacing the amplifier gain by \( A = A_{DC}/(1 + j\omega\tau_A) \) yields a second order transfer function with pole positions given by:

\[
P_{1,2} = \frac{-\tau_A + \tau_E}{1 - A_{DC}} \pm \frac{\sqrt{\left(\tau_A + \tau_E\right)^2 - 4\tau_A\tau_E}}{2\tau_A\tau_E} \frac{1 - A_{DC}}{1 - A_{DC}}
\]  

(8.1)
### TABLE 8.1. Pre-amplifier configurations for a pure capacitive source

<table>
<thead>
<tr>
<th>basic circuit</th>
<th>gain function amplifier</th>
<th>transfer function</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>a) Current-to-current amplifier</strong></td>
<td>$A = \frac{u_0}{u_i} = A_{DC}$</td>
<td>$A_i = \frac{i_{out}}{i_s} = \frac{AR_{f1} + (A-1)R_{f2}}{R_L + (1-A)R_{f2}}$</td>
</tr>
<tr>
<td><img src="image" alt="Diagram of current-to-current amplifier" /></td>
<td></td>
<td>$\frac{1}{p\frac{(R_{f1}+R_{f2})R_L+R_{f1}R_{f2}C_s}{R_L+(1-A)R_{f2}}+1}$</td>
</tr>
<tr>
<td><strong>b) Transimpedance amplifier</strong></td>
<td>$A = \frac{u_0}{u_i} = A_{DC}$</td>
<td>$Z_i = \frac{u}{i_s} = R_f\left(\frac{A_{DC}}{1-A_{DC}}\right)\frac{1}{p\left(\frac{R_fC_s}{1-A_{DC}}\right)+1}$</td>
</tr>
<tr>
<td><img src="image" alt="Diagram of transimpedance amplifier" /></td>
<td></td>
<td>$A = \frac{u_0}{u_i} = \frac{A_{DC}}{1 + j\omega \tau_A}$</td>
</tr>
<tr>
<td><strong>c) Transimpedance amplifier with double feedback loop</strong></td>
<td>$A = \frac{u_0}{u_i} = A_{DC}$</td>
<td>$Z_i = \frac{R_f\left(\frac{A_{DC}}{1-A_{DC}}\right)}{p^2\frac{\tau_A^2}{1-A_{DC}} + \frac{\tau_A + \tau_E}{p^2\frac{1}{1-A_{DC}}+1}}$</td>
</tr>
<tr>
<td><img src="image" alt="Diagram of transimpedance amplifier with double feedback loop" /></td>
<td></td>
<td>$A = \frac{u_0}{u_i} = \frac{A_{DC}}{1 + j\omega \tau_A}$</td>
</tr>
</tbody>
</table>

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It is clear from (8.1) that the poles become complex for some values of $\tau_A$, $\tau_E$ and $A_{DC}$. In order to obtain a stable, sufficiently damped response, the second order Butterworth positions for the poles can be approximated, for large values of $A_{DC}$ (see equation (8.1)), by using one of the following conditions for the delay times: $\tau_E = 2\tau_A(1 - A_{DC})$ or $\tau_E = \tau_A/(2(1 - A_{DC}))$. It is common practice to choose the first solution for $\tau_E$ (the second solution is only of limited use). We assume for reasons of simplicity that the gain-bandwidth product of the amplifying component is a linear function of the maximum achievable oscillation frequency $f_{Max}$ within a given process technology$^1$. The time constant $\tau_A$ can then be approximated as:

$$\tau_A = \frac{|A_{DC}|}{2\pi f_{Max}}$$  \hspace{1cm} (8.2)

Substitution in (8.2) yields:

$$\tau_E = 2\frac{|A_{DC}|^2}{(2\pi f_{Max})^2}$$  \hspace{1cm} (8.3)

This equation makes clear that for a given silicon process technology the choice of $A_{DC}$ results directly in conditions on $R_I$ and $C_S$ or visa versa and should be considered an important parameter with respect to the stability and damping conditions on the transfer characteristic of the transimpedance amplifier.

Compensation of the transfer characteristics using two feedback loops

Design parameters associated with the transimpedance amplifier of Table 8.1b are found to share a rather fixed relationship so as to guarantee a sufficiently damped transfer characteristic. For very wide bandwidths this limits design freedom since more than the stability condition must be met. In [8.13] a dual-feedback variant is introduced as shown in Table 8.1c to compensate for the time delay of the amplifying element. An extra voltage feedback loop [8.13] is introduced to provide additional phase adjustment and deal with the peaking problem. The capacitance $C_f$ introduces an extra pole and zero in the transfer function as shown by nodal analysis of the circuit of Table 8.1c. The most important effect of the feedback capacitance $C_f$ however, is the direct and dominant influence on the pole positions (note that this is particularly valid for larger values of $G$ (see Table 8.1c)). This influence on the pole positions remains also valid when considering a second order function for the amplifying component (e.g. $A = A_{DC}/(1 + p\tau_A)^2$). To illustrate the effect of $C_f$ on the pole positions we consider the circuit of Figure 8.2. We have simulated this circuit using data taken from an experimental double poly bipolar process technology [8.12]. The photo diode capacitance is taken to be 0.1 pF. In Figure 8.3 simulation results are given for $C_f$ set to zero and 0.03 pF. As can be seen in Figure 8.3a, $C_f$ can be used to manipulate the pole positions without affecting the noise level (see Figure 8.3b). Reduced peaking leads to lower phase variation within the bandwidth of the amplifier (see Figure 8.3c where the phase difference $\Delta\phi$ of the transfer is plotted with respect to the constant delay time.

---

1. Note that we found in Chapter 2 that the maximum of $f_{Mac}$ is independent of the transistor geometry and biasing.
\[ \frac{u}{i_s} = \left| \frac{u}{i_s} \right| e^{-j(\Delta \phi + \omega t)} \] The circuit topology of Table 8.1c, has been realized in SiGe technology \cite{8.13} resulting in a very-wide band amplifier which handles bit rates up to 20 GB/s.

![Figure 8.2. Transimpedance amplifier with dual-feedback loop](image)

![Figure 8.3. The transimpedance (a), spectra of equivalent input noise current (b) and phase behaviour (c) as function of frequency for the circuit shown in Figure 8.2 with \( C_f \) set to zero and 0.03 pF](image)

1. It must be noted that the transimpedance gain in this reference was not measured using an actual photodiode, but was simulated using the measured s-parameter data obtained with a wafer prober in a circuit configuration with an ideal capacitive signal source.
8.2.2 Feedback amplifiers with inductive input tuning

In the previous sections we considered the design of pre-amplifiers for purely capacitive sources. In practice, however, series inductance resulting from the photodiode (InP) amplifier (Si) bondwire interconnection is often difficult to avoid in a hybrid configuration. The combination of diode capacitance and bondwire inductance will lead, for sufficiently high frequencies, to an input circuit resonance, which reduces the noise level while leading to a peak that degrades the flatness of the gain-frequency characteristic (see Figure 8.4).

![Resonance Diagram](image)

**Figure 8.4.** Resonant input circuitry connected to a nonideal transimpedance amplifier input.

In practice, this input network resonance should be placed outside the desired frequency range (by keeping the length of the bondwires as short as possible). To optimize the signal-to-noise ratio, the resonance described should be used for noise reduction and be compensated by the amplifier design [8.10, 8.16, 8.14]. One compensation technique is to shift the poles of the input circuitry directly into the Butterworth positions.

**Butterworth compensation**

An optical transimpedance amplifier based on an ideal nullor with a constant voltage gain is shown with its transfer and noise characteristic in Table 8.2a. The transimpedance amplifier has an input impedance of almost zero within the design bandwidth which is limited by a single pole as discussed in section 8.2.1. Modifying this set-up by introducing an inductive bondwire interconnect between the capacitive source and the input of the amplifier (see Table 8.2b) leads to two complex poles on the imaginary axis and resonance at frequency:

\[ f_{res} = 1/(2\pi \sqrt{L_b C_s}) \]

The resonance leads to a reduction of the noise level for this configuration.
TABLE 8.2. Evaluation of pre-amplifier configurations using an ideal amplifying element (nullor) for purely capacitive sources and capacitive sources connected with inductive bondwires

<table>
<thead>
<tr>
<th>Feedback pre-amplifier configuration</th>
<th>poles and zeroes</th>
<th>Transimpedance $Z_i(=u/i_s)$ and the spectrum of the equivalent noise current at the amplifier input $S(i_{tot})$</th>
</tr>
</thead>
<tbody>
<tr>
<td>transimpedance amplifier with no inductive tuning</td>
<td><img src="image" alt="Image of transimpedance amplifier with no inductive tuning" /></td>
<td><img src="image" alt="Graph of transimpedance amplifier with no inductive tuning" /></td>
</tr>
<tr>
<td>transimpedance amplifier with inductive tuning</td>
<td><img src="image" alt="Image of transimpedance amplifier with inductive tuning" /></td>
<td><img src="image" alt="Graph of transimpedance amplifier with inductive tuning" /></td>
</tr>
<tr>
<td>transimpedance amplifier with inductive tuning and Butterworth compensation</td>
<td><img src="image" alt="Image of transimpedance amplifier with inductive tuning and Butterworth compensation" /></td>
<td><img src="image" alt="Graph of transimpedance amplifier with inductive tuning and Butterworth compensation" /></td>
</tr>
</tbody>
</table>

For more information on $S(i_{tot})$ see "Further justification for the use of this Figure of Merit" on page 42
In order to shift the input network poles to the Butterworth positions, an amplifier should be applied with nonzero positive input impedance. A configuration that has a well-defined input impedance within its working bandwidth, is the characteristic impedance amplifier of Table 8.2c. This configuration combines noise reduction with a well-behaved gain-frequency transfer characteristic.

The same strategy can be applied to the configuration of Table 8.2c using a realistic amplifying element with one dominant pole, and the poles shifted to the third-order Butterworth positions. The simplest practical implementation is shown in Figure 8.5a.

Figure 8.5. Single transistor configuration characteristic impedance pre-amplifier with inductive tuning

In Figure 8.5a the transistor dimensions and surrounding elements must be determined. To obtain useful initial values, we apply a design method that yields an approximate third-order Butterworth transfer characteristic given by:

$$\frac{u_{out}}{i_s} = \frac{A}{p^3 + \frac{p^2}{\omega_b} + \frac{p}{\omega_b} + 1}$$  \hspace{1cm} (8.4)$$

In Figure 8.5b, the active device of Figure 8.5a is modelled using the assumption that the Miller capacitance is dominant over the base-emitter capacitance. Solving the nodal equations, we obtain the following equation for the transfer characteristic:

$$\frac{u_{out}}{i_s} = \frac{A}{ap^3 + bp^2 + cp + 1}$$  \hspace{1cm} (8.5)$$

$a$, $b$, $c$ and $A$ are given by:
\begin{align}
a &= LC_s C_t \left( R_l + \frac{R_{bs}}{S} \right) \\
b &= LC_s + C_s C_{ts} (R_e (R_{bs} + R_t S) + R_{bs} R_l) + \frac{C_s C_{ts} (R_l - R_e^2 g_e - R_e) (R_{bs} + R_t S)}{1 + g_e (R_e + R_l)} \\
c &= C_t (R_{bs} + R_t S) + R_e C_s + \frac{C_s (R_l + R_t + R_e (g_e R_t - 1) - R_e^2 g_e)}{1 + g_e (R_e + R_l)} \\
A &= \frac{((R_{bs} + R_t S)(1 + g_e R_e)) p + (1 + g_e R_e - g_e R_t)) R_l}{1 + g_e (R_e + R_l)} = R_l
\end{align}

with the circuit parameters

- $C_s$ : photodiode capacitance
- $L$ : bondwire inductance
- $R_l$ : shunt feedback resistor
- $R_e$ : series feedback resistor
- $R_t$ : load resistor

and the transistor parameters

- $S$ : scaling factor of the transistor
- $R_{bs}$ : base resistance reference transistor
- $C_{ts}$ : base-collector capacitance reference transistor
- $g_e$ : transconductance

Setting (8.5) equal to (8.4), we obtain the following conditions for $a$, $b$ and $c$:

\begin{align}
a &= \frac{1}{\omega_b^2} \\
b &= \frac{2}{\omega_b^2} \\
c &= \frac{2}{\omega_b}
\end{align}

(Note that $A = R_l$ requires $R_l$ and $R_l > R_e$). Using the values for $C_s$, $\omega_b$, $R_{bs}$, $g_e$, $C_{ts}$ and $R_l$, as starting parameters, we obtain, based on the conditions on $a$, $b$, and $c$, a set of expressions for the dimensioning of the bondwire inductance $L$, the transistor size $S$ and the circuit elements $R_l$, $R_t$, and $R_e$. The equations involved are exact based on the network topology of Figure 8.5b assuming that $\omega_b = 1/\sqrt{LC_s}$. The final equations are given below:

\begin{align}
L &= \frac{1}{C_s \omega_b^2} \\
S &= \frac{\sqrt{LC_s - C_{ts} R_{bs}}}{C_{ts} R_t} \\
R_l &= \frac{R_{bs} + R_t S - C_s \omega_b R_{bs} R_l}{C_s \omega_b R_{bs}}
\end{align}
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\[ R_e = \frac{R_s g_e + R_{bs} g_e - C_s \omega_b R_s (S + R_{bs} g_e)}{C_s \omega_b R_s g_e} \]  
(8.14)

When the base-emitter capacitance is negligible, this method will yield a transfer characteristic close to the third-order Butterworth characteristic. We have applied the above to the first-stage design of a 10 GHz pre-amplifier using data for an experimental double poly bipolar process technology [8.12]. The \( C_s \) of the photo diode is 0.1 pF, the transimpedance gain \( A = 1000 \) (\( R_f \) is set to 1000 \( \Omega \)). Straight forward calculation results in an approximate third order Butterworth response. To improve on the noise performance one can lower the resistance \( R_e \), increasing peaking, thus yielding noise reduction and bandwidth enlargement (see Figure 8.6a and 8.6b). The main penalty for this action is the phase variation within the bandwidth of the amplifier (see Figure 8.6c, which depicts the phase difference with respect to a constant delay time).

**Figure 8.6.** a) The amplifier transimpedance, b) equivalent noise current, c) phase behaviour as function of frequency for the circuit shown in Figure 8.5 using the calculated values for \( L \), \( S \), \( R_f \) and \( R_e \) and the same circuit with \( R_e \) set to 1 \( \Omega \)

<table>
<thead>
<tr>
<th><strong>starting values</strong></th>
<th><strong>calculated values</strong></th>
</tr>
</thead>
<tbody>
<tr>
<td>( C_s )</td>
<td>0.1 pF</td>
</tr>
<tr>
<td>( f_b )</td>
<td>10 GHz</td>
</tr>
<tr>
<td>( R_t )</td>
<td>1000 ( \Omega )</td>
</tr>
<tr>
<td>( R_{bs} )</td>
<td>52.7 ( \Omega )</td>
</tr>
<tr>
<td>( C_{ts} )</td>
<td>25.8 fF</td>
</tr>
<tr>
<td>( I_c )</td>
<td>1 mA</td>
</tr>
<tr>
<td>( L )</td>
<td>2.53 nH</td>
</tr>
<tr>
<td>( S )</td>
<td>0.565</td>
</tr>
<tr>
<td>( R_f )</td>
<td>862 ( \Omega )</td>
</tr>
<tr>
<td>( R_e )</td>
<td>55.6 ( \Omega )</td>
</tr>
</tbody>
</table>

The above design example illustrates that, using modern Si technology with inductive input tuning, a stable well behaved circuit design can be realized that combines wide-band transfer of 10 GHz with low equivalent input noise current and phase variation. Fine tuning of the
circuit can best be performed by considering the transfer of the whole circuit, not only the first stage. For this reason the equations (8.11) to (8.14) should be used to calculate initial design values.

8.2.3 Experiments

As a practical example, we have designed and built a conventional transimpedance amplifier array for use with a four channel optical wavelength demultiplexer (see Figure 8.1 for the system concept). The choice for this type of amplifier is based on the expected spread in capacitance (0.3 to 1 pF) of the InP photodiodes. This spread in capacitance prohibited the use of inductive peaking techniques for noise reduction and bandwidth extension. The layout of the hybrid receiver is given in Figure 8.7.

![Image of the hybrid receiver layout](image)

**Figure 8.7.** Layout of the hybrid Wavelength Demultiplexer Receiver

The optical chip (InP) and the electrical chip (Si) are mounted on a 0.8 mm thick epoxy print (FR4) and are connected by bondwires. The pre-amplifier array has been designed to meet the following requirements and conditions:

- 3 dB bandwidth 2.5 GHz.
- Photodiode capacitance in the range of 0.3 pF to 1 pF.
- Anode connectable photo diodes (common cathode for the diode array).
- Insensitive to bondwire inductance and print layout.
- Low crosstalk level.
- Realization in an experimental silicon process with only limited design facilities.
The above conditions combined with the short time available for the design, limited our choice to a simple and straightforward circuit design. A conceptual schematic for the pre-amplifier array is given in Figure 8.8.

![Pre-amplifier array schematic](image)

**Figure 8.8.** Electrical schematic of the WDM receiver with transimpedance amplifiers

As indicated in Figure 8.7 and Figure 8.8, considerable attention has been paid to channel isolation. By using properly grounded planes between the signal paths and an alternate ground-signal-ground connection scheme for the pre-amplifier array the electrical crosstalk is significantly reduced. The crosstalk caused by the print layout can be even further reduced by using a thinner substrate with a higher dielectric constant, facilitating the use of smaller layout dimensions.
Results and discussion

The measurements were carried out as discussed in [8.19]. We restrict ourselves here to the frequency response (see Figure 8.9) and the crosstalk. As can be seen in Figure 8.9, a 3 dB bandwidth of approximately 1 GHz has been realized. This is lower than the estimated 3 GHz when using 0.5 pF photo diodes. The explanation for this deviation is found in an unexpectedly high parasitic series resistance of the photo diodes, yielding an early roll-off of the gain frequency characteristics. The crosstalk for two neighbouring channels is found to be at least 25 dB down at 1 GHz. From simulations, it was concluded that a significant part of the crosstalk is caused by coupling of the bondwires at the output of the pre-amplifiers. Simulation indicates that isolation may be improved by adding extra grounded bondwires at the outer channels to reduce the relatively high level of crosstalk between channels 1 and 2 and channels 3 and 4.

![Figure 8.9. Frequency response and crosstalk measurements](chart.png)
8.3 A high-gain AGC amplifier with a 3 dB bandwidth of 4 GHz

In the following sections the hierarchical design of an integrated AGC amplifier in silicon that uses the developed RF design environment, is addressed. The amplifier chip has been realized in QUBIC, a Philips Semiconductors BiCMOS foundry process, it features 1 micron geometry and encompasses more than eighty active devices. The AGC amplifier was designed for use in a 2.5 GBit/s coherent optical receiver. The amplifier was required to have a 3 dB bandwidth of at least 4 GHz and a minimum voltage gain of 30 dB (equivalent to an $s_{21}$ of 24 dB). Additional requirements were a gain control range greater than 30 dB and the use of a standard 32 pin quad flat-pack ceramic package.

8.3.1 The circuit design

The well-ordered design of complex integrated analog circuits is predicated on limited interaction between the constituent circuit blocks. One way to satisfy this, is the use of cascaded amplifier cells with a large intercell impedance mismatch, which provides a potentially wide bandwidth [8.1]. Interconnections between the amplifier stages must be kept short in respect to the minimum wavelength involved. The work of Reimann and Rein [8.7] who described an AGC amplifier design with a 3 dB bandwidth of 2.5 GHz was used as a starting point for this study.

The design of the AGC amplifier included additional specifications related to gain control, temperature stabilization and balance as well as to the unbalanced application of the circuit. Further, in all the simulations, the influence of bondwires, process tolerances etc. have been considered. The top level of the AGC amplifier design, including packaging parasitics, is given in Figure 8.10. The unbalanced operation for characterisation by using a network analyzer (see Chapter 7) is given in this figure. A block diagram of the silicon chip is depicted in Figure 8.11.

![Figure 8.10](image_url) Top level of the AGC amplifier in measurement configuration

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A high-gain AGC amplifier with a 3 dB bandwidth of 4 GHz

Figure 8.11. AGC amplifier block diagram

The signal travels from left to right passing the matching input buffer (IB), two gain-controllable amplifier cells (A1 and A2), each with a maximum of 12 dB gain, a fixed 12 dB gain amplifier cell (A3) and the output buffer (OB). For stability reasons, the ease of compensation techniques and the fact that DC coupling between stages is used, differential architecture is required. The gain control signals are related to the differential voltage coming from the AC component peak detector PDAC and the DC reference peak detector PDDC. The peak detectors feed their signals to the off-chip integrator circuit. The harmonic distortion of the high-frequency signal is lowered by using an offset control circuit to reduce unbalance in the dc operating points of the amplifier stages.

8.3.2 The input buffer

The implementation of the input buffer together with an unbalanced 50 ohm external source is shown in Figure 8.12. It should be noted that, in combination with an external matching circuit, the impedance level can be chosen to be 50 or 100 ohms. The extra resistor (marked with an asterisk in Figure 8.12.) is necessary in this input circuit in order to obviate common mode to differential mode conversion of the supply voltage disturbance component on chip. The bondwire inductance in combination with the input impedance of the emitter follower input buffer can lead to unwanted resonances. Considerable effort has been expended on the development of a multipurpose wide-band input buffer to circumvent this problem. A solution has been found in a configuration that uses a series RC-network in parallel with the input transistor to compensate for the negative input impedance. This solution yields an input buffer transfer characteristic (including package effects) that is flat within 2 dB up to at least 4 GHz. An additional advantage of the input compensation is that this circuit block has a very low power consumption.
8.3.3 The amplifier cells

The design of the wide-band amplifier cells is based on the circuit principles first proposed by Cherry and Hooper 33 years ago [8.1]. The combination of alternating transadmittance (TAS) and transimpedance stages (TIS) gives a substantial impedance mismatch between succeeding stages and leads to excellent wide-band performance. A dc-coupled differential amplifier cell based on this principle is given in Figure 8.13.

Figure 8.12. The input buffer with unbalanced input circuitry for testing purposes

Figure 8.13. Principle circuit of the differential amplifier cells
A high-gain AGC amplifier with a 3 dB bandwidth of 4 GHz

This cell consists of a Cherry and Hooper stage and two emitter-follower stages. The emitter followers provide a dc level shift and increased impedance transformation. Proper transistor dimensioning and biasing are essential to obtain 4 GHz wide-band performance. The base resistance of the transistors involved is one of the bandwidth limiting factors in cascaded Cherry and Hooper stages. Scaling up the emitter length can reduce the base resistance but this will also increase the junction capacitances. Through careful transistor design, a low base resistance in combination with acceptable junction capacitances can be obtained at a moderate bias current. The equivalent circuit parameters for a typical transistor as used in the AGC amplifier are given in Table 8.3

<table>
<thead>
<tr>
<th>transistor property</th>
<th>value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Emitter mask size</td>
<td>4 identical 2.4 x 2.4 ( \mu ) m(^2) emitters</td>
</tr>
<tr>
<td>Cut-off frequency</td>
<td>9.5 GHz</td>
</tr>
<tr>
<td>Current gain</td>
<td>90</td>
</tr>
<tr>
<td>Emitter-base capacitance</td>
<td>59.6 fF</td>
</tr>
<tr>
<td>Collector-base capacitance</td>
<td>44.0 fF</td>
</tr>
<tr>
<td>Collector-substrate capacitance</td>
<td>65.2 fF</td>
</tr>
<tr>
<td>Base resistance</td>
<td>72.1 ( \Omega )</td>
</tr>
</tbody>
</table>

**Bias conditions**

For a well-behaved functioning of the DC offset control and a proper transfer under clipping conditions, the DC transfer function should be optimized. That this is desirable can be illustrated by plotting the differential input-to-output voltage characteristics for different ratio’s of the current sources \( I_1 \) and \( I_2 \) (see Figure 8.13 and Figure 8.14). For this plot, we have assumed that all transistors are biased for maximum \( f_T \) and the resistors \( R_{sh} \) and \( R_s \) are determined by the desired AC voltage gain \( A_{vol} = R_{sh}/R_s = 5 \). As can be observed from Figure 8.14, the current ratio \( I_1/I_2 \) has a remarkable influence on the large-signal behaviour. This behaviour is caused by the fact that the output voltage \( V_{out} \) is a superposition of the inverting \( I_2 \) and the noninverting \( I_1 \) at the output collector resistors. From Figure 8.14 we deduce that the current ratio \( I_1/I_2 \) should be taken greater than 2 to enforce a monotonic transfer characteristic.

**Adjustments for a very-wide-band transfer**

To further increase bandwidth, a decrease in the TAS feedback with frequency is desired. This can be implemented by adding a simple capacitor or a tunable peaking impedance in parallel to the series feedback emitter impedance (see Figure 8.13).

This peaking impedance changes the local feedback in the Cherry and Hooper stage and can be used to overcome problems posed by process tolerances and variation of the bond-wire inductances. The cells A1 and A3 (see Figure 8.11) have been provided with this peaking facility. By using this externally controllable tuning facility (see Figure 8.15), the slope of the gain frequency characteristic can be modified, cancelling out hard-to-control parasitic effects, and yielding a flat overall gain-frequency characteristic.

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Figure 8.14. The DC transfer characteristic of the Cherry and Hooper stage

![Diagram showing the DC transfer characteristic](image)

Figure 8.15. Circuitry for an externally tunable feedback impedance

![Diagram showing the circuitry](image)

In the previous chapter, we saw that for stability reasons it's very important to keep the circuitry perfectly balanced. So, when adding extra capacitance to reduce the local feedback, an anti series or parallel connection should be applied to cancel out the parasitic bottom plate to substrate capacitance of an integrated capacitor.

Consistent with the dynamic range requirement, the first two amplifier cells (A1, A2) have
variable gain. Gain control of these cells is based on the application of a four-quadrant multiplier (often used in balanced mixers) which offers wide dynamic range and high linearity for large input voltage swings. In principal differential signals are converted to common-mode signals at low gain levels. In the case of total conversion of the differential signal into a common-mode signal, no amplification occurs. A TAS with a four-quadrant multiplier is shown in Figure 8.16. This proved to be well suited for the present task [8.7]. We used the circuit shown in Figure 8.16 in the first amplifier cell (A1). The schematic for the second amplifier cell (A2) shown in Figure 8.17 is similar to that of cell A1, with the exception of the reversed gain control and signal input. In this configuration, four (equal) series feedback resistors and two shunt capacitors are required in the two upper differential stages. This different set-up for the first and second variable gain cell has two advantages:

- Two emitter-follower stages are sufficient to shift the signal level between the first and second cell.
- This approach provides compensation of the gain-frequency characteristics of cells A1 and A2 for different gain levels. This is made possible since cell A1 the gain control is part of the ac signal in path in contrast with the situation in cell A2.

The current sources in Figure 8.13 are implemented as simple resistors. A current mirror at this point is undesirable due to the dominant parasitic capacitances of the transistors, which would lead to a decrease in impedance with frequency.

![Figure 8.16. A Cherry and Hooper stage with a four-quadrant multiplier (used in cell A1)](image-url)
8.3.4 The output buffer

The output buffer should fulfill the following requirements:

- Floating output combined with a good impedance match at the output (to avoid instability see Chapter 7).
- A flat frequency characteristic.
- Insensitive to variation in the bondwire inductance.
- External output impedance (open collector output).

This list of requirements on the output buffer is nontrivial. In particular, the matching problem (which leads to a 25 ohm load, as seen from the chip), in combination with the inductance of the bondwires which range from 2 to 6 nH, is problematical. Paralleling pins will reduce the inductance. One commonly used solution has a balanced open collector output to provide high output impedance. However, sensitivity to bondwire variation remains a problem. Feedback contributed by the parasitic capacitances $C_{bc}$ of the output transistors, results in additional mismatch in the output coupled with some peaking in $s_{21}$. This leads in turn to reduction in the stability factor $K$. Simulations have shown that a modified open collector buffer that uses the external output circuit depicted in Figure 8.18 is less sensitive to this problem.
A high-gain AGC amplifier with a 3 dB bandwidth of 4 GHz

Figure 8.18. The output buffer

The compensation circuitry has a positive influence on the stability factor $K$ in unbalanced operation as well as on the output match. This is illustrated in Figure 8.19.

**Figure 8.19.** Simulated output match ($s_{22}$) and stability factor $K$ as function of frequency for two different types of output buffer
8.3.5 The gain control

The gain-control-voltage generation is based on a two-Peak-Detector (PD) structure as shown in Figure 8.11. We have chosen two PD's to cancel out the effects of temperature variation. One PD detects the maximum value of the output signal (dc and ac component). The second PD detects only the value of the dc component. The difference between the output signals of the PD's is directly related to the ac amplitude. Temperature variations which affect the dc level of the output signal will not influence the differential voltage between the PD outputs.

The differential voltage output of the peak detector structure is fed to an external integrator. The output of the integrator circuit is connected to the AGC controller (on chip). The AGC controller supplies the control voltages for the gain cells A1 and A2. The symmetrical structure of the controllable amplifier cells demand stringent requirements on the control voltages. Control signal deviation from zero causes cell amplification. If the control signals change sign, amplification will once again occur. To ensure gain control stability, the differential gain control signal should be between 0 (no amplification) and 150 mV (maximum gain). Higher voltages will disturb the amplifier operation. A second condition for stable behaviour of the gain control is the absence of high-frequency components on the control voltages. Extra capacitors in cells A1 and A2 reduce the bandwidth of the gain control.

8.3.6 The offset control.

In high gain dc-coupled amplifiers, automatic offset control is mandatory. This is because a small offset at the input will cause a major change in operating point in the following differential stages. An offset in the operating point will lead to an increase in the second harmonic of the HF signal, and this should be avoided. A simple integrator circuit has been used to obtain offset control. For test purposes, offset control was realized off chip.

8.3.7 Further circuit design remarks

To ensure proper behaviour of the circuit, conscientious attention to detail was of the utmost importance. Three of the most significant design aspects are listed below:

- In order to reduce the bondwire inductance of the most important signal paths, the size of the chip was customized to the size of the standard 32 pin quad flat-pack ceramic package.
- Particular attention has been paid to avoiding asymmetry in the layout of the chip.
- All critical capacitors (on chip) in the HF path were specially placed in pairs such that their parasitics are balanced to substrate.

Layout generation is in conformance with the standard design flow of the QUBiC process [8.8]. A photograph of the chip showing the first amplifier cell is given in Figure 8.20. In this figure, the balancing of parasitics in the chip layout can be observed.
8.3.8 Simulations

The development of the AGC amplifier was carried out with the aid of HP’s Microwave Design System (MDS) and Pstar (Philips’ in-house-simulator, and part of QUBiTic’s recommended design flow). Fine tuning was carried out using the advanced bipolar transistor model, Mextram. After fine-tuning, Gummel-Poon and Mextram yielded comparable results. The resulting low current levels tend to mask differences in the Mextram and the Gummel-Poon models in this application.

Although dc and ac analysis are rather straightforward, the calculation of large-signal behaviour is more troublesome. The behaviour of the feedback circuitry and the great difference in time constants between the HF signal path and the gain control loop complicate the simulation. This has proved to be independent of the simulation method employed. Both Harmonic Balance (HB) and Time Domain (TD) methods have their disadvantages. In the case of HB (as implemented in MDS release 4.0), the gain control feedback loop causes a poorly chosen initial guess of the circuit simulator. Consequently, convergence of the solution takes excessive computing time. Time domain simulations are problematical because of the difference in time constants in the HF signal path and the gain control loop. The computation of steady-state conditions seems, in this case, interminable. In spite of these difficulties, we have analysed the large-signal behaviour of the complete network and the operation of the AGC loop. The results obtained with these advanced simulators have been used to verify the circuitry under development and are in conformance with the measured results.
8.3.9 Experimental configuration and results

The packaged chip was soldered to a low-cost FR4 (0.8 mm) glass-epoxy pc board. Use of this material facilitated drill-hole metallization to provide good grounding. In the test print design, extra attention was paid to obtaining suitable frequency characteristics while avoiding interaction between input and output. In the most sensitive areas of the test circuit, uncoupling of the ac signals is carried out using two surface mounted device (SMD) capacitors in parallel with different values (e.g. 150 pF and 22 pF) to prevent capacitor self-resonance peaks from influencing the characteristics to be measured [8.11].

The frequency response of the test print placed in a Cascade Microtech MTF26 test fixture was measured with a Hewlett Packard 8510B / 8516A network analyzer - test set combination. Time domain measurements were carried out with a Hewlett-Packard 54120T 20 GHz Digitizing Oscilloscope. For the spectral measurement, we used a Hewlett-Packard 8592A 50 kHz - 22 GHZ Spectrum analyzer.

8.3.10 The gain frequency characteristics

The simulated and the measured gain frequency responses for several fixed gain levels as plotted in Figure 8.20 are in excellent agreement. The measured (3 dB) bandwidth is 4 GHz compared to a simulated bandwidth of 4.2 GHz. The gain control range is seen to be better than 50 dB.

![Figure 8.21. The measured and simulated (using the Mextram model) \( s_{21} \) as function of frequency of the AGC amplifier for a set of fixed gain levels](image)

8.3.11 Large-signal behaviour

Large-signal performance was determined by setting the amplifier to its maximum amplification and increasing the input power from -60 dBm to -10 dBm. Simulated and measured
A high-gain AGC amplifier with a 3 dB bandwidth of 4 GHz

Harmonic content versus input power is depicted in Figure 8.22. In the automatic gain control mode, worst case conditions for harmonic distortion occur when input and output signals are maximal (resp 700 mV and 400 mV peak to peak). Under these conditions, the third harmonic component (harmonic distortion) is typically more than 20 dB down. The time domain data for this situation using a 300 MHz input signal is illustrated in Figure 8.23. Note that the second and fourth harmonics will be lower in level than the third, due to the balanced operation of the circuit. Their amplitude behaviour is strongly dependent on the DC balance of the differential stages.

![Graph showing harmonic content versus input power](image)

**Figure 8.22.** Simulated (using the Mextram model) and measured harmonic content versus input power with the amplifier set for maximum gain
8.3.12 The AGC control

The operation of the AGC amplifier for various sinusoidal input levels is shown in Figure 8.24. An input dynamic range of 30 dB is controlled to a fixed output level.

Figure 8.24. More or less constant output voltage of the AGC amplifier for an input dynamic range of 30 dB
Conclusions

In summarizing the experimental results, we conclude that the AGC amplifier meets the performance specifications given in Table 8.4.

<table>
<thead>
<tr>
<th>parameter</th>
<th>measured result</th>
</tr>
</thead>
<tbody>
<tr>
<td>max. voltage gain</td>
<td>36 dB</td>
</tr>
<tr>
<td>3 dB bandwidth</td>
<td>4 GHz</td>
</tr>
<tr>
<td>gain control range</td>
<td>&gt; 50 dB</td>
</tr>
<tr>
<td>max. dynamic input voltage</td>
<td>700 mV</td>
</tr>
<tr>
<td>max. dynamic output voltage</td>
<td>400 mV</td>
</tr>
<tr>
<td>supply voltage</td>
<td>6 V</td>
</tr>
<tr>
<td>power consumption</td>
<td>450 mW</td>
</tr>
<tr>
<td>matchable impedance level</td>
<td>50 - 100 ohm</td>
</tr>
</tbody>
</table>

8.4 Conclusions

Using advanced simulation programs and well-established silicon foundry process technology (QUBIC) a low-cost, low-power, high-gain, wide-band AGC amplifier chip with large dynamic range has been designed for mounting in a standard ceramic package. Testing was performed using glass-epoxy pc board. Simulated and measured data show excellent agreement.

8.5 References


Chapter 9  Conclusions and recommendations

9.1 Overview

The work presented in this thesis deals with high-frequency aspects of silicon bipolar IC technology and design. The contents can be divided in three. Firstly, HF bipolar IC technology characterization in terms of operating speed and noise properties is introduced. Secondly, the current state of compact public domain bipolar transistor models is discussed and thirdly, wide-band amplifier design is considered with attention focused on circuit topology and its influence on stability.

This chapter reviews the most important results and conclusions placing them in a wider context with suggestions for future work.

9.2 Figures of Merit

The Figures of Merit treated in this thesis provides means to rank bipolar process technologies in terms relevant to real circuit design, e.g. the maximum oscillation frequency, switching speed and noise properties. A relatively small set of process characteristics including series resistances, depletion capacitances and delay time are shown to be sufficient for the ranking. The Figures of Merit discussed are process technology specific and thus not restricted to a single device. This implies that one can rate process technologies without recourse to circuit theory.

In spite of the achievements in this area, there is still an important area open for the development of Figures of Merit. It is most desirable to have similar qualifications for the large signal properties of bipolar
transistors\(^1\), for example, maximum power efficiency, maximum power gain and output power under large-signal conditions for various biasing conditions (class A, AB, B or C). The design of transistors for optimum high frequency power handling is of enormous importance in present day process technology development. A clear and unified way to link process parameters to output stage power performance would be most useful.

9.3 Modelling of the bipolar transistor

In Chapter 4, four of the most important public domain compact models have been presented in tabular form in an unified manner, complete with their schematics, parameter descriptions and precise formulation. Differences in the formulation have been discussed and supported by graphical illustrations. Currently, the bipolar community is occupied with choosing a new "standard" as successor to the widely used Gummel Poon model. Europe tends to favour Mextrax while America may prefer VBIC95. At the time of writing of this thesis, the Mextrax model is unmatched in accuracy and performance compared to the VBIC95 model. Nevertheless, the compatibility of VBIC95 with the Gummel Poon model makes the model more accessible to a wider public than Mextrax. It may, therefore, be sometime before a single new standard emerges.

Given the current state of the art most bipolar transistors can accurately be modelled. Significant problems remain, however, in the area of bipolar power devices. The distributed nature of these devices is accompanied by considerable temperature variation over the die. This combination of an extensive bondwire complex, integral matching networks as well as the temperature gradient leads to a difficult modelling task which must be dealt with through segmentation.

9.3.1 High current operation and distortion

In the discussion of compact modelling nonlinear signal distortion introduced by the bipolar transistor under high current conditions is seen to be significant. In Chapter 5 attention has been paid to the influence of the parameters of the epilayer model on distortion properties at the onset of quasi-saturation. In Chapter 6, the base-collector charge formulation of the Mextrax model is extended with the charge \( \Delta Q_c \). Use of this extension, results in monotonic Early voltage and \( f_t \) versus collector current behaviour and a significantly improved modelling of high-current distortion at low as well as at high frequencies. This is illustrated using data introduced in Chapters 5 and 6.

The stringent requirements on linearity and spectral purity for circuits operating in densely populated frequency bands has stimulated an increased interest in the nonlinear behaviour of the bipolar transistor. In Chapter 5 we have found that a number of epilayer parameters of the physical based Mextrax model had a direct and or dominant influence on the high-current signal distortion. This suggest, that transistor performance with respect to distortion can be improved by changing the transistor doping profile and or planar geometries. This is, however, a far from nontrivial problem considering the transistor physics and circuit performance.

\(^1\) Note that the Figure of Merit for switching speed (\( \tau_{op} \)) is based on large signal conditions under the assumption that the transistor never enters quasi- or hard-saturation.
9.4 The design of integrated silicon wide-band amplifiers

High frequency amplifier design has always taken account of the question of stability. Most studies, however, treated single-ended amplifiers with one active device, concentrating on finding the proper source and load terminations for optimum noise and power gain, while avoiding oscillation. In modern wide-band IC design, the use of integrated balanced characteristic impedance amplifiers as general purpose building blocks is common practise. Contemporary stability studies of these amplifiers emphasize the negative influence of package and mounting parasitics on stability. In general, mounting parasitics limit the full exploitation of the potential gain-bandwidth product (GB) of modern HF silicon process technology. For this reason, minimization of package-related parasitics like bondwire inductance and pin-to-pin capacitance is highly desirable. In practice, however, the minimization of mounting parasitics is limited to the package or mounting technology available or specified by the customer. We have chosen to reformulate the stability problem in balanced amplifiers in generic terms in order to obtain a set of explicit guidelines for the designer in respect to the IC mounting configuration and circuit topology, thus minimizing the influence of parasitics. This stability analysis, which is not limited to a specific circuit, gain level, amplifier phase shift or mounting parasitic value, considers three different amplifier topologies namely: the single-ended amplifier, the balanced amplifier in differential operation and the balanced amplifier in unbalanced operation. The main conclusions found for these different configuration are summarized on page 154. Although the stability analysis in this thesis assumes on-chip termination, some attention is paid to the effect of off-chip matching. It has been found that worst-case conditions with respect to stability occur in the main for an amplifier phase shift of $\phi = -\pi/2$.

We have shown, theoretically that using conventional chip mounting techniques and applying narrowly spaced input and output lines (cancelling the feedback parasitics), stable balanced amplifiers can be realized with very high gain and large bandwidth. Amplifiers with floating output are shown to behave well in balanced as well as unbalanced operation and are relatively insensitive to asymmetry.

9.4.1 Design examples

With the implementation of Mextram, MOS model 9 and parts of the QUBiC process library in HP's Microwave Design System a HF silicon design environment has been created which provides a unique combination of accurate models and powerful simulator tools. In Chapter 8, a number of demonstrator circuits illustrating the use of this design environment are presented, namely, a series of pre-amplifiers and an AGC amplifier both intended for use in optical telecommunication systems. The pre-amplifiers make use of local as well as overall feedback techniques, depending on individual bandwidth and noise requirements, while the AGC amplifier is based on the use of local feedback. The pre-amplifiers and the AGC amplifier were realized in Philips Research's experimental double poly process and Philips Semiconductors 1 $\mu$m Bipolar/CMOS process QUBiC, respectively.

Application of the latest developments in SiGe process technology to the design of a series of very wide-band balanced amplifiers, with bandwidths in excess of 40 GHz should prove useful in verifying the stability analysis of Chapter 7.
The design of integrated silicon wide-band amplifiers
Summary

This thesis addresses in detail a number of issues related to the application of silicon technology for the realization of integrated high frequency circuits. The subjects discussed can be divided into three categories, namely:

**Technology characterization:** Here the accent is placed on the most important component in HF silicon design the bipolar transistor. The high frequency behaviour of bipolar transistors is traditionally expressed in terms of cut-off frequency $f_T$ and the maximum frequency of oscillation $f_{Max}$. In the case of integrated circuits, however, the $f_T$ and $f_{Max}$ are of limited applicability. Our discussion is based on two “new” Figures of Merit which better suit the reality of integrated circuit design. These Figures of Merit which have been developed in our group are related to the optimum switching speed $\tau_{opt}$ and the high frequency noise behaviour of the bipolar transistor configured for common emitter service. With the information provided it is possible, based on just a limited set of process parameters, to investigate the feasibility of realizing specific system functionality in a given process technology.

**Modelling:** Integrated circuit design is based on the use of equivalent electronic circuits for applicable active components. The closer these equivalent circuits approximate the device physics, the more efficiently and precisely the device behaviour can be explored. The accuracy of the model is, therefore, of great importance during the design phase. For this reason an important part of this thesis considers compact bipolar transistor models. In overview some properties and formulations for the four most important public domain transistor models are tabulated. In order of complexity these are: Ebers-Moll, Gummel-Poon, Extended Gummel-Poon (VBIC95) and Mextram. Model characteristics are compared for AC, DC and large-signal behaviour. More detailed analysis of the large-signal behaviour has led to an improved formulation of the base-collector charge in bipolar epitaxial models. This in turn resulted in improved modelling of nonlinear distortion at the onset of quasi-saturation, as well as in monotonic $f_T(I_C)$ and Early characteristics for low doped bipolar epitaxial transistors.

**Design:** Stability plays an important role in the design of wide-band amplifiers for telecommunication applications. Modern high frequency silicon technology facilitates the realization of very wide-band high-gain amplifiers. In general these amplifiers are limited in their gain-bandwidth product by unavoidable capacitive and inductive interconnect parasitics. This thesis presents a systematic analysis of stability aspects of wide-band amplifiers providing guidelines for the choice of amplifier topology so as to minimize sensitivity to interconnect parasitics, excitation type and possible asymmetries.

Finally, for illustrative purposes we present a number of circuits developed using the high frequency design environment realized during this thesis work. A series of low-noise pre-amplifiers and an automatic gain control amplifier (AGC) designed for use in optical demonstrator systems are described.
Samenvatting

Dit proefschrift behandelt een aantal facetten van de toepassing van silicium in het realiseren van geïntegreerde hoogfrequente schakelingen. De behandelde onderwerpen kunnen in drie categorieën verdeeld worden:

**Technologiekarakterisatie:** hierbij is een accent gelegd op de belangrijkste component in het HF silicium-ontwerp: de bipolaire transistor. Van dit onderdeel worden traditioneel de hoogfrequente eigenschappen uitgedrukt in de afsnijfrequentie $f_T$ en de maximale oscillatiefrequentie $f_{Max}$. Voor geïntegreerde schakelingen zijn deze kwaliteitsgetallen echter minder geschikt. Dit is de motivatie voor de bespreking van twee "nieuwe" kwaliteitsgetallen die beter aansluiten bij de ontwerppraktijk van geïntegreerde hoogfrequente schakelingen. De kwaliteitsgetallen die ontwikkeld zijn in de onderzoeksdoel hebben betrekking op de schakelnelheid $\tau_{opt}$ van CML-poorten en op het hoogfrequente ruisgedrag van een bipolaire transistor in een geaard-emitterconfiguratie. De zo verkregen informatie maakt het mogelijk, op basis van een beperkt aantal procesgegevens, een afschatting te maken van de realiseerbaarheid van bepaalde systeemfuncties met een gegeven procestechnologie.

**Modellering:** de ontwerptechniek van geïntegreerde schakelingen kenmerkt zich door het gebruik van equivalentele elektronische vervangingschemas voor de toe te passen active componenten. Naarmate deze vervangingsschemas de fysica beter beschrijven, kunnen de componenta eigenschappen efficiënter worden benut. De nauwkeurigheid van het model is dus van groot belang in de ontwerp fase. Om deze reden is een belangrijk deel van dit proefschrift gewijd aan compacte bipolaire transistormodellen. Dit hoofdstuk geeft een overzicht van de formulering en de eigenschappen van de vier belangrijkste, in de open literatuur vrij toegankelijke, transistormodellen. Dit zijn in volgorde van complexiteit: Ebers-Moll, Gummel-Poon, Extended Gummel-Poon (VGIC95) en Mextram. Van deze modellen worden de modelkarakteristieken onderling vergeleken voor DC-, AC- en groot-signaalcondities. Nadere bestudering van de groot-signalieigenschappen heeft geleid tot een uitgebreidere formulering van de basis-collectorlading voor bipolaire epilaag-transistormodellen. Dit resulteert in een verbeterde modellering van de niet-lineaire distorsie bij de aanzet van quasi-saturation, alsmede het verdwijnen van niet-fysische discontinuïteiten in de $f_T(I_C)$ karakteristieken en Early spanningen voor laag gedoteerde epilaagtransistoren.

**Ontwerptechniek:** stabiliteit is een belangrijk aspect in het ontwerp van breedbandversterkers voor telecommunicatie-toepassingen. Met behulp van de huidige siliciumtechnologie met sterk verbeterde hoogfrequente eigenschappen is het in principe mogelijk om zeer breedbandige versterkers met een hoge versterking te realiseren. In het algemeen zijn deze versterkers echter begrensd in hun versterkings-bandbreedteprodukt door het onvermijdelijke parasitaire reactieve gedrag van de IC-aansluitingen. Dit proefschrift bevat een systematische behandeling van de stabiliteitsaspecten van breedbandversterkers en geeft richtlijnen voor de te kiezen versterkertopologie. Het uitgangspunt hierbij is de versterker zo stabiel mogelijk te maken onafhankelijk van de aansluitconfiguratie, aansluitparasieten en eventuele asymmetrie. Ter illustratie van de tijdens dit promotieonderzoek gecreeëerde ontwerpomgeving is een aantal circuits ontwikkeld voor gebruik in een optische telecommunicatieontvanger: een serie van ruisarme voorversterkers en een versterker met een automatische volumeregeling (AGC).

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Samenvatting 193
Biography

Leo C.N. de Vreede was born in Delft, the Netherlands, on August 22, 1965. He received the B.S. degree in electrical engineering from the Hague Polytechnic in 1988. His bachelors thesis dealt with the realization of microwave filters using broadside-coupled inhomogenous transmission lines.

In the summer of 1988 he joined the staff of the Microwave Component Group of the Laboratory of Telecommunication and Remote Sensing Technology of the Department of Electrical Engineering, Delft University of Technology. From 1988 to 1990 he worked on the characterization and physically based modelling of CMC capacitors which resulted in the first accurate, predictive model for these devices.

Since 1991 Mr. de Vreede has been involved in the HF design and modelling of silicon based integrated circuits. One of his primary tasks was the study and implementation of accurate nonlinear models in commercial microwave design software in order to create a design environment suitable for the development of HF silicon ICs. He was the guest of Hewlett Packard in Santa Rosa, California in the summer of 1993 working on the Mextram implementation.
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