Development of silt measuring methods

Electronic signal processing:
A detection method for HF-bursts
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Ing. G.J. Dorenbos
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1. Introduction.

The circuit described in this report is part of the test-system built for attenuation- and scattering measurements on silt and particle suspensions. With this circuit, the frequency range of the detection circuit is extended from 20 MHz to 100 MHz. A complete description of this HF-detection circuit will be given, including specifications and measured performance.

The reported work was carried out on behalf of the Dutch Ministry of Transport and Public Works, Hydro-Instrumentation Department.
2. Principle.

Detection of attenuation-bursts is possible between about 1 and 20 MHz, using the existing LF-detection circuitry. However, detection of bursts is also needed in the frequency range from 20 to 100 MHz. Therefore a circuit has been developed to convert these HF-signals to a (IF-) frequency that can be detected using the existing LF-detection circuitry (AM-detector, integrator, etc). This conversion is done by mixing the received burst with a (LO-) frequency 10 MHz above or below the burst-frequency. The difference-frequency (10 MHz) is filtered from the output-frequencies with a bandpass-filter and used as input for AM-detection. The Local Oscillator consists of a frequency-synthesizer with a GPIB-interface, so the frequency-setting is directly computer-controlled for maximum flexibility and performance.

Fig. 2.1 Basic HF-detection circuit.
The next chapters contain a description of the several parts of the RF-detection circuit, Appendix B contains the schematic diagrams of the circuit.
3. LO-Synthesizer.

Fig. 3.1 shows a block diagram of a synthesizer formed by a PLL with a programmable divider. The schematic diagram of the circuit realised is shown in Fig. B.1.

![Block diagram of LO-Synthesizer](image)

**Fig. 3.1 Single-loop frequency synthesizer.**

- The frequency of the VCO (SP1648) is determined by the LC-tank-circuit. The value of $L_1$ is determined by the number of turns on the (adjustable) core, the value of $C$ (here D2) by the control voltage on the varactor-diodes. $L_1$ is tuned for an output-frequency from 25 MHz to 90 MHz, when the control-voltage varies from 1 V to 30 V.

- The HEF4750 contains the reference-oscillator and phase-detector. The reference-oscillator is a crystal-oscillator operating on 4.4 MHz, divided by 440 (set with the dip-switches), so the reference-frequency is 10 kHz. The reference-frequency is slightly adjustable with C7. The HEF 4750 actually contains two phase-comparators. One that is fast but not accurate, for fast settling of the loop, and one that is slow but accurate. The latter is necessary for a spectrally pure output-signal. (i.e. low phase-noise).
- The loop-filter is an active, first order lowpass filter which generates the VCO control-voltage.

- The programmable divider consists of a prescaler (Q1 - SP8660) and a programmable divider (Q2 - MC14515). The divide-ratio is $10 \times n$ ($n = 2^0 \ldots 2^{14}$). This results in a minimal frequency-step of $10 \times 10 \text{ kHz}$. Because of the difference in supply voltages between Q2 and Q5 a level-translator (Q3) must be used.

- The VCO is buffered with Q8 (MWA 110). R25 together with Q8's input impedance (50 Ohm) forms a voltage divider. This is done to reduce the VCO-output loading. After Q8 the signal is split and amplified for feedback and output. The output-level is appr. 0 dBm. (for more output-power adjust R25). 

---

1 This output-configuration is somewhat overdone. Probably a high-speed comparator for feedback, and a single amplifier for output-buffering also will meet the requirements. Instead of R24 and R25 one may use an impedance-trafo.

Appendix B.2 shows a schematic diagram of the mixer-circuit. The SL6440C is an active, high level, double balanced mixer. This mixer is preferable to a passive mixer, like the MiniCircuits SRA-3MH, because of the low insertion-loss (even gain is possible), while the performance is not significantly worse. In the configuration used here, the insertion-loss is appr. 0 dB. The penalty one pays is that two supplementary supply-voltages (10V, 12V) are needed. The performance of the mixer depends on the value of the supply-voltages. Therefore two separate adjustable supply-regulators are used. The output-trafo is used to convert the 50 Ohm load (filter) to a 200 Ohm load, which matches the mixer output-circuit.

The IF-frequency first was chosen to be 10.7 MHz, because ceramic filters are available for this frequency. However, ceramic filters perform well with continuous signals, not with bursts. That's why a 9 pole Chebyshev, 50 Ohm bandpass filter (highpass + lowpass) was chosen later.¹

¹ The measured characteristics at first seemed rather good. However a measurement made after some months showed a significant degradation in performance! So it is worth trying to build a bandpass-filter with less components, to achieve a better performance. Note the specifications (bandwidth...) needed!
5. GPIB-Interface.

Appendix B.3 shows the schematic diagram of the GPIB-interface circuit. The GPIB-interface is build around the HEF4738 GPIB-controller. Some external circuitry is added for buffering, initialisation and 8 to 16 bits conversion. It is configured as a basic listener and talker. The device-handshake is not used. The clock-frequency is 1 MHz, which means a maximum datatransfer-rate of 100 kbytes/second.
APPENDIX A  Electrical characteristics.

Mixer.

Supply voltage :  15 V  (12 V, 10 V)
Supply current :    95 mA  (I_p = 24 mA)
Conversion gain :     -1..0 dB
LO-input :            0 dB
LO-IF isolation :      27 dB
1 dB Compression point : > 8 dBm  (spec. 15 dBm)

Filter.

Center frequency :  11.1 MHz
-3 dB bandwidth :    2.5 MHz
Slope :             > 60 dB
Out-of-band rejection : > 45 dB
Insertion loss :  < 1 dB

LO-synthesizer

Supply voltage :    5, 15 V  (30 V)
Supply current :    215 mA
Frequency range :    25..90 MHz
Frequency resolution :  100 kHz
Frequency deviation :   +170 Hz/MHz (1)
Output level :       -1..0 dBm
Programming :        14 bit, binary (f = n * 100 kHz)

GPIB-interface

Supply voltage :    5 V
Supply current :    95 mA
Transfer rate :     max 100 kB/sec
Configuration :     Basic Talker/Listener,
                    Device I/O 16 bits (2 bytes)
                    Address set with jumpers (2)

---

1 The reference-frequency does not exactly equal 10 kHz.
The transfer characteristic of the mixer + filter (for continuous signals) is shown in fig. A.1. for several frequencies. These graphs show the linearity of the mixer, and the small difference in conversion gain over the entire frequency range.

In fig. A.2. the frequency-response of the mixer + filter (bursts) is shown. The bursts are generated with the burst-generator used in the measurement-system. The measured response (IF-filter) is compensated for the frequency-response of the PM5390S RF-synthesizer.

Fig A.3. shows the transfer characteristic of the IF-filter. Proper construction (shielding, components etc.) will enhance the filter performance above 40 MHz.

Some examples of signals in the measurement system are shown in fig. A.4.
SL6440 MIXER + FILTER
Transfer characteristics vs. frequency
RF = 20, 60, 100 MHz
IF filter output (dBm)
RF input (dBm)
SL6440 MIXER + FILTER

Frequency response of mixer + filter, compared with PM5390S (5 dBm, 50 Ohm).
Fig. A.3. IF-filter transfer characteristic.
Fig. A.4. Waveform examples.
APPENDIX B  Circuit diagrams
APPENDIX C  Software

FUNCTION LO_synt_init :INTEGER;

{ This function opens the LO-synthesizer interface  }
{ for the GPIB-PC card.            }
{ Address = 2; mark the jumpers on the interface-card  }
BEGIN
  bdname[1] := 'D';
  LO_synt_init := ibfind(bdname);
END;

PROCEDURE LO_frequentie (devicenr :INTEGER; VAR frequentie :REAL);

{ This procedure sets the LO-frequency on the LO-synthesiser  }
{ by programming the binary value of the frequency in 100kHz  }
{ The LSB of the value has to be programmed first.        }
{ NB. VAR frequentie in MHz!                               }
{ After programming the frequency, bit0 (of 0..15) is checked  }
{ for out-of-lock state of the synthesizer.                }
CONST mask = 2#00000000000000001;

VAR uit_waarde,count :INTEGER;
  comando        :woord;
  hulp           :BYTE;

BEGIN
  uit_waarde := ROUND(10 * frequentie);
  hulp := LOBYTE(uit_waarde);
  comando[1] := CHR(hulp);
  hulp := HIBYTE(uit_waarde);
  comando[2] := CHR(hulp);
  ibwrt(devicenr,comando,2);
  IF (iinsta AND ERR) > 0 THEN message;

  { Here the frequency is programmed  }
  { Now check for out-of-lock.    }
  { bit0 is HIGH for out-of-lock.  }
  { This may take a little time... }

  count := 0;
REPEAT
    ibrd(devicenr,commando,2);
    IF (ibsta AND ERR) > 0 THEN message;
    count := count + 1;
    UNTIL (count = 10) OR (((ORD(commando[1])) AND mask) = 0);
    IF (((ORD(commando[1])) AND mask) = 0
        THEN writeln('LO-frequentie = ',(uit_waarde/10):4:1,' Mhz')
        ELSE writeln('ERROR, synthesiser niet in lock')
    END;

PROCEDURE Set_LO_frequentie ( burst_frequentie :REAL);
{
This procedure determines the value of the LO-frequency
Here the IF-frequency is declared, and determined
whether mixing occurs with burst-frequency +/- IF-freq.
}
CONST IF_frequentie = 10.7 {MHz};
    mix_omslag = 60 {MHz};

VAR freq_LO :REAL;

BEGIN
    IF (burst_frequentie > 20) AND (burst_frequentie <= 100)
        THEN BEGIN
            IF burst_frequentie < mix_omslag
                THEN freq_LO := burst_frequentie + IF_frequentie
            ELSE freq_LO := burst_frequentie - IF_frequentie;
            LO_frequentie (dv1, freq_LO);
        END;
    END;
IEC/IEEE BUS INTERFACE

The HEF4738V is an implementation of the IEC bus as described in IEC report 66 CO 22 (interface system for programmable measuring apparatus) as well as in IEEE standard 488-1975 (standard digital interface for programmable instrumentation).

Together with bus drivers, level converters and multiplexers it is suitable for connecting electronic programmable and non-programmable equipment to an IEC/IEEE interface bus.

All inputs have standard HE4000B family levels.

In the circuit the following standard interface functions are incorporated:
- Complete source handshake (subset SH1)
- Complete acceptor handshake (subset AH1)
- Basic talker with serial poll and talk-only mode (when \( I_t = \text{LOW} \), subset T1; \( I_t = \text{HIGH} \), subset T5)
- Basic listener with listen-only mode (when \( I_t = \text{LOW} \), subset L1; \( I_t = \text{HIGH} \), subset L3)
- Complete service request (subset SR1)
- Complete remote local (subset RL1)
- Remote parallel poll configuration (subset PP1)
- Complete device clear (subset DC1)
- Complete device trigger (subset DT1)
- Some controller facilities

![Diagram](image)

Fig. 1 Basic IEC/IEEE bus interface using the HEF4738V.

**SUPPLY VOLTAGE**

<table>
<thead>
<tr>
<th>rating</th>
<th>recommended operating</th>
</tr>
</thead>
<tbody>
<tr>
<td>-0.5 to 18 V</td>
<td>4.5 to 12.5 V</td>
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</tbody>
</table>

**FAMILY DATA**

<table>
<thead>
<tr>
<th>IDD LIMITS category</th>
<th>LSI</th>
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</thead>
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<td></td>
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</tbody>
</table>
GENERAL DESCRIPTION
The inputs IRFD, IDAC, IDAV, IIFC, IREN, IDAT, IDV and IDIO1 to IDIO7 must be connected via an inverting TTL to LOCOS level converter to the respective bus lines: NRFD, NDAC, DAV, IFC, REN, ATN, IDY and DIO1 to DIO7. The outputs ORFD, ODAC, ODAA and ODRS can drive one standard TTL load and are suitable for driving NRFD, NDAC, DAV and SRO via an inverting bus driver circuit.
The parallel poll outputs OP1, OP2, OP3 and OPP can also drive one standard TTL load. Outputs OP1, OP2 and OP3 are connected to flip-flops, which store the attendant bits P1, P2 and P3 of the last PFE message. OP1, OP2 and OP3 have to be decoded externally and multiplexed to the DIO lines when OPP is LOW.
All other output stages are standard HE40008 family.
Most of the functions in the IEC/IEEE interface IC are realized with synchronous sequential logic, which is driven from the clock input CP. HIGH to LOW transitions are used to synchronize input signals and LOW to HIGH transitions trigger the internal flip-flops. In order to meet the IEC/IEEE timing specifications, the maximum clock frequency is 2 MHz. The maximum data transfer is then 200 kbytes/second.

Input IrFD (not ready for next message) and output Odvd (data valid device) are intended for a two-wire handshake procedure between the acceptor function in the IC and the data output of the device (instrument to be connected to the interface system). The procedure is made so that if the device reacts fast enough, the handshake procedure can be omitted by interconnecting Odvd and IrFD. The conditions to be fulfilled by the device are:
- The device must be able to accept a data byte within one clock period after dvd goes HIGH under all conditions.
- The device must be ready to process a data byte within two clock periods plus the minimum settling time of the talker devices under all conditions.

Input IrFa (not new byte available) and output Odcd (don't change data) are intended for a two-wire handshake procedure with the source function in the IC and the data output of the device (instrument). The procedure is made so that if the device reacts fast enough the handshake procedure can be omitted by interconnecting Odcd and IrFa. The conditions to be fulfilled by the device are:
- The device must be able to set a new data byte on the bus within one clock period after dcd goes LOW under all conditions.
- The device must be able to have the next data byte available within seven clock periods under all conditions.

Input IaR and output Ored should be connected to an external parallel-in/serial-out (when Ored is HIGH parallel-in, when LOW serial-out) shift register, which must be connected to the clock CP and must trigger on the LOW to HIGH transitions. The data on the parallel inputs of this external shift register are loaded in parallel and shifted-out via input IaR into an internal shift register. The eleven serial input signals are in the order of shifting: A5, A4, A3, A2, A1, ton, lon, lt, rsv, rti and ist.
Signals A5, A4, A3, A2 and A1 represent the device talker and listener address. When signal 1 (either listener or talker) is HIGH, a listener addressing sets the talker to the idle state and a talker addressing sets the listener to the idle state (subset T5 and L3). With it LOW, the device can be addressed to be a listener and a talker. Because of the serial input procedure, all these input signals arrive in the interface functions of the IC between 16 and 32 clock cycles.
The signals ton, lon, rsv, rti and ist are standard IEC/IEEE inputs. When using ton or lon no controller action is possible.
The output Ocr or Otrg is HIGH for one clock pulse if DCAS (device clear active state) or DTAS (device trigger active state) is active.

The output Odioc is HIGH when LCS (local state) or LWLS (local with lock-out state) is active.
Output OsrQ is HIGH when the rsv signal is read from the external shift register and the SRDS (request service state) is active. After this request has been answered by a serial poll, OGRS is HIGH in the APRS (affirmative poll response state). The inverted signal on OGRS must be multiplexed to bus-line DIO7, together with the status byte of the other DIO lines, when output Osp is HIGH in the SPAS (serial poll active state).
When the device is in the SPAS state the signal rsv may be removed (can be checked on OGRS).
N.B.: When the interface has asked for service via rsv and is addressed as talker in the serial poll mode, a handshake must be initialized by the device via IrFa.

Input Iacts and output Oact are intended for use of this IC in a controller. When Iacts is HIGH, the source handshake function will exit SIDS and SWS and enter respectively SGNS and SWS. When the controller function is not used, the input Iacts must be connected to VSS. Output Oact is HIGH if the tct message is sent over the interface and the ACDS state is active. A HIGH on input Ipon sets each function to its initial state. This level can be set to LOW after the IC has received 32 clock pulses at stabilized supply voltage.
LIST OF USED ABBREVIATIONS

- A1 to A5: address
- ACDS: acceptor data state
- AFRS: affirmative poll response state
- ATN: attention
- AVD: address valid
- cats: controller active or transfer state
- clr: device clear
- CVD: command valid
- DAC: data accepted
- DAV: data valid
- DCAS: device clear active state
- dcd: don't change data
- DCL: device clear
- DIO: device input/output
- DTAS: device trigger active state
- dvd: data valid device
- EO1: end of output/identify
- GTL: go to local
- IDY: identify
- IFC: interface clear
- ist: individual status
- LLO: local lock-out
- loc: local
- LOCS: local state
- Ion: listen only
- It: decides whether the device can only be listener/talker or listener and talker simultaneously
- LWLS: local with lock-out state
- MLA: my listen address
- MTA: my talk address
- nba: new byte available
- NRFD: not ready for data
- NDAC: not data accepted
- GTA: other talk address
- P1 to P3: parallel response messages
- PCA: parallel poll configure accepted
- pon: power on
- PP: parallel poll message enable
- PPC: parallel poll configure
- PPD: parallel poll disable
- PPE: parallel poll enable
- PPU: parallel poll unconfigure
- rdy: ready for next message
- red: ready for next shift cycle
- REN: remote enable
- RDF: ready for data
- RQS: requested service
- rsr: request for service
- rtl: return to local
- SDC: selected device clear
- SGNS: source generate state
- SIDS: source idle state
- SIWS: source idle wait state
- sp: serial poll
- spaq: serial poll active state
- spd: serial poll disable
- SPE: serial poll enable
- sr: shift register
- SRQ: service request
- SREQ: request service state
- SWNS: source wait for new cycle state
ta: talk active
tct: talk control	on: talk only
trg: trigger
UNL: unlisten

D.C. CHARACTERISTICS

<table>
<thead>
<tr>
<th>VDD V</th>
<th>VIL</th>
<th>VOL</th>
<th>VOH</th>
<th>symbol</th>
<th>-40°C min.</th>
<th>max.</th>
<th>+25°C min.</th>
<th>max.</th>
<th>+85°C min.</th>
<th>max.</th>
</tr>
</thead>
</table>

- Output current:
  - HIGH; see note: 5 mA
  - LOW, see note: 0.4 mA

- Output current for pins: 5 = OPP, 6 = OP3, 7 = OP2, 8 = OP1, 15 = ORFD, 16 = ODAC, 19 = OSRD, 23 = ODAX. These pins can drive one standard TTL load.

Note

Fig. 4 Waveforms showing data exchange in talker function.

Fig. 5 Waveforms showing data exchange in listener function.
The HEF4750V frequency synthesizer is one of a pair of LOCMOS devices, primarily intended for use in high-performance frequency synthesizers, e.g., in all communication, instrumentation, television and broadcast applications. A combination of analogue and digital techniques results in an integrated circuit that enables high performance. The complementary device is the universal divider type HEF4751V.

Together with a standard prescaler, the two LOCMOS integrated circuits offer low-cost single loop synthesizers with full professional performance. Salient features offered (in combination with HEF4751V) are:

- Wide choice of reference frequency using a single crystal.
- System operation to > 1 GHz.
- Typical 15 MHz input at 10 V.
- Flexible programming:
  - frequency offsets
  - ROM compatible
  - fractional channel capability.
- Programme range 6½ decades, including up to 3 decades of prescaler control.
- Division range extension by cascading.
- Built-in phase modulator.
- Fast lock feature.
- Out-of-lock indication.
- Low power dissipation and high noise immunity.

APPLICATION INFORMATION
Some examples of applications for the HEF4750V in combination with the HEF4751V are:

- VHF/UHF mobile radios.
- HF s.s.b. transceivers.
- Airborne and marine communications and nav aids.
- Broadcast transmitters.
- High quality radio and television receivers.
- High performance citizens band equipment.
- Signal generators.

SUPPLY VOLTAGE

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</tr>
</thead>
<tbody>
<tr>
<td>-0.5 to +15</td>
<td>9.5 to 10.5 V</td>
</tr>
</tbody>
</table>
FUNCTIONAL DESCRIPTION

Phase comparator 1

Phase comparator 1 (PC1) is built around a SAMPLE and HOLD circuit. A negative-going transition at the V input causes the hold capacitor \( C_A \) to be discharged and after a specified delay, caused by the

Phase Modulator by means of an internal \( V' \) pulse, it produces a positive-going ramp. A negative going transition at the R input terminates the ramp. Capacitor \( C_A \) holds the voltage that the ramp has attained. Via an internal sampling switch this voltage is transferred to \( C_C \) and in turn buffered and made available at output \( PC_1 \).

If the ramp terminates before an R input is present, an internal end of ramp (EOR) signal is produced. These actions are illustrated in Fig. 3.

Fig. 3 Waveforms associated with PC1.

The resultant phase characteristic is shown in Fig. 4.

PC1 output voltage

\[ V' = \frac{V}{V_R} \]

Fig. 4 Phase characteristic of PC1.

PC1 is designed to have a high gain, typically 3200 V/cycle (at 12.5 kHz). This enables a low noise performance.

Phase comparator 2

Phase comparator 2 (PC2) has a wide range, which enables faster lock times to be achieved than otherwise would be possible. It has a linear \( \pm 360^\circ \) phase range, which corresponds to a gain of typically 5 V/cycle. This digital phase comparator has three stable states:
- reset state
- \( V' \) leads R state
- \( R \) leads \( V' \) state

Conversion from one state to another takes place according to the state diagram of Fig. 5.

Fig. 5 State diagram of PC2.

Output PC2 produces positive or negative-going pulses with variable width; they depend on the phase relationship of R and \( V' \). The average output voltage is a linear function of the phase difference.

Output PC2 remains in the high impedance OFF state in the region in which PC1 operates. The resultant phase characteristic is shown in Fig. 6.
Reference oscillator

The reference oscillator normally operates with an external crystal as shown in Fig. 2. The internal circuitry can be used as a buffer amplifier in cases where an external reference should be required.

Reference divider

The reference divider consists of a binary divider with a programmable division ratio of 1 to 1024 and a prescaler with selectable division ratios of 1, 2, 10, and 100, according to the following tables:

### Binary divider

<table>
<thead>
<tr>
<th>N (A0 to A1)</th>
<th>division ratio</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>1024</td>
</tr>
<tr>
<td>0 &lt; N &lt; 1023</td>
<td>N</td>
</tr>
</tbody>
</table>

### Prescaler

<table>
<thead>
<tr>
<th>programming word (NEO, NS1)</th>
<th>division ratio</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>1</td>
<td>2</td>
</tr>
<tr>
<td>2</td>
<td>10</td>
</tr>
<tr>
<td>3</td>
<td>100</td>
</tr>
</tbody>
</table>

In this way suitable comparison frequencies can be obtained from a range of crystal frequencies. The divider can also be used as a ‘stand alone’ programmable divider by connecting input TRA to VDD, which causes all internal analogue currents to be switched off.

Biasing circuitry

The biasing circuitry uses an external current source or resistor, which has to be connected between the TRA and VSS pins. This circuit supplies all analogue parts of the circuit. Consequently the analogue properties of the device, such as gain, charge currents, speed, power dissipation, impedance levels etc., are mainly determined by the value of the input current at TRA. The TRA input must be decoupled to VDD, as shown in Fig. 7. The value of CDD has to be chosen such that the TRA input is ‘clean’, e.g. 10 nF at RA = 58 kΩ.

---

**Phase modulator**

The phase modulator only uses one external capacitor, Cg, at pin TCB. A negative going transition at the V' input causes Cg to produce a positive-going linear ramp. When the ramp has reached a value almost equal to the modulation input voltage (at MODI), the ramp terminates, Cg discharges and a start signal to the Cg ramp at TCA is produced. A linear phase modulation is reached in this way. If no modulation is required, the MOD-input must be connected to a fixed voltage of a certain positive value up to VDD. Care must be taken that the V' pulse is never smaller than the minimum value to ensure that the external capacitor of PC1 ICa) can be discharged during that time. Since the V' pulse width is directly related to the TCB ramp duration, there is a requirement for the minimum value of this ramp duration.
### RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>$V_{DD}$</th>
<th>$V_{IL}$</th>
<th>$V_{IH}$</th>
<th>$I_{OL}$</th>
<th>$I_{OH}$</th>
<th>$P_{tot}$</th>
<th>$P_{STG}$</th>
<th>$T_{amb}$</th>
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</thead>
<tbody>
<tr>
<td>Supply voltage</td>
<td>$V_{DD}$</td>
<td>-0.5 to +15 V</td>
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<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Voltage on any input</td>
<td>$V_{1}$</td>
<td>-0.5 to $V_{DD}$ +0.5 V</td>
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<td></td>
<td></td>
<td></td>
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</tr>
<tr>
<td>D.C. current into any input or output</td>
<td>$I_{i}$</td>
<td>±1 max.</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>10 mA</td>
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<tr>
<td>Power dissipation per package</td>
<td>$P_{TOT}$</td>
<td>max.</td>
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<td></td>
<td></td>
<td></td>
<td>500 mW</td>
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<tr>
<td>Power dissipation per output</td>
<td>$P_{STG}$</td>
<td>max.</td>
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<td></td>
<td></td>
<td></td>
<td>100 mW</td>
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<tr>
<td>D.C. CHARACTERISTICS at $V_{DD} = 10$ V ± 5%; voltages are referenced to $V_{SS} = 0$ V, unless otherwise specified; for definitions see note 1.</td>
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### Frequency Synthesizer

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<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>$T_{amb}$ (°C)</th>
<th>$V_{OL}$</th>
<th>$V_{OH}$</th>
<th>$I_{OL}$</th>
<th>$I_{OH}$</th>
</tr>
</thead>
<tbody>
<tr>
<td>Output voltage</td>
<td>$V_{OL}$</td>
<td>-0.3 $V_{DD}$</td>
<td></td>
<td></td>
<td>50 mV</td>
<td></td>
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<tr>
<td>HIGH</td>
<td>$V_{OH}$</td>
<td>min. 0.7 $V_{DD}$</td>
<td></td>
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<tr>
<td>Logic output current LOW, at $</td>
<td>I_{O}</td>
<td>&lt; 1$ μA</td>
<td>$V_{OL}$</td>
<td>50 mV</td>
<td>-</td>
<td>50 mV</td>
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<tr>
<td>HIGH</td>
<td>$V_{OH}$</td>
<td>min. $V_{DD}$-50 mV</td>
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<tr>
<td>Logic output current LOW, at $V_{DDL} = 0.5$ V</td>
<td>$I_{OL}$</td>
<td>5.5 -</td>
<td>-</td>
<td>4.6 -</td>
<td>-</td>
<td>3.6 -</td>
</tr>
<tr>
<td>output, $PC_{2}$, OUT</td>
<td>$I_{OL}$</td>
<td>2.8 -</td>
<td>-</td>
<td>2.4 -</td>
<td>-</td>
<td>1.9 -</td>
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<tr>
<td>$V_{EDR}$</td>
<td>$V_{DD}$ - $V_{TCA}$</td>
<td>-0.9</td>
<td>-</td>
<td>0.7</td>
<td>-</td>
<td>0.6</td>
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<tr>
<td>EOR source</td>
<td>$V_{EOR}$</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>-</td>
</tr>
<tr>
<td>$V_{OL}$</td>
<td>$V_{OL}$</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>-</td>
</tr>
<tr>
<td>$V_{OH}$</td>
<td>$V_{OH}$</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>-</td>
</tr>
<tr>
<td>TCA</td>
<td>$IO$</td>
<td>-</td>
<td>-</td>
<td>13</td>
<td>-</td>
<td>-</td>
</tr>
<tr>
<td>TCB</td>
<td>$IO$</td>
<td>-</td>
<td>-</td>
<td>2.5</td>
<td>-</td>
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<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>$T_{amb}$ (°C)</th>
<th>$V_{OL}$</th>
<th>$V_{OH}$</th>
<th>$I_{OL}$</th>
<th>$I_{OH}$</th>
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</thead>
<tbody>
<tr>
<td>Logic output current HIGH; at $V_{OH} = V_{DD}$ -0.5 V</td>
<td>$I_{OH}$</td>
<td>1.5 -</td>
<td>1.3 -</td>
<td>1.0 -</td>
<td>-</td>
<td>mA</td>
</tr>
<tr>
<td>outputs $OL$, $PC_{2}$, OUT</td>
<td>$I_{OH}$</td>
<td>1.4 -</td>
<td>1.2 -</td>
<td>0.9 -</td>
<td>-</td>
<td>mA</td>
</tr>
<tr>
<td>Output TCA sink current</td>
<td>$I_{O}$</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>mA 3.4,5</td>
</tr>
<tr>
<td>Output TCA source current</td>
<td>$I_{O}$</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>mA 3.4,6</td>
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<tr>
<td>Internal resistance of TCC</td>
<td>$R_{I}$</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>kΩ 3.4</td>
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<tr>
<td>[output swing]</td>
<td>$&lt; 200$ mV specified output range:</td>
<td>0.3 $V_{DD}$ to 0.7 $V_{DD}$</td>
<td>$R_{I}$</td>
<td>-</td>
<td>-</td>
<td>-</td>
</tr>
<tr>
<td>Output TCC voltage with respect to TCA input voltage</td>
<td>$\Delta V$</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>V 3.4,7</td>
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<tr>
<td>Output $PC_{2}$ sink current</td>
<td>$I_{O}$</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>mA 3.4,8</td>
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<tr>
<td>Output $PC_{2}$ source current</td>
<td>$I_{O}$</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>mA 3.4,9</td>
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<tr>
<td>Internal resistance of $PC_{2}$ [output swing]</td>
<td>$&lt; 200$ mV specified output range:</td>
<td>0.3 $V_{DD}$ to 0.7 $V_{DD}$</td>
<td>$R_{I}$</td>
<td>-</td>
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</tr>
<tr>
<td>Output $PC_{2}$ voltage with respect to TCC input voltage</td>
<td>$\Delta V$</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>V 3.4,10</td>
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<tr>
<td>EOR generation</td>
<td>$V_{EGR}$</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>V 3.4,11</td>
</tr>
</tbody>
</table>

**Notes:**

1. $T_{amb}$: Ambient temperature
2. $I_{OH}$: Output high current
3. $I_{OL}$: Output low current
4. $V_{OL}$: Output low voltage
5. $V_{OH}$: Output high voltage

**Unit:**

- mA: Milliampere
- kΩ: Kilohm
- V: Volt

**October 1980**
A.C. CHARACTERISTICS

General note

The dynamic specifications are given for the circuit built up with external components as given in Fig. 8, under the following conditions: for definitions see note 1; for definitions of times see Fig. 19:

- $V_{DD} = 10 \pm 5\%$;
- $T_{amb} = 25^\circ C$;
- input transition times $< 20$ ns;
- $R_A = 68$ k$\Omega \pm 30\%$ (see also note 4);
- $C_A = 270$ pF; $C_B = 150$ pF; $C_C = 1$ nF; $C_D = 10$ nF; unless otherwise specified.

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Min.</th>
<th>Typ.</th>
<th>Max.</th>
<th>Unit</th>
<th>Conditions</th>
<th>Notes</th>
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<tbody>
<tr>
<td>Slew rate</td>
<td>$T_{CA}$</td>
<td>52</td>
<td>25</td>
<td>V/µs</td>
<td>$R_A = \text{minimum}$</td>
<td>12</td>
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<tr>
<td></td>
<td>$T_{TCB}$</td>
<td>20</td>
<td>10</td>
<td>V/µs</td>
<td>$R_A = \text{minimum}$</td>
<td>12</td>
</tr>
<tr>
<td>Ramp linearity</td>
<td>$T_{CA}$</td>
<td>2</td>
<td>2</td>
<td>%</td>
<td>$V_{MOD} = 4\ V$</td>
<td>13</td>
</tr>
<tr>
<td></td>
<td>$T_{TCB}$</td>
<td>2</td>
<td>2</td>
<td>%</td>
<td>$V_{MOD} = 6\ V$</td>
<td>13</td>
</tr>
<tr>
<td>Start of TCA ramp delay</td>
<td>$T_{CBA}$</td>
<td>200</td>
<td>200</td>
<td>ns</td>
<td></td>
<td></td>
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<tr>
<td>Delay of TCA hold</td>
<td>$T_{C}$</td>
<td>40</td>
<td>50</td>
<td>ns</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Delay of TCA discharge</td>
<td>$T_{C}$</td>
<td>60</td>
<td>60</td>
<td>ns</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Start of TCB ramp delay</td>
<td>$T_{CB}$</td>
<td>60</td>
<td>60</td>
<td>ns</td>
<td></td>
<td></td>
</tr>
<tr>
<td>TCB-ramp duration</td>
<td>$T_{CB}$</td>
<td>60</td>
<td>60</td>
<td>ns</td>
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<td></td>
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<tr>
<td>Required TCB min.</td>
<td>$T_{CB}$</td>
<td>150</td>
<td>150</td>
<td>ns</td>
<td></td>
<td>14</td>
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<tr>
<td>ramp duration</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Pulse width</td>
<td>$V : \text{LOW}$</td>
<td>20</td>
<td>20</td>
<td>ns</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>$V : \text{HIGH}$</td>
<td>20</td>
<td>20</td>
<td>ns</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>$R : \text{LOW}$</td>
<td>20</td>
<td>20</td>
<td>ns</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>$R : \text{HIGH}$</td>
<td>20</td>
<td>20</td>
<td>ns</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>$STB : \text{LOW}$</td>
<td>20</td>
<td>20</td>
<td>ns</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>$STB : \text{HIGH}$</td>
<td>20</td>
<td>20</td>
<td>ns</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Fall time</td>
<td>$T_{C}$</td>
<td>50</td>
<td>50</td>
<td>ns</td>
<td></td>
<td></td>
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<tr>
<td></td>
<td>$T_{CB}$</td>
<td>50</td>
<td>50</td>
<td>ns</td>
<td></td>
<td></td>
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<tr>
<td>Prescaler input frequency</td>
<td>$FR$</td>
<td>30</td>
<td>30</td>
<td>MHz</td>
<td>all division ratios</td>
<td></td>
</tr>
<tr>
<td>Binary divider frequency</td>
<td>$FDIV$</td>
<td>30</td>
<td>30</td>
<td>MHz</td>
<td>all division ratios</td>
<td></td>
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<tr>
<td>Crystal oscillator frequency</td>
<td>$FOSC$</td>
<td>10</td>
<td>10</td>
<td>MHz</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Average power supply current with speed-up 1:10</td>
<td>$I_P$</td>
<td>3.6</td>
<td>3.6</td>
<td>mA</td>
<td>locked state</td>
<td>15</td>
</tr>
<tr>
<td>Average power supply current without speed-up</td>
<td>$I_P$</td>
<td>3.2</td>
<td>3.2</td>
<td>mA</td>
<td></td>
<td>16</td>
</tr>
</tbody>
</table>

NOTES

1. Definitions:
   - $R_A$ = external biasing resistor between pins TRA and VSS; 68 k$\Omega \pm 30\%$.
   - $C_A$ = external timing capacitor for time/voltage converter, between pins TCA and VSS.
   - $C_B$ = external timing capacitor for phase modulator, between pins TCB and VSS.
   - $C_C$ = external hold capacitor between pins TCC and VSS.
   - $C_D$ = decoupling capacitor between pins TRA and $V_{DD}$.
   - Logic inputs: V, R, STB, A0 to A9, NS0, NS1, OSC.
   - Logic outputs: OL, PC2, XTL, OUT.
   - Analogue signals: TCA, TCB, TCC, TRA, PC1, MOD.

2. TRA at $V_{DD}$; TCA, TCC and MOD at VSS; logic inputs at VSS or $V_{DD}$.

3. All logic inputs at VSS or $V_{DD}$.

4. $R_A$ connected; its value chosen such that $I_{TRA} = 100\ \mu A$.

5. The analogue switch is in the ON position (see Fig. 9).

Fig. 8 Test circuit for measuring a.c. characteristics.

Fig. 9 Equivalent circuit for note 5.
6. The analogue switch is in the ON position (see Fig. 10).

7. This guarantees the d.c. voltage gain, combined with d.c. offset:
   Input condition: \(0.3 \, V_{DD} < V_{TCA} < 0.7 \, V_{DD}\)
   \[\Delta V = V_{TCC} - V_{TCA}\]


9. Equivalent circuit for \(PC_1\) sink current.

10. This guarantees the d.c. voltage gain, combined with d.c. offset:
    Input condition: \(0.3 \, V_{DD} < V_{TCC} < 0.7 \, V_{DD}\)
    \[\Delta V = V_{PC1} - V_{TCC}\]

11. Switching level at TCA, generating an EOR signal, during increasing input voltage.

12. Specified range

13. Definition of the ramp linearity at full swing.

14. The external components and modulation input voltage must be chosen such that this requirement
    will be fulfilled, to ensure that \(CA\) is sufficiently discharged during that time.
NOTES (continued)

15. Circuit connections for power supply current specification, with speed-up 1 : 10. V and R are in the range of PC1, such that the output voltage at PC1 is equal to 5 V.
- \( f_{\text{OSC}} = 5 \text{ MHz (external clock)} \)
- \( f_{\text{STB}} = 12.5 \text{ kHz} \)
- \( f_{\text{V}} = 125 \text{ kHz} \)

Fig. 17 Circuit for note 15.

16. Circuit connections for power supply current specification, without speed-up. V and R are in the range of PC1, such that the output voltage at PC1 is equal to 5 V.
- \( f_{\text{OSC}} = 5 \text{ MHz (external clock)} \)
- \( f_{\text{STB}} = 12.5 \text{ kHz} \)
- \( f_{\text{V}} = 12.5 \text{ kHz} \)

Fig. 18 Circuit for note 16.
(1) Forbidden zone in the locked state for the positive edge of V and R and both edges of STB.

Fig. 19 Waveforms showing times in the locked state.
SP1648
VOLTAGE-CONTROLLED OSCILLATOR

The SP1648 is an emitter-coupled oscillator, constructed on a single monolithic silicon chip. Output levels are compatible with ECL III logic levels. The oscillator requires an external parallel tank circuit consisting of the inductor (L) and capacitor (C). A varactor diode may be incorporated into the tank circuit to provide a voltage variable input for the oscillator (VCO). The device may also be used in phase locked loops and many other applications requiring a fixed or variable frequency clock source of high spectral purity. The SP1648 may be operated from a +5.0V dc supply or a -5.2V dc supply, depending upon system requirements.

Operating temperature range:
-30°C to +85°C (Ceramic)
-6°C to +75°C (Plastic)

<table>
<thead>
<tr>
<th>SUPPLY VOLTAGE</th>
<th>GND PINS</th>
<th>SUPPLY PINS</th>
</tr>
</thead>
<tbody>
<tr>
<td>+5.0V dc</td>
<td>7, 8</td>
<td>1, 14</td>
</tr>
<tr>
<td>-5.2V dc</td>
<td>1, 14</td>
<td>7, 8</td>
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</table>

ORDERING INFORMATION
SP1648DP (Commercial - plastic package)
SP1648DG (Commercial - ceramic package)
SP1648BB DG (Plessey High Reliability Specification)

Fig. 1 Block diagram and pin connections (top view)

Fig. 2 Circuit diagram of SP1648
### ELECTRICAL CHARACTERISTICS

<table>
<thead>
<tr>
<th>Characteristic</th>
<th>Min</th>
<th>Max</th>
<th>Typ</th>
<th>Std</th>
</tr>
</thead>
<tbody>
<tr>
<td>Current (mA)</td>
<td>3</td>
<td>3.4</td>
<td>3.3</td>
<td>3.2</td>
</tr>
<tr>
<td>Voltage (V)</td>
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<td>0.04</td>
<td>0.03</td>
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### TEST VOLTAGE/CURRENT

<table>
<thead>
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<th>Min</th>
<th>Max</th>
<th>Typ</th>
<th>Std</th>
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<td>5.15</td>
<td>5.15</td>
<td>5.15</td>
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<tr>
<td>Input voltage</td>
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<td>4.5</td>
<td>4.5</td>
<td>4.5</td>
</tr>
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</table>
OPERATING CHARACTERISTICS

Fig. 1 illustrates the circuit schematic for the SP1648. The oscillator incorporates positive feedback by coupling the base of transistor TR7 to the collector of TR8. An automatic gain control (AGC) is incorporated to limit the current through the emitter-coupled pair of transistors (TR7 and TR8) and allow optimum frequency response of the oscillator.

In order to maintain the high Q of the oscillator, and provide high spectral purity at the output, a cascode transistor (TR4) is used to translate from the emitter follower (TR5) to the output differential pair TR2 and TR3. TR2 and TR3, in conjunction with output transistor TR1, provide a highly buffered output which produces a square wave. Transistors TR10 through TR14 provide this bias drive for the oscillator and output buffer. Fig. 3 indicates the high spectral purity of the oscillator output (pin 3).

When operating the oscillator in the voltage controlled mode (Fig. 5), it should be noted that the cathode of the varactor diode (D) should be biased at least 2 V above Vcc (=1.4V for positive supply operation).

When the SP1648 is used with a constant dc voltage to the varactor diode, the output frequency will vary slightly because of internal noise. This variation is plotted versus operating frequency in Fig. 6.

Typical transfer characteristics for the oscillator in the voltage controlled mode are shown in Figs. 7, 8 and 9. Figs. 7 and 9 show transfer characteristics employing only the capacitance of the varactor diode (plus the input capacitance of the oscillator, 60fF typical). Fig. 8 illustrates the oscillator operating in a voltage controlled mode with the output frequency range limited. This is achieved by adding a capacitor in parallel with the tank circuit as shown. The 1kΩ resistor in Figs. 7 and 8 is used to protect the varactor diode during testing. It is not necessary as long as the dc input voltage does not cause the diode to become forward biased.

**Fig 5 The SP1648 operating in the voltage-controlled mode**

The larger-valued resistor (5kΩ) in Fig. 9 is required to provide isolation for the high-impedance junctions of the two varactor diodes.

The tuning range of the oscillator in the voltage controlled mode may be calculated as:

\[
\text{fmax} = \frac{C_s}{\sqrt{C_s (\text{max}) + C_s}}
\]

\[
\text{fmin} = \frac{1}{2\pi \sqrt{L (C_s (\text{max}) + C_s)}}
\]

where \( f_{\text{max}} \) is the maximum frequency of oscillation.

- \( C_s \) = shunt capacitance (input plus external capacitance).
- \( C_s \) = varactor capacitance as a function of bias voltage.

Good RF and low-frequency by-passing is necessary on the power supply pins (see Fig. 3).

Capacitors (C1 and C2 of Fig. 5) should be used to bypass the AGC point and the VCO input (varactor diode), guaranteeing only dc levels at these points.

For output frequency operation between 1MHz and 50MHz ± 0.1f Capacitor is sufficient for C1 and C2. At higher frequencies, smaller values of capacitance should be used; at lower frequencies, larger values of capacitance. At higher frequencies the value of bypass capacitors depends directly

**Fig 6 Frequency deviation test circuit**

Note: Any frequency deviation caused by the signal generator and SP1648 power supply should be determined and minimised prior to testing.
upon the physical layout of the system. All bypassing should be as close to the package pins as possible to minimise unwanted lead inductance.

The peak-to-peak swing of the tank circuit is set internally by the AGC circuitry. Since voltage swing of the tank circuit provides the drive for the output buffer, the AGC potential directly affects the output waveform. If it is desired to have a sine wave at the output of the SP1648, a series resistor is tied from the AGC point to the most negative power potential (ground if +5.0V supply is used, -5.2V if a negative supply is used).

At frequencies above 100MHz typ. it may be necessary to increase the tank circuit peak-to-peak voltage in order to maintain a square wave at the output of the SP1648. This is accomplished by attaching a series resistor (1kΩ minimum) from the AGC to the most positive power potential (+5.0V if a +5.0V supply is used, ground if a -5.2V supply is used).
SL6440C
HIGH LEVEL MIXER

The SL6440C is a double balanced mixer intended for use in radio systems up to 100MHz. A special feature of the circuit allows external selection of the DC operating conditions by means of a resistor connected between pin 11 (Bas) and VCC. When biased for a supply current of 50mA the SL6440C offers a 3rd order intermodulation intercept point of typically 30dBm, a value previously unobtainable with integrated circuits. This makes the device suitable for many applications where double ring mixers had previously been used and offers the advantages of a voltage gain, low local oscillator drive requirement and superior isolation.

The SL6440C (in a 16-lead DIL plastic package) is specified for operation from -30°C to +85°C.

FEATURES
- -30dBm Input Intercept Point
- +15dBm Compression Point (1dB)
- Programmable Performance

APPLICATIONS
- Fm and Bw Band Transmitters
- Fm Broadcast Transmitters
- Interferometers
- Meas. Indicators

ABSOLUTE MAXIMUM RATINGS
Supply voltage and output pins: 15V
(Derate above 25°C, 8mW/°C)
Storage temperature range: -60°C to +150°C
Programming current into pin 11: 50mA

PACKAGE THERMAL DATA
Thermal resistance: Junction-Ambient: 125°C/W
Junction-Case: 46°C/W
Time constant: Junction-Ambient: 1.9 mins
Max. chip temperature: 150°C

ELECTRICAL CHARACTERISTICS
Test conditions (unless otherwise stated):
V: 1 12V V: 2 10V L: 25mA 30°C to 85°C (SL6440C)
Local oscillator input level: 0dBm Test circuit Fig. 2

<table>
<thead>
<tr>
<th>Characteristic</th>
<th>Value</th>
<th>Units</th>
<th>Conditions</th>
</tr>
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<tbody>
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<td>150</td>
<td>MHz</td>
</tr>
<tr>
<td>Oscillator frequency 3dB point</td>
<td>100</td>
<td>150</td>
<td>MHz</td>
</tr>
<tr>
<td>3rd order input intercept point</td>
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<td>-</td>
<td>dBm</td>
</tr>
<tr>
<td>Third order intermodulation distortion</td>
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<td>-</td>
<td>dB</td>
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<tr>
<td>Second order intermodulaton distortion</td>
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<td>-</td>
<td>dB</td>
</tr>
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<td>1dB compression point</td>
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<td>dB</td>
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<td>Noise figure</td>
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<td>dB</td>
</tr>
<tr>
<td>Conversion gain</td>
<td>7</td>
<td>-</td>
<td>dB</td>
</tr>
<tr>
<td>Carrier leak to signal input</td>
<td>40</td>
<td>-</td>
<td>dB</td>
</tr>
<tr>
<td>Level of carrier at IF output</td>
<td>-25</td>
<td>-</td>
<td>mV</td>
</tr>
<tr>
<td>Supply current</td>
<td>7</td>
<td>-</td>
<td>mA</td>
</tr>
<tr>
<td>Supply current (total from V: 1 &amp; V: 2)</td>
<td>60</td>
<td>500</td>
<td>mA</td>
</tr>
<tr>
<td>Local oscillator input</td>
<td>250</td>
<td>-</td>
<td>mVrms</td>
</tr>
<tr>
<td>Local oscillator input impedance</td>
<td>1.5</td>
<td>-</td>
<td>kΩ</td>
</tr>
<tr>
<td>Signal input impedance</td>
<td>1000</td>
<td>-</td>
<td>kΩ</td>
</tr>
</tbody>
</table>

NOTE: Supply current in Pin 3 is equal to that in Pin 14 and is equal to 7. See also V: 1 = 2. See also V: 2 1V.
CIRCUIT DESCRIPTION

The SL6440 is a high level mixer designed to have a linear RF performance. The linearity can be programmed using the I, pin (11).

The output pins are open collector outputs so that the conversion gain and output loads can be chosen for the specific application.

Since the outputs are open collector they should be returned to a supply Vcc1 through a load.

The choice of Vcc1 is important since it must be ensured that the voltage on pins 3 and 14 is not low enough to saturate the output transistors and so limit the signal swing.

The voltage on pins 3 and 14 is always greater than Vcc2 the output will not saturate. The output frequency response will reduce as the output transistors near saturation.

Minimum Vcc1, (Iu x RL) - Vcc2

where Iu, programmed current

RL, DC load resistance

Vcc2, max signal swing at output

Iu, the signal swing is not known

Minimum Vcc1, 2(Iu x RL) - Vcc2

In this case the signal will be limiting at the input before the output saturates.

The device has a separate supply (Vcc2) for the oscillator buffer (pin 4).

The current (Iu) programmed into pin 11 can be supplied via a resistor from Vcc1 or from a current source.

The conversion gain is equal to

Gdb = 20 Log Iu + 0.0765

Gdb = 20 Log Iu + 0.0765 for single-ended output

2 RL x Iu for differential output

Device dissipation is calculated using the formula

mW diss = 2 Iu x V0 + V0 x Iu x Vcc2 Diss

where V0: voltage on pin 3 or pin 14

V0: voltage on pin 11

Iu: programming current (mA)

Vcc2 Diss: dissipation obtained from graph (Fig. 5)

As an example Fig. 7 shows typical dissipations assuming Vcc1 and Vcc2 are equal. This may not be the case in practice and the device dissipation will have to be calculated for any particular application.

Fig. 4 shows the intermodulation performance against Iu. The curves are independent of Vcc1 and Vcc2 but if Vcc1 becomes too low the output signal swing cannot be accommodated and, if Vcc2 becomes too low the circuit will not provide enough drive to sink the programmed current. Examples are shown of performance at various supply voltages.

APPLICATIONS

The SL6440 can be used with differential or single-ended inputs and outputs. A balanced input will give better carrier leak. The high input impedance allows step-up transformers to be used if desired whilst high output impedance allows a choice of output impedance and conversion gain.

Fig. 2 shows the simplest application circuit. The input and output are single-ended and Iu is supplied from Vcc1 via a resistor. Increasing RL will increase the conversion gain, care being taken to choose a suitable value for Vcc1.

Fig. 8 shows an application with balanced input, improved carrier leak, and balanced output for increased conversion gain. A lower Vcc1 giving lower device dissipation can be used with this arrangement.

DESIGN PROCEDURE

1. Decide on input configuration using local oscillator data

2. Decide on output configuration and value of conversion gain required.

3. Decide on Vcc1 and Vcc2 using intermodulation and compression point graphs

4. Using values of conversion gain, Vcc2, load and Iu, already chosen, decide on value of Vcc1

5. Calculate device dissipation and decide whether heat sink is required from maximum operating temperature considerations.
The SP8660 is a low power emitter coupled logic counter with an open collector output capable of driving TTL or CMOS. It has internally biased inputs and an open collector.

**FEATURES**
- AC Coupled Inputs
- Low Power Consumption
- Open Collector Output CMOS and TTL Compatible

**QUICK REFERENCE DATA**
- Supply Voltage: 5.0V
- Power Consumption: 50mW
- Temperature Range: -30°C to +70°C
- 8 Lead Plastic Package

**ABSOLUTE MAXIMUM RATINGS**
- Supply Voltage: 8V
- Open Collector Output Voltage: 12V
- Storage Temperature Range: -30°C to +70°C
- Max. Junction Temperature: +175°C
- Output Sink Current: 10mA
- Max. Clock I/P Voltage: 2.5V p-p
### ELECTRICAL CHARACTERISTICS

Supply voltage: Vcc = 5.0V ± 0.25V, Vss = 0V  
Temperature: T = 30°C to 70°C

<table>
<thead>
<tr>
<th>Characteristic</th>
<th>Symbol</th>
<th>Value</th>
<th>Units</th>
<th>Conditions</th>
<th>Notes</th>
</tr>
</thead>
<tbody>
<tr>
<td>Maximum frequency (sinewave input)</td>
<td>Fre</td>
<td>150</td>
<td>MHz</td>
<td>Input = 200-1000mV</td>
<td></td>
</tr>
<tr>
<td>Minimum frequency (sinewave input)</td>
<td>Fm</td>
<td>40</td>
<td>MHz</td>
<td>Input = 400-1000mV</td>
<td></td>
</tr>
<tr>
<td>Power supply current</td>
<td>Is</td>
<td>13</td>
<td>mA</td>
<td>Vcc = 5.25V</td>
<td>k</td>
</tr>
<tr>
<td>Output high voltage</td>
<td>VOH</td>
<td>9</td>
<td>V</td>
<td>Vcc = 5V</td>
<td>Note 4</td>
</tr>
<tr>
<td>Output low voltage</td>
<td>VIL</td>
<td>400</td>
<td>mV</td>
<td>Pin 4 = 1.5kΩ to 10V</td>
<td>Note 4</td>
</tr>
</tbody>
</table>

### OPERATING NOTES

1. The clock inputs (pin 1 and 8) should be capacitively coupled to the signal source. When driven single-ended, the input signal path is completed by connecting a capacitor from the unused input to ground.
2. In the absence of a signal the devices will self-oscillate. This can be prevented by connecting a 3kΩ resistor from either input to ground. If the device is driven single-ended, it is recommended that the pull-down resistor be connected to the decoupled unused input. There will be a loss in sensitivity of approximately 200mV.
3. The device will operate down to DC but the input slew rate must be better than 100V/µs.
4. The open collector output will drive 3 TTL loads, and thus requires a suitable resistor to Vcc to maintain noise immunity. In order to ensure noise immunity, this resistor should not exceed 4.7kΩ. For interfacing to CMOS, the open collector may be returned to a +10V line via a 3.3kΩ resistor. The output sink current must not exceed 10mA, and the use of too low a value of resistor may lead to a loss of noise immunity, especially at low temperatures.
5. Input impedance is a function of frequency. See Fig 4.
6. The rise time of the open collector output waveform is directly proportional to the load capacitance and load resistor value. Therefore, the load capacitance should be minimised and the load resistor kept to a minimum compatible with system power requirements. In the test configuration of Fig 5, the output rise time is approximately 20ns and fall time is 10ns typically.

---

![Fig 3 Typical input characteristics](image1.png)

*Tested as specified above.

![Fig 4 Typical input impedance](image2.png)

Test conditions: Supply voltage 5.0V, ambient temperature 25°C, frequencies in MHz, impedances normalised to 50 ohms

![Fig 5 Test circuit](image3.png)

![Fig 6 Typical application showing interfacing](image4.png)

![Fig 7 Interfacing to TTL Load not to exceed 3 TTL unit loads](image5.png)
### Switching Characteristics

<table>
<thead>
<tr>
<th>Characteristic</th>
<th>Symbol</th>
<th>Min</th>
<th>Max</th>
<th>Typ</th>
<th>Min</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Output Rise Time</td>
<td>t_{rr}</td>
<td>3</td>
<td>5</td>
<td>30</td>
<td>50</td>
<td>80</td>
<td>ns</td>
</tr>
<tr>
<td>Output Fall Time</td>
<td>t_{rf}</td>
<td>9</td>
<td>5</td>
<td>100</td>
<td>50</td>
<td>80</td>
<td>ns</td>
</tr>
<tr>
<td>Output Pulse Width</td>
<td>t_{pp}</td>
<td>5</td>
<td>5</td>
<td>100</td>
<td>50</td>
<td>150</td>
<td>ns</td>
</tr>
<tr>
<td>Phase with t_{pp}</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Input Rise and Fall Time</td>
<td>t_{rise}, t_{fall}</td>
<td>5</td>
<td>3</td>
<td>70</td>
<td>50</td>
<td>120</td>
<td>ns</td>
</tr>
<tr>
<td>Input Pulse Width</td>
<td>t_{ip}</td>
<td>5</td>
<td>5</td>
<td>100</td>
<td>50</td>
<td>150</td>
<td>ns</td>
</tr>
</tbody>
</table>

### Frequency Characteristics

<table>
<thead>
<tr>
<th>Characteristic</th>
<th>Symbol</th>
<th>Min</th>
<th>Max</th>
<th>Typ</th>
<th>Min</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Operating Frequency</td>
<td>f_{osc}</td>
<td>5</td>
<td>3</td>
<td>11</td>
<td>20</td>
<td>32</td>
<td>MHz</td>
</tr>
<tr>
<td>Input + SG Wave 50 Vpp</td>
<td>V_{pp}</td>
<td>5</td>
<td>17</td>
<td>21</td>
<td>14</td>
<td>21</td>
<td>MHz</td>
</tr>
<tr>
<td>Input + Sin Wave 500 mV</td>
<td>V_{pp}</td>
<td>5</td>
<td>17</td>
<td>21</td>
<td>14</td>
<td>21</td>
<td>MHz</td>
</tr>
<tr>
<td>Operating Frequency</td>
<td>f_{osc}</td>
<td>5</td>
<td>3</td>
<td>11</td>
<td>20</td>
<td>32</td>
<td>MHz</td>
</tr>
<tr>
<td>Input + SG Wave 100 Vpp</td>
<td>V_{pp}</td>
<td>5</td>
<td>17</td>
<td>21</td>
<td>14</td>
<td>21</td>
<td>MHz</td>
</tr>
<tr>
<td>Input + Sin Wave 500 mV</td>
<td>V_{pp}</td>
<td>5</td>
<td>17</td>
<td>21</td>
<td>14</td>
<td>21</td>
<td>MHz</td>
</tr>
</tbody>
</table>

### Pin Descriptions

- **f_{y} (Pin 1)** — input to N portion of synthesizer, f_{y} is typically derived from loop VCO and is AC coupled into Pin 9. For larger amplitude signals generated CMOS Logic levels, DC coupling may be used.
- **V_{pp} (Pin 2)** — Circuit Ground
- **V_{DD} (Pin 3)** — Positive power supply
- **P_{DD} (Pin 4)** — Three state output of phase detector for use as loop error signal. Double ended outputs are also available for this purpose (see f_{y} and f_{y}').
- **Frequency f_{y} > f_{y}'** as f_{y} Loading Negative Pulses Frequency f_{y} < f_{y}' or f_{y} Lagging Positive Pulses Frequency f_{y} = f_{y}' and Phase Coincidence High Impedance State

- **RA0, RA1, RA2 (Pins 5, 6, and 7)** — These three inputs establish a code defining one of eight possible divide values for the total reference divider, as defined by the table below.

<table>
<thead>
<tr>
<th>Reference Address</th>
<th>Code</th>
<th>Total Divide Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>RA2</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>RA1</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>RA0</td>
<td>0</td>
<td>2</td>
</tr>
</tbody>
</table>

**OSC_{in}**, **OSC_{out}** (Pins 26 and 27) — These pins form an on-chip reference oscillator when connected to terminals of an external parallel resonant crystal. Frequency setting capacitors of appropriate value must be connected from **OSC_{in}** to ground and **OSC_{out}** to ground. **OSC_{in}** may also serve as input for an externally generated reference signal. This signal will typically be AC coupled to **OSC_{out}**, but for larger amplitude signals generated CMOS Logic levels, DC coupling may be used. In the external reference mode, no connection is required to **OSC_{in}**.

- **LD (Pin 28)** — Lock detector signal. High level when lock is locked (f_{y}, f_{y}' at same phase and frequency). Pulses low when lock is out of lock.
PHASE LOCKED LOOP - LOW PASS FILTER DESIGN

\[ A_1 = \frac{P_{out}}{R_1} \]
\[ A_2 = \frac{P_{in}}{R_1} \]
\[ V_{out} = V_{vco} \]

**Definitions:**
\[ N = \text{Total Division Ratio in Feedback Loop} \]
\[ P_{in} = V_{in} \times R_1 \]
\[ P_{out} = V_{out} \times R_1 \]
\[ V_{vco} = 2\pi f_{vco} \]
\[ f_{vco} = \frac{1}{R_1 C_1} \]

**Note:** Sometimes \( A_1 \) and \( A_2 \) are both used in feedback loop. The value \( f_{vco} \) should be such that the center frequency of the network does not significantly affect any elements.

**Related Phase Locked Loop Frequency Synthesizers**

<table>
<thead>
<tr>
<th>Part Number</th>
<th>Format</th>
<th>Prescaler</th>
<th>Phase Detector</th>
</tr>
</thead>
<tbody>
<tr>
<td>MC145141</td>
<td>4 Bit Digital</td>
<td>Single</td>
<td>3 State</td>
</tr>
<tr>
<td>MC145146</td>
<td>6 Bit Digital</td>
<td>Dual</td>
<td>3 State 2 Output</td>
</tr>
<tr>
<td>MC145148</td>
<td>6 Bit Digital</td>
<td>Dual</td>
<td>3 State 2 Output</td>
</tr>
<tr>
<td>MC145151</td>
<td>Parallel Output</td>
<td>Single</td>
<td>3 State 2 Output</td>
</tr>
<tr>
<td>MC145152</td>
<td>Parallel Output</td>
<td>Dual</td>
<td>3 State 2 Output</td>
</tr>
<tr>
<td>MC145155</td>
<td>Series Output</td>
<td>Single</td>
<td>3 State 2 Output</td>
</tr>
<tr>
<td>MC145156</td>
<td>Series Output</td>
<td>Dual</td>
<td>3 State 2 Output</td>
</tr>
<tr>
<td>MC145167</td>
<td>Series Output</td>
<td>Single</td>
<td>3 State Analog</td>
</tr>
<tr>
<td>MC145159</td>
<td>Series Output</td>
<td>Dual</td>
<td>3 State Analog</td>
</tr>
</tbody>
</table>
MC3440A, MC3441A, MC3443A

QUAD GENERAL PURPOSE INTERFACE
BUS TRANSCIEVERS

The MC3440A, MC3441A, MC3443A are quad bus transceivers intended for use in instruments and programmable calculators equipped for interconnection into complete measurement systems. These transceivers allow the bidirectional flow of digital data and commands between the various instruments. Each of the transceiver versions provides four open-collector drivers and four receivers featuring input hysteresis.

The MC3440A version consists of three drivers controlled by a common Enable input and a single driver without an Enable input. Terminations are provided in the drivers. The MC3441A differ in that all four drivers are controlled by the common Enable input. Again, the terminations are provided. The MC3443A is identical to the MC3441A except that the D4 signaling has been omitted. As such, it is pin-compatible and functionally equivalent to the SN75133. It offers the advantage of reduced input requirements.

- Receiver input hysteresis provides excellent noise rejection
- Open-circuit for dummy output permits wire-OR connection
- Tailored to meet the standards set by the IEEE and IEC Committees on Instrument Interface (488-1978)
- Terminations provided (except MC3443A version)
- Provides Electrical Compatibility with General Purpose Interface Bus

### MAXIMUM RATINGS

<table>
<thead>
<tr>
<th>Parameter / Symbol</th>
<th>Value / Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Supply Voltage (VCC)</td>
<td>5.0 V</td>
</tr>
<tr>
<td>Input Voltage Range</td>
<td>-0.3 V to 5.5 V</td>
</tr>
<tr>
<td>Output Current</td>
<td>10 mA</td>
</tr>
<tr>
<td>Maximum Forward Voltage</td>
<td>60 V</td>
</tr>
<tr>
<td>Maximum Diode Reverse Voltage</td>
<td>60 V</td>
</tr>
<tr>
<td>Maximum Power Dissipation</td>
<td>500 mW</td>
</tr>
</tbody>
</table>

### SWITCHING CHARACTERISTICS

- **High Input Logic State**
  - Typical 
  - Minimum
- **Low Input Logic State**
  - Typical 
  - Minimum

### LATCH-UP CHARACTERISTICS

- **Input/Output Current**
  - Maximum

### ELECTRICAL CHARACTERISTICS

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
</tr>
</thead>
<tbody>
<tr>
<td>Icc</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>VIL</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>VIH</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>VCC</td>
<td>5.0 V</td>
<td></td>
<td></td>
</tr>
<tr>
<td>VILH</td>
<td>0.0 V</td>
<td>0.06 V</td>
<td></td>
</tr>
<tr>
<td>VILL</td>
<td>-1.6 V</td>
<td>-0.3 V</td>
<td>-0.8 V</td>
</tr>
<tr>
<td>VIH</td>
<td>4.2 V</td>
<td>5.0 V</td>
<td></td>
</tr>
<tr>
<td>VIL</td>
<td>-0.3 V</td>
<td>-0.8 V</td>
<td>-1.6 V</td>
</tr>
<tr>
<td>ICC</td>
<td>0.5 mA</td>
<td>10 mA</td>
<td></td>
</tr>
<tr>
<td>ICC</td>
<td>0.5 mA</td>
<td>10 mA</td>
<td></td>
</tr>
<tr>
<td>ICC</td>
<td>0.5 mA</td>
<td>10 mA</td>
<td></td>
</tr>
<tr>
<td>ICC</td>
<td>0.5 mA</td>
<td>10 mA</td>
<td></td>
</tr>
<tr>
<td>ICC</td>
<td>0.5 mA</td>
<td>10 mA</td>
<td></td>
</tr>
</tbody>
</table>

### DRIVER PORTION

- **Input Enable Currents**
  - Maximum

### RECEIVER PORTION

- **Input Impedance**
  - Maximum

### BUS TERMINATION PORTION (Does not apply to MC3443A)

- **Input Voltage (Vil) at 08 V**
  - Typical
  - Minimum
- **Input Voltage (Vih) at 12 mA**
  - Typical
  - Minimum

### POWER SUPPLY CONSUMPTION

- **Typical Dropout Voltage**
  - 0 V

### IMPLEMENTATION - GPIB MEASUREMENT SYSTEM

- **Programmable Delay Time from Driver Input to Low Logic State**
  - Minimum
  - Maximum
- **Programmable Delay Time from Driver Input to High Logic State**
  - Minimum
  - Maximum
- **Programmable Delay Time from Enable Input to Low Logic State**
  - Minimum
  - Maximum
- **Programmable Delay Time from Enable Input to High Logic State**
  - Minimum
  - Maximum

### DRIVER PORTION

- **Programmable Delay Time from Input B to High Logic State**
  - Minimum
  - Maximum

### RECEIVER PORTION

- **Programmable Delay Time from Input A to Low Logic State**
  - Minimum
  - Maximum

For more information, refer to the MC3443A version.
TRIPLE DIODE FOR A.M. RADIOS

Triple silicon planar variable capacitance diode in a plastic envelope.
It is intended for electronic tuning of LW, MW and SW-band of a.m. radio receivers.

<table>
<thead>
<tr>
<th>QUICK REFERENCE DATA</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Each diode</strong></td>
</tr>
<tr>
<td>Continuous reverse voltage</td>
</tr>
<tr>
<td>Forward current (d.c.)</td>
</tr>
<tr>
<td>Junction temperature</td>
</tr>
<tr>
<td>Reverse current at V_R = 32 V</td>
</tr>
<tr>
<td>Diode capacitance at f = 0.5 MHz</td>
</tr>
<tr>
<td>V_R = 1 V</td>
</tr>
<tr>
<td>V_R = 30 V</td>
</tr>
<tr>
<td>Series resistance at f = 0.5 MHz</td>
</tr>
</tbody>
</table>

MECHANICAL DATA
Dimensions in mm
SOT-60

RATINGS Limiting values in accordance with the Absolute Maximum System (IEC134)
These ratings hold for each diode

Voltage
Continuous reverse voltage
V_R max. 32 V
Current
Forward current (d.c.)
I_F max. 50 mA
Temperatures
Storage temperature
T_{stg} -55 to +80 °C
Junction temperature
T_J max. 80 °C

CHARACTERISTICS for each diode
T_{amb} = 25 °C unless otherwise specified
Reverse current
V_R = 32 V
I_R < 50 nA
V_R = 32 V; T_{amb} = 60 °C
I_R < 200 nA
Diode capacitance
V_R = 0.5 V
C_d typ. 290 pF
V_R = 1 V
C_d 230 to 280 pF
V_R = 10 V
C_d > 55 pF
V_R = 20 V
C_d > 16 pF
V_R = 30 V
C_d < 13 pF

Anode = anode capacitance
C_{a1-a2} or C_{a1-a3} or C_{a2-a3}
C_{a-a} typ. 20 fF
Series resistance at f = 0.5 MHz
C_d = 200 pF
r_D < 4 Ω
MATCHING PROPERTIES

The capacitances of the three diodes in their common envelope may differ within certain limits. The total, relative capacitance differences between any two diodes m and n in the triplet (where m and n may be 1, 2 or 3) may be regarded as being built up of a basic part k, and an additional part s.

Basic part

Expressed as a percentage for the reverse voltage range 1 V ≤ V_R ≤ 30 V, k is a constant, obeying the following equation:

\[ k = \left| \frac{C_m - C_n}{C_m} \right| \times 100\% \leq 6\% \]

V_R = 1 V

It may be compensated by means of the coil.

Additional part

Again expressed as a percentage this is a variable difference over the above voltage range:

\[ s = \left| \frac{C_m - C_n}{C_m} \right| \times 100\% - k \]

with the following values:

| [\#1] ≤ 1% at 1 V < V_R ≤ 6 V |
| [\#2] ≤ 2% at 6 V < V_R ≤ 20 V |
| [\#3] ≤ 3% at 20 V < V_R ≤ 30 V |

The shaded area represents the maximum possible deviation in capacitance at k_max for any two individual diodes in one envelope versus reverse voltage.
delft hydraulics
consultancy & research