A Quiet Digitally Assisted Auto-Zero-Stabilized Voltage Buffer with 0.6pA Input Current and 0.6μV Offset

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3.1 A Quiet Digitally Assisted Auto-Zero-Stabilized Voltage Buffer with 0.6pA Input Current and 0.6pV Offset

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The readout of high impedance sensors and sampled voltage references [1] requires amplifiers with both low offset and low input current. Chopper amplifiers can achieve low offset, but the switching of their input chopper gives rise to significant input current (40 to 110pA) [2-4]. Auto-zero (AZ) amplifiers require less input switching, but exhibit more voltage noise. However, ping-pong amplifiers continuously swap two auto-zeroed input stages, leading to more switching [5,7]. In this work, an AZ stabilized topology is proposed, in which a single amplifier is always present in the signal path. Only one input switch is required, resulting in an input current of 0.6pA (max), a 66× improvement on the state-of-the-art [4]. Furthermore, a digitally assisted offset-reduction scheme reduces its low-frequency (LF) noise to the theoretical $\sqrt{5}$× limit. It also achieves a state-of-the-art maximum offset of 0.6pV.

The AZ stabilized amplifier is shown in Fig. 3.1.1. It consists of a 3-stage unity-gain buffer (BUF), whose offset ($V_{os}$) and 1/f noise are cancelled by an AZ stabilization loop, which consists of an integrator (INT) and two OTAs: AZ1 and AZ3. During phase $\phi_1$, AZ1 is auto-zeroed. Its input is shorted and the resulting output current is integrated on capacitors $C_{11-12}$ (10pF each). AZ2 then converts the result into a current that cancels $V_{os}$. The corresponding correction voltage $V_{p}$ is stored on the input capacitors $C_{21-22}$ (5pF each) of AZ2. During phase $\phi_2$, AZ1 senses the buffer’s offset, which, due to feedback, appears between its inputs. The output current of AZ1 is then integrated on capacitors $C_{11-12}$ (10pF each), thus generating, via AZ3, an appropriate cancellation current. The corresponding correction voltage $V_{os}$ is stored on the input capacitors $C_{21-22}$ (5pF each) of AZ2. To achieve $\mu$V-level offset, each stabilization loop should have $\leq$120pB gain. This is achieved by a single gain-boosted integrator amplifier (INT), which is multiplexed between the two loops.

The main drawback of auto-zeroing is increased LF noise due to the fold-back of wideband thermal noise. In the chosen topology, the LF voltage-noise spectral density is theoretically limited to $\sqrt{5}V_{n}$, where $V_{n}$ is the thermal noise density of $C_{11}$. The thermal noise density of an AZ and BUF (Fig. 3.1.2). This can be understood as follows. During one AZ cycle, AZ1 first auto-zero itself before auto-zeroing BUF, thus contributing $V_{os}$ to the total LF noise. Adding the contribution of BUF, this leads to a total of $\sqrt{5}V_{n}$. However, after AZ1 auto-zeroes itself, its sampled noise is stored by $C_{21-22}$ and so reaches the output in both AZ phases. This means that its contribution to the total LF noise is correlated, leading to a minimum LF noise density of $\sqrt{5}V_{n}$.

To reduce noise folding, the ratio between the AZ loop bandwidth (BW$_{AZ}$) and the auto-zeroing frequency $f_{az}$ should be minimized. Reducing the former is preferable, since increasing $f_{az}$ increases the rate of switching spikes, and hence, input current. This requires either large integration capacitors or a large ratio between the transconductances of AZ1 & BUF and AZ2 & AZ3, respectively. Simulations show that a ratio of about 500× is required to reach the $\sqrt{5}$× limit (Fig. 3.1.2). However, this limits the offset correction range of each loop to $\pm 500\mu$V. In order to handle the expected mV-range, a digitally assisted coarse/fine channel and body-diodes of SW$_{2}$ are operated at zero reverse bias. The same technique is applied to AZ1’s input switches SW$_{4-6}$, as their leakage will otherwise discharge $C_{11-12}$ and cause CM transients. The S&H switches SW$_{3}$ are simultaneously closed to sample the external voltage and opened to start the hold phase. The voltage drift across $C_{11}$ is then an accurate measure of the buffer’s input current, avoiding the need for low-leakage bootstrapped ESD diodes.

The digitally-assisted AZ stabilized voltage buffer was realized in a 0.18μm CMOS process (Fig. 3.1.7). It has an active area of 0.55mm$^2$, 0.12mm$^2$ of which is taken by the S&H circuit and draws 210μA from a 1.8V supply. With a 1V input and $f_{az} = 15$kHz, measurements show that its input current is below 0.6pA (15 samples), and that its offset does not exceed 0.6μV (Fig. 3.1.4). In Fig. 3.1.5, the buffer’s voltage noise spectral density is shown. Over BW$_{AZ}$ a LF noise density of 29nV/√Hz is achieved, which equals the $\sqrt{5}$× noise limit. No tones at $f_{az}$ can be seen, demonstrating the effectiveness of the spike reduction techniques. The voltage drift across $C_{11}$ is also shown (typical sample, 1V input). With AZ off, there is negligible leakage, illustrating the effectiveness of the low-leakage techniques. With $AZ$ on, the variation in input current over the buffer’s input range (0.1 to 13V) indicates that it is indeed mainly due to the charge injection of SW$_{2}$. In Fig. 3.1.6 the performance of the auto-zeroed voltage buffer is summarized and compared with the state-of-the-art. It achieves 66× less input current (0.6pA), as well as state-of-the-art offset (0.6μV) and competitive LF voltage noise ($29nV/\sqrt{Hz}$).

References:
Figure 3.1.1: Block diagram of an auto-zero stabilized voltage buffer.

Figure 3.1.2: Simulated voltage noise density for different transconductance ($g_m$) ratios of AZ1 & BUF and AZ2 & AZ3, respectively (50x, 100x, 250x and 500x).

Figure 3.1.3: Block and timing diagram of the digitally-assisted auto-zero stabilized voltage buffer.

Figure 3.1.4: Histograms (15 samples) of the measured offset (without and with AZ) and input current ($f_{AZ} = 15$ kHz, $V_{in} = 1$V).

Figure 3.1.5: Measured voltage noise density: with and without AZ (Top left). The input current ($I_{in}$) vs the input voltage for a typical sample (Top right). The capacitor voltage drift of a typical sample with and without AZ (Bottom).

Figure 3.1.6: Performance summary and comparison with previous works.
Figure 3.1.7: Die micrograph.