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31.4 A -91dB THD+N Resistor-Less Class-D Piezoelectric Speaker Driver Using a Dual Voltage/Current Feedback for LC Resonance Damping

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Piezoelectric speakers are gaining popularity on account of their improving form-factor and audio quality, making them a good fit for many audio applications such as in televisions, laptops, etc. Such speakers can be modelled as a large capacitive load, and so are typically driven by a Class-A amplifier via a series resistor that ensures driver stability, and limits load current, but wastes power [1,2]. In [3], the Class-A amplifier is replaced by a more power-efficient Class-D amplifier (CDA) in series with an additional inductor. However, a series resistor is still required to damp the resulting LC resonant circuit, which could otherwise draw excessive currents when excited by large-signal distortion (e.g. clipping) harmonics around the LC resonance frequency. Alternatively, by using a feed-forward architecture based on LC filter diagnostics to limit overshoot currents, the series resistor can be replaced by a second inductor, at the expense of increased system complexity and cost [4].

This paper describes a resistor-less Class-D piezoelectric speaker driver that only requires a single inductor. LC resonance is damped by a dual-voltage/current feedback architecture, which is enabled by an on-chip current-sensing scheme. Furthermore, the use of a push-pull (PP) modulation scheme minimizes the amplifier's idle power consumption. Finally, chopping is implemented to improve linearity and PSRR across output power levels. The amplifier can drive load capacitances up to 4μF at full scale output power levels. The amplifier can drive load capacitances up to 4μF at full scale output power levels. The amplifier can drive load capacitances up to 4μF at full scale output power levels.

Figure 31.4.1 shows a simplified system block diagram of the proposed driver. In addition to a voltage-feedback (VFB) path, a parallel current-feedback (CFB) path is implemented to increase the output power of the CDA around the LC resonance frequency (fLC), thus achieving damping without the power penalty of a series resistor. The output load current ρd,SC (= IN,SC – ρd,CM) is sensed via a single sense resistor Rs, and thus the effective feedback factor of the CFB, βCFB = VDH – VCM/VCM, is Rs/Rd,CM, where VCM is the load impedance seen at the switching output node (VCM), and K is a CFB gain factor. The combination of the two feedback paths results in an overall feedback factor (βtotal) with a peak around fLC and a fixed gain (normalized to unity) at other frequencies. This causes a notch in the CDA's closed-loop transfer function (VCM/VDC) that increases its output impedance around fLC, and thus damps LC resonance. Since the notch is created by the LC impedance itself, it is insensitive to LC tolerance and aging. As shown in Fig. 31.4.1, increasing K results in more damping, but also increases the CFB gain in the audio band, and thus increases the effect of CFB nonlinearity. Further away from fLC, the highly linear VFB dominates and determines the CDA's unity-gain frequency. In this work, K is made programmable.

Load-current sensing is achieved by sensing the IR drop across two on-chip sense resistors Rs,pp (20mΩ) in the H-bridge, as shown in Fig. 31.4.2. In a PP modulation scheme, only one side of the H-bridge switches, depending on the polarity of the audio signal, while the other side is grounded via a non-switching low-side device (M1,pp) and Rs,pp. This single-sided switching scheme reduces switching losses by half, and significantly reduces the ripple current during idle operation since the pulse width would theoretically approach zero [5]. It also enables the use of a single readout amplifier to provide a quasi-continuous measure of fLC by switching its input between the two sense resistors depending on the polarity of the audio signal (20Hz to 20kHz).

Compared to off-chip resistors, on-chip resistors offer a more compact and low-cost current-sensing solution. However, they have nonlinear IV characteristics, which worsen at high load currents, due to the combination of their temperature dependence and self-heating. To mitigate these effects, the CFB path is established via the virtual ground of the 2nd integrator (Fig. 31.4.2), ensuring that the CFB nonlinearity and noise are suppressed by the gain of the 1st integrator. Inserting a low-pass filter (fLP = 1/(2πRC) ~ 40kHz) in the CFB path results in a flat CFB gain (K) (referred to the CDA input) above 40kHz, thus allowing some flexibility in setting fLC (= 40kHz). While increasing fLC would further suppress CFB non-linearity, it would also require a higher fLP, and therefore a smaller L for a certain C, resulting in larger ripple currents and power loss. Rs,pp are implemented with diffusion resistors, since they are less susceptible to aging than poly resistors, and they also exhibit less temperature dependence than metal resistors.

As illustrated in Fig. 31.4.3, the PWM signals for a PP-modulated output stage H-bridge are generated by comparing the differential output of the loop filter (LFTD,pp) with two 180° phase-shifted triangular carriers (VTR,D,pp). When LFTD,pp is lower than both VTR,D,pp and VSW,pp=14.4V, when LFTD,pp is higher than both VTR,D,pp and VSW,pp=14.4V, and finally VSW,pp=0V. Since the single-sided switching operation creates large CM content at VCM, mismatch in RF,pp or CMRR in the 1st integrator can cause significant distortion, especially for large signals [5]. To mitigate mismatch, Rs,pp are chosen. Switching nonidealities are reduced by ensuring that the chopping transitions occur when both VCM,pp are grounded, such that CMV only switches near-zero signals. To minimize the CM-to-DM leakage due to the finite CMRR of the 1st integrator, a CM regulator is used to fix the virtual ground CM voltage (VCM,pp,CM) to a DC value (~1.1V). In-band CM-to-DM leakage due to the mismatch of RF,pp and CM8=1.2 in the CM regulator is also removed by chopping.

This 3rd-order CFF loop filter, based on active-RC integrators, is used to create high loop gain around the output stage. Besides Rk (20kΩ) and OTK, RCM8=1.2 also contribute noise and are set to 25kΩ as a trade-off between noise and the output swing of the CM regulation amplifier. The closed-loop gain of the CDA is set by RF,R/RE (= 8). An oscillator, based on an active-RC integrator, generates both VTR,D,pp (1MHz, thus 2MHz in feedback), and the chopping clock (fCH = 125kHz). The edges of the latter are aligned with the peaks of VCM,pp to ensure that the chopping transitions occur when both VCM,pp are grounded. All RC networks are made 2-bit trimmable to account for process spread, and share the same trim code. Core LV devices (1.8V) are used for CHN and CHN, whereas HV LDMS devices are used for CHN [6].

The prototype IC, shown in Fig. 31.4.7, was fabricated in a 0.18μm BCD process and occupies 7mm². Powered from 14.4V / 1.8V supplies (PDC, VDD Đi), it drives a 4μF capacitor via a series 1.1μH inductor (fL = ~75kHz). The amplifier draws 8.5mA / 5mA from PDC, 7.5mA / 2mA from VDD Đi in idle/active operation. Figure 31.4.4 (Top) shows the THD+N across input frequency for an output voltage VCM = 5Vpp with CFB gain K=1.25/2.5 respectively. Across output amplitude (Fig. 31.4.4 Bottom), the THD+N peaks at ~87.3dB / 89.5dB for 1kHz and 6kHz inputs for K= 1.25 / 2.5, respectively. Figure 31.4.5 (Top-Left) demonstrates the efficacy of the CFB by comparing the measured system STF (normalized to a unity gain), with a simulated STF (parameters extracted from LC impedance measurement) with the same LC filter used in the measurements. The STF peaking is reduced by 20dB and 22dB for K= 2.5 respectively. Figure 31.4.5 (Bottom-Left) shows the amplifier’s power consumption across output amplitude while driving G = 4μF. The amplifier consumes 4.9W for a 4.4Apeak load current, which is dominated by the conduction and switching losses of the output stage. To emulate the same damping using a conventional CDA, a resistor (0.2Ω and 0.35Ω corresponding to K=1.25 and 2.5, respectively) would then need to be connected in series with C. A power saving of about 1.9W and 3.5W is achieved with K=1.25 and 2.5 respectively. As anticipated, the choice of K is a trade-off between the amount of damping, thus power saving, and large-signal linearity. Figure 31.4.5 (Top-Right) shows the measured PSRR when PDC is perturbed by a Vpp sine wave.

Figure 31.4.6 summarizes the performance of the proposed piezoelectric driver and compares it with the state of the art. Thanks to the dual voltage/current feedback architecture, it is the only piezoelectric driver capable of damping LC resonance without a series resistance or any foreground calibration, and it offers a very compact load configuration (1L + C). The CDA can deliver -4.4Apeak, 1.5x higher than [1] and 3x higher than [2,3]. Compared to [4], it achieves a 3.7x better THD+N for 1kHz input signal, a 3.6x reduction in idle power consumption, and 3.9x lower power consumption for large load current (3.5Apeak). Moreover, it achieves competitive DR, output noise, and PSRR.

References:
Figure 31.4.1: Simplified block diagram of the proposed dual voltage/current feedback piezoelectric speaker driver (Top); and the effect of CFB on the LC resonance and forward-path STF (Bottom).

Figure 31.4.2: Simplified schematic of the CFB network (Top-Left); corresponding waveforms of signals (Right); and effective input-referred CFB gain K (Bottom-Left).

Figure 31.4.3: Simplified schematic of the CDA with chopper network and virtual ground CM regulation (Top), and corresponding waveforms of PP modulator and chopper signals (Bottom).

Figure 31.4.4: Measured performance of the CDA for $P_{ \text{VDD} } = 14.4 \text{V}$ and $C_L = 4 \mu \text{F}$: THD+N across $f_\text{IN}$ for $V_O = 5 \text{V}_{\text{RMS}}$ (Top), and THD+N across output amplitude (Bottom).

Figure 31.4.5: Effect of CFB on LC resonance (Top-Left); PSRR of the CDA [4 samples] (Top-Right); power consumption vs $V_O$ for $C_L = 4 \mu \text{F}$ and $f_{\text{IN}} = 10 \text{kHz}$ and 12kHz (Bottom).

Figure 31.4.6: Performance summary and comparison with existing state-of-the-art piezoelectric speaker drivers.
Figure 31.4.7: Die micrograph of the CDA.