Energy-Efficient Capacitive-Sensor Interface Based on an Incremental Delta-Sigma Modulator Employing Current-Starved Inverter-Based OTAs

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Abstract

An interface circuit for a fully-integrated capacitive humidity-sensor is implemented using 0.16μm standard CMOS technology. This interface circuit is intended to be used in a smart RFID sensor platform. This thesis focuses on improving the energy-efficiency of the interface circuit. A third-order incremental delta-sigma converter based on switched-capacitor integrators is presented. Due to the fact that the operational trans-conductance amplifier (OTA), as a major building block for an integrator, consumes most of the power in the whole interface circuit, this work mainly concentrates on improving the energy-efficiency of the OTAs in the three integrators. A fully-differential current-starved inverter-based OTA structure is proposed for the integrator. A dynamic power-down scenario is applied to reduce the power consumption by approximately 20%. Detailed analysis and design optimizations are also provided. The interface achieves 13-bit capacitance-to-digital conversion while consuming 6.8μW from a 1.2V supply, resulting in a figure-of-merit (F.o.M) around 0.17pJ/Step. The circuit design and layout of a test chip are presented. Simulation results confirm the expected improvement in energy-efficiency.

Key words: RFID, humidity-sensors, delta-sigma modulators, switched-capacitor circuits, operational trans-conductance amplifiers, power-down techniques, energy-efficiency, standard CMOS technology.
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Chapter 1

Introduction

Recently, radio-frequency identification (RFID) is widely used in a large number of applications including supply chain management, access control, public transportation and food-quality monitoring. Meanwhile, sensor systems are prevalent and commonly applied in every single corner of our daily life. Combining sensory systems such as temperature, humidity, pressure and pH with RFID opens up many new applications which make our life easier and better. To bring these applications into the market, sensors with low-power consumption are essential, which help extend the lifetime of batteries and consequently reduce the cost. Within a sensor, the interface circuit is a major block and consumes considerable power. Thus, how to reduce power consumption in interfaces is a primary problem that needs to be addressed. This thesis describes the design of a capacitive-sensor interface tailored to the specifications of a CMOS compatible humidity-sensor that achieves 13-bit capacitance-to-digital conversion while consuming 6.8μW from a 1.2V supply, resulting in a figure-of-merit (F.o.M) of 0.17pJ/Step. Together with the humidity sensor, this interface forms a smart humidity sensor tailored for RFID applications.

In this introductory chapter, the backgrounds of the RFID smart humidity sensor are explained, followed by the motivation and objectives of this work and the basic operating principles of CMOS smart humidity sensors. A set of requirements for the capacitive-sensor interface is drawn based on the humidity-sensor specifications. This is followed by a description of the research context consisting of a brief review of the state-of-the-art. The challenge to be addressed is then described, i.e. to improve the energy-efficiency while maintaining performance. Finally, the structure of the rest of the thesis is introduced.

1.1 RFID with Smart Humidity Sensor

RFID merged with fully-integrated smart sensors (including temperature, relative humidity, pH etc.) is a newly-raised subject that opens up many attractive applications. An RFID label equipped with a smart humidity-sensor can be applied into food quality tracing and instant condition monitoring. This can effectively prevent food spoilage and save enormous amounts of money.

1.1.1 Backgrounds

Radio-Frequency identification (RFID) is a technology that uses communication via
electromagnetic waves to exchange data between a terminal and an object such as a product, animal, or person for the purpose of identification and tracking. It invariably involves interrogators (also known as readers) and tags (also known as labels). Most RFID tags contain at least two parts. One is an integrated circuit for storing and processing information, modulating and demodulating a radio-frequency (RF) signal, and other specialized functions. The other is an antenna for receiving and transmitting the signal [1].

A humidity sensor, also called hygrometer, measures and regularly reports the relative humidity in the air. Nowadays, an increasing number of humidity sensors are fabricated using integrated circuit (IC) technology and directly produce a digitized output value, forming what we called smart sensors [2, 3], in order to make the sensor system more compact and economical.

1.1.2 Motivation and Objectives

With the increasing mass-production capability on food, people have to face the fact that lots of food is spoiled half-way and thrown away. A 2004 University of Arizona study reveals that Americans squander some $42 billion annually on spoiled food. Lead researcher Timothy Jones reported that, on average, U.S. households discarded 14 percent of their food purchases. It is estimated that a family of four tosses out up to $590 per year worth of meat, fruits, vegetables and grain products alone [4].

In order to reduce food spoilage and prevent this grim wastage, an increasing attention for food safety is probably the most critical and inevitable challenge that the food industry will have to face in the coming years. Food tracing is, indeed, one of the main instruments to guarantee the quality of the products [5]. Adding sensing functionality to RFID tags opens up many new applications, such as tracking and monitoring the conditions of perishable products throughout the logistics chain [6, 7]. RFID tags equipped with sensors can provide valuable information about the transportation and storage conditions of such products (including temperature, CO₂, relative humidity etc.), which can be used to better predict expiry-date dynamically and thus significantly reduce loss due to spoilage. Relative humidity, as one of the key factors of perishable products, should be detected anyway.

Given such an urgent demand and large market, it makes sense to try to fabricate smart humidity sensors into RFID tags. During the past few years, this application has given a considerable boost to the development of smart RFID labels, capable of storing the data concerning the product, monitoring the environmental conditions, and transmitting the collected information upon request.

The PASTEUR project, a European collaboration in context of the Catene framework, targets the development of a wireless sensor platform for monitoring of perishables based on RFID technology. The final goal of this project is to develop a smart RFID
A data logger for cool chains and perishable goods. An impression of such a device is shown in Figure 1.1 below [8].

![Impression of the PASTEUR project product.](image)

A first prototype of the sensor-enabled RFID label will be capable of detecting temperature and relative humidity. NXP Research develops CMOS-compatible sensors in their 0.16\(\mu\)m CMOS process (C14) and provides system integration. The Electronic Instrumentation (EI) lab at Delft University of Technology designs the required smart temperature sensor and smart humidity-sensor.

Smart RFID labels, however, are only economically viable if the sensors and associated electronics can be produced in a low-cost, mass-production technology. Moreover, the limited amount of energy available in RFID labels lays critical requirements on the energy consumption of the attached sensor systems, such as stable operation at very low current level (less than 10\(\mu\)A) and energy level (less than 1\(\mu\)J per measurement), in order to prolong the lifetime of the battery in RFID labels and consequently lower the cost. Besides, they should directly present easily-readable digital outputs corresponding to the detected physical factors.

Typically the radio would be dominant in terms of power consumption, but here communication is passively done on a carrier provided by the reader. The battery assisted passive (BAP) tag has a small battery on board that provides power to process and record sensor data at regular time intervals, even if the tag is not in the proximity of an RFID reader. Thus, within this kind of smart RFID label, the interface circuit is the most power-hungry element compared to the radio and the sensing element, and its functionality determines the displayed output. Therefore, low-power interface circuits are of great importance and deserve substantial attention. However, current humidity-sensor interfaces either use discrete components [6, 7], or only provide a voltage output [9], or consume too much energy [9, 10]. Some attractive interfaces consuming very little power are competent for energy consumption requirements [11], but they are not targeted at this application. What’s more, their energy-efficiency can be further improved by means of novel design.

This thesis presents dedicated effort on improving the energy-efficiency of a sensor
interface designated for a CMOS-compatible smart humidity sensor. With this design
aiming at further improvements in energy-efficiency of capacitance-to-digital
converters, smart RFID labels with humidity sensors will be more feasible in the
market and the mentioned benefits can be brought into effect in that wide range of
applications.

1.1.3 Basic Principles

Generally speaking, capacitive humidity sensing is the most widely used technique for
humidity-sensors, where the relative humidity (RH) change is detected by a
humidity-induced dielectric constant change of thin films. The most widely used
materials as humidity-sensitive dielectrics are polyimide films, as they provide high
sensitivity, linear response, low response time, and low power consumption [12]-[15].
The advantages of capacitive humidity sensors include a high energy-efficiency, as in
principle no static power is consumed, and compatibility with standard IC fabrication
technologies, as the humidity-sensing capacitor can be implemented in the top metal
layer on silicon. A capacitive humidity-sensor consisting of a polyimide capacitor
fabricated on a silicon substrate is shown in Figure 1.2 [8].

![Diagram of a capacitive humidity-sensor.](image)

The capacitance value is expressed theoretically as below

\[
C_x = \varepsilon_x \cdot \frac{A}{d} = C_o (1 + S_d H) \tag{1.1}
\]

where

- \(C_x\) sensing capacitor value
- \(C_o\) offset capacitance
- \(\varepsilon_x\) humidity-sensitive dielectric constant
- \(A\) the effective area
- \(d\) the distance between two metal layers
- \(S_d\) “dielectric sensitivity” of the sensor
- \(H\) relative humidity for detection
A compact and energy-efficient readout circuit producing a precise digital representation of $C_m$, known as a capacitance-to-digital converter, is required to form a smart humidity sensor. To implement this fully-integrated capacitive humidity sensor, the humidity-sensitive capacitor employs a structure of meander-fork electrodes in the top metal layer, topped with a humidity-sensitive dielectric layer, and the interface circuit is integrated underneath with a shielding layer of Metal 4 in-between [16].

1.2 Design Requirements

The goal of this master thesis is to design an energy-efficient smart interface circuit for capacitive humidity-sensors. The humidity-sensor specifications are shown in Table 1.1, as well as its equivalent circuit in Figure 1.3.

![Figure 1.3: Equivalent circuit.](image)

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Nominal capacitance $C_m$ (50%RH)</td>
<td>1.8 pF*</td>
</tr>
<tr>
<td>Minimum capacitance $C_m$ (30% RH)</td>
<td>1.6 pF*</td>
</tr>
<tr>
<td>Maximum capacitance $C_m$ (95% RH)</td>
<td>2.25 pF*</td>
</tr>
<tr>
<td>Linearity (20-90% RH)</td>
<td>0.9901</td>
</tr>
<tr>
<td>Sensitivity</td>
<td>0.01 pF/%RH</td>
</tr>
<tr>
<td>Temp. coefficient</td>
<td>0.00105 pF/°C</td>
</tr>
<tr>
<td>Parasitic capacitances ($C_{p1}, C_{p2}$)</td>
<td>&lt; 0.3 pF</td>
</tr>
<tr>
<td>Shunt resistance $R_{sh}$</td>
<td>&gt;1G ohm</td>
</tr>
</tbody>
</table>

* These values are measured with respect to ground, therefore including $C_{p1}$ and $C_{p2}$. The device-to-device variation is within 10% on the median value.

The interface circuit to be designed is a capacitance-to-digital converter (no analog output), which should consume quite a small amount of energy for each conversion. A set of requirements are listed in Table 1.2, in line with the specifications of the humidity-sensor. A resolution of 0.1% RH is desired for this smart humidity-sensor, which can be translated into a resolution requirement for the interface as below:
where \( full-scale \) is the whole input range of the sensing capacitor, \( N \) is the resolution of the interface. Usually the whole input range is set larger than the maximum capacitance variation in order to provide a region with high linearity and no distortion due to overloading. A conservative \( full-scale \) of \( 1pF \) is assumed, while the capacitance variation is \( 0.48pF \), the resolution for the interface is required as:

\[
N \geq \log_2 \left( \frac{1pF}{0.1 \cdot 0.01pF} \right) \approx 10\text{(bits)}
\]  

In principle 10-bit is adequate for this humidity-sensor, but a target of 13-bit is set to build a standard interface platform in the future and to accommodate process tolerances and temperature cross-sensitivity, which increase the range of capacitances that the interface has to be able to handle.

### Table 1.2: Target specifications for the interface circuit

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Requirement</th>
</tr>
</thead>
<tbody>
<tr>
<td>Energy/conversion</td>
<td>&lt; 1( \mu )J</td>
</tr>
<tr>
<td>Conversion time</td>
<td>&lt; 10ms</td>
</tr>
<tr>
<td>Resolution</td>
<td>13 bits</td>
</tr>
<tr>
<td>Linearity</td>
<td>?</td>
</tr>
<tr>
<td>Supply voltage range</td>
<td>1.2V ~ 1.8V</td>
</tr>
<tr>
<td>Peak supply current</td>
<td>&lt; 100 ( \mu )A</td>
</tr>
<tr>
<td>Shutdown current</td>
<td>&lt; 10nA</td>
</tr>
<tr>
<td>Process</td>
<td>0.16( \mu )m CMOS</td>
</tr>
<tr>
<td>Die area</td>
<td>&lt; 0.3 mm(^2)</td>
</tr>
</tbody>
</table>

#### 1.3 Context of the Research

A capacitance-to-digital converter (CDC) can be regarded as a specialized analog-to-digital converter (ADC), where the analog input signals are capacitance. The operating principles and characteristics of various kinds of ADCs have been discussed in detail in [17], and some performance comparisons have been summarized. Numerous architectures have been developed, which can be classified in many ways. Among these classifications, one is based on the bandwidth, resolution and power-consumption requirements of different applications [18], which is quite helpful to guide the design choice. Nyquist ADCs can not achieve high-resolution due to their critical reliance on matching of analog circuits. Oversampled ADCs trade speed for accuracy, which is quite suitable for DC or narrow-band signals. Delta-sigma ADCs, as one special kind of oversampled ADCs, only use simple analog blocks to achieve high accuracy. They are characterized with high tolerance on process variation and environmental effects, as well as low area- and power-consumption. Conclusively
speaking, delta-sigma conversion is a good candidate for high-resolution conversion of narrow-band input signals in a mixed-signal environment.

Currently, delta-sigma conversion is applied in an increasingly number of interfaces because of its advantages on low-power consumption and high tolerance on non-idealities (switching-noise interference, elements mismatch, etc.). A performance summary on state-of-the-art capacitive-sensor interfaces employing delta-sigma conversion is shown in Table 1.1, along with preliminary target specifications. The reported Figure-of-Merit (F.o.M) is derived from the well-known expression evaluating general purpose ADCs, which is described as below:

$$ F.o.M = \frac{Power_{total} \times T_{measurement}}{2^{ENOB}} \quad (1.4) $$

Table 1.3 reveals the evidence that there is still a gap between the prior art of delta-sigma conversion based interfaces designated for capacitive sensors and the target in this work. Lots of preliminary work for this project has been done by Zhichao Tan, a PhD candidate of EI lab at TU Delft. This thesis represents another step forward and improves the energy-efficiency of the capacitive humidity-sensor interface.

<table>
<thead>
<tr>
<th>TABLE 1.3: PERFORMANCE SUMMARY ON STATE-OF-THE-ART INTERFACE CIRCUITS AND TARGET IN THIS THESIS</th>
</tr>
</thead>
<tbody>
<tr>
<td>Supply voltage</td>
</tr>
<tr>
<td>-----------------</td>
</tr>
<tr>
<td>Current consumption</td>
</tr>
<tr>
<td>Modulator order</td>
</tr>
<tr>
<td>OTA block</td>
</tr>
<tr>
<td>Measurement time</td>
</tr>
<tr>
<td>Resolution</td>
</tr>
<tr>
<td>F.o.M</td>
</tr>
</tbody>
</table>

(1) N.A.—Not Available.
(2) TBD—To Be Determined

1.4 Challenges

Energy per measurement, the most direct and crucial parameter weighing the energy-efficiency and limiting the battery lifetime, equals the total power consumption multiplied by the measurement time. There are therefore two main challenges in the design of a capacitive-sensor interface with high energy-efficiency. First, the total power consumption should shrink into an ultra-low level. Second, the measurement time has to be cut down as short as possible.

The first challenge is one of ultra-low-power sensor interface design, and can be broken down in two sub-challenges: one is low voltage supply and the other is high
current-efficiency, since total power consumption is calculated as supply voltage multiplied by total current. Supply voltage can be reduced as process scales down, due to the correspondingly scaled threshold voltage. Also some novel structures enable the circuit to work at a relatively low supply voltage. Current-efficiency improvement mainly relies on elegant circuit design to make full use of every single current-burning path and save unnecessary current as long as the circuit stably stays in normal operation region. As a matter of fact, a sophisticated combination of these two is usually adopted so as to achieve an ultra-low-power circuit. This is the main topic of Chapter 3 of this thesis.

The second challenge is the design of an ADC that accurately processes the humidity-sensitive capacitor value and generates the desired digital relative humidity reading within a time as short as possible. The system-level design of such an ADC will be discussed in Chapter 2.

1.5 Thesis Outline

The organization of this thesis is outlined as follows.

Chapter 2 presents the system-level design. It starts with an overview of the whole system concept. Basic operation principles of delta-sigma ADCs are discussed, followed by an architectural review on delta-sigma modulators and practical considerations on high-order structures. That leads to a final diagram for the interface, along with simulation results to prove its adequate performance.

Chapter 3 dives into detailed transistor-level design for OTAs which dominate the energy consumption of delta-sigma conversion based interfaces. Conventional OTAs and an inverter-based OTA are discussed and a performance comparison on them is drawn. A new structure of current-starved inverter-based OTA is proposed. The applied common-mode feedback circuit is discussed and a technique to dynamically power-down the OTAs in the switched-capacitor integrators of a delta-sigma modulator is introduced.

Chapter 4 demonstrates the final realization combining the techniques discussed in Chapter 2 and 3. A layout ready for fabrication is shown, as well as post-layout simulation results. The interface achieves 13-bit resolution while consuming 1.36nJ per measurement, which corresponds to a figure-of-merit of 0.17pJ/Step. The results are compared with previous work, showing that this interface has the lowest energy per measurement compared to prior art.

This thesis ends with conclusions and a summary in Chapter 5. Special sections have been devoted to other applications of the work and future work on this smart humidity-sensor interface.
Chapter 2

System-Level Design

This chapter starts with a brief introduction to the system concept. Then delta-sigma analog-to-digital converters (ADCs) are discussed, which are particularly suited for the narrow bandwidth signals found in smart humidity sensors. The following subsections discuss the system-level design based on practical considerations of different structures for sigma-delta modulators. In the end, a final diagram is illustrated and corresponding simulation results are shown.

2.1 System Concept

Figure 2.1 shows the block diagram of an existing smart humidity-sensor that will form the basis of the design presented in this work [16]. The blocks integrated on-chip are surrounded by a dotted line.

In figure 2.1, \( C_x \) is the CMOS–compatible humidity-sensitive capacitor which is directly inserted to the interface for low design complexity and low area consumption. The output of the smart humidity sensor, \( D_{RH} \), is a digital representation of the relative humidity (RH). A ratiometric measurement scheme is required: the ratio of a relative humidity dependent capacitor value and a reference capacitor value is determined using an analog-to-digital converter. Therefore, \( C_x \) can be digitized ratiometrically with respect to an on-chip reference capacitor \( C_{ref} \), which will be discussed in detail in the next section. The operation of the delta-sigma conversion based interface is controlled by a set of synchronous clock signals generated by a Timing and Control block. A typical delta-sigma ADC consists of a delta-sigma modulator and a...
decimation filter. The modulator produces an oversampled bit-stream $bs$ representing the input signal $C_x$. The decimation filter cuts off the out-of-band noise of the total shaped quantization noise from this bit-stream, and brings the data rate back to Nyquist-rate. In this work, the decimation filter is implemented off-chip for flexibility, but can be easily co-integrated.

According to the humidity-sensor specifications, $C_x$ varies from 1.6pF at 30% RH to 2.25pF at 95% RH. Since $C_x$ has a baseline value of about 1pF that may vary substantially from device to device, a programmable offset capacitor $C_{off}$ is used to subtract the baseline capacitance from $C_x$ and consequently compensate for process variation. Besides, it enables more effective use of delta-sigma converter’s dynamic range. $C_{off}$ can be programmed digitally from 0.1pF to 1.5pF in steps of 0.1pF [16]. Thus, the interface produces a digital output representing the ratio of $C_x' = (C_x - C_{off})$ and $C_{ref}$. Figure 2.2 [8] illustrates the corresponding ratiometric measurement scheme.

![Figure 2.2: Ratiometric measurement scheme.](image)

### 2.2 Incremental Delta-Sigma Conversion Based Interface

During the past few years, delta-sigma converters are widely used in narrow-band signal conversion due to some unique advantages. In this section, first the principle and corresponding advantages will be introduced. Then, incremental operation for delta-sigma conversion will be discussed, which is used to meet specific requirements in instrumentation, measurement and sensor/transducer applications. Finally, the modulator, as a core part among all the blocks in an incremental delta-sigma converter, is described.

#### 2.2.1 Delta-Sigma ADCs

The main design targets of the interface tailored for capacitive humidity-sensors are drawn in Section 1.3, in line with the humidity-sensor requirements. Bandwidth (speed) is quite easy to handle, since smart humidity-sensors operate with dc-signals or low-frequency signals (up to a few hundred Hz). However, a high-resolution performance (13-bit accuracy) should be achieved while area and power consumption should be kept as low as possible, especially in the battery-powered, sensor-equipped RFID applications.
The most serious limitation on high-resolution Nyquist-rate ADCs is that in today’s widely used low-voltage CMOS digital circuits technology it is not possible to manufacture high-precision analog elements (resistors, capacitors, etc.) on which classical Nyquist-rate ADCs relies so much [18]. Delta-sigma ADCs break down the stringent reliance on precise analog elements, and employ fewer simple analog blocks to achieve adequate performance. The advantages of delta-sigma ADCs come from three aspects: First, they sample the incoming signals at a much higher rate than the bandwidth, which is called oversampling. It is quite useful to attenuate the noise spectrum density and cut down the total in-band noise (consisted of quantization noise and thermal noise). Theoretically speaking, resolution increases 0.5 bit by every doubling oversampling ratio, defined as $f_s/2BW$. Second, the quantization error brought in by the low-resolution (often one-bit) quantizer, can be further moved outside the signal band, where it can be filtered out. This so-called noise-shaping results in much more than 0.5 bits per doubling of OSR, which is very attractive for implementation in CMOS technology: resolution can be traded for speed. Third, the oversampled data is converted back to Nyquist frequency by means of digital low-pass filtering and resampling (decimation), producing the multi-bit digital output data ($D_{RH}$ in this case).

### 2.2.2 Incremental Operation

Classical delta-sigma ADCs mainly used in telecommunication and consumer electronics applications are characterized by their signal processing parameters, such as dynamic range ($DR$) and signal-to-noise ratio ($SNR$). On the contrary, the goal in sensor applications is to digitize individual samples or the average value of a noisy dc signal, and must exhibit an excellent sample-by-sample conversion performance (with low non-linearity, offset and gain error) [18]. In this case, converters can be set to operate in “single-shot” mode: they power up to produce a single conversion result (e.g. a relative humidity), and power down again to fall into “sleeping” status, waiting for next call. These delta-sigma converters tailored to instrumentation and sensor applications are usually referred to as “incremental (delta-sigma) converters” [24, 25]. The total energy consumption is reduced to an extremely low level, as the “sleeping” mode hardly burns energy. In this thesis, the performance of incremental delta-sigma converters is evaluated in terms of its absolute accuracy, which is expressed as the effective number of bits ($ENOB$), and the power consumption per measurement. This result in the Figure-of-Merit (F. o. M) expressed in (1.4).

### 2.2.3 Charge Balancing

Based on the linear model and general structure of a delta-sigma modulator with a single-bit quantizer [26], the core part of the capacitive-sensor interface is illustrated in figure 2.3. Input variable is the capacitance value of the sensing capacitor, instead of an analog voltage or current.
Equation 2.1: Charge balancing for capacitive-sensor modulator.

\[ V_{ref} \cdot (C_x - C_{off} + C_{ref}) \cdot (N_{total} - N_1) + V_{ref} \cdot (C_x - C_{off} - C_{ref}) \cdot N_1 = 0 \]
where $A = C_{\text{off}} - C_{\text{ref}}$, $B = 2C_{\text{ref}}$.

As $C_{\text{off}}$ and $C_{\text{ref}}$ is assumed to be constant (process variation and systematic error will be calibrated by programmable $C_{\text{off}}$ as mentioned in section 2.1), $C_x$ can be precisely expressed by the bit-stream density $\mu$, which is accurately generated in the delta-sigma modulator.

### 2.3 Architectures for Incremental Delta-Sigma Modulators

To reduce energy consumption, one possible solution is to reduce number of conversion clock cycles ($N$), which accounts for measurement time. Higher-order modulators can effectively achieve this goal. There are numerous architectures for the modulator implementation. In this section, based on the first-order incremental (or charge-balancing) delta-sigma modulator, higher-order extensions are raised up [18] and one suitable structure is chosen.

#### 2.3.1 First-order Incremental Delta-Sigma Converter

A first-order incremental converter with a bipolar input range is shown in Figure 2.4 [18]:

![Discrete-time model of a first-order incremental converter with a bipolar input range.](image)

It consists of a first-order modulator and a counter (digital sinc filter). The first-order modulator is implemented by one discrete-time integrator (switched-capacitor integrator) and one comparator. The fundamental drawback of the first-order bipolar incremental converter is that it must be operated through $2^n_{\text{bit}}$ clock cycles to achieve $n_{\text{bit}}$-bit resolution [18]. This is not competent for the low energy consumption requirements, because the power-on mode is too long and the thermal noise is much over-suppressed by the total cycles in the incremental operation.

#### 2.3.2 Extensions to Higher-order Modulators

One possible solution is to search for different (mainly higher-order) structures, which operate in a similar manner, but achieve much shorter conversion time due to the
higher-order architecture. In delta-sigma modulators, there are two ways to increase the achievable SNR in general: one is using multi-stage (MASH or cascaded) architecture, the other is to use higher-order modulators [18]. The latter is chosen as the architecture-level (system-level) design.

Theoretically speaking, 1st-order delta-sigma modulator own a usable input range as large as full-scale input (FS), where overloading of the integrator outputs is prevented. When the order goes higher in single-loop, which means the circuit complexity increase, the maximum input is limited within a fraction of full-scale. Typically, usable input range for 2nd-order delta-sigma converters is 0.75FS, and further shrinks to 0.67FS for 3rd-order delta-sigma converters [26]. These values are conservative and valid for most design cases. The stability problems associated with high-order single-loop modulators can be eased by the structure of the cascade modulator, also called the multi-stage or MASH (for Multi-stAge noise-SHaping) modulator [26]. However, it is not considered in this thesis due to its critical matching requirement on realization of the analog transfer function. This work employs single-loop filter, in which the number of cascaded integrators denotes the order of the single-loop filter. The value of $C_{ref}$ is chosen to be 0.8pF. This is, in principle, larger than what is needed (0.65pF) if the absolutely varying value $C_x'$ is digitized using half of the maximum input range $[-C_{ref}, C_{ref}]$. This value was nevertheless chosen to maintain compatibility with potentially more sensitive versions of the sensor obtained using variations of the post-processing flow [16].

Due to the higher loop-gain and more aggressive noise shaping, higher-order modulators are used if the number of cycles ($N$) through the conversion needs to be further reduced. This is quite helpful to reduce the total energy per measurement because it cuts down the total measurement time. A single-bit quantizer is used to generate the bit-stream ($bs$) and the order of the digital filter is chosen the same as that of the modulator. It is true that using higher-order filtering and appropriate dither signal can increase resolution assuming the same number of cycles, without modifying the analog hardware significantly [18]. However, this is not considered and applied here. An attractive example of third-order cascaded-integrators, feed-forward (CIFF) structure [27] is shown in Figure 2.5:

![Figure 2.5: A third-order Cascaded Integrator, Feed-Forward (CIFF) architecture with the input](image-url)
signal fed forward to the input of the quantizer.

For this feed-forward architecture, an expression for the equivalent number of bits \((ENOB)\) has been derived in [18]:

\[
n_{\text{bit}} = \log_2 \left( \frac{2 \max(V_{\text{in}})}{V_{\text{ref}}} \right) = \log_2 \left( \frac{U_{\text{max}} b c_i c_2}{b c_i c_2} \right) \approx 3 \log_2 \left( \frac{N - 2}{3!} \right) \approx 3 \log_2 (N) + \log_2 (b c_i c_2) - 2.6
\]

where \(U_{\text{max}}\) is the maximum normalized (dimension-less) input signal. In the last approximation \(U_{\text{max}} = 1\) and \(N \gg 1\) were assumed. This indicates a required number of cycles for \(n_{\text{bit}}\)-bit resolution [18]:

\[
N = \text{fix} \left( \frac{3!}{b c_i c_2} \right) U_{\text{max}}^{\frac{2^{n_{\text{bit}}}}{3}} + 2
\]

which can, under the same assumption, be approximated as:

\[
N = 2^{\log_2 \left( \frac{n_{\text{bit}} + 3.6 \log_2 (b c_i c_2)}{3} \right)}
\]

The \(a_i\) \((i = 1, 2, 3)\) coefficients are used to control the pole-zero map of the noise-transfer-function \((NTF)\), and \(b = c_i = 1\) initially. These latter coefficients are used to scale the integrators’ maximum output swing \(V_{\text{omax},i}\) \((i = 1, 2, 3)\). All these characteristics facilitate the \(NTF\) optimization and \(V_{\text{omax},i}\) control. A flexible requirement on \(V_{\text{omax},i}\) enables more choices for the operational trans-conductance amplifier (OTA) based integrator design.

### 2.3.3 Minimum Required Number of Cycles

Here only quantization noise is considered that is noise-shaped and filtered to generate required accuracy. Given those restrictions on the architecture, the minimum required number of cycles in incremental operation can be estimated by calculation.

For 1\(^{\text{st}}\)-order incremental modulator [18]:

\[
ENOB = \log_2 (N - 1) \approx \log_2 N
\]

For 2\(^{\text{nd}}\)-order incremental modulator [18]:

\[
ENOB = \log_2 \left[ U_{\text{max}}^{0.5N(N-1)} \right] \approx 2 \log_2 N + \log_2 (U_{\text{max}}) - 1
\]

where \(U_{\text{max}}\) is the maximum normalized (dimension-less) input signal and usually limited to 0.75. \(U_{\text{max}} = 0.75\) results in a numerical expression of \(ENOB\) for practical 2\(^{\text{nd}}\)-order incremental modulator as:

\[
ENOB \approx 2 \log_2 N - 1.415
\]

For 3\(^{\text{rd}}\)-order incremental modulator with CIFF architecture (Figure 2.5) [18]:

15
\[ ENOB = \log_2 \left[ U_{\text{max}} b c_1 c_2 \frac{(N-2)(N-1)N}{3!} \right] \approx 3 \log_2 N + \log_2 (bc_1 c_2) - 2.6 \quad (2.11) \]

where in the last approximation \( U_{\text{max}} \approx 1, N \gg 1 \) were assumed.

However, the system with unscaled factors and input signal can hardly work due to stability issue. \( U_{\text{max}} \) can be limited to 0.75, as in 2\(^{\text{nd}}\)-order modulator, and the coefficients can be improved. What’s more, the scaling factor can be optimized with the input signal even limited to \( U_{\text{max}} = 0.67 \), resulting probably the best achievable \( ENOB \) as a function of \( N \) in this structure. A numerical expression of \( ENOB \) for practical 3\(^{\text{rd}}\)-order incremental modulator is derived as:

\[ ENOB \approx 3 \log_2 N - 6.601 \quad (2.12) \]

For 4\(^{\text{th}}\)-order incremental modulator with the same CIFF architecture as 3\(^{\text{rd}}\)-order mentioned before (4\(^{\text{th}}\) order CIFF, dark blue):

\[ ENOB = \log_2 \left[ U_{\text{max}} b c_1 c_2 c_3 \frac{N(N-1)(N-2)(N-3)}{4!} \right] \approx 4 \log_2 N + \log_2 \left( \frac{U_{\text{max}} b c_1 c_2 c_3}{24} \right) \quad (2.13) \]

\( U_{\text{max}} \) is limited to 0.5 and optimized coefficients can be generated using synthesizeNTF and realizeNTF, the functions of the Delta-Sigma Toolbox in Matlab. A numerical expression of \( ENOB \) for practical 4\(^{\text{th}}\)-order incremental modulator is derived as:

\[ ENOB \approx 4 \log_2 N - 14.102 \quad (2.14) \]

Equations of (2.8), (2.10), (2.12) and (2.14) are plotted in figure 2.6 to show the \( ENOB \) obtained as a function of \( N \) for practical examples of modulators of different orders (1\(^{\text{st}}\) order, 2\(^{\text{nd}}\) order, 3\(^{\text{rd}}\) order and 4\(^{\text{th}}\) order).
Figure 2.6: Effective number of bits obtainable as a function of the number of cycles $N$.

Figure 2.6 shows the fact that to achieve a required $ENOB$ with a specific architecture a higher order modulator does not always result in a smaller number of cycles. The $ENOB$, as a function of $N$, could be universally expressed as:

$$ENOB = L_o \log_2 N - X$$  \hspace{1cm} (2.15)$$

where $L_o$ denotes the order of the modulator, $X$ denotes the degradation factor accounting for the fact that the loop filter has to be “tamed” to ensure stability. If ideal condition applies to all, which means stability issue is out of consideration and $X=0$ is used for all, the lines cross at the same point where $N=1$, $ENOB=0$. This undoubtedly results in the statement that higher order modulators always result in smaller number of cycles if a specific $ENOB$ is required. However, in practical case, the lines drift in parallel due to the degradation factor. Higher order modulators usually correspond to larger degradation factors. Therefore, the crossing points move to somewhere in the middle area (Figure 2.6). As a result, a higher order modulator does not always result in a smaller number of cycles. With the requirement of 13-bit accuracy, a 3$^{rd}$-order CIFF modulator is better than a 4$^{th}$-order CIFF modulator in terms of achieving fewest cycles.

2.3.4 Switched-Capacitor Integrator

The discrete-time integrator can be implemented with a Switched-Capacitor (SC) circuit. It is most adequate as a readout circuit for capacitive-sensors, for it transforms the input capacitance into a form of analog signal (voltage) that can be easily processed in the modulator. What’s more, it sufficiently eliminates the effect of the
parasitic capacitances and does not need complex driving voltages [28]. The switched capacitors, along with the Operational Trans-conductance Amplifier (OTA), form the switched-capacitor integrator. In first-stage, the SC circuit charges the sensing capacitors with a dc reference voltage, and integrates these charges on a capacitor, $C_{int}$ (Figure 2.7). Thus, an output voltage is derived as:

$$V_{out} = V_{ref} \frac{C_X}{C_{int}}$$  \hspace{1cm} (2.16)

In higher-order loop filter, it is a little different in other stages: a sampling capacitor with fixed capacitance is charged by the output voltage of the prior stage.

In the SC integrators, even if infinite time were available for settling, the sampling capacitor would not be completely discharged due to the finite DC gain of the OTA. This gain causes a fraction of the output voltage $V_{out}$ present at the input of the op-amp. Such leakage of the integrator’s output voltage to its input limits the ENOB of the delta-sigma modulator. Detailed analysis has been done in [29], giving out a rough estimation on the minimum required DC gain for each stage, in a 1st-order modulator and a 2nd –order modulator. To be conservative, in a 3rd-order modulator, $A_o = 70$dB is set as the minimum DC gain requirement for each OTA so as to reduce the errors associated with leakage to a negligible level. This DC gain should be maintained across the whole output swing range of the OTA.

### 2.3.5 $kT/C$ Noise versus Quantization Noise

In previous sections, only quantization noise is taken into consideration to get the Effective Number of Bits (ENOB) as a function of number of cycles ($N$) (shown in Figure 2.6). As a matter of fact, thermal noise in SC circuits will degrade the final accuracy if the thermal noise contribution is not limited to a sufficiently low level. The noise mainly comes from two parts: one is the intrinsic thermal noise of the OTAs; the other one is the thermal noise introduced by switches. In general delta-sigma modulators, input-referred thermal noise will be suppressed by oversampling ratio
Similarly, in incremental operation it is averaged during the consecutive cycles in the decimation filter. Only the noise contribution of the first integrator is significant, since the noise in later stages is noise-shaped by the loop [18, 30]. The intrinsic thermal noise of the OTA in the first integrator is usually transformed into an output-referred voltage source and is also noise-shaped. Therefore, only the noise in the SC circuit of first integrator is taken into account.

The equivalent output variance due to the input-referred thermal noise can be derived as [18]

\[ \overline{v^2_{n,th}} = k \frac{v^2_{th}}{N} \]  

where \( k = 1, \frac{4}{3}, \frac{9}{5} \) for 1st-order, 2nd-order and 3rd-order incremental delta-sigma modulators, due to different weighting coefficients of the filters [4]. Just for a simple estimation, the equivalent ENOB due to thermal noise can be derived as

\[ ENOB_{thermal} = \log_2 \left( \frac{\max(V_{in})}{\overline{v^2_{n,th}}} \right) = \frac{1}{2} \log_2 (N) + \log_2 \left( \frac{V_{in,max}}{\sqrt{k \cdot v^2_{n,i}}} \right) \]  

where \( V_{in,max} = V_{ref}/2 = 0.175V \) and \( v_{n,i} \) is the input-referred thermal noise of the first integrator.

In this work, fully-differential structure, where input and output are both differential pairs, is introduced, since it provides much better rejection of common-mode (CM) noise and high-frequency power-supply variations compared to its single-end counterpart. The input-referred thermal noise \( v_{n,i} \) in a fully-differential SC integrator can be derived as [14]:

\[ \overline{v^2_{n,i}} = \frac{8kT}{C_{s1}} \left( 1 - \frac{1}{1 + \frac{1}{x}} \right) (V^2) \]  

where \( x = g_mR_{on}, \) \( C_{s1} \) is the single-end sampling capacitance of the first integrator. In this case, \( C_{s1} \) is half of the sensing capacitance \( C_s. \)

The goal of system-level design is to reduce the number of cycles \( N \) as low as possible so as to save energy consumption per measurement, while maintaining the required accuracy. Figure 2.8 shows the ENOB as a function of \( N \) for quantization noise and thermal noise respectively, based on Equations (2.8), (2.10), (2.12), (2.14) and (2.18). It is clear that the higher the order of the incremental delta-sigma modulator, the more aggressively the quantization noise is suppressed as \( N \) increases. Different slopes result in different crossover points. On one side, it is quantization noise dominant while on the other side it is thermal noise dominant. Anyhow, all the noise contribution should satisfy the required ENOB.
For a given ENOB, a minimum $N$ is required if only quantization noise is considered. At the same time, the suppressed thermal noise corresponding to the chosen $N$ should not exceed the quantization noise. If it does, a larger $N$ has to be chosen in order to further suppress the thermal noise. When $N$ grows so large that it even meets the minimum $N$ requirement of a lower-order loop filter, this lower-order delta-sigma modulator should be used for its lower circuit complexity and better stability. As a conclusion, the order of loop filter should be properly chosen so that thermal noise and quantization noise are comparable around the minimum required $N$. In this way, probably the lowest value of $N$ is achieved so that the total measurement time is minimized to save energy. Figure 2.8 shows that for 13-bit ENOB, a 3rd-order delta-sigma modulator with optimized CIFF structure needs fewer cycles than a 4th-order modulator, and the minimum required $N$ resulting from quantization noise reduces the thermal noise to almost the same level. The minimum $N$ locates between 80 and 120.

### 2.4 System Simulation Results

A third-order cascaded-integrators feed-forward (CIFF) structure (Figure 2.9) is used to verify the previous discussions. The global feed-forward path is omitted due to special difficulty on multiplexing input sensing capacitor. The scaling coefficients $a_i$ ($i = 1, 2, 3$), $b$, $c_i$ ($i = 1, 2$) are chosen based on previous experimental results.
Figure 2.9: Architecture of the delta-sigma modulator for the interface.

Figure 2.10 shows the quantization error over the usable input range. In this ideal condition, only quantization noise is considered as noise contribution to calculate SNR and corresponding accuracy. As discussed in Section 2.3.5 that the two dominating noise sources, quantization noise and thermal noise, locate at a comparable level so that the number of conversion cycles can be fairly low. Based on Equation (2.12), the minimum required $N$ is about 85 if 13-bit ENOB is desired in this work. To leave some margin, $N=100$ is chosen for the simulation. Figure 2.10 shows that the quantization error is only 0.3 LSB of 13-bit ENOB, with sufficient margin left for other noise sources.

Figure 2.10: Quantization error versus input (N=100 with CoI decimation filter).

2.5 Diagram for the Incremental Delta-Sigma Modulator

Figure 2.11 shows the diagram of a third-order incremental delta-sigma modulator
with single-bit quantizer employing a fully-differential switched-capacitor (SC) circuit.

![A third-order delta-sigma modulator with single-bit quantizer.](image)

A CIFF structure is chosen but there is no global input feed-forward path, since input capacitance \( C_x \) is a sensing element which is difficult to multiplex. The discrete-time integrators are implemented by SC circuits with OTAs. The bit-stream is fed back to control the charge polarity of the reference capacitor.

### 2.6 Conclusion

As a conclusion for system-level design, this chapter has shown that a 3rd-order incremental delta-sigma modulator with single-bit quantizer employing the CIFF structure is used to implement the capacitance-to-digital converter. To achieve 13-bit ENOB with minimum required number of conversion cycles \( N \), this 3rd-order modulator is the optimal choice, because the \( kT/C \) noise of the first switched-capacitor integrator is comparable to the quantization noise in this case. A global input feed-forward path is avoided due to the fact that it yields relatively little output-swing reduction and would require duplicating the sensor capacitor. DC gain of the OTAs should be larger than 70dB in order to suppress the degradation from DC gain nonlinearity and leakage.
Chapter 3

Energy-Efficient Circuit Implementation

This chapter dives into circuit-level design in terms of energy-efficiency. Several candidates for the Operational Trans-conductance Amplifier (OTA) implementation are described and compared as a starting point. A fully-differential current-starved inverter-based OTA structure is proposed for the integrators. A dynamic power-down scenario is applied to reduce the power consumption of the modulator by about 40%. Then common-mode feedback circuit is chosen, followed by a brief calculation for $g_m$ requirement and current consumption. Finally, an integrated transistor-level schematic is illustrated and corresponding simulation results are shown.

3.1 Candidates for Energy-Efficient Circuit Implementation

An operational trans-conductance amplifier (OTA) is a major building block and consumes most of the power in switched-capacitor (SC) circuits [11]. The challenge to achieve low-power consumption in an OTA can be broken down in two sub-challenges: one is low voltage supply and the other is high current-efficiency, since total power consumption is calculated as the supply voltage multiplied by the total current. The continuing feature size scaling in CMOS technology has enabled a decrease of supply voltages. However, the threshold voltage is not scaled as aggressively as the transistor dimensions. Therefore, supply voltage should anyhow be high enough so as to activate the transistors and suppress leakage current. Given this fact, this chapter mainly focuses on the current-efficiency to achieve high energy-efficiency.

3.1.1 Conventional OTA Based Integrators

The operational amplifier (op-amp) is one of the most versatile and important building blocks in analog circuit design. The performance is usually limited due to various factors such as gain, bandwidth (speed), slew rate, voltage swing, etc [31]. The op-amp applied in integrators should provide sufficient input trans-conductance $g_m$ to charge and discharge the integrated capacitor within required settling period. This kind of op-amp is specially called as Operational Trans-conductance Amplifier (OTA). In an energy-efficient switched-capacitor integrator circuit, current-efficiency ($g_m$ generated per unit current) of the OTA is the most crucial issue. Besides, DC gain, which limits the settling accuracy, and output swing, which defines the maximum differential output that would not cause saturation, also deserve substantial attention.
The simplest OTA can be implemented by four MOS transistors, defined as single-stage OTA. It is characterized by very high speed and rather low DC gain. Two kinds of cascode structure can be simply included to improve the DC gain without adding complex circuits. They are known as telescopic cascode OTA and folded-cascode OTA. Cascode transistors are capable to enhance the DC gain above the design target (70dB) so that some advanced gain boosting techniques are not worthy introducing. Above all, two candidates are shown in Figure 3.1.

![Figure 3.1: Two candidates for current-efficient OTA: (a) Folded-Cascode; (b) Telescopic Cascode](image)

### 3.1.2 Inverter-Based Integrators

There has been another approach to improve power-efficiency. It is an inverter-based switched-capacitor (SC) circuit that does not utilize a conventional OTA [11]. The gates of PMOS and NMOS transistors are connected together so that they both contribute to the input trans-conductance while sharing the same supply current. As a result, the intrinsic current efficiency doubles. Class-C inverter is employed where PMOS and NMOS both operate in weak inversion and, as MOS transistors operating in weak inversion can provide a larger value of $g_m/I_d$ than that in strong inversion [32], denoted as current efficiency.
An auto-zeroing technique is essentially introduced to cancel the offset and form a virtual ground. Figure 3.2 [11] shows the operational diagram of auto-zeroing an inverter-based SC integrator. During $\phi_1$ phase, the inverter is switched to form a unity gain configuration and $V_{OFF}$ is sampled in $C_c$. At the same time, the $V_f$ is sampled in $C_S$ with respect to the signal ground. During $\phi_2$ phase, the $V_X$ should be $V_{OFF}$ due to the negative feedback formed through $C_i$. This forces $V_G$ to be the signal ground because $C_c$ holds $V_{OFF}$. Thus, the node $V_G$ can be considered as a virtual ground and the charge in $C_S$ should be transferred into $C_i$ in a way similar to the conventional SC circuits. This inverter-based switched-capacitor integrator has been applied in delta-sigma modulators that operate at supply voltages as low as 0.7V while consuming only $22\mu$W [11]. In Figure 3.3, a pair of inverters forms a fully-differential OTA that could also be counted in as a candidate for high current-efficiency.

3.1.3 Performance Comparison

The current-efficiency can be evaluated as the number of unit currents $I$ that is needed
to generate a given $g_m$, which is clearly shown in Figure 3.4.

In this comparison, it is assumed that a folded-cascode OTA biased at a current $I$ in all its branches generates a trans-conductance $g_m$. To generate the same $g_m$, a telescopic-cascode OTA needs only $2I$, as the input and current sources stay in the same path sharing current, improving the current efficiency by a factor of 2 at the expense of smaller output swing or higher supply voltage. An inverter-based OTA just needs a current $I$ to generate the same $g_m$, as both the PMOS and NMOS transistors contribute to the input trans-conductance. Table 3.1 summarizes the properties of OTA candidates that can be used in SC circuits. Although a comparison based on accuracy figures is not possible, Table 3.1 clearly shows that the inverter-based OTA structure is the most attractive candidate for its dominant current-efficiency.

**Table 3.1. Performance Comparison for OTA Candidates**

<table>
<thead>
<tr>
<th></th>
<th>Folded-Cascode</th>
<th>Telescopic-Cascode</th>
<th>Inverter-based</th>
</tr>
</thead>
<tbody>
<tr>
<td>Energy Efficiency</td>
<td>--</td>
<td>0</td>
<td>++</td>
</tr>
<tr>
<td>Low Supply Voltage</td>
<td>0</td>
<td>-</td>
<td>+</td>
</tr>
<tr>
<td>Output Swing</td>
<td>0</td>
<td>-</td>
<td>+</td>
</tr>
<tr>
<td>DC gain (settling accuracy)</td>
<td>+</td>
<td>+</td>
<td>-</td>
</tr>
<tr>
<td>Bandwidth (speed)</td>
<td>0</td>
<td>0</td>
<td>+</td>
</tr>
<tr>
<td>PSRR</td>
<td>+</td>
<td>+</td>
<td>-</td>
</tr>
</tbody>
</table>

++: very good, +: good, 0: average, -: poor, --: very poor

As a conclusion, the inverter-based OTA structure has the main advantage of highest
current efficiency among all the candidates. However, some disadvantages of this inverter-based OTA can not be neglected. First of all is the high sensitivity of self-generated biasing point to process variation, which could be eliminated by auto-zeroing technique. Second is the low DC gain provided by simple inverter, which could be enhanced by cascode transistors. Last but not least, the poor power supply rejection ratio (PSRR) make the noise effect in both ends (supply and ground) a serious issue. What’s more, simple inverter-based OTA can not directly be used in a system that supply voltage may vary significantly.

3.2 Current-Starved Inverter-Based OTA

To overcome the drawbacks of the simple inverter-based OTA summarized at the end of last section, a new structure of current-starved inverter-based OTA with simple cascodes is proposed.

3.2.1 Structure

Conventional OTAs usually have better PSRR than inverter-based OTA due to the PMOS current source in the top which provides supply current to the differential pair. This current source can also be applied in the inverter-based OTA to gain an adequate PSRR, at the cost of extra voltage headroom (typically 0.2V in 0.16μm standard CMOS technology) for the current source. Another NMOS current sink can also be included in the bottom, not only for structural symmetry, but also for better negative supply (ground in this case) rejection ratio. What’s better, these properly biased transistors characterize the OTA with less sensitivity of active-region biasing to variations in processing, temperature, and supply. Auto-zeroing technique is avoided and the OTA could fall “asleep” during stand-by phase, saving much power. This kind of structure, where a floating inverter is sandwiched between a current source and a current sink, was first proposed and applied in voltage control oscillators as current-starved inverter [33]: inverter with both PMOS tail sourcing current and NMOS tail sinking current. This current-starved inverter is also employed in ring-oscillator [34], delay element [35], and filters [36]. The structure is shown in Figure 3.5.
Two novel fully complementary self-biased CMOS differential amplifiers have been presented [37]. Both differ from conventional CMOS differential amplifiers in having fully complementary configurations and in being self-biased through negative feedback. The amplifiers have been applied as precision high-speed comparators in commercial VLSI CMOS integrated circuits [37]. The fully complementary structure, i.e., each n-type device operates in push-pull fashion with a corresponding p-type device, denotes as current-starved inverter and results in primary performance enhancement on robustness, the capability of supplying switching currents which are significantly greater than the quiescent bias current, and nominal doubling of differential-mode gain (due to doubling of $g_m$ as both PMOS and NMOS transistors contribute to $g_m$).

However, the intrinsic gain provided by the inverter is low (around 40dB). That cannot meet the DC gain requirement and the nonlinearity of gain will deteriorate the performance significantly in terms of accuracy. A simple cascode structure can be used to enhance the gain. As a result, the fully-differential OTA in switched-capacitor integrator can be replaced by a pair of current-starved cascode inverters shown in Figure 3.6. The pair of cascode inverters floating between two current tails can also be regarded as a combination of two differential pairs.

This fully complementary structure inherits the characteristic of conventional OTA such as good PSRR, robustness to process variation and environmental effects, etc. The connection of PMOS and NMOS input transistors, forming current-starved inverter structure, doubles the nominal $g_m$ and DC gain. The input transistors operate at weak inversion region in order to provide a high current efficiency. The cascode transistors operate at weak inversion as well so that less headroom is required for
overdrive voltage and larger output swing is available.

![Figure 3.6: Current-starved inverter-based cascode OTA.](image)

### 3.2.2 Operation Mode

Based on the characteristic of this current-starved inverter-based cascode OTA, auto-zeroing technique is not required to define the operation point. Therefore, during $\phi_1$ phase, input signal is sampled by charging the sampling capacitor and the OTA just stand-by, instead of auto-zeroing. During $\phi_2$ phase, charge stored in sampling capacitor containing information of input signal is transferred to integrated capacitor $C_I$ and corresponding output voltage is formed up. This is the same as conventional OTA based SC integrator, but current efficiency doubles and consequently the supply current can be cut half down when the $g_m$ requirement is the same.

What’s more, the OTA can be dynamically powered down during the stand-by phase that would save considerable power. This dynamic power-down scenario will be discussed and realized in next section. Nevertheless, there are six transistors in-series from supply to ground, resulting in quite limited output swing and relatively high supply voltage for stable operation in standard CMOS technology. Approximately speaking, supply voltage should be 0.3V higher but current efficiency nearly doubles if the OTA is powered down in half period. Eventually, some power can be saved and the energy-efficiency can be improved.
3.3 Dynamic Power-Down Scenario

As the OTA consumes most of the power in a switched-capacitor integrator, dynamically powering down the OTA when it is stand-by can significantly improve the energy-efficiency. Powering down the OTA can be simply realized by cutting off the supply. The main challenge lies in powering up the OTA sufficiently: the transition time from power-down mode to power-on mode should be fast enough and all the transistors in the OTA should be resettled to normal operation region within this limited period. Two possible power-down scenarios are discussed in detail.

3.3.1 Pull up/down Scenario

This can be implemented in several ways. The top supply node can be switched to supply voltage $V_{dd}$ during power-on period, and switched to ground $gnd$ during power-down period. The charging and discharging the parasitic capacitance of all the transistors would be quite a heavy load so that it would take very long time to accomplish the transition. A better and conservative way is to turn off the current source and sink as switches. This can be implemented by pulling up the PMOS gate voltage to supply and pulling down the NMOS gate voltage to ground during power-down mode. The $V_{gs}$ of current source and sink nearly approach zero due to the pull up/down scenario so that the leakage current is extremely low. In this approach, only the parasitic capacitances of current source and sink need to be recharged before OTA starts to work. However, the size of the transistors implementing the tail-current sources is so large that the corresponding gate-source capacitance is relatively large. These parasitic capacitances have to be charged by the current flowing in the input branch of the current mirror, of which the tail-current sources are part. For power-efficiency, the current in this input branch is typically much lower than the tail current. If this current is required to charge up the gate-source capacitance fast enough (less than 10% of the period), it will typically have to be increased, which is not desirable in this low-current, power-efficient application. An alternative way is to cut off the cascode transistors by in the same way (pull up/down gate voltages). The cascode transistors are smaller so the powering up speed improves a bit, but still unacceptable with the very low current levels at which the bias circuit is typically operated. Increased current spent in the circuit that biases the cascodes is undesirable, which is the same case as before.

3.3.2 Isolation Scenario

In low-current applications, increasing bias currents is not a suitable way to enhance the driving capability. One possible solution could rely on employing slower clock signals, which means longer settling time. As a result, however, measurement time increases and more energy are consumed.
Isolation scenario can effectively improve the start-up procedure. When the OTA finishes its job and is ready to be powered down, it is isolated from the supply by high impedance. From then on, all the transistors in the OTA are isolated to hold the charge in their parasitic capacitance. Leakage is inevitable but can be reduced to a negligible level. In this case, the OTA is not in “deep sleep” (which means all the parasitic capacitances are completely discharged) and can be easily “woken up” (which means all the transistors are resettled to normal bias point and ready to operate). The biasing just needs to compensate for the very little leakage charge and the OTA can rapidly start up and resettle to normal operation point. The current-starved inverter-based cascode OTA with dynamic power-down scenario implemented by isolation switching is shown in Figure 3.7.

![Figure 3.7: Dynamic power-down implemented by isolation switching.](image)

### 3.4 Common-Mode Feedback (CMFB) Circuit
Fully-differential circuits are often applied in mixed-signal designs to improve immunity to common-mode disturbances generated by the digital circuits, the class-AB drivers, the clock drivers, etc [32]. However, a common-mode feedback (CMFB) is required to stabilize the average or common-mode output level so as to guarantee a normal and constant biasing point for the fully-differential circuit. It is called the common-mode feedback (CMFB) circuit.

One common kind of CMFB circuits is implemented by another amplifying circuit. It has to measure the differential output voltages, cancel the differential signals and close the feedback loop. Also, the CMFB amplifier always operates in unity-gain. The open-loop gain of the CMFB amplifier is used to increase the common-mode rejection ratio. However, the stabilization of the common-mode output voltage does not need to be so accurate so that the gain is not a critical issue. Besides, the speed of CMFB amplifier should be faster than that of differential amplifier so that it is able response rapidly and stabilize the common-mode operation point sufficiently. Yet, in some specific circuits such as some delta-sigma converters, high speed amplifiers are only used in the low-frequency region. In this case this specification can be relaxed considerably [32]. Anyway, this kind of CMFB circuit takes additional current.

Due to the relaxed requirement on the CMFB circuit tailored for delta-sigma converters, another kind of CMFB circuit, which is probably the simplest candidate, is introduced. It uses a pair of MOS transistors operating in the linear region for the common-mode feedback. The differential outputs are connected to the gates of these transistors. Their drains are connected together to cancel the differential signal and the feedback loop is closed [32]. As the input transistors of the CMFB circuit operate in the linear region, this structure provides moderate gain and relatively slow response. However, it does not consume any extra current so as to be rather a current-efficient solution.

The two mentioned CMFB circuits are both implemented with transistors. The output swing is a last but not least problem. It is limited by both the output swing of differential amplifier and by the common-mode input range of the CMFB amplifier (whichever is smaller). Considering the design challenges for CMFB circuits, the switched-capacitor technique is introduced, resulting in the switched-capacitor common-mode feedback circuit. The main advantages of SC-CMFBs are that they impose no restrictions on the maximum allowable differential input signal, have no additional parasitic poles in the CM loop, and are highly linear. However, SC-CMFBs inject nonlinear clock-feedthrough noise into the OTA output nodes and increase the load capacitance that needs to be driven by the OTA. Hence, SC-CMFBs are typically used in switched-capacitor applications [38].

Finally, in this low-current, power-efficient interface design, the CMFB circuit implemented by linear MOS transistors is chosen to achieve high current-efficiency, as a main purpose, and prevent extra load capacitance at outputs, which indirectly
reduce the required current level. As this CMFB circuit is designed for the OTA that employed in a delta-sigma modulator, the relatively low gain and low speed can be tolerated. Figure 3.8 shows the current-starved inverter-based cascode OTA with linear MOSTs CMFB.

Most designs use a mid-supply common-mode reference for symmetry, but it is not valid in this work. The design target for the supply voltage is from 1.2V to 1.8V, but the common-mode output voltage, which sets up a proper bias for the OTA, should be stable and constant. Therefore, the CMFB circuit is placed in the bottom employing NMOS transistors so as to achieve a ground-referred common-mode output voltage.

![Diagram](image)

Figure 3.8: current-starved inverter-based cascode OTA with linear MOSTs CMFB

### 3.5 Intrinsic Noise

The power spectral density (PSD) of the intrinsic thermal noise current of a MOSFET is given by

\[
S_n(f) = 4kT\varepsilon_m A^2 / Hz
\]  

(3.1)
where $g_m$ is the trans-conductance of the device, coefficient $\varepsilon$ is derived to be equal to $2/3$ for a strong-inversion region and $1/2$ for a weak-inversion region. The noise in tail-current source/sink is common-mode noise and does not contribute to the differential input-referred noise. The noise in cascode transistors is attenuated by their intrinsic gain and can be neglected compared to the noise level of input transistors. Therefore, assuming that both PMOS and NMOS have the same trans-conductance $g_m$, the input-referred thermal noise voltage of this current-starved inverter-based cascode OTA is obtained as follows:

$$S_v(f) = \frac{kT}{g_m} [V^2 / Hz]$$

(3.2)

where $g_{mw}$ is the trans-conductance of one single MOS transistor in weak-inversion region. As a matter of fact, $g_{mw}$ is larger (2~4 times) than $g_{ms}$, which is the trans-conductance of the strong-inversion transistor, for a given bias current [32]. Thus, the thermal noise level of this OTA is approximately ten times lower than that of a conventional OTA for a given bias current.

Another dominant noise source is flicker noise or $1/f$ noise caused by charge carriers getting trapped and later released as they move in the channel. It is given by:

$$S_v(f) = \frac{K}{C_{ox}WL\cdot f} [V^2 / Hz]$$

(3.3)

where $W$ and $L$ are the width and length of a transistor, $C_{ox}$ the gate capacitance per unit area, $f$ is the frequency and $K$ is a process-dependent parameter. Note that flicker noise is not white, most of whose power is concentrated at low frequencies. In many cases, the effects of flicker noise may be reduced using large input devices. Also, advanced techniques such as correlated double sampling or chopper stabilization [39] can be used to suppress the flicker noise, or to modulate it to out-of-band frequencies, if necessary.

### 3.6 $g_m$ Requirements and Current Consumption

The supply current required for the OTA is determined by the settling requirement. The clock frequency is 500 kHz, which is kept the same as that in previous design, resulting a period time of 2us. To achieve sufficient settling accuracy, settling time is set to be 0.8us in each period. In switched-capacitor circuits, if the system requires an $m$-bit performance, the settling error at the output must be less than half an LSB, which results in the condition:

$$e^{-t/\tau} \leq 2^{m+1}$$

(3.4)

This is equivalent to:

$$t \geq (m+1)\tau\ln2$$

(3.5)
where \( t \) is the settling time, \( m \) is the required effective number of bits, and \( \tau \) is the charge-transfer-time constant.

When the capacitance-to-voltage converter is implemented with a one-stage OTA, based on the model shown in Figure 3.9, the charge-transfer-time constant can be expressed as [40]:

\[
\tau = \frac{1}{g_m} \left( C_{in} + C_L + \frac{C_{in} \cdot C_L}{C_{int}} \right)
\]

(3.6)

Substituting (3.2) into (3.3), the \( g_m \) requirement can be calculated as:

\[
g_m = \ln(2^{m+1} \frac{t}{C_{in} + C_L + \frac{C_{in} \cdot C_L}{C_{int}}})
\]

(3.7)

where \( C_{in} \) is total input capacitance, \( C_{int} \) is the integrate capacitance, \( C_L \) is total load capacitance.

![Figure 3.9: Equivalent model to calculate the charge-transfer-time constant.](image)

For different stages, the equivalent input and load capacitances are different. Based on the value of the capacitors determined by the system-level design, the calculation of current consumption for each OTA is shown in Table 3.2.

<table>
<thead>
<tr>
<th>TABLE 3.2. CURRENT CONSUMPTION CALCULATION</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Required ( g_m )</strong></td>
</tr>
<tr>
<td>-------------------------</td>
</tr>
<tr>
<td>1(^{st} ) OTA</td>
</tr>
<tr>
<td>2(^{nd} ) OTA</td>
</tr>
<tr>
<td>3(^{rd} ) OTA</td>
</tr>
</tbody>
</table>

A unit bias-current of 50nA is used to generate the supply currents for the three OTAs via current mirrors. The multiple of current source/sink is 48 for first OTA, 16 for second OTA, and 8 for third OTA, resulting in the same current density. Then the size of tail-current source/sink, the \( g_m \) and the current consumption of the three OTAs are scaled in the same ratio.

### 3.7 OTA1 Simulation Results
Since the three OTAs have the same structure and scaled sizes, only the simulation results for the OTA1 (employed in the first integrator) are shown, as it is the most critical one. In this section, DC gain and input $g_m$, which affect the leakage effect and settling accuracy respectively, are simulated and shown. Followed is the output swing which is defined so as to prevent overloading of the integrator. The noise performance is also shown in the end, which proves that the intrinsic noise is much lower than the tolerable value and advanced techniques tailored for reducing flicker noise are not essentially needed.

### 3.7.1 DC Gain and Input Trans-conductance $g_m$

Figure 3.10 shows the Bode diagram, which depicts the DC gain and the input trans-conductance $g_m$ of the OTA1.

![Figure 3.10: Bode diagram.](image)

The DC gain is 79.4dB which meets the design target and even leave quite a large margin. The $GBW$ is expressed as:

$$GBW = \frac{g_m}{2\pi C_L} \quad (3.8)$$

where $C_L$ is the total load capacitance. A load capacitor of 50pF is connected at the output and the parasitic load capacitance is assumed to be neglected. This results in a $g_m$ of 60μS. The $g_m$ derived from the operation point of transistors is 63μS, which is
quite close to the calculated one from \( GBW \). This also meets the requirement drawn in Table 3.2. Similar simulation results are obtained for the OTA2 and OTA3, which are employed in the second and third integrators respectively, but not shown here.

### 3.7.2 Output Swing

Figure 3.11 plots the DC gain versus output swings for the OTA1. It clearly shows that even though the DC gain nonlinearity happens along with the varying swing, the DC gain is always above 76dB within 200mV output swing. Beyond 200mV, the gain drops dramatically. OTA gain nonlinearity is a potential source of error in low-voltage applications because of the low intrinsic gain of scaled MOS transistors operating in weak inversion region [41]. To be conservative, 200mV is set as a requirement of output swing for integrators. The DC gain requirement (70dB) is always met and the accuracy will not be affected by the imperfections of the OTAs.

![Figure 3.11: DC gain vs. output swing.](image)

### 3.7.3 Intrinsic Noise Performance

Figure 3.12 plots the input-referred \( PSD \) of the intrinsic noise in the OTA1. The flicker noise dominates in the low frequencies and drops with a slope of 10dB/dec, which is in line with the theoretical Equation (3.3). The flicker noise corner stays approximately at 40kHz, which is fairly far away from sampling frequency \( (f_s=500kHz) \). The flicker noise can be treated as “slow-varying” offset at input. Recalling Equation (2.1) for charge balancing, this “slow-varying” offset \( V_{off,flicker} \) will
affect the actual charging voltage ($V_{\text{ref}} - V_{\text{off,flicker}}$ in stead of $V_{\text{ref}}$), but not affect the finally expression of $C_x$ in ratiometric measurement scheme. Therefore, dc offset and low-frequency noise of the OTAs are not critical in this design and advanced circuit techniques such as chopper stabilization is not introduced in this work.

Figure 3.12: PSD of intrinsic noise.

**3.8 Conclusion**

As a conclusion for transistor-level design, this chapter has shown that a structure of current-starved inverter-based cascoded OTA, which is much more current-efficient than conventional OTAs, is employed in the switched-capacitor integrators to form the modulator. The core part of the OTA is isolated from the supply and ground when it is stand-by, in order to save power. CMFB circuit implemented by linear MOSTs is used to prevent extra current consumption. The DC gain and output swing of this OTA meet the requirements obtained in system-level design. Thanks to the good noise performance and robustness of the current-starved inverter-based cascoded OTA, advanced techniques for reducing the effects of OTA imperfections such as autozeroing and chopper stabilization are not included.
Chapter 4

Final Realization

This chapter describes the final realization of a 3\textsuperscript{rd}-order incremental delta-sigma modulator, in which the techniques introduced in the previous chapters have been applied. It is implemented using 0.16\textmu m standard CMOS technology and achieves 13-bit capacitance-to-digital conversion. Layout is shown and the post-layout simulation results confirm the expected improvement in energy-efficiency. A comparison with previous work, included at the end of this chapter, shows that it consumes, to date, the least energy per measurement.

4.1 A 3\textsuperscript{rd}-order Incremental Delta-Sigma Modulator Employing Current-Starved Inverter-Based OTAs with Dynamic Power-Down Scenario

A block diagram of the sensor chip is shown in Figure 4.1. As mentioned in Section 2.1, \( C_x \) is the CMOS–compatible humidity-sensitive capacitor which is directly inserted to the interface for low design complexity and low area consumption. It consists of a structure of meander-fork electrodes of 100\textmu m × 100\textmu m in the top metal layer, topped with a humidity-sensitive dielectric layer [16]. An off-chip 3\textsuperscript{rd}-order cascade-of-integrators decimation filter converts the bit-stream into a digital number \( D_{RH} \) representing the relative humidity. A separated on-chip circuit is used to generate the modulator’s reference voltage \( V_{ref}=0.35\text{V} \). The modulator’s reference capacitor \( C_{ref} \) is also included on-chip. A programmable capacitor array forms \( C_{off} \) to subtract the baseline of \( C_x \). An on-chip bias circuit generates biasing voltages for the cascode transistors and a common-mode reference voltage. For the sake of testing and debugging when the chip is back, some on-chip circuits are designed so that the measured capacitance can be the sensing capacitor, or an external capacitor with specified value, and all the output voltages of the integrators can be amplified and easily measured externally. Finally, a Timing&Control circuit generates clock signals for switches and control signals in order to enable/disable specified operations via an external clock and configuration signals.
Figure 4.1: Block diagram of the smart humidity sensor.

This thesis focused on the design of the core part: an energy-efficient 3rd-order delta-sigma modulator. Figure 4.2 depicts a circuit diagram of this modulator. The sensor capacitance $C_x$ is embedded in this modulator as sampling capacitor of the first integrator. The modulator is implemented with fully differential circuit so that $C_x$ is split into two halves. Each half is assumed to vary from 0.8pF to 1.2pF. $C_{off}$ is also split into two halves and each half is set to be 1pF as a baseline in the middle. A CIFF structure is adopted but the global input feed-forward path is discarded because it would require duplicating the sensor capacitors and provides little advantage in this single-bit modulator in terms of signal swing reduction at the integrator outputs. Three switched-capacitor integrators are used to form a 3rd-order loop filter. A summing circuit adds all the outputs of the integrators and feeds them into a comparator, which generates the bit-stream $bs$. Due to charge balancing, $C_x$ can be expressed ratiometrically as a precise function of $C_{ref}$ and $\mu$, where $\mu$ is the bit-density of the bit-stream ($0 \leq \mu \leq 1$). This system-level structure is designed to perform a capacitance-to-digital conversion with a 13 bits resolution while consuming a small number of clock cycles ($N=100$).

The three OTAs employ the current-starved inverter-based cascode structure with linear MOSTs as CMFB circuit, shown in Figure 3.8 in Section 3.4. Each OTA need its own control (the pair of linear MOSTs), but the common-mode voltage biasing path is shared, as shown in Figure 4.3. The three OTAs also share a single current mirror that provides the tail currents. The sizes (multiples of equal unit devices) of the three tail-current sources are proportional to the desired $g_m$ of the three OTAs, resulting equal current densities.
Figure 4.2: Realization of a 3rd-order, one-bit delta-sigma modulator as a fully-differential switched-capacitor circuit.
Figure 4.3: Realization of three current-scaled inverter-based cascade OTAs with shared common-mode voltage biasing.
The comparator is implemented as a dynamic latch preceded by a preamp (shown in Figure 4.4 [29]), which prevents kickback to the summing capacitors. The size of input transistors should be carefully chosen as a compromise between speed and accuracy. Large input transistors result in large $g_m$, which means the delay would be small and the response is fast. On the contrast, small input transistors result in small parasitic gate-source capacitance, which will reduce the effect of voltage attenuation due to charge redistribution between summing capacitors and these parasitic capacitors. Finally size of input transistors of preamp is set as 15/0.25.

![Figure 4.4: Circuit diagram of the latched comparator.](image)

A biasing circuit (shown in Figure 4.5) is used to generate the common-mode reference voltage $V_{cm}$ and the bias voltages $V_{bp}$ and $V_{bn}$ for the PMOS and NMOS cascode transistors in the OTAs. $V_{cm}$ is defined by the $V_{GS}$ of $MN_1$, which is precisely determined by the bias current and the size of $MN_1$. The bias point $V_P$ is also fixed when the size of $MP_1$ is fixed. $V_{bp}$ is given by $V_P$ subtracting $V_{GS}$ of $MP_2$. $V_{bn}$ is generated in the same way as $V_{cm}$, defined by the $V_{GS}$ of $MN2$. Therefore, $V_{cm}$, $V_{bp}$ and $V_{bn}$ are all generated in terms of the corresponding $V_{GS}$ which is accurately fixed by the bias current. Decoupling capacitors are introduced to stabilize the bias voltages. This circuit also provides bias currents for the comparator and the input current for the current mirror in Figure 4.3 that biases the OTAs.
A separate circuit (Figure 4.6) is used to generate the reference voltage $V_{ref}$ to which the capacitors at the input of the modulator are charged. It consists of two current mirrors with common source, where the input is a bias circuit of 0.2μA. $V_{ref}$, as an output voltage, is defined by $V_{gs,MP1} + V_{gs,MN1} - V_{gs,MN2}$, or $V_{gs,MP2}$ directly. The bias current in the input branch is a fixed value, and results in a fixed current in the output branch via the two current-mirrors. Therefore, $V_{gs,MP1}$, $V_{gs,MN1}$, $V_{gs,MN2}$, and $V_{gs,MP2}$ are fixed due to the relationship between the current and the gate-source voltage of a MOS transistor so that $V_{ref}$ is precisely generated. Besides, the common source node at the output branch facilitates $V_{ref}$ with good driving capability and low intrinsic resistance in series-connect.

**Figure 4.6: Circuit diagram of $V_{ref}$ generation.**

### 4.2 Layout
Figure 4.7 shows the layout of the 3\textsuperscript{rd}-order delta-sigma modulator. The tail-current sources for the three OTAs are placed as close as possible in order to obtain good matching. This also applies to the CMFB linear MOS transistors. The main bodies (a pair of cascode inverters) of the three OTAs are distributed separately according to the signal flow.

![Figure 4.7: Layout of the 3\textsuperscript{rd}-order delta-sigma modulator.](image)

### 4.3 Simulation Results

CIFF structure is quite convenient to control the output swing of integrators via the scaling coefficients. The output swing is limited within the target of 200mV so as to prevent overloading. Figure 4.8 shows that the chosen coefficients can properly scale the signal flow and restrain the outputs of integrator within desired range. The y-axis is normalized with bipolar $V_{\text{ref}}$ of 0.35V. The output swing of 1st, 2nd and 3rd integrator can be easily calculated, which are 180mV, 130mV and 80mV respectively. None of them exceed the design target (200mV).
As discussed in Section 2.2.3, the humidity-sensing capacitance $C_x$ can be expressed as a function of $C_{off}$, $C_{ref}$ and bit-stream density $\mu$. Therefore, the final accuracy depends on the accuracy of $C_{off}$ and $C_{ref}$ besides $\mu$. In schematic simulations, the exact values of $C_{off}$ and $C_{ref}$ have first been determined by ac simulation, so as to be able to qualify the error contribution of the modulator from subsequent transient simulations of the modulator. The result is shown with red line in Figure 4.9. These figures are achieved with the $N$ (number of clock cycles) equal to 100, supply voltage of 1.2V, normal room temperature of 27 degree and nominal process corner. The simulated error contribution of the modulator exceeds $\pm 0.5\text{LSB}$ of 13 bits at the two extremes. But this can be improved by increasing $N$ or introducing two-point calibration. The latter will be discussed and introduced in the following paragraphs.

The error is input-signal dependent, which is small at central and large at positive/negative extremes. This phenomenon is in line with the system-level simulation result where only quantization error is taken into account. The underlying reason of this gain error could be that the flicker noise of the OTA can be assumed as a slow varying “offset” and this is transformed into an input-signal dependent variation during the charge integration. One more bit can be obtained if this gain error is canceled.

In post-layout simulation, precise values of $C_{off}$ and $C_{ref}$ can not be readily extracted. Therefore, calibration is introduced to cancel this effect. Infinite accuracy is assumed at both ends (0.8pF and 1.2pF) of the input range to get virtual values of $C_{off}$ and $C_{ref}$. These values are then applied the intermediate points to get the INL. The black line in
Figure 4.9 shows the post-layout simulation results. In this simulation, only the layout parasitics of the modulator were taken into account, which is probably the most significant among all the blocks. After calibration at both ends, a 13-bit ENOB is obtained. This two-point calibration is also applied to the schematic simulation results to make a clear comparison between schematic and post-layout simulation results. Therefore, the layout parasitics of the modulator are negligible and will not degrade the performance on accuracy.

Current consumption is a primary factor that evaluates the energy efficiency. Without applying the dynamic power-down approach, the modulator consumes about 3.9 μA (3.6 μA distributed to the three OTAs and 0.3 μA distributed to the comparator), while the "supporting" circuits, including bias circuit and reference voltage generation, consume about 3.2 μA. When dynamic power-down approach is applied to the three OTAs, the current can be saved. Figure 4.10 shows the post-layout simulation results for total current consumption and current savings corresponding to different duty cycles, as well as the theoretical results.
Waking up the sleeping OTAs consumes extra dynamic current, resulting in less current savings than expected. This is quite evident when the dynamic power-down period is quite short (less than 300ns). If the power-down period is too short that the OTAs are waked up before they fall into “steady sleep”, the current savings are dramatically lower than the expected value. But when the power-down period is sufficiently long, the current savings increase linearly as duty cycle increases. However, the current savings saturate to a maximum value when duty cycle exceeds 46%, corresponding to 0.92µs for power-down period. The underlying reason may be that a minimum period is required to resettle the OTAs to a proper biasing condition, even though they are isolated during stand-by phase. If the resettle period is sufficiently long with the normal dynamic recharging current that the OTAs are completely ready when the integration period comes, the current savings increase proportional to duty cycle. Otherwise, the OTAs calls for more dynamic recharging current to pull them back to normal operation point, which means the linearity between current saving and duty cycle is broken. This regularity is depicted in Figure 4.10.

Corner effect is taken into investigation to see whether the process variation will degrade the performance in terms of accuracy and current consumption. The robustness of the OTAs is significantly improved so that the modulator is not sensitive to corner effect. But the OTAs fail to work properly at the corner of snsp (slow NMOS and slow PMOS) when supply voltage is 1.2V, since the transistors with increase threshold voltage in slow corner requires sufficient headroom for the
tail-currents, corresponding to sufficiently high supply voltage. For other corners, the process variations do not degrade the performance. When supply voltage is raised up to 1.5V or 1.8V, the corner effect is negligible and does not degrade the performance in terms of accuracy.

The above results are all obtained at room temperature, which is normally 27 degree. Considering temperature effect, the simulation for accuracy is redone at -10 degree and 80 degree respectively, to see whether this interface can maintain the performance within the commercial temperature range. Figure 4.11 shows that the $ENOB$ is degraded by about 1.5 bits at -10 degree and maintained 13 bits at 80 degree after two-point calibration.

![Figure 4.11: Accuracy for -10 and 80 degree respectively.](image)

This interface is not able to work at quite a low-temperature. The reason could also be the insufficient margin of supply voltage. The threshold voltage of transistors increases when temperature decreases. At -10 degree the 1.2V supply voltage can not provide enough headroom for the tail-currents due to the increased threshold voltage, which means some transistors are not operating normally. This ends up with a big accuracy drop.

### 4.4 Benchmark

Table 4.1 compares the performance of the interface discussed in this chapter with previous work. The work in column 1 to 4 ([19], [20], [21], [22]) is done in academic field, while the work in column 5 [23] is done in industry field. Column 6 shows the work done in EI lab of TU Delft designate for PASTEUR project. This table clearly shows that the capacitive-sensor interface described in this work achieves the lowest
figure-of-merit (energy consumption per step) to date.

### Table 4.1: Performance Summary on State-of-the-Art Interface Circuits and Target in This Thesis

<table>
<thead>
<tr>
<th></th>
<th>[19]</th>
<th>[20]</th>
<th>[21]</th>
<th>[22]</th>
<th>[23]</th>
<th>[16]</th>
<th>This work</th>
</tr>
</thead>
<tbody>
<tr>
<td>Supply voltage</td>
<td>3V</td>
<td>1V</td>
<td>1.8V</td>
<td>3.3V</td>
<td>1.8V</td>
<td>1.8 V</td>
<td>1.2V~1.8V</td>
</tr>
<tr>
<td>Current consumption</td>
<td>3.3μA</td>
<td>1.5μA</td>
<td>460μA</td>
<td>436μA</td>
<td>70μA</td>
<td>5.85 μA</td>
<td>5.7μA</td>
</tr>
<tr>
<td>Modulator order</td>
<td>1st</td>
<td>2nd</td>
<td>3rd</td>
<td>1st</td>
<td>N.A.*</td>
<td>2nd</td>
<td>3rd</td>
</tr>
<tr>
<td>OTA block</td>
<td>Class AB</td>
<td>Class AB</td>
<td>Telescopic</td>
<td>N.A.*</td>
<td>N.A.*</td>
<td>Folded-Cascode</td>
<td>Current-Starved Inverter</td>
</tr>
<tr>
<td>Measurement time</td>
<td>100ms</td>
<td>1s</td>
<td>0.025ms</td>
<td>0.128ms</td>
<td>10ms</td>
<td>10.2 ms</td>
<td>0.2ms</td>
</tr>
<tr>
<td>Resolution</td>
<td>9 bit</td>
<td>12 bit</td>
<td>9.7 bit</td>
<td>11 bit</td>
<td>11 bit</td>
<td>13 bit</td>
<td>13bit</td>
</tr>
</tbody>
</table>

N.A.* —— Not Available.

### 4.5 Test and Debug Plan

The layout of the modulator has been completed and is ready to be included in a test chip along with the other blocks shown in Figure 4.1. To facilitate testing and debugging of the silicon, various features have been included. First of all, the dynamic power down scenario can be enabled or disabled by external control voltage through a separate pin. Second, the unit biasing current and reference voltage can be either self-generated or externally provided. Last but not least, the differential outputs of the three OTAs can be extracted and tracked separately. Via a test multiplexer, they can be fed to a pair of on-chip source-followers which can drive an off-chip load, allowing the output voltages of the OTAs to be observed on an oscilloscope without affecting the operation of the modulator.
Chapter 5

Conclusions and Future Work

This final chapter summarizes the main achievements of this thesis. It also provides an outlook to future work on energy-efficient capacitive-sensor interfaces.

5.1 Conclusions

The initial objective of this thesis was to develop an energy-efficient interface for capacitive humidity-sensors. The delta-sigma ADC has been chosen from architecture view due to its significant advantages on narrow-band signal processing, for instance its capability of providing high resolution without relying on accurately matched components and its excellent performance in terms of low power- and area-consumption. Incremental operation tailored to instrumentation and sensor applications is applied to save energy by reducing conversion time, while maintaining an excellent sample-by-sample conversion performance (with high absolute accuracy, high linearity and low offset). What’s more, the order of the loop filter in the incremental delta-sigma modulator, which is the core part of the incremental delta-sigma ADC, has been carefully chosen. Based on thorough theoretical calculation and analysis, a third-order modulator is the optimal choice for this application, since it achieves the required thermal and quantization noise levels at the minimum number of conversion cycles. As a result, a 3rd-order delta-sigma modulator with single-bit quantizer employing CIFF structure is used.

As the OTAs in switched-capacitor integrators consume most power, a power-efficient circuit should be employed. Diving into the circuit-level implementation of the OTAs in the modulator, a novel structure of current-starved, inverter-based cascode OTA has been chosen, offering better current-efficiency compared to conventional structures. Further more, compared to the simple inverter, the current-starved structure is less sensitive to non-idealities, for instance mismatch and offset resulting from variations in processing, temperature and supply voltage. As a result, advanced techniques to reduce imperfections of the OTAs such as auto-zeroing and chopper stabilization are not introduced. A dynamic power-down scenario is applied to these OTAs: fall “asleep” and save current when they just standby for the coming integration period, and “wake up” to work and consume current when sampling period is finished and integration starts.

The interface has been implemented in 0.16μm standard CMOS technology. The layout of the delta-sigma modulator, which is key to the performance of the interface,
has been completed. Post-layout simulations have been performed to verify the performance of the interface. It achieves a resolution of 13 bits in a conversion time of 0.2ms, which is adequate for the requirements for the humidity-sensing application. It consumes 5.7μA from a 1.2V supply, corresponding to an energy consumption of 1.37nJ per measurement. Compared to previous capacitive-sensor interfaces (107nJ in [16] as the prior art), the energy-efficiency is improved significantly.

Without applying the dynamic power-down approach, the modulator consumes 3.9μA (3.6μA distributed to the three OTAs), while the “supporting” circuits, including bias circuit and reference voltage generation circuit, consume 3.2μA. When the dynamic power-down scenario is applied to the OTAs in the modulator, up to 1.5μA is saved (42% of three OTAs’ current consumption and 21% of total current consumption) corresponding to a power-down clock with a 45% duty cycle. The saved amount is somewhat lower than expected, since waking up the OTAs requires extra dynamic current to charge parasitic capacitance and resettle them to their normal biasing point. The savings obtained by the dynamic power-down scenario can be improved by various means, which will be discussed in the subsequent section.

5.2 Future Work

The power down scenario is realized by the means of isolating the current-starved inverter-based cascode OTAs from the supply and ground. Though a leakage current of around 15nA exists, the bias circuit is capable to compensate for this. It can successfully wake the OTAs up and bring them to their proper bias point. However, the extra dynamic current during the settling period reduces the power saved by the dynamic power-down scenario approach. This could be improved by reducing the leakage current (enhanced isolation) and thus the dynamic recharge current.

The current distribution clearly reveals that the OTAs in the modulator, which would be dynamically powered down, consume only 55% of the total current. If the current consumption ratio between OTAs and supporting circuits is larger, the power down scenario will be more effective in improving power-efficiency. This could be implemented in two ways: one is to further reduce the current consumption of the bias circuit and the reference voltage generation circuit. In this case, however, the unit bias current of the input branch in the current-mirror that provides the tail-currents and the bias currents used to generate bias voltages (such as $V_{bp}$, $V_{bn}$, $V_{cm}$) can not be reduces, because they need to start up the OTAs rapidly. The other is to increase the current consumption that would be dynamically powered down, which means larger $g_m$ can be provided and consequently a higher clock frequency can be used. However, a higher clock frequency results in a shorter settling period, and consequently a shorter start-up time, which means the current in the supporting circuits has to be increased. Therefore, an optimum balance between the currents distributed to the modulator and the supporting circuits can be chosen to maximize the current savings.
All the discussion above focuses on improving the dynamic power-down scenario to increase energy-efficiency. As a matter of fact, many other methods can be introduced to implement a power-efficient OTA. A tree-diagram shown in figure 5.1 depicts possible solutions for low-power implementations of the OTA of a switched-capacitor integrator.

Figure 5.1: Possible solutions for low-power OTA implementation

The inverter-based OTA can be used to implement a low-voltage, low-power switched-capacitor integrator when it works in Class-C operation [11]. Folded-cascode and telescopic-cascode are prevalent structures that applied in conventional OTAs. In this work, current-starved inverter-based OTA is chosen due to the better performance in current-efficiency and robustness compared the other options used in previous designs. Cascode transistors are brought in to enhance the gain at the expense of slightly higher supply voltage. The SC circuit operates in half-delay mode and a dynamical power-down scenario is applied to further reduce current consumption. On the contrast, a dynamic biasing scenario will achieve a comparable current-efficiency if the SC circuit operates in full-delay mode. Figure 5.2 [11] shows the SC integrator operating in full-delay mode.

Figure 5.2: SC integrator using OTA in full delay mode. (a) $\phi_1$ phase. (b) $\phi_2$ phase.
Recalling (3.7), the required $g_m$ can be expressed in terms of equivalent input and load capacitances ($C_{in}$ and $C_L$) of the OTA. In the two non-overlapping clock phases ($\phi_1$ and $\phi_2$), these capacitances are different, resulting in different $g_m$ requirements. Consequently different optimal biasing currents can be used, which means the OTA can be dynamically biased in different phases. This approach is referred to as the dynamic biasing scenario. Another derivative could be dynamic clocking, which means the period assigned to the two phases can be dynamically controlled to meet the settling requirement.

Until now a clock signal is required to synchronize the clock signals in SC circuits and specify the period that used to settle down, resulting in a certain current consumption requirement. It is an external clock signal generated off-chip in this work but in a typical application that clock would be generated on chip. However, this global synchronized clock can be avoided if the integrators are able to self-detect their outputs and automatically switching when it is settled with a sufficient accuracy. No matter how low the biasing current is, the integrator would settle down. This kind of integrator is referred to as a self-timed integrator. Besides, it saves the power consumed in the clock generation circuit. Nevertheless, the application is quite limited, just suitable for instrumentation measurement and sensor applications where conversion speed is quite low.

As a summary, based on the achievements in this thesis, there is still a lot of work remaining that could be done in the future. The dynamic power down scenario can be improved to make the current saving more effective. Besides dynamic power-down, other solutions such as dynamic biasing and self-timed integrators are also interesting and worth studying in the track of current saving.
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