Electrical Analysis of Ultrashallow Junctions

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Chapter 1 Introduction

1.1 Background

As first introduced in 1970s, the Moore’s law [1], the number of transistors that can be placed inexpensively on an integrated circuit has doubled approximately every two years, has received a great success in the downscaling of microelectronic devices, particularly for complementary-metal-oxide-semiconductor (CMOS), concurrent with the speed and performance enhancement, the cost per functionality is reducing for smaller MOSFET node[2]. This success has traditionally been paced by the development of new lithography tools, masks, photoresist materials, and critical dimension etch processes[3].

With continued downward scaling, the CMOS technology is facing challenges to achieve shallower junction depth (<10 nm) to control of short channel effect while concurrently optimizing the sheet resistance, doping abruptness for source and drain extension (SDE). At the same time, making low-resistance contact to, shallow, highly-doped source/drain (S/D) regions while minimizing parasitic resistance[4].

Since the S/D regions doping profile is crucial for the performance of CMOS device, novel doping technology is emerging for making ultrashallow junctions, such as low energy ion implantation[5], chemical vapor deposition[6], selective solid-phase epitaxy[7], excimer laser annealing[8]. The characterization of ultrashallow junction becomes an important issue.

1.2 Conventional characterization techniques

Commonly used characterization techniques for doping profile such as Electrochemical Capacitance-voltage Profiler (ECV), spreading resistance, Hall effect, Optical techniques, Secondary ion mass spectrometry (SIMS), Rutherford backscattering (RBS) are detail discussed in [9]. Here only a brief description is introduced for each technique.
Electrochemical capacitance-voltage profiler has no limitation on depth and the sensitivity is good, eminently suitable for III-V materials. But it is destructive, requiring very careful sample preparation and problems may arise due to highly doped surface layers, high contact resistance or poor etching [9].

Spreading resistance profiling technique is commonly used for Si to generate resistivity and dopant density depth profiles. It has very high dynamic range \((10^{12}–10^{21} \text{ cm}^{-3})\) and is capable of profiling very shallow junctions into the nm regime. However, the profiling accuracy depends on the setting of carrier mobility in data analysis and complex sample preparation and data analysis is required too [9].

Hall Effect technique can derive the carrier type as well as the average carrier density of the sample, this is only suitable for uniformly doped samples, for non-uniformly doped samples, an average value is determined [9].

Optical technique such as infrared spectroscopy, high sensitivity is obtained from Fourier transform techniques, the detection limits are extremely low while it is contactless and nondestructive. But it operates under very low temperatures and it is not suitable for thin layers such as epitaxial layers [9].

Secondary ion mass spectrometry (SIMS) technique is the most commonly used method for dopant density profiling. It has high spatial resolution and can be used for any semiconductor. It is most sensitive for B in Si. But it only tells the chemical impurity concentration instead of the electrically active doping concentration, thus it can be used only before any activation anneals. Moreover, complex and expensive equipment is required [9].

Rutherford backscattering (RBS) technique is a non-destructive, quantitative technique without recourse to standards, it is capable of detecting activation effectiveness of implanted ions through ion channeling. But the low sensitivity and the requirement of specialized equipment is its biggest drawback [9].
In summary, all the mentioned techniques have their own limitations and most of them require complex structures or equipments

1.3 Objective

In the view of the general trends in the field of junction formation, reliable techniques of forming ultra-abrupt ultrashallow junction with consuming less energy is appreciated. Thus when developing new doping techniques, or trying to lower the thermal budget of the doping techniques, simple characterization techniques without complex equipment or structure is needed before using detail but complex characterization techniques to determine whether a Schottky diode or pn junction diode is successfully created by the doping technique.

In this thesis, two electrical characterization techniques are introduced. The two techniques are using the same, very simple structure-lateral transistor structure composes of three diodes. The three diodes are placed side by side and created in the same doping technique. With simple measurements of collector current and/or diode current, the type of the devices can be easily determined.

1.4 Outline

In Chapter 2, basic knowledge of conventional lateral bipolar transistor, the structure we used in this thesis, is introduced. Measurements and calculations showed that the one dimensional equation of collector current is still valid in the transistor compose of ultrashallow pn junctions.

In Chapter 3, “Schottky lateral transistor”, a lateral transistor composes of three Schottky diodes, is introduced. The difference in collector current between Schottky lateral transistor and normal lateral transistor is discussed. Through this difference, we can determine the type of emitter diode.
In Chapter 4, the influence of geometry and physics variables on collector current and the difference lies in the collector current are discussed. Also, the effect of deposition layer is discussed.

In Chapter 5, another method to distinguish pn diode and Schottky diode using lateral structure is introduced. Instead of collector current, we make use of the I-V characteristics of the target diode. And the transition from Schottky diode to pn diode is discussed.
Chapter 2 Basic Knowledge of Lateral Transistor

2.1 Introduction of lateral transistor

Different like vertical bipolar transistor, whose emitter, base and collector are placed vertically. The emitter and collector of a lateral bipolar transistor are created side by side on the same semiconductor surface. In this arrangement, the injected minority carriers will flow parallel to the surface, hence the name “lateral transistor” [10]. Figure 2.1(a) and 2.1(b) show the geometry of the vertical bipolar transistor and the lateral bipolar transistor with the corresponding minority carriers’ current paths. In the vertical transistor the injected carrier will flow toward the underlying collector junction, and the emitter is surrounded by the base region, which is surrounded by the collector region. While in the lateral transistor, the emitter is not completely surrounded by the collector region, and as seen from the surface, the distance between emitter and collector should be less than the diffusion length of the minority carrier in order to collect the injected carriers as much as possible.

Figure 2.1 Simple structure of vertical bipolar transistor (a) and lateral bipolar transistor (b) and the corresponding current paths of injected carriers.
2.2 Carrier transport in lateral transistor

2.2.1 The structure used in this study

The structure considered in this study is depicted in Figure 2.2, for simplicity, stripe geometry is used, where

- \( L \) Length of the emitter/collector,
- \( d \) Junction depth,
- \( W_C \) Collector width,
- \( W_B \) Intrinsic base width,
- \( W_E \) Emitter width,
- \( A_{ev} \) Vertical emitter area = \( L \times W_E \),
- \( A_{el} \) Lateral emitter area = \( L \times d \).

![Lateral transistor in stripe geometry.](image)

In this study, devices may have different fabrication techniques, which means that the parameters relate to the fabrication technique, such as junction depth \( d \), may be different.
among devices. But for a specific device, all the junctions such as emitter-base and collector-base junctions are treated in the same way, they are fabricated in the same time with the same technology, so the junctions are the same in the device. Besides, the length of emitter and collector are kept equal. For simplicity, the substrate is used as base directly, so the substrate current $I_S$ is just the base current.

And if not specified, all the measurements are performed at room temperature, i.e., $25 \, ^\circ C$ or 298 K.

### 2.2.2 Basic principle of operation

The basic operation principle of a lateral transistor is more or less the same as a normal vertical transistor. Take an nnp lateral transistor for illustration. When emitter-base (E-B) pn junction is forward-biased, and the base-collector (B-C) pn junction is reverse-biased as shown in Figure 2.3(a), this configuration is called the forward-active operation mode [11]: The E-B junction is forward-biased, the Fermi level in the p-type base region is lower than that in the n-type emitter region, compared between the energy band diagrams Figure 2.3(c) and Figure 2.3(d) we can see the barrier which holds back the large concentration of electrons in the emitter region and keeps them from flowing into the base region is now reduced, so electrons from the emitter are injected across the E-B junction into the base, these injected electrons are excess minority carriers in the base. And when those excess minority carriers diffuse across the base region into the B-C depletion region, they are swept into the n-type collector region immediately. Since the B-C junction is under reverse-biased, the electric field in the depletion region is big enough to sweep all the minority carrier electrons into the collector region, and also there is no potential barrier to stop the flow of electrons, the minority carrier electrons concentration at the edge of the B-C junction is ideally zero. So there will be a large gradient in the electron concentration as shown in Figure 2.3(b). We want as many as possible to reach the collector without recombining with any majority carrier holes in the base. For this reason, the width of the base needs to be small compared with the minority carrier diffusion length.
Furthermore, measurement shows that no matter B-C junction is reverse biased or zero biased, as shown in Figure 2.4, the lateral bipolar transistor is still in forward-active mode, the collector current and base current are nearly constant in these two situations, and the collector current is nearly constant when the reverse bias voltage of collector-base is changing as shown in Figure 2.5, the electric field is already big enough to sweep all the minority carriers that arrive at the edge of the junction at zero bias.

Figure 2.3 Biasing of an npn lateral bipolar transistor in the forward-active mode, (b) minority carrier distribution in an npn lateral bipolar transistor operating in the forward-active mode, (c) energy band diagram of npn lateral bipolar transistor under zero bias and (d) under a forward-active mode bias [11].
Figure 2.4 Base current and collector current of npn lateral transistor as a function of $V_{EB}$ when B-C junction is zero biased ($V_{CB}=0$) and reversed biased ($V_{CB}=0.5V$). The emitter diode (deposited with TiN+As, laser annealed at 1200 mJ/cm$^2$) area is 20×1 µm$^2$.

Figure 2.5 Base current and collector current of npn lateral transistor as a function of $V_{CB}$ (collector-base junction under reverse bias) when $V_{EB} = -1.0V$. The emitter diode (deposited with TiN+As, laser annealed at 1200 mJ/cm$^2$) area is 20×1 µm$^2$. 
2.2.3 Transport mechanism of lateral transistor

The emitter will inject electrons into the base region in every direction, which makes three main transport paths for injected electrons as shown in Figure 2.6, namely:

① a purely lateral flow originating from the emitter sidewall,
② a flow along curved trajectories originating from under the emitter,
③ a vertical flow originating from under the emitter.

![Figure 2.6 Carrier transport paths in a lateral transistor.](image)

Most injected electrons in path ① and ② will diffuse across the base region into the collector, which makes collector current $I_C$, and few of them will recombine with majority holes in the base and donate part of the base current $I_B$. In path ③, the injected electrons will flow to the base and finally recombine with holes.

2.2.4 Collector Current

In one-dimensional model, assuming low current operation and neglecting recombination in the intrinsic base, the collector current $I_C$ of npn lateral bipolar transistor is[12]

$$I_c = J_{nE} \cdot A \cdot \text{el} \cdot \text{csch} \left( \frac{W_B}{L_n} \right)$$  \hspace{1cm} (2.1)

$$J_{nE} = \frac{e D_n n_0}{L_n} \left[ \exp \left( \frac{e V_{EB}}{n k T} \right) - 1 \right]$$  \hspace{1cm} (2.2)

where

$J_{nE}$ \hspace{0.5cm} Electron current density of Emitter-Base Diode,

$L_n$ \hspace{0.5cm} Diffusion length of electrons,
$D_n$ Diffusion coefficient of electrons,

$n_{p0}$ Minority carrier (electron) concentration in the intrinsic base,

$V_{EB}$ Voltage between emitter and base (= applied voltage between emitter and base at low current),

$n$ Ideality factor,

$k$ Boltzmann constant,

$T$ Absolute temperature.

$csch(W_B/L_n)$ is a hyperbolic function, which is approximately equal to $L_n/W_B$, so equation (2.1) becomes

$$I_c = J_{ne} \cdot A_{el} \cdot \frac{L_n}{W_B}$$

(2.3)

### 2.2.5 Actual device

Starting from a p-type Si substrate with a surface doping of $10^{17}$ cm$^{-3}$, 400 nm of LPCVD TEOS is deposited. The contact windows are plasma-etched to Si and deposited with As monolayer. Just before the deposition, the native oxide at Si interface is removed by 4 min HF 0.55% dip etch. 30 nm TiN is sputtered at 280 °C and on top of it is 100 nm of Al LAP (Laser Annealing Protection) layer which is sputtered at 50 °C. Then the contact windows are laser annealed as illustrated in Figure 2.7(a) after the Al LAP layer is removed from the contact windows by wet etch. With enough laser annealing energy, the As interfacial layer and underneath very shallow layer of Si is melt and the As is doped into the Si. All the Al LAP is removed before metallization, the TiN layer is exposed and no need of dip etch. During the metallization, 675 nm Al/Si(1%) is sputtered at 50 °C (Figure 2.7(b)) and then the metal is patterned.
The device that being used is a ultrashallow pn junction, which is laser annealed at 1200 mJ/cm². A heavily doped n region, the donor concentration is about $1 \times 10^{19}$ cm$^{-3}$, is fabricated on a p-type wafer, which the acceptor concentration is $1 \times 10^{15}$ cm$^{-3}$, with a surface doping of $1 \times 10^{17}$ cm$^{-3}$.

The thickness of the heavily doped n region is around 10-20 nm, but the width of depletion region is about 130 nm, which is more than 10 times larger than the n-region thickness. Thus the depletion width should be taken into account during the calculation.
Figure 2.8 Schematic of lateral transistor with ultrashallow pn junctions

For the ultrashallow pn junction in our case, the hole current is small compared to the electron current, the electron current in p-type doped region dominates in diode current, so the electron current can be approximately expressed as

\[ J_{ne} = \frac{I_E}{A_{ev}} \]  

(2.4)

Then the collector current \( I_C \) is

\[ I_c = \frac{I_E}{A_{ev}} \cdot A_{el} \cdot \frac{L_n}{W_B} \]  

(2.5)

\( I_E \) is the emitter current that was measured on the emitter-base diode, \( A_{ev} \) equals to \( L \times W_E = 20 \times 1 = 20 \ \mu m^2; A_{el} = L \times d \), where \( d \) is the depletion region width, which is changing with \( V_{EB} \); \( L_n \) equals to 40–60 \( \mu m \) and \( W_B \) is 4 \( \mu m \).

Compare the calculated collector current with the measured result in Figure 2.9, the calculated current fits well with the measured value, which proves the theory is valid with lateral transistor composed of ultrashallow pn junctions.
Figure 2.9 (a) I-V output characteristic of emitter-base diode (deposited with TiN+As, laser annealed at 1200 mJ/cm²) (b) gummel plot of npn lateral transistor (c) comparison between measured and calculated collector current. The emitter area is 20×1 µm².
Chapter 3 Distinguish PN Diode and Schottky Diode by the Collector Current

Since for ultrashallow pn junctions, the active heavily doping region is very shallow, which can be as shallow as 2 nm [6]. The ultrashallow region can be easily partially or even fully depleted. The introduced method in this chapter based on the collector current of lateral transistor, from which a clear difference can be observed between the lateral transistors compose of pn junction diodes and Schottky diodes. Through the determination of the type of diode, we can determine whether there is an active doped region or not.

3.1 “Schottky lateral transistor”

If the devices are treated in the same way as described in chapter 2.2.5 but no laser annealing is applied, we will have a device in lateral transistor structure with three Schottky diodes as shown in Figure 3.1, and we call it “Schottky lateral transistor” by now.

During the measurement, collector current is observed when the “Schottky lateral transistor” is biased in forward-active mode. As shown in Figure 3.2, when the “collector” diode is reverse biased at 0.5 V, the collector current when $V_{EB}$ is small is just the reverse-bias current of the “collector” Schottky diode, as the increasing of $V_{EB}$, the “collector” current increases as well and it could be much larger than the reverse-bias current. And when $V_{EB}$ is large, the “collector” current is constant no matter the “collector” diode is reverse biased or not.

Normally we know collector current in a conventional transistor is caused by minority carriers’ behavior, but Schottky diode is a majority carrier device due to the current of a Schottky diode is from thermionic emission of majority carriers. Next, the composition of this collector current will be discussed.
Figure 3.1 Stripe geometry of “Schottky lateral transistor”.

Figure 3.2 Gummel plot of a “Schottky lateral transistor” under forward-active mode. The emitter diode (deposited with TiN+As, no laser annealing) area is 20×1 µm².
3.1.1 Introduction of Schottky collector

In conventional bipolar transistor, the collector-base junction is pn junction and the metal contact to collector is ohmic contact. If, however, a metal is employed as the collector and contacted to the base region directly, we have a Schottky diode at the collector-base junction and the collector is a Schottky collector [13].

When an npm bipolar transistor is biased in forward active mode as shown in Figure 3.3(b) just in the same way as an npn bipolar transistor in Figure 3.3(a). The E-B junctions are identical in these two situations. The injected electrons from emitter will diffuse across the base region and reach the B-C junction. For npm transistor, the electric field in the space charge region of B-C junction will sweep the minority carrier electrons into the metal which acts as a Schottky collector. So the npm transistor will collect the injected carriers from the emitter effectively just like a normal npn transistor.

![Energy diagrams of npn bipolar transistor (a) and npm bipolar transistor (b) under forward-active mode bias.](image-url)
Figure 3.4 Gummel plot of npn lateral transistor (a) and Schottky lateral transistor (b). The emitter areas are all 40×1µm².

Compare with conventional bipolar transistor, the Schottky collector transistor has many advantages.

Because of the Schottky barrier, minority carriers in the base can be collected efficiently from the metal side without significant reverse injection of majority carriers into the base. The suppression of minority carrier reverse injection from the Schottky diode collector permits the design of non-saturating inverter logic circuits with adequate performance, lower power dissipation, and high integration density [14]. And this phenomenon has been demonstrated for large dimension PNM transistors[13].

Additionally, the storage time in the collector is negligibly small, thus forming an inherently fast switch[15].

Designs similar to the n-Schottky collector device in the past have been proposed and predicted to give potentially better BJT speed performance due to the low collector resistance, transit time and storage time [16].
And the Schottky collector has been reported a significant improvement in collector breakdown voltage, which is about 12 times higher when compared with the conventional thin film lateral Schottky collector bipolar transistor on silicon-on-insulator [17].

### 3.1.2 Mechanism of Schottky diode

As described in [18], there are five basic transport processes under forward bias (the inverse processes occur under reverse bias) as shown in Figure 3.5, namely:

- **Figure 3.5 Five basic transport process under forward bias.** (1) Thermionic emission. (2) Tunneling. (3) Recombination. (4) Diffusion of holes. (5) Diffusion of electrons.

(1) emission of holes from the semiconductor over the potential barrier into the metal--the dominant process for Schottky diodes with moderately doped semiconductors, (2) quantum mechanical tunneling of holes through the barrier (important for heavily doped semiconductors and responsible for most ohmic contacts), (3) recombination in the space-charge region (identical to the recombination process in a pn junction), (4) diffusion of holes in the depletion region, and (5) electrons injected from the metal that diffuse into the semiconductor (equivalent to recombination in the neutral region).

### 3.1.3 Direction of collector current

The definition of current direction is that the positive current direction is the transport direction of holes. And if an electrode is injecting holes from the metal or injected
electrons from the semiconductor, the current direction is positive; On the contrary, if it is injected holes from the semiconductor or injecting electrons into the semiconductor, then the current direction is in negative direction.

From Figure 3.6(a) we can see the emitter current is in negative direction, which means holes are injected from the semiconductor corresponding to that E-B junction is a p-type Schottky diode in forward biased. While for the collector current in Figure 3.6 (b), the current is in positive direction, which gives us two possibilities, at the collector, the semiconductor is injecting electrons into the metal or/and injected holes from the metal.

### 3.1.4 Composition of collector current

Since the collector current is the current we got in a lateral transistor set-up when collector is under reverse bias, and from the analysis above, the collector current may compose of:

1. Emission of holes from the metal over the potential barrier into the semiconductor, which is the reverse-biased current of Schottky diodes, i.e., the inverse

![Figure 3.6 Emitter current (a) and collector current (b) in a Schottky lateral transistor set-up. Both diodes are deposited with TiN+As, and no laser annealing applied. Diode areas are 20×1 µm².](image)
process of the transport process 1 in Figure 3.5. But from Figure 3.2, the collector current is much higher than the reverse-biased current, so this is not the dominate current.

(2) Quantum mechanical tunneling of holes from the metal through the barrier into the semiconductor, i.e., the inverse process of transport process 2 in Figure 3.5. But from temperature measurement, the collector current increases with increasing temperature as shown in Figure 3.7, so the tunneling is not dominating in the collector current either, since the tunneling current should remain constant when change the temperature.

(3) Diffusion current of electrons, which are injected from emitter as shown in Figure 3.5, transport process 5. When a Schottky diode is forward biased at $V_A$, the barrier $\Phi_{Bn0}$ that prevents holes in metal from injecting into semiconductor is lowered by a value of $V_A$ as shown in Figure 3.8(a), the electric field in the space-charge region is reduced at the same time. More electrons from metal side can be injected into semiconductor and become excess minority carriers, some of the excess carriers will recombine with majority carrier holes in the p-type substrate (base), and some of them will diffuse across the base region and get out from collector. The diffusion current of electrons is possibly the main current of the collector current.

![Gummel plot of a Schottky lateral transistor under different measurement temperature.](image)

*Figure 3.7 Gummel plot of a Schottky lateral transistor under different measurement temperature. The emitter diode (deposited with TiN+As, no laser annealing) area is 20×1 µm².*
3.1.5 Device simulation

At the mean while, device simulation is processed in ISE-TCAD to further investigate the composition of collector current.

The device is created in DEVISE, as shown in Figure 3.9, start with a $1 \times 10^{15}$ cm$^{-3}$ p-type Si substrate, and the thickness of the substrate is 525 µm, same as the thickness of a 4 inch wafer, since a front-back measurement is used in the electrical measurement. The surface doping layer is 200 nm thick with $1 \times 10^{17}$ cm$^{-3}$ p-type doping. The electrical contacts are defined as follow: both emitter and collector contacts are identical, which are Schottky contact, the Schottky barrier height of the contact is 0.61 V from the I-V-T measurement (which will be discussed in Chapter 4), the back wafer contact, i.e., the base contact is an ohmic contact.
In the simulation, the emitter voltage is swept from 0 to -1 V. The base contact is biased at 0 V always, so the emitter-base voltage is just the applied emitter voltage. The collector contacts are biased at 0 or 0.5 V. In this set-up, the Schottky transistor is biased in forward-active mode.

From the simulation result of collector current in Figure 3.10, both electron and hole donate current to collector current. Electron current and hole current increase with increasing emitter-base voltage when $V_{EB}$ is small, and hole current is bigger than electron current. As $V_{EB}$ increasing, hole current reaches a limit and stop increasing, this limit is the reverse-bias current. And then the electron current keeps increasing and becomes the main current in the end when $V_{EB}$ equals to -1.0 V, device simulation is conducted to see how the electrons transport in the device.
As illustrate in Figure 3.11, the electron current flow is from collectors to emitter, so the direction of electron current is positive as described in chapter 3.1.3, which is also shown in Figure 3.6.
Figure 3.11 Simulation of electron current distribution and electron current path in Schottky lateral transistor when $V_{EB} = -1.0$ V

Figure 3.12 Closer of Schottky lateral transistor (a), emitter (b) and collector (c) and the corresponding electron transport path (red line).
So the transport direction of electrons is from emitter to collector as shown in Figure 3.12, since the transport direction of electrons is the opposite of current direction, which suggests that the electrons are came from emitter.

And from the simulation of emitter I-V output characteristics in Figure 3.13, the majority current of a p-Schottky emitter is hole current, which is consistent with the theory. Besides hole current, electron current is observed as well, and as shown in Figure 3.12(b), the electrons are injected from metal into substrate, which is corresponding with process 5 in Figure 3.5.

![Figure 3.13 I-V output characteristics of simulation of emitter Schottky diode.](image)

The injected electrons are separated into two groups, one group diffused across base region and got out from the collectors, process ① in Figure 3.12(a). Another group of electrons diffused in the substrate and then recombined with majority carrier holes, process ② in Figure 3.12(a), which is identical to the recombination process in neutral region. And the electron current of emitter, base and collector is shown in Figure 3.14.
Besides electron current, holes also donate current to collector current. As the increasing of emitter-base voltage, the emitter current is increasing too. As shown in Figure 3.15, when $V_{EB}$ equals to -1.0 V, the base-collector voltage is around -0.4 V, which means the collector Schottky diode is reverse biased at 0.4 V, this is due to the increasing current and the resistance between emitter and collector will reverse bias the base-collector diode, which makes the reverse-biased current.
And if the collectors are reverse-biased at 0.5 V from the beginning, the hole current will remain unchanged during the whole operation. As shown in Figure 3.16, when electron current is small, the collector current is mainly hole current, as the emitter-base voltage is increasing, the electron current increases too, and becomes the dominate part of the collector current.

Gummel plot of Schottky lateral transistor in simulation is plotted in Figure 3.17, it shows the same trend as the measurement result on real device in Figure 3.2, the increasing collection current of injected carriers is the dominate current of $I_C$. 
Figure 3.16 Simulation of collector current when $V_C$ is reverse-biased at 0.5 V

Figure 3.17 Gummel plot of simulation result of Schottky lateral transistor
### 3.1.6 Transport mechanism of Schottky lateral transistor

The lateral bipolar transistor behavior is observed from the simulation, the minority carrier transport paths are shown in Figure 3.18, which is nearly the same as Figure 2.6, the transport paths in normal lateral transistor, so the collector current of a Schottky lateral transistor can be described by equation (2.3)

\[ I_c = J_{nE} \cdot A_{cl} \cdot \frac{L_E}{W_B}. \]

But the lateral area of Schottky diode is really small, and the path of most injected electrons from emitter is not a purely lateral flow but a flow along curved trajectories originating from under the emitter, so the factor \( A_{cl} \) may cause inaccuracy when calculating the collector current.

Since the transistor behavior is observed in the Schottky diodes based lateral transistor structure, we can call this device “Schottky lateral transistor”. And the operation principle of a Schottky transistor is the same as conventional transistor, the emitter-base Schottky diode is forward biased, the potential barrier to prevent the electron in the metal from injecting into semiconductor is lowered as shown in Figure 3.19, so there will be more electrons injected into the p-type substrate (base) and become minority carriers, then the
injected electrons will diffuse across the base region and be collected by the collector-base Schottky diode, which makes the collector current.

![Energy diagram of Schottky lateral transistor in zero bias (a) and in forward-active mode (b).](image)

**Figure 3.19 Energy diagram of Schottky lateral transistor in zero bias (a) and in forward-active mode (b).**

### 3.2 The difference in collector current between normal transistor and Schottky transistor

From the above investigation, both the collector current of normal transistor and Schottky transistor can be described by equation (2.3). If we have npn and Schottky transistor on the same substrate, i.e., $L_n$ is identical in both transistors, and the devices are in the same geometry, so $W_B$ is equal in the two cases and ignoring the difference in $A_{el}$ due to that the lateral area is not the dominate part of the collector current and most of the collector current in a Schottky transistor is not pure lateral current. Thus the difference of collector current is determined by the electron current density $J_{nE}$.

For pn diode and Schottky diode, the current can be expressed as:
\[ I_{pn} = I_s \cdot [\exp \left( \frac{V}{nV_T} \right) - 1] \quad (3.1) \]

\[ I_{Sch} = I_{st} \cdot [\exp \left( \frac{V}{nV_T} \right) - 1] \quad (3.2) \]

where \( I_s \) and \( I_{st} \) is the saturation current for pn and Schottky diode respectively.

Substitute the exponential part of \( J_{nE} \) in equation (2.3) with equation (3.1) and (3.2), electron current density of emitter \( J_{nE} \) can be described as

\[ J_{nE} = \frac{eD_n n_p 0}{L_n} \exp \left( \frac{eV_{EB}}{nkT} \right) - 1 = \frac{eD_n n_p 0}{L_n} \frac{I_{pn}}{I_s} \quad (or \quad \frac{I_{Sch}}{I_{st}}) \quad (3.3) \]

So the difference in collector current is

\[ \frac{I_{c_{PN}}}{I_{c_{Sch}}} = \frac{J_{nE_{PN}}}{J_{nE_{Sch}}} = \frac{I_{E_{PN}}}{I_s} \quad (3.4) \]

Measurements of pn and Schottky diodes are shown in Figure 3.20, the current at -1.0 V is \( 1.2 \times 10^{-3} \) A for pn diode and \( 7.5277 \times 10^{-4} \) A for Schottky diode. To extract the saturation current, linear curve fittings are conducted to both pn and Schottky diodes on the linear region in a semi-log plot, the value of the fitted curve at 0 V is the saturation current, namely \( 5.1156 \times 10^{-14} \) A for pn diode and \( 1.3973 \times 10^{-10} \) A for Schottky diode. In this way, we can get the ideality factor from the gradient of the fitted line as well. From equation (3.4), the difference in collector current should be

\[ \frac{I_{E_{PN}}}{I_s} = \frac{1.2 \times 10^{-3}}{5.1156 \times 10^{-14}} = 4354.24 \quad \text{times.} \]

From the measurement result of collector current, as shown in Figure 3.21, the collector current of npn transistor is \( 1.678 \times 10^{-4} \) A and \( 3.521 \times 10^{-8} \) A for Schottky transistor, the difference in collector of npn transistor over Schottky transistor is 4765.69 times larger, which is approximately equal to the calculated value above.
Chapter 3 Distinguish PN diode and Schottky Diode by the Collector Current

Figure 3.20 I-V output characteristic of emitter-base (deposited with TiN+As) diode when it is a Schottky diode (no laser annealing) and a pn diode (laser annealed at 1200 mJ/cm²). The diode areas are all 20×1 µm².

Figure 3.21 Collector current of npn transistor and Schottky transistor. The emitter areas are all 20×1 µm².
3.3 The mechanism of the difference in collector current between normal transistor and Schottky transistor

From equation (3.3), the main difference in $I_C$ between normal transistor and Schottky transistor is the minority carrier current density $J_{nE}$ of emitter-base diode, which is determined by the quantity of minority carriers that the emitter can inject into the base.

The concentration of injected minority carriers at the depletion region edge of emitter-base diode for a npn transistor and a Schottky transistor on a p-type substrate which is the same as the npn transistor can be expressed as [11]:

$$\delta n_p = n_{p0} \cdot \left[ \exp \left( \frac{qV_a}{kT} \right) - 1 \right]$$  \hspace{1cm} (3.5)

where $V_a$ is the voltage drop over the E-B junction, determined by

$$V_{EB} = V_a + I_E \cdot R_s$$  \hspace{1cm} (3.6)

$I_E$ is the emitter diode current and $R_s$ is the series resistance of the substrate (base).

When the diode current is small, $V_a$ equals to the applied voltage $V_{EB}$. As $V_{EB}$ increases, $I_E$ increases simultaneously, when $I_E$ is large enough, the factor $I_E \cdot R_s$ can not be ignored, which will limit the voltage drop over the junction $V_a$. In reverse, limited $V_a$ will limit $I_E$ too, just like what we saw in Figure 3.20, the saturation region of the diode current. And for Schottky diode, the saturation current is thousands times larger than pn diode’s, which means at the same applied voltage, the current of a Schottky diode is much larger than a pn diode, so the $I_E$ of the Schottky diode saturates at smaller $V_{EB}$, thus the voltage drop $V_a$ of the Schottky diode is smaller than pn diode, according to equation (3.5), there will be less injected minority carriers, so less $I_C$ for Schottky lateral transistor.

We can also see this in the energy biagram, since $V_a$ for pn diode is larger than Schottky diode. The barrier that prevents the minority carrier from injecting into the base decreases more for pn diode, so it will be easier for the injection, more carriers will be injected into the base, thus $I_C$ is larger for npn transistor.
3.4 Conclusion

The mechanism of Schottky lateral transistor is discussed, a big gap of collector between the normal lateral transistor and Schottky lateral transistor is observed, and through this we can determine the type of the emitter diodes.

To determine the type of the emitter diodes, several routes can be used. Take the diodes fabricated by laser annealing technique for instance, compare the collector current $I_C$ at $V_{EB} = -1$ V, if a pn junction has already been got at high energy, $I_C$ of the lateral transistor form by this type of pn junctions can be set as a reference, by lowering the laser annealing energy, if the emitter diodes are still pn diodes, $I_C$ will stay close to the reference value. On the other hand, $I_C$ of the Schottky lateral transistor can also be set as reference, by increasing the energy, at the energy when the emitter diode transform into pn diode from Schottky diode, as shown in Figure 3.23, a bump increase of collector current can be observed.
Figure 3.23 Collector current of lateral transistor of which the diodes are laser annealed at different energy densities. The emitter diode (deposited with TiN+As) areas are all 20×1 µm².

Additionally, this method is only functional collector current starts to saturate, at when a stable difference between the collector current of the two type lateral transistors can be got.
Chapter 4 Characterization of Lateral Transistor

From the previous chapter we know that we can get collector current from both normal and Schottky lateral transistor, and there is a gap between the collector current of these two types of transistor. Next, the influence of geometry and physics variables on the collector current, and the effect of deposition layer will be discussed.

4.1 Influence of geometry and temperature variables

For the characterization of geometry variables of base and collector regions, the devices being used are pnp lateral transistors and Schottky lateral transistor on the same n-type substrate. For the rest of characterizations, devices are processed in the same way as mentioned in chapter 2.2.5.

4.1.1 The influence of base width

To investigate the influence of base width $W_B$ on collector current $I_C$, the author did several measurements on lateral bipolar transistor structure, as shown in Figure 4.1, with different $W_B$. The geometry of pnp transistor and Schottky transistor is identical.

![Schematic view of pnp lateral transistor and Schottky lateral transistor](image)

Figure 4.1 Schematic view of pnp lateral transistor (a) and Schottky lateral transistor (b) used to investigate the influence of $W_B$ on $I_C$.

The lateral transistor is biased under forward-active mode. The areas of emitter and collector diodes are the same, $40 \times 1 \, \mu m^2$. The collector current is listed in Table 4-1 when
emitter-base junction is forward biased at 1.0 V with $W_B$ varies from 4 to 48 µm. Base on equation (2.3), $I_C$ is inverse proportional to $W_B$, $I_C$ should increase with decreasing $W_B$, and this trend can be seen from Table 4-1 and Figure 4.2 for both pnp transistor and Schottky transistor. A clear linear relation can be seen in the plot of $I_C$ vs. $1/W_B$, which is shown in Figure 4.2. This trend is consist with equation (2.3) and it can be expressed as

$$\frac{I_C}{1/W_B} = J_{pE} \cdot A_e \cdot L_n = \text{Constant}$$  \hspace{1cm} (4.1)

The constant in equation (4.1) the slope of the linear-fit line, which is $2.95 \times 10^{-7}$ in Figure 4.2(a) and $1.02 \times 10^{-7}$ in Figure 4.2(b), and the difference between the slopes of pnp transistor and Schottky transistor is just the difference in $I_C$ when $W_B$ is equal, about 290 times, which is equal to the difference in $I_C$ between pnp and Schottky transistor as listed in Table 4-1.

![Figure 4.2 Collector current at $V_{EB}=1.0V$ of lateral PNP (a) and Schottky (b) bipolar transistor with different base width. The emitter areas are all 40 x 1 µm²](image-url)
Table 4-1 Collector current at $V_{EB}=1.0$ V of lateral PNP and Schottky bipolar transistor with different base width.

<table>
<thead>
<tr>
<th>$W_B$ [µm]</th>
<th>4</th>
<th>9</th>
<th>10</th>
<th>12</th>
<th>14</th>
<th>18</th>
<th>48</th>
</tr>
</thead>
<tbody>
<tr>
<td>IC [A]</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>PNP Transistor</td>
<td>-9.6 ×10^{-6}</td>
<td>-6.7 ×10^{-6}</td>
<td>-6.3 ×10^{-6}</td>
<td>-6.0 ×10^{-6}</td>
<td>-5.6 ×10^{-6}</td>
<td>-4.3 ×10^{-6}</td>
<td>-2.4 ×10^{-6}</td>
</tr>
<tr>
<td>Sch Transistor</td>
<td>-3.3 ×10^{-8}</td>
<td>-2.3 ×10^{-8}</td>
<td>-2.2 ×10^{-8}</td>
<td>-1.9 ×10^{-8}</td>
<td>-1.7 ×10^{-8}</td>
<td>-1.4 ×10^{-8}</td>
<td>-0.8 ×10^{-8}</td>
</tr>
<tr>
<td>Difference</td>
<td>290</td>
<td>292</td>
<td>286</td>
<td>315</td>
<td>329</td>
<td>307</td>
<td>300</td>
</tr>
</tbody>
</table>

4.1.2 The influence of collector area

The devices we used here are same as in Figure 4.1, and collectors with different area are used to see how the collector area affects the collector current.

The size of emitter is $40 \times 1$ µm² for all transistors, since emitters and collectors in all the devices have the same length, $L$ of collector is 40 µm too. Collector width $W_C$, as shown in Figure 4.3, is changing from 1µm to 40µm, namely 1, 2, 4, 6, 10, 40 µm, in this way the collector area is changing with width.

For pnp lateral transistor, the collector current is not affected by the collector area as shown in Figure 4.4. With different collector area, the change of collector current is quite
few, and it is hard to tell this difference is caused by the variation of devices or the smaller resistance between emitter and collector due to larger collector area.

![Figure 4.4 Collector current of PNP lateral transistor with different collector area. The emitter areas are all 40×1 µm²](image)

While for the Schottky lateral transistor, as shown in Figure 4.5(a), the collector current increases with increasing collector area, this may due to that the larger the area, the bigger the reverse-biased current, since the reverse-biased current is directly proportional to the area.

To rule out the influence of the reverse-bias current, pn collectors are used to replace the Schottky diode collector in Schottky lateral transistor, since the reverse bias current of pn diode is much lower compare to Schottky diode with same area. And the measurement result is shown in Figure 4.5(b), the variation of collector current with different collector areas is very small.

Thus we can draw the conclusion that the minority carrier current of collector is not affected by the collector area. But smaller collector area or smaller $W_C$ is preferred in
order to get rid of the influence of large saturation current when vertical area is big, which will influence the difference in collector current.

4.1.3 The influence of emitter geometry

(1) The influence of emitter perimeter

The perimeter of emitter will affect the collector current. The devices being used in this study are in the way that emitter and collectors are parallel with each other, most of the injected carriers that cause the collector current are injected from the sidewall of the emitter. So if the perimeter of emitter increases, the area of sidewall increases as well, there will be more carriers can reach the collector instead of recombining in the substrate, i.e., there will be more collector current.

Fist measurements are performed on lateral transistors in stripe structure like Figure 4.6(a), with same emitter area but different emitter perimeter, the length of collector is equal to emitter. The size of emitter is 20×1 µm² and 40×0.5 µm², the areas are all 20 µm² but the perimeters are 42 µm and 81 µm respectively. The measurement results are shown in Figure 4.7 for npn transistor and Figure 4.8 for Schottky transistor. For both transistors, the collector current of 40×0.5 µm² emitter is larger than the 20×1 µm² one. This is because the parallel length between emitter and collector of 40×0.5 µm² emitter is two times longer than the 20×1 µm² emitter, hence the sidewall area, i.e., the lateral area

![Collector current of Schottky lateral transistor (a) and Schottky transistor with pn junction collector (b). The emitter areas are all 40×1 µm²](image-url)
of emitter that faces to collector, is larger of 40×0.5 µm² emitter, and collector current is directly proportional to lateral area of emitter, so the collector current will be bigger with larger $A_e$.

![Figure 4.6 Lateral transistor in stripe structure (a) and ring structure (b)](image)

Figure 4.6 Lateral transistor in stripe structure (a) and ring structure (b)

![Figure 4.7 I-V output characteristics of emitter-base pn diode (deposited with TiN+As, laser annealed at 1200 mJ/cm²) and collector current of npn lateral transistor with same emitter area but different emitter perimeter.](image)

Figure 4.7 I-V output characteristics of emitter-base pn diode (deposited with TiN+As, laser annealed at 1200 mJ/cm²) and collector current of npn lateral transistor with same emitter area but different emitter perimeter.
Figure 4.8 I-V output characteristics of emitter-base Schottky diode (deposited with TiN+As, no laser annealing) and collector current of Schottky lateral transistor with same area but different perimeter.

To further investigate the influence of perimeter, ring structure lateral transistor as shown in Figure 4.6 is used. Since for stripe structure, not all the injected carriers from side wall will be collected by the collector, as shown in Figure 4.9, part of them will inject into substrate (base) and recombine with minority carriers. Different like stripe structure, the emitter in ring structure is surrounded by the collectors, so all the carriers which are injected from the sidewall of emitter will be collected by the collectors.

Figure 4.9 Top view of carrier transport paths of stripe lateral transistor.

The lateral transistors which are used have same area, around 400 µm$^2$, and the perimeter of the rectangular emitter is 100 µm, which is much smaller than the ring emitter, 860.7
μm. The measurement results are shown in Figure 4.10 and Figure 4.11. It clearly shows that the collector current in ring structure is larger than in stripe structure.

![Figure 4.10 I-V output characteristics of emitter-base pn diode (deposited with TiN+As, laser annealed at 1200 mJ/cm²) and collector current of npn lateral transistor with same emitter area, different emitter perimeter in different geometry.](image)

![Figure 4.11 I-V output characteristics of emitter-base Schottky diode (deposited with TiN+As, no laser annealing) and collector current of Schottky lateral transistor with same emitter area, different emitter perimeter in different geometry.](image)

(2) The influence of emitter area

As which was depicted above, the collector current can be determined by equation (2.3) and (3.3), since all the devices are treated in the same way, the only variables in equation (2.3) and (3.3) are $I_E$ and $I_s$ or $I_{st}$. From the measurements in Figure 4.12 and Figure 4.13, the $I_s$ or $I_{st}$ increases more than $I_E$ at -1.0 V with increasing area, so according to equation
(2.3) and (3.3), the larger the emitter area, the smaller the collector current, which is proved in figures as well.

![Figure 4.12 I-V output characteristics of emitter-base pn diode (deposited with TiN+As, laser annealed at 1200 mJ/cm²) and collector current of npn lateral transistor with different perimeter in stripe geometry with different emitter areas.](image)

![Figure 4.13 I-V output characteristics of emitter-base Schottky diode (deposited with TiN+As, no laser annealing) and collector current of Schottky lateral transistor with different perimeter in stripe geometry with different emitter areas.](image)

The measurements are also did on ring structure lateral transistors, the geometry is listed in Table 4-2, these ring structure transistors have same equal but different areas. As shown in Figure 4.14 and Figure 4.15, the collector current decreases with increasing area.

<table>
<thead>
<tr>
<th>Ring width [µm]</th>
<th>2</th>
<th>3</th>
<th>4</th>
<th>5</th>
<th>6</th>
<th>7</th>
<th>8</th>
</tr>
</thead>
<tbody>
<tr>
<td>Perimeter [µm]</td>
<td>860.7</td>
<td>860.7</td>
<td>860.7</td>
<td>860.7</td>
<td>860.7</td>
<td>860.7</td>
<td>860.7</td>
</tr>
<tr>
<td>Area [µm²]</td>
<td>215.1</td>
<td>430.3</td>
<td>860.7</td>
<td>1721.5</td>
<td>2582.3</td>
<td>4303.9</td>
<td>17215.9</td>
</tr>
</tbody>
</table>
4.1.4 Influence of temperature on collection current

Finally, although the emitter geometry will affect the collector current a little bit, the difference in $I_C$ for the devices have same geometry is still in the same order.

The measurement results of collector current with increasing measurement temperature are shown in Figure 4.16 for npn lateral transistor and Figure 4.17 for Schottky transistor.
For npn transistor, the collector current at -1.0 V does not change much with temperature. But for Schottky transistor, the temperature has a big influence on the collector current.

As shown in Figure 4.17, the reverse-bias voltage of collector will not affect the collector current. When the temperature is low, such as 273 K and 298 K, the collector current at -1.0 V is much larger than the reverse-bias current. While increasing temperature, the reverse-bias current increases much more rapidly than the collection current. When the temperature is high, the dominate current of collector current is already reverse-bias current.

And when the temperature is as low as 243 K (-30 °C), a clear linear region of collector current is observed as shown in Figure 4.18, which is another proof that the collector current of Schottky transistor has the same mechanism as the collector current of normal npn transistor.

![Figure 4.16 Collector current of npn lateral transistor under different measurement temperature. The emitter diode (deposited with TiN+As, laser annealed at 1200 mJ/cm²) area is 20×1 µm²](image-url)
Figure 4.17 Collector current of Schottky lateral transistor under different measurement temperature. The emitter diode (deposited with TiN+As, no laser annealing) area is 20×1 µm²

Figure 4.18 Gummel plot of Schottky lateral transistor at 243 K (-30 °C), V_C=0 V. The emitter diode (deposited with TiN+As, no laser annealing) area is 20×1 µm²
4.2 Influence of deposition layer on Schottky lateral transistors and Schottky diodes

During laser annealing process, the energy is out of control, there is a big fluctuation of the applied laser annealing energy from the target value and the part of the TiN layer is removed due to the extreme high laser energy. Before metallization, HF dip etch is applied to remove the native oxide since the As layer is exposed to air at the region where TiN is removed.

Since the TiN layer, which is deposited by PVD sputtering, is non-conformal. After metallization, in some region, especially at the edges of the contact windows, the Al directly lands on the Si substrate and acting as Schottky diodes which give higher current at the all bias regime compare to TiN Schottky diodes and pn junctions with same dimension. And the rough interface between metal and semiconductor will cause many surface states which will act as recombination centers. Due to these reasons, the performance of the devices on this wafer is poor.

4.2.1 Measured results of npn lateral transistor

During the measurements over npn lateral transistors, as described by equation (2.3), collector current is determined by the ideality factor of the emitter diode. When the ideality factors are nearly constant for the two diodes, the collector current is nearly the same, despite of the fact that there is almost 10 times difference between the leakage current levels, which is shown in Figure 4.19. On the other hand, compare the two diodes with same leakage current level but different ideality factor, as shown in Figure 4.20, the more close to 1 of the ideality factor, the bigger the collector current.
Figure 4.19 pn junction diodes (Emitter to Substrate) with nearly same ideality factor but different leakage level current and the corresponding collector current. The emitter diode (deposited with TiN+As) areas are all 40×1 µm².
4.2.2 Measured results of Schottky lateral transistor

But when Emitter-Base diode is Schottky diode, the collector current is mainly determined by the leakage current level (Figure 4.21) instead of ideality factor (Figure 4.22). When two diodes have same leakage current level, we will get same collector current no matter the ideality factors are same or not, which is not consistent with equation (2.3).
Figure 4.21 Schottky diodes (Emitter to Substrate) with nearly same ideality factor but different leakage current level and the corresponding collector current. The emitter diode (deposited with TiN+As) area is 40×1 µm².
Figure 4.22 (a) Schottky diodes (Emitter to Substrate) with nearly same leakage current level but different ideality factor and the corresponding collector current (b). The emitter diode (deposited with TiN+As) area is 40×1 µm².

To determine why the $I_C$ of Schottky lateral transistor is influenced by the leakage current in these devices, the effect of the deposition layer needs to be investigated.

### 4.2.3 Methods to extract SBH

For a p-type Schottky diode, the current density $J_{Sch}$ is determined by thermionic emission and can be expressed as [2]

$$J_{Sch} = J_{st} \left[ \exp \left( \frac{qV}{kT} \right) - 1 \right]$$  \hspace{1cm} (4.3)

where

$$J_{st} = A^* T^2 \cdot \exp \left( -\frac{q\phi_{bp}}{kT} \right)$$  \hspace{1cm} (4.4)
is the saturation current density, $\Phi_{Bp}$ is the Schottky barrier height, $A^*$ is the effective Richardson constant, $T$ is the absolute temperature, $q$ is the elementary charge and $k$ is the Boltzmann’s constant.

To extract the Schottky barrier height (SBH), two methods are used in this thesis, one is the I-V method, using equation (4.4), the SBH can be calculated as follow,

$$\phi_{Bp} = \frac{kT}{q} \ln \left[ A^* \cdot \frac{T^2}{J_{st}} \right]$$

(4.5)

Besides, the I-V-T method is used too. The relation of between SBH and diode electrical characteristics can be obtained from equation (4.3), the SBH can be expressed as

$$\phi_{Bp} = \frac{\log \left( \frac{J}{T^2} \right) \cdot k}{1/T} - V_A$$

(4.6)

$V_A$: The voltage applied on the metal side of a P-Schottky diode

### 4.2.4 Effect of the deposition layer on surface states

When metal is making intimate contact with a semiconductor, a barrier will be formed at the metal-semiconductor interface, and the general expression of the barrier height is

$$q\phi_{Bp0} = E_g - q(\phi_M - \chi)$$

(4.7)

for p-type Schottky. But from the previous studies, the barrier height may not simply follow the expression, there are some variations from the theoretical values that be calculated by equation (4.7). This is because that the barrier height is not only determined by work function, but also the semiconductor surface or interface states.

Although we try to make perfect contact between metal and semiconductor, but the presence of interface states is unavoidable, a more detailed energy diagram of a metal to p-type semiconductor contact in thermal equilibrium is shown in Figure 4.23.
Figure 4.23 Energy diagram of p-type Schottky with interface-trap charge

Figure 4.23 shows some acceptor states above $q\Phi_0$ and below $E_F$, these states are acceptor states, which will tend to contain electrons and will be negatively charged. If we neglect the surface states, the Schottky barrier height simply is

$$q\phi_{bp0} = E_g - q(\phi_M - \chi)$$

If the surface states can not be neglected, the expression of Schottky barrier height becomes to

$$q\phi_{bp0} = q\Phi_0$$  \hspace{1cm} (4.8)

In this case the Fermi level at the interface is pinned by the surface states at the value $q\Phi_0$ above the valence band. The barrier height is independent of the metal work function and is determined entirely by the surface properties of the semiconductor.

The measurement result on p-type Schottky diodes is listed in Table 4-3, and shown in Figure 4.24, for both aluminum and titanium Schottky diodes, the diodes with arsenic interfacial layer give a higher Schottky barrier height compared to the ones without
interfacial layer. And for Schottky diodes with aluminum, there are no distinguishable linear regions as shown in Figure 4.24, so the I-V-T method can not be performed, and the SBH in I-V method is extracted at 273 K, the I-V-T results for diodes with Ti are shown in Figure 4.25.

Table 4-3 Measured result of SBH for p-type Schottky diodes

<table>
<thead>
<tr>
<th>SBH-Φ_{BP0} (V)</th>
<th>Al only</th>
<th>Al+As</th>
<th>Ti only</th>
<th>Ti+As</th>
</tr>
</thead>
<tbody>
<tr>
<td>I-V</td>
<td>0.35</td>
<td>0.36</td>
<td>0.56</td>
<td>0.59</td>
</tr>
<tr>
<td>I-V-T</td>
<td>---</td>
<td>---</td>
<td>0.59</td>
<td>0.61</td>
</tr>
</tbody>
</table>

Figure 4.24 Measured I-V characteristics of Al and Ti on p-type semiconductor, compared to diodes with As deposition layer. The diode areas are all 40×1 µm².
And as shown in Figure 4.26, in a transistor, emitter with higher $\Phi_{Bp}$ gives higher collector current. This is due to that $q(\Phi_{Bp} + \Phi_{Bn})=E_g$, $\Phi_{Bn}$ can be considered as the barrier to prevent the electrons in the metal from injecting into semiconductor. So if $\Phi_{Bp}$ is higher, then $\Phi_{Bn}$ will be lower, thus the electrons in the metal can be injected into semiconductor more easily, so the collector current will be larger.
Figure 4.26 Measured collector current in Schottky transistor set-up. The emitter areas are all 40×1 µm².

While for metal on n-type semiconductor, the Schottky diodes with interfacial layer give lower Schottky barrier height which is listed in Table 4-4, thus the saturation current is higher in Figure 4.27.

Table 4-4 Measured result of SBH for n-type Schottky diodes

<table>
<thead>
<tr>
<th>SBH-Φ_{Bn0} (V)</th>
<th>Al only</th>
<th>Al+As</th>
<th>Ti only</th>
<th>Ti+As</th>
</tr>
</thead>
<tbody>
<tr>
<td>I-V</td>
<td>0.78</td>
<td>0.66</td>
<td>0.52</td>
<td>0.51</td>
</tr>
<tr>
<td>I-V-T</td>
<td>0.68</td>
<td>0.61</td>
<td>0.45</td>
<td>0.44</td>
</tr>
</tbody>
</table>
Figure 4.27 Measured I-V characteristics of Al and Ti on n-type semiconductor, compared to diodes with As deposition layer. The diode areas are all 40×1 µm².

Figure 4.28 I-V-T temperature dependent characteristics of Schottky diodes with and w/o deposition layer
For Schottky lateral transistor on n-type substrate, the collector current is mainly due to the diffusion of holes. If the SBH of n-Schottky diode is higher, than the barrier for holes in the metal to inject into the semiconductor is lower, thus the collector current is higher when the SBH of emitter is lower in Figure 4.29.

![Graph showing collector current vs. emitter-base voltage with different materials and with or without As deposition.](image)

**Figure 4.29** Measured collector current in Schottky transistor set-up. The emitter areas are all 40×1 µm².

The results agree with the established theory that arsenic layers passivate the acceptor-like surface states and enhance the donor-like surface states, thus lowering the Schottky barrier height for n-Schottky and raising the Schottky barrier height for p-Schottky.

### 4.2.5 Modulation of Schottky barrier height

Furthermore, the barrier height can be modified due to image-force lowering.

Figure 4.30 shows the idealized controlled barrier contacts with a thin n+-layer on a p-type substrate for barrier increase.
For a normal Schottky diode with no extra doping, the electrical field is

\[ E(x) = \frac{qN_a}{\varepsilon_s} (W - x) \quad 0 \leq x \leq W \]

When an extra n+-layer is doped in to the p-type substrate, then

\[ E(x) = -E_m + \frac{qN_d}{\varepsilon_s} x \quad 0 \leq x \leq a \]

\[ = \frac{qN_d}{\varepsilon_s} (W - x) \quad a \leq x \leq W \]
\[ E_m = \frac{q}{\varepsilon_s} \left[ N_d \cdot a - N_a (W - a) \right] \] is the maximum value of electrical field.

When \( E(x) = 0 \), electrical potential \( \phi(x) = -\int E(x)dx \) reaches maximum, so when

\[
x = \frac{1}{N_d} \left[ N_d a - N_a (W - a) \right], \quad E = 0,
\]

\[
\phi(x) = -\int E(x)dx = \phi_{Bp0} + E_m \cdot x - \frac{qN_d}{2\varepsilon_s} \cdot x^2
\]

The change in SBH is \( \Delta \phi_{Bp} = E_m \cdot x - \frac{qN_d}{2\varepsilon_s} \cdot x^2 \), which is determined by the factor \( N_d \cdot a \).

The higher of \( N_d \cdot a \), the higher of \( \Phi_{Bp} \).

And this conclusion can be seen in Figure 4.31, with increasing laser annealing energy, more arsenic will be doped into the substrate and be doped deeper, since the \( N_d \) is constant, \( 1 \times 10^{19} \text{ cm}^{-3} \) in this case, the factor \( N_d \cdot a \) will be bigger, thus \( \Phi_{Bp} \) will be larger too, the reverse-bias current is lower with increasing laser annealing energy.

Also the Schottky barrier height under different laser annealing energy densities and the doping depth which is calculated by the equation above are listed in Table 4-5, which also shows that the larger the laser annealing energy, the deeper the doping depth, the larger the Schottky barrier height.

<table>
<thead>
<tr>
<th>Laser annealing energy density [mJ/cm²]</th>
<th>0</th>
<th>600</th>
<th>700</th>
<th>800</th>
<th>900</th>
</tr>
</thead>
<tbody>
<tr>
<td>( \Phi_{Bp} ) [eV]</td>
<td>0.6156</td>
<td>0.6532</td>
<td>0.7356</td>
<td>0.7644</td>
<td>0.8280</td>
</tr>
<tr>
<td>Doping depth [nm]</td>
<td>0</td>
<td>3.09</td>
<td>4.11</td>
<td>4.54</td>
<td>5.37</td>
</tr>
</tbody>
</table>
Figure 4.31 Diode current of p-Schottky (deposited with TiN+As) with different laser annealing energy densities. The diode areas are all 20×1µm²

So the reason why the collector current of this Schottky lateral transistor is determined by the leakage current level is clear. During laser annealing process, the energy density is much higher than the target value (0 mJ/cm²), the overheat will melt part of the arsenic deposition layer, the melted arsenic will dope into the substrate, as described above, the doping will increase the Schottky barrier height, and the diode current is

\[ I_{sch} = I_{st} \cdot \exp\left( \frac{V_A}{nV_T} \right) - 1 = I_{st} \cdot \exp\left( \frac{V_A - I_{sch} \cdot R_s}{nV_T} \right) - 1 \]

when diode current is high, the series resistance will consume some applied voltage and limit the diode current, since the diode being measured are on the same substrate, the series resistance for every diode should be constant, the diode current level of every diode at -1.0V is around the same level, which also can be observed from the measurement results in Figure 3.1-4. Thus although a diode has a higher ideality factor, the leakage current may be lower, and from Chapter 4, the collector current of transistors on the same substrate is also determined by \( I_E/I_{st} \), so the collector current might be higher with higher leakage current but lower ideality factor.
For pn junctions, all the arsenic are doped into the substrate, the difference of leakage current is mainly determined by how many recombination centers are created during the laser annealing process due to the energy fluctuation, and the more the recombination centers, the higher the ideality factor.

4.3 Conclusion

The difference in collector current between normal transistor and Schottky transistor is discussed. If the geometry variables are changed, although there is some variation for specific device, the difference in $I_C$ for devices with same geometry will remain in the same order when the reverse current of collector is small. And the temperature has a big influence on the collector on Schottky lateral transistor, thus lower temperature is preferred.

And the influence of the deposition layer is discussed. Fist the As deposition layer can passivate the acceptor-like surface states and enhance the donor-like states. And the doping by the deposition layer can modulate the SBH. Furthermore, higher of the SBH for majority carriers, the lower the barrier for minority carriers will be, and the collector current will be larger.
Chapter 5 Distinguish PN Diode and Schottky Diode by the Diode Current

The method which is introduced in previous chapters to distinguish between pn junction diode and Schottky diode is only valid when collector current starts to saturate due to the series resistance effect of emitter-base junction, this is because a stable multiple can only be observed in the saturation region of the collector current.

In this chapter a new, simple method will be introduced to distinguish between pn diode and Schottky diode base on the diode current in the linear region of I-V semi-log plot.

5.1 I-V measurement results for pn diode and Schottky diode

The measurement setup for pn diode is shown in Figure 5.1, the structure is the same as lateral transistor we used in previous chapters. First only the target diode, the middle diode among the three, is biased and the bilateral diodes are not contacted as shown in Figure 5.1(a), the diode current $I'$ of the target diode is measured. Then all the three diodes are biased simultaneously as shown in Figure 5.1(b), but only the diode current $I''$ of the target one is measured. Compare the current values that we got from the target diode in two steps, the current in the second step is much lower than in the first step as shown in Figure 5.2.

Same measurements are performed on Schottky diode as shown in Figure 5.3 and the target diode current $I'$ when only bias the target diode and $I''$ when bias the three diodes at the same time are measured. From the measurement result in Figure 5.4, the current in the two steps is constant in the linear region.
Figure 5.1 Measurement setup for pn junction diode and minority carriers’ diffusion paths. The solid line is the path of the target diode.

Figure 5.2 Current of target diode when only bias the target diode $I'$, and bias the three diodes simultaneously $I''$, the target diode is a pn junction diode. The diode (deposited with TiN+As, laser annealed at 1200 mJ/cm$^2$) area is $20\times1\mu m^2$. 
Figure 5.3 Measurement setup for Schottky diode and thermionic emission paths for majority carriers. The solid line is the path of the target diode.

Figure 5.4 Current of target diode when only bias the target diode $I'$, and bias the three diodes simultaneously $I''$, the target diode is a p-type Schottky diode. The diode (deposited with TiN+As, no laser annealing) area is $20 \times 1 \mu m^2$. 
5.2 Mechanism of the diode current deviation

Compare the measurement result between pn diode and Schottky diode, we found for pn diodes, the current of bilateral diodes will influence the current of the target diode, while the bilateral diodes have no influence on the target diode current for Schottky diodes.

For pn junction diode, the main current is minority carriers’ diffusion current when the forward applied voltage is small. Under forward bias, the n-region of the diode injects electrons into the p-type substrate. The injected electrons diffuse in the substrate and recombine with majority carrier holes at the end, which makes the electron diffusion current. The electron diffusion current density can be expressed as

\[ J_n(x) = qD_n \left. \frac{d(\delta n_p(x))}{dx} \right|_{x=0} \]  \hspace{1cm} (5.1)

where \( \delta n_p(x) \) is the excess minority carrier electrons’ concentration. The 0 point in Figure 5.5 is the edge of depletion region from the p-type side. At \( x=0 \),

\[ \delta n_p(0) = n_{p0} \cdot \left[ \exp \left( \frac{qV_a}{kT} \right) - 1 \right] \]  \hspace{1cm} (5.2)

where \( V_a \) is the forward-bias voltage over the diode and \( n_{p0} \) is the minority carrier electrons’ concentration in thermal equilibrium.

From equation (5.1), we can see that the electron current is determined by the factor \( d(\delta n_p(x))/dx \), which is the gradient of excess minority carrier electrons’ concentration. When only forward bias the target diode, the minority carriers’ transport path is shown in Figure 5.1(a), which is the same as we get from the text books and the excess minority carriers’ distribution is \( \delta n_p(x) \) in Figure 5.5. On the other hand, when apply the same voltage to all the three diodes, all the n-type regions will inject electrons to the substrate. For certain regions, the distribution of injected electrons will overlap with each other (Figure 5.1(b)) and the concentration of electrons will be higher than the situation when only the target diode is biased, thus the gradient of excess minority carriers’ concentration is lowered, and lower the diode current of the target diode.
Figure 5.5 Minority carriers distribution in the substrate when only bias the target diode and bias the three diodes at the same time.

For Schottky diodes, the main current is thermionic emission current of majority carrier holes, which is emitted from semiconductor into metal as shown in Figure 5.3. No matter the bilateral diodes are biased or not, there is no influence on the emission of the target diode, so the diode current is constant in the two situation.

If we define the deviation of diode current is

$$\Delta = \frac{I' - I''}{I'} \times 100\% \tag{5.3}$$

Then the deviations for diodes fabricated as chapter 2.2.5 with different laser annealing energy densities are listed in Table 5-1 when diodes are forward biased at -0.1V, -0.3V and -0.5V, the deviations are calculated only when the diode current is in the linear region.

<table>
<thead>
<tr>
<th>Energy density (mJ/cm²)</th>
<th>0</th>
<th>600</th>
<th>700</th>
<th>800</th>
<th>900</th>
<th>1000</th>
<th>1100</th>
<th>1200</th>
</tr>
</thead>
<tbody>
<tr>
<td>-0.1V</td>
<td>2.2%</td>
<td>0.2%</td>
<td>1.8%</td>
<td>0.3%</td>
<td>3.1%</td>
<td>110.7%</td>
<td>102.6%</td>
<td>95.7%</td>
</tr>
<tr>
<td>-0.3V</td>
<td>--</td>
<td>0.4%</td>
<td>0.6%</td>
<td>0.4%</td>
<td>1.2%</td>
<td>94.2%</td>
<td>95.9%</td>
<td>90.1%</td>
</tr>
<tr>
<td>-0.5V</td>
<td>--</td>
<td>--</td>
<td>--</td>
<td>--</td>
<td>--</td>
<td>76.5%</td>
<td>78.1%</td>
<td>80.0%</td>
</tr>
</tbody>
</table>
Figure 5.6 Diode (deposited with TiN+As) current of diodes with different laser annealing energy densities. The diode areas are all 20×1µm²

From Table 5-1, we can see that for diodes with laser annealing energy densities from 0 to 900 mJ/cm², the deviation is few percent, these diodes are Schottky diodes when the applied voltage is small. But for diodes with energy densities from 1000 to 1200 mJ/cm², the deviation is several dozens percent or even more than 100%, these diodes are pn junction diodes. The difference between pn diodes and Schottky diodes is very obvious.

### 5.3 Transition from Schottky diode to pn diode

For diodes with laser annealing energy densities from 700 to 900 mJ/cm², although in Figure 3.23, the diodes are pn junction diodes, from the discussion above, they are still Schottky diodes when the applied voltage is small. Thus these diodes showed a transition from Schottky diodes to pn diodes.
For instance, I-V characteristics of diode which is laser annealed at 900 mJ/cm$^2$ is shown in Figure 5.7(a) and a comparison with diodes annealed at 0 and 1200 mJ/cm$^2$, which are Schottky diode and pn diode at all bias regime respectively is shown in Figure 5.7(b).

Figure 5.7 (a) I-V characteristics of diode annealed at 900 mJ/cm$^2$ and (b) comparison with Schottky diode and pn diode. The diode (deposited with TiN+As) areas are all 20×1µm$^2$. 
From Figure 5.7(a), we can see that in small forward regime, the diode current increases exponentially with applied voltage. When increasing the forward bias voltage, the diode current starts to saturate at point ①, which is before point ② (Figure 5.7(b)) when the series resistance start to limit the diode current. This is because that for real device, the doping profile is not uniform, the doping depth is shallower at the edges than at the middle region since the heat at the edges will be conducted to the substrate faster. When forward bias the diode, the depletion region becomes smaller with increasing bias voltage, at a point, the depletion region width is smaller than the doping depth, and then this region is un-depleted and acting as a pn diode. And with continue increasing the bias voltage, the effective area of Schottky diode is smaller and smaller, the effective area of pn diode is larger and larger. Since at the same bias voltage, diode current of pn diode is smaller than Schottky diode, the diode current increases slowly with increasing bias voltage. At the end, most region of the device is un-depleted and behaves exactly as a pn diode (Figure 5.7(b)).

And the I-V characteristics of diodes which are annealed at 800 mJ/cm² are shown in Figure 5.8. For smaller dimension diode, 2×1 µm², the I-V curve is typical for p-type Schottky diode. For the diodes 20×1 µm² and 40×1 µm², we can see the clear transition from Schottky diode into pn diode, just like what is discussed above. For larger dimension diode, 40×2 µm², the I-V curve in forward bias regime is like a pn junction diode.
The reason for this phenomenon is that during the laser annealing process, the Si substrate acts like a heat sink, which will extract heat from the annealed region. For small dimension devices, more percentage of heat will be conducted to the substrate than the large dimension devices. Thus for large dimension devices, more arsenic in the deposition layer will be melt and doped into substrate, and it will be doped deeper, so for large dimension devices, it may require lower energy to form pn diodes than the small devices.

**5.4 Conclusion**

Through the deviation of the linear region of the target diode current, the type of the diode can be determined easily.
But this method is only valid in the linear region of diode current. Since \( V_{app} = V_a + I_D R_s \), where \( V_{app} \) is the external applied voltage, \( V_a \) is the voltage drop on the diode, \( I_D \) is the diode current and \( R_s \) is the series resistance. When bias the three diodes simultaneously, the diode current is the sum of the three diode current, so the voltage drop on each diode \( V_a \) is lowered when \( R_s \) takes effect, thus the current is smaller for both pn diode and Schottky diode.

And the transition from Schottky diode to pn diode is observed. The dimension of the devices also has impact on the formation of ultrashallow junctions.
Chapter 6 Conclusions and Recommendations

6.1 Conclusions

To determine whether active doping regions are present in the devices, or whether the devices are pn diodes or Schottky diodes, two methods based on the current-voltage measurements are introduced. These two methods can identify the type of the diode at different forward bias regimes and they are based on the same structure—lateral transistor structure. In the following, the main conclusions of this thesis are summarized.

First, the published theory for conventional lateral transistor which is formed by deep pn junction diodes is still valid for the lateral transistor formed by ultrashallow pn junction diodes. And this equation can also be applied to the collector current of Schottky lateral transistor, it is proved by device simulation that the Schottky emitter will inject carriers to the base and the injected carriers can be collected by the collector. Through the big difference in collector between Schottky transistor and normal transistor, the type of the diodes can be determined.

Except the influence of collector diode reverse current, geometry variables and temperatures won’t affect the difference in collector current, the collector of Schottky transistor and normal transistor change in the same manner which is consistent with the one dimensional collector current equation. Use smaller collector area and measure at low temperature can get rid of the influence of reverse current.

At last, the type of the diode is determined by the diode current. The diode current of pn diodes is strongly influenced by the bilateral diodes, and this influence is not observed for Schottky diodes. Pn junction can be formed at lower laser annealing energy for large dimension devices.
6.2 Recommendations

The future work about the techniques to determine whether a doping layer is formed is mainly to increase the detection sensitivity.

Detection of the existence of doped layer is a challenge. As the scaling of the devices, the doping depth should be smaller and smaller, but the shallow doped region can be easily depleted by the metal-semiconductor depletion region and the depletion at the pn junction interface. For the devices we already have, very shallow doped region may be already created even when no laser annealing is applied, thus the sensitivity needs to be improved.

To increasing the sensitivity, possibly methods are employing pn junction diode collector; measuring at very low temperature; optimizing measurement structure, conventional vertical bipolar transistor may give a better sensitivity performance, the target region is the emitter-base junction, or we can find a way to combine the two introduced techniques in this thesis, to give a better sensitivity performance.
Bibliography


Summary

Title: Electrical analysis of ultrashallow junctions
By: Lin Qi

With continued downward scaling, it has become a great challenge to form ultrashallow junctions and low-ohmic contacts that meet all the requirements. The ultrashallow region can be easily partially or even fully depleted. The introduced methods in this thesis can easily determine whether the diodes are Schottky diodes or pn diodes by simple current-voltage measurements. Through the determination of the type of diode, we can determine whether there is an active doped region or not.

In Chapter 2, basic theory of lateral transistor is introduced. The structure we used in this thesis is the lateral transistor structure which composes of three diodes, and the three diodes are placed side by side. And the published theory for conventional lateral transistor which is formed by deep pn junction diodes is still valid for the lateral transistor formed by ultrashallow pn junction diode.

In Chapter 3, Schottky lateral transistor is introduced. For p-Schottky diode at forward bias regime, besides the hole current by thermionic emission, it also injects electrons from the metal into the semiconductor. Thus in the lateral transistor which composes of three Schottky diodes, collector current is got during the measurement, which is also proved by device simulation. Through the big difference in collector between Schottky transistor and normal transistor, the type of the diodes can be determined.

In Chapter 4, characterization of lateral transistor shows that except the influence of collector diode reverse current, geometry variables and temperatures won’t affect the difference in collection current, the collector of Schottky transistor and normal transistor change in the same manner. Thus smaller area and low temperature is preferred to get rid of the influence of reverse current. Also, the As deposition layer can passivate the acceptor-like surface states and enhance the donor-like surface states. And the modulation of Schottky barrier height is discussed.
In Chapter 5, the type of the diode is determined by the diode current. For Schottky diode, the target diode current remains the same no matter the bilateral diodes are biased or not; while for pn junction diode, the deviation is very big. And during the fabrication of ultrashallow junction pn diode, dimension is also an important issue to be considered, measurements shows that less energy is required for large dimension devices.
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