A Pitch-Matched ASIC with Integrated 65V TX and Shared Hybrid Beamforming ADC for Catheter-Based High-Frame-Rate 3D Ultrasound Probes

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A hybrid beamforming ADC for catheter-based high-frame-rate 3D ultrasound probes

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Intra-cardiac echocardiography (ICE) probes (Fig. 32.2.1) are widely used in electrophysiology for their good procedure guidance and relatively safe application. ASICs are increasingly employed in these miniature probes to enhance signal quality and reduce the number of connections needed in mm-diameter catheters [1-5]. 3D visualization in real-time is additionally enabled by 2D transducer arrays with, for each transducer element, a high-voltage (HV) transmit (TX) port, to generate acoustic pulses of sufficient pressure, and a receive (RX) path, to process the resulting echoes. To achieve the required reduction in RX channels, micro-beamforming (μBF), which merges the signals from a subarray using a delay-and-sum operation, has been shown to be an effective solution [3,4]. However, due to the frame-rate reduction that is associated with μBF, these designs cannot serve emerging high-frame-rate imaging modes (~1000 volumes/s) like 3D blood-flow imaging and transducer center frequency. Finally, the time-domain plots in Fig. 32.2.4 show 65V pulsing and a demonstration of the TGC in one PE cycle, confirming the availability of the full DR for high frame-rate imaging.

As shown in Fig. 32.2.5, a transducer array is directly mounted on top of the ASIC. To enable manufacturing on the small prototype, the chip is enlarged and two dummy element rings are included. For acoustic measurements, the assembly is immersed in a water tank and connected to an FPGA through a 1m cable. By sweeping the transducer surface pressure at all AFE gain settings and recording the ADC outputs, the characterized DR is found to be 91dB (Fig. 32.2.4). The input-referred noise at the highest gain with the transducer elements loaded by water is 12.7nV/√Hz at 6MHz, around 5nV/√Hz higher than what the electronics are designed for with the difference being attributed to the thermal noise of the transducer. Two tones appear due to mismatch in the μBF S/H cells but by recording and subtracting the pattern, they are readily removed. The power of each channel is measured, with a delta-pitch-matched configuration with a sub-array of 3 elements, the ultrasound signal is checked and a demonstration of the TGC in one PE cycle, confirming the availability of the full DR for high frame-rate imaging.

The ADC is strongly integrated with the architecture of the ultrasound ASIC (Fig. 32.2.3). A charge-sharing successive-approximation (SAR) first stage directly employs the S/H cells of the μBF as sampled inputs [3], avoiding the need for a power-hungry, high-bandwidth ADC driver as in [1,2]. To minimize the area and power impact of the converter, a hybrid structure between the energy-efficient, fast but area-wise inefficiently scalable SAR first stage and an area-efficient, linear but slow single-slope (SS) second stage is chosen. In contrast to [2], the SS ramp is generated using compact current sources rather than a capacitive digital to analog converter (CDAC). For the 10b 24MS/s μBF data, the range is 12-bit and the 48dB CDAC resolution of 10b 24MS/s data is found to be 25.6μW/element in 1mW operation and 1.23mW/element with the difference being attributed to the thermal noise of the transducer. Two tones appear due to mismatch in the μBF S/H cells but by recording and subtracting the pattern, they are readily removed. The pulse-echo imaging experiment with a phantom of 3 needles placed in front of theASIC is described in Fig. 32.2.6. While the aperture is too small to provide the resolution of a full array, the needle heads can clearly be distinguished in 3D space, demonstrating the imaging capability of the system at the intended frame-rate.

References:
PGA
Element-Level MOSCAP CDAC Cell
Local Calibration (showing 3b SAR conversion for simplicity).

Figure 32.2.1: Overview of the application and applied techniques.

Figure 32.2.2: System block diagram with analog front-end details.

Figure 32.2.3: Circuit diagram of the shared hybrid ADC with timing diagram (showing 3b SAR conversion for simplicity).

Figure 32.2.4: Electrical and acoustic measurement results.

Figure 32.2.5: Die micrograph with subarray floorplan, distribution of area/power and state-of-the-art comparison of miniature ultrasound probe ADCs.

Figure 32.2.6: Imaging of a 3-needle phantom in a watertank: experimental setup, example subgroup output, 8-mode image, and 3D rendering.
<table>
<thead>
<tr>
<th></th>
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<th></th>
<th></th>
<th></th>
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<tbody>
<tr>
<td><strong>Process</strong></td>
<td>180 nm BCD</td>
<td>180 nm</td>
<td>180 nm BCD</td>
<td>180 nm</td>
<td>N/A</td>
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<tr>
<td><strong>Transducer</strong></td>
<td>2D PZT</td>
<td>2D PZT/CMUT</td>
<td>2D CMUT</td>
<td>2D PZT</td>
<td>2D PZT</td>
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<tr>
<td><strong>Array Size</strong></td>
<td>8 x 9</td>
<td>6 x 6</td>
<td>64</td>
<td>4 x 4</td>
<td>6 x 24</td>
</tr>
<tr>
<td><strong>Integrated</strong></td>
<td>✔</td>
<td>✔</td>
<td>✔</td>
<td>✔</td>
<td>✔</td>
</tr>
<tr>
<td><strong>Transducer</strong></td>
<td>✘</td>
<td>✔</td>
<td>✔</td>
<td>✔</td>
<td>✔</td>
</tr>
<tr>
<td><strong>Center Freq.</strong></td>
<td>6 MHz</td>
<td>5 MHz</td>
<td>7 MHz</td>
<td>5 MHz</td>
<td>5 MHz</td>
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<td><strong>Pitch-Matched</strong></td>
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<td>✔</td>
<td>✔</td>
<td>✔</td>
<td>✔</td>
</tr>
<tr>
<td><strong>Element Pitch</strong></td>
<td>160 μm x 160 μm</td>
<td>250 μm x 250 μm</td>
<td>100 μm x 150 μm</td>
<td>64 x 64</td>
<td>150 μm x 150 μm</td>
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<tr>
<td><strong>Integrated TX</strong></td>
<td>✔</td>
<td>✔</td>
<td>✔</td>
<td>✔</td>
<td>✔</td>
</tr>
<tr>
<td><strong>Max. TX Voltage</strong></td>
<td>60 V</td>
<td>63.2 V</td>
<td>60 V</td>
<td>N/A</td>
<td>N/A</td>
</tr>
<tr>
<td><strong>Digitization</strong></td>
<td>✔</td>
<td>✔</td>
<td>✔</td>
<td>✔</td>
<td>✔</td>
</tr>
<tr>
<td><strong>RX Architecture</strong></td>
<td>AFE + µBF</td>
<td>AFE + µBF + ADC + Datalink</td>
<td>AFE + ADC</td>
<td>AFE</td>
<td>AFE + µBF + ADC + Datalink</td>
</tr>
<tr>
<td><strong>Channel Reduction</strong></td>
<td>12-fold</td>
<td>N/A</td>
<td>N/A</td>
<td>N/A</td>
<td>36-16 fold</td>
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<tr>
<td><strong>Supported Frame Rate</strong></td>
<td>1000 vol/s</td>
<td>N/A</td>
<td>N/A</td>
<td>N/A</td>
<td>15-20-150 fold</td>
</tr>
<tr>
<td><strong>Active Area / El.</strong></td>
<td>0.632 mm²</td>
<td>0.063 mm²</td>
<td>0.464 mm²</td>
<td>0.023 mm²</td>
<td>0.028 mm²</td>
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<tr>
<td><strong>RX Power / El.</strong></td>
<td>1.23 mW</td>
<td>1.14 mW</td>
<td>5.2 mW</td>
<td>1.54 mW</td>
<td>0.91 mW</td>
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<tr>
<td><strong>Input DR</strong></td>
<td>91 dB</td>
<td>97.5 dB</td>
<td>N/A</td>
<td>89 dB</td>
<td>85 dB</td>
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<tr>
<td><strong>Peak SNR</strong></td>
<td>52.5 dB</td>
<td>57.5 dB</td>
<td>N/A</td>
<td>49.8 dB</td>
<td>51.8 dB</td>
</tr>
</tbody>
</table>

*Transducers on separate board connected with wires
† Scalability limited by transducer connection out of pitch
‡ ADC only, excluding AFE
§ Including the dailink and LVDS drivers

Figure 32.2.7: Performance summary and comparison with the state of the art in ultrasound catheter imaging systems.