Electrical characterization of PureB layers in contacts, diodes and transistors

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Electrical characterization of PureB layers in contacts, diodes and transistors

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For the degree of Master of Science in Electrical Engineering, Microelectronics at Delft University of Technology

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# Table of Contents

<table>
<thead>
<tr>
<th>Section</th>
<th>Page</th>
</tr>
</thead>
<tbody>
<tr>
<td>Acknowledgements</td>
<td>vi</td>
</tr>
<tr>
<td>1 Introduction</td>
<td>1</td>
</tr>
<tr>
<td>1.1 PureB deposition using CVD</td>
<td>2</td>
</tr>
<tr>
<td>1.2 Ultrashallow Junction Applications of PureB</td>
<td>5</td>
</tr>
<tr>
<td>1.3 Thesis Outline</td>
<td>9</td>
</tr>
<tr>
<td>2 Theory</td>
<td>11</td>
</tr>
<tr>
<td>2.1 Junction Field-Effect Transistor</td>
<td>11</td>
</tr>
<tr>
<td>2.1.1 What is Field Effect?</td>
<td>11</td>
</tr>
<tr>
<td>2.1.2 JFET operation</td>
<td>12</td>
</tr>
<tr>
<td>2.1.3 Device characteristics</td>
<td>14</td>
</tr>
<tr>
<td>2.2 Noise Theory</td>
<td>17</td>
</tr>
<tr>
<td>2.2.1 Thermal Noise</td>
<td>17</td>
</tr>
<tr>
<td>2.2.2 1/f Noise</td>
<td>18</td>
</tr>
<tr>
<td>3 DC Analysis of PureB layers</td>
<td>19</td>
</tr>
<tr>
<td>3.1 PureB in Contacts</td>
<td>19</td>
</tr>
<tr>
<td>3.1.1 Two-Terminal Method</td>
<td>20</td>
</tr>
<tr>
<td>3.1.2 The Cross-Bridge Kelvin Resistance Method</td>
<td>29</td>
</tr>
<tr>
<td>3.2 PureB in $p^n$ configuration</td>
<td>31</td>
</tr>
<tr>
<td>3.2.1 $pnp$ Bipolar Junction Transistor</td>
<td>33</td>
</tr>
<tr>
<td>3.2.2 $p^n$ Diode</td>
<td>36</td>
</tr>
<tr>
<td>3.3 PureB 'gated' JFETs</td>
<td>40</td>
</tr>
<tr>
<td>4 Conclusions</td>
<td>46</td>
</tr>
<tr>
<td>Bibliography</td>
<td>48</td>
</tr>
</tbody>
</table>
# List of Figures

1.1 The energy diagram of different possible diborane decomposition modes ........................................ 4  
1.2 Doping reaction model for Si surface exposure to B$_2$H$_6$ dopant gas ............................................. 5  
1.3 Cross-sections of (a) Varactor diode and (b) Photodiode ................................................................. 8  
1.4 Schematic representation of the emitted signals after the primary electrons interaction with a sample ................................................................. 9  

2.1 Cross-section of a JFET .......................................................................................................................... 12  
2.2 $I_D$ vs $V_{DS}$ characteristics .............................................................................................................. 13  

3.1 Cross-section of the two-terminal test structure used ....................................................................... 21  
3.2 Layout of dies / openings across the wafer ......................................................................................... 22  
3.3 Varying PureB thickness ...................................................................................................................... 22  
3.4 Ellipsometry Result ............................................................................................................................. 23  
3.5 12 min deposited PureB layer at 700°C ............................................................................................. 24  
3.6 19 min deposited PureB layer at 700°C ............................................................................................. 26  
3.7 20 min deposited PureB layer at 450°C ............................................................................................. 27  
3.8 Comparison of contact resistance between different processing conditions ............................... 28  
3.9 Schematic of a CBKR structure ............................................................................................................ 29  
3.10 Contact Resistance vs 1/Area ........................................................................................................... 31  
3.11 Schematic of a vertical bipolar transistor .......................................................................................... 33  
3.12 Collector and Base Currents for 700°C PureB .................................................................................. 35  
3.13 Comparison of collector and base Currents under different process conditions ....................... 37  
3.14 Collector and Base Currents at different temperatures .................................................................. 38  
3.15 BJT Arhenius Plot ............................................................................................................................... 39  
3.16 Schematic Top View of the Ring Structure ....................................................................................... 41  
3.17 JFET Ring Structure fabricated in DIMES ...................................................................................... 41  

Master of Science Thesis  Sivaramakrishnan Ramesh
<table>
<thead>
<tr>
<th>Figure</th>
<th>Description</th>
<th>Page</th>
</tr>
</thead>
<tbody>
<tr>
<td>3.18</td>
<td>Comparison of Output Characteristics of JFET</td>
<td>43</td>
</tr>
<tr>
<td>3.19</td>
<td>Comparison of Top Gate Leakage</td>
<td>44</td>
</tr>
<tr>
<td>3.20</td>
<td>Comparison of Channel Resistance</td>
<td>44</td>
</tr>
<tr>
<td>3.21</td>
<td>Comparison of Transconductance</td>
<td>45</td>
</tr>
</tbody>
</table>
List of Tables

3.1 PureB Deposition Process Parameters ............................................. 23
3.2 CBKR Measurement ........................................................................ 30
3.3 CBKR and Two-Terminal Comparison ................................................. 31
3.4 BJT Process Conditions ................................................................... 33
3.5 Diode Process Conditions ................................................................. 40
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Delft, University of Technology
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To my grandparents

“The only way to discover the limits of the possible is to go beyond them into the impossible.”
— Sir Arthur Charles Clarke
Over the past few decades, the key to the continuous improvement in the performance of the work horse of semiconductor industry, i.e. MOSFET, is scaling [1]. In 1974 when Robert Dennard and his team [2] proposed a set of rules to scale the various device parameters for improved performance, little did they know that it will revolutionize the silicon industry. They reported that if the channel length (horizontal dimension) of a field-effect transistor (FET) was scaled arbitrarily, the short channel effects start to dominate. The solution suggested was then to simply scale both the vertical and horizontal dimensions with the same scaling factor. The vertical dimensions include the source/drain formation and the junction depth. The source/drain junction plays a significant role in the device performance. As the device downscaling continues, there is always the need for novel technologies to satisfy the device dimension requirements.

In that aspect, the formation of source/drain junction has been complemented by the development of newer technologies that are aimed at forming highly-doped, ultra-shallow, damage-free junctions. The most common technique being the low-energy ion-implantation followed by a high-temperature anneal. However, due to the lattice defects caused by implantation, an unwanted broadening of the doping profile is realized, termed as damage-induced tran-
sient enhanced diffusion (TED) [3]. This effect is even worsened in the case of boron (B) dopants. Needless to say, B is the most commonly used p-type dopant. Previously it has been demonstrated by the ’Silicon Device Integration’ group, at ’Delft Institute of Microsystems and Nanoelectronics’ (DIMES), TU Delft, that a low temperature (500°C to 700°C) chemical vapor deposition (CVD) of pure boron (PureB) can be a very attractive substitute for B-implantation [4]. This low temperature CVD of PureB helps in the formation of high quality and ultra-shallow p⁺n junctions. The deposition process is conformal and PureB has better selectivity to Si. Since the PureB technology is compatible with standard semiconductor processing due to the low deposition temperature, it is also ideal for shallow source / drain junction formations in future technology nodes CMOS devices.

In the following sections of this chapter, we will look in to the chemistry behind the nanometer-deep p⁺n junction technology through PureB CVD process and briefly discuss the various current and potential applications for such a technology.

### 1.1 PureB deposition using CVD

In recent years, the chemical vapor deposition of pure boron (dubbed as pure B) has been recognized as an alternate method to the more conventional damage inducing ion-implantation technique. It is possible to obtain p-type doping from pure B deposition, by exposing Si surface to diborane (B₂H₆) in an oxygen-free environment [4]. It is convenient to use B₂H₆ which is a widely used p-type dopant gas. It has also been demonstrated that the chemical concentration of B in the Si surface after PureB exposure exceeds the solid solubility limit [5]. However, the active dopant concentration depends on various deposition conditions like temperature, pressure, source gas concentration. There are various merits to pursue this alternate technique to implantation. In general, CVD processes are less expensive, achieve high throughput, are compatible with standard semiconductor processing and can lead to a well-controlled growth even at low temperatures.

Clean Si surface is exposed to diborane in a Si/SiGe epitaxial CVD reactor. For a 700°C deposition, it has been observed [6] that during the initial stages of the process the boron
atoms quickly react with the Si surface and form an uniform thin layer of pure B. From then on, further deposition occurs on top of this pure B layer. This second reaction is much more slower and has a well-controlled deposition rate. It is also noted that at lower deposition temperatures, the carrier gas used (H\textsubscript{2} or N\textsubscript{2}) strongly influences the film uniformity.

The net chemical reaction for boron deposition is given by [6],

\[ \text{B}_2\text{H}_6(g) \rightarrow 2\text{B}(s) + 3\text{H}_2(g) \]  \hspace{1cm} (1.1)

where (\textit{g}) is the gas phase and (\textit{s}) is the solid phase of the reactants and the products.

However, there are many sub-reactions occurring before the final boron deposition. Even though the deposited boron is very stable (does not readily oxidize in air), the diborane gas used for deposition is thermodynamically unstable [6]. Kota Sato et al. [7] have experimentally concluded that B\textsubscript{2}H\textsubscript{6} decomposes to form borane (BH\textsubscript{3}) molecules which is thermodynamically the most likely scenario (see figure 1.1).

\[ \text{B}_2\text{H}_6(g) \rightarrow 2\text{BH}_3(g) \]  \hspace{1cm} (1.2)

During the PureB CVD process in the presence of H\textsubscript{2} gas, it is possible that some Si surface sites are passivated with H atoms (Si\_H) and some are just left with dangling bonds (Si\_°). The disintegrated BH\textsubscript{3} molecules will now react readily with the available surface sites in the following way [5]:

\[ \text{Si\_H} + \text{BH}_3 \rightleftharpoons \text{Si\_HBH}_3 \]  \hspace{1cm} (1.3)

\[ \text{Si\_HBH}_3 + \text{Si\_H} \rightarrow \text{Si\_H} + \text{Si\_HBH}_3 \]  \hspace{1cm} (1.4)

\[ \text{Si\_HBH}_3 + \text{Si\_HBH}_3 \rightarrow 2\text{Si\_H} + \text{B}_2\text{H}_6 \]  \hspace{1cm} (1.5)
1.1 PureB deposition using CVD

Figure 1.1: The energy diagram of different possible diborane decomposition scenarios [7]

\[
\begin{align*}
\text{BH}_2 + \text{BH}_4 : 6.3 \text{ eV} &= 145.3 \text{ kcal mol}^{-1} \\
\text{BH}_3 \text{H}_2 + \text{H}_2 : 4.2 \text{ eV} &= 96.7 \text{ kcal mol}^{-1} \\
\text{H}_2 \text{BH}_2 + \text{H}_2 : 2.5 \text{ eV} &= 57.7 \text{ kcal mol}^{-1} \\
2\text{BH}_3 : 1.7 \text{ eV} &= 39.2 \text{ kcal mol}^{-1} \\
\end{align*}
\]

\[\text{B}_2\text{H}_6\]

\[\text{Si}^\circ + \text{BH}_3 \rightarrow \text{SiB} + 3\text{H} \quad (1.6)\]

\[\text{SiB} \rightarrow \text{Si}^\circ + \text{B}(\text{diffused}) \quad (1.7)\]

In reaction 1.3 a BH$_3$ molecule physically adsorbs onto a H terminated Si site while its structure being intact. This is termed as **physisorption**, caused by the weak van der Waals force between the two reactants and so it is easily reversible. The reverse reaction is called **reflection**.

Reaction 1.4 tells us how a BH$_3$ molecule migrates from one Si-H site to another. Hence the name **migration**.

When two physisorbed BH$_3$ molecules recombine to form the source gas B$_2$H$_6$, we get the **recombination** reaction 1.5.

Reactions 1.6 and 1.7 are the ones that are useful to us. Basically they show how Si is doped with B. In the former, the borane reacts with a Si dangling bond and the B atom chemically adsorbs onto the free Si atom releasing atomic hydrogen. In some cases the chemically ad-
sorbed B diffuses into Si as in the latter. The two reactions are termed as chemisorption and diffusion respectively. The released atomic H in reaction 1.6 goes on to start many sub-reactions.

For a detailed discussion on the kinetics and reactions involved during pure B deposition, readers are requested to refer to [4, 6, 8]. A basic model incorporating the reactions discussed above is shown in figure 1.2.

![Doping reaction model for Si surface exposure to B$_2$H$_6$ dopant gas](image)

**Figure 1.2:** Doping reaction model for Si surface exposure to B$_2$H$_6$ dopant gas [5]

### 1.2 Ultrashallow Junction Applications of PureB

The study of doping techniques and junction formation is probably as old as the semiconductor industry itself. The pn junction plays a significant role in the device performance. As the device downscaling continues, there is always the need for novel technologies to satisfy the ever-growing demands aimed at forming highly-doped, ultra-shallow, damage-free junctions.

The ion implantation technique which has a well controlled dose implantation and doping profile uniformity is commonly used for doping and junction formation. But as the implantation energy is reduced to form shallow junctions, the dose rate decreases [9]. Hence, it is difficult to form highly-doped ultrashallow junctions that are the need of the hour. Moreover, this technique causes damage to the substrate inducing diffusion. Similar methods like plasma doping and cluster beam implantation were considered and failed due to implantation...
1.2 Ultrashallow Junction Applications of PureB

damage and non-uniform doping profiles. In this juncture, attention is turned towards the gas phase doping of CVD PureB. The 2011 edition of the International Technology Roadmap for Semiconductors (ITRS) [10] stresses the need and challenges to form ultrashallow junctions and lists gas phase doping as a potential candidate for 2013 and beyond.

Ultrashallow junctions formed by CVD PureB have been used in many application-specific requirements other than the regular Bipolar and CMOS devices [5, 11, 12, 13]. They are

- Highly linear varactor diodes used in tunable RF circuits
- Photodiodes to detect low penetration-depth beams such as light from the ultra-violet (UV) and extreme UV spectrum
- Low energy electron detectors for scanning electron microscope (SEM)

**Varactor Diode**

As the application suggests, a varactor diode has a variable reactance which when controlled can help achieve a well-tunable RF circuit. The depletion capacitance per unit area of the diode is given by [5]

\[
C = \frac{\epsilon_0 \ast \epsilon_{Si}}{W(N_D(x), V_R)}
\]

where \(\epsilon_0\) and \(\epsilon_{Si}\) are permittivities in vacuum and Si respectively. \(W\) is the depletion region width which is a function of the bulk n-type doping profile, \(N_D(x)\) and the reverse bias voltage, \(V_R\).

From equation 1.8, we can see that by appropriately tailoring the bulk doping profile, RF circuits with excellent tunable characteristics is achieved. However, the desired \(N_D(x)\) can be attained only with a heavily doped and abrupt p\(^+\) junctions. The PureB deposition offers an abrupt p\(^+\) junction with high doping efficiency and low series resistance (very thin junctions).

A point to be noted is the low deposition temperature offered by the PureB technology, as higher temperatures can disrupt the desired \(N_D(x)\) profile with undesirable diffusion. Thus,
resulting in a high-linear, high-quality, varactor diodes for high-speed, wide tuning bandwidth RF circuits. More detailed discussions on varactor diode application are provided in [5, 14].

**Photodiode**

Any photodetector device works on the principle of generation and separation [15]. Excess electron-hole pairs are generated in the depletion region of the pn junction and separated by the applied reverse bias electric field creating a reverse current indicating the detection. Thus a pn junction and its space charge region are an important basis for photodiode applications. When radiation is incident on a semiconductor, the intensity decreases exponentially with the distance from the surface as given in equation 1.9. Therefore, the excess carrier generation rate which is proportional to the intensity also decreases.

\[
I_R(x) = I_{R0} \exp(-\alpha x)
\]  

(1.9)

where \(I_{R0}\) is the radiation intensity incident on the surface and \(I_R(x)\) is the intensity decaying with distance 'x' from the surface. \(\alpha\) is a material property and a constant, termed as the absorption coefficient.

From above equation we can understand that the maximum generation of excess electron-hole pairs will happen close to the surface of the junction where the radiation intensity is maximum. Hence an ultrashallow junction with space charge region close to the surface will be an excellent choice for photodiode applications. In addition, there has been a lot of advancement in the semiconductor tools manufacturing industry focused on sub-100nm wavelength (UV spectrum) photolithography tools. Hence there is considerable effort in developing photodiodes for these low penetration-depth beams detection applications. It is also important that the ultrashallow junction formed has a high doping efficiency, which if not met will have a negative effect on the sensitivity of the detector [5].

In general, the diodes used for this application are exposed to heavy radiation (photon flux) and suffer from hydrocarbon contamination [12]. The cleaning process involves aggressive
treatments and eventually reduce the performance and device reliability. And so, developing highly-doped, defect-free ultrashallow junctions that are unaffected by these harsh conditions will improve the device performance and reliability which are otherwise compromised by the current doping techniques and design trade-offs [5, 12]. It has been recently demonstrated [11, 12] that the CVD PureB junctions provide a high-quality, defect-free, abrupt junctions, improving the optical efficiency and spectral responsivity. The p⁺-region formed by PureB deposition boasts of a high effective gummel number [3, 11], thereby suppressing the electron injection from the n-region and reducing the noise, i.e., dark current, resulting in a more sensitive detector. Figure 1.3 shows the simple cross-sections of a varactor diode and a photodiode.

Figure 1.3: Cross-sections of (a) Varactor diode and (b) Photodiode [5]

Low Energy Electrons Detector

In a scanning electron microscope, a beam of electrons called the primary electrons, are accelerated through an electron gun and are focused towards the desired sample surface. The primary electrons interact with the specimen in various ways that can be grouped in two broad categories - elastic and inelastic interactions. The resulting signals / electrons from these interactions (see figure 1.4), each carry a distinct information on the topography and composition of sample [13]. So it is required to collect and distinguish between these different
types of electrons. This is where the detectors come in.

![Diagram of emitted signals](image)

**Figure 1.4**: Schematic representation of the emitted signals after the primary electrons interaction with a sample [13]

We know that the maximum generation of excess electron-hole pairs will happen close to the surface of the junction where the radiation intensity is maximum. So a question arises, why not Schottky diodes? There are many advantages of using a PureB diode over a Schottky diode or a regular photodiode [13]. A Schottky diode in general has a high reverse current, the conversion efficiency at the surface is less due to unwanted carrier recombination. PureB diodes as we have seen earlier do not suffer from the above setbacks and are a level-ahead with respect to a regular photodiode. Moreover boron, being a low atomic number element, will induce lesser scattering of incoming electrons thereby increasing the range of the detector [11].

### 1.3 Thesis Outline

The aim of the work presented in this thesis is focused on the electrical characterization of Pure-B layers (as deposited Boron layers) in contacts, diodes and bipolar & junction field...
effect transistors. In order to understand the material property of the deposited boron layers, contact resistance measurements were performed. Different structures, namely, the kelvin structures and large contact openings were used not only to measure the resistivity of the layers but also to understand the deposition kinetics and influence of oxide coverage [16]. The junction quality of the PureB layers with the Si surface for different processing conditions was also studied by characterizing the diodes and bipolar transistors fabricated from this processing scheme.

Chapter 2 gives a theoretical introduction to the working of a junction field effect transistor (JFET). It also briefly talks about the various types of noise present in a JFET and stresses upon the 1/f noise. Chapter 3 discusses the DC characterization performed on pure B layers. Chapter 4 concludes the work and gives a brief summary on the results discussed.
In this chapter we shall review some basic concepts related to junction field-effect transistors and $1/f$ noise.

### 2.1 Junction Field-Effect Transistor

*This section is summarized from 'Chapter 13: The Junction Field-Effect Transistor' of the book 'Semiconductor Physics and Devices - Basic Principles' by Donald A. Neamen*

#### 2.1.1 What is Field Effect?

The current flow between two ends (generally ohmic metal contacts) of a semiconductor can be controlled by applying an electric field in perpendicular to the semiconductor surface. This phenomenon of modulating the conductance of the semiconductor is termed as 'field effect'.

In a field effect transistor only the majority carriers (n-type or p-type) participate in the conduction or operation of the device. Hence, it also goes by the name 'unipolar transistor'. Since the minority carriers are not involved, JFET (junction field effect transistor) can achieve
very high cut-off frequency. JFETs find applications in circuits that require low noise and high input impedance amplifiers.

### 2.1.2 JFET operation

In a pn junction field effect transistor (pn JFET), the gate (control terminal) is formed by a highly doped \( p^+/n^+ \) region and a moderately doped \( n \) (\( n \)-channel)\( /p \) (\( p \)-channel) region forms the channel under the gate. In general, a JFET is a depletion mode device, i.e., it is 'on' by default. A reverse biased gate voltage is applied to turn it 'off'. A typical cross-section of a JFET is shown in figure 2.1. Since the mobility of electrons is high compared to the mobility of holes, an \( n \)-channel JFET operates at a higher frequency compared to the \( p \)-channel JFET.

![Figure 2.1: Schematic cross-section of a JFET](image)

The channel between source (\( S \)) and drain (\( D \)) of a JFET can be modeled as a resistor such that the drain current (\( I_D \)) varies almost linearly with the drain-source voltage (\( V_{DS} \)) for low \( V_{DS} \) values. The value of the resistance in this case is obtained from the slope of the \( I_D vs V_{DS} \) characteristics.

When the gate-to-channel region is maintained in reverse bias condition, the space charge region (depletion region) between the gate and the channel becomes larger, as shown in figure 2.1. As the reverse bias condition is increased, the space charge region widens and the channel width reduces increasing the channel resistance. The reverse bias condition at which the space charge region engulfs the channel width completely, such that \( I_D \) is essentially zero, is referred to as **pinchoff**.

Suppose the gate-to-source voltage (\( V_{GS} \)) is fixed. Then for small values of \( V_{DS} \) the \( I_D vs V_{DS} \) characteristics...
2.1 Junction Field-Effect Transistor

$V_{DS}$ curve is linear (linear region of operation). As $V_{DS}$ increases, such that the gate-to-channel is reverse biased near the drain terminal, the effective channel resistance increases. This will decrease the slope of the $I_D$ vs $V_{DS}$ curve. Further increasing $V_{DS}$ will result in pinchoff condition at the drain terminal. The drain current saturates at this point and is ideally invariant of $V_{DS}$, acting like a constant current source. The drain-to-source voltage at this condition is termed as $V_{DS}(sat)$ and this region of operation is called saturation. Figure 2.2 shows a common $I_D$ vs $V_{DS}$ characteristics at different $V_{GS}$ values for an $n$-channel JFET. The different regions of operation are marked for reference.

![Figure 2.2: $I_D$ vs $V_{DS}$ characteristics with different regions of operations](image)

In the saturation region, as $V_{DS}$ increases $I_D$ remains the same. The reason is as follows. Let $L$ be the length of the channel between the source and drain. At pinchoff, let the channel and the drain terminal be separated by the space charge region of width $\Delta L$ (see figure 2.1). Now the remaining channel which is not pinched-off, i.e. $\prime L - \Delta L'$, will be at the same potential (for the condition $\Delta L \ll L$) as just before pinchoff, which is $V_{DS}(sat)$. The charge carriers in the channel experience the electric field due to this constant potential until they reach the...
space charge region near the drain terminal. Hence \( I_D \) has the same value as that for the \( V_{DS}(sat) \) case and is not influenced by the increase in \( V_{DS} \).

### 2.1.3 Device characteristics

A JFET usually has a top gate and a bottom gate, with the channel sandwiched between the two gates. Let’s consider an one-sided JFET, i.e either the top gate or the bottom gate is biased for simplicity. All further discussion in this chapter is performed for an \( n \)-channel JFET, unless otherwise specified. Let ‘\( a \)’ be the channel thickness and ‘\( h_1 \)’, \( h_2 \) be the depletion region widths extending from the gate to the channel on the source terminal-side and drain terminal-side respectively. Then for a channel doping concentration of \( N_d \) and gate doping concentration of \( N_a \), we have,

\[
h_1 = \sqrt{\frac{2\varepsilon_s(V_{bi} - V_{GS})(N_a + N_d)}{eN_aN_d}} \tag{2.1}
\]

\[
h_2 = \sqrt{\frac{2\varepsilon_s(V_{bi} + V_{DS} - V_{GS})(N_a + N_d)}{eN_aN_d}} \tag{2.2}
\]

where \( V_{bi} \) is the built-in potential voltage between the \( p \)-doped gate and \( n \)-channel. \( V_{GS} \) is the gate-to-source voltage and \( V_{DS} \) is the drain-to-source voltage. \( V_{DS} \) does not have an effect in the source terminal-side.

At pinchoff, the channel is completely pinched off by the depletion region at the drain terminal and so \( h_2 = a \). The \( V_{GS} \) for this condition is termed as the pinchoff voltage, \( V_p \) and \( V_{DS} \) is termed as the saturation voltage, \( V_{DS}(sat) \). The term \( V_{bi} + V_{DS} - V_{GS} \Rightarrow V_{bi} + V_{DS}(sat) - V_p = V_{p0} \), called the internal pinchoff voltage, is then given by

\[
V_{p0} = \frac{ea^2N_d}{2\varepsilon_s} \tag{2.3}
\]

With the terms defined above let us derive the \( I - V \) relation for the JFET.
2.1 Junction Field-Effect Transistor

Drain Current

We know that the JFET can be modeled as a resistor. When $V_{DS}$ and $V_{GS}$ are applied, the depletion region width changes along channel and so the channel thickness varies. This results in a varying resistance along the channel. Let $R(x)$ be the resistance at any point $x$ along the channel length. Then,

$$R(x) = \rho \frac{x}{A(x)}$$

where $\rho$ is the resistivity and $A(x)$ is the cross-section area of the conducting region defined as the product of the gate width, $W_G$ and $(a - h(x)) - a$ is the channel thickness and $h(x)$ is the varying depletion region width along the channel.

From ohm’s law, we have,

$$I = \frac{V}{R}$$

Thus, the current $I(x)$ at a point $x$ along the channel is given by,

$$I(x) = \frac{V(x)}{R(x)} = \frac{V(x)A(x)}{\rho * x}$$

$$\Rightarrow I(x) = \frac{V(x)N_d\mu_e A(x)}{x} = \frac{V(x)N_d\mu_e W_G h(x)}{x}$$

Substituting the boundary conditions for $h(x)$ from equations 2.1 and 2.2 and solving for the entire channel length, we get,

$$I_D = I_P[3\left(\frac{V_{DS}}{V_{p0}}\right) - 2\left(\frac{V_{DS} + V_{bi} - V_{GS}}{V_{p0}}\right)^{3/2} + 2\left(\frac{V_{bi} - V_{GS}}{V_{p0}}\right)^{3/2}]$$

(2.4)

where the pinchoff current, $I_P$ is defined as,
\[ I_P = \frac{\mu_n (eN_d)^2 W_G a^3}{6\epsilon_s L} \]

Equation 2.4 is for the drain current in the linear region and not valid in the saturation condition. In that case the drain current is given by,

\[ I_D(sat) = I_P[1 - 3(\frac{V_{bi} - V_{GS}}{V_{p0}})(1 - \frac{2}{3} \sqrt{\frac{V_{bi} - V_{GS}}{V_{p0}}})] \tag{2.5} \]

In practice an approximation of equation 2.5 is used,

\[ I_D = I_{DSS}(1 - \frac{V_{GS}}{V_p})^2 \tag{2.6} \]

\[ I_{DSS} = I_P[1 - 3(\frac{V_{bi}}{V_{p0}})(1 - \frac{2}{3} \sqrt{\frac{V_{bi}}{V_{p0}}})] \]

**Transconductance**

The gain of a JFET is defined as the transconductance. It is the measure of the control of the gate voltage over the drain current. It is given by,

\[ g_m = \frac{\partial I_D}{\partial V_{GS}} \tag{2.7} \]

Substituting equations 2.4 and 2.6 we can get the transconductance in the respective regions.

\[ g_{mLinear} = \frac{3I_P}{2V_{p0}} \left( \frac{V_{DS}}{\sqrt{V_{p0}(V_{bi} - V_{GS})}} \right) \tag{2.8} \]

\[ g_{mSaturation} = -\frac{2I_{DSS}}{V_p} (1 - \frac{V_{GS}}{V_p}) \tag{2.9} \]
2.2 Noise Theory

The aim of this section is to provide a brief theoretical introduction to noise, especially the $1/f$ noise, which is the topic of interest. Noise, in general, is a random, unwanted signal that interferes with the desired signal. When the source of this unwanted disturbance is identified, steps can be taken to minimize its effects. Since noise is random, its amplitude at a given instance cannot be predicted. Its root-mean-square (rms) value, however, can be measured. Noise measurements not only provides information on possible noise sources, but also can indicate the quality of the device [17, 18]. Let us now briefly look into the two common types of noise.

2.2.1 Thermal Noise

We know JFET can be modeled as a voltage controlled resistor. When the drain-to-source voltage, $V_{DS} = 0$, the channel of the FET will be an uniform resistor / conductor. Even when the bias is zero, if the temperature of the device is above absolute zero, the carriers in the channel are thermally agitated resulting in a random excited motion. This is termed as 'Thermal Noise'. The noise current spectral density is then given by [19]

$$S_I(f) = \frac{4k_BT}{R}$$ \hspace{1cm} (2.10)

and the noise voltage spectral density is given by

$$S_V(f) = 4k_BT R$$ \hspace{1cm} (2.11)

where, $k_B$ is the Boltzmann constant, $T$ is the temperature in kelvin and $R$ is the channel resistance.

Since equations 2.10 and 2.11 are always non-zero for $T > 0K$, we can never completely eliminate thermal noise.
2.2 Noise Theory

2.2.2 1/f Noise

1/f noise is one of the longest unsolved problems in physics. It is common to all electronic devices and determines the detection limit of low frequency measurement. The noise power spectrum of 1/f noise follows a $1/f^\gamma$ power law, with $\gamma$ varying between 0.8 and 1.3 [20] for different devices. Hence the name ‘1/f’. Although the origin for 1/f noise in devices is still a question of debate, two 1/f noise models are widely considered [21] - the McWhorter model and the mobility noise model. The former advocates that 1/f noise is caused by fluctuations in the number of free carriers while the latter, as the name suggests, talks about the relation between carrier mobility fluctuations and 1/f noise.

Let us now consider a JFET with a channel resistance, $R$. When a constant voltage is applied across $R$ we observe fluctuations in the current, $I(t)$ across $R$. Since $V = I \ast R = constant$, $I(t)$ can only occur when fluctuations in resistance ($R(t)$) is observed. Thus we have [21, 22],

$$V = I(t)R(t) = constant$$

$$\Rightarrow \frac{\partial I}{I} + \frac{\partial R}{R} = 0 \Rightarrow \frac{\partial I}{I} = -\frac{\partial R}{R}$$

and so

$$\frac{S_I(f)}{I^2} = \frac{S_R(f)}{R^2} = \frac{C_{1/f}}{f} = \frac{\alpha_H}{Nf}$$

(2.12)

where $C_{1/f}$ is termed as the relative noise intensity, $N$ is the total number of charge carriers and $\alpha_H$ is the dimensionless Hooge’s parameter.

Equation 2.12 is the empirical Hooge’s equation that defines the Hooge’s parameter, $\alpha_H$, which is used as a figure of merit to study and compare the 1/f noise present in different devices.
Chapter 3

DC Analysis of PureB layers

In this chapter we shall study the electrical characteristics of the PureB layer. Many devices such as contacts, diodes, pnp-bipolar (BJT) & n-channel junction field effect transistors (JFET) were fabricated under different processing conditions and electrically characterized. The influence of process parameters and patterns present on the wafer on the PureB deposition and properties have also been discussed. The analysis presented here will help further understand and exploit the PureB layer.

3.1 PureB in Contacts

One of the important applications of the PureB technology is photodiodes for detecting low energy electrons and low-penetration depth beams. The penetration depth of these particles will be in the order of a few nm and so it is necessary to have a nm—thin junction [23]. Hence, the problem of determining the thickness of such a thin layer comes up. There are various material characterization methods available that can reveal many parameters of the junction / PureB layer including its thickness. However, they are very complex, time consuming and expensive [24]. A simple and quick technique to verify the PureB thickness is to measure
its vertical resistance. The contact resistance $R_{cont}$ of a layer with thickness $t$ and a contact cross-section area $A$ is given by,

$$R_{cont} = \rho * \frac{t}{A}$$  \hspace{1cm} (3.1)

where $\rho$ is the resistivity of the layer.

When the cross-section area and the resistivity are known, the thickness can be calculated by measuring the resistance. Since $\rho$ is a material property, it is a constant. So by accurately calculating it from layers with known thickness values, we can confidently measure layers with unknown thickness values. In this work, PureB layers with different thicknesses were characterized and the resistivity was calculated. Different structures were used for the measurement. The measurement and the results are discussed below.

### 3.1.1 Two-Terminal Method

A simple two-point $I - V$ measurement of the PureB layers were done on special test sites with different sizes and the resistivity was then extracted. These special structures had dual purpose. It has been reported in literature [16] that the deposition rate of the PureB process depends on the oxide coverage ratio and the deposition window sizes on the wafer and loading effects. To study these parameters, Si wafers covered with oxide were taken and cm-wide windows were opened. PureB was deposited and metalized and patterned (with $\mu m$-size pads) to get the final structure. From these structures a few things can be concluded 1) How the thickness of PureB varies along the window - This was confirmed by ellipsometry and resistance measurement 2) The effect of oxide coverage and other parameters on deposition can be studied 3) The diffusivity and selectivity of PureB on Si and $SiO_2$ can also be studied. In this work we will concentrate only on thickness variation and the corresponding change in resistance.

Figure 3.1 shows a schematic cross-section of the two-terminal test structure used. $R_1$ is a combination of the vertical resistance of the PureB layer and the resistance at the Si-B
interface (ignored in the analysis). $R_2$ is the resistance contributed by the substrate and can be neglected due to the low resistivity of the substrate used. The total resistance measured from the top to bottom is given by

$$R_{\text{total}} = R_1 + R_2 (R_2 \ll R_1)$$

$$R_{\text{total}} = R_1 = \rho \frac{t}{A}$$  \hspace{1cm} (3.2)

The set of contact areas used for measurement are 4$\mu$m, 6$\mu$m, 8$\mu$m and 10$\mu$m. By finding the difference in resistance between any two non-similar contact area structures, the resistivity of the layer can be calculated. For example

$$R_{\text{cont1}} = \rho \frac{t}{A_1}$$

$$R_{\text{cont2}} = \rho \frac{t}{A_2}$$

$$R_{\text{cont1}} - R_{\text{cont2}} = \rho \cdot t \cdot \left[\frac{1}{A_1} - \frac{1}{A_2}\right]$$  \hspace{1cm} (3.3)
The slope of the above relation will give the $\rho \times t$ term. Then by using the thickness value obtained from ellipsometry measurement the resistivity of the Boron layer can be calculated.

Figure 3.2 gives a schematic layout of the large openings / dies across the wafer. Dies numbered 24, 25, 34 and 35 will be considered for analysis here. From ellipsometry results, it was observed that the deposited boron thickness changed along the length of the window as shown in figure 3.3. This is due to the differences in deposition rate and diffusion length of the PureB caused by the local loading effects [16]. An ellipsometry measurement result is shown here for example (see figure 3.4). After PureB deposition on these large windows, contact metalization was performed with a given set of areas as mentioned earlier. This set-pattern was repeated as a \( nxn \)-matrix array across the large opening and the difference in thickness for areas in a given set can be neglected for the resistivity calculation.

![Figure 3.2: Layout of dies / openings across the wafer](image)

![Figure 3.3: Varying PureB thickness](image)
Table 3.1 lists out the process parameters used for PureB deposition. Let’s discuss the results one-by-one.

**Table 3.1: PureB Deposition Process Parameters**

<table>
<thead>
<tr>
<th>Sample No.</th>
<th>Deposition Time</th>
<th>Deposition Temperature</th>
<th>Alloy Anneal Condition</th>
</tr>
</thead>
<tbody>
<tr>
<td>Sample 1</td>
<td>12 minutes</td>
<td>700 °C</td>
<td>H$_2$ anneal</td>
</tr>
<tr>
<td>Sample 2</td>
<td>19 minutes</td>
<td>700 °C</td>
<td>H$_2$ anneal</td>
</tr>
<tr>
<td>Sample 3</td>
<td>20 minutes</td>
<td>450 °C</td>
<td>N$_2$ anneal</td>
</tr>
</tbody>
</table>

PureB was deposited for 12 minutes at 700 °C and contact areas were metalized with Al/1%Si. A post-metalization anneal (PMA) was performed in H$_2$ ambient for better alloying and contact of metal with the layer. Taking the position of die 24 as origin, figure 3.5a shows how the contact resistance of PureB layer is varying along the x-axis across different dies. The plot is for a 10µmx10µm area device. If we carefully notice, the resistance of each die slowly drops until it reaches the centre of the die and then increases again. This observation is consistent with the varying PureB thickness. Since the variation in resistance is following the change in thickness across the die, we can say that PureB resistance is the dominating resistance obtained from the measurement and so other parasitics are ignored for the analysis. The change in resistance is also better described by a box plot as shown in figure 3.5b.
3.1 PureB in Contacts

(a) Contact Resistance

(b) Box Plot

Figure 3.5: 12 min deposited PureB layer at 700°C - 10μmx10μm device
Similar results were also observed for the 19 minutes deposition (see figure 3.6). Figure 3.7 gives the results for the 450°C deposition sample annealed in N\textsubscript{2}. By comparing the contact resistance between the three processing conditions, we observe (figure 3.8) that the 700°C deposition samples 1 & 2 have similar characteristics, while the 450°C sample differs. For very low temperature depositions, parameters like carrier gas used, partial pressure maintained in the reaction chamber etc., play a vital role in the film quality and deposition rate [5]. This could be a reason for the difference in the characteristics observed. This gives us an idea how different processing conditions and loading effects influence the deposition. For samples 1 & 2, the resistivity calculated from equation 3.3 was about 400-500Ωcm and the \( \rho \times t \) term was found to be around \( 2 - 3 \times 10^{-4} \Omega cm^2 \).
3.1 PureB in Contacts

(a) Contact Resistance

(b) Box Plot

Figure 3.6: 19 min deposited PureB layer at 700°C - 6µm x 6µm device
Figure 3.7: 20 min deposited PureB layer at 450°C - 8µm x 8µm device
Figure 3.8: Comparison of contact resistance between different processing conditions - 4µm x 4µm device.
3.1.2 The Cross-Bridge Kelvin Resistance Method

In the two-terminal method, we saw that the measured resistance was consistent with the deposited thickness across the die. However, we cannot completely neglect the parasitics involved in the measurement [25]. The parasitics for example, could include the bottom contact resistance, the spreading resistance under the PureB layer. For a more accurate value of the contact resistance, an easy and reliable measurement, that can effectively minimize the parasitics, is needed. Cross-Bridge Kelvin Resistor (CBKR) structures will exactly satisfy this requirement. CBKR structures are extensively used in the industry to characterize very low contact resistances [26]. However, these structures do have limitations with respect to parasitics generated by non-ideal contact geometries. In this analysis we shall use a special type of kelvin structure [27] to study the contact resistance of PureB layers (see figure 3.9). The structure is compatible with the existing DIMES processes for fabricating the pure B deposited bipolar transistors which will be discussed in the next section. Table 3.2 gives the list of devices that were fabricated under different conditions.

The measurement is done by forcing a voltage $V_{12}$ between contacts 1 and 2 and measuring the corresponding current, $I_{12}$ and voltage $V_{34}$ between contacts 3 and 4. The contact resistance is then given by [27],

\[
R = \frac{V_{34}}{I_{12}}
\]
From equation 3.1, we have \( R = \rho \frac{t}{A} \)

Thus by plotting \( R_{\text{cont}} \) with \( 1/A \), we get the \( \rho \times t \) term, which can then be used to determine either the resistivity or the thickness. Figure 3.10 shows the contact resistance measured for two different devices. Table 3.2 gives the values of \( \rho \times t \) term obtained from the measurement. The values calculated using kelvin structures for the 700 °C devices are about two orders of magnitude higher than that obtained for the two-terminal structures. In order to validate the values obtained, we also performed a two-terminal-like measurement on the kelvin structures, since the diffusion bar will have a negligible resistance. Table 3.3 compares the values obtained from the two measurements. The values seem to be consistent. Also as we saw in section 3.1.1, the two-terminal measurement values obtained were also consistent with the thickness trend. Some of the possible explanations for this anomaly could be that the processing steps involved such as contact metalization, patterning and etching were different for these two devices and the patterns present in the wafers were also different. That could have probably influenced the deposition. However, this huge magnitude of difference in resistivity values was not expected. However, this warrants further investigation before anything concrete can be concluded.

\[
R_{\text{cont}} = \frac{V_{34}}{I_{12}}
\] (3.4)

**Table 3.2: CBKR Measurement**

<table>
<thead>
<tr>
<th>Sample No.</th>
<th>Deposition Parameters</th>
<th>( \rho \times t ) (in ( \Omega cm^2 ))</th>
<th>Resistivity, ( \rho ) (in ( \Omega cm ))</th>
</tr>
</thead>
<tbody>
<tr>
<td>Sample 1</td>
<td>20s, 700 °C, Pure B</td>
<td>3.42x10^{-7}</td>
<td>-</td>
</tr>
<tr>
<td>Sample 2</td>
<td>10min, 700 °C, Pure B</td>
<td>2.65x10^{-2}</td>
<td>( \approx 4 - 5 \times 10^4 )</td>
</tr>
<tr>
<td>Sample 3</td>
<td>30min, 700 °C, Pure B</td>
<td>8.52x10^{-2}</td>
<td>( \approx 10^4 - 10^5 )</td>
</tr>
<tr>
<td>Sample 4</td>
<td>500 °C, Pure B</td>
<td>4.78x10^{-4}</td>
<td>-</td>
</tr>
<tr>
<td>Sample 5</td>
<td>400 °C, Pure GaB</td>
<td>4.01x10^{-4}</td>
<td>-</td>
</tr>
</tbody>
</table>
Figure 3.10: Comparison of contact resistance measured from CBKR structures with two different processing conditions

Table 3.3: CBKR and Two-Terminal Comparison

<table>
<thead>
<tr>
<th>Sample No.</th>
<th>$\rho * t$ (in $\Omega cm^2$) - from CBKR</th>
<th>$\rho * t$ (in $\Omega cm^2$) - from two-terminal</th>
</tr>
</thead>
<tbody>
<tr>
<td>Sample 1</td>
<td>3.42x10^{-7}</td>
<td>4.23x10^{-7}</td>
</tr>
<tr>
<td>Sample 2</td>
<td>2.65x10^{-2}</td>
<td>2.42x10^{-2}</td>
</tr>
<tr>
<td>Sample 3</td>
<td>8.52x10^{-2}</td>
<td>7.16x10^{-2}</td>
</tr>
<tr>
<td>Sample 4</td>
<td>4.78x10^{-4}</td>
<td>3.81x10^{-4}</td>
</tr>
<tr>
<td>Sample 5</td>
<td>4.01x10^{-4}</td>
<td>4.33x10^{-4}</td>
</tr>
</tbody>
</table>

3.2 PureB in $p^+n$ configuration

The most common requirements for a junction doping technology are

- high doping efficiency
- ideal junction (defect-free)
3.2 PureB in $p^+n$ configuration

In this section we shall see PureB junctions demonstrate very high doping efficiency and good junction quality. CVD PureBoron was deposited as $p^+$ junctions in diodes and emitters in BJTs, under different processing conditions. These devices were later characterized to test the quality of the junction and doping. From the $I-V$ characteristics of the PureB $pn$ junctions in diode and BJT we can understand how the deposition conditions affect the normal working of these devices. Gummel plot was performed on the BJTs, which is a measurement of the base ($I_B$) and collector ($I_C$) currents as a function of the emitter-base voltage, $V_{BE}$ for a constant base-collector voltage, $V_{BC}$. Many important parameters can be studied from this plot, namely,

- the common-emitter current gain, $\beta = \frac{I_C}{I_B}$
- ideality factors of the junctions
- quality of the emitter-base junction

The third parameter is a very crucial one because it will reveal if PureB deposition has caused any defects. By extracting the Si band-gap at the interface, we can determine the quality.

Current from a $pn$ junction can be expressed empirically in the form [28]

$$I \approx \exp\left(-\frac{E_g - qV}{nkT}\right)$$  \hspace{1cm} (3.5)

where $E_g$ is the semiconductor junction band-gap, $V$ is the applied voltage, $n$ is the ideality factor, $k$ is the boltzmann constant and $T$ is the temperature at which measurement is performed.

Thus by measuring the base and diode $I-V$ plots at different temperatures, we can extract the $E_g$. The base current is due to the injection of electrons from base into emitter. If the PureB deposition has caused any damage, then the base current will be far from ideal ($n > 1$) and $E_g < 1.12eV$ (Si band-gap). Thus it is a measure of the quality of the emitter-base junction. Also from $\beta$, we will have an idea about how good the base electrons are suppressed.
at the emitter. It is a measure of the the doping of the junction. Higher the doping, higher the suppression and lower the base current, $I_B$.

### 3.2.1 $pnp$ Bipolar Junction Transistor

Figure 3.11 shows a schematic of a bipolar transistor fabricated with PureB deposited emitter. Different process conditions were considered (see table 3.4) and gummel plots were measured for these devices.

**Figure 3.11:** Schematic of a vertical bipolar transistor with PureB deposited emitter

#### Table 3.4: BJT Process Conditions

<table>
<thead>
<tr>
<th>Sample No.</th>
<th>Deposition Parameters</th>
<th>Gain, $\beta$ (@ 25°C)</th>
<th>$E_g$ (in eV)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Sample 1</td>
<td>20s, 700°C, Pure B</td>
<td>16.5x10^{-2}</td>
<td>1.24</td>
</tr>
<tr>
<td>Sample 2</td>
<td>10min, 700°C, Pure B</td>
<td>26.8</td>
<td>1.13</td>
</tr>
<tr>
<td>Sample 3</td>
<td>30min, 700°C, Pure B</td>
<td>36.7</td>
<td>1.18</td>
</tr>
<tr>
<td>Sample 4</td>
<td>500°C, Pure B</td>
<td>9.11</td>
<td>1.10</td>
</tr>
<tr>
<td>Sample 5</td>
<td>400°C, Pure GaB</td>
<td>8.78</td>
<td>1.17</td>
</tr>
<tr>
<td>Sample 6</td>
<td>400°C, Pure Ga</td>
<td>4.86x10^{-2}</td>
<td>1.16</td>
</tr>
<tr>
<td>Sample 7</td>
<td>Implanted Emitter (Run # DI1464, W1)</td>
<td>15.2</td>
<td>1.24</td>
</tr>
</tbody>
</table>

Figure 3.12 gives the collector and base currents from samples 1 – 3, measured at room temperature (25°C) for a 1x2µm² area emitter. We can see that even for a 20 seconds deposition sample, there is collector current measured. When there is hole injection from
emitter into collector through the base, collector current occurs. So this is an indication of the surface being p-doped. From figure 3.12b we see that the base currents for both 10 minutes and 30 minutes deposited samples are very low and have an ideal behaviour \((n \approx 1.02)\). The electrons injected from the base are being suppressed at the emitter-base junction. If there were defects then this would not be the case. This tells us that the junction is heavily doped and it is defect-free. We also see that for the 20 seconds deposited sample the base current is about two orders of magnitude higher than the longer deposition time samples. This is because, from such a short deposition time, the surface is not as heavily doped as the other two. So there is not enough holes to suppress the electron injection from base.

Sample 7 is a reference sample with an implanted emitter junction used for comparison purposes. Samples 5 & 6 have pure GaB and pure Ga deposited as emitters at low a temperature. Pure GaB like pure B has excellent properties \([11]\) and it will be useful to compare and study the electrical characteristics of these materials. This experiment spread is very interesting because emitters with different deposited materials and an implanted emitter are compared and also low temperature processes are studied. Figure 3.13 shows the collector and base currents compared between different samples. The collector currents of the deposited emitter and the implanted emitter (plotted in red) have the same ideal behaviour. We can notice that the implanted emitter current is slightly lesser than the deposited ones in the ideal-diode region. Also in the reverse-bias condition, the saturation current for deposited emitters are an order of magnitude less compare to the implanted emitter. This indicates that the surface of the deposited emitter has a high doping efficiency compared to the implanted emitter. Also interesting is that this characteristic is observed for materials deposited at a lower temperature \((< 700^\circ C)\). This only validates the effectiveness of the pure B technology. Figure 3.13b gives the base currents for these samples. A couple of points to be noted here

- The base current for a 700°C pure B matches that of the implanted emitter in the ideal-diode region, while the current for the implanted device goes on to increase. This indicates that PureB suppresses the electron injection much more effectively than the implanted one
Figure 3.12: Collector and Base Currents for 700°C PureB. The emitter area is 1x2µm². The measurement was performed at room temperature.
3.2 PureB in \( p^+n \) configuration

- When the deposition temperature decreases the PureB doping also decreases, thereby increasing the injection of electrons and hence an increase in the base current. This is very clearly observed from the data. The base currents from the 500°C pure B and 400°C pure GaB are higher than the 700°C pure B. Even when we look at the 500°C pure B and 400°C pure GaB, the former is slightly less due to the relatively higher pure B doping. And finally for a zero B material, i.e. pure Ga, the base current is about 2 – 3 orders of magnitude high. These factors are also supported by the current gain values obtained (see table 3.4). This is a fine indication how effective and useful pure B deposition can be.

**Arhenius Plot**

Now that we have seen pure B has a very high doping efficiency and better electron suppression compared to an implanted emitter, let us go a step further and validate the formation of a defect-free junction. For this we performed gummel plots at different temperatures between –10°C to 150°C. For example, the collector and base currents measured at different temperatures for the 500°C pure B is shown in figure 3.14. Then by applying the equation 3.5 we extracted the Si band-gap, \( E_g \) at the interface. This relation between current and inverse of temperature is termed as 'arhenius plot'. The arhenius plot for the 500°C pure B sample is shown in figure 3.15.

If pure B deposition induces defects at the junction, then the recombination current \( (n \geq 2) \) will be dominant and value of \( E_g \) extracted from the arhenius plot will be close to 0.6eV (half of the Si band-gap). Table 3.4 lists the values of \( E_g \) extracted for the 1x2\( \mu m^2 \) emitter area devices fabricated under different conditions. We can see that the \( E_g \) is close to 1.12eV or in other words, the PureB deposition does not cause damage and we get a defect-free junction.

**3.2.2 \( p^+n \) Diode**

Now that we have demonstrated advantages of pure B deposition, it is time to study the influence of deposition conditions on the junction in detail. For this purpose \( p^+n \) diodes were
Figure 3.13: Comparison of collector and base currents under different process conditions. The emitter area is 1x2 \mu m^2. The measurement was performed at room temperature.
3.2 PureB in $p^+n$ configuration

![Graph](image)

(a) Collector Current

![Graph](image)

(b) Base Current

**Figure 3.14:** Collector and Base Currents at different temperatures. The emitter area is $1x2\mu m^2$.
3.2 PureB in $p^+n$ configuration

Fabricated and characterized. We already have the proof of concept, i.e bipolar transistors with pure B deposited emitters, so we turn the attention to diodes for further analysis since they are simple and quick to fabricate. Similar analysis procedure as earlier was followed in order to extract the $E_g$ for diodes. Many processing conditions, such as deposition pressure, deposition temperature, carrier gas were changed for this study. For the discussion here we shall consider two devices fabricated in similar conditions but differing in the deposition pressure (see table 3.5). Sample 1 was fabricated at atmospheric pressure and sample 2 at reduced pressure of 95 Torr. The table 3.5 also lists the extracted $E_g$ for 1x2$\mu$m$^2$ diode area devices. We see that sample 1 has larger deviation of $E_g$. This can be explained from the chemistry involved in the pure B deposition. If we recall from section 1.1, many reactions occur during the course of the deposition. There are also a few reactions involving the Si surface sites that are passivated with H atoms (Si_H). When the pressure inside the deposition chamber is high, the carrier gas concentration, which is H$_2$ here, will also be high. So there will be many H atoms available and hence more sites passivated with H (Si_H). The B atoms have to fight with H$_2$ for the deposition since the ambient temperature (450°C) is not high enough to release the Si_H bonds. This decreases the probability of PureB deposition. So uniform deposition of PureB is not possible. This results in lumpy formation and so the contact metal deposited will see

Figure 3.15: Arhenius plot of a 500°C pure B sample. The emitter area is 1x2$\mu$m$^2$. 
3.3 PureB 'gated' JFETs

The Silicon Device Integration group in DIMES has successfully developed and fabricated pure boron (PureB) based Silicon Photodiodes for application in Scanning Electron Microscopes (SEM). These detectors used in SEM have a low sensitivity and a good low-noise pre-amplifier stage is desired to prevent the degradation of the signal obtained from the detector [13]. It is well understood that On-Chip integration of electronics gives the best performance including high signal-to-noise ratio, low parasitic capacitance. In general, Junction Field Effect Transistors (JFETs) have proved to be one of the best candidates available for low-noise pre-amplifier application [29, 30]. On-chip integration of JFETs with detectors will be easier if the JFET fabrication process is compatible with the PureB detectors and greatly simplified if a low-temperature scheme (< 700°C) is considered.

During the course of this work, n-channel JFETs fabricated with pure B deposited shallow gates, with deposition temperatures of 500°C, were electrically characterized to study how good the pure B gate can control the implanted channel. The JFETs were fabricated in parallel with the bipolar transistors, using the same process flow. The JFETs were designed as ring structures, as shown in figure 3.16. The gate length is given by the difference in the outer and inner ring radii of the top gate ring. Devices with the following gate lengths were used - 1µm, 2µm, 4µm, 6µm, 10µm.

The ring gate structure was developed to improve the control of the gate over the channel. These structures are so designed, such that the top gate width, which is the circumference

<table>
<thead>
<tr>
<th>Sample No.</th>
<th>Deposition Conditions</th>
<th>$E_g$ (in eV)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Sample 1</td>
<td>450°C, H$_2$, atm</td>
<td>0.89</td>
</tr>
<tr>
<td>Sample 2</td>
<td>450°C, H$_2$, 95 Torr</td>
<td>1.24</td>
</tr>
</tbody>
</table>
of the top gate ring, is kept a constant throughout for all gate lengths. This will solve the problem of fringing currents that are usually present in a normal structure by allowing to subtract those parasitic contributions. Figure 3.17 shows the top view of a ring structure JFET, fabricated in DIMES, used for characterization.

In this analysis we shall compare the DC characteristics of JFETs with implanted gate and a 500 °C pure B deposited gate. Figure 3.18 shows the output characteristics for a 4µm gate length device with different process conditions. At first look, we see that the implanted gate
device has a very low saturation point (pinchoff) and for a gate-source-voltage ($V_{GS}$) of as low as $-0.5V$, the drain current, $I_D$ is almost negligible. This shows that the top gate has an extremely good control over the channel, courtesy of the heavy gate implantation. The figure also shows the plot for a $500^\circ C$ PureB deposited device. The saturation point looks relatively high and even for $V_{GS} = -4V$, the $I_D$ is going strong. We must keep in mind that the pure B was deposited at a low temperature of $500^\circ C$. From section 3.2.1, we clearly know that at such a low temperature the doping efficiency reduces. However, the point to be noted is that even at such a condition, we get obvious JFET characteristics.

For a fixed $V_{GS}$, as $V_{DS}$ increases, such that the top-gate-to-channel junction is reverse biased, a reverse bias leakage current flows through the top gate. The leakage is a measure of how good the junction is and it has to be as low as possible. Figure 3.19 compares the gate leakage current for the implanted and the PureB JFETs. We can see that the PureB device has a lower leakage ($\approx 2$ times less) even for such a high reverse-biased condition. This again is an indication of how good the junction is and we can imply that PureB does not cause any damage to the junction.

Figure 3.20 shows the channel resistance ($R_{ch}$) as a function of the top gate length. $R_{ch}$ was calculated from the reciprocal of the channel conductance for the condition where $V_{DS} \approx 0$, $V_{GS} \approx 0$. The PureB JFET has a lower $R_{ch}$ compared to the implanted one. Also the plot is linear for the PureB device (see inset). The observed trend could be because in a JFET with implanted gate, the dopants could out-diffuse and reduce the channel width thereby increasing the $R_{ch}$.

The transconductance ($g_m$) of a JFET can be extracted from the transfer characteristics ($I_D$ vs $V_{GS}$). The $g_m$ is given by the slope of the transfer plot for the condition $V_{DS} \geq V_{DS}(sat), V_{GS} \approx 0$. Figure 3.21 gives the $g_m$ of the two devices for different gate lengths. At this point we cannot directly compare and explain the differences observed in the $R_{ch}$ and $g_m$ between the implanted and PureB JFETs. Simply because, there are various process parameters involved. More runs and measurements will give a better insight into this. From the results we can realize that it is possible to obtain JFET characteristics with a low
Figure 3.18: Comparison of Output Characteristics of JFET. The gate length is $4\mu m$. 

(a) Implanted Gate

(b) $500^\circ C$ PureB Deposited Gate
Figure 3.19: Comparison of Top Gate Leakage for different gate lengths

Figure 3.20: Comparison of Channel Resistance for different gate lengths
temperature pure B deposition. The aim of this exercise is to have a proof of concept, that on-chip integration of JFETs with pure B detectors can soon be a reality.

Figure 3.21: Comparison of Transconductance for different gate lengths
Chapter 4

Conclusions

Diodes fabricated with pure B layers under multiple processing conditions have been electrically characterized to get the bigger picture of process influence on device performance. Bipolar Transistors (BJT) with boron deposited shallow emitters have been studied and compared with an implanted emitter BJT. The resistivity of pure B has been critically analyzed.

The DC characteristics of the devices and all the parameters needed to evaluate the physical properties of pure B layers have been presented. The device structures have been described. Thickness and resistivity results confirm the process and pattern dependency of deposition rate of PureB. About two orders of difference in magnitude is observed in the resistivity of PureB layers measured from two different structures and techniques. However, the results from each method are individually consistent. The difference in processing steps and patterns present on the wafers are suspected to be the reasons for the deviation in the results. Nevertheless, further study is required before anything concrete is concluded.

Diodes and BJTs with an ideality factor close to 1 have been fabricated with PureB. The crucial role played by deposition conditions is revealed from the results of the pure B diode characterization. One such influence of deposition pressure has also been discussed. The common-emitter current gain and the trend observed between the base currents of boron and
gallium based transistors, sufficiently support the theory that pure B have a higher doping-
efficiency and superior electron-injection-suppression. It has also been identified from the
arhenius plots of the $I - V$ that pure B do not cause any damage to the junction during
deposition making it a favourable candidate for ultrashallow junction doping.

JFETs with pure B deposited gate have been characterized. The output characteristics,
channel resistance and the transconductance have been presented. It has been identified
that it is possible to successfully fabricate a working JFET from low temperature PureB
deposition. More experiments and measurements are needed to completely understand and
optimize the process parameters to get the desired output.


