Reduction of UHF Power Transistor Distortion With a Nonuniform Collector Doping Profile

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Abstract—The linearity of a class-A, bipolar UHF power transistor is investigated. The device is intended for transmission of signals with multiple (TV) channels. Mixing between the various channels must be suppressed, which makes linearity an important parameter. This paper presents a novel approach, where *process technology* is specifically optimized to minimize distortion. It is shown that particularly the nonlinear collector–base capacitance strongly affects the linearity of this type of device. With a modified collector–base doping profile, the capacitance is manipulated. A nonuniform profile is introduced that significantly reduces third-order intermodulation. The profile consists of an arsenic doped spike that is grown epitaxially into the (otherwise) lightly doped collector. This reduces the bias dependence of C_{cb} and improves the tradeoff between linearity and breakdown or ruggedness. The reduction in third-order intermodulation is demonstrated both experimentally and by mixed-level MDS/MAIDS simulations.

Index Terms—Bipolar transistor, collector–base capacitance, epitaxy, intermodulation distortion.

I. INTRODUCTION

INTERMODULATION distortion is a key parameter for many RF circuits. In particular, transmitters for signals containing multiple channels (e.g., TV signals) have tight constraints on intermodulation to suppress mixing between channels.

Despite the fact that distortion originates primarily inside the active devices of a circuit, solutions are most often sought in the domain of *systems* and *circuit design*. Here a different approach is presented where distortion is minimized by specifically optimizing *process technology*.

An important source of distortion comes from nonlinear feedback by the collector–base capacitance. This capacitance is primarily determined by the doping profile of the n^- collector region. Unfortunately, optimization of this profile is restricted by requirements on breakdown voltage (BV_{cb0}).

BV_{cb0} of HF power devices is typically much higher than strictly necessary for normal operation because the device must be able to withstand some degree of abuse (ruggedness). The device must not be destroyed when it is loaded with a large impedance mismatch. Therefore, BV_{cb0} is increased by using a (too) wide and lightly doped collector. This shifts the optimum bias point for minimum distortion [1] away from the nominal bias point. In fact, it is shifted completely out of the safe operating area (SOA) into the area in the I_C – V_{ce} plane where the maximum power dissipation of 50 W is exceeded. Consequently, the point of maximum linearity cannot be used without exceeding the maximum power-dissipation limit.

Ruggedness will be represented by BV_{cb0} , under the assumption that these two parameters are strongly correlated. Although many other parameters can be associated with ruggedness (e.g., packaging, emitter-ballasting, transistor-layout), BV_{cb0} is considered to be the most strongly related to the areas of *process technology* and *device physics*, which are most relevant for the concept discussed here.

In this paper, a nonuniform collector doping profile is introduced that improves the tradeoff. Linearity and ruggedness are decoupled to a certain degree, which makes ruggedness a less dominant factor. This allows the bias point with maximum linearity to be shifted back into the SOA. The concept is evaluated using the mixed-level simulator MAIDS (Microwave Active Integral Device Simulator) [2].

MAIDS is a *device* simulator incorporated within Hewlett-Packard's Microwave Design System (MDS). This combination is capable of performing combined harmonic-balance and device simulations of complete RF circuits [3]. A bipolar device is specified in terms of doping profile and semiconductor material parameters rather than extracted compact model parameters. This explicit specification of the doping profile circumvents the limitation of compact models which must implicitly assume a certain shape in the doping profile (in most cases a uniformly or linearly graded profile). Hence, a tool like MAIDS is essential for evaluating devices with a more exotic, nonuniform collector doping profile as that presented here.

The simulated profile is then experimentally verified. For this purpose, special devices have been fabricated and measured. They are based on the (commercially available) Philips BLW-898 bipolar UHF linear power transistor, intended for linear amplification of signals in the 470 to 860 MHz frequency band. Experimental collector doping profiles were fabricated by using a newly developed epitaxy process that enables fabrication of sharp (50 nm wide) arsenic doped spikes [4], [5].

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Fig. 1. Measured output power at fundamental and third-order intermodulation frequencies for various collector currents (for Philips BLW-898 at 860 MHz and $V_{cc} = 25$ V). The nominal bias current ($I_c = 1.1$ A) is also indicated.

II. BACKGROUND

In bipolar transistors, two nonlinear components are of importance:

- the exponential dependence of collector-current and emitter-base (e-b) storage charge on e-b voltage; closely related to the transconductance ($g_m = dI_c/dV_{be}$);
- the nonlinear dependence of collector-base admittance on collector current and voltage; closely related to collector-base capacitance (C_{cb}).

In the following qualitative explanation, it will be clarified why these nonlinear elements are fundamentally different and why they should be considered separately.

All the higher order derivatives of g_m are approximately proportional to I_c due to the near exponential relationship between I_c and V_{be} . By increasing I_c , the forward gain can be increased. In this case, the overall gain already stabilizes at a low current density (where high current effects are still insignificant) due to local feedback from bondwires and emitter resistance. P_3 (power at third-order intermodulation frequencies), however, continues to decrease sharply with increasing I_c (at a constant input power) because the forward gain is still increasing. This is equivalent to the case whereby amplifier distortion is decreased by increasing the loop gain.

However, when a dominating nonlinearity appears in the feedback (β), an increase in loop gain ($A\beta$) will not decrease P_3 anymore ($\lim_{A \rightarrow \infty} P_{out}/P_{in} = 1/\beta$) [6]. So when I_c is increased, distortion dominated by g_m will decrease until it eventually drops below distortion caused by feedback nonlinearity that depends on the nonlinear coefficients of β (primarily C_{cb} for HF power BJTs [7]).

This is verified by examining P_3 and P_{out} versus I_c , shown in Fig. 1. It has been measured by applying a two-tone input signal (at $f_1 = 859.5$ MHz and $f_2 = 860.5$ MHz; $P_{in} \approx 6$ dBm) to the device. P_3 is then measured at $f = (2f_1 - f_2)$ and $f = (2f_2 - f_1)$ (the magnitude of both components is equal).

Indeed, a sharp slope in P_3 is observed at low I_c , followed by an abrupt transition (also observed in [1], [7], [8]). The high-frequency (HF) class-A power transistor considered here is typically biased beyond this point (nominal bias in the figure). Here

Fig. 2. (a) Schematic representation of the distribution of electric field in the collector for increasing V_{cb} . (b) The maximum electric field versus V_{cb} , for both a "reach-through" and a wide collector.

g_m -related distortion is negligible compared to that caused by C_{cb} .

It must be emphasized that these two regimes correspond to effects taking place in different regions of the device. Therefore, it is imperative to determine which regime is relevant prior to attempting technology optimization.

These considerations indicate that the collector region is most relevant. Hence, efforts to improve the linearity of this device must be directed toward C_{cb} nonlinearity, which can be influenced by modifying the collector doping profile. However, this could also affect the breakdown-voltage (BV_{cb0}). Therefore, BV_{cb0} must also be evaluated for a fair comparison.

III. THE COLLECTOR DOPING PROFILE

Traditionally, a collector doping profile consists of a highly doped sub-collector which is formed by the substrate or a buried layer, and a lightly, uniformly doped epi-layer placed between the sub-collector and the collector-base junction. This region is required to accommodate the electric field induced by the collector-base voltage (V_{cb}). In Fig. 2 the field distribution in such a collector is shown schematically for different V_{cb} s (the triangular area). To prevent breakdown, E_{max} must be kept below a given threshold (E_{crit} ; determined by material parameters). To achieve this, the collector is made wide and lightly doped when operation at high V_{cb} is required. Conversely, for a low V_{cb} , a narrow and highly doped collector can be used, which is beneficial for the high-frequency performance.

The power transistor considered here has a very wide collector. Under normal operation, the space charge region does not extend all the way into the highly doped subcollector, but ends somewhere in the lightly doped collector region. As V_{cb} increases, both E_{max} (the maximum electric field) and the width of the space charge region increase. The net result is that E_{max} increases approximately as the square root of V_{cb} .

Once the space-charge region touches the highly doped sub-collector, the *reach-through* condition is reached. The depletion layer is now confined between the highly doped regions of the base and subcollector. As a result, E_{max} increases nearly linearly with V_{cb} . This is shown in Fig. 2, where V_{rt} indicates the onset of "reach-through."

Beyond V_{rt} , E_{max} in a narrow collector increases more rapidly with increasing V_{cb} than in a wide collector that has not reached the "reach-through" condition yet. Therefore, a narrow

Fig. 3. Doping profile of an n^+ spike collector with the corresponding electric field for a normal and high V_{ce} (25 and 50 V). The two design parameters W_{top} and ΔE are indicated.

collector results in a lower BV_{cb0} and a poor ruggedness. For linearity, however, the “reach-through” condition is highly desirable because the fixed depletion-layer width reduces the bias dependence of the collector–base depletion capacitance.

Both collector design concepts can be found in commercially available transistors. For devices where ruggedness is most important, a wide collector is used, and for devices where linearity is more important, the “reach-through” concept is used. This paper introduces a profile that is actually a combination of the two, resulting in a better tradeoff between breakdown and linearity.

The profile consists of a sharp n-type spike that is introduced in the collector. It is designed so that with normal bias the collector–base depletion layer ends in the spike ($V_{ce} = 25$ V). This is shown in Fig. 3. The depletion boundary is *pinned* to the spike, thus reducing the variation in depletion width. This results in a lower C_{cb} variation. When a high collector–base voltage ($V_{ce} = 50$ V) is (inadvertently) applied, the spike is depleted, and the depletion layer extends into the low-doped region between the spike and the buried layer ($3 < x < 6$ μm). The regained square root dependence of E_{max} on V_{cb} will now enhance *buffering* of the excess voltage.

In the ideal situation, a delta-doped spike is placed so that, under normal bias, the depletion layer boundary is pinned at this one position. When V_{ce} is further increased, the spike is fully depleted. The limitation on the total doping in the spike is that it should be completely depleted well before breakdown. To meet this requirement, the increase in electric field, ΔE , resulting from depletion of the spike, must be kept below 0.20 MV/cm (E_{crit}). ΔE will be used to represent the magnitude of the spike. It follows from Poisson’s equation that this value is proportional to the total charge in the spike.

In the experimental situation, the as-grown spike has a finite width of about 50 nm and maximum doping levels around 10^{17} cm $^{-3}$. Thus the spike width is 100 times smaller and the peak doping 100 times higher than that of the ≈ 5 -μm-wide, lightly doped (3×10^{15} cm $^{-3}$) collector region. This is a good approximation of a delta-doped spike. In the experimental situation, the distance from the spike to the silicon surface (W_{top}) is used to adjust the optimal bias point. The situation shown in Fig. 3 with

$\Delta E = 0.07$ MV/cm, $W_{top} = 3$ μm and biasing at $V_{ce} = 25$ V results in a BV_{cb0} that is about 20% lower than that for a uniform profile of the same width and magnitude. Doubling the collector voltage to 50 V increases the maximum electric field by only 53%, which demonstrates the buffering mechanism. The pinning effect can be traded for buffering by varying the magnitude or position of the spike, resulting in more flexibility when making the tradeoff between breakdown/ruggedness and linearity.

IV. SIMULATIONS

In the following simulations, two devices with the basic doping profile shown in Fig. 3, have been compared:

- a reference device with no spike in the collector;
- a spike device where the spike itself is defined as a Gaussian profile with a width of 50 nm and $\Delta E = 0.07$ MV/cm.

Moreover, the accuracy of the simulations has been verified by comparison to measurements of the standard Philips BLW-898 transistor as reference device.

A. Device Simulations

The influence of the spike on the current–voltage dependence of C_{cb} has been investigated with device simulations carried out in MAIDS. The collector–base capacitance and cb-conductance (caused by avalanche) of the intrinsic device have been calculated for various collector voltages and currents. This analysis gives no quantitative information about the device linearity, but it is very suitable for determining (within a short simulation time) the optimum bias point and the bias regions where various physical effects dominate.

First contours of constant collector–base (feedback) conductance and susceptance ($j\omega \cdot C_{cb}$) have been simulated. In Figs. 4 and 5 they are plotted on the I_c – V_{ce} plane. The feedback varies 0.5 mS between adjacent contours. In addition to the contours, two other lines are shown: the line enclosing the safe operating area ($I_c \cdot V_{ce} \leq 50$ W, the upper limit for power dissipation) and lines approximating the domain of a 35-dBm two-tone signal at the output (load line).

The region with the lowest density of contours has the lowest variation in feedback admittance and can therefore be assumed to have the highest linearity [1]. This region is indicated by the dotted circle in Figs. 4 and 5.

Important sources of nonlinearity can be identified from the figure. The depletion capacitance variations dominate when V_{ce} is low (indicated by D.C.), the effects of quasi-saturation dominate at high I_c and low V_{ce} (indicated by Q.S.), and avalanche multiplication effects dominate at high V_{ce} (indicated by A.M.). The position of the load-line in Fig. 4 confirms that the linearity is limited by the variation of depletion capacitance at low power levels, whereas quasi-saturation dominates at high power levels.

Fig. 4 shows the situation for the reference device. The most linear region is seen to lie outside the safe operating area (indicated by the dotted circle) and can therefore normally not be exploited.

The situation for the spike device is shown in Fig. 5. With respect to the reference device, the most linear region has be-

Fig. 4. Contour lines of constant feedback admittance (in mS at 860 MHz) and conductance (in mS) for the reference device. Also included are the boundary of maximum power dissipation ($P_{diss} = 50$ W) and an approximate load line that corresponds to 35-dBm output power. The dotted circle indicates the optimum bias region.

Fig. 5. Contour lines of constant feedback admittance (in mS at 860 MHz) and conductance (in mS) for the spike device ($W_{top} = 3 \mu\text{m}$, $\Delta E = 0.07$ MV/cm). Also included are the boundary of maximum power dissipation ($P_{diss} = 50$ W) and an approximate load line that corresponds to 35-dBm output power. The dotted circles indicate the shift of the optimum bias region.

come smaller but has been shifted into the safe operating area (from the gray to the black dotted circle). The quasi-saturation boundary is moved to slightly higher currents, but the most distinct difference is the decreased variation of the depletion capacitance at the nominal bias point ($I_C = 1$ A, $V_{ce} = 25$ V). This illustrates the effect of pinning the collector-base depletion boundary to the spike.

B. Mixed Level Harmonic-Balance/Device Simulations

For a quantitative investigation of linearity, not only an accurate model of the device is necessary but also the circuit in which it is used must be described. For this purpose, the class-A test circuit provided in the Philips BLW-898 documentation has been implemented in MDS. A schematic of the simulation circuit is given in Fig. 6.

The circuit provides bias and matching from 50Ω to the device impedances at 860 MHz. The package, prematch capacitor, and bondwires of the device are included in the simulation cir-

cuit because they strongly influence the device impedances. A schematic of the internal circuitry is given in Fig. 7.

The package is included as an S-parameter dataset and the prematch capacitor as a lumped element. The inductances and coupling of the bondwires were determined from their geometry by using a physical model [9]. They are implemented in the simulation circuit as lumped elements. Finally, the active (silicon) part of the device has been included in two ways: as a MEXTRAM compact model for quick simulations [10] and as a set of MAIDS elements for accurate modeling of nonuniform collector doping profiles [2]. The intrinsic device, the extrinsic device, and the active area perimeter are represented by three separate MAIDS elements.

The internal and external circuitry is kept constant for all devices that are considered. The circuitry is optimal for the reference device.

With harmonic balance simulations, the intermodulation distortion of the simulation circuit has been determined for a two-tone input signal with a center frequency of 860 MHz and a tone spacing of 1 MHz. In Fig. 8, both the simulated and measured output power at the fundamental and intermodulation frequencies are shown for increasing input power. With respect to the reference device, the linearity of the spike device is improved by 10 dB. The gain, however, is reduced by 1 dB due to the higher collector-base capacitance. The latter also can be observed by comparing Figs. 4 and 5. Consequently, in terms of output power, the improvement in linearity is 7 dB, which is still quite significant.

The observed improvement was not caused by the increase of C_{cb} . When C_{cb} of the reference device was increased artificially by adding a lumped capacitor, no improvement (in terms of output power) was observed.

The measurements were performed with a setup of bias tees and tuners (Microlab FXR SF-11N), which is more flexible than the test circuit. The tuners were configured to match the output and input impedance to obtain a maximum output power and a minimum input reflection ($P_{refl}/P_{input} < -20$ dB), respectively. The tuners provide a good impedance matching at the fundamental frequency, but at the higher harmonics it differs from the test circuit. This affects the intermodulation distortion at high power levels, but at low power levels ($P_{input} < 25$ dBm), a good agreement was found between the measurements and the (MAIDS or MEXTRAM) simulations of the test circuit with the reference device. Simulations where the test circuit was replaced by a dataset of S-parameter measurements of the tuners also shows good agreement with the measured values (not shown in Fig. 8). The measurements on the devices with a spike are discussed in more detail in the next section.

V. EXPERIMENTAL RESULTS

With a few minor adjustments in the process flow, the experimental BLW-898 transistor was fabricated on a series of wafers with an arsenic doped epilayer. The layers were grown in a commercially available, lamp-heated, single-wafer CVD reactor (the ASM Epsilon One). To obtain a sharp arsenic spike in the profile, a newly developed technique was applied. Hereby the *in situ* arsenic doping is accurately controlled during

Fig. 6. Schematic of the Philips BLW-898 test circuit. It provides bias and matching to $50\ \Omega$ to the input (top) and the output (bottom).

Fig. 7. Schematic of the Philips BLW-898 internal circuitry. Including the package, bondwire inductance and coupling, and the prematch capacitor.

the entire epi-growth process [4], [5]. The growth conditions (gas pressures, deposition time, and temperature) are kept well within the specification of the CVD equipment and no exceptional accuracy is required of any parameter. Hence, these layers are grown with the same reproducibility as normally achieved with this reactor (in the order of a few percent).

The doping profiles of typical “as-grown” spikes, as determined by CV profiling through a thin top-layer, are shown in Fig. 9. The corresponding ΔE is also calculated from these measurements. It increases from 0.05 to 0.35 MV/cm as the doping in the spike is increased.

In the epi-layers used for the experimental transistor fabrication, two parameters were varied: the spike magnitude, resulting in ΔE values of: 0.04, 0.046, 0.077, and 0.10 MV/cm, and the top-layer thickness, resulting in W_{top} values of 2, 2.5 and 3 μm. Uniformly doped epi-layers with a thickness of 2, 3, and 5.5 μm were also included for comparison.

The (on-wafer) measured C_{cb} of devices with a ΔE of 0.077 MV/cm is shown in Fig. 10. The transition of the depletion

Fig. 8. Total input power versus total output power is shown for the fundamental and third-order intermodulation frequencies of a two-tone signal at 860 MHz with a 1-MHz tone spacing. Simulations on the reference and spike profile were carried out with MAIDS. The validity of MAIDS is substantiated by MEXTRAM simulations and measurements of the reference device.

boundary from the pinning to the buffering region can be identified from the figure.

For the available devices, the open-emitter breakdown voltage (BV_{cb0}) is shown in Table I. The table shows that the buffering is only effective in devices with a 2-μm top layer. This is the result of slight autodoping that is still present in the epi-layers. It has doped the top layer somewhat higher

Fig. 9. CV profiles of "as-grown" arsenic spikes. The integral amount of doping is converted to ΔE (given in MVcm^{-1}).

Fig. 10. Measured C_{cb} of experimental devices with a spike magnitude of $\Delta E = 0.077 \text{ MV/cm}$ and various top-layer thicknesses ($W_{top} = 2, 2.5, 3 \mu\text{m}$). The CV curve of a reference device is included for comparison (solid line).

than anticipated. Despite considerable efforts to prevent this, the undesirable effect could not be completely eliminated. We speculate that further refinement of the epitaxy process can improve this.

Two-tone measurements were performed at 860 MHz (and 1-MHz tone spacing) with the setup of tuners and bias tees discussed in the previous section. Devices with $2 \mu\text{m}$ W_{top} are compared, as these show the most effective buffering. The results for the 0.046- and 0.077-MV/cm spike are shown in Fig. 11. With an intercept point (OIP3) in excess of 62 dBm (total output power), the experimental devices have a linearity comparable to the simulated values. The reference device has an OIP3 of 57 dBm, thus, an improvement of 5 dBm (10 dB in IM3) is achieved. However, due to the thinner top layer, this performance is obtained at a lower V_{ce} of 20 V. For the $2\text{-}\mu\text{m}$ uniformly doped collector, biased in a "reach-through" condition (the c-b depletion region extends from the base into the n^+ substrate), an OIP3 of 60 dBm was found (also shown in Fig. 11). We attribute this lower value to the fact that this device could not be biased at V_{ce} above 15 V due to oscillations caused by operating the device too close to BV_{ce0} .

The deviation of the measurements from the simulations at high power levels ($P_{in} > 25 \text{ dBm}$) is attributed to limitations of

TABLE I
 BV_{ce0} (IN V) FOR EPI-LAYERS WITH TOP-LAYER THICKNESS VARIED FROM 2 TO $3 \mu\text{m}$ (HORIZONTAL) AND A SPIKE WITH ΔE VARIED FROM 0.04 TO 0.1 MV/cm (VERTICAL) (SEE FIG. 3) VALUES FOR A UNIFORMLY DOPED EPI-LAYER ARE INCLUDED FOR COMPARISON. THE REFERENCE DEVICE HAS A UNIFORMLY DOPED ($3 \times 10^{15} \text{ cm}^{-3}$) EPI-LAYER THAT IS $5 \mu\text{m}$ THICK

	W_{top}	$2 \mu\text{m}$	$2.5 \mu\text{m}$	$3 \mu\text{m}$	ref
ΔE					
Uniform		34	NA	61	> 60
0.04 MV/cm		47	47	57	
0.046 MV/cm		46	49	58	
0.077 MV/cm		45	50	58	
0.10 MV/cm		NA	48	53

Fig. 11. Measured third-order intermodulation for spike devices with a $2\text{-}\mu\text{m}$ top layer ($\Delta E = 0.046, 0.077 \text{ MV/cm}$). The measurements of the reference device, a "reach-through" device with a $2\text{-}\mu\text{m}$ top layer, and the MAIDS simulation results (see Fig. 8) are included for comparison.

the measurement setup. For these measurements, a low ohmic bias network at the collector would be preferred over a bias tee to prevent modulation of the supply voltage [11].

VI. CONCLUSION

A nonuniform collector doping profile is introduced for bipolar RF power transistors enabling a more flexible tradeoff between breakdown/ruggedness and linearity. It is demonstrated that a doping spike in an otherwise lightly doped collector profile can reduce the variation of the collector-base depletion capacitance at a specific bias point, and thus improve the linearity of the device. With mixed-level harmonic-balance circuit/device simulations using MDS and MAIDS, the effects on linearity have been evaluated. Simulations show that the intermodulation distortion of an UHF linear power transistor is decreased by 7 dB.

Measurements on experimental devices show that the novel collector-profile increases the linearity (IM3) by 10 dB,

reaching levels that are comparable to a “reach-through” collector, while its BV_{cb0} is 35% higher.

With a stronger suppression of autodoping in the top layer, it will be possible to fabricate devices that can operate at the nominal bias point ($V_{ce} = 25$ V). Nevertheless, the present experiments clearly demonstrate the improvement that was aimed for.

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