Printed Graphene and Silicon

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Preface

This thesis is written as partial satisfaction for the requirements of the Master of Science Degree in Microelectronics at faculty of Electrical Engineering, Mathematics and Computer Science, at Delft University of Technology.

This work focuses on combining solution-processable silicon and carbon materials into devices. This work will contribute to the fabrication of quality devices by combining new materials such as graphene and liquid silicon, which have great potentials on applications in revolutionary electrical devices.

In this work, I would like to thank the people who gave me help during the bottlenecks in my research:

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Abstract

Mass production of flexible electronics can be achieved through printing electronics at low temperature. Graphene and liquid silicon are potential materials for printed electronics. We were aiming at fabricating a printed Schottky diode. Liquid silicon, the organic semiconductors and metal oxide due to its ability to transform into crystallized silicon with high mobility. Graphene was used for printed Schottky diode not only because of its promising electrical properties but also because there is lack of printed metal to form Schottky junction with silicon. This printed process is compatible with substrate with low thermal budget.

We have improved the photo-polymerization process of liquid silicon by increasing the UV irradiation 15 times. In this way, the optical properties of polysilane are more like silicon and cannot be oxidized in the open air. Thus, the liquid silicon process can be simplified. The liquid silicon was polymerized with UV irradiation and crystallized with excimer laser. We have simulated the heat transfer for polysilane under laser with 50mJ/cm². At the surface the temperature of the layer is up to 280°C and at the bottom the temperature is 40°C which indicated the laser energy induce much less kinetic energy at the bottom than the top.

We have introduced a cleaner way of transferring CVD graphene by photoresist as transfer media. This is because photoresist can be removed using mild organics like acetone. We used photonic curing system to reduce graphene oxide. In this way, the throughput is largely increased due to the ease of the process. Both of these graphene are compatible with printing process. The resistance of RGO is lower than transferred CVD graphene while the defects of RGO is much higher than CVD graphene. We have fabricated Si/graphene Schottky diode using CVD graphene and RGO. The ideality factor was 1.75 and 8.38, respectively. The work function of graphene was extracted as 4.73eV(RGO) and 4.8eV(CVD).

This work presents the possibility of liquid silicon and graphene utilized in printing electronics.

Key words: graphene, liquid silicon, printed electronics, Schottky diode
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Chapter 1
Introduction

Instead of constantly pursuing the physical limitation of Moore’s law, there are other ways to flourish the electronic industry economically and diversely. Investigations based on new fabrication methods and functions, which can be realized by new type of materials, are being implemented. The concept of printed electronics is a promising approach.

Conventional methods for electronic integrated circuits are complex and expensive due to the high-cost machinery they require. Also, these methods are based on batch processing which limits the production process. Compared to conventional methods, the reason why the printing method is appealing results from the potential of thin-film device production in a simpler and economical way through mass production. In addition, when the inks used for these printing methods processed at low temperature, new or improved functionalities such as flexible electronics can be made. By exploiting and applying new materials other than conventional semiconductors, favorable properties can be combined. So far, most of the research has focused on organic semiconductors because they are relatively easy to convert into a solution as inks. However, their electrical carrier mobility (< 1cm²/Vs) and stability are limited compared to crystalline silicon devices. Although the carrier mobility of metal oxide, such as InGaZnO, is much higher than organic semiconductors (around 30 cm²/Vs), it is still an order of magnitude lower than poly-silicon (>100 cm²/Vs).

Liquid silicon, which is a precursor of amorphous silicon in liquid phase at room temperature, presents a better choice of printed electronics because of its ability to be converted into crystallized silicon. It has been used in applications such as Thin Film Transistors (TFTs) [4,15,25] by solution process. For TFTs fabrication, researchers mainly focused on improving its performance by increasing the carrier mobility. In 2006, Shimoda, et al. [2] introduced the fabrication of poly-crystallized silicon (carrier mobility of 108 cm²/Vs) TFTs using liquid silicon. In 2012, Zhang [15,25] et al. and Trifunovic [4] reported to have fabricated single-grain silicon TFTs from Cyclopentasilane (CPS), which is one form of liquid silicon, using grain filter which greatly increased the mobility (423 cm²/Vs). Liquid silicon presents the possibility of printing electronics in mass production since it does not require a vacuum condition to fabricate devices. Because liquid silicon is highly reactive to oxygen in the open air, an inert environment is still necessary for the process. In their research, CPS was polymerized into polysilane by UV irradiation and then annealed to create a 3D silicon network. Polysilane as an intermediate product, although more stable than CPS, still can be easily oxidized in the open air. In
this case, liquid silicon can only be taken out of the inert environment after the complete transformation to a-Si. More research is needed to simplify this process.

The high speed devices made from liquid silicon show the potential to be used in high frequency circuits. These printed electronics provide a promising way to the realization of ultra-low-cost Radio Frequency Identification (RFID) tags. For printed RFID in ultra-high frequency (UHF) band, it is possible only if the mobility of the devices can achieve around 500 cm$^2$/Vs which makes liquid silicon a suitable candidate. For HF circuits, the Schottky diode is vastly used resulting from its fast recovery time (in Pico seconds) because of the small amount of stored charge. Thus, the switching ability of Schottky makes it suitable for high frequency circuit build. In order to optimize the performance of printed HF circuit, it is desirable to improve the characteristics of Schottky diode, which plays an important role in such circuits. However, there is a lack of printable metals which can form a Schottky junction with silicon. In this case, other materials are desirable. Graphene has been reported in Schottky diode fabrication with silicon by different methods [43,44,47,48,49,47]. As a carbon based material, graphene demonstrates theoretically promising electrical, mechanical, thermal and optical properties compared to conventional materials. It can be compatible with printed electronics because of its flexibility and diverse ways of production.

Transferred chemical vapor deposition (CVD) graphene and reduced graphene oxide are suitable candidates for printing electronics. The transfer method can be described as following: 1, transfer media deposition on the graphene; 2, graphene detachment from the growth catalyst by etching; 3, graphene positioning and transfer media removal. However, the most widely used transfer method with poly(methylmethacrylate) (PMMA) inevitably leaves residuals on graphene which has a large impact on the electrical properties of graphene. In this case, a cleaner way of transfer method is needed. For the reduced graphene oxide, it is theoretically more compatible with printing process due to the fact that graphene oxide is normally mixed with water as an ink. It is certain that the physical characteristics of these graphene sheets are different. However, the difference of characteristics between the Schottky diode fabricated by these two graphene sheets still remains unknown.

The schematic of the Schottky diode fabrication process can be described as in figure 1.1. The liquid silicon is transformed into poly-silicon (figure 1.1 a). After silicon doping and crystallization, graphene is deposited on silicon (figure 1.1 b). At last, the metal is deposited on graphene and silicon as electrodes (figure 1.1 c). The Schottky junction forms at the interface between graphene and silicon. The metal, as electrodes, forms Ohmic contact with silicon and graphene, respectively.
Goal

The goal of this thesis is to fabricate Schottky diode with liquid silicon and printed graphene.

Approach

In this work, Schottky diodes made of liquid silicon and two kinds of graphene will be introduced as following steps:

The photo-polymerization process of liquid silicon will be optimized using UV irradiation with higher energy in order to produce stable polysilane. The polysilane will be annealed and crystallized using excimer laser. In this way, liquid silicon is able to be deposited on arbitrary substrates with low thermal budget such as paper or plastic.

Graphene will be prepared using two ways: CVD growth and graphene oxide reduction. A new way of transfer method for CVD graphene will be introduced using photoresist and an adhesive Gel-Pak. In this way, the transfer media residuals can be decreased greatly. And graphene oxide will be reduced using a photonic curing system. In this way, the throughput of graphene will improved.
Si/graphene Schottky diodes will be designed and fabricated using CVD transferred graphene and reduced graphene oxide, respectively. The diodes will be characterized and compared using I-V measurements.

**Thesis Structure**

Liquid silicon polymerization is discussed in Chapter 2. The graphene transfer and graphene oxide reduction is presented in Chapter 3 followed by the graphene Schottky diode in Chapter 4. Conclusion and discussion are made regarding to the previous chapters in Chapter 5.
Chapter 2
Formation of stable printed polysilane layers

Liquid silicon as a precursor of amorphous silicon plays a big role in printed electronics. In order to fabricate a printed Schottky diode on arbitrary substrate, liquid silicon is required to be transformed into amorphous silicon and crystallized. The general transformation from liquid silicon to amorphous silicon can be described as: (1) liquid silicon polymerization using UV irradiation to produce polysilane and (2) polysilane pyrolitic transformation to a-Si. However, the polysilane as the intermediate product during transformation is not stable which means polysilane can be easily oxidized in the open air. In this chapter, we focus on producing stabilized polysilane using UV irradiation with higher density in order to simplify this process. Since the optical properties of polysilane and silicon oxide are very different, the stability of the polysilane will be confirmed by optical measurements. The polysilane will be crystallized using excimer laser. The heat transfer simulation of polysilane under laser will be made to understand the heat distribution during crystallization and the thermal effect polysilane could be induced to the substrate.

2.1 Introduction

In this thesis, the term ‘liquid silicon’ refers to a family of silicon compound in liquid state at room temperature. Theoretically, hydrosilanes are great candidates in semiconductor fabrication because they exhibit semiconductor properties when converted to solid state. The choice is then limited by either a straight molecule (\(\text{Si}_n\text{H}_{2n+2}\)), a cyclic molecule (\(\text{Si}_n\text{H}_{2n}\)) or a multi-cycled compound (\(\text{Si}_n\text{H}_{2n-2}\)) [3]. A single structure cyclic compound is preferred for two reasons. Firstly, they are more easily to polymerize due to the reason that they are highly reactive to UV light. Secondly, a single cyclic structure is easier to synthesize and purify. When \(n\) is more than or equal to 3, the compound is liquid at room temperature and will transform into amorphous silicon when the temperature reaches 300°C. For \(n\) is smaller than 10, the boiling point of the compound is less than 300°C which means this kind of compound will evaporate before decomposition because the thermal energy is not enough to break the Si-H bond. Cyclopentasilane which is \(\text{Si}_5\text{H}_{10}\) has been chosen for its high reactivity to UV light and its relative stability [5]. Thus, polymerization with UV light[3] to transform the compound into long chain molecules in order to increase the boiling point is necessary for the following thermal decomposition. CPS can be converted to poly(dihydrosilane) [1] (polysilane) by ring-opening polymerization, which occurs when UV light radiation is applied. In this thesis, liquid silicon refers to CPS. More information about CPS is shown in appendix A.
CPS recently has drawn great attention and opened up new attempts of achieving revolutionary electronics fabrication since it was found in 1973. Studies of liquid silicon are conducted in several institutes in the world. Researchers have been mainly focused the performance of devices by increasing the carrier mobility. In 2005, Shimoda, et al. introduced the fabrication of poly-crystallized silicon TFTs from CPS in which the mobility of the device reached 108cm²/Vs [2]. In 2012, Zhang et al. and Trifunovic et al. fabricated single-grain silicon TFTs from CPS using grain filter which greatly increased the mobility of the device at 423cm²/Vs [4]. In order to transfer CPS into amorphous silicon, researchers introduced an intermediate product which is polymerized CPS (polysilane). Polysilane, although much more stable than CPS, is still can be easily oxidized in the open air which means the liquid silicon can only be taken out of an inert environment when it is completely transformed into a-Si. In this work, a stable printed polysilane layer will be presented using UV irradiation with higher density. In this way, the electronic fabrication using liquid silicon can be simplified because an inert environment won’t be necessary for the following process.

In this chapter, the principle of silicon film production using liquid silicon will be introduced including photo-polymerization, pyrolytic transformation and excimer laser crystallization. The effect of UV irradiation with different intensity on liquid silicon will be studied. Optical measurements are performed for polysilane. Thermal simulation of polysilane during laser crystallization will be presented.

2.2 Amorphous silicon film produced from CPS

Normally, both CPS and polymerized CPS are highly reactive to oxygen and water: pure CPS inflames immediately when exposed to the open air; polymerized CPS turns into silicon dioxide in the open air. To avoid these reactions in order to produce high quality silicon, an inert gas environment is necessary. In this thesis, MBRAUN GmbH Glovebox filled with nitrogen gas is a perfect option as equipment to operate in this aspect (figure 2.1). In this work, most of the processing steps are taken place in the glovebox.

The glovebox is a sealed container designed to allow one to manipulate in a low level of oxygen and water atmosphere using constant gas circulation filtered by catalysts. In this way, CPS which is sensitive to these materials can be processed in an inert environment (nitrogen). Gloves are installed in the front transparent window so that users can place their hands in gloves to see and perform works.

The key features of the glovebox consist of a gas purification system (MB-20-G), a pressure gauge, an antechamber and a control panel. The gas purification system provides automated oxygen and water removal in order to reach an inert atmosphere (commonly water concentration <0.1 ppm, oxygen concentration < 0.1 ppm). The purification cylinder used for absorbing oxygen and water is made of a
copper catalyst and a molecular sieve, respectively. The pressure gauge adjusts the pressure inside of glovebox automatically while manual pressure control is also available via foot pedals. The antechamber allows the transportation of tools and materials in and out of glovebox without changing the atmosphere. The pressure and levels of oxygen and water are monitored through the control panel. In the operational area, a UV lamp called UV AHAND 250GS and a hot plate are installed so that UV exposure and thermal decomposition can be performed. The samples can be taken out of the glovebox only after the conversion to amorphous silicon.

![Figure 2.2: MBRAUN GmbH Glovebox](image_url)

### 2.2.1 CPS deposition by doctor blade coating

Doctor blade is a generic term for any steel, rubber, plastic or other type of blade used to apply or remove liquid from another surface [7]. In this work, doctor blade is used to smoothly spread the liquid on a substrate. Although spin coating is more frequently used for the same purpose and exhibits good uniformity, it inevitably wastes lots of coating materials. In addition, doctor blade is more compatible to a gravure printing system which is a great precursor for the final goal: mass production by printing silicon. Also, CPS deposition has to be done at an elevated temperature to improve wetting properties.

### 2.2.2 Polymerization of CPS

The strategy of transferring CPS into hydrogenated amorphous silicon (a-Si: H) is to convert CPS to polysilane by photo-polymerization first. When an ultraviolet (UV) light is induced on CPS, the energy provided by the radiation will cleave Si-Si bond which makes the CPS open their rings and
form – (SiH$_2$)$_5$- radicals [3]. Thus, a high molecular weight polysilane chain can be obtained. Compared with CPS, polysilane are more stable to avoid violent chemical reactions with water or oxygen, and more importantly, its boiling point becomes higher than 300°C which avoids the evaporation during thermal decomposition. The viscosity of the sample after polymerization is much higher, and it even becomes solid if the energy of UV light is high or the exposure time is long enough. This high viscosity makes the solution process impossible. Although the viscosity can be controlled by adding organic solvents, this process will possibly lead to insolubility and contamination during mixing. That’s why polysilane is not usually used as a doctor blade coating material directly at the first place.

Most of the CPS will be converted into polysilane by ring opening. However, the reaction is more complicated in practice. According to Dong Lim Kim et.al, if more than one Si-Si bond is broken in a single CPS molecule, small pieces of silicon radicals will be created and remain in the solution[8]. In addition, if the UV could provide sufficient energy, it will not only cleave the Si-Si bond (53kcal/mol) but also the Si-H bond (76kcal/mol). After the breakage of the Si-Si bond and Si-H bond, some Si atoms are combined with each other to form polysilane chains and the others become Si radicals and make no bonds. These silicon dangling bonds are connected with each other and cause the branching of polysilane. In the meanwhile, the amount of broken bonds correlates with the UV exposure time. As the exposure time increases, the bond breakings increase and the content of hydrogen would decrease until it reaches a certain point. Consequently, the molecule structures and hydrogen concentration are dependent on the type of UV and the exposure time. Both of them are in dynamic changes during the UV exposure process.
In this work, two kinds of UV system are used. One is the UV AHAND 250GS (Honle UV Technology) and the other is LED Flood Array 375 nm wavelength (Loctite Corporation). For UV AHAND 250GS, two filters are available of which the black light filter was used. The spectral distribution is displayed in figure 2.2 (a). It shows that the peak power density of this UV is around 370 nm and the power density can been seen as Gaussian distribution. There are two precautions that have to be taken when using it: First, this UV requires some warm-up time in which the irradiance gradually reaches its maximum. Thus, the irradiance is smaller than it is expected in the beginning. Second, the distance between the sample and UV has a big influence on the power density on the sample (figure 2.2 b). It exhibits the inversely exponential relationship between the distance and power.

In this work, since the UV AHAND 250GS is installed in a fixed position in the glovebox, the distance is around 20cm as a constant. According to the figure, the irradiance is about 20mW/cm$^2$.

For LED Flood Array 375 nm wavelength, the peak power density is 375 nm and within the working distance (25mm – 75mm), the typical irradiance is 300mW/cm$^2$. Due to its LED properties, the warm-up time is negligible. Also, the spectral distribution is similar as Gaussian as well. The major difference between these two UV lamps is the power density which is nearly 15 times. Thus, it can be considered that CPS will be more polymerized using LED Flood Array 375nm.
2.2.3 Transforming polysilane into amorphous silicon

Although many hydrogen atoms in polysilane are removed during UV exposure, another treatment is still needed to transform polysilane into amorphous silicon. The basic principle is to induce sufficient energy into polysilane in order to break the bond energy of Si-Si and Si-H and to create a 3D silicon network. According to previous work, this energy can be provided by thermal energy [9]. Conversion from polysilane to amorphous silicon (a-Si: H) can be achieved in temperature higher above 350°C [4][9]. Thus an inert environment is needed for its thermal annealing.

2.2.4 Silicon crystallization

Excimer Laser Crystallization (ECL) of a-Si is a relatively low temperature crystallization method for thin films [12]. The working method of ELC is the use of a high power short wavelength pulsed light source. The sufficient laser energy helps the a-Si film to reach near-complete melting state in order to convert the a-Si into a poly-Si film with large grains. Due to the shallow absorption depth of the laser in a-Si, it only heats up the film itself which makes the process compatible with substrates with low thermal budget. The pulse of the laser is required to be in nano or pico-seconds in order to prevent the heat losses due to heat transfer. The melting temperature of a-Si is about 200-300K below that of c-Si. Thus under heating crystallization it crystallizes before it melts. However, under pulsed-laser heating, the heat supply is so fast that the crystallization is bypassed, making the surface of a-Si melted. This liquid layer propagates downward because of the latent heat of crystallization and leaves polysilicon behind during cooling. If the laser energy is high enough, the polysilicon will be melted again and the liquid is allowed to cool down only after the end of the laser pulse, homogenous nucleation take place in the melt leading to small grain poly-Si. If the laser energy is not high enough, this re-melting will not occur and the film solidifies leading to fine grain poly-Si due to the relative long cooling down time.

In this work, laser crystallization is performed using Exitech M8000V System. The schematic is shown in figure 2.3. The gas used for the laser is a mixture of Xe and Cl₂ which will form the dimer of XeCl to generate 308nm wavelength radiation. In this system, 2 laser sources are used and combined by mirror M3 after attenuation. This will provide a pulse duration of approximately 25ns. Lenses LS1 and LS2 are used to guide the beam to the homogenizer which will trim the beam with a uniform spatial profile. Then the beam goes to the Field lens which sends the beam through a mask for the alignment of radiation to the Projection lens for the final exposure on the wafer surface. A quartz plate is placed between the Projection lens and the wafer to protect the lens from ablation of the sample. The X-Y-Z stage guarantees the accurate position of the wafer.
2.3 Experimental

In this section, the experimental procedure of fabricating amorphous silicon from CPS will be presented. The optical measurements for CPS, polysilane and amorphous silicon will be made. A heat transfer simulation of temperature distribution during polysilane laser annealing will be shown.

2.3.1 Silicon fabrication using CPS

1. The wafer (commonly silicon oxide on top) was transferred into the glovebox. Before the blade coating, the surface of the wafer was cleaned using the nitrogen gun in the glovebox to remove some particles.

2. The wafer was baked at 80°C on hotplate. A polymide blade was used to spread the CPS after dropping 15uL of CPS on the surface. Blading several times to make sure the liquid is uniformly spread and thinner. During this process, a small amount of CPS was evaporated. (figure 2.4 a)

3. The wafer was placed under the UV lamp to conduct photo-polymerization between 30 to 45 minutes. During this step, the CPS film started to solidify and some of the hydrogen came out. (figure 2.4 b)

4. The wafer was cooled down to room temperature and transferred out of the glovebox.

5. The wafer was placed under laser. The polysilane was crystallized with 300J/cm². (figure 2.4 c)
2.3.2 Measurements

Optical measurements are taken place using Lambda 950 (PerkinElmer Corporation). It is a spectrophotometer which can be used to measure transmittance and reflectance. Because in this measurement the material and the carrier substrate are measured together, the transmittance and reflectance are considered as a result of the whole stack system. To extract the absorption behaviour of the material, the substrate needs to be transparent even in short wavelength. In this thesis, quartz wafers are used as carrier substrate because it can be considered as totally transparent at 300 nm. Absorption is the transformation of radiant power to another type of energy, usually heat, by interaction with matter. When the transmittance and reflectance of a system have been known, the absorption can be calculated as:

\[ A = 1 - T - R \]

(1). CPS absorption

CPS was sealed between quartz samples and the edges of this system are sealed with tapes to prevent the oxygen. Figure 2.5 shows that the transmittance drops quickly from 365 nm. This means CPS can only interact with light of which wavelength is shorter than 365 nm.
(2). Polysilane absorption

Two kinds of polysilane were prepared on quartz wafer. The sample 1 was polymerized by UV AHAND 250GS and the sample 2 (figure 2.6 a) was polymerized by LED Flood Array 375nm for 45 minutes (figure 2.6 b). The major difference between these UV is their power density in which Flood UV is 15 times larger than UV AHAND since their spectral distributions are similar. The oxidation rate of polysilane is relatively slow especially for the one that is intensively polymerized. After UV, both sample 1 and 2 turned into light yellow while sample 2 is darker than sample 1. Figure 2.7 (a) and figure 2.7 (b) show the absorption behaviour of these without oxidation.

Figure 2.6: CPS TRANSMITTANCE BETWEEN QUARTZ

Figure 2.7: (a) CPS polymerized by UV AHAND 250GS, (b) CPS polymerized by LED Flood Array 375 nm
Figure 2.8: Transmittance, reflectance and absorption of CPS polymerized by (a) UV AHAND 250GS, (b) LED Flood Array 375nm.

Figure 2.9: After 2 hours exposure to the open air, the transmittance, reflectance and absorption of CPS polymerized by (a) UV AHAND 250GS, (b) LED Flood Array 375nm

The absorption behaviours of the polysilanes are quite different. Sample 2 started to absorb a wider range of light and the reflectance is much bigger. This means it behaves more like silicon. After 2 hours exposed in the open air, sample 1 (figure 2.8 a) absorbed less light while sample 2 (figure 2.8 b) stayed almost the same. This means sample 1 was being oxidized. As a result, when CPS is intensively polymerized, it is highly dehydrogenated and annealed to the level close to silicon. This is because when the UV could provide sufficient energy, it will not only cleave the Si-Si bond (53kcal/mol) but also the Si-H bond (76kcal/mol). As the energy increases, the bond breakings increase and the content of hydrogen would decrease until it reaches a certain point.

(3). Thermal simulation of polysilane under laser

Heat transfer in polysilane describes the heat distribution in the film. To study the heat transfer of polysilane during laser annealing, the major heat transfer model is the thermal energy provided by the
excimer laser. In this simulation, two assumptions were made: (1) The thermal properties of polysilane are constant; (2) heat convection and radiation are neglected. The kinetic energy induced in polysilane was provided by excimer laser which is highly dependent on the radiative absorption of polysilane. The wavelength of the XeCl laser is specified as 308 nm. Thus, the optical properties of polysilane in 308 nm are essential for the simulation.

According to the formula:

\[ T = T_0 e^{-\alpha t} \]

“t” is the thickness of the object. “\( \alpha \)“ is the absorption coefficient in certain wavelength. “\( T \)” represents the percentage of light pass through the object. “\( T_0 \)” is the original percentage of light on the object which can also be described as:

\[ T_0 = 1 - R \]

In which R is the percentage of light reflected by the surface. In order to calculate the absorption coefficient, T, R and t are required, respectively. The measurement in previous section, in which almost all the light was absorbed around 308 nm, results in a very small T. The inaccuracy and noise will significantly change the ratio of T and T_0. Thus, a thinner layer of polysilane (around 135 nm measured with Dektak) between quartz was produced with UV AHAND and the optical result is shown in figure 2.9. The parameters were extracted as: T = 27.2%, R = 14.3%, t = 135 nm. Then \( \alpha \) can be calculated as 8.6 x 10^6 /m. Although the reflection happens on the quartz surface, it will not influence the study of absorption coefficient. This is because R will not change the ratio between T and T_0 once the material and its thickness is fixed. The R is extracted from the measurement in previous section, which is 6.7%.

![Figure 2.10: Polysilane absorption (135 nm)](image-url)
In this thesis, Multiphysics 4.4 is used for simulation. According to the COMSOL simulator, the properties of polysilane, including heat capacity, density and thermal conductivity are required. Due to the complex and uncertain structure of polysilane, the thermal properties of polysilane remains unknown in the research so far. Plus, its high reactivity to oxygen and water makes the measurement complicated. If it is not reactive, it can be measured with transient plane source method which utilizes a plane sensor and a special mathematical model. By placing the sensor in-between the samples, the thermal conductivity can be measured. In this thesis, the thermal properties were assumed for those of hydrogenated silicon [69].

The used physical constants of polysilane are:

<table>
<thead>
<tr>
<th>Constant</th>
<th>Suffix</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Heat capacity</td>
<td>Cp</td>
<td>833 J/kg·K</td>
</tr>
<tr>
<td>Density</td>
<td>rho</td>
<td>1990 kg/m³</td>
</tr>
<tr>
<td>Thermal conductivity</td>
<td>k</td>
<td>10 W/m·K</td>
</tr>
<tr>
<td>Absorption Coefficient</td>
<td>α</td>
<td>8.6 x 10⁶ /m</td>
</tr>
<tr>
<td>Reflection</td>
<td>R</td>
<td>6.7%</td>
</tr>
<tr>
<td>Thickness</td>
<td>t</td>
<td>200 nm</td>
</tr>
</tbody>
</table>

The simulated heat transfer graph is shown in figure 2.10. It represents the temperature changing during the laser annealing with a pulse of the top surface (green), in the middle (red) and at the bottom (blue) of polysilane layer. The laser energy is 50mJ/cm². The initial temperature is set to 20 °C and the environment is set to 0 °C. According to the simulation results, the temperature in polysilane largely varies depending on the depths. The temperature on the surface can be as high as 230 °C while at the bottom the temperature only increases 40 °C. This is because of the high absorption coefficient of polysilane at 308nm. In this case, the absorbed laser energy drops exponentially through the layer. Figure 2.11 shows the pulse energy intensity through time. The intensity reaches its peak at 20nm where the temperature of the layer becomes the highest. However, this simulation is not accurate especially for higher energy because in practice the changing is much complex. Because of the complex structure of polymerized CPS, the thermal properties of polysilane are not certain. During the pulse, the thermal properties of polysilane are dynamic due to the loss of hydrogen. Also, the hydrogen will take some of the kinetic energy with it which is not negligible. Plus, if the energy is high enough, some of the energy is absorbed by the sample as latent energy during phase changing. Above all, the simulation will show a higher temperature than in practice especially when the energy is high. In practical, 50mJ/cm² is not high enough for phase changing. As a result, it is relatively precise.
Figure 2.11: Temperature (K) changes of the polysilne on the surface (green), in the middle (red) and at the bottom (blue) during laser annealing under 50mJ/cm² energy.

Figure 2.12: Pulse energy vs. time.
2.4 Conclusion

In this chapter, a more stable polysilane was presented using higher UV irradiation. The optical measurements of liquid silicon and polysilane were performed. For liquid silicon, it only absorbs the light in short wavelength. After polymerization, the absorption range extended to light with longer wavelength. With higher UV energy, the absorption behaviour of polysilen is more similar to silicon, also this kind of polysilane is harder to be oxidized when exposed to the open air, which indicates that higher UV energy extensively polymerized the CPS and turned it closer to silicon. The thermal transfer simulation of polysilane under laser was carried out resulting in that for a thin polysilane film. The laser has a much bigger effect on the top than that of the bottom. Consequently, the laser is able to anneal polysilane on the substrate with low thermal budget.
Chapter 3
Transfer and printing of graphene

3.1 Introduction to graphene

Graphene is a promising candidate for printed electronics. In order to fabricate printed Schottky diode, graphene with quality is required. Typically, researchers use transferred CVD graphene for device fabrication because its quality and large available area where poly(methyl methacrylate) (PMMA) is applied as transfer media [43][44]. However, PMMA cannot be removed easily. As a result, it inevitably leaves residuals which greatly influence the electrical properties of graphene. In this work, a cleaner way of graphene transfer will be introduced using photoresist as the transfer media. In this way, only very little amount of residuals will remain after the transfer without harming the structure of the graphene. Another popular way of quality graphene fabrication with large area can be performed using reduced graphene oxide (GO) [41]. GO, commonly mixed with a kind of solution, can be used to print on target substrate. With subsequent GO reduction, graphene layer is achieved. In this way, the graphene deposition is compatible with printing process which will simplify the device production. In this work, this printed graphene production will be introduced using photonic curing system for reduction. In this way, the throughput is largely enhanced.

In this chapter, the typical graphene fabrication will be introduced. A new way of graphene transfer will be presented using photoresist and Gel-pak. The reduced graphene oxide cured by a photonic system will be presented as a printed graphene. In addition, the characterizations of both graphene will be made and compared using Raman.

3.2 Graphene fabrication

10 years ago, atomic plane graphene did not even exist in physical theory due to thermodynamic instability at nanometre scale until 2004. During its fast development in recent years, it has ignited great interest to the industrial world to manufacture new types of devices [35]. Graphene is a two dimensional honeycomb-latticed material formed by carbon atoms. It can be stacked to form 3D graphite, rolled to form 1D nanotubes and wrapped to form 0D fullerenes [33]. It has been arousing great interest in theoretical research and practical studies such as microelectronics in recent years due to its promising properties: the electronic mobility can reach above 15,000 cm$^2$·V$^{-1}$·s$^{-1}$ with theoretically potential of 200,000 cm$^2$·V$^{-1}$·s$^{-1}$; the tensile strength is 130,000,000,000 Pascals which is much higher compared to 400,000,000 for A36 structural steel or 375,700,000 for Aramid; thermal conductivity is 5000W/m·K compared to 400 for copper.
In order to produce graphene some methods have been discovered. The very first method to implement fine graphene samples was mechanical exfoliation. However, it has its limitations such as low productivity and efficiency. That is because in order to exfoliate a single sheet, the van der Waals attraction between the first and second layer must be overcome without disturbing any subsequent sheets [33]. There are also alternative ways to this approach such as chemical efforts to exfoliate, bottom-up methods to grow graphene directly from organic precursors and catalyse growth on a substrate.

The major optimization for graphene fabrication is to efficiently manufacture large-scale, high quality and stable graphene films. In this section, methods of graphene fabrication, including mechanical exfoliation, chemical exfoliation and chemical vapour deposition will be introduced through time and its improvements.

3.2.1 Mechanical exfoliation

In 2004, Konstantin Novoselov and Andre Geim found a surprisingly easy way to produce the first graphene in history [34]. This very interesting work was taken place with scotch tape, which is used to separate graphene sheets from graphite flakes (figure 3.1(a)). By repeating a “stick and peel” process, monolayer graphene had been achieved following by gently pressing the tape on a target substrate.

Another interesting approach is micromechanical cleavage by applying an ultra-sharp diamond wedge with ultrasonic oscillation to highly ordered pyrolytic graphite (HOPG) [34]. In this way, few layers of graphene can be produced (figure 4.1 (b)). However, the size of graphene flakes in these methods are limited to few hundreds of micrometre size which is good enough for physical study and experimental devices, but not enough for industrial usage, which requires wafer-scale graphene synthesis and great electrical properties.
3.2.2 Chemical exfoliation

Chemical exfoliation is originally defined by inserting reactants between graphite layers in order to break the van der Walls forces between atoms. It is also required to prevent the recombining reactions between layers. In this way, solvents like N-Methyl-2-pyrrolidone (NMP) are effective during sonication of graphite in bath. This kind of solution is then centrifuged in order to obtain graphene flakes. Graphene solutions are commonly used as ink-jet printing, coating and electrophoresis deposition which is different from a dry process.

Another way of chemical exfoliation can be performed with graphite oxide which consists of graphene oxide sheets. The oxygen functionalities enable the graphene oxide layers of graphite oxide hydrophilic and water molecules can readily intercalate into the interlayers. Thus, very thin layers can be achieved with this method because the size of fabricated graphene corresponds to the size of graphene oxide. Followed by reduction, these exfoliated layers will produce graphene films. Figure 3.2 illustrate the relations between the graphite, graphite oxide, graphene oxide and graphene. However, the electrical properties are somehow compromised in this way because this kind of film is not necessary continuous. Thus it is only good for applications that do not need a high crystal quality such as being a strong and light material.

![Diagram of graphite, graphite oxide, graphene oxide and graphene](image)

Figure 3.14: Relations between graphite, graphite oxide, graphene oxide and graphene (Source: IDTechEx). Red arrows show the order of this process.

3.2.3 Chemical vapour deposition (CVD)

Among all the strategies to produce graphene, CVD has become one of the most popular and important techniques for graphene synthesis. Graphene CVD is not only easy to setup but also enables the continuous wafer-scale graphene films with high quality. It has shown great potential in industrial world. The most common equipment for CVD graphene synthesis is Aixtron BM Pro System (figure 3.2). This machine provides high performance heaters with ramp rates up to 300°C/minute, top side
wafer control, pulsed plasma and automatic process recipes. So it is very commonly used in research for not only graphene but also for carbon nanotubes.

In this method, graphene is fabricated by a combination of gas molecules in the reaction chamber. The principle of CVD graphene growth includes reactions in two steps: the pyrolysis to form disassociated carbon atoms and the formation of the carbon structure of graphene. Taking multilayer graphene growth with Ni as an example, the polycrystalline Ni films are first annealed in Ar/H₂ atmosphere at 900 - 1000°C to increase grain size and then exposed to H₂/CH₄ gas mixture. In this step, CH₄ decomposes and carbon atoms dissolve into Ni film. During the following cooling down process in Ar gas, carbon atoms diffuse out from Ni, whose solubility decreases as temperature goes down, and precipitate on the Ni surface to form graphene [35]. If the metal has low carbon solubility in the case of Cu, the sp²-formation directly happens at the surface. The parameters of the process depend on the type of catalytic metal, pressure, temperature, time of gas exposure and its concentration, heating and cooling rates. This method has some inherent drawbacks. Due to the mysterious relationship between graphene and metal catalyst, it is not easy to separate them without damaging the structure of graphene, or influencing the properties of graphene during transfer process. Another problem is that a completely uniform layer of graphene is hard to achieve in this method because the kinetic transport dynamics of gas is affected by diffusion and convection and these values change within the space of a reaction chamber which affects the reactions on the substrate.

In the first experimental works, graphene on the surface was composed by islands with different orientations. It is somehow solved with optimization in both graphene fabrication and graphene transfer in the next sections. In this thesis, multilayer graphene is fabricated and transferred.
3.2.4 CVD Graphene growth

A 100 nm thermal silicon oxide layer is deposited on silicon wafer (100). Then a 300 nm layer of PVD Ni is deposited using Solution of CHA Industries with 99.95% pure Ni target. This wafer is brought into Aixtron BM Pro system at 25 mbar and annealed at 910 °C in Ar (250sccm) and H₂ (1000sccm) environment for 120s in order to increase the grain size of Ni. Then 25sccm of methane (CH₄) is fed into the chamber to deposit graphene for 150 sec. After that, the wafer is cooled down to 400 °C with two different rates: 50°C/min and 200°C/min. An optical microscopic image is shown in figure 3.4(a). Also, A Raman spectroscopy (Renishaw inVia, 514nm laser) measurement is presented in figure 3.4(b). The noises are due to the Ni underneath. The G peak (1580 cm⁻¹) is higher than 2D peak (2690 cm⁻¹) which indicates that it is a multi-layer graphene. There is no evident D peak (1350 cm⁻¹) which means the structural defects are small.

![Image](image.png)

Figure 3.16: (a) Graphene on Ni observed with x20 lens under microscope, (b) Raman measurement of graphene on Ni.

3.3 Graphene transfer

3.3.1 Theory

After CVD fabrication of graphene, it is necessary to transfer graphene from growth substrate to target substrate without damaging the honeycomb structure of graphene or the target substrate. In general, there are two methods that can be used to satisfy this requirement: either carrier method or stamp method, for both of them a transportation carrier to preserve the structure intact of graphene is used.

In the carrier method, a thick organic film is typically required such as poly(methyl methacrylate) (PMMA) and polycarbonate (PC). Then the growth substrate is etched away with an inorganic acid so that the graphene/carrier stack is left. The resulting stack is then placed on top of the target substrate. Finally, the carrier film is removed by chemical or thermal treatment. It is essential for these films to
be relatively easy to remove without damaging the graphene. It also requires certain mechanical strength and good adhesion with graphene to ensure the quality of graphene to be identical to the way it was before the transfer.

In the stamp method, an elastic and adhesive film like PDMS (polydimethylsiloxane) is required to be attached to the graphene sheet on the growth substrate. Then the substrate is etched away with graphene/stamp stack left. The stack is then placed on top of the target substrate. Finally, the stamp is removed by mechanical detachment like slow peeling off (figure 3.5).

Figure 3.17: Transfer methods of graphene [31]

In both methods, the transfer polymer film works as a mechanical support for the graphene which should guarantee a gentle and defect-free release. For the carrier method, the transfer polymer layer itself can leave residuals after removal. In addition, due to the usage of aggressive chemicals for residuals removal, an extensive cleaning treatment is necessary. These steps will inevitably cause damage to the graphene sheet. For the stamp method, the adhesion between graphene and the target substrate has to be stronger than the adhesion between graphene and the stamp which means that the choice of substrate type is limited. In this way, the substrate must be flat and hydrophilic [31].

The technique developed by Chua [31] and his colleagues presents a modified stamp method in which a second polymer layer is applied between graphene and stamp (figure 3.5). In this way, the stamp works as mechanical support and the polymer layer works as transfer contact with graphene. This method makes the stamp and carrier complement each other well. To be specific, the polymer layer doesn’t necessarily need mechanical strength to support graphene because the stamp will sustain its
structure; the stamp doesn’t contact to graphene so that the mechanical stress during peeling off will be decreased dramatically.

In this paper, photoresist is applied as the carrier mentioned due to its good adhesion with graphene and can be removed with mild organic solution which will not likely damage the graphene sheet. Instead of PDMS, the elastic material in Gel-Box (Gel-Pak Corporation) is used as stamp because this material is commercially available, and more importantly, the gel is more adhesive than PDMS which prevents the detachment between photoresist and gel in the etching process[42]. And the adhesive force is not big enough to significantly impact the quality of the graphene film during the peeling-off process.

![Figure 3.18](image)

Figure 3.18: (a) Gel-Box as graphene transfer support, (b) Photoresist (after baking) on graphene samples, (c) Samples stacks are placed on the gel, (d) The gel is cut into pieces.

Graphene transfer in this paper can be simply described into few steps: photoresist deposition, sample cutting, nickel etching, sample cleaning and graphene transfer which will be further described in the following sections.

### 3.3.2 Experimental

**(a) Photoresist deposition**

A multilayer graphene on nickel substrate is prepared and stored in a clean room box before the process. The nickel layer is deposited on thermal silicon oxide layer on silicon wafer. Photoresist is
spin-coated with 500rpm for 10s and 1500rpm for 60s. In this way, photoresist will be smoothly spread out in the first 10s, and the latter 60s is to control the thickness of photoresist which is around 100nm and make it flatter. Then the wafer is put on a hotplate at 150°C for 60s to cure the photoresist. The photoresist is hard baked (figure 3.6 (b)).

![Figure 3.19: Nickel etching](image)

(b) Nickel etching

The wafer is then cut into pieces of around 1cm*1cm (figure 3.6c). After the baking process, samples form a stack of photoresist, graphene, nickel, thermal silicon oxide and silicon wafer (figure 3.8(a)). Next, the elastic material in the Gel-Box [42], which is referred to as gel in the in this work, is cut into slightly bigger pieces than the graphene samples. The gel is placed onto graphene samples (figure 3.6(c)) with proper pressure to make sure that gel and photoresist have a good contact. Air bubbles need to be avoided. It is important to choose the etchant carefully to prevent violent reaction by strong acid like nitric acid, because the hydrogen bubbles produced by nitric acid will cause irreversible damage to graphene. However, the acid should be strong enough to prevent unnecessary time consumption. In this work, 20% aqueous ferric chloride (FeCl₃) is used to etch the nickel layer (figure 3.7). This etchant will slowly but effectively etch the nickel layers with a mild pH. More importantly, it will not produce gas. The chemical reaction is as follows:

\[
2FeCl₃ + Ni \rightarrow NiCl₂ + FeCl₂
\]

The etching starts from the side of these samples and goes further into the centre until the nickel layers are completely removed (figure 3.8(d)). This process will approximately take 10 hours. After etching, a gel, photoresist and graphene stack is obtained floating on the etchant (figure 3.8(c)). And, the silicon oxide and silicon substrates sink to the bottom of the etchant. The reason why a gel needs to be of a larger area than the graphene sample is to decrease the etching time. It can be noticed that the
density of the gel is smaller than the solution, while the density of the substrate is bigger than the solution. During the etching, the gel tends to pull-up the sample and the substrate tends to pull down. In this way, the etchant solution will more easily reach the nickel layer which is between these two parts. Next, the gel with photoresist and graphene stack is cleaned with 10% hydrochloride to remove iron or iron compound contaminations. Then the samples are rinsed together in water to remove all the acid residues. The samples then are put on tissues with the graphene layer exposed in the open-air to get rid of water at room temperature for 2 hours. Now, the graphene is successfully transferred from the original substrate to photoresist with the gel. (Figure 3.8(c)).

Figure 3.20: (a) Graphene transfer preparation, (b) Ni etching from side in acid solution, (c) Graphene on photoresist and gel after etching, (d) Graphene sample placing on target substrate, (e) Baking the sample at 1500°C, (f) Remove the gel and photoresist
(c) Graphene transfer

A silicon oxide wafer is presented as graphene transfer target. The graphene stack is placed on a silicon oxide wafer with the graphene layer facing down. This whole system is then baked on a hotplate at 150 °C for 10 minutes with some pressure on the gel (Figure 3.8 (e)). The pressure needs to be slow and soft to prevent damage to graphene structure. The hot plate increases the adhesion between graphene and target substrate, in the meanwhile, decreases the adhesion between photoresist and gel. After 10 minutes, the gel can be slowly peeled off leaving the photoresist and graphene on the target substrate. The photoresist can be easily removed by acetone or mild organic solutions like isopropanol or acetone (Figure 3.8(f)). The transferred graphene on SiO$_2$ is shown in figure 3.9(a) and (b). Only few cracks can be observed in this way and the film is quite continuous. A comparison experiment is taken place in the meanwhile using PMMA transfer method. PMMA is spin coated in 1500rpm and cured 180°C for 1 minute. After etching, cleaning and transfer step mentioned, the results are shown in figure 3.9 (c) and (d). These non-uniform colour changes indicate PMMA leaves many residues on graphene with different thickness.

![Figure 3.21](image)

Figure 3.21: (a) Transferred graphene(photoresist method) on SiO$_2$ observed with x20 lens under microscope, (b) Transferred graphene (photoresist method) on SiO$_2$ observed with x5 lens under microscope, (c) Transferred graphene(PMMA method) on SiO$_2$ observed with x20 lens under microscope, (d) Transferred graphene (PMMA method) on SiO$_2$ observed with x5 lens under microscope.
A Raman spectroscopy measurement is also taken for transferred graphene using photoresist (figure 3.10). G peak is twice bigger than 2D peak indicating this is a multilayer graphene. D peak shows there is imperfection in this graphene. And the peak around 1000/cm$^{-1}$ is the overtone of silicon substrate. The resistance of transferred graphene is around 10k$\Omega$ measured by a multimeter.

![Raman measurement for graphene on SiO2](image)

**Figure 3.22: Raman measurement for graphene on SiO2**

### 3.4 Printing graphene from graphene oxide

#### 3.4.1 Graphene oxide introduction

Graphene oxide (GO) is a two dimensional material derived from graphite oxide (graphene oxide bulk) which is a compound of carbon, oxygen and hydrogen in variable ratios. It was first prepared by Oxford chemist Benjamin C Brodie in 1859 and developed by Hummers and Offeman in 1957 [38][39]. Recently graphene oxide has drawn intensive research interests because its role of being a precursor of graphene by reduction.

Graphite oxide has a similar layered structure to graphite but the plane of carbon atoms in graphite oxide is heavily decorated by oxygen-containing groups, including carbonyl (C=O), hydroxyl (-OH), epoxy (C-O-C) and carboxyl (COOH) groups (figure 3.11). These functional groups not only expand the interlayer but also make the atomic-thick layers hydrophilic[37]. Thus, these layers can be exfoliated in water under moderate ultra-sonication resulting in thin films of graphene oxide. These films can be partially reduced by removing the oxygen containing groups through chemical, sonolytic, microwave, photo thermal, photo catalytic and electrochemical methods [41].
3.4.2 Graphene oxide reduction

Graphene oxide can be solely reduced by heat treatment which is called thermal annealing reduction. Rapid heating (>2000°C/min) was usually used to exfoliate graphite oxide to achieve graphene due to the sudden expansion of CO or CO² gases evolved into the spaces between sheets during the rapid heat [37]. The rapid temperature increase also makes the oxygen-containing functional groups attached to carbon atoms decompose into gases, resulting in graphene sheets. In this work, photo-reduction was carried out using PulseForge 1300 photonic curing system (Novacentric Corporation). The PulseForge uses novel flashlamp and power supply technologies to deliver continuously adjustable, megawatt-intensity, microsecond-resolution pulses of broad-spectrum light to thermally process thin films (figure 3.12). In this way, the heat is only induced on the surface of the film with little thermal effect on the substrate.
3.4.3 Experimental

Graphite oxide powder was mixed with water in the density of 5mg/mL. After 10 minutes ultrasonication, graphene oxide solution was obtained. A droplet of GO solution was dropped on the surface of a silicon wafer. A hotplate was used to heat up the wafer in 70°C to get rid of the water. It is not desirable to use higher temperature in case the quick evaporation of water would damage the structure of graphene oxide. Then the sample was placed under the PulseForge and ready for the photonic curing. The voltage was set to 660V and the pulse duration was set to 5us resulting in 380°C on the surface as simulated using its simulator. The resistance of the reduced GO was measured using a multimeter which is around $1500\Omega$. The reduced GO was characterized using Raman (figure 3.13).

![Raman measurement for reduced GO on silicon](image)

The G peak is twice higher than 2D peak. This indicates this is a multilayer graphene. The big D peak suggests that there are more nanocrystalline structure and the presence of graphene edges and defects. Compared to transferred CVD graphene, the conductivity of reduced graphene oxide is better. This is because the reduced graphene oxide layer is thicker than CVD graphene. However, the defects of reduced graphene oxide are also worse than that of transferred graphene. This is because during the graphene oxide reduction, these oxygen-containing groups detach from carbon atoms leading to the vacancy and non-uniformity of graphene structure.
3.5 Conclusion

The graphene fabrication methods are introduced. And a cleaner way of CVD graphene transfer process is performed using photoresist and Gel-pak. The reduced GO was introduced and produced using a photonic curing system. The transferred graphene and reduced GO are characterized with Raman. In this method, for transferred CVD graphene, although some defects can be induced on graphene, it is good enough to start applying this graphene to devices. For thermally reduced graphene oxide, the defects are much bigger than transferred CVD graphene, and however, the conductivity is much better.
Chapter 4
Graphene and silicon Schottky diode

4.1 Introduction

Both transferred graphene as well as reduced graphene oxide mentioned in the previous chapter has minor thermal effect on the substrates, the process provides us a potential to fabricate devices on a substrate with a low thermal budget such as paper or plastic. This will also dramatically simplify the fabrication procedure compared to conventional devices because of printing.

In this chapter, the basic principle of the Schottky diode and why graphene can be used to form Schottky junction with silicon will be explained. A Schottky diode made from graphene (anode) and silicon (cathode) will be presented using transferred CVD synthesized graphene and reduced graphene oxide. This Schottky diode will be fabricated on an n-type silicon wafer. Schottky junction will be formed at the interface between graphene and n-type silicon. Ti is used as electrodes. The diode will be characterized using dc current – voltage (I-V) measurement. Characteristic of the interface between silicon and graphene will be extracted from the result in order to characterize the two kinds of graphene.

4.2 Schottky diode

4.2.1 Principle

A Schottky junction is typically formed at the interface of a metal and an n-doped semiconductor, enabling the electron transfer from semiconductor to metal resulting from an equal Fermi level. This state corresponds to thermal equilibrium in which no net current flows. This diffusion leaves positively charged donor atoms on the semiconductor side of the junction, resulting in an upward shift in both the conduction band and valence band of the semiconductor near the junction (figure 4.1a,b).
The parameter $\phi_{BO}$ is the ideal barrier height of the semiconductor contact, the potential barrier seen by electrons in the metal trying to move into the semiconductor. This barrier is known as Schottky barrier given by

$$\phi_{BO} = \phi_m - \chi,$$  \hspace{1cm} (1)

where $\phi_m$ is the metal work function, $\chi$ is the electron affinity of the semiconductor.

On the semiconductor side, $V_{bi}$ is the built-in potential barrier which is seen by electrons in the conduction band trying to move into the metal.

In the thermal equilibrium, more energy is needed for electrons to pass through the barrier because the positive charges tend to hold them. When the semiconductor is positively biased (reverse bias), the Fermi energy of semiconductor along with the conduction and valence bands will decrease, resulting
in the energy needed for electrons to flow into metal increasing (figure 3.1c), where \( V_R \) is the reverse bias voltage. This means that current does not pass from semiconductor to the metal. When the semiconductor is negatively biased (forward bias), the Fermi energy of the semiconductor along with the conduction and valence bands will increase, leading to the energy needed for electrons to flow into semiconductor decreasing (figure 3.1d), where \( V_a \) is the forward bias voltage. This means the current can easily pass from the metal to the semiconductor. This one-direction current flow device is named as Schottky diode.

Since the electron transport process of Schottky barriers is mainly dominated by thermionic emission, this process can be described by thermionic emission theory and the equation is given as:

\[
I = I_s \left[ \exp \left( \frac{qV}{\eta k_b T} \right) - 1 \right],
\]

(2)

where

\[
I_s = A A^* T^2 \exp \left( \frac{-q \phi_b}{k_b T} \right)
\]

(3)
is the reverse saturation current, \( q \phi_b \) is the Schottky barrier height, \( A \) is the contact area, \( A^* \) is the Richardson constant, \( T \) is the absolute temperature in Kelvin, and \( V \) is the applied voltage across the junction. When the forward bias greater than \( \frac{3 k_b T}{V} \), the equation can be simplified as

\[
I = I_s \exp \left( \frac{qV}{\eta k_b T} \right).
\]

(4)

\( I_s \) can be extracted by fitting the linear section of the semi-logarithmic plot and extending the fit to zero voltage. Once \( I_s \) is known, \( \phi_b \) can be extracted with the equation (4).

Also, the ideality factor \( \eta \) can be calculated.

When the forward voltage becomes even higher, the effect of series resistance is no longer negligible. Therefore, the equation becomes

\[
I = I_s \exp \left( \frac{q(V-I R_s)}{\eta k_b T} \right).
\]

(5)

The voltage across the Schottky barrier is equal to an applied voltage minus any voltage drop across the series resistance \( R_s \), that is \( V - IR_s \). \( R_s \) can also be extracted once \( I_s \) and \( \eta \) are known.

### 4.2.2 Interface investigation

For the fabrication of the silicon/graphene Schottky diode, metal electrodes are required for silicon and graphene to be able to have Ohmic contact. Thus, the diode consists of three interfaces between
different materials as graphene/silicon, graphene/metal and metal/silicon. In order to guarantee the rectification behaviour to be solely performed by the graphene/silicon interface, it is essential to form Ohmic contact with low resistance between graphene/metal and metal/silicon interface. Thus, investigations of these interfaces are important. Figure 4.2 shows the band diagram before the contacts in which $\phi_m$, $\phi_s$ and $\phi_G$ are the work function of metal, semiconductor and graphene, respectively.

The contact resistance ($R_c$) between graphene and metal limits the performance of the device. It has been reported that for carbon based devices, metals with good wettability, such as Ti, Cr and Fe show no difference in contact resistance regardless of their work function difference. However, as the wettability becomes worse, the contact resistance more strongly tracks the work function difference between carbon and the used metal [50]. Recent studies that investigate metal contacts to graphene demonstrate specific contact resistance in the order of $5 \times 10^{-6} \Omega \text{ cm}^2$ for Ti/Pt/Au contacts to graphene [51]. Furthermore, the lowest contact resistance was achieved as small as 700±500Ω for the Ti contact [52]. In this work, Ti is chosen as metal electrode to graphene not only because of its wettability but also because of its excellent adhesive capability on SiO$_2$ substrate or other insulators [53].

In order to form an Ohmic contact between silicon and metal, the most widely used technique is to highly dope the Si surface, in which the contact resistance does not depend strongly on the chosen metal (figure 4.3a). However, an Ohmic contact can also be achieved by lowering the barrier height at the metal/Si interface with relatively low doping concentration (figure 4.3b). According to Zhu et al, Ti ($\phi_m$=4.33V) and n-type silicon ($10^{15} \text{ cm}^{-3}$) contact shows linear current-voltage behaviour at room temperature without any barrier height tuning, it only begins to show sign of rectification at temperature lower than 244K [54]. Consequently, Ti can also be used as electrode for relatively low silicon doping levels. In this way, the fabrication of Schottky diode is greatly simplified by using Ti as the metal electrode and no additional extra doping for silicon.
Schottky barrier formation on various n-doped semiconductors silicon (Si), gallium arsenide (GaAs) or 4H-silicon carbide (4H-SiC), has been demonstrated using highly oriented pyrolytic graphite (HOPG) which is a semi-metal as ‘metal’ electrode. Being semi-metal means graphite has both electrons and holes as carriers in which the concentrations are lower than metals but higher than semiconductors. Consequently, the conduction band and valence band of graphite overlap leading to a partially metallic and partially semiconductor electrical property. Graphene is also expected to exhibit similar behaviour since the Schottky barrier characteristics are mainly governed by the first layer of graphite according to bond polarization theory [56]. Recent studies have confirmed this and successfully made heterojunction devices with a graphene family material [13-17]. Investigations of graphene’s work function approximated $\phi_{\text{graph}}$ to be 4.8eV [62]. Thus, Schottky barrier can be ensured between graphene and silicon. Graphene represents many advantages compared to traditional metals. Due to the strong bonding energy between carbon atoms, graphene should not diffuse into the semiconductor easily therefore the interface remains Schottky behaviour. Also, the work function of graphene can be tuned by employing an external electric field, reaction with organic and inorganic molecules, chemical modification of the surface, metal doping, substrate orientation, and a self-assembled monolayer formation [63]. This makes a wider usage of graphene/semiconductor Schottky diode based on controllable barrier height.

4.2.3 Schottky diode design

For the I-V measurements using the probe station, proper contact between sample and probe is necessary. Therefore, metal electrodes are needed for both graphene and silicon. As discussed in the previous section, Ti electrodes will be used. Considering the contamination purpose we have chosen to place the graphene in the last process step. The schematic of the graphene Schottky diode is shown in figure 4.4. One end of the graphene lies on the n-type silicon surface without touching the metal electrode on the silicon, the other end lies on the Ti pad on top of the SiO$_2$ insulator layer which prevents a direct contact between the metal electrode and the silicon substrate. In this schematic,
Ohmic contact is achieved by two interfaces: Ti/graphene and Ti/silicon. And a Schottky junction is achieved between graphene and n-type silicon. Because of manual graphene deposition, the structure is relatively big (2cm²). The series resistance is mainly caused by the bulk resistance of the substrate combined with the resistance of graphene.

![Figure 4.29: schematic of the graphene Schottky diode](image)

### 4.3 Experimental

#### 4.3.1 Production process

An n-type silicon wafer with dopant (phosphorus) concentration of 10¹⁶ cm⁻³ was used as substrate with <100> orientation. A 300nm TEOS based silicon dioxide layer was deposited by Novellus PECVD. Photoresist was coated and exposed by ASM PAS 5500/80 wafer stepper. And part of the SiO₂ layer was removed using Drvtek Triode 384T plasma etcher. A 500nm Ti layer was deposited on the wafer by sputter coater at 50°C. Again photoresist was coated and exposed. The Ti was etched using 0.5% HF for 5 minutes in order to expose the silicon area and cut off the contact between graphene electrode and silicon. This etching process could be longer to guarantee the total removal of silicon native oxide. At last, the sample was placed in an acetone bath to remove the photoresist for 1 minute at 40°C. For one sample, graphene layer was produced using chemical vapour deposition (CVD) on Ni layer of a wafer as described in detail in chapter 3. The graphene was transferred onto the substrate right after the removal of silicon native oxide in order to form a direct contact between silicon and graphene (figure 4.5 a). For the other sample, a graphene oxide solution was dropped on the pattern structure. Then the sample is baked on hotplate for 20 minutes to remove the water. The sample was cured using flash lamp. For the graphene oxide on silicon area, the flash power was set to 650V, and for the graphene oxide on Ti area, the flash power was set to 330V. Again, this graphene step has to be done right after the removal of silicon native oxide (figure 4.5 b).
Figure 4.30: Silicon based Schottky diode with (a) Transferred CVD graphene, (b) reduced graphene oxide

4.3.2 I-V measurements

I-V measurements were carried out using the probe station (Cascade Microtech Corporation) and semiconductor parameter analyzer (HP 4155A). The metal electrode on the SiO$_2$ layer was positively biased and the metal on the silicon is negatively biased. The measurements were taken under dark conditions. The I-V curves are shown in figure 4.6. For both of the samples, they show rectification behaviour. The current density of CVD transferred graphene Schottky diode is lower than that of RGO. For CVD SBD, the forward bias current begins to saturate at 1.8V and for RGO SBD, the forward bias current begins to saturate at 3V. These saturations are caused by series resistance which mainly consist of bulk resistance of the substrate and the resistance of graphene. These results indicate that the resistance of transferred CVD is much larger than that of RGO.
Figure 4.31: I-V characteristics of the graphene/silicon Schottky diode for CVD transferred graphene from -2 ~ 2 V on (a) linear scale, (b) semi-logarithmic scale; and for reduced graphene oxide from -5 ~ 5V on (c) linear scale, (d) semi-logarithmic scale.

4.3.3 Results analysis

$I_s$ can be extracted by fitting the linear section of the semi-logarithmic plot and extending the fit to zero voltage. According to Ivey, the Richardson constant of carbon is about 46 A/cm²K² [64]. The contact area of each sample is around 0.35 cm². Thus, $\phi_b$ can be calculated using

$$I_s = A^* T^2 \exp \left( \frac{-q \phi_b}{k_b T} \right).$$

The ideality factor $\eta$ then is calculated using

$$I = I_s \exp \left( \frac{qV}{\eta k_b T} \right).$$

The series resistance is calculated using

$$I = I_s \exp \left( \frac{q(V - I R_s)}{\eta k_b T} \right).$$

Physical constants and assumed parameters are shown in table 3.

<table>
<thead>
<tr>
<th>Name</th>
<th>Symbol</th>
<th>Value</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Richardson constant</td>
<td>$A^*$</td>
<td>46</td>
<td>A/cm²K²</td>
</tr>
<tr>
<td>Absolute temperature</td>
<td>$T$</td>
<td>300</td>
<td>K</td>
</tr>
<tr>
<td>Contact area</td>
<td>$A$</td>
<td>0.35</td>
<td>cm²</td>
</tr>
<tr>
<td>Electronic charge</td>
<td>$q$</td>
<td>1.602 x 10⁻¹⁹</td>
<td>C</td>
</tr>
<tr>
<td>Boltzmann’s constant</td>
<td>$k_b$</td>
<td>1.38 x 10⁻²³</td>
<td>J/K</td>
</tr>
</tbody>
</table>

The saturation current of transferred CVD graphene can be extracted from the semi-logarithmic I-V curve which is $8 \times 10^{-8}$ A. Once the saturation current is known, the $\phi_b$(CVD) can be calculated as 0.79eV, resulting in the work function of CVD graphene as 4.8eV. Neglecting the effect of series resistance by choosing the point of low voltage, the point (0.3, 6 x 10⁻⁵) is selected and the ideality factor is calculated as $\eta =1.75$. Considering the effect of series resistance by choosing the point of relatively high voltage, the point (0.7, 2 x 10⁻⁴) is selected and the series resistance is calculated as $Rs = 2533 \ \Omega$.

The saturation current of transferred CVD graphene can also be extracted from the semi-logarithmic I-V curve which is $1 \times 10^{-6}$ A. Then $\phi_b$(RGO) can be calculated as 0.72eV which in the work function of RGO is known as 4.73eV. The point (2, 1.2 x 10⁻³) is selected and the ideality factor is calculated as $\eta =8.38$. The point (4, 5 x 10⁻³) is selected and the series resistance is calculated as $Rs = 430 \ \Omega$. 
The work function of graphene can be determined by the type of structural strain in which the tensile strain increases the work function and the compressive strain decreases the work function. It can also be affected by the oxygen-containing group for RGO which increases the work function[65]. During the CVD graphene transfer, the tensile strain was induced by pressing the gel to the photoresist/graphene stack resulting in a work function increasing. For the RGO, it was affected by both ways: the carbon atom loss leads to a compressive strain which decreases the work function and the remaining oxygen-containing functional group increases the work function. As a result, the work function of RGO is smaller than that of CVD graphene.

In this work, the ideality factor is altered by the recombination in the graphene due to the defects of graphene. If the levels of defects are higher, the ideality factor becomes larger. Either transferred CVD graphene or RGO cannot avoid the defects in this work. However, the Raman results indicate that the level of defects of RGO is much higher than CVD graphene due to the initial oxidation of the carbon backbone as well as the thermal shock treatment induced decomposition of oxygen-containing groups [67]. This decomposition also removes carbon atoms resulting in the distortion of graphene structure. Also, the sudden released carbon dioxide induces the structure damage of RGO [68]. As a result, the ideality factor of RGO is much higher than transferred CVD graphene.

The series resistance is mainly contributed by the resistance of graphene itself. According to the previous chapter, the resistance of RGO is much smaller than transferred CVD graphene because of its higher thickness. Thus, the series resistance of RGO SBH is smaller. The series resistance has an impact on the diodes forward bias saturation current which means when forward bias is large enough, the effect of the series resistance dominates the I-V characteristics of SBD. For CVD graphene SBD, the current tends to saturate at 40mA while for RGO SBD, the saturation current is around 60mA. This is because the series resistance of CVD SBD is much larger than that of RGO SBD.

Figure 4.7 shows a band diagram of graphene/silicon SBD with the extracted parameters. The metal and silicon forms a junction with a low barrier height of 0.32eV which can be seen as an Ohmic junction. The graphene which is a zero band gap material can be seen as a metal in this case so it forms a Schottky junction with silicon and an Ohmic contact with Ti, respectively.
4.4 Conclusion

In this chapter, G/n-Si SBDs were fabricated using two kinds of graphene which are transferred CVD graphene and reduced graphene oxide. The barrier heights were extracted from the I-V plots and then work functions of these graphene were calculated which correspond to the value being reported. The characteristics of the diodes were investigated by I-V measurement. For both SBDs, the series resistances are mainly caused by the resistance of graphene. The resistance of CVD graphene (2533 Ω) is much higher than that of RGO graphene (430 Ω) because of the defects caused during transfer process. Also it is because RGO graphene has more layers than CVD graphene which enhance the conductivity. The ideality factor of CVD SBD is 1.75 while that of RGO is much higher (8.38) which could be probably caused by the charges recombination due to the high level of defects in RGO graphene. Both of the graphene can be used for printed Si/graphene SBDs.
Chapter 5
Conclusions

In this thesis, a printed Si/graphene Schottky diode was studied and fabricated. Liquid silicon and graphene are promising materials for printed electronics. In chapter 2, a more stable polysilane was produced using UV irradiation on liquid silicon with higher density (15 times higher than a normal one). The stability of the polysilane was confirmed by optical measurements. After liquid silicon irradiated under UV with 20mW/cm$^2$ (sample 1), the polysilane began to absorb the light at 370nm. After liquid silicon polymerized under UV with 300mW/cm$^2$ (sample 2), the polysilane began to absorb light at 410nm which is closer to the absorption spectrum of silicon. After exposed in the open air for 2 hours, the optical properties of sample 1 changed towards silicon oxide; the optical properties of sample 2 stayed the same. Thus, the photo-polymerization process can be optimized using UV at a higher energy. The heat transfer simulation of polysilane (polymerized with 20 mW/cm$^2$) under laser was conducted using 50mJ/cm$^2$ laser energy. The temperature on the surface was about 230°C and at the bottom was about 40°C. Thus, due to the high absorption coefficient of polysilane at laser wavelength (8.6 x 10$^6$/m), the laser can only heat up a shallow layer of polysilane. In this way, liquid silicon can be printed on arbitrary substrate with low thermal budget. In chapter 3, a cleaner way of CVD graphene transfer was introduced using photoresist and Gel-pak. Compared with PMMA, photoresist was easier to remove with mild organics such as acetone. A reduced graphene oxide (RGO) layer was produced using a photonic curing system. The D peak of transferred CVD graphene is 10% as high as G peak while the D peak of RGO is 50% as high as its G peak. This means the defects level of RGO are higher than CVD graphene. However, the resistance of CVD graphene (10kΩ) is much higher than RGO (1.5kΩ) measured by a multimeter. In chapter 4, Si/graphene Schottky barrier diodes (SBD) were fabricated using CVD graphene and RGO, respectively. Titanium was used as electrodes to form Ohmic contact with n-Si and graphene. The ideality factor of CVD SBD and RGO SBD were 1.75 and 8.38, respectively. The higher ideality factor of RGO SBD was caused by the carrier recombination in defects resulting from carbon atom loss and the sudden release of carbon dioxide. The series resistance of RGO SBD is much lower (430Ω) than CVD SBD (2533Ω). This is because RGO has more layers than CVD graphene. The work function of both graphene are extracted as 4.73eV (RGO) and 4.8eV (CVD).
## Appendix A
### Properties of CPS

<table>
<thead>
<tr>
<th>Name</th>
<th>Cyclopentasilane</th>
</tr>
</thead>
<tbody>
<tr>
<td>Formula</td>
<td>$\text{Si}<em>3\text{H}</em>{10}$</td>
</tr>
<tr>
<td>Molar mass</td>
<td>150.5 g/mol</td>
</tr>
<tr>
<td>Melting point</td>
<td>-10.5°C</td>
</tr>
<tr>
<td>Boiling point</td>
<td>194.3°C</td>
</tr>
<tr>
<td>Density</td>
<td>0.963 g/cm$^3$</td>
</tr>
<tr>
<td>Solubility in water</td>
<td>reacts</td>
</tr>
<tr>
<td>CAS number</td>
<td>289-22-5</td>
</tr>
</tbody>
</table>
Appendix B
Liquid silicon crystallization on CNT

B.1. Introduction

Single crystal silicon and polycrystalline silicon films are widely used in electronic devices. The crystal grain size of these films determines the electronic properties since it is difficult for charge carriers to cross grain boundaries. A bigger grain size is desirable for higher mobility devices. In order to obtain these crystallized materials, the nucleation mechanism from the crystallization of a-Si needs to be analysed.

Liquid silicon, as a precursor of amorphous silicon, enables the possibility of printing Si devices. CNT, as a potential material for vertical 3D interconnects, has attracted much interest in electronic research. Liquid silicon on CNT could be a new path of fabricating 3D integrated circuits (3D ICs) (figure B.1). In this way, these two applications can be combined. The thermal properties could be used for the nucleation for crystallizing silicon. However, there is still lack of research to see if it is possible to apply liquid silicon as a way to print silicon on top of these 3D CNT contacts. In this chapter, liquid silicon on CNT crystallization behaviour will be investigated.

![Figure B.33: Schematic of 3D-ICs cross section using liquid silicon and CNTs](image)

B.2 Carbon nanotubes

Carbon nanotubes (CNTs) are a cylindrical nanostructure material formed by a single-atom thick layer of carbon, which can be seen as a rolled-up graphene sheet (figure 3.2). They are first observed as multi-walled carbon nanotubes (MWCNTs) by Dr. Iijima in 1991 [18]. Two years later, Iijima [19] and Bethune [20] both observed the single-walled carbon nanotubes (SWCNTs). The chemical bonding of carbon nanotubes is composed entirely of sp² bonds, which are stronger than the sp³ bonds found in alkanes and diamond, providing carbon nanotubes’ unique properties such as high electrical conductivity, thermal conductivity and good mechanical strength and flexibility. For instance,
SWCNTs are stable up to 750°C in air and 1500-1800°C in an inert atmosphere [17]. CNTs also have a very high thermal conductivity. The thermal conductivity for an individual SWCNT is more than 6000 W/mK [21] which is much greater than that of diamond (2000 W/mK) and metals like copper (400 W/mK).

![Figure B.34: Schematic of single wall carbon nanotube as a rolled graphene layer [27]](image)

The synthesis methods of CNT growth vary from electric arc-discharge method, laser ablation method to catalytic chemical vapour deposition (CCVD). Among these methods, the CCVD process is the easiest and low cost. More importantly, since the arc-discharge and laser ablation require operation at extreme high temperatures, these methods do not allow direct integration on silicon substrates [22]. The CCVD method is considered to be the most favourable method for mass production.

In this work, only chemical vapour deposition is considered. For this method, substrates with nm-thin catalysts (e.g. Fe, Ni, Co, Pd and Cu) are placed in a tube furnace at temperatures from 500 to 1000°C which will break the catalysts into small particles by minimization of surface energy. A continuous flow of precursor (usually hydrocarbon gas like CH₄, C₂H₂, C₂H₄ or C₆H₆) mixed with H₂ or an inert gas like Ar and N₂ is introduced over a period of time. During this time, the catalyst will absorb the precursor and dissociate the hydrogen. Hydrogen flies away and carbon is dissolved into the metal. After reaching the solubility of carbon in the metal at that temperature, the carbon precipitates out and crystalizes in the form of carbon-nanotubes. There are two cases. When the interaction between catalyst and substrate is weak, hydrogen decomposes on the top of the metal and carbon diffuses down in which CNT grows at the bottom pushing the metal particles off the substrate. This is known as tip-growth model (figure 3.3 a). When the interaction between catalyst and substrate is strong, CNT fails to push the metal particles up resulting in the participation happening on the top of the metal. At the
Beginning carbon forms a hemispherical dome, and then continues to form the cylinder structure. This is known as base-growth model [29] (figure 3.3 b).

![Diagram of CNT growth models](image)

**Figure B.35:** Schematic of CNT growth (a) tip-growth model, (b) base-growth model [29]

In this work, base-growth model was used. CNTs were grown using AIXTRON Blackmagic CVD reactor which is the same for graphene growth. Samples were loaded into the chamber. And the chamber is pumped down to <0.1 mbar. After this pressure was reached, 700 sccm of H$_2$ gas was introduced at 500°C and 80 mbar for pre-annealing for 3 minutes. Then 50 sccm of C$_2$H$_2$ was introduced at the growth temperature. Once the growth time was reached, the gases and heater were cut-off and the system was pumped down. At last, the chamber was cooled under N$_2$ until the temperature was under 400°C.

### B.3 Liquid silicon crystallization method

Liquid silicon (CPS), as a potential silicon precursor for printing devices on flexible substrates, has been discussed in the previous chapter. In order to fabricate devices like diodes and transistors with higher performance, it is necessary to crystallize the a-Si for the increase in mobility. Generally, silicon can be crystalized by phase changing in two ways: solid-phase crystallization (SPC) and rapid thermal annealing (RTA). The SPC processes are able to convert amorphous silicon into poly-Si at high temperatures (>600°C) in a furnace for a long period of time. The RTA processes, compared to SPC, largely decreases the thermal budget and annealing time resulting in a higher throughput.
However, the grain size of the poly-Si produced by RTA is much smaller than SPC which limits the mobility. This is because in poly-Si, grains (crystallites) are separated by grain boundaries (GBs) which greatly influence the conduction properties. These GBs are mainly responsible for the scattering of majority carriers leading to a potential barrier between grains [28].

By increasing the grain size, the effect of GBs can be reduced. Figure 3.4 exhibits the effect of GBs on crystal structure and energy band diagram.

![Diagram showing grain boundary and crystallite](image)

Figure B.36: Effect of grain boundaries on (a) crystal structure, (b) potential barrier in energy band diagram [28]

Over the decades of research, a technique that is able to fabricate high quality poly-Si from a-Si is known as excimer laser crystallization (ELC). The basic principle of this process is to melt the silicon layer in a very short time using a laser, and poly-Si is achieved during subsequent solidification. Compared to thermal annealing, ELC produces poly-Si from the molten silicon, resulting to a higher quality poly-Si. Another advantage of this process is that it is compatible with substrates with a low thermal budget. In 2006, Shimoda, et al. introduced the fabrication of poly-crystallized silicon TFTs from liquid silicon using this technique [23]. However, the performance of this kind of devices is limited by the randomly positioned grain boundaries which results in low carrier mobility. In 2001, Wilt et al. developed a location controlled single grain (SG) TFT fabrication method based on a μ-
Czochralski method [24]. In 2012, Zhang, et al. used this method to produce TFTs using liquid silicon [25].

The schematic of the μ-Czochralski process is shown in figure 3.5. A silicon wafer is oxidized and patterned to create SiO$_2$ cavities of around 700nm deep (figure 3.5 a). These cavities are narrowed by depositing another silicon oxide layer using tetraethylorthosilicate (TEOS) by plasma-enhanced chemical vapour deposition (PECVD) in order to control the diameter of the cavities to around 100nm (figure 3.5 b). Next, an amorphous silicon layer is deposited on the wafer and crystalized using ELC. During the crystallization process, the silicon is molten to a certain depth in the cavity while at the bottom of cavity some silicon still remains solid. This is because in ELC, laser irradiation can only be absorbed by a shallow layer on the surface due to the high absorption coefficient of silicon. These solid amorphous silicon works as nucleation seeds and during the cooling down, solidification starts from the bottom and copy the pattern of the seeds to form a single-grain silicon layer (figure 3.5 c).

![Figure 3.5: Schematic of μ-Czochralski method: (a) first oxide layer to define the position, (b) second oxide layer to control the cavity size, (c) silicon crystallized from the bottom seed](image)

### B.4 Liquid silicon crystallization on CNT

In this section, an investigation of amorphous silicon (made from liquid silicon) crystallization (ELC) on CNT will be introduced and characterized. In this way, the CNTs could be used to be able to connect a bottom layer to a top layer of transistors. If the crystallization can start from the CNT, a transistor could be made easily. There are two assumptions. For one case, due to the unique nanostructure of CNT, it has the potential to work as a nucleation seed during silicon crystallization (figure 3.6 a). It is possible for silicon to be affected by the patterns of the CNTs during the crystallization from the bottom to the top. For the other case, due to the high thermal conductivity of CNT, the silicon
on CNT is colder than the outside area in which the silicon is not molten. The solid silicon becomes a nucleation seed and extends its structure near the CNT part (figure 3.6b).

In this work, CNTs were growth on a TEOS layer (80nm) of a silicon wafer as mentioned in the previous section. Liquid silicon (CPS) was deposited on CNTs using doctor blade and polymerized by UV lamp for 45 minutes. Next the wafer was baked at 350°C to transform polysilane into hydrogenated amorphous silicon (around 200nm). Then the wafer was placed in the furnace at 650°C for 2 hours to dehydrogenate the silicon. At last, the amorphous silicon was crystallized using excimer laser with 800, 850, and 900mJ/cm² fluence. Figure 3.7 shows the scanning electron microscope (SEM) images of CNTs and silicon on CNT before ELC crystallization. After the liquid silicon was deposited and transformed on CNT, there was a gap between the silicon on CNTs and the silicon on TEOS substrate. This is caused by the inherent gap (100-200nm) between CNTs and the surrounding substrate. This gap exhibits that the silicon layer failed to bridge the two areas so that no thermal conduction would happen during ELC crystallization (figure 3.8). The slopes of the silicon layer at the edge of the gap are caused by the volume shrinking of the liquid silicon during the transformation.

Figure B.39: SEM image of (a) CNTs, (b) amorphous silicon on CNTs
Figure 3.40: Schematic of the cross section after silicon deposited on CNTs

Figure B.41: Raman measurements of silicon without crystallization

Raman measurement takes place on the silicon without crystallization as a reference. The peak is in 480cm\(^{-1}\) which indicates that it is amorphous silicon. More importantly, it proves that although the TEOS layer is thin, the green laser of Raman cannot reach the crystal silicon substrate. As a result, the silicon substrate has no or very small effect on the Raman measurement (figure 3.9).

The Raman measurements are taken from within the CNT area, near the CNT area and away from CNT area. Figure 3.10 and 3.11 shows the scanning electron microscope (SEM) images and Raman measurements of silicon ECL crystallization with 800mJ/cm\(^2\) and 850mJ/cm\(^2\), respectively. After crystallization, the surface of silicon on CNTs becomes rough. This means, when silicon was molten, it tended to more adhere to, even penetrate into CNTs. All of the results exhibit a sharp peak at 520cm\(^{-1}\) which indicates that the silicon was crystalized. Figure 3.12 shows the scanning electron microscope (SEM) images and Raman spectroscopy measurements of silicon ECL crystallization with 900mJ/cm\(^2\). The Raman results indicate that the silicon on CNTs was poly-crystalized and the silicon
on the TEOS was micro-crystalized. According to Ishihara et al, the silicon films can be amorphized by pulse laser irradiation with energy higher than that for crystallization [26]. Because the CNTs are a better thermal conductive material, the temperature of silicon on CNTs during ECL crystallization was lower than the silicon on other areas. To be specific, the thermal conductivity of CNTs is around 5W/mK while the thermal conductivity of TEOS is about 0.1W/mK. For all of these energies, there is no clear evidence that show the crystallization behaviours between silicon near CNTs and silicon away from CNTs are different. Considering the gap as mentioned, there is no thermal transfer between the silicon on CNTs and outside of CNTs.

Figure 3.13 shows that it is possible that liquid silicon can fail to deposit on the substrate. This is because of the low accuracy of doctor blading method. The colour difference indicates that there is a different material in figure 3.13(b). Also, the Raman signal confirms that it is TEOS.

![Figure 3.13](image)

Figure 3.13: SEM and Raman measurements of silicon after ECL crystallization with 800ml/cm². (a) SEM image, (b) on CNTs, peak in 520cm⁻¹, (c) near the CNTs, peak in 520cm⁻¹, (d) away from CNTs, peak at 520cm⁻¹

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Figure B.43: SEM and Raman measurements of silicon after ECL crystallization with 850mJ/cm$^2$, (a) SEM image, (b) on CNTs, peak in 520cm$^{-1}$, (c) near the CNTs, peak in 520cm$^{-1}$, (d) away from CNTs, peak at 520cm$^{-1}$

Figure B.44: SEM and Raman measurements of silicon after ECL crystallization with 900mJ/cm$^2$, (a) SEM image, (b) on CNTs, peak at 520cm$^{-1}$, (c) near the CNTs, peak at 518cm$^{-1}$, (d) away from CNTs, peak at 518cm$^{-1}$
B.5 Discussions

Although CNTs has no thermal effect on the area around it, the energy needed for silicon on CNTs could probably higher than that on silicon oxide due to its higher thermal conductivity. Further investigation is still requested to confirm this using lower laser energy. If with a certain energy that is lower than 800mJ/cm², silicon on CNT cannot be crystallized while the silicon on TEOS can be crystallized.

B.6 Conclusion

Silicon (made from liquid silicon) ELC crystallization behaviour on CNTs was investigated. Silicon can be crystallized on CNTs. However, the crystallization products on CNTs are different than that of on flat surface. After the laser irradiation, silicon is molten and tends to penetrate in CNTs. Thus, the surface of the silicon is rough because it is largely influenced by the structure of CNTs. Thus, more researches are still needed to apply this technique for fabricating devices due to the surface roughness.
Bibliography


