Systematic Measurement and Optimization Of a Universal Transducer Interface in Resistive-Bridge Mode

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Abstract

The Universal Transducer Interface (UTI) is a mass-produced interface circuit which can realize the functions of measuring signals of various sensors such as capacitive sensors, resistive-bridge sensors and resistive sensors. For some of the front-ends, an instrumentation amplifier, which is implemented with dynamic-element-matching (DEM) for its feedback structure, is integrated in the chip. In certain UTI modes, this amplifier is used to amplify small output signals of a resistive-bridge sensor or a single resistive sensor before it enters the applied modulator.

According to customers’ complaints, the UTI doesn’t work well. This thesis describes how with systematic investigations three problems have been identified. The first one is that undesired offset is introduced by the limited common-mode rejection ability of the instrumentation amplifier. The second one is that for input common-mode voltages higher than 3.4V, the On-resistances of the applied NMOS switches that control the DEM loop, cause the system to be out of function. The third one is that the electromagnetic interference can introduces unwanted noise in the wiring of the external resistive-bridge sensor.

Two dynamic-offset-canceling techniques have been proposed and one of them has been realized on board. With these techniques, the offset has been successfully reduced from up to 200µV to about 7 µV. The noise introduced by interference can be eliminated by applying proper shielding.

Key words: resistive-bridge, resistive sensors, dynamic-offset-canceling, electromagnetic interference, universal sensor interfaces.
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1. Introduction

1.1 Background

Much information people care about is analog, such as temperature for a baker, humidity for a flower grower, and weight for everybody. Various sensors have been developed in order to convert important information (thermal, chemical, mechanical, magnetic or optical) to the electrical domain. Afterwards, an interface whose resolution is not lower than that of the sensor is used to convert the electrical information to digital domain so that the data can be further processed or used (Fig 1-1).

![Figure 1-1. How the analog information is acquired in the sensor system](image1)

Based on the objective to measure various kinds of sensor systems with a low-cost interface, a Universal Transducer Interface (UTI) was developed by Frank van der Goes in his Phd project [8]. The CMOS technology makes it feasible to realize multiple functions in a small-size interface. The increasing need for the sensor interfaces makes mass-production economical feasible, so that the cost per chip can be low. The UTI was commercialized by Smartec and is available in the market until now. The UTI can measure signals from various sensors such as capacitors, platinum resistors, thermistors, resistive bridges and potentiometers (Fig1-2). The UTI output signal is processed by a microcontroller, and transferred to the PC by a serial port (RS232). In the PC the information can be analyzed, for instance, by the Labview program.

![Figure 1-2. The UTI is able to measure signals from various sensors](image2)
1.2 Applications of the UTI in the resistive-bridge mode

In my master project, the research is focused on the performance of the UTI in the resistive-bridge modes (mode 9-mode 14) (appendix 1). There are many applications for the UTI in these modes. These applications include, for example, pressure sensor such as piezo-resistive gauge [1], and mΩ resistance measurements [2]. The imbalance in piezo-resistive gauges is caused by the piezo-resistive effect. The sensitivity of this type of pressure sensor is very high so that the maximum imbalance can be in the order of 4%. A disadvantage of these sensors is that the imbalance is also temperature dependent. This effect can, to the first order, be compensated for by measuring the bridge output voltage $V_{CD}$ relative to the current $I_B$ through the bridge. As shown in Fig 1-3, this current can be measured as $V_{CD}$ across a reference resistor $R_{ref}$. It is evident that the long-term stability of the sensor is also dependent on that of the reference resistor. Hence, this resistor should be chosen with care.

$$\text{pressure } \sim \frac{V_{CD}}{V_{AB}} = \varepsilon \frac{R_g}{R_{ref}} = \frac{R_c R_3 - R_1 R_4}{(R_1 + R_2 + R_3 + R_4) R_{ref}} \quad R_g = (R_1 + R_2) || (R_3 + R_4)$$

Figure 1-3. Schematic of temperature-independent biasing of a piezo-resistive pressure sensor in UTI modes 11 and 12.

Reference [2] introduces another application: the measurement of mΩ contact resistances. It is meaningful to measure the resistance value to judge whether a machine is still in contact or not and to use the corresponding information to control a system. As shown in Fig 1-4, $R_{bias}$ is used to bias the circuit so that the current in the sensor resistance is small enough to limit the self heating effect. According to [3], when the maximum ratio of $\frac{V_{CD}}{V_{CD}}$ is 0.25% , the instrumentation amplifier is needed, which is the case in mode 12 (Appendix 1).
1.3 Challenges, motivations and objective

The UTI has been in the market for many years and a variety of complaints came from those customers using the UTI in the resistive-bridge modes in which the front-end instrumentation amplifier was used. These complaints were that the UTI was very noisy or that it ran out of function, etc. At the start of my project, the details of these complaints and their causes were missing. In my master project, my task was to explore the problems through systematic measurement and to dig out the mechanism behind the problems. My final objective was to propose some methods to solve the problems so that the UTI could work well in the resistive-bridge modes. Such development-driven research activities are quite meaningful both for the customers of the UTI from the application point-of-view and for the laboratory from a scientific point-of-view.

1.4 Outline

This thesis is organized as follows. The working principle of the UTI and some measurement techniques applied in the UTI are introduced in the chapter 2. Chapter 3 presents the measurement results which show that a systematic error is introduced in the UTI because of the limited common-mode rejection of the IA. A dynamic offset-cancelation technique that can reduce the error is proposed and experimentally verified. Chapter 4 presents the measurement results which prove that a significant amount of noise is caused by interference. It is shown that this problem can be solved with proper shielding and shielding techniques. Chapter 5 presents the conclusion of the thesis and future work that can be further done.
2. Working principle

Understanding the working principle is a first requirement to dig into the details of a problem. Therefore, a brief introduction of UTI in the resistive-bridge modes is presented now. The system architecture is shown in Fig 2-1. A DC drive voltage is chopped to an AC voltage before it excites the sensor so that the effect of low-frequency interference, 1/f noise of the front-end electronics can be eliminated by the low-pass filter, while the wanted sensor signal is saved. The imbalance of the resistive bridge, presented by the ratio $V_{CD}/V_{AB}$ (Fig 1-3), represents the wanted information. As was introduced in section 1.2, the typical maximum imbalance of the bridge is 0.25% for mΩ resistance measurement and 4% for piezo-resistive gauges, respectively. Since both $V_{AB}$ and $V_{CD}$ are facing the same voltage-to-time modifier, front-end electronics is used to divide $V_{AB}$ by 32 and multiply $V_{CD}$ by 15 so that they can fit in the same dynamic range of the voltage-to-time ($V$ to $T$) modifier when the maximum imbalance is 0.25%. When the maximum imbalance is 4%, $V_{CD}$ is directly transferred to the voltage-to-time modifier. The signal is converted to the time domain by the voltage-to-time modifier and the function of analog-to-digital is realized by measuring the period, with the help of a counter in the micro-controller. After the information is transferred to the PC via a serial port, it can be read, for instance, by Labview program.

![Figure 2-1. The system architecture when UTI is working in resistive-bridge modes](image)

2.1 Front-end electronics

2.1.1 Instrumentation amplifier with DEM loop

The 15 times amplification is realized by an instrumentation amplifier with resistive feedback with dynamic element matching [4] (Fig 2-2). The connections to the two negative input nodes of the Op-amps are made with switches $S_1$ and $S_2$, respectively. No current flows through switch $S_1$ so that the voltage across $R_1$ is $V_{in}$. The outputs of the two Op-amps supply the current and the voltage drop across switches $S_3$ and $S_4$ introduces non-linearity. To solve the problem, the sense switches $S_5$ and $S_6$ are used so that the effect of non-linearity of the forcing
switches is eliminated. The output of the IA can be expressed as follows:

\[
V_{\text{out}} = \frac{R_1 + R_2 + \cdots + R_{15}}{R_1} V_{\text{in}}
\]  

(2-1)

The accurate 15-time amplification can be achieved only when the resistances in the feedback loop are identical, which is obviously conflicts with the reality. In case of a mismatch \( \varepsilon \), a resistance \( R_i \) can be expressed as:

\[
R_i = R_0 (1 + \varepsilon_i),
\]  

(2-2)

where \( R_0 \) represents the average value of the 16 resistances.

\[
\sum_{i=1}^{16} \varepsilon_i = 0, \quad i \in [1,16],
\]  

(2-3)

When dynamic element matching is used [1], the gain error is reduced to only:

\[
\delta \approx \frac{1}{16} \sum_{i=1}^{16} \varepsilon_i^2
\]  

(2-4)

Figure 2-2. The schematic of an instrumentation amplifier with dynamic element matching technique [1]
2.1.2 Divider with DEM technique

The drive voltage $V_{AB}$ of the system is 5V, which is much larger than the input range of the voltage-to-time modifier. In order to solve the dynamic range problem, a voltage divider is needed to divide $V_{AB}$ by 32 and the diagram is shown in Fig 2-3. The divider is composed of 8 resistances and 4 capacitances. The resistance ladder provides a division ratio of 8. When measuring the bridge voltage, only one of the four capacitances is used to sample the signal while 4 capacitances are used when measuring output of the bridge. Therefore, the division ratio of 4 is realized by this method. To overcome the division-ratio error caused by the mismatch of the resistances and that of the capacitances, dynamic-element-matching technique is used. The switches $S_{r,1}$ to $S_{r,9}$ and $S_{c,1}$ to $S_{c,4}$ are applied to choose the signal path so that there are totally 32 types of signal paths and the DEM technique is realized.

Figure 2-3. The schematic of the voltage divider with dynamic element matching technique

2.2 Voltage to time modifier

The conversion from voltage to time is realized by an integrator. The circuit diagram and the related signals are seen in Fig 2-4. $V_{o1}$ and $C_{o1}$ are used to provide enough time to sample $V_{o,IA \_dm}/2$ on $C_s$, $V_{o2}$ and $C_{o2}$ are used to provide enough time to charge $C_{o1}$ by $V_{o1}$ in case that $V_{o,IA \_dm}/2$ is very small or even zero. In phase 1, the charge of $Q_1 = V_{o1}C_{o1}$ of $C_{o1}$ is pumped into the integrator and removed by integration of $I_{int}$. At the same time, a charge of $Q_2 = (V_{o,IA \_dm}/2 + V_{o,IA \_cm})C_s$ is pumped into $C_s$. In phase 2, the charge of $Q = (-V_{o,IA \_dm}/2 + V_{o,IA \_cm})C_s + V_{o2}C_{o2}$ is pumped into $C_s$ and the difference of the charges, which is $Q_2 = V_{o,IA \_dm}C_s + V_{o2}C_{o2}$, is removed by the integration of $I_{int}$. For the complete period in one measurement cycle, $T_{msm}$, it is found that:

$$T_{msm} = \frac{4(V_{o,IA \_dm}C_s + V_{o2}C_{o2} + V_{o1}C_{o1})}{I_{int}}$$ (2-5)

The term $V_{o2}C_{o2} + V_{o1}C_{o1}$ in equation 2-5 can be calibrated by the three-signal calibration technique, which will be introduced in 2.3. Therefore, the voltage $V_{o,IA \_dm}$, which involves the
information of the wanted signal, is linearly converted to the time domain.

2.3 Measurement technique

2.3.1 Three-signal-calibration method

The three-signal calibration is performed at the system-level. This autocalibration technique can eliminate the effects of offset and unknown gain. This technique can be explained practically by the example of measuring the weight of a stone with an inaccurate scale. Let’s assume that the scale is a linear system whose function is \( W_{\text{screen}} = AM + B \). \( W_{\text{screen}} \) is the number seen on the scale and \( M \) is the real weight of the stone.

In three-signal calibration technique, the first measurement is done when nothing is put on the scale and \( W_{\text{offset}} \) is the number seen on the scale.

\[
W_{\text{offset}} = B \quad (2-6)
\]

The second measurement is done when the real stone is measured by the scale. \( W_s \) is the number seen on the scale and \( M_s \) is the real weight of the stone.

\[
W_s = AM_s + B \quad (2-7)
\]
The third measurement is done when the reference is measured by the scale, \( W_{\text{ref}} \) is the number seen on the scale and \( M_{\text{ref}} \) is real weight of the reference.

\[
W_{\text{ref}} = AM_{\text{ref}} + B \tag{2-8}
\]

Although A and B are unknown parameter, by combining equations 2-6, 2-7 and 2-8, \( M_x \) can be calculated as follows:

\[
\frac{M_x}{M_{\text{ref}}} = \frac{W_x - W_{\text{offset}}}{W_{\text{ref}} - W_{\text{offset}}} \tag{2-9}
\]

Even when A and B drift with time, the relative accuracy is maintained with the help of this technique, using equation 2-9.

To apply this technique, in the UTI one measurement cycle is divided into three measurement phases. Assuming that there are n periods in one measurement phase, using equation 2-5, the three time intervals in the UTI can be express as:

\[
T_x = n \frac{4(V_{o_{14\_dm}}C_s + V_{o_2}C_{o_2} + V_{o_1}C_{o_1})}{I_{\text{int}}} \tag{2-10}
\]

\[
T_{\text{offset}} = n \frac{4(V_{o_2}C_{o_2} + V_{o_1}C_{o_1})}{I_{\text{int}}} \tag{2-11}
\]

\[
T_{\text{ref}} = n \frac{4(V_{\text{ref}}C_s + V_{o_2}C_{o_2} + V_{o_1}C_{o_1})}{I_{\text{int}}} \tag{2-12}
\]

From these equations, it can be derived that:

\[
\frac{V_{o_{14\_dm}}}{V_{\text{ref}}} = \frac{T_x - T_{\text{offset}}}{T_{\text{ref}} - T_{\text{offset}}} \tag{2-13}
\]

The output signal of the UTI is as shown in Fig 2-5. For identification reasons, \( T_{\text{off}} \) is separated into two periods.

![Figure 2-5. The output of UTI](image)

Since the sensor signal is calculated from these three periods, memory and calculation unit are required. This can be realized by using a micro-controller.
2.3.2 Chopping technique

As was shown in Fig 2-1, the drive voltage is chopped to a high frequency, i.e. a frequency higher than the corner frequency of the $1/f$ noise. Also the effect of low-frequency interference can be eliminated. To explain the ability of the system for suppression of low-frequency interference, we simplified the system as shown in Fig 2-6.

Assume that the chopping frequency is $1/2T$ and $C_s=C_{int}$, according to [5], the transfer function in z-domain $V_{int}(z)/V_{LF}(z)$ is given by $H_1(z)$:

$$H_1(z) = 1 - z^{-1}$$  \hspace{1cm} (2-14)

Translation of (2-14) to the frequency domain results in $H_1(e^{j\omega T})$

$$H_1(e^{j\omega T}) = 2j \exp\left(-\frac{j\omega T}{2}\right) \sin\left(\frac{\omega T}{2}\right)$$ \hspace{1cm} (2-15)

The modulus of $H_1(e^{j\omega T})$ is depicted in Fig 2-7.

The frequency of $V_x$ is located at the maximum of the transfer function and the low-frequency interference is located close to zero and filtered.
3. Dynamic common-mode offset cancelation

3.1 Theoretic derivation of the offset in the resistive-bridge mode

When the IA is used in the resistive-bridge modes (mode 10/mode 12/mode 14), measurement results indicate that a systematic offset is introduced. Since the DC drive voltage is chopped, the common-mode voltage at the input of the IA is a square voltage (Fig 3-1). It has been found that the value of the offset strongly depends on the amplitude of the common-mode square voltage.

When the amplitude of the common-mode square voltage is close to rail to rail, this offset is caused by the difference between the offsets caused by (a) the mismatches of the NMOS input pairs and (b) those of the PMOS input pairs. The details of this phenomenon will be discussed in section 3.1.1.

When the amplitude of the common-mode square voltage is in the range so that both PMOS input pairs and NMOS input pairs function, this offset is caused by the difference between the gains of the two Op-amps, which will be discussed in details in section 3.1.2.

The switches controlling the DEM loop are found to be just NMOS switches. With the increase of the common-mode input voltage, the on-resistances of the switches will increase until the Op-amps can not be operational for common-mode input voltages higher than 3.5V. The details will be discussed in 3.1.3.

3.1.1 Mismatches of P-input pairs and of N-input pairs

The inputs of the Op-amps used in the UTI are composed of both an NMOS pair and a PMOS pair, as shown in Fig 3-2. For mode 12, the measurement setup of the UTI is as shown in Fig 3-3. According to the requirements in the UTI application notes [6], the voltage $V_{AB}$ over the reference resistor should be between 100 mV and 200mV. Therefore, in the circuit of Fig 3-3 (b), the common-mode square voltage at the input of IA is close to the rail-to-rail value. As is seen in Fig 3-2, only NMOS input pairs are functioning when the common-mode voltage $V_{cm1}$ is higher than $V_{dd}-V_{gs}-V_{dsat}$ while only PMOS input pairs are working when common-mode
voltage $V_{cm2}$ is lower than $V_{gs} + V_{dsat}$.

Since the input-referred offset of a CMOS Op-amp is in the order of mV, the difference between offsets of NMOS input pairs and PMOS input pairs is likely to cause a systematic offset which is big compared to the measurement full-scale bridge-output voltage, which in mode 12 amounts to 12.5mV only.

![Figure 3-2. Input stage of the Op-amp](image)

![Figure 3-3. Measurement structure in mode 12](image)

### 3.1.2 Mismatch of the Op-amps

In mode 10, the common-mode voltage at the input of the IA is about 2.5V (Fig 3-4), which is big in comparison with the signal to be measured. Since the Op-amps are not ideal, due to finite CMRR, a differential output voltage $V_{od}$ is produced by the common-mode input $V_{ic}$ of the IA.

$$V_{od} = V_5 - V_6 = \frac{R_1 + R_3 + R_4}{R_2} \frac{1}{(\frac{R_1}{R_2} + A_1 + 1)(\frac{R_3}{R_2} + A_2 + 1) - \frac{R_1}{R_2} \frac{1}{R_2}} (A_1 - A_2)V_{ic}$$  \(3.1\)

(Detailed calculation can be found in Appendix 2)
Since A1 and A2 are more than 100dB and \( \frac{R_s + R_x + R_i}{R_2} \) is 15, \( V_{od} \) can be approximated as \( \frac{15 \Delta A}{A_1 A_2} V_{ic} \). Therefore, the mismatch of the gains of the two Op-amps will cause finite common-mode rejection ability.

![Instrumentation amplifier used in UTI](image)

**Figure 3-4. Instrumentation amplifier used in UTI**

As discussed in section 2.3.2, in the UTI a chopping technique is used (Fig 3-5), which eliminates any constant offset at the input of the IA. However, since the common-mode voltage at the input of the IA is chopped between \( V_{cm1} \) and \( V_{cm2} \) as is shown in Fig 3-6, the variable offset caused by the changing common-mode voltage is not fully removed by this chopping technique. When the common-mode voltage is \( V_{cm1} \), the corresponding differential output is \( V_{od_{1}} \). When the common-mode voltage is \( V_{cm2} \), the corresponding differential output is \( V_{od_{2}} \).

For the full period time \( T \) it holds, that

\[
T_{1x} + T_{2x} + T_{3x} + T_{4x} = \frac{4C_s (15V_x)}{I_{int}} + \frac{2C_s (V_{od_{1}} - V_{od_{2}})}{I_{int}}
\]

Therefore, due to the finite common-mode-rejection ability of the IA, the difference between the offsets produced by \( V_{cm1} \) and \( V_{cm2} \) introduces systematic offset.

![Synchronous detection to suppress the offset from the amplifier and common-mode voltage](image)

**Figure 3-5. Synchronous detection to suppress the offset from the amplifier and common-mode voltage**
3.1.3 NMOS switches inside the DEM loop

Investigations of the layout of the IA showed that the switches controlling the DEM loop are made by NMOS transistors (Fig 3-7). Since the ON-resistance of a NMOS switch strongly depends on the input voltage, so that a high common-mode input voltage can result in a high On-resistance, thus causing failure of the system.

![Image of sequence chart showing changing V_od which causes offset](image)

**Figure 3-6.** Sequence chart showing changing $V_{od}$ which causes offset

With Cadence, using actual layout information, a simulation of the On-resistance has been done. For this simulation, we used the schematic of Fig 3-8. The simulated On-resistance vs. $V_{gs}$ is plotted in Fig 3-9. When $V_{gs}$ is larger than 1.7V, the on-resistance is smaller than 10k$\Omega$. When $V_{gs}$ decreases from 1.7V to 1.5V, the ON-resistance increases dramatically from 10 k$\Omega$ to 1 M$\Omega$.

![Image of NMOS switches used to control the DEM loop](image)

**Figure 3-7.** NMOS switches are used to control the DEM loop

With Cadence, using actual layout information, a simulation of the On-resistance has been done. For this simulation, we used the schematic of Fig 3-8. The simulated On-resistance vs. $V_{gs}$ is plotted in Fig 3-9. When $V_{gs}$ is larger than 1.7V, the on-resistance is smaller than 10k$\Omega$. When $V_{gs}$ decreases from 1.7V to 1.5V, the ON-resistance increases dramatically from 10 k$\Omega$ to 1 M$\Omega$.
As is seen in Fig 3-10, the difference between the outputs of the two Op-amps is $V_d$, which could be approximated as

$$V_d = \frac{2R_{on} + R_1 + R_2 + R_3}{R_2} V_{off}. \quad (3-1)$$

The simulation result shows that $R_1$ and $R_3$ are equal to 39.2 kΩ and $R_2$ equals to 5.6 kΩ. With the increase of $V_{ic}$, $R_{on}$ of the switch will increase to a huge value so that $V_d$ will become very big. At a certain moment, $V_d$ is too big to be handled by the Op-amp and Op-amp will clip.
The effect of this has also been verified, using a Cadence simulation for the circuit of Fig 3-11. The input-referred offset in CMOS technology, which is in the order of a few mV, was modeled with a voltage source of 1mV at the input of the upper Op-amp. The simulated output voltages of the two Op-amps are shown in Fig 3-12. When the input common-mode DC voltage is increased to 3.35V, the upper Op-amp starts to clips so that the system is out of function. Fig 3-13 shows that, when the common-mode input voltage increases from 3.35V to 3.64V, the differential output of the IA in front of the modulator decreases from 15mV to 0.
3.2 Measurement results and analysis

3.2.1 DC measurement

A series of DC measurements has been performed to prove that the chopping technique used in the UTI is able to eliminate the effect of a constant offset in front of the modulator.
The measurement setup is shown in Fig 3-14. An external DC voltage source $V_{dc}$ is used to modify the common-mode DC voltage at the input of the IA. When $V_{dc}$ is increased from 0V to 10V, the common-mode DC voltage increases from 0V to 5V. Nodes C and D are short-circuited so that the input-referred offset can be calculated from the measured result. The input-referred noise is calculated from the standard deviation of 1000 measurement results. The measurement has been done in a grounded shielded box.

For mode 10/slow mode (the mode with an IA), the measured input-referred offset and noise are shown in Fig 3-15 and Fig 3-16, respectively. In Fig 3-15, for a DC common-mode voltage between 3.4V to 3.6V, an offset peak is found. Apart from this region, the chopping technique works well and an input-referred offset of less than 10μV is found. The appearance of the offset peak will be analyzed in section 3.5. Over the entire common-mode range, the input-referred noise is below 1.5μV (Fig 3-9). Because this noise is partly caused by that of the external DC voltage sources, the measured value of 1.5μV is reasonable close to the 700nV mentioned in the application notes [6].

![Figure 3-14. The DC measurement setup in a grounded shielded box](image)

![Offset ($V_{cd}$) vs. common-mode DC voltage (mode 10/slow mode)](image)

(a) When $V_{dc}$ is changed from 0V to 10V
Figure 3-15. Input-referred offset vs. common-mode DC voltage (mode 10/slow mode)

Figure 3-16. Input-referred noise vs. common-mode DC voltage (mode 10/slow mode)

The noise behavior and input-referred offset measured in mode 9 (in which no instrumentation amplifier is used) are shown in Fig 3-17 and Fig 3-18 respectively. When the common-mode DC voltage increases from 0V to 5V, both noise and offset are within a reasonable range. Therefore, it proves that the offset peak which appears in mode 10 is caused by the use of the instrumentation amplifier.
3.2.2. AC measurement

A series of AC measurements has been performed to prove that the variable offset voltage caused by the changing common-mode voltage introduces a systematic offset, as was analyzed in 3.1.

The measurement setup is shown in Fig 3-19. Nodes C and D are short-circuited so that the input-referred offset can be calculated from the result. To modify the amplitude of the common-mode square voltage, a potentiometer of 202 Ω is used. The common-mode square-wave voltage at nodes C and D is shown in Fig 3-20. The amplitude $V_c$ of this voltage amounts to:

$$V_c = V_{cm1} = \frac{V_{dd}}{2} = \frac{R_{b2} + R_{s2}}{R_{b1} + R_{b2} + R_{s1} + R_{s2}} V_{dd} - \frac{V_{dd}}{2}$$ (3-2)
When $R_{x2}$ is increased from 0 $\Omega$ to 202 $\Omega$, $V_c$ increases from -2.2V to 2.2V. The input-referred offset and noise behavior measured in mode 10 (with IA) are shown in Fig 3-21 and Fig 3-22, respectively. When $V_c$ is lower than -1.1V or higher than 1.1V (Fig 3-14(a)), the offset varies significantly, which matches with the occurrence of the peak in the DC measurements (to be analyzed in 3.5). For $-1.1V < V_c < 1.1V$, Fig 3-14(b) shows the zoomed-in plot of the measurement results. This figure shows a linear relation between the offset and $V_c$, which is in agreement with the effects of gain mismatching (see section 3.1.2). The noise behavior is shown in Fig 3-22. This figure shows a dramatical increase of the noise for common-mode voltages lower than -1.1V or higher than 1.1V.

![Figure 3-19. The AC measurement setup in a grounded shielded box](image)

![Figure 3-20. Common-mode voltage at nodes C and D in time domain](image)

(a) When $R_{b2}$ changes from 0 $\Omega$ to 202 $\Omega$
For mode 9 (without IA), the measured input-referred offset and input-referred noise are shown in Fig 3-23 and Fig 3-24, respectively. For $-2.2V < V_c < 2.2V$, both offset and noise are within the requirements (appendix 1). Therefore, it can be concluded that the undesired behavior of the UTI in mode 10 results is caused by the IA.
3.3 Two Dynamic Offset Cancelation Techniques and Feasibility Verification

3.3.1 Dynamic Op-Amp matching (DOAM)

When the two Op-amps would be perfectly matched, the measured offset can be removed. To deal with the unavoidable mismatch, the same can be achieved by dynamic Op-amp matching (DOAM) [7].

To realize this, two quads of switches are needed in front and after the IA (Fig 3-25). In order to illustrate how DOAM is working, the sequence chart is shown in Fig 3-26. From $T_1$ to $T_4$, $\varphi_4$ is close while $\varphi_3$ is open, which makes the time interval from $T_1$ to $T_4$ equal to $\frac{1}{I_{int}} \int_{t_{off}}^{t_{on}} (60V_c + 60V_{off}) + 2C_s(V_{ad,c1} - V_{ad,c2})$. From $T_5$ to $T_6$, $\varphi_3$ is close while $\varphi_4$ is open, which makes the
time interval from \( T_5 \) to \( T_8 \) equal to \( \frac{C_i(60V_i + 60V_{off})}{I_{int}} + \frac{2C_i(V_{out,c2} - V_{out,c1})}{I_{int}} \). Therefore, the offset introduced from \( T_1 \) to \( T_4 \) is compensated by that introduced from \( T_5 \) to \( T_8 \).

Therefore, the switches only need to be turned on or turned off once in the middle of \( T_x \).

Secondly, since the DEM resistance loop is used in the UTI, the switches needed in DOAM after the IA are already inside UTI [4], as is seen in Fig 3-27. Only two additional pairs of switches are needed in front of the IA in UTI, which means a relaxed requirement on the number of additional components.

---

**Figure 3-25 The schematics of the system with DOAM**

**Figure 3-26. The Sequence Chart after DOAM is used**

There are two reasons why UTI is a suitable system to integrate DOAM technique. Firstly, the measured signal is converted to the time domain and every full measurement cycle \( T_x \) (Fig 2-5) is the sum of 256 time intervals (each interval is from \( T_1 \) to \( T_4 \) shown in Fig 3-26) (slow mode) [6][appendix 1]. Therefore, the switches only need to be turned on or turned off once in the middle of \( T_x \). Secondly, since the DEM resistance loop is used in the UTI, the switches needed in DOAM after the IA are already inside UTI [4], as is seen in Fig 3-27. Only two additional pairs of switches are needed in front of the IA in UTI, which means a relaxed requirement on the number of additional components.
3.3.2 Dynamic common-mode voltage matching (DCMVM)

An alternative method to remove the offset is to use dynamic common-mode voltage matching. The switches are placed after the power supply and in front of the inputs of IA, as is seen in Fig 3-28. The principle is the same as that of dynamic Op-amp matching. The offset produced from \( T_3 \) to \( T_8 \) compensates that produced from \( T_1 \) to \( T_4 \). Since the power supply has already been chopped by switches, only 2 pairs of switches are needed in front of the IA to realize dynamic common-mode voltage matching. Both DOAM and DCMVM can realize the same function and the numbers of the extra switches needed are identical. However, the DCMVM technique can also be realized with discrete (external) components. With DOAM this is not the case, since the IA has already been integrated in the UTI.

3.3.3 Verification experiment on feasibility

To verify the theoretical analysis in 3.3.2, as a first experiment, the UTI was tested in mode 10/slow mode. The test has been performed using the full UTI system as shown in Fig 3-29, including the microcontroller and PC. For the input circuit at the sensor side, two measurement setups have been used, as shown in Fig 3-30. According to the calculation, in both setups, (a) and (b), the voltages \( V_{cd} \) should be equal to 125 \( \mu V \). However, in the measurement setup of Fig 3-30(a), the measured \( V_{cd1} \) was equal to 195.74 \( \mu V \). It can be concluded that the offset was
about 71 μV offset. Next, the polarity of power supply was converted and Nodes C and D were exchanged (Fig 3-30(b)), so that the dynamic common-mode voltage matching was realized manually. The measured $V_{cd2}$ was equal to 51 μV. So the offset amounted to about -74 μV. However, the mean value of $V_{cd1}$ and $V_{cd2}$ is about 123 μV, which only has 2 μV offset. This experiment shows that it is possible to reduce the offset by using DCMVM as proposed 3.3.2.

![Figure 3-29. Test Structure](image)

![Figure 3-30. Two measurement setups](image)

### 3.4 Board-level realization of DCMVM

#### 3.4.1 DCMVM with a frequency divider with a ratio of 4

As has been discussed in 3.3, switches and control signal are needed to realize the DCMVM. To implement the technique step by step, a board-level realization has been done first. The nodes E and F are chopped in all three phases of a measurement period. In our design, the voltage $V_E$ of node E has been chosen to produce the control signal. As has been analyzed in 3.3, the frequency of the control signal should be at least two times less than the chopping frequency from $V_E$. Fig 3-31 shows the frequency-divider circuit that has been used. This circuit provides a divider ratio of 4. The structure of the board-level system and the picture of
the board are shown in Fig 3-32 and a sequence chart is shown in Fig 3-33. The details of the components used in this setup are listed in Appendix 3.

Figure 3-31. A frequency-divider circuit with a ratio of 4 formed by Dual flip flops

Figure 3-32. Board-level system structure

Figure 3-33. Sequence chart when positive 4-sub-frequency circuit realized by positive-edge-triggered D flip flop is used.
The same measurement as that reported in 3.2.2 has been done. The input-referred offset and noise behavior are shown in Fig 3-34 and Fig 3-35 respectively. These figures show that there is a significant reduction of the input-referred offset. For $V_c > -1.1\text{V}$ or $< 1.1\text{V}$ an offset level was found that was less than 7 $\mu\text{V}$ (slightly visible in Fig 3-34(b)). For $-1.1\text{V} < V_c < 1.1\text{V}$, the input-referred noise was about 1.2$\mu\text{V}$ (Fig 3-35). The explanation of the slightly higher noise is that some extra components are added into the system. For $V_c < -1.1\text{V}$ or $> 1.1\text{V}$, DCMVM could not help since the system is out of order, which will be explained in section 3.5.

\[V_c (\text{V})\]

\[\text{Offset (} \mu\text{V)}\]

\(\text{With DCMVM}\)

\(\text{Without DCMVM}\)

\(\text{With DCMVM}\)

\(\text{Without DCMVM}\)

Figure 3-34. Input equivalent offset vs. common-mode AC voltage:
(a) For $0 \Omega < Rb2 < 202 \Omega$, (b) Close-up graph.
The measurements reported in 3.3.3 have been repeated with this new DCMVM system. Taking into account the on-resistances of the analog switches, which is about 10 Ω, the measurement setup is as shown in Fig 3-36. When using DCMVM, the measured $V_{cd}$ was 127.2 μV (it should be 125 μV) and the noise is 1 μV. The value of $V_{CD}$ agrees rather well with the average value of the measurements reported in Section 3.3.3. When $V_c$ is lower than -1.1V or higher than 1.1V, the system is out of function.

![Figure 3-35 Input-referred noise vs. common-mode AC voltage](image)

*Figure 3-35 Input-referred noise vs. common-mode AC voltage*

![Figure 3-36. Measurement structure](image)
3.4.2 DCMVM with frequency divider with a ration of 32

In the UTI, in the DEM loop of the IA, 16 resistances have been used. As is shown in Fig 3-37, with a 4-times ratio of the frequency divider, the offset introduced from $T_2$ to $T_9$ is compensated by that introduced from $T_{10}$ to $T_{17}$. Since for different loop positions the gains are different, the offset is not fully compensated. In the slow mode, the loop rotates 8 cycles. Therefore it could be of interest to apply 32-times divider. In that case, the offset introduced in one full cycle will be compensated by that in the next full cycle. Fig 3-38 shows a setup for such a divider circuit.

![Figure 3-37](image-url)

**Figure 3-37.** Sequence chart when a 32-times divider with positive-edge-triggered D flip-flops are used.

![Figure 3-38](image-url)

**Figure 3-38.** A circuit with a division ratio of 32.

The input-referred offset and noise behavior measured in mode 10/slow mode are shown in Fig 3-32 and Fig 3-33 respectively. When $V_c$ is higher than -1.1V and lower than 1.1V, the input-referred offset of the system with 32 sub-frequency circuit is smaller than 5 μV, which is slightly better than that of the system with 4-times divider circuit. At the same time, the noise behavior is also slightly improved. However, when $V_c$ is higher than 1.1V or lower than -1.1V, the performance of the system with a 32-times divider is even worse than that with 4-times one. Therefore, when $V_c$ is higher than 1.1 V or lower than -1.1V, there is another effects that
deteriorates the whole system. This will be discussed in section 3.5.

**Figure 3-32.** Input equivalent offset vs. common-mode AC voltage: (a) For $0 \Omega < R_b < 202 \Omega$, (b) close-up graph.
3.5 The analysis of the offset peak in DC measurement

Since the on-resistances of the NMOS switches in the DEM loop depend on the power supply of the system, an experiment has been done to investigate the effect of changing the power supply voltage. The measurement setup is shown in Fig 3-34. The input-referred offset measured in mode 10 (with IA) is shown in Fig 3-45. The common-mode DC voltage, where the offset peak locates, decreases with the decrease of the power supply. This result matches well with the previous analysis. Therefore, if the NMOS switches are replaced by suitable CMOS switches, the problems of the offset peak in DC measurement and deteriorated performance when $V_c$ is higher than 1.1 V or lower than -1.1 V in AC measurement will be solved.

Figure 3-34. The setup of the experiment
Figure 3-35. Input-referred offset vs. DC common-mode voltage
4. Suppression of Susceptibility to EMI of UTI

Some customers complained about the noise performance in the resistive-bridge modes with IA. The bridge structures are shown in Fig 4-1. In our experiments, we found that it is difficult to reach the specified 700nV resolution (appendix 1). This appeared to be due to EMI. During the measurement, two EMI phenomena exist. One is the fluctuation (Fig 4-2) of the offset voltage for the case that the loop-area of the bridge is not minimized, which is about several cm². The other is the increased noise when bridge is connected to the UTI by a long cable (Fig 4-3). To understand EMI problems clearly, the following questions need to be answered[8].

- Where are the noise sources and how can they be characterised
- Which part of the system is susceptible to the noise source
- How is the noise coupled into the system

If any of these three questions can be answered for a practical setup it might be possible to solve the EMI problems. These questions will be discussed in detail in chapter 4.

![Figure 4-1. Measurement structure in mode 9-12](image)

(a) mode 9/10  (b) mode 11/12

![Figure 4-2. Measured fluctuations of the offset voltage in mode 10/ slow for the case that the bridge is forming a loop.](image)
4.1 Systematic measurement

When facing EMC problems, most designers limit themselves to look for standard solutions, such as applying filters, grounding, screening and proper wiring, etc. However, it is also necessary to have insight into the fundamental causes. Since there are many reasons causing EMC problems, a systematic approach is needed.

4.1.1 Noise inside the UTI

At the beginning of the EMI study, an investigation has been done on the internal noise in UTI. The noise in the UTI is contributed by the comparator, the integrator, resistors, Op-amps and the power supply. All noise sources can be transferred to an equivalent input-referred noise voltage $V_{n,i}$ and an equivalent input-referred noise current $I_{n,i}$, as is seen in Fig 4-4. In [5] it has been calculated that the equivalent input noise voltage is 780nV in UTI in bridge mode with IA.

![Figure 4-4. The input equivalent voltage and input equivalent current in the system](image)

The maximal imbalance that can be measured in mode 10 is 0.25%. In order to make imbalance within the range, 4 resistors with almost equal values were chosen to form the bridge. A grounded shielded box has been used to block the path, through which external noise...
is coupled to the UTI. Three bridges with different bridge resistances are made and the corresponding measured noise figures are shown in table 4-1. The input equivalent noises in all measurements are below 800nV, which fits well with the theoretic calculation. Therefore, specification of the resolution in resistive-bridge mode can be reached if the internal noise is the only counted noise source.

<table>
<thead>
<tr>
<th>Bridge Resistance</th>
<th>Noise (nV)</th>
</tr>
</thead>
<tbody>
<tr>
<td>460 Ω</td>
<td>789</td>
</tr>
<tr>
<td>2.2 k Ω</td>
<td>760</td>
</tr>
<tr>
<td>5.6 k Ω</td>
<td>762</td>
</tr>
</tbody>
</table>

Table 4-1 Measured noise in mode 10/slow mode with shielding. The noise was derived from 4000 measurement samples.

To investigate the influence of the input noise current of the Op-amp, a similar measurement has been done in the shielded box. For this test, the measurement structure is as simple as that in Fig 4-4. This measurement was performed for different values of the resistor values $R_a$. The results are shown in Fig 4-5. It can be concluded that now the noise voltage equals the one specified in the application note. Furthermore, with the increase of the resistor values, there is hardly a change of the noise behavior. It can be concluded that the input noise currents of bonding pads, the protection circuits and the Op-amp have is not significant for the noise behavior of the system.

![Figure 4-4. Measurement Structure](image)

![Figure 4-5. Noise vs. Input Impedance](image)

4.1.2 Noise outside the UTI

The measurement has been repeated with the same resistive bridges as those mentioned in 4.1.1, for the case that there is no shielding. The input-referred noise figures are higher than 1.5μV (calculated from the stand deviation of 4000 measurement results). Compared with those in Table 4-1, the noise is increased when the setup is not shielded.
4.1.3 Immunity of UTI to the common-mode interference

Although shielding can solve the EMI problem in UTI, it is still necessary to understand how the EMI is coupled into the system. Interference can be classified into common-mode interference and differential-mode interference. In a first test, the resistances were connected as shown in Fig 4-4. Since input nodes C and D were short-circuited, no differential interference existed at the input.

Four different $R_a$ were chosen and the measurement was done without shielding. Input noise behaviors were shown in Table 4-2. All noises were around 700nV, which is close to the specifications in the application notes. It can be concluded that the UTI is immune to the common-mode interference in a lab environment. However, many customers of UTI apply the UTI in an industrial environment, where EMI can be much stronger than in laboratory. Therefore, we performed further testing with a well-defined source of interference:

<table>
<thead>
<tr>
<th>Resistance</th>
<th>Noise (mode 10)</th>
</tr>
</thead>
<tbody>
<tr>
<td>560Ω</td>
<td>719 nV</td>
</tr>
<tr>
<td>1.2 kΩ</td>
<td>692 nV</td>
</tr>
<tr>
<td>5.6 kΩ</td>
<td>674 nV</td>
</tr>
<tr>
<td>9.6 kΩ</td>
<td>669 nV</td>
</tr>
</tbody>
</table>

Table 4-2 Measurement Results in mode 10/slow mode without shielding, resolution calculated from 4000 samples

The measurement setup is shown in Fig 4-6. An external 5V DC voltage source in series with a sine-voltage generator was used. The UTI and the resistors were shielded in a grounded shielded box. The input-referred offset and noise behavior (mode 10/slow mode) were measured for various amplitudes and frequencies of the sine voltage.

![Figure 4-6. Measurement Setup](image)

Since the 50 Hz mains is one of the main interference sources, in a first test the frequency of the sine voltage is kept at 50 Hz and the $V_{cd}$ is measured when the amplitude of the sine voltage is increased. The plot of the input-referred offset and noise behavior in mode 10 are shown in Fig 4-7 and Fig 4-8, respectively. When the RMS value $V_{rms}$ of the sine wave is less than 1.2V, the man-made interference has little influence on the system. When the $V_{rms}$ is between 1.2 and 1.7V, the magnitudes of both offset and noise increase due to the interference. When $V_{rms}$ is...
higher than 1.7V, the system is out of function.

![Offset vs. Vrms (mode 10 / f(Vsin)=50Hz)](image)

**Figure 4-7. Input-referred offset vs. Vrms (mode 10/slow mode)**

![Noise vs. Vrms (mode 10 / f(Vsin)=50Hz)](image)

**Figure 4-8. Input-referred noise vs. Vrms (mode 10/slow mode)**

The same measurement has been performed in *mode 9*. The input-referred offset and input-referred noise behavior are shown in Fig 4-9 and Fig 4-10. When $V_{\text{rms}}$ is between 0 and 2V, the interference has little effect on the offset. When $V_{\text{rms}}$ is between 500 mV and 2V, the noise increases linearly with the increase of $V_{\text{rms}}$. It can be concluded that when $V_{\text{rms}}$ is smaller than 1.2V, the use of the DEM IA increases the immunity of the system to the 50Hz interference. However, when $V_{\text{rms}}$ is bigger than 1.2V, it will cause increased offset.

![Offset vs. Vrms (mode 9/f(Vsin)=50Hz)](image)

**Figure 4-9. Input-referred offset vs. Vrms (mode 9/slow mode)**
4.1.4 Immunity of the UTI to high frequency interference

The setup is shown in Fig 4-11. The measurement is done in a grounded shielded box. The interfering voltage $V_{\text{int}}$ is added by the signal generator and the signal has a sine-wave shape.

$$V_{\text{int}} = V_p \sin(\omega t)$$  \hspace{1cm} (4-1)

In Fig 4-11(a), the peak voltage between nodes C and B caused by the man-made interference can be calculated as follows:

$$V_{p_{\text{CB}}} = \frac{0.5R}{0.5R + \frac{1}{2\pi fC}} V_p \approx \pi RC f V_p,$$  \hspace{1cm} (4-2)

In order to keep $V_{p_{\text{CB}}}$ constant, the product $fV_p$ in equation 4-2 should be kept constant. For $V_p = 5V$ and $f = 100kHz$, $V_{p_{\text{CB}}}$ is 1.55 mV. In the setup of Fig 4-11(b), when a divider is added, $V_{p_{\text{CB}}}$ is 140.5 µV. The effect of this interference upon the offset and noise is shown in Fig 4-12 and 4-13. The interference voltage causes problems when the amplitude of the interference between the C and D nodes is in the millivolt level. However, when the interference between the C and D nodes is reduced to the hundred microvolt level, the problems of noise and offset are obviously improved. Usually, high-frequency interference is coupled into the system through radiation, and its amplitude will not be as high as millivolt level as long as the distance between the interference and the circuit is not too small. Therefore, the system could work well as long as this distance between circuit and the noise source such as micro-controller or DC-DC converter has been taken into account.
Figure 4-11. The schematics shows how the interference is added: (a) without divider (left)  
(b) with divider (right)

Figure 4-12. Input-referred offset vs. Frequency of the interference

Figure 4-12. Input-referred noise vs. Frequency of the interference
4.2 The Relation between Susceptibility to EMI and Bridge Structure

After many measurements, it is found that EMI phenomenon exists as long as the bridge forms a loop. For example, let us consider the connection of bridge resistors as depicted in Fig 4-13. Fig 4-14 shows a sequence of measurement samples for mode 10 without and with shielding and those measured in mode 9. In both mode 9 and mode 10, the noise is higher than the specifications on the [6]. The fluctuation of the measurement results causes the increase of the noise.

EMI has little influence when there is no loop in the resistive structures, such as that in Fig 3-23 and that in Fig 4-6. According to [8], the magnetic field is likely to be the source from which noise is produced.

![Figure 4-13, Resistive bridge structure which is susceptible to EMI](image)
In practical application, there are cables between the UTI and resistive bridge. To investigate the effect of the cable, an experiment shown in Fig 4-15 has been done. In comparison, the measurement has been done on the measurement setup when there exists no cable between the sensor and the UTI. The resistive bridge is shielded to remove the unwanted noise discussed in section 4.2 so that only the effect caused by the cable can be shown in the measurement result. The length of the cable is 20cm and it is twisted to eliminate the effect caused by the loop form by the cable. The experiment has been done in the lab environment. The input-referred noise behaviors are calculated from the measurement results and shown in Table 4-4.
Figure 4-15. The resistive bridge is shielded in the measurement

<table>
<thead>
<tr>
<th>Mode</th>
<th>Noise</th>
</tr>
</thead>
<tbody>
<tr>
<td>Without cable</td>
<td></td>
</tr>
<tr>
<td>mode 9 (without IA)</td>
<td>4.5 μV</td>
</tr>
<tr>
<td>mode 10 (with IA)</td>
<td>0.69 μV</td>
</tr>
<tr>
<td>With Cable</td>
<td></td>
</tr>
<tr>
<td>mode 9</td>
<td>9 μV</td>
</tr>
<tr>
<td>mode 10</td>
<td>0.9 μV</td>
</tr>
</tbody>
</table>

Table 4-4. Measurement Results

Figure 4-16, the equivalent circuits of the measurement with cable and without cable.

The Noise increases with the existence of the cable. To investigate the phenomenon in detail, the system is modeled as seen in Fig 4-16 corresponding to four measurement setups. $V_{n,1}$ and $I_{n,1}$ stands for the input-referred noise voltage and noise current caused by the IA respectively. $V_{n,2}$ and $I_{n,2}$ stands for the input-referred noise voltage and noise current caused by the modulator respectively. During previous measurement, it has been proved that the noise does not change when the input impedance is changed. Therefore, the equivalent noise currents are omitted during the noise calculation. $V_{n,c,dm}$ is the differential noise coupled by the cable and $V_{n,c,cm}$ is the common-mode noise coupled by the cable. In equation 4-5 and equation 4-6, $V_{n,c,dm, cm}$ stands for the equivalent differential noise caused by the common-mode noise at the input of the modulator.
(V_{n1})^2 + \left(\frac{V_{n2}}{15}\right)^2 = (0.69uV)^2 \tag{4-3}

(V_{n2})^2 = (4.5uV)^2 \tag{4-4}

(V_{n1})^2 + \left(\frac{V_{n2}}{15}\right)^2 + (V_{n,c,dm})^2 + \left(\frac{V_{n,c,dm}_{cm}}{15}\right)^2 = (0.9uV)^2 \tag{4-5}

(V_{n1})^2 + (V_{n,c,dm})^2 + (V_{n,c,dm}_{cm})^2 = (9uV)^2 \tag{4-6}

To judge whether the noise is mainly coupled in differential-mode way or common-mode way, assume \( V_{n,c,dm,cm} \) is zero and do the calculation.

From (4-5)-(4-3), \( V_{n,c,dm} = 0.577uV \)

From (4-6)-(4-4), \( V_{n,c,dm} = 7.79uV \)

Big difference exists between the two results.

Assume \( V_{n,c,dm} \) is zero.

From (4-5)-(4-3), \( V_{n,c,dm}_{cm} = 8.6uV \)

From (4-6)-(4-4), \( V_{n,c,dm}_{cm} = 7.79uV \)

The result fits much better. Therefore, the interference in the laboratory is mainly coupled at the input in common-mode way and IA suppresses the effect by 15×.

It is concluded that the cable between the sensor and the UTI will introduce common-mode interference the DEM Op-amp works well and helps to reduce the effect of common-mode interference.
5. Conclusions and Future Work

5.1 Conclusions

The systematic measurement has been done on the UTI under the resistive-bridge modes with the instrumentation amplifier. Because the switches in the DEM loop are made by NMOS transistors, the system will be out of function when the On-resistances of the switches is too high when common mode voltage is higher than 3.7V. When the common mode voltage is lower than 3.7V and the system is functioning, a systematic error, proportional to the amplitude of the common-mode square voltage, is introduced because of the limited common-mode rejection ability of the instrumentation amplifier. Two dynamic-offset-canceling techniques are proposed and one of them has been realized on board. It successfully reduces the systematic error from up to 200μV to about 7μV when the common mode voltage is smaller than 3.7V. The resistive bridge forms a loop and it will pick up differential interference in the ambient when changing electromagnetic field exists in the environment. This problem can be solved by the grounded shielding technique. When a long cable is used to connect the sensor to the UTI interface, it will pick up the common-mode interference in the ambient. The instrumentation amplifier could help to reduce the effect. An alternative way is shielding the wire.

5.2 Future Work

The optimization has only been realized on the broad level because the schematic of UTI is not available. It will be very meaningful to redesign UTI and integrate the dynamic-offset-canceling technique in the new chip to improve the performance of UTI. There are several improvements to be done as follows.

- Reverse the UTI's schematic from the layout
- Replace the NMOS switches in the DEM loop by the CMOS switches
- Integrate the dynamic-offset-canceling technique in the new chip.

More investigation can be done on the topic of interference to so that new methods can be proposed apart from the traditional shielding methods.
Appendix 1. Application notes when the UTI works in the resistive bridge modes

Mode 9. Ub2: resistive bridge, ref. is Vbridge, +/- 4% imbalance

In this mode, a resistive bridge can be measured where the ratio of the bridge output voltage $V_{CD}$ and the bridge supply voltage $V_{AB}$ represents the physical signal. The measurement range of the bridge imbalance is +/-4% in this mode.

The connection of the bridge to the UTI is shown in Fig A-1. The driving voltage across the bridge $V_{EF}$ is a square wave with amplitude $V_{DD}$. The frequency of this signal is 1/4 of the internal oscillator frequency.

Because force/sense wires are used, the bridge is measured in a 4-wire setup, as shown in Fig A-1 (a). The signals measured in the various phases are given in Table 16.

![Fig A-1. Connection of the resistive bridge to the UTI for the Ub2 mode in a 4-wire setup (a) and a 2-wire setup (b)](image)

During phase 2, the voltage across the bridge $V_{AB}$ is measured. A very accurate on-chip voltage divider divides this voltage by 32. This divider does not need calibration. After division, $V_{AB}$ is processed in the same way as $V_{CD}$.

<table>
<thead>
<tr>
<th>Phase</th>
<th>Measured voltages</th>
<th>Output periods</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>$V_0$</td>
<td>$T_{off} = NK_2V_0$</td>
</tr>
<tr>
<td>2</td>
<td>$V_{AB}/32 + V_0$</td>
<td>$T_{AB} = NK_2(V_{AB}/32 + V_0)$</td>
</tr>
<tr>
<td>3</td>
<td>$V_{CD} + V_0$</td>
<td>$T_{CD} = NK_2(V_{CD} + V_0)$</td>
</tr>
</tbody>
</table>

Table A-1. Measurement phases of the Ub2 mode
To find the bridge imbalance, the microcontroller calculates:

\[
M = \frac{1}{32} \frac{T_{\text{phase3}} - T_{\text{phase1}}}{T_{\text{phase2}} - T_{\text{phase1}}} = \frac{V_{CD}}{V_{AB}} \quad (A-1)
\]

The specifications are listed in Table A-2.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Typical value</th>
</tr>
</thead>
<tbody>
<tr>
<td>( K_a )</td>
<td>56 ( \mu )A/V</td>
</tr>
<tr>
<td>( V_0 )</td>
<td>0.54 V</td>
</tr>
<tr>
<td>Bridge excitation</td>
<td>( A ) ( V_{DD} )</td>
</tr>
<tr>
<td>Excitation current from E and F</td>
<td>20 mA</td>
</tr>
<tr>
<td>Bridge resistance ( R_b )</td>
<td>( 250 ) ( \Omega ) ( &lt; P_b &lt; 10 ) ( k\Omega )</td>
</tr>
<tr>
<td>Bridge output voltage</td>
<td>max ( \mu )A, -0.2V</td>
</tr>
<tr>
<td>Accuracy</td>
<td>11 bits</td>
</tr>
<tr>
<td>Offset</td>
<td>10 ( \mu )V</td>
</tr>
<tr>
<td>Resolution (SF = 0)</td>
<td>7 ( \mu )V</td>
</tr>
</tbody>
</table>

**Table A-2. Specifications of the Ub2 mode**

**Mode 10. Ub1: res. bridge, ref. is Vbridge, +/- 0.25% imbalance**

In this mode, a resistive bridge can be measured where the ratio of the bridge output voltage and the bridge supply voltage represents the physical signal. *The main difference with mode Ub2 is that the measurement range of the bridge imbalance is 0.25%. (\( V_{CD} = 12.5 \) mV for \( V_{DD} = 5V \)).* The connection of the bridge to the UTI is the same as in the Ub2 mode. An on-chip 15-times voltage amplifier amplifies the small output voltage before it is processed in the same way as the divided voltage across the bridge. Both the amplifier and divider do not need calibration. To calculate the bridge imbalance, Equation A-1 can be used, where 32 must be replaced by 480. Due to the use of the force/sense wires, the bridge is measured in a 4-wire setup. The various voltages measured during each phase are indicated in Table A-3. The specifications are listed in Table A-4.

<table>
<thead>
<tr>
<th>Phase</th>
<th>Measured voltages</th>
<th>Output periods</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>( V_0 )</td>
<td>( T_{off} = NK_2 V_0 )</td>
</tr>
<tr>
<td>2</td>
<td>( V_{AB}/32 + V_0 )</td>
<td>( T_{AB} = NK_2 (V_{AB}/32 + V_0) )</td>
</tr>
<tr>
<td>3</td>
<td>( 15V_{CD} + V_0 )</td>
<td>( T_{CD} = NK_2 (15V_{CD} + V_0) )</td>
</tr>
</tbody>
</table>

**Table A-3. Measured voltages during each phase of the Ub1 mode**
Table A-4. Specifications of the Ub1 mode

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Typical value</th>
</tr>
</thead>
<tbody>
<tr>
<td>$K_2$</td>
<td>56 $\mu$S/V</td>
</tr>
<tr>
<td>$V_0$</td>
<td>0.54 V</td>
</tr>
<tr>
<td>Bridge excitation</td>
<td>$V_{DD}$</td>
</tr>
<tr>
<td>Excitation current from E and F</td>
<td>20 mA</td>
</tr>
<tr>
<td>Bridge resistance $R_b$</td>
<td>$250 \Omega &lt; R_b &lt; 10 \text{k}\Omega$</td>
</tr>
<tr>
<td>Bridge output voltage</td>
<td>max +/- 12.5 mV</td>
</tr>
<tr>
<td>Accuracy</td>
<td>10 bits</td>
</tr>
<tr>
<td>Offset</td>
<td>10 $\mu$V</td>
</tr>
<tr>
<td>Resolution (SF = 0)</td>
<td>700 nV</td>
</tr>
</tbody>
</table>

Mode 11. Ib2: resistive bridge, ref. is Ibridge, +/- 4% imbalance

In this mode, a resistive bridge can be measured where the physical signal is represented by the output voltage of the bridge and the current through the bridge. This current $I$ is converted into a reference voltage. The connection of the bridge and the reference element is shown in Figure A-2(a). The value of $R_{\text{ref}}$ should be chosen such that $V_{AB}$ is between 0.1 V and 0.2 V. This mode can also be used to measure platinum resistors in a 4-wire setup. This is shown in Fig A-2(b). The advantage in comparison with mode Pt is that now only three phases have to be measured.

Figure A-2. Connection of the resistive bridge and a reference resistor to the UTI (a) and connection of a platinum resistor in 4-wire setup (b)

<table>
<thead>
<tr>
<th>Phase</th>
<th>Measured voltages</th>
<th>Output periods</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>$V_0$</td>
<td>$T_{\text{off}} = NK_2 V_0$</td>
</tr>
<tr>
<td>2</td>
<td>$V_{AB}+V_0$</td>
<td>$T_{AB} = NK_2 (V_{AB} + V_0)$</td>
</tr>
<tr>
<td>3</td>
<td>$V_{CD}+V_0$</td>
<td>$T_{CD} = NK_2 (V_{CD} + V_0)$</td>
</tr>
</tbody>
</table>

Table A-5. Measured voltages for each phase of the Ib2 mode
Mode 12. Ib1: resistive bridge, ref. is Ibridge, +/- 0.25% imbalance

This mode is similar to mode 11. The connection of the bridge and the resistor is shown in Figure A-2. The difference with mode 11 is that the bridge imbalance range is +/- 0.25%.

The voltage across the reference resistor should be between 0.1 V and 0.2 V, as in mode 11. The bridge output voltage is amplified 15 times before it is processed in the same way as the reference voltage. The voltages measured during each phase are indicated in Table A-7. The specifications of the Ib1 mode are listed in Table A-8.

<table>
<thead>
<tr>
<th>Phase</th>
<th>Measured voltages</th>
<th>Output periods</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>$V_0$</td>
<td>$T_{ef} = NK_2 V_0$</td>
</tr>
<tr>
<td>2</td>
<td>$V_{AB} + V_0$</td>
<td>$T_{AB} = NK_2 (V_{AB} + V_0)$</td>
</tr>
<tr>
<td>3</td>
<td>$15V_{CD} + V_0$</td>
<td>$T_{CD} = NK_2 (15V_{CD} + V_0)$</td>
</tr>
</tbody>
</table>

Table A-7. Measured voltages during each phase of the Ib1 mode

To find the bridge imbalance, the microcontroller calculates:

$$M = \frac{T_{phase3} - T_{phase1}}{15} = \frac{V_{CD}}{IK_{ref}}$$  \hspace{1cm} (A-2)

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Typical value</th>
</tr>
</thead>
<tbody>
<tr>
<td>$K_2$</td>
<td>56 μS/V</td>
</tr>
<tr>
<td>$V_0$</td>
<td>0.54 V</td>
</tr>
<tr>
<td>Bridge excitation</td>
<td>AC $V_{DD}$</td>
</tr>
<tr>
<td>Excitation current from E</td>
<td>20 mA</td>
</tr>
<tr>
<td>and F</td>
<td></td>
</tr>
<tr>
<td>Bridge resistance $R_b$</td>
<td>$250 \Omega &lt; R_b &lt; 10 \text{k}\Omega$</td>
</tr>
<tr>
<td>Bridge output voltage</td>
<td>max +/- 12.5 mV</td>
</tr>
<tr>
<td>Accuracy</td>
<td>10 bits</td>
</tr>
<tr>
<td>Offset</td>
<td>10 μV</td>
</tr>
<tr>
<td>Resolution (SF = 0)</td>
<td>700 nV</td>
</tr>
</tbody>
</table>

Table A-8. Specifications of the Ib1 mode
Mode 13. Brg2: resistive bridge +/- 4% and 2 resistors

In this mode, a resistive bridge with a maximum imbalance of +/-4% and two resistors can be measured. One of the resistors can be temperature dependent, so the bridge output can be digitally corrected for temperature effects. Both the voltage across the bridge and the current through the bridge are measured. The connection of the elements to the UTI is shown in Figure A-3. \( V_{EF} \) is a square wave with amplitude \( V_{DD} \) at \( 1/4 \) of the oscillator frequency. The voltage across \( R_{ref} \) should be between 0.1 V and 0.2V.

The voltages to be measured are indicated in Table A-9.

Figure A-3. Connections of the sensors to the UTI

<table>
<thead>
<tr>
<th>Phase</th>
<th>Measured voltages</th>
<th>Output periods</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>( V_0 )</td>
<td>( T_{off} = NK_2 V_0 )</td>
</tr>
<tr>
<td>2</td>
<td>( V_{AB} + V_0 )</td>
<td>( T_{AB} = NK_2 (V_{AB} + V_0) )</td>
</tr>
<tr>
<td>3</td>
<td>( V_{CD} + V_0 )</td>
<td>( T_{CD} = NK_2 (V_{CD} + V_0) )</td>
</tr>
<tr>
<td>4</td>
<td>( V_{EF} + V_0 )</td>
<td>( T_{EF} = NK_2 (V_{RF} + V_0) )</td>
</tr>
<tr>
<td>5</td>
<td>( V_{EA}/32 + V_0 )</td>
<td>( T_{EA} = NK_2 (V_{EA}/32 + V_0) )</td>
</tr>
</tbody>
</table>

Table A-9. Signals during the various phases of mode Brg2

The voltage across the bridge \( V_{EA} \) is divided by 32 before it is processed in the same way as the other measured voltages. The bridge imbalance \( V_{CD}/V_{EA} \) is obtained from:

\[
M = \frac{1}{32} \frac{V_{CD}}{T_{phase1} - T_{phase2}} = \frac{V_{CD}}{V_{EA}} \quad (A-3)
\]

The specifications of this mode are listed in Table A-10.
Table A-10. Specifications of the Brg2 mode

For the measurement of the signal $V_{BF}$, due to the effect of the internal connection wires of the UTI, an error of 1.2% will be caused on the result of $V_{AB}/V_{BF}$. This measured error depends on the supply current of the resistive bridge and the temperature.

Mode 14. Brg1: resistive bridge +/- 0.25% and 2 resistors

This mode is similar to mode 13. The connection is shown in Fig A-3. The difference with mode 13 is that the measurement range of the bridge imbalance is 0.25%. The bridge output voltage $V_{CD}$ is amplified 15 times before it is processed further. The voltages measured during each phase are indicated in Table A-11. The specifications are listed in Table A-12. For the measurement of the signal $V_{BF}$, due to the effect of the internal connection wires of the UTI, an error of 1.2% will be caused on the result of $V_{AB}/V_{BF}$. This measured error depends on the supply current of the resistive bridge and temperature.

Table A-11. Measured voltages during each phase of the Brg1 mode

<table>
<thead>
<tr>
<th>Phase</th>
<th>Measured voltages</th>
<th>Output periods</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>$V_{0}$</td>
<td>$T_{ab} = NK_2V_0$</td>
</tr>
<tr>
<td>2</td>
<td>$V_{ab} + V_0$</td>
<td>$T_{cd} = NK_2(V_{ab} + V_0)$</td>
</tr>
<tr>
<td>3</td>
<td>$15V_{CD} + V_0$</td>
<td>$T_{ef} = NK_2(15V_{CD} + V_0)$</td>
</tr>
<tr>
<td>4</td>
<td>$V_{BF} + V_0$</td>
<td>$T_{be} = NK_2(V_{BF} + V_0)$</td>
</tr>
<tr>
<td>5</td>
<td>$V_{EA}/32 + V_0$</td>
<td>$T_{fa} = NK_2(V_{fa}/32 + V_0)$</td>
</tr>
<tr>
<td>Parameter</td>
<td>Typical value</td>
<td></td>
</tr>
<tr>
<td>----------------------------</td>
<td>------------------------</td>
<td></td>
</tr>
<tr>
<td>$K_\Omega$</td>
<td>56 $\mu$A/V</td>
<td></td>
</tr>
<tr>
<td>$V_o$</td>
<td>0.54 V</td>
<td></td>
</tr>
<tr>
<td>Excitation $V_{EX}$</td>
<td>AC $V_{IN}$</td>
<td></td>
</tr>
<tr>
<td>Excitation current from E and F</td>
<td>20 mA</td>
<td></td>
</tr>
<tr>
<td>Bridge resistance $R_b$</td>
<td>$250 , \Omega &lt; R_b &lt; 10 , k\Omega$</td>
<td></td>
</tr>
<tr>
<td>Bridge output voltage</td>
<td>max $\pm 12.5 , mV$</td>
<td></td>
</tr>
<tr>
<td>Accuracy $V_{CD}/V_{EM}$</td>
<td>10 bits</td>
<td></td>
</tr>
<tr>
<td>Linearity $V_{AB}/V_{BF}$</td>
<td>12 bits</td>
<td></td>
</tr>
<tr>
<td>Offset $V_{CD}$</td>
<td>10 $\mu$V</td>
<td></td>
</tr>
<tr>
<td>Offset $V_{AB}$</td>
<td>10 $\mu$V</td>
<td></td>
</tr>
<tr>
<td>Resolution $V_{CD}$ (SF = 0)</td>
<td>700 nV</td>
<td></td>
</tr>
<tr>
<td>Resolution $V_{AB}$ (SF = 0)</td>
<td>7 $\mu$V</td>
<td></td>
</tr>
</tbody>
</table>

Table A-12. Specifications of the mode Brg1
Appendix 2. Theoretic calculation of differential output due to common-mode input

As is seen in Fig A-4, a differential output voltage is produced by the common-mode input voltage if non-ideality exists in practice. The detailed calculation of the relation between $V_{od}$ and $V_{ic}$ is done as follows:

$$\begin{align*}
(V_{ic} - V_2)A_1 &= V_5 \\
(V_{ic} - V_4)A_2 &= V_6 \\
\frac{A_1(V_{ic} - V_2) - V_2}{R_1} &= \frac{V_2 - V_4}{R_2} \\
\frac{V_4 - A_2(V_{ic} - V_4)}{R_3} &= \frac{V_2 - V_4}{R_2} \\
V_{ic}A_1 &= \frac{R_1}{R_2}(V_2 - V_4) + (A_1 + 1)V_2 = -\frac{R_1}{R_2}V_4 + V_2\left(\frac{R_2}{R_1} + A_1 + 1\right) \\
V_{ic}A_2 &= -\frac{R_2}{R_2}(V_2 - V_4) + V_4(A_2 + 1) = -\frac{R_1}{R_2}V_5 + V_4\left(\frac{R_2}{R_2} + A_2 + 1\right)
\end{align*}$$

$$\begin{align*}
\left\{\frac{R_3}{R_2} + A_2 + 1\right\}V_4\left(-\frac{R_1}{R_2}\right) + V_2\left(\frac{R_1}{R_2} + A_1 + 1\right)\left(\frac{R_3}{R_2} + A_2 + 1\right) &= \left(\frac{R_3}{R_2} + A_2 + 1\right)V_{ic}A_1
\end{align*}$$

$$\begin{align*}
\left(-\frac{R_1}{R_2}\right)V_4\left(\frac{R_1}{R_2} + A_2 + 1\right) - \frac{R_1}{R_2}\left(-\frac{R_1}{R_2}\right)V_2 &= \left(-\frac{R_1}{R_2}\right)V_{ic}A_2
\end{align*}$$

Subtract (2) from (1),

$$V_2 = \frac{\left(\frac{R_1}{R_2} + A_1 + 1\right)\left(\frac{R_1}{R_2} + A_2 + 1\right) - \frac{R_1}{R_2}}{\left(\frac{R_1}{R_2} + A_1 + 1\right)}V_{ic}$$
\[ V_5 = (V_{ic} - V_2) * A_i = A_i \frac{1 + A_2 + \frac{R_3}{R_2} + \frac{R_1}{R_2}}{(\frac{R_1}{R_2} + A_i + 1)(\frac{R_3}{R_2} + A_i + 1) - \frac{R_1 R_3}{R_2 R_2}} V_{ic} \]

In the same way, \( V_6 \) is calculated as follows:

\[
\begin{align*}
\left\{ \begin{array}{l}
\frac{R_3}{R_2} V_4 A_i = -\frac{R_1}{R_2} \frac{R_2}{R_2} V_4 + V_2 \frac{R_3}{R_2} (\frac{R_1}{R_2} + A_i + 1) \cdots \cdots \cdots (3) \\
(\frac{R_1}{R_2} + A_i + 1) A_2 V_{ic} = -\frac{R_3}{R_2} (\frac{R_1}{R_2} + A_i + 1)V_2 + V_4 (\frac{R_1}{R_2} + A_i + 1)(\frac{R_3}{R_2} + A_2 + 1) \cdots (4)
\end{array} \right.
\]

Add (3) and (4),

\[
V_6 = (V_{ic} - V_2) * A_2 = A_2 \frac{\frac{R_3}{R_2} + \frac{R_1}{R_2} + A_i + 1}{(\frac{R_1}{R_2} + A_i + 1)(\frac{R_3}{R_2} + A_i + 1) - \frac{R_1 + R_3}{R_2 R_2}} V_{ic}
\]

\[
V_{ad} = V_5 - V_6 = \frac{R_2}{(\frac{R_1}{R_2} + A_i + 1)(\frac{R_3}{R_2} + A_i + 1) - \frac{R_1 R_3}{R_2 R_2}} (A_i - A_2) V_{ic}
\]
Appendix 3. The links of the data sheets of the discrete components

The set-up of the board level realization of DCMVM is shown in Figure A-5. The links of the datasheets of the discrete components can be found in:

- Dual positive-edge-triggered D-type flip-flops[9]
- SPST CMOS analog switches[10]

Figure A-5. The board level realization of DCMVM
Bibliography