Design and Control of A Class of Multiphase Series-Resonant Power Converters
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PROEFSCHRIFT

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Dit proefschrift is goedgekeurd door de promotoren

Prof. ir. O.H. Bosgra en
Prof. dr. ir. A.J.A. Vandenput
Aan mijn ouders
Aan Ineke
Preface

This thesis is the final result of a research project which has spanned several years. In 1984, shortly after obtaining my MSc. degree from Delft University, an opportunity arose to continue my MSc. work in a new project. One of the aims of this project was to find out whether the then newly developed multiphase series-resonant (SR) power converter could be successfully applied to wind turbines. It was expected that the very good dynamical characteristics and the inherent high efficiency of the SR converter could be used to obtain tighter control of the wind turbine, possibly leading to lower sensitivity of the whole turbine to disturbances caused by either the wind or the electrical grid.

Financing for the project was provided by BEOP, the Bureau for Energy Research Projects of the ministry of economic affairs. The fast developments in the field caused the bureau to change names twice during the project, and now it is called NOVEM, the Dutch Organization for Energy and Environmental Affairs.

After some bureaucratic hassles, the work started in the spring of 1985 in the Laboratory for Power Electronics in Delft. The main work consisted of the design and construction of a three-phase to three-phase SR converter for 15 kW power rating. At that time, this was one of the most complex SR converters in existence. Several new control concepts needed to be formulated, simulated, and implemented in electronic hardware. After two years, we had a working prototype ready. Unfortunately during the run of the project it became clear that the complexity and component cost would be a severe disadvantage for this converter in this particular application. However, the possibilities of this equipment made it an interesting candidate for applications at the other end of the electrical energy spectrum. Electrical drives with high dynamic performance could possibly be powered with these converters, possibly leading to higher efficiency and robustness.

In an attempt to reach higher power levels with this equipment, a new project was started in 1987. As a first step, some basic problems connected to the parallel operation of multiple SR power converters were attacked. A new algorithm for the control circuit was formulated, and successfully tested near the end of 1988 on a prototype converter consisting of two paralleled modules of 6 kW rating.
Even though the work had provided good results, it could not be continued at the Delft Laboratory for Power Electronics because of personnel restrictions. I was happy to find a new and inspiring environment in the Laboratory for Measurement and Control, where an opportunity to conclude the work with this thesis was provided.

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During the long time span of this work many people have made a contribution. Although it is impossible to be complete, there are several I would like to thank in particular:

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- Sjoerd de Haan, who first acted as my Msc. supervisor, was an inspiring colleague and project leader,
- Arend Berends taught me a great deal about the handicraft of constructing physical circuits, and provided coffee to keep the motor running,
- Bert Bohlander helped more than once to solve complicated organizational problems,
- Rob Schoevaars and Kees Weijermans were ever ready to discuss technical and other matters,
- Cees den Ouden and Fred van der Zwan performed most of the construction of the parallel converter modules,
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- The staff of the Laboratory for Measurement and Control, who provided the room to discuss various technical and non technical matters, and the infrastructure to perform the simulations and text editing,
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Chapter 1

Introduction

This thesis treats two problems related to the development of series-resonant power converters. We want to know how to design such a power converter, and, after the design is finished, we would like to know how to control it. It is by no means a coincidence that both subjects are covered in the same work.

Most power electronics courses [40, 91, 80, 68] tend to treat only the operation of the power circuit of several basic types of power converters. Some kind of control system is assumed, but hardly ever made explicit. This attitude might stem from the common practice in industry, where not very long ago one team would design a power circuit, and then hand over the circuit to the “electronics” group, which would develop a control circuit.

The engineering practice mentioned before does not provide a good vehicle to perform trade-offs between the design of the power hardware and its control circuit, and consequently does not always lead to an economically optimal design for the complete converter system. As will be shown later, in the case of the multiphase series-resonant converter the power circuit and the control are very intimately connected, to the point where proper operation of the circuit without its controller is impossible. Newer power electronics courses, like [43] show an integrated approach to the design of a power circuit and its control system. We will try to follow a similar path here.

As an introduction to the subjects we like to treat in this thesis, we will start with a brief description of one type of series-resonant converter, the full-bridge configuration. This configuration will serve as a vehicle to show some of the salient features of a typical (and often used) series-resonant converter.

After this introduction, we will place the series-resonant converter in a historical perspective. Some developments in the power circuit and its control system, triggered by developments in the semiconductor market and insights in the operation of the system will be shown. The historical development of the circuit will lead us to a problem statement.

The last section of this chapter is used to show how the problem statement has been translated to the subsequent chapters.
1.1 The full-bridge series-resonant converter

In its most simple configuration, the full-bridge series-resonant (SR) converter is composed of four active semiconductor switches (e.g. thyristors), eight passive semiconductor switches (diodes), input and output filters ($C_i$ and $C_o$), and (of course) a resonant circuit consisting of an inductor ($L_{res}$) and a capacitor ($C_{res}$). The schematic has been drawn in figure 1.1.

![Schematic of the full-bridge series-resonant converter](image)

Figure 1.1: Schematic of the full-bridge series-resonant converter

Four of the diodes are connected in antiparallel to the active semiconductors, and provide a free-wheeling path for the resonant current. The other four diodes are connected in a full-wave rectifier bridge. For simplicity we will assume here that both the active semiconductors and the diodes act as ideal, i.e. lossless switches. For the same reason we will assume that no losses occur in the other circuit components, except for the load. Inspection of the circuit shows that both the input and the output voltage need to be nonnegative.

The operation of the circuit is most easily explained starting from the situation where $C_{res}$ is charged to a negative voltage $V_C$, which is sufficiently large to induce current to flow. As long as no thyristors are fired, the only way current can flow is through the diodes of the input bridge and those of the output rectifier. The current induced by a large negative voltage on $C_{res}$ will start to flow through diodes $D_2$, $D_3$, $D_5$ and $D_8$. The source current is negative, so energy is fed back to the source ($E_s$). This phase of the operation of the circuit is denoted by ‘diode current’ (for obvious reasons), ‘reverse phase’ (because of the direction of energy flow), or ‘first current segment’.

After a certain time delay, governed by the control circuit, two thyristors ($Th_1$ and $Th_4$) are fired in order to take over the current flow from $D_3$ and $D_2$ respectively. The direction of the source current changes abruptly, and
the source now delivers energy to the converter. This phase is denoted by 'thyristor current', 'forward phase', or 'second current segment'.

Analysis of the properties of the circuit in the time domain [46] or using Laplace transforms reveals that during both the first and second current segment the circuit can be described as an undamped second-order system, thus having its poles located on the imaginary axis. The associated frequency \( \omega_{\text{res}} \) is given by:

\[
\omega_{\text{res}} = \frac{1}{\sqrt{L_{\text{res}} C_{\text{res}}}}
\]  

These pole locations correspond to (co)sine wave shapes in the time domain. In particular, the current in the resonant circuit will have a sinewave shape. This implies that after a certain time this current will become zero, which allows the semiconductors, which carry this current, to turn off. This is an important feature of any series-resonant converter: turn-off of current flow is governed by the circuit, and not by the semiconductors. One implication of this feature is that normal thyristor devices (SCR's), which have no means to be turned off by themselves, can be used in this circuit.

Normally, after the succession of a 'first' and 'second' current segment the capacitor voltage is reversed in polarity. If the value of the reversed capacitor voltage is high enough, a new 'first' current segment will be initiated, this time with current flowing through diodes \( D_1, D_4, D_6 \) and \( D_7 \). As before, energy is fed back to the source in this phase. Again, a 'second' current segment can be started by firing thyristors \( Th_3 \) and \( Th_2 \), and at the end of this segment, when the current has become zero, the capacitor voltage has reversed again to a negative value. From here on the sequence of operations repeats. To illustrate the above, figure 1.2 shows a simulation of the development in time of the currents in some branches.

These time traces clearly show one of the advantageous features of the series-resonant concept: most voltages and currents in the circuit are shaped smoothly. This implies that switching losses in the semiconductors can remain quite low, and that relatively little electromagnetic radiation (EMI) will be produced. The low switching losses, related to the limitation of \( di/dt \) which is inherent to the resonant technique, allow relatively slow power semiconductors, i.e. thyristors, to be used at elevated frequencies. This property has been one of the main reasons for the development of resonant converters in the first place [77]. The relatively high frequencies which can be attained also allow the magnetic and capacitive components used in the hardware of the converter to remain small. Furthermore these high frequencies -in principle- allow the converter to react to environmental changes with a very short time delay. This implies among others, that with adequate control measures an SR converter can be made virtually short-circuit proof.
Figure 1.2: Time traces of some currents and voltages in the converter of figure 1.1

1.2 Some history

1.2.1 DC-HF

The combination of automatic turn-off and low switching losses makes the series-resonant circuit a perfect partner of the SCR thyristor, one of the first solid-state power devices to come on the market in the 1960-ies. One of the first uses of the technique was in induction heating [60]. For this application, the series-resonant converter can be an almost perfect tool to convert DC (or rectified AC) power to high frequency currents in the material to be heated. The technique allows high power levels to be reached, and in the most commonly used circuit uses only two controlled switches of the thyristor type. The resonant circuit in this application is damped by the resistive load, and the designer needs to make sure that the damping will remain low enough to allow the oscillations to sustain. In most cases the load characteristics can be assumed to vary slowly, and the amount of power transmitted to the load can be controlled through the firing frequency of the active switches.
1.2.2 DC-DC

The high internal frequencies and other advantages possible with the series-resonant technique make it a promising candidate for other types of conversion equipment as well. Replacement of the resistive AC load by a capacitively loaded rectifier circuit leads to the first step in this series: the resonant DC-DC converter. The capacitive loading of the circuit effectively decouples the value of the (resistive) load from the resonant circuit. This implies that the output current and voltage will be smooth DC quantities. Also, in this configuration the damping of the resonant circuit will no longer be provided by the load characteristics, but by parasitic resistances in the wiring and the semiconductors. Consequently, if we design the circuit to have low resistive losses, the damping will be low, irrespective of the actual loading conditions.

The low damping leads to a circuit which, compared to the AC-resistor loaded situation, is very hard to control. A slight variation in the firing frequency of the semiconductors can lead to a very large variation in load current. Moreover, the gain from firing frequency to load current depends on several badly defined and temperature sensitive parasitics of the circuit. In the limiting case of a lossless converter, the gain of the circuit tends to zero, and the output current to infinity, i.e. in this case the converter is uncontrollable through frequency modulation. Clearly a new concept for the control of this kind of converter was needed.

1.2.3 Improvements to DC-DC

The need for excess energy to be transported out of the resonant circuit was first recognized by Schwarz [77]. In a first attempt to achieve this he used additional inductive coupling between the resonant circuit and the load. Later, and we think this also reflects the changes in availability and pricing of the materials involved (i.e. the 'new' semiconductor versus the 'classic' magnets), a superior solution for the transportation of the excess energy was found using two additional semiconductors. The new circuit, applied to a half-bridge configuration, has been described in [78], which we regard as one of the 'foundation' papers concerning resonant techniques. The new method can be used under no-load and short-circuit conditions, even when no physical damping (ideal circuit) is present. We consider this to be an important property of any control technique for power conversion equipment: the concept should be independent of the non-ideal behaviour of the circuit components. This way it is guaranteed that when new (better) circuit components become available, they can be used in the old circuit without endangering the control.

1.2.4 DC-AC

Changing the output configuration (once more) from a simple passive rectifier to a full-wave thyristor bridge, and with adequate programming of
these switches, it was possible to obtain four-quadrant DC-DC operation [82]. Building a four-quadrant DC to single-phase AC output then appeared to be only a minor step. However, the high slope of the desired (AC) output voltage tends to cause tracking and stability problems with the control circuit commonly used in DC-output converters [25].

1.2.5 Multiphase

A next logical step in the application of series-resonant converters would be to use the technique for the generation of multiphase (DC or AC) waveforms. First results had been reported by Schwarz [81] regarding a three-phase AC to DC converter, where the input currents had a square-wave like appearance. A next step was taken in [29]. Here a power circuit which was topologically equivalent to the one used in [81] was used to prove that the simultaneous generation of three sinewave currents, using a single resonant circuit, was possible. A primary requisite for the technique to work was the tight control of the state of the resonant circuit. The work reported in [81] and the simulation studies in [28] had shown that the original ASDTIC control system was rather sensitive to changes of input- and/or output voltages. Especially in a multi-phase configuration, where subsequent resonant pulses are taken from different input- and output terminals, the voltage(s) applied to the resonant circuit change in a rather unpredictable manner. In [28] a method (Vcpeak control) was proposed which made it possible to precisely control the primary state variables, i.e. capacitor voltage ($V_C$) and inductor current ($I_{res}$) in such situations. The method showed that generation of multiphase AC currents, which can be regarded as a sort of ‘worst case’ situation as far as converter design is concerned, was possible [26, 29, 37].

1.2.6 Control

As will be shown later, for almost any type of SR converter a feedback control circuit is indispensable for proper (i.e. stable, see [12]) operation. In the historical sequence of converters described above, the complexity of the control circuit, and the relative importance of its design, rises fast. Only the simplest types of power circuit (for example DC-DC converters in discontinuous mode) can be operated without feedback control. At the other end of the range, for multiphase Series-Resonant AC converters, operation of a power circuit without feedback control is impossible, and as has been described in the previous section, the circuit could only be made to work after a proper control strategy had been developed. However, even for the simpler types drastic improvements in stability and speed of response are possible with a properly designed control circuit.

For example it was found out that the frequency-controlled DC-DC resonant converter, which was stable in every useful operating point, had a very bad transient behaviour. Moving from one operating point to another needed to be done with utmost care, because otherwise either very large voltages and
currents could build up in the circuit or the oscillation would die out. For another control method (ASDTIC [76]), it was found that the circuit was only stable for a limited range of the ratio of output to input voltage \((q)\) [24, 25]. Application of the Vpeak control [28] to the same power circuit showed drastic improvements in behaviour [69, 44].

1.3 Problem statement

This then is where the work reported in this thesis starts. A variety of series-resonant converter systems (DC, AC, single-phase, multiphase, and combinations thereof) has been constructed, and it is expected that a whole new class of converter systems with a common underlying principle is going to be developed.

Considering these expected developments, there is a definite need for a consistent approach to the control of these systems, especially for the as yet untackled case of multiphase to multiphase (m-m) power converters. The results reported in [29] suggest that for an m-m converter a problem of load sharing between the multiple inputs will arise. For a large total number of in- and outputs, it also becomes desirable to invent a modular approach to the control of the converter, such that the control circuit of a three-phase to three-phase converter can be based on the same architecture as, for example, a three-phase to DC converter.

In the course of this work another related problem became apparent. For a modular approach to electronic power conversion, for specific dynamic reasons, or in order to attain higher power levels than possible with one single converter, it can be desirable to be able to parallel several converter modules and perform a specific synchronization of their operation. The advantages of this particular synchronization, called 'phase staggering', are well known [53]. However, the control problem: how to synchronize multiple modules dynamically, has not been solved even for the simplest case, i.e. DC-DC conversion.

The basic problems we would like to solve in this thesis are therefore the following:

- Devise a control algorithm which takes care of the dynamic load sharing between the input phases of a multiphase to multiphase series-resonant power converter,

- Devise a hardware architecture which allows a common solution to the control of \(m\)-phase to \(n\)-phase series-resonant power converters, independent of the values of \(m\) and \(n\),

- Devise an algorithm and architecture which allows multiple power modules to perform synchronized load-sharing (phase-staggering).

If these problems can be solved, use of the series-resonant converter in the full range of applications envisioned by Schwarz [79] becomes possible.
1.4 Structure of this thesis

The first step towards creation of an actual SR converter will be to develop in chapter 2 a model of the idealized SR converter. This model, which describes the detailed behaviour of the resonant converter during one (half)cycle of the resonant wave, applies to both single- and multiphase implementations. The model of the idealized SR converter consists of a resonant circuit with infinite quality (no damping), connected via one or more switch matrices consisting of ideal switches to the external world. Some basic equations describing the operation of this idealized converter are derived.

From the idealized description two roads are taken: first, in chapter 3, a control structure is derived and used to illustrate the approach we will take in this work to the control of multiphase SR converters. The control structure chosen is based on the physics of the idealized converter. A hierarchical control structure is presented, which allows a modular and testable electronic circuit implementation of the controller.

Chapter 4 sidesteps to describe some of the simulation tools which were developed in the project. A software environment is presented which in its most detailed version allows the simulation to have a one-to-one relationship with the actual hardware. Tools have also been developed with different levels of refinement for specific needs, i.e. precise simulation of the power circuit and/or the control electronics. These tools are used to test the intended operation of the converter, and provide a first check for the sensitivity of the whole system for component deviations.

We continue with a second modelling approach which leads to a description of the detailed behaviour of the power circuit during switching phenomena, which is discussed in chapter 5. It is shown that an optimal choice for the transient-limiting components (snubbers) violates the assumptions made for the control design to some extent.

With the availability of detailed models, the simulation tools provide a means of evaluating a specific design of the hardware.

The dynamical and non-linear models which were developed in chapter 5 are used in chapter 6 for the design and simulation of the power circuit. Two prototype 3-phase AC to 3-phase AC converters are described. The first converter is a 15 kW prototype which was primarily used to test the new control concepts on a nontrivial power level. The second prototype is developed to test the new concept for phase-stagerring control, and operates at a power level of 6 kW.

The hardware of the control electronics is treated in chapter 7. The controller implementation can be used for a large variety of SR converters, for paralleled modules, and for different numbers of input and output terminals.

Chapter 8 presents some measurements which were done on the actual converters. These measurements are compared to some of the simulation results, and an attempt is made to explain the differences.

To finish, conclusions and recommendations are presented in chapter 9.
Chapter 2

Operation of the Generalized Series-Resonant Converter

In order to design and control the series-resonant (SR) converter we need to build up some understanding on how it operates, i.e. we want to develop a model. This model can then help us to:

a) Obtain a ‘feeling’ of the basic operation of the converter,

b) Design the power circuit, and dimension its components,

c) Design a control algorithm,

d) Design the necessary electronics hardware, and evaluate its performance.

The converter can be represented as a switching, and therefore time-varying, structure. Methods to deal with this kind of circuit if the switching phenomena are of a periodic nature have been developed in the literature on power electronics (see for example [43]). Unfortunately, the multiphase systems we want to treat here do not operate on a periodic basis, the main reason being a possible asynchronism between input and output grids and the resonant circuit.

Another approach would be to model the converter as a sampled-data system, the sampling instants being the instants in time where a switch action is initiated. Like before, this approach is likely to fail because, as will be shown later, the sampling intervals are not equal and dependent on process conditions.

The considerations above force us to go back to the ‘roots’ of electronics, and develop a model of the converter based on its physical operation. In order
to understand what is going on, we will first study a simplified, idealized
version of the power circuit. Later, we will add some important parasitics
and try to formulate how the model can be used for design purposes.

2.1 Building blocks for the simplified model

The simplified SR power conversion system which we are going to study first,
is composed from the following parts:

- An energy input (connected to the source(s)),
- An energy output (connected to the load(s)),
- One or more semiconductor switch matrices,
- A resonant circuit,
- A control module.

We will discuss the physical properties of these parts somewhat further in
the following sections. A more topological, or system-oriented, approach will
be given in section 2.2.

For a first approach in modelling the circuit, we will assume the circuit
to be as “ideal”, i.e. lossless, as possible. In particular we will assume that:

a) The resonant capacitor and inductor have no parallel or series resis-
tance,

b) The semiconductor switches appear as a zero resistance when closed, as
a zero conductance when open, with instantaneous switching between
these two modes,

c) The source and load have zero impedance, i.e. act as perfect voltage
sources.

Assumptions a) and b) can be considered as a 'limit' case for the design of
the power circuit: the closer we get to this case, the better the efficiency of
the converter.

2.1.1 Energy input and output

The distinction between energy input and energy output as seen from the con-
verter side is quite artificial. If the converter involved allows four-quadrant
operation, for example, the flow of energy between source and load can be
in both directions. A more general approach would specify a power con-
verter to have multiple ports. Each port would then be able to cope with an
implementation-dependent subset of combinations of voltage and current at
its terminals.
2.1.2 Source and load

Source and load will be characterized by the relationship between voltage(s) and current(s) at their respective terminals. A distinction could be made between active and passive sources and loads. However, as seen from the converter terminals, the difference between active and passive is not obvious.

As an example, an RC filter, which is a distinctly passive circuit for positive values of R and C, can for a short time span deliver power to the converter. In most cases the converter operates in a much shorter time frame than its environment, which implies that the difference between said RC circuit and an active circuit, for example a braking DC motor, could not be told from measurements at the converter terminals during only this short time frame.

A characteristic of source and load which is important to most SR converters is their impedance for high frequencies. For the operation of many types of converters it is assumed that the respective terminals are connected to either a high (current source) or a low (voltage source) impedance. In most cases the type of source and load as seen by the converter can be adjusted by means of a shunt capacitor (to approximate a voltage source) or series inductor (to approximate a current source). In the following we will assume that adequate series or shunt filters are present, if needed.

2.1.3 Switch matrices

The function of the switch matrices is to connect the source and load to the resonant circuit. They can be implemented using a large variety of (combinations of) semiconductor devices. Series-resonant converters have been reported using power diodes [77], bipolar transistors [49, 87], power MosFets [47], thyristors [81], GTO's [72], and probably more.

Resonant techniques can be used to shape the applied voltage and current profiles to the idiosyncrasies of a specific semiconductor type. GTO's, for example, can be used in a "soft turn-off" circuit, which effectively minimizes the losses caused by the otherwise troublesome tail current [16].

2.1.4 Resonant circuit

As the name suggests, the resonant circuit in a series-resonant converter consists of the series connection of an inductor and a capacitor. It will be shown later that the resonant circuit carries the highest current in the power circuit. Also, in most SR converters, the voltage across the resonant circuit will be at least as high as the highest voltage difference between any pair of (input and/or output) terminals. Therefore these components often suffer the heaviest load (in terms of VA product) of the converter.
## 2.2 Topology

The simplified series-resonant converter can be schematically depicted as follows:

![Figure 2.1: Composition of an SR power converter](image)

In figure 2.1 both source and load are connected to the resonant circuit by means of a switch matrix, SW1 resp. SW2. Although source and load are depicted as one-ports here, they can just as well be implemented as multiport configurations. A three-phase power grid is an example of such a situation.

The particular implementation of the switch matrices SW1 and SW2 and the type of source and load leads to a classification of series-resonant power converters. In this work we will restrict ourselves to sources and loads with a voltage-source (capacitive) character. Although at first sight this choice might be considered a very restrictive one, it covers the majority of present-day applications of series-resonant converters, and quite a few new topologies [21] as well. Furthermore it will be made plausible that the control methods which have been found for this class can, with trivial or minor modifications, also be used for some other classes of series-resonant converters.

The switch matrices serve to connect two of the in- or output terminals to two nodes of the resonant circuit. From a system theoretical point of view, the switch matrices can impose constraints on state variables of the subsystems found on both sides of the matrix. This will be the case if the switch actions induce either a series connection of inductors and/or current sources or a parallel connection of capacitors and/or voltage sources. In such a case, the result of the interconnection is a composite system with singular properties [96], i.e. the dimension of the state space of the composite system is less then the sum of the dimensions of the state spaces of the subsystems. The best known situations which result in a singular system are the following:

a) Short circuit of either the input or output terminals. This can be interpreted as an attempt to parallel a zero voltage source (closed switch) with a (large) capacitance representing load or source. Clearly this is a situation which normally needs to be avoided.

b) A switching action (closing) could lead to a parallel connection of the resonant capacitor to either a pair of input- or output terminals. In this case we need to be sure that at the moment of interconnection the voltages on the respective capacitors are exactly equal, i.e. the voltage across the switch needs to be exactly zero at the moment of switching, otherwise serious switching losses (impulsive behaviour) might occur.
c) Dually to the situation described above, an opening of a switch could lead to a series connection of two inductors. Here we need to be sure that the current through the switch is exactly zero at the moment of opening.

We like to remark here that even if we are able to make the voltage resp. current difference at the instant of on, resp. off switching exactly zero, the switches can be subject to step-like changes in the covariable. An example can be given with the circuit of fig. 2.2:

\[ \text{Figure 2.2: Example of stepwise current load on a diode switch in a rectifier} \]
\[ \text{a: (left) Circuit} \]
\[ \text{b: (right) Waveforms of voltages and currents in the circuit} \]

The half wave rectifier in fig. 2.2 is loaded capacitively. The diode, which for simplicity is assumed to have no forward voltage drop, turns on when the input voltage \( U_{in} \) and the voltage on the capacitor are equal. At this moment, the current \( I_d \) carried by the diode changes in a stepwise fashion. In a practical setup this leads to very high values for \( di/dt \) and consequently to large turn on losses. For this particular setup the switching stress can be lowered by connecting an inductor in series with the diode.

From the cases b) and c) and the example it can be concluded that if we want to reduce switching losses, the two subsystems at both sides of the switch matrix need to be of a different 'nature'.

We like to state this conclusion as a

**Rule 1** To minimize switching losses a semiconductor switch should be connected between sections of the power network with capacitive and inductive behaviour, respectively.

We can apply Rule 1 to the switch matrices SW1 and SW2, which connect an outside world with voltage source (i.e. capacitive) character to the resonant circuit. Connection of the switch matrices directly to the resonant capacitor \( C_{res} \) evidently violates rule 1. As in the rectifier example given before, in such a setup the current through the semiconductor switches would show
steplike transients, which could lead to high stress \( (di/dt) \) on the power semiconductors and losses. Therefore we see that in the configuration which is commonly denoted as a parallel resonant inverter, where the output rectifier is connected across the resonant capacitor, usually an inductor is connected directly after this rectifier bridge (see for example [17]).

We may conclude that at least one terminal of the individual switch matrices needs to be connected in series with the resonant inductor. Although this is a severe restriction, still a multitude of configurations is possible. The possible configurations can be divided into two classes:

- configurations with two switch matrices, separated from each other by the resonant circuit,

- configurations with only one (possibly large) switch matrix, which connects to both sides of the resonant circuit.

These two configurations are shown in fig. 2.3 a) and b) respectively.

![Diagram](image)

**Figure 2.3:** Configurations of switch matrices and resonant circuit  
a: (upper) Two switch matrices separated by the resonant circuit (two resonant circuits have been drawn for symmetry)  
b: (lower) One switch matrix common to both inputs and outputs

The commonly used types of SR converters are mostly composed as in fig. 2.3a. For example, the full bridge configuration which has been introduced in chapter 1 and the often used half bridge SR converter are of this type. One of the reasons for the popularity of this specific configuration is that in some (important) cases an HF transformer can be used to obtain galvanic isolation and/or voltage scaling. However, already in the DC-DC converter the design and operation of this transformer is far from trivial, and the inclusion of such
a transformer can lead to stability problems (see for example [41, 42, 49, 54, 13]).

For the single phase converter, the magnetizing voltage applied to the transformer contains components depending on the difference between the voltages across the resonant circuit on two subsequent resonant halfcycles. This implies that when the slope (frequency content) of some input and/or output voltage is too high the transformer can be easily driven into saturation.

For a converter with multiphase input and/or output, the voltage applied to the resonant circuit during subsequent halfcycles is composed of fractions of different input and output voltages. Here a transformer can not be used without additional control to limit the excursions of the main flux [98].

If no transformer is used in the configuration of fig. 2.3.a, the output voltage will exhibit steep common-mode voltage transients with respect to the input. This implies that if a load is to be powered at some distance, the cables will emit appreciable Radio-Frequency (RF) power. This phenomenon is absent in the implementation of fig. 2.3.b, where all terminals can be (and normally are) shorted to a common neutral with filter capacitors.

The observations above will, depending on the particular circumstances, lead to a choice for a converter with one or two switch matrices. Despite the differences regarding the applicability of transformers and the RF noise, both types of converters have many characteristics in common. Therefore we will first develop the part of the theory regarding the operation of the multiphase series-resonant converter which is common to both types.

2.3 Internal operation of the simplified model

In this section we will start to analyze the properties of the simplified model of the SR converter. As a first step we will show that the model of the converter between two successive switching instants is independent of the particular configuration. The differential equations which describe the operation of the simplified model lead to a solution which can be displayed as a circle in a plane spanned by the two state variables $V_C$ and $I_{res}$.

Considerations concerning the energy stored in the resonant circuit lead to an operation mode which bounds this energy. For this operation mode one additional switching action is needed between two consecutive zero crossings of the resonant current. The values of the state variables at the moment of switchover are computed.

2.3.1 Matrix notation

With the assumptions made in section 2.1, the series-resonant power converter reduces to a resonant circuit which, by means of switches, can be connected to one or more external voltage sources. As seen from the terminals of the resonant circuit, every valid combination of switch positions shows up as either an open circuit or an ideal voltage. In the latter case, the value
of this voltage source is composed of the individual external sources $V_{ext}$ as follows:

$$V_{LC} = \sum a_i \cdot V_{ext}$$

(2.1)

with $a_i \in [-1, 0, 1]$, depending on the switch positions.

The difference between the two types of SR converter of fig. 2.3 shows in the translation of switch positions to the $a_i$ of equation 2.1. In order to obtain a convenient notation, we will first introduce the switch-position matrix $T_{sw}$. This $(2 \times n)$ matrix contains a “1” where the corresponding switch is closed, and zeros elsewhere. Figure 2.4 shows some examples:

$$T_{sw} = \begin{pmatrix} 1 & 0 & 0 \\ 0 & 0 & 1 \end{pmatrix} \quad \begin{pmatrix} 0 & 1 & 0 & 0 \\ 0 & 1 & 0 & 0 \end{pmatrix} \quad \begin{pmatrix} 1 & 0 \\ 0 & 1 \end{pmatrix}$$

Figure 2.4: Examples of switch positions and $T_{sw}$ contents

Note that, in order to avoid short-circuit, only one nonzero entry per row is allowed. For brevity, we also like to introduce the matrix $D$, which is defined as:

$$D = \begin{pmatrix} 1 & -1 \end{pmatrix}$$

(2.2)

and the column vectors $\mathbf{V}_{in}$ and $\mathbf{V}_{out}$, which contain the actual input- and output voltages, respectively. Using this notation, equation 2.1 can be rewritten as

$$V_{LC} = DT_{swi} \mathbf{V}_{in} - DT_{swr} \mathbf{V}_{out}$$

(2.3)

for the converter with two switch matrices, and as

$$V_{LC} = DT_{sw} \mathbf{V}_{in}$$

(2.4)

for the converter with one switch matrix. Effectively, as long as the switch positions do not change, the resonant circuit "sees" a copy of one or more of the voltages which are applied externally.

### 2.3.2 Differential equations

For the simplified analysis here we will assume the voltage $V_{LC}$ applied to the resonant circuit to be constant between successive switch operations. With
this assumption, the circuit between two successive switch operations reduces to a DC source, with a value given by equations 2.3 or 2.4, connected to the resonant circuit. The resulting circuit is shown in figure 2.5, together with some of the notational conventions which we will use in this chapter.

![LC circuit with $V_{LC}$](image)

Figure 2.5: LC circuit with $V_{LC}$

The equations which describe the evolution in time of this circuit are the following:

\[
L_{res} \frac{d}{dt} I_{res} = V_{LC} - V_C \tag{2.5}
\]

\[
C_{res} \frac{d}{dt} V_C = I_{res} \tag{2.6}
\]

From these equations the network behaviour can be computed, for example by using Laplace transforms. The time responses of the resonant current and the capacitor voltage can be written as follows:

\[
I_{res}(t) = Y_{res}(V_{LC} - V_{C0}) \sin(\omega_{res}t) + I_{res0} \cos(\omega_{res}t) \tag{2.7}
\]

and

\[
V_C(t) = V_{C0} + (V_{LC} - V_{C0}) (1 - \cos(\omega_{res}t)) + Z_{res} I_{res0} \sin(\omega_{res}t) \tag{2.8}
\]

where $Z_{res} = 1/Y_{res} = \sqrt{L_{res}/C_{res}}$ signifies the characteristic impedance of the resonant circuit, $\omega_{res} = 1/\sqrt{L_{res}C_{res}}$ is the undamped resonant angular frequency of the circuit and $V_{C0}$ and $I_{res0}$ are the values of the capacitor voltage and current at $t = 0$, respectively.

### 2.3.3 State plane description

The waveforms of both the capacitor voltage $V_C$ and the resonant current $I_{res}$ are (co)sinusoidal. An interesting and illustrative way of depicting these signals together is found in [69]. The trajectories of both signals can be shown in the state plane, i.e. a plane with cartesian coordinates with the first state variable ($V_C$) along the horizontal axis, and the second ($I_{res}$) along
the vertical axis. With proper scaling the combined trajectory shows as a circle, with centre at $(V_{LC}, 0)$ and radius $\sqrt{(V_{LC} - V_C)^2 + (Z_{res}I_{res})^2}$. An example is shown in figure 2.6.

![Diagram of trajectory](attachment:trajectory.png)

**Figure 2.6:** Relation between $V_C$ and $I_{res}$ depicted in the state plane

With the sign conventions of figure 2.5 it will be obvious that the trajectory of figure 2.6 will be followed in a clockwise direction. In a physical configuration only a part of the circle will be covered, because of the initial values of the state variables and the limitations in polarity of current and/or voltage of the electronic power switches.

### 2.3.4 Energy considerations

If we consider the operation of the circuit between two successive current zero crossings, the energy $E_c$ absorbed by the resonant circuit can be computed:

$$E_c = 2C_{res}V_{LC}(V_{LC} - V_{C0})$$

(2.9)

Clearly, for all but the most trivial values of $V_{LC}$ and $V_{C0}$ the energy content of the resonant circuit will change. If we were to operate the circuit on a repetitive basis, for example by using a $V_{LC}$ with the shape of a square wave, the energy in the circuit, and the values of $V_{C0}$ and $I_{res}$, could become infinitely large. Therefore normally a mechanism is implemented which will remove the excess energy from the resonant circuit. The method we will use for this purpose consists of switching $V_{LC}$ in such a way that the net energy absorbed by the resonant circuit will be zero, i.e. the energy content of the resonant circuit at two successive current zero crossings will be the same. In formula:

$$\frac{1}{2}C_{res}V_{C0}^2 = \frac{1}{2}C_{res}V_{C2}^2 \Rightarrow$$

$$V_{C2} = \pm V_{C0}$$

(2.10)
with $V_{C_0}$ the initial value of the voltage on the resonant capacitor, $V_{C_2}$ its final value, and $C_{res}$ the value of the resonant capacitor. For any nontrivial situation, only the minus sign in equation 2.10 makes sense, and the capacitor voltage will be exactly inverted after every resonant halfcycle.

The inversion of $V_C$ after every half cycle implies that cyclical operation of the converter is possible, because the initial conditions for the next current pulse are (apart from the minus sign) exactly equal to those of the present current pulse.

Due to the switching of $V_{LC}$ we now need to distinguish two time intervals. We will assume here that $V_{LC}$ will be switched only once, at time $t = t_1$. The two time intervals will be denoted by first current segment ($t \in [t_0, t_1]$) and second current segment ($t \in [t_1, t_2]$) respectively.

The following derivation applies:

\[
0 = E_c = \int_{t_0}^{t_2} V_{LC} I_{res} dt
= \int_{t_0}^{t_1} V_{LC1} I_{res} dt + \int_{t_1}^{t_2} V_{LC2} I_{res} dt
= \int_{t_0}^{t_1} V_{LC1} I_{res} dt + \int_{t_1}^{t_2} V_{LC2} I_{res} dt
\]

(2.11)

where $V_{LC1}$ and $V_{LC2}$ denote the voltages applied to the resonant circuit during the first and second current segments, respectively. Because equation 2.12 applies to the operation of the circuit during the interval between two consecutive current zero crossings, the sign of $I_{res}$ will not change. With this in mind, inspection of equation 2.12 reveals that the sign of $V_{LC1}$ must be opposite to the sign of $V_{LC2}$, i.e.

\[
V_{LC1} V_{LC2} < 0
\]

(2.13)

If we now return to the state plane description of the behaviour of the resonant circuit, the operation of the circuit can be depicted as in figure 2.7.

The trajectory in fig. 2.7a is composed of two circle segments. The first segment is centred around $(V_{LC1}, 0)$ and has radius $|V_{LC1} - V_{C0}|$, the second segment is centred around $(V_{LC2}, 0)$ and has radius $|V_{LC2} - V_{C2}|$.

As has been said, with this operation mode the voltage $V_C$ on the resonant capacitor is precisely inverted after every current pulse. The inversion itself can be taken care of by a proper selection of switches. Therefore, by induction this implies that every subsequent current pulse will be subject to the same value of the initial capacitor voltage $V_{C0}$ as the first one. In the following section we will derive under which conditions of the terminal voltages this - so far assumed - exact inversion of $V_C$ is possible.
2.3.5 Values of state variables at switchover

The value of $V_C$ where the transition of the trajectory from the first to the second circle takes place $(V_{C1})$ can be computed starting with equation 2.12:

\[
0 = V_{LC1} \int_{t_0}^{t_1} I_{res} dt + V_{LC2} \int_{t_1}^{t_2} I_{res} dt \\
= V_{LC1} C_{res} (V_{C1} - V_{C0}) + V_{LC2} C_{res} (V_{C2} - V_{C1}) 
\]

(2.14)

Rearranging equation 2.14 and dividing by $C_{res}$ we obtain:

\[
V_{C1} = \frac{V_{LC1} V_{C0} - V_{LC2} V_{C2}}{V_{LC1} - V_{LC2}} 
\]

(2.15)

which can be further simplified by substitution of $V_{C2} = -V_{C0}$ (equation 2.10) to:

\[
V_{C1} = V_{C2} \frac{V_{LC1} + V_{LC2}}{V_{LC2} - V_{LC1}} 
\]

(2.16)

Inspection of equation 2.16 shows that, if the signs of $V_{LC1}$ and $V_{LC2}$ are opposite, $V_{C1}$ will lie between $-V_{C2} = V_{C0}$ and $V_{C2}$, as we would expect.

In order to obtain a solution for the value of the resonant current at $t = t_1$ we start with the equation which describes the relation between $V_C$ and $I_{res}$ for the first current segment:

\[
(V_C - V_{LC1})^2 + (Z_{res} I_{res})^2 = (V_{C0} - V_{LC1})^2 
\]

(2.17)

Substitution of the value of $V_C$ at $t = t_1$, i.e. equation 2.16 yields:

\[
(V_{C2} V_{LC1} + V_{LC2})^2 + (Z_{res} I_{res})^2 = (V_{C0} - V_{LC1})^2 
\]

(2.18)

\[
(Z_{res} I_{res})^2 = (V_{C0} - V_{LC1})^2 - (V_{C2} V_{LC1} + V_{LC2})^2 \frac{V_{LC1} + V_{LC2}}{V_{LC2} - V_{LC1}} 
\]

(2.19)
which, after some manipulation, reduces to:

\[(Z_{\text{res}}I_{\text{res}})^2 = -4V_{LC1}V_{LC2}V_C \frac{(V_C + V_{LC2} - V_{LC1})}{(V_{LC2} - V_{LC1})^2}\] (2.20)

which is the equation for the value of \(I_{\text{res}}\) we were looking for.

If a solution for \(Z_{\text{res}}I_{\text{res}}\) exists, the factors at the right-hand side of equation 2.20 must yield a positive value. The first part, \(-4V_{LC1}V_{LC2}\), is indeed positive by equation 2.13. The numerator, being a square, is also positive, thus we obtain

\[V_C(V_C + V_{LC2} - V_{LC1}) > 0\] (2.21)

which can be divided in two cases:

\[V_C > 0 \quad \land \quad V_C > (V_{LC1} - V_{LC2})\] (2.22)
\[V_C < 0 \quad \land \quad -V_C > (V_{LC2} - V_{LC1})\] (2.23)

Equations 2.22 and 2.23 apply to the operation of the circuit with negative and positive resonant current \((I_{\text{res}})\) respectively. For brevity, we will only develop the case of positive current flow further. Combining equation 2.23 with equation 2.13 we obtain a further subdivision:

\[V_C < 0 \quad \land \quad V_{LC1} > 0 \land V_{LC2} < 0 \land V_C < 0\] (2.24)
\[V_C < 0 \quad \land \quad V_{LC1} < 0 \land V_{LC2} > 0 \land V_C < (V_{LC1} - V_{LC2})\] (2.25)

Here a large difference shows up: in the case of equation 2.24 \(V_C\) can have any value, as long as it is negative. In the case of equation 2.25 \(V_C\) has an upper limit. The corresponding trajectories in the state plane are shown in figure 2.8.

![Figure 2.8: State plane representations for super- and subsynchronous conversion](image)

**Figure 2.8:** State plane representations for super- and subsynchronous conversion

a: (left) For equation 2.24
b: (right) For equation 2.25

Geometrically the rightmost part of equation 2.25 can be interpreted as the need for the two circles in fig. 2.8.b to intersect. No such restriction is present in fig. 2.8.a: an intersection of the two circles is always possible here.
2.3.6 Interpretation

The circuit operation as described by equations 2.24 and 2.25 respectively not only shows up differently in the equations. The circuits which can be used to generate the corresponding waveforms are subject to rather different restrictions as well. A first observation regards the range of inverter frequencies connected to each operating mode. Inspection of the geometries of fig. 2.8 reveals that the total pulse time (proportional to the sum of the angles of the circle segments [69]) for the situation in fig. 2.8.a will always be lower than \( \pi/\omega_{\text{res}} \), which implies that the inverter frequency for this circuit will always be higher than the resonant frequency (supersynchronous). Similarly, the inverter frequency for the circuit of fig. 2.8.b will always lie below the resonant frequency (subsynchronous).

Another difference between the supersynchronous and subsynchronous converter exists regarding the semiconductor switches which can be used. For brevity we will only consider the case of positive resonant current. In the supersynchronous converter the voltage applied to the circuit is lowered at the switching moment \( (i_1) \). This implies that thyristor-type devices cannot be used for this converter: the thyristor which would be fired to start the second current segment would never take over the current flow. For the same situation in a subsynchronous converter the voltage applied to the resonant circuit during the second current segment is higher than during the first current segment, which means that thyristors can be turned off gracefully. This "commutation requirement" will later be used to determine the firing sequence of the individual semiconductors.

Close inspection of the circuits used in super- and subsynchronous series-resonant converters shows that the (idealized) switch types needed to build these converters are each other's dual. For the subsynchronous converter an element with the characteristics of an (ideal) thyristor is needed, whereas the switches for the supersynchronous converter need the characteristics of an (ideal) dual thyristor, i.e. an element which can turn off any time, but turn on only at zero voltage (see [17]). The duality between the two converter types goes further than this: where in the subsynchronous converter commutation of the current from the semiconductor which switches off to the one switching on is the primary source of switching losses, in the supersynchronous converter the voltage commutation is more troublesome. The snubber circuits commonly used in the two converter types underline this observation: for the supersynchronous converter a virtually lossless snubber can be built with capacitors only (see [88]), for the subsynchronous converter (commutation) inductances are used (see [32]).

2.3.7 Voltage and current limits

In this section we will derive the constraints which are applicable to the voltages and currents applied to the resonant circuit. We will only perform the derivation for the case of the subsynchronous converter, which can be
constructed with normal thyristors (SCR's) as switching devices. However, the derivation of the supersynchronous converter follows a completely parallel path.

Voltage limits

For the operation mode where the capacitor voltage is exactly inverted after every halfcycle, we like to recapitulate the restrictions on the terminal and capacitor voltages for positive resonant current (equations 2.10, 2.13 and 2.25):

\begin{align}
V_{C0} &< 0 \quad \text{(2.26)} \\
V_{C2} &= -V_{C0} \quad \text{(2.27)} \\
V_{LC1} &< 0 \quad \text{(2.28)} \\
V_{LC2} &> 0 \quad \text{(2.29)} \\
V_{C0} &< (V_{LC1} - V_{LC2}) \quad \text{(2.30)}
\end{align}

For some value for the peak capacitor voltage $V_{C2}$, the restrictions in equations 2.26...2.30 confine the allowed values of $V_{LC1}$ and $V_{LC2}$. The allowed range for these two voltages is sketched in fig. 2.9.

![Diagram showing the range of allowed terminal voltages](image)

**Figure 2.9**: The range of allowed terminal voltages (shaded)

If in equation 2.30 we substitute the most negative differential terminal voltage for $V_{LC1}$, and the most positive differential terminal voltage for $V_{LC2}$, we obtain an upper bound on $V_{C0}$, i.e. a lower limit on the peak capacitor voltage. As this bound is valid for a worst-case combination of terminal voltages, it is valid for *any* combination of terminal voltages which is subject to equations 2.28 and 2.29.

The lower bound on $V_{C2}$ thus derived is conservative in the sense that not every possible combination of $V_{LC1}$ and $V_{LC2}$ will actually be used. Which
terminal voltages will be used for the operation of the converter is determined by a selection algorithm. The algorithm we will use, which will be presented in chapter 3, allows for a much lower value of $V_{C2}$ than the worst-case value discussed before. Generally, a low value for $V_{C2}$ is advantageous with respect to the voltage stress on the semiconductors.

Current limits

During current flow, the active input- and output terminals of the converter are connected in series with the resonant circuit. Therefore, the maximum current flowing in a particular terminal can never exceed the maximum current in the resonant circuit. The average current flowing through the resonant circuit is given by the quotient of the charge $Q$ and the time:

$$I_{av} = \frac{Q}{T_{inv}} \quad (2.31)$$

$$= f_{inv} C_{res} \Delta V_{C} \quad (2.32)$$

$$= 2f_{inv} C_{res} V_{C2} \quad (2.33)$$

If we assume $V_{C2}$ to be fixed at a constant value, the maximum current in the resonant circuit appears at the maximum inverter frequency $f_{inv}$. This frequency is limited by the properties of the resonant circuit and the minimum allowable turn-off time ($t_q$) of the thyristors. We can conclude that the average current in the resonant circuit, and therefore in any input- or output terminal of the converter, is limited. Therefore the converter behaves as a current source, with a current limit which is independent of the actual terminal voltage. As the range of allowable terminal voltages includes zero, we can claim that the converter is (statically!) short-circuit proof.

2.4 Extensions to the simplified model

The simplified model which has been developed in the preceding sections does not fully cover the physical reality. The main simplifications in the model are:

- It only applies to voltage-in, voltage-out converters,
- it is only valid for lossless converters,
- the effects of snubber- and commutation networks have been neglected,
- the switching phenomena in the semiconductors are not accounted for,
- no voltage ripple on the terminals is incorporated.

Some of these shortcomings of the simplified model can be easily accounted for. As has been shown in [69] the model can be easily adapted to
the case of current source or load. The state plane trajectory for this case is still built up from circle segments, but the centre of the circles no longer lies on the ordinate.

Up to some extent losses can also be accounted for. In most relevant cases, conduction losses in the resonant circuit and the semiconductor devices can be modeled as the series connection of an effective voltage source and an effective resistance [45]. The voltage source can be thought incorporated in source and/or load, leading to a slight shift of the centerpoints of the circles in the state plane.

The effective resistance gives rise to damping of the resonant phenomena, therefore the state plane trajectory will for this case be built up from spiral segments. Clearly the equations for this case will be much harder to handle mathematically than for the undamped situation.

The influence of the snubber networks and the switching behaviour of the semiconductors will be studied in chapter 5.

Commutation phenomena lead to a change of the shape of the state plane trajectories. The equations which describe the commutation will be discussed in appendix A. The numerical values of the deviations caused by the commutation will be discussed in chapter 6.

Incorporation of ripple on the terminal voltages will lead to a more complex resonant circuit, of a class which is both voltage- and current loaded. A formal analysis of the phenomena in such a circuit appears to be feasible (see [69]). However, for simplicity we will neglect the influence of voltage ripple in the following.

2.5 Discussion

In this chapter some general considerations regarding the structure of series-resonant power converters have been treated. Observations with respect to switching losses in the power semiconductors have led to two major topological classes of converters. For both classes some key equations, describing the behaviour of the converter when two-segment current waveforms are used, have been derived. A further distinction has been made with regard to operation modes. Two dual classes of operation exist, one of which can be used with normal thyristors (SCR's) as switching devices, whereas the other one needs power semiconductors which can be switched off actively.

Comparison of the two converter topologies

In the foregoing sections some properties of SR converters with one or two switch matrices have been discussed. Both converter topologies allow the construction of multiphase to multiphase systems. However, the two basic topologies differ with respect to some important characteristics:

- The two-matrix converter produces substantial high-frequency common-mode voltages, which in combination with appreciable cable lengths can
become the source of severe electromagnetic pollution,

- the implementation of voltage measurements in the two-matrix converter will be much harder because of these common-mode voltages,

- in the two-matrix converter topology the resonant current flows through four semiconductors (two in the input matrix and two in the output matrix) in series, whereas in the other type only two semiconductors in series conduct the current flow. Therefore it might be expected that the conduction losses, and probably the total losses as well, in the one-matrix topology can be substantially lower,

- in the one-matrix topology inclusion of a transformer, for galvanic isolation and/or voltage scaling, is not possible. Inclusion of a high-frequency transformer in the two-matrix type in principle is straightforward. However, the question how to keep the main flux in this transformer out of saturation has not yet been solved fundamentally,

- as will be shown in section 3.5, the maximum voltage on the resonant capacitor can be much lower for the one-matrix topology compared to the two-matrix case, which implies that

- the semiconductors in the two-matrix topology are subject to larger voltages than in the single-matrix converter (see also [51], which discusses a similar configuration). This advantage is (of course) countered by a higher average current. However, for the same VA product, semiconductors with larger current capacities appear to be easier to obtain than devices with high voltage ratings.

Restriction to the single matrix topology and to thyristors

The foregoing arguments and the power levels we want to achieve have led us to restrict our treatment as follows:

- The converter configuration which we will discuss in the following is the one which uses only one switch matrix, and

- we will only use thyristors as switching devices.

A schematic of this topology has been given in figure 2.10.

The topology is built up from a number of identical branches containing bidirectional switches, all of which are connected to a common series-resonant circuit consisting of $C_{res}$ and $L_{res}$.

The terminals at the left of figure 2.10, which serve as connections to the outside world, can be used as input or output of the converter, depending on the application. Which role a particular terminal plays is decided by the control circuit; the branches in the power circuit are identical. The following section supplies some examples of applications for different numbers of terminals.
Figure 2.10: General simplified schematic of the power circuit of the one-matrix SR converter with thyristors

The drawing in figure 2.10 loosely defines a class of multiphase series-resonant converters, whence the title of this thesis. Summarizing the considerations which have been presented in this chapter, the elements in this class of converters have the following common properties:

- They contain one resonant circuit,
- Both sides of the resonant circuit are connected to one switch matrix,
- The switch matrix is implemented with antiparallel pairs of thyristors,
- The switch matrix is symmetric with respect to the different connections to the outside world,
- Source and load both present a low impedance to the converter,
- The resonant circuit is operated subsynchronously, i.e. the frequency of the resonant current lies below the resonant frequency.

Even though we will only treat one basic converter topology in detail, we like to note that the methods developed for this topology can be readily applied to the two-matrix converter type as well. Simulations [30] have shown that both the one- and two-matrix converter types can deliver a similar performance. Apart from the matters mentioned above, the main difference for an implementation lies in the more complicated ‘bookkeeping’, caused by the presence of two switch matrices instead of one.

Applications

The total number of terminals (input and output) for the one-matrix topology can range from three to infinity. Table 2.1 (definitely incomplete) shows some applications for several numbers of terminals.

Examples of the basic configuration of the power circuit for these applications have been given in figure 2.11.
Table 2.1: Applications of one-matrix SR converters for a number of terminals

<table>
<thead>
<tr>
<th>number of terminals</th>
<th>applications</th>
</tr>
</thead>
</table>
| 3                   | One-phase DC-DC converter (see [92])  
Three-phase reactive power controller (see [63]) |
| 4                   | idem with starpoint connection  
DC-DC (+/-) to DC/DC (+/-) converter |
| 5                   | Three-phase to DC (+/-) converter or vice-versa |
| 6                   | Three-phase to three-phase converter |
| 7                   | idem with neutral connection |
| 9                   | Three-phase in, three-phase out uninterruptible power supply with +/- 0 battery connection |

Figure 2.11: Four examples of configurations of series-resonant power converters.

  a) (Upper left): Single phase DC to DC or AC converter  
b) (Lower left): Three-phase reactive current compensator  
c) (Upper right): Three-phase to three-phase DC or AC to DC or AC converter  
d) (Lower right): Three-phase to three-phase uninterruptible power supply with centre-tapped energy storage

The converters which have been constructed in the course of this work all have a three-phase to three-phase setup. However, the control electronics has been set up in such a way that lower numbers of terminals can be used as well.
Chapter 3

Control Algorithms

Resonant power converters are used to transform electrical power supplied in one form (AC, DC, single- or multiphase) to another. In many cases, the shape(s) of the waveform(s) to be generated is (are) supplied as (a) reference signal(s), and we like to view the converter system as a sort of (multiphase) power amplifier. The main objectives which we like to achieve with the converter system (=power part + control) have been formulated in section 3.1. As the transfer functions from control inputs to outputs are badly known and supposedly nonlinear, feedback control is generally used in order to minimize deviations between the reference signals and actual outputs.

Series-resonant converters have for a long time been characterized as being hard to control in a feedback configuration. For a DC-DC converter, the gain from a often-used control input (the delay angle $\psi_r$) to output (the average rectified resonant current) shows enormous variations over the useful operating range [21, 28]. Techniques to stabilize DC-DC converters have been developed [25, 47], but these tend to slow the response to input or load variations over a considerable part of the operating range [70]. This needs not be a problem for DC-DC converters, where both input and output can be buffered with relatively large capacitors. However, the application of the circuit has spread out towards four-quadrant [82], AC [50] and multiphase [30, 85, 32, 31] systems.

In these converters, input and output voltages as seen by the resonant circuit can vary considerably over the time span of a few resonant cycles due to the AC character of the waveforms, the dynamical switching between multiple phases, or both. The complexity of these converters makes it rather hard to apply classical control structures, as will be shown in section 3.2.

The control of series-resonant converters made a major step forward with the introduction of Vpeak- [26] or Optimal Trajectory [70] Control. With these techniques the internal state of the converter is measured and used to enhance the stability and controllability of the system. The technique will be introduced in section 3.3.
Once the converter is stabilized using $V_{\text{peak}}$ control, it can be viewed as a process which transfers discrete amounts of electrical charge. The amount and the polarity of the charge moved to a particular terminal per unit of time correspond to an average current in this terminal. Section 3.4 discusses how this current can be applied for either current- or voltage control.

As the input- and output terminals of the converter need to be serviced by the same resonant circuit, a mechanism is needed which schedules the connection of terminals to the resonant circuit. This mechanism will be discussed in section 3.5.

The actual current flow in the terminals of the converter is constrained by several physical conservation laws. The nature of the constraints and their consequences are shown in section 3.6.

The topology of the power circuit used in this work allows multiple power modules to be connected in parallel, and dynamically share a load. The principle of this technique and a possible control algorithm are dealt with in section 3.7.

The control structure derived here is based on a simplified model of the power converter. Therefore it needs to be checked whether the controller is robust with regard to modelling errors. The major differences between the simplified model and the actual converter, together with implications for the quality of the control, are discussed in section 3.8.

### 3.1 Objective

The control system should govern the power converter in such a manner that the following objectives can be reached:

- Safe operation of the converter, i.e. provide a predefined upper bound on the component stresses,

- Optimal generation of input and output signals, according to some error criterion.

We will deal with these two objectives in the two following sections.

#### 3.1.1 Safe operation

We will only consider the safety of the thyristors here, as they are the most vulnerable components of a converter system. For thyristors, the following causes for failure have been reported [22]:

- overvoltage (leading to badly controlled turn-on, high dissipation, or both)

- overcurrent (leading to hot spots)

- too short recovery time ($t_{q}$) before application of forward voltage (possibly leading to unwanted turn-on)
A straightforward control structure

- transient overvoltage \((dv/dt, \text{leading to unwanted turn-on})\)
- transient overcurrent \((di/dt, \text{hot spots})\)
- too low gate drive

From these six causes only the first three can be easily influenced by the control. The transient phenomena can be accommodated to some extent with snubbers. The design of these circuits will be discussed in chapter 5. The gate drive depends on the design of the gate pulse amplifiers, and we will assume that these have been correctly matched to the thyristors.

3.1.2 Optimal generation of input and output signals

If we want the converter to behave as a (possibly multiphase) power amplifier, this implies that the differences between the reference signals and the corresponding control outputs need to be small. For the case which we will develop later, where the converter outputs are voltage-controlled and the inputs are current-controlled, the situation at the outputs is obvious, because we assume the corresponding reference signals to be supplied externally. For the input currents, however, the situation is more complicated. It will be argued in section 3.6 that the three references for the input currents can not be chosen freely. For a three-phase to three-phase converter effectively one degree of freedom remains. We will use this freedom to produce input currents with a predictable power factor.

3.2 A straightforward control structure

The electrical schematic of the power circuit of a three-phase to three-phase single-matrix converter has been drawn in figure 3.1. We will assume that the impedance of the source and load circuits has been made sufficiently low using capacitive filters (see section 2.1.2).

![Power circuit of a three-phase to three-phase SR converter (for simplicity snubbers are left out)](image)

Figure 3.1: Power circuit of a three-phase to three-phase SR converter (for simplicity snubbers are left out)
It is worthwhile to emphasize here that, even though the drawing at a first look might suggest otherwise, the converter circuit in figure 3.1 belongs to the class which has been introduced in section 2.5, in particular figure 2.10. Often it is convenient to draw the resonant circuit in the middle, but evidently this does not change the operation of the circuit.

The schematic can be used to advantage to model the physical operation of the converter. For control purposes, however, we like to identify control inputs and control outputs of the converter, i.e. we want to obtain answers to the following questions:

- Where can we influence the operation of the converter?
- Which quantities do we wish to control?

Besides these two important matters, we also like to know the process dynamics, i.e. in which way do the inputs influence the outputs, and disturbances, i.e. environmental quantities which do influence the operation of the system, but which we cannot influence directly.

Note that the concepts input and output in control, which essentially is concerned with the processing of information carry a completely different meaning than in electrical power engineering, where we are mostly concerned with the processing of energy. In the following, we will use both terms freely where misunderstanding is unlikely, and use the prefix ‘power’ or ‘control’ if needed.

A common use of the circuit of figure 3.1 would be to connect the power inputs (left three terminals) to a given (three-phase) supply, and the power outputs (right three terminals) to a three-phase load. For this situation, the three signal classes identified above can be described as follows:

Control inputs are the gate signals of the 24 thyristors in the circuit. Assuming a correct design of the gate amplifiers, these signals can only have two values: On or Off.

Control outputs are electrical quantities at the terminals of the converter. Depending on the type of power supply and the type of load, we can choose the outputs of the system to be voltages or -currents, both at input and output terminals. It needs to be noted that for a particular terminal we can only choose either current or voltage as an output of the system. The value of the covariable\(^1\) will then be determined by the characteristics (impedance) of the external circuit.

Disturbances consist of the covariables of the outputs.

The choice whether to choose for a current or a voltage to be the controlled variable in a particular terminal is free, in principle. However, common sense indicates that the characteristics of the external circuit will play a role here.

---

\(^1\)A variable when multiplied with its covariable yields an energy flow (power). In our context currents and voltages are each other's covariables.
For example, if the power is supplied by the utility grid, which can be modeled as a voltage source with low impedance, it will be very hard to change the voltage with the converter. In this situation it makes sense to try to control the input currents of the converter, and to consider the input voltages as disturbances.

In the following, we will assume that we want to control the output voltages and the input currents of the converter. Consequently, the output currents and input voltages will be considered to be disturbances. For control purposes, the converter can then be considered as a 24 input, 6 output system.

The observations above lead to a ‘classical’ setup for a control structure for the converter, which has been depicted in figure 3.2.

![Figure 3.2: Possible control structure](image)

In the setup of fig. 3.2 the measured values of the output voltages and input currents are compared with their respective reference values, and the errors are used to derive new signals to fire the thyristors.

Unfortunately, the structure of figure 3.2 can not be expected to work. Several reasons can be put forward:

- In principle the error signals alone contain insufficient information to be able to compute the thyristor firing signals. Even for the (much simpler) case of DC-DC single phase power conversion, the actual value of the error does not indicate (for example) the switching frequency of the semiconductors.

- By the nature of the process, the error signal(s) have a rippling appearance, which makes action based on these signals alone very hard to define.

- The process dynamics, i.e. the “transfer functions” from the 24 digital inputs to the 6 analog outputs are very complicated. There is no way to derive from the error signals alone even the polarity of a particular transfer function. For example, in one situation, firing a particular
thyristor can lead to a more positive current in a terminal, whereas in another situation firing the same thyristor does not have any influence. In still another situation, firing once again the same thyristor could lead to a short-circuit and destruction of the converter.

3.3 State based control

The different situations mentioned above can be interpreted as a representation of the internal dynamics of the process, i.e. the dynamical behaviour of internal states. The relevant states can be easily identified in the simplified model which has been described in chapter 2. The state space of the converter can be thought of as spanned by the following coordinates:

- The current $I_{res}$ in the resonant inductor $L_{res}$ and the voltage $V_C$ on the resonant capacitor $C_{res}$, which have already been introduced as state variables in chapter 2, and

- the positions (On/Off) of the switches in the simplified model, which corresponds to the conducting or nonconducting state for the corresponding thyristors in fig. 3.1.

The first two states are analog quantities, the other 24 (or 12, depending on the description) can, as will be shown later, be considered to be digital (On/Off) states. It has to be noted that the actual behaviour of the converter is a (small) subspace of the total state space. For example, if all switches are turned Off, no current can flow in the resonant circuit. Also, we would like to exclude states which correspond to short-circuit.

In control theory it is well-known that any plant with linear dynamics can be stabilized if full state information is available. The converter we are dealing with here is not a linear system, but state information can be used to advantage here as well. Of the 26 states mentioned above, two ($V_C$ and $I_{res}$) can be directly measured in the circuit. The other 24 states can not be measured directly, as they correspond to internal quantities of the power semiconductor chips. Therefore we have chosen to estimate these states with an observer structure, i.e. a circuit which mimics the relevant dynamics of the subsystem under interest. This estimate for the state is then used instead of the real state.

The internal state of an SCR thyristor is composed of a three-dimensional charge pattern in the semiconductor junction. However, for the control of the converter the relevant information concerning the switching of an SCR can be summarized as a digital quantity: either the SCR is able to withstand a forward voltage, or it is (or may be) not. An observer for this quantity can therefore be implemented with very little electronic hardware. The state of the observer is stored in a digital flipflop, which is set if the SCR in question receives a gate pulse when the voltage difference between anode and cathode ($V_{ak}$) is positive. The flipflop is reset when $V_{ak}$ has been negative during a
time exceeding the turnoff-time \((t_q)\) of the SCR. Therefore if the flipflop is in the off state, the SCR is capable of blocking forward voltage (safe); in the on state, the SCR can be carrying current or be in the process of turning off (unsafe).

### 3.3.1 Vcpeak control

For safe operation of the converter, we like to have predictable upper bounds for component stresses. In particular we want to be able to limit the maximum values of (rms) current and voltage applied to the semiconductors. These voltages and currents are directly related to the voltages and currents in the resonant circuit. A feasible way to limit the stress on the thyristors is therefore to limit these values in the resonant circuit. The state plane description in chapter 2 suggests a method for limiting the voltage on the resonant capacitor. After firing the thyristors for the first current segment the state variables \(I_{res}\) and \(V_C\) are monitored until the trajectory of the first current segment crosses the intended trajectory (circle) for the second segment. Two methods can be used here:

- computation of the distance of \((V_C,I_{res})\) on the first trajectory to the centre of the second trajectory, and initiating the crossover to the second current segment when this distance equals the radius of the second trajectory,

- initiating the crossover to the second current segment at the value of \(V_C\) given by equation 2.16.

Both methods will be discussed in the following.

### 3.3.2 Vcpeak control by radius computation

This control method will be discussed referring to figure 3.3, which is a copy of the left-hand part of figure 2.7.

![Figure 3.3: State plane trajectory of \((V_C,I_{res})\) with radii](image-url)
The distance $R_1$ from a point on the trajectory of the first current segment to the centre of the trajectory of the second current segment is given by:

$$R_1 = \sqrt{(Z_{\text{res}}I_{\text{res}})^2 + (V_C - V_{LC2})^2}$$ (3.1)

At the instant of switchover to the second current segment this distance should be equal to the radius $R_2$ of the trajectory of the second current segment, i.e.

$$R_1 = R_2 = \sqrt{(V_{C2} - V_{LC2})^2}$$ (3.2)

The instant of switchover can therefore be computed from equation 3.2. Taking into account that $R_1 > R_2$ on the first trajectory, the condition for switchover from the first to the second current segment can be derived as follows:

$$R_1 \leq R_2 \Rightarrow$$ (3.3)

$$\sqrt{(Z_{\text{res}}I_{\text{res}})^2 + (V_C - V_{LC2})^2} \leq \sqrt{(V_{C2} - V_{LC2})^2} \Rightarrow$$ (3.4)

$$(Z_{\text{res}}I_{\text{res}})^2 + (V_C - V_{LC2})^2 \leq (V_{C2} - V_{LC2})^2 \Rightarrow$$ (3.5)

$$(V_{C2} - V_C)(V_{C2} + V_C - 2V_{LC2}) \geq (Z_{\text{res}}I_{\text{res}})^2$$ (3.6)

This condition can be implemented in hardware using some operational amplifiers and two analog multipliers.

### 3.3.3 $V_{C\text{peak}}$ control through computation of $V_{C1}$

Another method to obtain the condition for turnover to the second current segment is by computing the value of $V_C$ at which turnover should occur ($V_{C1}$) and comparing this value with the measured value of $V_C$. The value of $V_{C1}$ is indicated in figure 3.4.

![Figure 3.4: State plane trajectory of $(V_C, I_{\text{res}})$ with $V_{C1}$](image)

If for simplicity we assume $I_{\text{res}} > 0$, the condition for switchover to the second current segment is given by:

$$V_C > V_{C1}$$ (3.7)
from which we derive, using equation 2.16:

\[ V_C > V_{C2} \times \frac{V_{LC1} + V_{LC2}}{V_{LC2} - V_{LC1}} \]  \hspace{1cm} (3.8)

It is interesting to note that the right-hand side of equation 3.8 can be computed before the start of the current pulse, because all values \( V_{C2}, V_{LC1}, V_{LC2} \) are known already at that instant. This makes it feasible to use a common circuit for the computation of this value for several paralleled converters. In equation 3.8 \( V_C \) is the only quantity which needs to be measured during the current flow. As \( V_C \) can be compared directly to the computed value of \( V_{C1} \), delay in the circuit can be much less than for the circuit implementation of equation 3.6. Another interesting feature of this implementation is that no measurement of the resonant current and scaling with \( Z_{res} \) in the circuit is needed.

### 3.4 Current and voltage control

Input and output signals of the converter consist of currents and voltages. For a given terminal (input or output) of the converter we can define either the current or the voltage as the variable to be controlled. A problem arises here because of the shape of the terminal current, which is essentially a copy of (a part of) the current in the resonant circuit. Due to the pulsating character of this current, the actual error signal, defined as

\[ \text{error} = (\text{reference}) - (\text{measured quantity}) \]  \hspace{1cm} (3.9)

will always show a certain deviation from zero. This error signal can therefore not be used to control the converter directly.

#### 3.4.1 The current ASDTIC controller

An elegant way to overcome this problem has been proposed by Schwarz [76]. The method, which is usually denoted by the acronym ASDTIC (Analog Signal to Discrete Time Interval Converter) is based on the observation that because of the low-pass filtering performed at the converter terminals, the quantity we would really like to control is the average value of the current, not its instantaneous value. Therefore we can use the time integral of equation 3.9 as the actual error signal which is used to control the converter (Err). Typical wave shapes of the signals involved are shown in fig. 3.5.

The operation of the converter would then be governed by the signal \( \text{Err}(= \int (i - i_{ref}) dt) \) crossing an upper or lower bound, which corresponds to an excess or shortage of charge respectively. As long as the signal \( \text{Err} \) remains between the two bounds no action is taken.

The distance between the upper and lower bound in this scheme can be computed from the expected worst-case value of the ripple (corresponding to the shortest possible pulse in the resonant circuit) on the integrated
error signal. On average, however, the ripple is much lower than its worst-case value, because the pulses are longer than minimum. The result for the ASDTIC-control will then be that the ripple signal will stay close to one of the bounds, which implies that a steady-state error will be present.

A common way to deal with steady-state errors is to include a proportional-integral (PI) controller in the chain. In our case this circuit needs to be placed before the comparison with the bounds. The effect of the integral action can be limited to a range corresponding to the distance between the two bounds, as this is the maximum steady-state deviation which can be expected.

3.4.2 The voltage ASDTIC (ripple) controller

If we want to control the voltage at one of the terminals of the converter directly, we encounter a similar problem as with the current ASDTIC controller due to the ripple on the terminal voltage. However, integration of the error signal in this case is not needed. Why this is so will be discussed referring to fig. 3.6.

In the current ASDTIC, the current reference is subtracted from the measured current and the resulting difference integrated. Thus the output of this integrator (ASD_i in fig. 3.6.a) is given by:

$$\text{ASD}_i = K_i \int (i - i_{ref}) dt$$  \hspace{1cm} (3.10)
Figure 3.6: Two implementations of ASDTIC control
a: (left) Signal processing in current ASDTIC
b: (right) Output filter configuration, which serves as integrator in the voltage ASDTIC

where $K_i$ signifies the scaling done while measuring the currents.

For the voltage ASDTIC a voltage reference is subtracted from the measured voltage, so the error signal ASD$_u$ is given by:

$$\text{ASD}_u = K_u (U - U_{\text{ref}})$$

(3.11)

with $K_u$ the voltage measurement scaling factor. With reference to figure 3.6.b, which shows the filter capacitor normally connected to the terminals of an SR converter, this equation can be further manipulated to

$$\text{ASD}_u = \frac{K_u}{C_f} \int (i - i_{\text{load}}) dt - K_u U_{\text{ref}}$$

(3.12)

With appropriate scaling, the formulae are very similar: the role of the integrator in the current ASDTIC is taken over by the filter capacitor $C_f$. The similarity led us to adopt the same algorithm for the voltage control as for the current control: as long as the voltage error remains between bounds, no action is taken.

### 3.5 The line selection algorithm

The resonant converters described here all consist of one resonant circuit which, by means of one switch matrix, is connected to several terminals. This structure implies that the resonant circuit needs to be time-shared between the individual terminals. If, for example, two outputs both want to be supplied with the same current, this will not be possible at exactly the same moment. However, by sending the individual current pulses alternatingly to the first and second output, we are able to supply both outputs with the desired (average) current.

A completely new question therefore arises in the control of this kind of, i.e. multiphase, converters. We do not only need to decide here when to start a new current pulse, but also to which terminals the resonant circuit will be connected.
For the general case of a converter with \( n \) inputs and \( m \) outputs, the problem how to supply the \((n+m)\) individual terminals with current becomes increasingly complex. In the following we will describe an algorithm (see also [28, 29, 26, 37, 38, 31, 32]) which performs the selection of the terminals which will be connected to the resonant circuit for one resonant (half)cycle.

The line selection algorithm is subject to the following restrictions:

- Use a minimum number of switching actions per resonant (half)cycle, in order to reduce switching losses,

- select terminals which make it possible for the resonant circuit to remain in an oscillating mode, i.e. keep the peak capacitor voltage \( V_{C2} \) between predescribed bounds (see section 3.3.1),

- select terminals and direction of current flow which will reduce the individual ASBTIC error signals,

- permit a simple hardware implementation.

In section 2.3 it has been shown that we need to use at least two current segments if we want to be able to use the circuit cyclically. To minimize switching losses, we will in the following use only this minimum.

The topology of the circuit treated here dictates that the resonant current always flows through two thyristors. The only choice left to minimize the number of switch operations is the way we switch over from the first to the second current segment.

Most existing series-resonant power topologies use a switching pattern in which at a segment border two semiconductor switches are turned on and two others are turned off. However, in our topology, where only one switch matrix is used, it is also possible to operate the converter in such a way that only one switch needs to turn on and one other needs to be turned off at the segment border [92, 31]. An example has been depicted in figure 3.7.

In figure 3.7a current flows from terminal \( R \), via the resonant circuit, to terminal \( U \). After some time, a new thyristor is fired in branch \( S \), the resonant current commutates from branch \( R \) to \( S \), and we arrive in the situation of figure 3.7b.

Figure 3.7 shows that with this method, only three terminals of the converter are used for a particular halfcycle. One of these \((U\) in the example\) carries current during the complete halfcycle, another \((R\) only during the first current segment, and the third one \((S\) only during the second current segment. For one individual halfcycle, the schematic of the active part of the converter can be redrawn as in fig. 3.8.

The positions of the toggle switch correspond to the first and second current segments, respectively. If we compare figure 3.8 with equation 2.13 it shows that the two voltage sources in fig. 3.8 must present themselves to the resonant circuit with opposite polarities. In other words, the voltage of the circuit node \((a\) between the two voltage sources must lie between the
The line selection algorithm

Figure 3.7: Example of the current flow in the three-phase to three-phase converter of figure 3.1.
   a: (upper) During the first current segment
   b: (lower) During the second current segment

Figure 3.8: Active part of the converter during one halfcycle

voltages of the “extreme” nodes (b) and (c). The circuit diagram also shows that circuit node (a) corresponds to the terminal which carries current during the complete resonant (half)cycle, and that the direction of the current in this terminal is opposite to the two other currents in terminals (b) and (c). This brings us to the following

**Rule 2** For cyclical operation of the resonant circuit, the one terminal out of the three involved for one resonant (half)cycle that is to carry current in a unique direction needs to carry a voltage in between the voltages of the other two terminals involved in this particular cycle.

For the design of the control electronics of our subsynchronous converter we like to note that, once we know which three terminals will be involved for a
particular resonant (half)cycle, the switching pattern will be completely defined by Rule 2, the desired direction(s) of current flow and the commutation requirement (see section 2.3.6).

Another consequence of Rule 2 is that the peak capacitor voltage, which is subject to equation 2.30, can be much lower than its worst-case value. Inspection of figure 3.8 shows that in our context the peak capacitor voltage needs to be higher than the maximum voltage difference between any two terminals of the converter. Direct application of equation 2.30 would lead to twice that value.

From the restrictions mentioned above and the discussion thereafter we have distilled the following line-selection algorithm:

1. Compare the error signals ASD\textsubscript{i} and/or ASD\textsubscript{u} of all (n + m) terminals against each other in order to find the terminal with the largest positive error and the one with the largest negative error (corresponding to a desired negative and positive current flow respectively).

2. check each of the remaining (n + m − 2) terminals together with the two which have been selected before for compliance with Rule 2.

Clearly, if we do find three terminals using this algorithm, we can initiate a resonant (half)cycle which will indeed move the individual error signals closer to zero, while keeping the energy in the resonant circuit at an appropriate level. It remains to be shown that we will necessarily find such a set of three. The algorithm can go wrong in two ways:

1. All error signals are either positive or negative. This implies that we try to make the converter generate electrical charge out of nothing, which is clearly (Kirchhoff’s current law) impossible. An outer control loop, which will be discussed in subsection 3.6.1, will cure this situation,

2. the check for a third terminal for compliance with Rule 2 generates no result. This implies that we try to make the converter generate or consume net energy, which for an idealized, lossless, Vpeak controlled converter is impossible because of the law of conservation of energy. A second outer control loop, which will be discussed in subsection 3.6.2, will adjust the reference signals in such a direction that this situation will be resolved.

The interaction of the selection algorithm with these two outer control loops implies that, whenever the selection algorithm finishes with no result, we can just “try again”, and eventually come up with a valid result.

### 3.6 Restrictions due to conservation laws

In this section, we will consider the consequences of two well-known conservation laws for the operation of a multiphase to multiphase converter. Here,
for the first time, we will try to arrive somewhat closer to reality, and assume that the converter is not ideal. In particular, we will investigate the problem associated with a converter which is subject to power losses (of an as yet unspecified nature) and measurement errors.

A general \(n\)-input, \(m\)-output converter connected to \(n\) sources and \(m\) loads has been depicted in fig. 3.9.

![Converter Diagram](image)

Figure 3.9: Converter with \(n\) inputs and \(m\) outputs

We will discuss the consequences of Kirchhoff’s Current Law (KCL) and the Law of Conservation of Energy (LCE) with respect to this figure.

### 3.6.1 Kirchhoff’s current law

If we apply Kirchhoff’s current law to the circuit of fig. 3.9, we obtain the following equation:

\[
\sum_{k=1}^{n} i_{nk} + \sum_{k=1}^{m} i_{outk} = 0 \tag{3.13}
\]

If we were to apply a current ASDTIC controller to every individual terminal of this converter, we would obtain \((n + m)\) ASDTIC error signals (see equation 3.10). Combining with equation 3.13, we obtain the following expression for the sum of the ASDTIC signals \(ASD_s\):

\[
ASD_s = \sum_{k=1}^{n+m} ASD_k
\]

\[
= K_i \sum_{k=1}^{n+m} \int i_k dt - K_i \sum_{k=1}^{n+m} \int i_{refk} dt
\]

\[
= -K_i \int \sum_{k=1}^{n+m} i_{refk} dt \tag{3.14}
\]

where for convenience of notation we have combined inputs and outputs in one summation. Clearly, equation 3.14 implies that if we want to keep the individual error signals low, the sum of the reference signals should be zero. In other words, we should not ask the converter to produce currents which violate KCL.
In a practical situation, we can of course choose to generate the references $i_{refk}$ such that their sum equals zero. However, due to the finite accuracy of the waveform generator and of the measurement of the individual currents, and due to the integration of the $\sum i_{refk}$ in equation 3.14, large ASDTIC error signals could still exist in this situation. A possible solution to this problem is to use the right-hand side of equation 3.14 to generate an extra input to some or all of the ASDTIC integrators, in time bringing ASD$_i$ to zero.

If the converter system is governed by both current and voltage control, a more complex situation arises. Without going into detail, it can be said that again in this situation the signal ASD$_u$ can be used to generate extra inputs to the ASDTIC integrators, bringing their sum to zero. Details of the implementation will be discussed in chapter 7.

### 3.6.2 Conservation of energy

In this section, we will assume that in a physical converter power losses occur in the elements which compose the power circuit. The total power loss $P_{loss}$ absorbed by the converter of fig. 3.9 can be expressed as:

$$P_{loss} = P_{in} + P_{out} = \sum_{k=1}^{n} u_{ink}i_{ink} + \sum_{k=1}^{m} u_{outk}i_{outk} \tag{3.15}$$

As $P_{loss}$ in general is an unknown function of the actual terminal currents and voltages, it will be impossible to generate current and/or voltage references which will satisfy equation 3.15. Of course the circuit itself will always satisfy equation 3.15, which implies that without taking appropriate measures the error signals ASD$_u$ and/or ASD$_i$ will get out of bounds.

An approximate solution to the problem of generating reference signals which satisfy equation 3.15 for the case of a current-input, voltage-output converter has been given in [38] and will be briefly treated here.

Suppose we have a converter system where a distinction has been made between "master" (output) and "slave" (input) terminals, such that voltage references are generated for the master terminals, which are in some way controlled to follow these references. The slave terminals then carry current to cater to the power need of the converter. One way to generate current references $i_{refk}$ for the slave terminals of the converter is:

$$i_{refk} = \frac{P_{uk}}{\sum_{j=1}^{n} u_{jk}^g} \tag{3.16}$$

which for $P =$ constant will generate input currents at power factor 1. If the actual slave currents of the converter equal their references, $P$ represents the actual input power, otherwise $P$ can be interpreted as an estimate for the input power.

The problem now is to obtain a good estimate. For an approximate
solution to this problem we will first define a new quantity $E_{ex}$ as:

$$E_{ex} = \sum_{k=1}^{n} ASD_k u_k$$

(3.17)

The interpretation of $E_{ex}$ will be given later. For current-controlled inputs, equation 3.17 can be rewritten as:

$$E_{ex} = \sum_{k=1}^{n} u_k \int (i_k - i_{ref_k}) dt$$

(3.18)

For the relatively short time scale we consider here, the $u_k$ can be considered constant, so we can move them inside the integration. In this way we arrive at:

$$E_{ex} \approx \sum_{k=1}^{n} \int u_k (i_k - i_{ref_k}) dt$$

(3.19)

which can be rewritten as:

$$E_{ex} \approx \sum_{k=1}^{n} \left( \int u_k i_k dt - \int u_k i_{ref_k} dt \right)$$

(3.20)

After substitution of equation 3.16 and changing the order of the summation and integration we obtain:

$$E_{ex} \approx K_i \int (P_{in} - P) dt$$

(3.21)

which indicates that $E_{ex}$ is approximately proportional to the time integral of the mismatch between the real power at the slave (input) side of the converter ($P_{in}$) and the value which is used to compute the slave current references. $E_{ex}$ can therefore be used to change the value of $P$, the estimate for the input power, in the right direction. An implementation of the technique will be shown in chapter 7.

### 3.6.3 Additional restrictions

Besides the restrictions which have been discussed in sections 3.6.1 and 3.6.2, which deal with the complete converter system (all terminals), restrictions can also apply to a subset of the terminals only. Specifically for the converter which is composed of two switch matrices connected to a common resonant circuit (see fig. 2.3), KCL dictates that the sum of (the low frequency content of) the input currents, and also of the output currents, will be zero. A similar restriction applies if the converter feeds a floating load.
3.7 Phase-staggering

Phase-staggering control of an $n$-tuple power modules is a technique which, by means of phase-shifting the pulse pattern of the individual modules, makes the complete converter system appear as one converter with $n$-fold power rating and operating frequency. For example, if we consider two SR DC-DC power converters operating in parallel, we obtain a converter system where the lowest harmonic in the input- and output currents appears at four times the operating frequency of the individual converters. An example of this situation has been sketched in fig. 3.10.b.

![Waveforms](image)

Figure 3.10: Unfiltered output currents and output voltage for two paralleled modules (simulated)
- a: (left) Without phase staggering
- b: (right) With phase staggering

This compares favourably to the situation where the converters are just crudely connected in parallel: then the lowest harmonic in these currents would appear at twice the operating frequency (see fig. 3.10.a). The higher ripple frequency makes filtering of both input- and output waveforms easier. Note that for clarity we have used a very small filter capacitor in the setup which produced figure 3.10.

For the case of DC to DC conversion, an analysis of the reduction in harmonic content which can be achieved is relatively easy (see [52]), and the technique has been applied successfully in several cases [65, 94]. Although an analytical approach is likely to fail if we want to consider the case of paralleled multiphase power converters, common sense indicates that a similar reduction could be possible here.

The advantages of using phase-staggering control are several. In particu-
lar, phase-staggering can be used to:

- Raise the power level of the converter system beyond the level possible with a single module,
- achieve substantial reduction in harmonic content of input- and output waveforms,
- provide redundancy in the converter system,
- allow for smaller filtering equipment,
- raise the controllable bandwidth of the input and/or output signals,
- allow slower operation of the individual modules, which enlarges the choice in power semiconductors.

A severe disadvantage of the technique is that the number of semiconductors and other power components rises linearly with the number of modules.

### 3.7.1 Control

As long as the converter system considered here operates in steady-state, shifting the pulse patterns of the individual modules can be achieved using a phase-lock loop (PLL) circuit and a divider. For operation under transient conditions, however, the extra dynamics introduced by the voltage controlled oscillator (VCO) and the loop filter of the PLL tend to either slow down the response or cause stability problems. Therefore we have tried to provide a solution without introducing additional dynamics.

For simplicity, we will first consider the case of a single ASDTIC-controlled DC-DC converter here. This circuit can be regarded as a VCO on its own: the frequency of the pulses generated by the converter depends (even linearly) on the value of the reference signal. If we compare this VCO with the setup which is common in digital frequency synthesizers [14, 15, 101], the similarity is striking (see figure 3.11).

The digital VCO consists of a register, which is clocked at a certain rate $f_{\text{clock}}$. At every clock pulse, the contents of the register are updated with new values, which are computed as the sum of the old register contents and the reference input. If the addition overflows, i.e. if the new contents do not fit in the (finite-size) register, an overflow pulse is generated. The average frequency $f_{\text{av}}$ of the overflow pulses is given by:

$$f_{\text{av}} = f_{\text{clock}} \times \frac{\text{reference value}}{\text{maximum register contents} + 1}$$  \hspace{1cm} (3.22)

In the case of the digital VCO it is well-known that the contents of the register can be interpreted as the excess phase at a certain instant. Similarly, the contents of the integrator in our ASDTIC-controlled converter can be regarded as excess charge.
If we want the digital VCO to generate multiple shifted pulse streams, a feasible solution would be to add a sequencer to the circuit of figure 3.11.a, and make the reference signal proportionally larger to arrive at the same pulse rate for the individual streams. The equivalent solution to the analog VCO, i.e., the converter, would then be to change the pulse generating circuit in such a way that multiple converter modules would be fired sequentially. Both the digital and analog circuits for the generation of multiple pulse streams have been depicted in fig. 3.12.

As in the digital case, we can now make the analog reference signal \( n \) (the
number of modules) times higher than before, to arrive at the same pulse rate for the individual converters. Clearly this fits with our expectation that the multi-module converter system will deliver \( n \) times the current of one module.

Essentially, the problem how to control \( n \) paralleled power modules has been solved now: by sharing only one ASDTIC circuit for all modules, no additional dynamics is introduced, and automatic load sharing is accomplished. Unfortunately, however, the analog and digital circuits are not completely equal. The contents of the digital register in fig. 3.12 will develop in time as a discretized saw-tooth signal: directly after an overflow is generated, the contents of the register are subject to a stepwise transition down. The contents of the analog integrator do not exactly follow this pattern. The wave shape of the ASDTIC integrator signal, which has been depicted in figure 3.5 on page 38, shows some resemblance to a sawtooth, but due to the time it takes to generate the current pulse, no more than that. Especially it needs to be noted that, due to the sinewave pulse shape, the actual integrator signal will remain out of (upper or lower) bounds for a finite time after the initiation of the pulse. This implies that, without appropriate countermeasures, a second, third etc. power module would be fired directly after the first. The converter modules tend to synchronize themselves, which means that phase staggering can not be achieved in this way.

A possible solution to this problem could be to change the appearance of the integrator signal by adding some compensation. If the compensated signal looks like a sawtooth, then the analog setup will be completely similar to the digital case, and the problem be solved. Now from equation 3.10 it can be seen that if we add the signal \(-K_i \int (i) dt\) to the integrator output, we will obtain \(K_i \int (-i_{ref}) dt\), which is linear in time, for the compensated signal. The signal \(-K_i \int (i) dt\), which is no other than a scaled replica of the voltage on the resonant capacitor, is readily available in the \(V_{cpeak}\) control circuit. The setup has been sketched in figure 3.13.

![Diagram](image)

**Figure 3.13:** Setup of the compensation of the integrated error

In the definition of the compensation signal an integration constant is implicitly available. A sensible way to use this freedom is to set the compensation equal to zero when no current flows. For this case, the shapes of relevant signals are shown in figure 3.14.a.
Figure 3.14: Shape of current ($I$), 'raw' integrator signal ($e$), compensation ($c$), and compensated integrator signal ($e+c$)

a: (left) For a terminal conducting during a complete halfcycle
b: (middle) For a terminal conducting during the first segment only
c: (right) For a terminal conducting during the second segment only

Up to now we have discussed the case where the output current of the converter consists of the rectified resonant current. In the case of a multiphase converter, terminal currents can be composed of the first current segment, the second current segment, or both. The solution indicated above can easily be adapted to this case: only an appropriate portion of the scaled capacitor voltage is used for compensation of the integrator output. The cases of current flow during the first segment or second segment only have been depicted in fig. 3.14.b and 3.14.c respectively. Note that the level where the scaled replica of the capacitor voltage is 'cut off' is equal to $V_{C1}$. In a type 2 Vcpeak predictor circuit (see section 3.3.3) this signal is readily available, which implies that the overhead in terms of hardware for the implementation of the compensation can be relatively small.
3.8 Deviations

The algorithms which have been presented for V peak-, current-, voltage-, and phase-staggering control all rely on the simplified model of the converter which has been developed in chapter 2. However, in the combination of a real converter with a real control circuit processes take place whose effects are not incorporated in this model. As has been indicated in section 2.4, the simplified model of the power circuit could, in principle, be extended in order to incorporate some of these 'parasitic' processes. In this section we will try to obtain an impression of the consequences of the deviations caused by the imperfection of the simplified model and of the control circuit for the control design.

3.8.1 Conduction losses

Up to now we have assumed the resonant circuit and the semiconductor switches to be lossless. In a real converter this will of course never be the case. All power components (semiconductors, wiring, inductors, and capacitors) are subject to parasitic conduction losses. As a first approximation we will divide these losses into two classes:

- Voltage losses, i.e. losses which are proportional to the average value of the current involved and can therefore be represented by a DC voltage source in the current path,

- Resistive losses, i.e. losses which are proportional to the square of the rms value of the current involved.

As far as control design is concerned, voltage losses can be catered to by an appropriate 'shift' of the measured voltages. The structure of the controller does not need to change.

Resistive losses are harder to handle. According to [69] in the presence of resistive losses the trajectory of $I_{rcs}$ versus $V_C$ changes to a logarithmic spiral. An explicit expression for $V_{C1}$ is not possible in this situation. For small values of the resistive damping, the logarithmic spiral can be approached by a circle with a slightly adjusted centre point and radius. The adjustment can be made with small offsets in the values of $V_{LC1}$ and $V_{LC2}$ which are fed to the predictor circuit.

3.8.2 Snubbers

In the presence of snubber circuits the operation of the power circuit becomes rather complicated. The snubbers, which for the converters studied here will consist of an R/L/C combination, have two major impacts on the power circuit:

- They introduce non-linear elements in the circuit, which makes analytical evaluation of their influence effectively impossible, and
• they raise the complexity of the circuit (number of nodes and branches) enormously, which has more or less the same effect.

Because of this, the influence of a specific snubber circuit on the operation of the control circuits can only be analyzed by means of simulation. Some simulation results will be presented in chapter 6. For the same reasons, the proper selection of a snubber circuit is a complicated task. This matter will be treated in chapter 5.

3.8.3 Commutation

When commutation inductances are introduced in the converter circuit, both the shape of the resonant current pulse and the mathematical description of this waveform differ significantly from the situation without commutation. An analysis of the phenomena which take place during commutation has been made in appendix A. The waveforms involved now consist of three segments instead of two. If we try to make a derivation of the value of $V_{c1}$ similar to the one in equations 2.14...2.16, it turns out that an explicit formulation of the values of the capacitor voltage at the start ($V_{c1a}$) and end ($V_{c1e}$) of the commutation interval is not possible (see appendix A). A possible solution to this problem could be to solve the implicit equations describing the commutation process with an iterative method. However, with such a method much of the simplicity of the $V_{cpeak}$ control is lost. Therefore we have not pursued this solution any further.

3.8.4 Time granularity and delay

An implementation of the control electronics will in most cases be based on a synchronous design of its digital part. An asynchronous design is possible in principle, but will, due to the complexity of the control system, be very hard to design and debug. A consequence of the use of a synchronous design, which runs on the edges of one common system clock, is that control actions can be initiated only at discrete points in time. This implies that in general control actions will be started somewhat later than optimal.

As an example, in a DC-DC converter the turnover from the first to the second segment of the resonant current will occur slightly after the optimal moment which is computed by the $V_{cpeak}$ controller. Consequently, the capacitor voltage will fall short of its intended value, and the $V_{cpeak}$ controller will try to compensate by adjusting the instant for turnover of the next current pulse. After several of these cycles, the computed instant for turnover will be one system clock cycle earlier than before, and turnover will be initiated more or less at the right moment. The result is that the peak capacitor voltage will be slightly too low for several pulses, and then build up again. This mode of operation has been depicted in figure 3.15.

As can be seen in figure 3.15, the result is that a beat frequency appears in the capacitor voltage (and, as a consequence, in the resonant current).
An even more complex pattern can appear when the current control tries to compensate for the slightly diminished charge which is delivered every pulse.

The consequences of pure time delay in the Vpeak control circuit are of a somewhat different nature. As before, due to the delay the turnover to the second current segment will be initiated somewhat too late. This will result in a final value of the capacitor voltage which is too low. In order to correct for this low capacitor voltage, in the next resonant cycle the Vpeak control will try to start the second current segment a little earlier. The process is of an iterative nature, but for practical values of the time delay it will converge very fast. The overall result is that the converter will operate with a peak capacitor voltage which is stable, but lower than the desired value.

It needs to be stressed that the consequences of time granularity and delay in practice are only visible in a pure DC-DC single phase context without commutation inductances. In general, commutation and the active switching between multiple terminals induce much larger deviations of the capacitor voltage.

### 3.8.5 Voltage ripple

The assumptions we made concerning the smoothness of the terminal voltages will not be fulfilled in a practical configuration. In an economically designed converter, the filter capacitors will be kept as small as possible, depending on the needs of the power source and the load. Practical values of the filter capacitors for AC-AC converters lie in the range of 10 to 100 times the resonant capacitor. As a consequence, if we assume the source and load circuits to have a negligible shunting effect at the frequencies considered, there will be a voltage ripple on the terminals in the range of 1 to 10% of the peak-to-peak voltage swing on the resonant capacitor. As a first approximation, the filter capacitors can be incorporated into the resonant circuit with appropriate weights. The resulting circuit then becomes of the more complex type which is both voltage- and current loaded. As a consequence, the centres of the
state plane trajectories will no longer lie on the line $I_{res} = 0$, which makes the analytical evaluation of the phenomena hard, to say the least.

3.9 Discussion

The series-resonant multiphase power converter, considered as a system to be controlled, has a rather special structure. The input signals are binary, outputs are analog, and the system operation is governed by fast internal dynamics. Therefore control of the system through output feedback alone is not possible.

Measurement and/or reconstruction of the state (both digital and analog) of the converter, and recognition of some properties of the simplified model which has been derived in chapter 2, allows the fast internal dynamics of the system to be controlled through a non-linear system, which here is called a $V_{cpeak}$ predictor. Two possible concepts for such a predictor have been shown.

Once the fast internal dynamics have been tamed, control of the system outputs (currents and/or voltages) becomes possible. The system outputs, by the nature of the process, have a rippling nature. An interpretation of these outputs is needed in order to obtain usable information for the control system. It is found that the philosophy of ASDTIC control \cite{76} can be extended to the multiphase case, both for current- and voltage control.

The resonant circuit in a multiphase converter needs to supply current to all converter terminals. An algorithm, which caters to those terminals with the largest deviations first, is used to select three out of the available terminals, which will be used for the duration of one resonant halfcycle.

Kirchhoff’s current law and the law of conservation of energy lead to restrictions to the reference signals supplied to the controlled converter. The number of degrees of freedom for these references is at least two lower than the number of terminals of the converter. Two independent controllers adjust the reference signals in order to take care of these restrictions.

For dynamic phase-staggering of multiple power modules one more control system is needed. In order to make sure that the individual modules are synchronized in the right way, information about the state of these modules is fed forward to the error signal.
Chapter 4

Simulation Tools

In the process of designing a power converter and its associated circuitry we often need to know whether a certain step in the design yields the desired result. With the availability of (micro)computers today, it has become commonplace to use simulation techniques to verify a design.

The most important factors which determine the choice for a simulation package are the following:

a) The quality of the user interface,
b) the accuracy of the results,
c) the speed of the simulation,
d) the range of possible models,
e) the portability across different hardware platforms,
f) the flexibility (importing/exporting results from other tools),
g) the price.

In general, a trade-off needs to be made between these factors. At the beginning of this project (in 1984), only a PDP-11 computer was available for simulation work. The available packages which would in principle allow simulation were the following:

- FORTRAN-IV
- ONSI-PASCAL
- PSI

The number (150) of available blocks (note we had only 64k bytes available at the time!) directly ruled out the use of PSI. Both FORTRAN and PASCAL were
viable candidates for the implementation of simulation packages. Because of its more structured approach to programming, PASCAL was chosen.

During the project, personal computers became available. The PASCAL software which had been developed at that stage, was ported to the PC Turbo Pascal compiler [4]. On this new hardware platform, graphical features could be added using a dedicated library [3]. With the availability of newer and faster compiler products [5] the packages were ported with minor effort.

The major advantages of using a higher programming language for simulation work are the following:

- In principle, any model structure can be used, including state event mechanisms which are important in power electronics (see [7]),
- the simulation can run much faster than on a general-purpose simulator, such as PSI or \textsc{matrix},
- as long as file formats etc. are known, input or output can be used or supplied in any format with reasonable programming efforts.

A major disadvantage of a higher programming language is the user interface: instead of the currently popular ‘Click a mouse button and Go!’ approach some Real Programming (with a keyboard) is still needed.

4.1 Applications

During the project which is described in this work, simulation software was developed for the following purposes:

- Evaluation of the line selection algorithm,
- evaluation of power handling capability,
- evaluation of the algorithm for phase-staggering,
- evaluation of switching stresses on components,
- verification of the control hardware.

Unfortunately, these different aspects could not all be implemented handily in one single simulation package, because of two reasons:

a) The large size of the circuit, both power part and control electronics. For a three-phase to three-phase converter, the power circuit comprises 24 thyristors, as many non-linear inductances, and several elements more. The control electronics features over 300 integrated circuits of rather diverse nature, and mixed analog and digital signal processing.

b) The large spread in time scales. These range from tens of nanoseconds for the components of the digital control system, through microseconds for several parts of the power circuit, to tens of milliseconds for the analog control circuits and the waveforms of the utility grid.
The combination of a) and b) above implies that the complete system could not be simulated in detail in an acceptable time on a personal computer. If we (optimistically) assume the computer to operate at 1 Mflops, and we need an estimated average of 50 flops per integrated circuit, with a time step of 50 ns we would obtain:

\[
\frac{t_{\text{real}}}{t_{\text{sim}}} = \frac{1 \text{step}}{50 \text{ns}} \cdot \frac{300 \text{IC's} \cdot 50 \text{flops/IC}}{\text{step}} \cdot \frac{1 \text{s}}{1 \text{Mflop}} = 300000 \tag{4.1}
\]

which means that we would need about 3.5 days to simulate 1 second. Clearly this time is unacceptably long. Therefore we have opted to use several simulation approaches which each highlight a different aspect of the operation of the converter.

### 4.2 Common properties

All simulation packages have been written in a high-level language (Pascal), as this yields the fastest simulation with reasonable programming efforts.

The programs all have a similar structure, which in pseudocode can be written as follows:

```plaintext
initialize; {give state variables a start value}
input; {let the user make changes if (s)he wants}

repeat
    compute; {solve network equations}
    check_for_changes; {are switches opening or closing?}
    update; {perform integration for state variables}
    output; {show results on screen, or write to file}
until stop; {time runs out or user wants to finish}

terminate;
```

This basic scheme still allows many different implementations, which will be discussed in the following sections. One choice which is common to all the packages is the integration method. An important consideration for this choice is that, because we are working with switching networks, the accuracy of an integration algorithm can not easily be proved. For simplicity and ease of dealing with state events we have chosen to use the well-known Euler algorithm. For this algorithm the network problem needs to be solved only once for every time step. The accuracy of this method can be easily verified by running the same simulation with different time steps, and it is relatively easy to implement a state event mechanism. We will come back to that subject in section 4.5.
4.3 Evaluation of the terminal selection algorithm: program Tslct

For evaluation of this algorithm, which has been presented in section 3.5, it is necessary to simulate the behaviour of the converter over the time span of several cycles of the utility grid (mostly 50 or 60 Hz). This simulation covers the longest time span of all, therefore it is important to make the time step as large as possible, and to keep the program as simple as can be justified with regard to accuracy.

As mentioned before, the diversity of time scales involved in an electronic power converter implies a very long simulation time if we want to incorporate every possible physical phenomenon. However, it has been verified experimentally [48, 29] and proven theoretically (for linear systems) [56] that if a system contains dynamic properties at two sufficiently different time scales, than the fast dynamics can be approached with static properties, and the behaviour of the complete system can be approached with the slower dynamics.

The practical implementation of this idea is as follows. During the flow of resonant current we assume the input- and output voltages of the converter to be constant. This makes it possible to solve the differential equations which describe the operation of the converter for one halfcycle analytically, similar to the approach which has been taken in chapter 2. This analytical solution can be used to compute the charges displaced during the cycle, and these in their turn are used to update the voltages at the terminals of the converter.

The reasoning above implies that the time step in the simulation is chosen to be as large as one resonant cycle, and is therefore not constant. This time step, typically tens of µs, is sufficiently large to make simulation of hundreds of milliseconds in a short time possible.

The algorithms which are used to control the converter are represented as such, no specific hardware implementation is used. Therefore, besides for the evaluation of the control algorithm, this setup is also useful to obtain insight in stresses on the passive components (especially mean and rms currents) under different loading conditions. The simulation is applied to the power circuit as depicted in fig. 4.1.

For simplicity, in the simulation the resonant capacitor \( C_{\text{res}} \) is turned around (i.e. \( V_C \) is inverted), after every halfcycle of the resonant current \( I_{\text{res}} \). This setup ensures that the resonant current will always be positive, which simplifies the equations and the bookkeeping in the simulation.

For the bookkeeping in the simulation program, heavy use has been made of the matrix structure which has been introduced in section 2.3.1. Voltages, currents, displaced charges, and several variables more have been represented as vectors. Which switches turn on during the simulation of one resonant halfcycle can then be traced with three variables. These variables in their turn can be used to index into the aforementioned vectors. This data structure allows a very compact notation to be used.

As an example, here is how the terminal with the highest error signal is
selected from all terminals:

```plaintext
terminalfound := false;
for terminal := r to w
  do if terminalfound
  then begin
    if error[terminal] > error[worstterminal]
      then worstterminal := terminal;
  end
  else begin
    worstterminal := terminal;
    terminalfound := true;
  end;
```

A similar loop can be used for the lowest (most negative) error signal and for the selection of a third terminal.

### 4.3.1 Examples

The output of the simulation can take several shapes, depending on the demands of the user. The following figures serve as examples of the output of this package.

Fig. 4.2 shows an example of the scope-like traces, taken from a simulation of 100 ms. The converter is used here as an interface between a 33 Hz supply and a load to be powered with 50 Hz.

For simplicity this simulation does not shows the wave shape of the individual current pulses (which would hardly be visible anyway), but shows the total charge per pulse which is supplied to a particular terminal of the converter. The lengths of the pulses in the six current traces of fig. 4.2 are proportional to the size of this displaced charge. Note that the sign convention here is such that positive current flows from the outside world to the converter, both for inputs and outputs.

Figure 4.3 shows the part of the $V_{LC1} - V_{LC2}$ plane (see also figure 2.9) covered during normal operation.
Figure 4.2: Example of the waveforms as generated in the line selection simulation at full load
Simulation time: 50 ms.
$U_u...U_w$: output voltages (220 V rms)
$i_r...i_t$: input currents (both unfiltered and filtered)
$i_u...i_w$: output currents (unfiltered)

The range of $V_{LC1} - V_{LC2}$ applied to the converter is used for snubber design.

Besides graphics, the package can also evaluate the values of mean, rms and peak currents applied to the semiconductors and the passive parts of the power network. These values will be used in chapter 6 for the design of the power circuit.

4.4 Evaluation of the phase-staggering algorithm: program Simb5

For a first evaluation of the phase-staggering control algorithm we have designed a simulation using the power circuit of figure 4.4.

The individual power modules of this circuit represent the smallest possible converter of the structure which has been presented in figure 4.1. The input bridge consists of two branches, the output of only one branch. This particular topology has been described more fully in [93, 92].

The neutral of the output is connected to the neutral of the source. For simplicity, the source is composed of a split ideal DC voltage source, only the output voltage $U_o$ is controlled, and $U_o$ is restricted to be smaller in
Figure 4.3: The part of the $V_{LC1} - V_{LC2}$ plane which is covered during operation of the converter under the same conditions as in figure 4.2. The dots represent samples which correspond to 10 seconds operation of the converter, the dashed line indicates the border according to equation 2.30.

Figure 4.4: Power circuit used for the evaluation of phase-staggering control magnitude than the input voltages $\pm E_s/2$. As has been indicated in section 3.4 a PI-controller with limits on the I-action is used in order to centre the rippling output voltage around the reference.

In order to evaluate the phase-staggering algorithm, a number of these power modules is connected in parallel, both at the source- and the load side. The restriction on $U_o$ implies that the output will always receive the
full resonant waveform, i.e. the only compensation signal needed is the signal which has been shown in figure 3.14a, trace c.

Figures 4.5 and 4.6 show some results of the simulation.

![Graph showing I1, I2, Uo, err, and errcomp](image)

Figure 4.5: Results of the simulation of two paralleled power modules without phase-staggering control. The resonant frequency is 10 kHz, the output frequency 200 Hz.
Horizontal axis: time (0.5 ms)
Upper traces: output currents (I1 and I2),
Middle traces: output voltage (Uo) and error (magnified 10 times),
Lower trace: compensated error signal with bounds (dotted).

The differences between both the shape of the output voltage Uo and the magnitude of the compensated error signal errcomp in figures 4.5 and 4.6 show the intended operation of phase-staggering control. Clearly the ripple on the output voltage in figure 4.6 is much smaller than in figure 4.5.

The lower traces in figures 4.5 and 4.6 show that the compensated error signals tend to stay close to the bounds against which they are tested. Therefore the distance between these bounds needs to be larger than the charge displaced by one resonant pulse. It can be made proportionally smaller (see figure 4.6) when phase-staggering control is used, as the displaced charge per switch action is smaller in this case.

Note that in figures 4.5 and 4.6 a very low ratio between the resonant and generated frequency was used in order to obtain a well-visible ripple.
4.5 **Switching stresses on semiconductor components: program DVDT15**

During turn-on and turn-off the semiconductors are subject to a variety of stresses due to the switching. The most well-known stresses related to switching are:

- $\frac{di}{dt}$ stress
- $\frac{dv}{dt}$ stress
- Overvoltage due to snap-off

We assume these stresses to be dependent only on the initial conditions (voltages applied to the resonant circuit) of a particular resonant (half)cycle. It is then possible to analyze these stresses over a range of voltages, and evaluate at which moment in time the stresses applied to the semiconductors have their maximum value.

Because of the consequences of non-linear phenomena very small time constants can be present in the circuit if a complete model of the thyristors and their surrounding circuitry (see chapter 5) is used. This implies that for accuracy of the simulation a small time step needs to be used. If an explicit integration method, such as Euler or Runge-Kutta [9] is used, a small time step is needed for stability of the integration algorithm as well.

Snubber networks can be used to alleviate the switching stresses applied to the semiconductors. The snubber networks we have used in this work are
composed of inductors (both saturating and non-saturating), resistors, and capacitors. As the stresses on the semiconductors are largely dependent on the detailed switching behaviour of the semiconductors themselves, models are needed for the detailed behaviour of these devices. These models will be considered more fully in chapter 5. Here we will assume that these models are available.

The switching behaviour of the network introduces a new simulation artifact which becomes visible when detailed simulation is needed. The problem at hand is that whereas thyristors can be turned on at will at (almost) any time we wish, the turnoff time is dictated by the network and the thyristor, and therefore generally will not coincide with one of the simulation time steps. This "state event" mechanism [6] is typical for many power electronic circuits. In a simulation context it can be taken care of by interpolation. For our purposes linear interpolation proved to be successful. The technique will be illustrated referring to figure 4.7a.

![Figure 4.7: Incorporating state events in a numerical integration](image)

a) (left) Simulation with a fixed time step $dt$
b) (right) Simulation with one adjusted time step $dt'$

Suppose that, at a certain simulation time $t_0$ the value of a current $I$ in our simulation crosses through zero. If this would, for example, be the current flowing through an ideal diode, then this device would turn off at $t = t_0$, and therefore the current at $t = t_{n+1}$ should be zero. However, because in our simulation the value of $I$ is evaluated only at discrete instants in time, we would detect a negative current, which is clearly impossible in this circuit.

Our approach has been as follows. If we assume a reasonable accuracy of the simulation in the first place, the current on the interval $[t_n, t_{n+1}]$ can be approximated with a straight line. The value of $t_0$ can then be computed as follows:

$$t_0 = \frac{I_{n+1}t_n - I_nt_{n+1}}{I_{n+1} - I_n}$$  \hspace{1cm} (4.2)

If we now repeat the numerical integration starting from $t = t_n$ with a new time step $dt'$ defined by $dt' = t_0 - t_n$, then, apart from round-off errors, we will obtain a value for $I_{n+1}$ which is exactly zero.
After this intermediate computation with a smaller time step $dt'$ we can continue the numerical integration with the old time step $dt$. The resulting time vector and the values obtained for the current are shown in figure 4.7b.

If more state changes can be expected, the scheme indicated above must be applied using the lowest value for $t_0$ for all state changes which have occurred in the interval of interest.

This mechanism has been applied to a power network which is composed of a number of identical branches, one of which is shown in figure 4.8.

![Diagram of a power network with Th2, Th1, Ls2, Ls1, Lc2, Lc1, Lc0, Lc3, Ls0, Ls3, Th0, Th3, and connections to resonant circuits.]

Figure 4.8: One branch of the power network which is used for the simulation of switching phenomena.

Each semiconductor is shunted by an $R - C$ series circuit. This combination is on its turn connected in series with two inductors, one of which is saturable, the other one is linear. A complete branch, which is connected to one (input- or output) terminal, is composed of four semiconductors with their aforementioned circuitry.

The complete power circuit consists of a number (minimal three) of these branches, connected to the resonant circuit. For the analysis of the switching phenomena, we assume that for the first segment current flows through branches 0 and 1, and for the second current segment through branches 0 and 2. Switchover from the first to the second current segment is initiated by a Vcpeak predictor of one of the types discussed in section 3.3.1.

The other branches in the circuit are not actually switching, but act as a kind of snubber across the resonant circuit.

An example of the output of this package is given in figure 4.9.
4.6 Verification of the control electronics: program Simphs

For the implementation of the control algorithm which has been described in chapter 3 a combination of analog and digital electronics is used (see chapter 7). For the verification of the functioning of this electronics, preferably before the implementation into hardware itself, we would like to have a simulation which is a direct copy of the (intended) implementation.

The digital part of the control electronics, which has to perform quite a few algorithmic functions, tends to become rather complicated for this type of converter. Therefore it was decided in an early stage to use programmable logic (EPLD's, see [2]) for the implementation of the digital electronics. Programmable logic allows changes to the function of the circuit to be made without any hardware changes, and therefore is an almost ideal tool for de-
developing complicated digital hardware. This advantage, however, leads to problems with regard to the relation between the implemented hardware and the simulation.

The problem here is that we want to be sure that the simulation uses exactly the same data as the hardware. The data for the hardware implementation is supplied as a text file, which is taken as input by a ‘logic compiler’, i.e. a program which checks the data for errors and produces a fuse map which can be used to program the logic integrated circuits. As a by-product, the logic compiler we have used ([39]) can produce a file with boolean equations, which describe the operation of the programmed device. These boolean equations come in a format which is very similar to the PASCAL code we would like to use as a part of the simulation package. The following piece of code is an example of the ‘boolean’ output of the logic compiler:

```
........

SHIFT_MODSEQ :=
   AAN & /MS0_Q & /MS1_Q
+ AAN & /LAATSTE_MOD & MS0_Q & MS1_Q & /TWIN_1_Q;

SIGNU_HPL_HNL_Q :=
   LS1_Q & SIGNU_HPL_HNL_Q & /WR
+ /LS0_Q & LS1_Q & /SIGN_ITOL_V & /UTOL_UUL & WR
+ /LS0_Q & LS1_Q & SIGN_ITOL_V & UTOL_UUL & WR
+ LS0_Q & LS1_Q & SIGNU_HPL_HNL_Q ;

........
```

We have used a custom-made program to translate this description to the corresponding PASCAL code. The output of this program for the code shown above is as follows:

```pascal
procedure dig_ana_LGC;
begin
   with omz.anadig do

   ........

   SHIFT_MODSEQ:=
   (AAN AND (NOT MS0.q) AND (NOT MS1.q)) OR
   (AAN AND (NOT LAATSTE_MOD) AND MS0.q AND
   MS1.q AND (NOT TWIN_1.q));

   ........
```

end; {with statement}
end; {of procedure dig_ana_LGC}
procedure dig_ana_reg;
begin
    with omz.anadig do
    begin

        ........

        SIGNU_HPL_HNL.d:=
        (LS1.q AND SIGNU_HPL_HNL.q AND (NOT WR)) OR
        ((NOT LSO.q) AND LS1.q AND (NOT SIGN_ITOL.v) AND
        (NOT UTOLE_UUL) AND WR) OR
        ((NOT LSO.q) AND LS1.q AND SIGN_ITOL.v AND UTOLE_UUL AND WR) OR
        (LSO.q AND LS1.q AND SIGNU_HPL_HNL.q);

        ........

    end; {with statement}
end; {of procedure dig_ana_reg}

Two separate PASCAL-procedures are produced, because a difference needs

to be made between mere booleans and register values.

The method described above allows the simulation of the digital part of
the hardware to be a direct map of the (programmed) hardware itself.

Unfortunately, for the analog part of the hardware this method cannot be
used. Therefore this part of the circuit operation, and also the communication
between the different circuit boards, has been programmed manually. Most
of this programming work consists of bookkeeping, which can be greatly
simplified by defining some adequate procedures in Pascal. In particular, we
made sure that both digital and analog (three-state) busses were not left in
an undefined (floating) state. Although the manual translation of an analog
circuit diagram to simulation code can be a bit tedious, it needs to be done
only once. We expect that, with the introduction of hardware description
languages [59], this coding part can in time be automated as well.

4.7 Discussion

Simulation tools can serve to verify the proper operation of a circuit before it
even exists. They can be a very valuable tool in design, because they allow the
designer to perform experiments without risking costly power components.
Assuming that the simulation is a precise copy of the actual apparatus, any
'what-if' scenario can be played and evaluated.

A common problem in simulation of complex circuits is that large amounts
of computer power and/or time are needed to perform a detailed simulation.
A possible way out is to divide the simulation job into separate parts with
different degrees of refinement. Using this method, a number of simulation
packages has been built, each of which emphasizes a particular phenomenon of the circuit.

The fastest approach uses analytical approximate solutions for the computation of phenomena on a relatively long time scale. Other setups allow switching phenomena to be studied in detail, to evaluate the operation of the electronic control circuit, and to compute the effects of phase-stagerring two or more power modules.
Chapter 5

Modelling Fast Transients

The design of a power electronic converter can roughly be split up in two phases. The first phase is involved with the design of a power circuit and control methods which together permit a desired flow of energy. The second phase, which we will consider in some detail here, treats the design of the circuit with regard to transient phenomena. These phenomena occur at or around the instants where the power switches in the circuit open or close. Without proper measures, the values of transient voltage \( (dv/dt) \) and current \( (di/dt) \) may easily be too high for the power semiconductors involved. In most cases, the transient wave shapes of current and voltage applied to these devices need to be well-defined, and maximum values for the transient wave shapes are supplied by the manufacturer. Often, shaping networks (snubbers) are used in order to arrive at limited values for the rate of rise of forward blocking voltage \( (dv/dt) \) and current \( (di/dt) \).

It will be clear that the operation of these snubbers is of prime importance for the reliability of the whole converter system. Unfortunately, the design of these networks is not a straightforward matter. The designer is confronted with a large number of choices to be made with regard to topology and component values.

A complete treatment of the subject of snubber design could easily fill a thesis by itself. Therefore we will restrict our treatment to only one snubber topology, and to one type of active semiconductor. However, we think that the methods used here can be applied to most other power circuits as well.

Outline

This chapter is composed as follows. After a brief introduction to snubbing in section 5.1, a simplified model is used to derive the total amount of snubber losses in an SR converter. A crude approximation shows that total snubber losses might easily be larger than the sum of the losses in the semiconductors, thereby stressing the importance of proper snubber design.

In section 5.2 the specific snubber topology which has been used for this
work is developed. Application of simulation data to a simplified circuit model leads to a first estimate for $\sigma$, the ratio of commutation vs. resonant inductors. It is shown that for some of the circuit elements nonlinear models are needed in order to obtain insight in the behaviour of the circuit. Application of saturable inductors for the limitation of $dv/dt$ leads to a special interaction between a thyristor which turns off and its antiparallel neighbour. Analysis of this interaction shows that it is useful to use two separate saturable inductors in this situation.

In order to evaluate the choices made so far, nonlinear dynamic models for the operation of some of the components are developed in section 5.3. The models are derived from either data sheet specifications, or from data provided by some easy to perform measurements.

The actual choice of snubber circuits is intimately linked to the design of the rest of the power circuit and is therefore deferred to chapter 6.

## 5.1 General remarks

The power network which we will analyze here is indicated in fig. 5.1.a. It represents the part of a multiphase converter which is active during one halfcycle of the resonant current.

![Resonant power network](image)

Figure 5.1: Resonant power network
a: (left) Schematic of resonant power network
b: (right) Shape of currents through some branches

The network is composed of a full-wave multiphase thyristor bridge (matrix) which is connected to a resonant circuit which is used to obtain low $di/dt$ values at turn-on and turn-off of the thyristor switches.

Without loss of generality, we will assume that a resonant halfcycle has been initiated with current flow during interval $S_1$ through thyristors $Th_{r1}$ and $Th_{r3}$. We will zoom in at what is happening in the switching matrix at the boundary between the first and second current segment as indicated by $t_1$ in fig. 5.1.b. At $t = t_1$ a third thyristor, say $Th_{s1}$, is turned on in order to take over the current flow from thyristor $Th_{r1}$. Associated with this takeover
a voltage transient across thyristors \( Th_{r2} \) and \( Th_{t2} \) occurs. In the absence of parasitical circuit elements the \( dv/dt \) applied to thyristors \( Th_{r2} \) and \( Th_{t2} \) will be infinite, possibly causing parasitical turn-on and consecutive short circuit of the power source and/or the load. Similarly, the \( di/dt \) applied to \( Th_{r1} \) (turning off) and \( Th_{t1} \) (turning on) will be infinitely high. For \( Th_{r1} \) this will lead to a high value of the reverse-recovery charge (read: losses) and for \( Th_{t1} \) to possible damage due to current crowding or hot spot formation.

In order to lessen the \( di/dt \) and \( dv/dt \) stresses on the semiconductors, snubber networks are introduced in the power circuit. These networks are dimensioned to translate the infinitely steep voltage and current steps described before into steps with limited slope and limited overshoot. For unipolar operation a variety of networks, often with the possibility to recover a part of the energy which could be dissipated in the network, has been invented [8]. For bipolar operation the choice is very limited. Networks with recovery of energy are feasible, but tend to be too complex to be reliable [97].

Snubbers, whose primary role is to shape the voltage and current waveforms applied to the semiconductors, also lead to a specific energy loss for every switching cycle. In applications where the switching frequency is low, this needs not be a problem, and overrating the snubbers seems to be an acceptable (-ed, see [83]) method. However, as losses in snubber circuits are directly proportional to the average switching frequency, overrating at high frequencies could easily lead to a strong decrease in overall efficiency.

First, we will compute the order of magnitude of the energy dissipated in the snubbers.

### 5.1.1 An approximation to total snubber losses

A very rough approximation of the losses in the snubber circuits can be made if we assume that for every resonant halfcycle the voltage on the snubber capacitors reverses from \( \pm 0.5V_{C2} \) to \( \mp 0.5V_{C2} \). If we assume that every thyristor is equipped with its own snubber, the total loss \( W_{snub} \) can be computed by summing the losses over all \( 4 \times (n + m) \) snubbers. Thus we obtain:

\[
W_{snub} = 4 \times (n + m) \times 0.5 \times C_d \times V_{C2}^2
\]

(5.1)

For the example of a 3-phase to 3-phase converter \( (n = m = 3) \), with \( V_{C2} = 800V \) and \( C_d = 10nF \), this evaluates to 76.8 \( mJ \) per halfcycle. This number compares rather badly to the losses in the semiconductors, which for this example lie in the range of 8 \( mJ \) per conducting thyristor [83]. In section 5.2.2 we will show that the estimate made in equation 5.1 is rather conservative. However, the result obtained underlines the necessity of a more thorough analysis of the phenomenon.
5.2 Snubber model and topology

5.2.1 A linear snubber network

The basical setup of a common bipolar protection network in the series-resonant converter of fig. 5.1.a is shown in fig. 5.2.

![Bipolar thyristor snubber diagram](image)

Figure 5.2: Bipolar thyristor snubber

The network consists of a capacitor $C_d$, resistor $R_d$ and inductor $L_d$. Analysis of the circuit is straightforward and has been treated in many textbooks (see for example [57, 91]). Qualitatively it will be clear that a proper choice of $L_d$, $R_d$ and $C_d$ could give us the desired transient response. As we are also interested in the losses occurring in the circuit, we will analyze these somewhat further.

5.2.2 An approximate evaluation of the influence of commutation circuits on snubber losses

The energy dissipated in the resistor of an $R - C$ snubber depends strongly on the shape of the applied voltage. For a step-wise change of the applied voltage from 0 to $V$ volts, it is well known that the dissipated energy $W$ in $R$ follows from

$$W = \frac{1}{2} CV^2$$

Equation 5.2 applies in general for a step-wise change of the applied voltage from an initial voltage $V_1$ to a voltage $V_1 + V$. It can be easily seen that, if we shape the applied voltage from one single step to a succession of two steps of half the magnitude, the energy dissipated in $R$ will be halved. Both situations have been depicted in figure 5.3.

The losses in the snubber resistor in the situation of fig. 5.3.b will be half as large as in the case of fig. 5.3.a only if we assume the time constant of the snubber to be much lower than the time between the two consecutive steps in fig. 5.3.b. In general, a key parameter for the evaluation of the losses appears to be the ratio between the snubber time constant and the time the applied voltage takes to rise.

In the context of the series-resonant converter, the voltage applied to the snubber circuits can, in a first approximation, be thought to be composed as follows (see [36]):
Figure 5.3: Losses in an R − C snubber for two different shapes of the applied voltage
a: (left) One step of magnitude V
b: (right) Two steps of magnitude $\frac{1}{2}V$

a) Short stepwise transitions at or close to the switching actions, connected by

b) relatively long smooth transitions between the switching actions.

We will assume here that the only significant power losses in the snubbers appear because of a) (see also [62]).

For a simplified power circuit, where only linear inductances are used, the magnitude of the voltage steps applied to the R − C snubbers at the switching instants can be derived analytically. The result of this analysis is a rather long mathematical expression. The voltage steps are found to depend among others on:

- The voltages on the terminals selected for the particular current pulse, and

- the ratio of the commutation inductance to the total resonant inductance ($\sigma$).

This last parameter is interesting here, because we have some freedom to choose the value of the commutation inductances, as long as the $di/dt$ applied to the thyristors is below the allowed maximum. We would like to obtain a practical insight in the dependence of the snubber losses on this parameter. Therefore we have taken a batch of samples from the terminal
Figure 5.4: Energy loss in the snubber circuits as a function of $\sigma$, the ratio between the commutation and total resonant inductance

selection simulation program T slec t (see section 4.3 and [38]), and computed the resulting loss. The result has been plotted in fig. 5.4.

Clearly a proper choice of the commutation inductance is not only important for the switching losses in the semiconductors, but also for the losses in the snubbers. The rather weak minimum between a ratio of 0.2 and 0.5 still allows a wide choice.

5.2.3 Adding the thyristor junction capacitance

Unfortunately, in a practical situation the network model as shown in fig. 5.2 often is not sufficient. The capacitance of the thyristor junction, which is strongly dependent on the applied voltage, appears to play a role in the network behaviour. If we incorporate this capacitance in the network, we obtain a nonlinear circuit problem of third order, which by itself makes an analytical approach practically impossible.

A solution to this problem would then be to choose $C_d$ an order of magnitude larger than $C_{th}$, the (average) junction capacitance, and to neglect the influence of $C_{th}$ in the design. Using this approach our design problem would be completely fixed (even overconstrained), having three degrees of freedom ($C_d$, $L_d$ and $R_d$) and four constraints ($dv/dt$, overshoot, $di/dt$, and $C_d = 10C_{th}$). The relevant formulae, being of second and first order, can be solved analytically. One disadvantage of this method is that the snubber capacitance $C_d$ in general will be much larger than strictly necessary, leading to higher power losses in the snubbers, cooling problems and decreased efficiency of the converter.
5.2.4 Saturating inductors

Experience has shown us that with this method the implementation of $L_d$ is strongly dependent on the power of the converter system. When using large thyristors at relatively high frequencies, the value of $L_d$ obtained is approaching or exceeding the value of the total inductance needed in the resonant circuit ($L_{res}$). The main reason for this behaviour is that the maximum allowed $\frac{dv}{dt}$ for a thyristor, given a maximum for $V_{ak}$ and for $t_q$, seems to be more or less independent of the current rating.

The effective resonant inductance is composed of the 'real' resonant inductance with two commutation inductances ($L_d$) in series. The lowest value for the effective resonant inductance then equals $2L_d$, and if this value is too large this would indicate that such a circuit would not even be feasible. In order to exit from this dead-end situation we have used saturating inductances for (a part of) $L_d$. In this way we obtained some sort of decoupling between the $di/dt$ and $dv/dt$ design.

5.2.5 Nonlinear snubber network

The model of the snubber network with the thyristor then becomes as indicated in fig. 5.5.

![Bipolar thyristor snubbers with nonlinear effects incorporated](image)

Figure 5.5: Bipolar thyristor snubbers with nonlinear effects incorporated

A saturable inductor ($L_s$), in combination with an RC snubber across the thyristors, is used in order to obtain low $\frac{dv}{dt}$ values during switching transients in the network. Nonsaturating inductances ($L_c$) are used to obtain smooth transition (commutation) of the current from one thyristor branch to another. In designing such a network we would like to be able to obtain limited $di/dt$ and $dv/dt$, low voltage overshoot, low snubber losses, and low component count.

If we attack this design question, a first problem is posed by the circuit being nonlinear, which for all practical cases means that an analytical solution is not possible. In this era of personal computers this doesn't need to be a large problem: if we assume that for every circuit component a model is available, simulation tools provide for a fast check of the circuit operation, regardless of nonlinearities and circuit complexity. Simulation also allows us to use a very general formulation of the problem: using this tool it is possible
to incorporate the nonlinear behaviour of both the junction capacitance $C_{th}$ and the saturating snubber inductance $L_d$. This approach has already been used in the simulation which yielded figure 4.9.

With the simulation approach we can design the network using a snubber capacitance which is much smaller than in the method mentioned before, reducing power losses in the snubbers considerably. The method is also suited for incorporating nonlinear snubber capacitors, which are likely to have similar advantages as in the GTO context [73, 89, 90, 99, 100]. A drawback of this approach is that we need data concerning the thyristor junction capacitance, which in general is not supplied in thyristor specs on a regular basis. We will deal with this problem in section 5.3.2.

Before a final design can be made however, we need to pay attention to a nasty phenomenon occurring just after commutation, which will be described in the following section.

### 5.2.6 Commutation

A simplified converter model with commutation inductances added is described in appendix A. Instead, here we will concentrate on the full model of the circuit, i.e. with nonlinear junction capacitance, snubbers, and saturating inductances present.

For the discussion of the commutation process the "active" part of the converter network of fig. 5.1.a has been redrawn, with its snubbers, in fig. 5.6.a.

Main components are six thyristors, two voltage sources, the resonant tank circuit, and the snubber networks. We will assume that during the first current segment thyristors $Th_{r1}$ and $Th_{r3}$ are closed. In order for commutation to be possible with the indicated direction of the resonant current ($I_{cs}$), the voltage $U_2$ needs to be higher than $U_1$. The actual commutation of current flow from branch $r$ to branch $s$ is initiated when thyristor $Th_{s1}$ is fired. Referring to fig. 5.6.b, the process can be described as follows. After switch-on of thyristor $Th_{s1}$ the current $I_2$ in $L_{cs}$ and $L_{ss}$ starts to rise gradually, which results in the saturation of $L_{ss}$ after a short time. The current in $L_{cr}$ and $L_{sr}$ will decay, allowing $L_{sr}$ to get out of saturation after a while. The current in thyristor $Th_{r1}$ will cross through zero, allowing it to turn off. Depending on circuit parameters, the stored charge in thyristor $Th_{r1}$ will cause a reverse current peak through $L_{sr}$ which could cause $L_{sr}$ to saturate again for a short while (see lower trace in fig. 5.6.b). If $L_{sr}$ would be shared with the antiparallel thyristor ($Th_{r2}$) (as is the case in fig. 5.6.a) this saturation almost eliminates the snubber inductor. Clearly this situation could lead to very high $dv/dt$ values for thyristor $Th_{r2}$. A solution to this problem has been presented in [32]. It consists in using separate saturating inductors for the antiparallel thyristors. A possible new snubber configuration with separate $L_s$ inductors is shown in fig. 5.7. The configuration of a complete branch of the power network has already been shown in figure 4.8.
The analysis of the network problem with saturable inductors protecting the individual thyristors can become rather complicated. In general the thyristor data sheets do not contain the information which is needed to compute the exact values of reverse recovery charge and thereby $dv/dt$ for the case of varying $di/dt$. Experiments and simulations showed that the most dangerous location in time regarding $dv/dt$ is the moment just after thyristor $Th_{r_1}$ turns off. Depending on the dimensioning of the snubber circuit, the snap-off of the reverse current through thyristor $Th_{r_1}$ can cause a high reverse voltage across thyristor $Th_{r_1}$ and a high $dv/dt$ on thyristor $Th_{r_2}$. 
5.3 Obtaining model parameters

As has been discussed before, our approach has been to develop a simple model for every nontrivial component in the network, such that this model can be used in a simulation context. For the extraction of parameters, models which feature only data sheet specs are preferred.

For our purpose, we need to model the following phenomena:

1. saturating inductances
2. nonlinear thyristor junction capacitance
3. stored charge in the thyristor junction (for computation of the reverse-recovery current)

5.3.1 Saturating inductances

The saturating inductances were modeled according to the following formula:

$$L_s(i) = \frac{L_0}{1 + \left| \frac{i}{k_0} \right|^n} \quad (5.3)$$

The values of $L_s(i)$ can be measured using a commercial L-C meter, or, depending on the brand of magnetics used, obtained from some manufacturers' data sheets (see for example [71]). The setup for these measurements is depicted in fig. 5.8.a.

A current supply biases the two cores (which are assumed to be equal) at some DC value. The measurement is performed through a separate winding, which is wound such that no transformatory coupling exists between the L-C meter and the DC supply. From several measurements (typically 10-20)
the model parameters $L_0$, $k_0$, and $n$ can be calculated using a least-squares optimization. An example of the fitting of the model of equation 5.3 to measured data for a toroidal ferrite core is given in fig. 5.8.b.

5.3.2 Off-state junction capacitance

The basical setup for this measurement has been depicted in fig. 5.9.a.

A high-voltage power supply biases the thyristor junction at the desired value. The actual small-signal junction capacitance is measured with a commercial L-C meter. In order to protect the L-C meter, its input is shorted while changing the bias voltage. A choice of the values of $R_b$ and $C_s$ should be made such that their influence on the measurement is minimal. In order to obtain reasonable values for the junction capacitance, this measurement should be effected at the expected junction temperature. As in the case of the saturable inductor above, a simple model is matched to the measured data by means of a least-squares fit. The model we have used is described
Figure 5.9: Measurement of $C_{th}(v)$
  a: (upper) Circuit setup
  b: (lower) Example of data and fitted curve

by:

$$C_{th}(v) = \frac{C_0}{\sqrt{1 + \frac{v}{V_0}}} \quad (5.4)$$

where the values of $C_0$, $n$, and $V_0$ are supplied by the least-squares procedure. We found the best fit to our measurement data to occur at a value of $n$ close to 3. According to semiconductor physics [102], $n = 3$ corresponds to a semiconductor junction with a gradual change from n- to p- type material over the junction. An example of the fit of equation 5.4 to measured data is given in fig. 5.9.b.

5.3.3 Stored charge in the thyristor junction

The internal operation of a thyristor during turn-on and turn-off is a complicated problem to analyze. For the best approximation to physical reality, often a three-dimensional finite-element model of the semiconductor device is used, to obtain a solution for the local charge density [11]. However, the end user of the device often does not have access to the exact device data.
which are necessary to implement such an approach. Also, it can be expected that a simulation of several thyristors in a circuit with this method will consume a considerable amount of computer time. Therefore, a more practical approach seems to be to use the data which is supplied by the manufacturer on a routine basis to derive a simple model for the switching behaviour of the thyristor [95].

It has been shown in [32] that the main problem for designing snubbers is to obtain a predictable response at turn-off, therefore we will concentrate on this problem. The data which is supplied by the manufacturer specifies the reverse-recovery charge \( Q_{rr} \) and the peak of the reverse-recovery current \( I_{rr} \) as a function of the peak current \( I_{TM} \) and current slope \( (di/dt) \). For one of the thyristor types which have been used for this work, these characteristics are shown in fig. 5.10.

![Graph showing Qrr [μC] and Irr [A] as functions of di/dt [A/μs].](image)

**Figure 5.10:** Reverse-recovery parameters for thyristor SKFT 60 at T=125°C, parameter: \( I_{TM} \) (copied from [83])

a: (left) Charge

b: (right) Peak current

Our simple charge-control model can be expressed as:

\[
\frac{dQ_{junc}}{dt} = \frac{Q(i) - Q_{junc}}{\tau_2}
\]  

(5.5)

The parameter \( \tau_2 \) is a measure of the speed with which the junction charge adapts to a new value for the current. In our model the opening of the thyristor switch is governed by the charge \( Q_{junc} \) becoming zero. After this moment, the current through the thyristor decays exponentially to zero with another time constant \( \tau_2 \). In a first try to obtain our model parameters we have simulated our model under the data sheet conditions, with \( Q(i) \) modeled as \( Q(i) = \tau_1 i \), i.e. with a junction charge which depends linearly on the current. The results of this fit were rather unsatisfactory. A second trial was made with \( Q(i) \) depending on \( i \) in a manner similar to the bipolar
transistor as described in [55]. $Q(i)$ is then expressed as

\[
Q(i) = \begin{cases} 
\tau_{1a}i & \text{for } i \leq I_s \\
\tau_{1a}I_s + \tau_{1b}(i - I_s) & \text{for } i > I_s
\end{cases}
\quad (5.6)
\]

\[
Q(i) = \quad (5.7)
\]

The values for the reverse-recovery charge ($Q_{rr}$) and the peak of the reverse-recovery current ($I_{rr}$) obtained from this model are shown in fig. 5.11.

Figure 5.11: Reverse-recovery parameters for the model of thyristor SKFT 60, parameter: $I_{TM}$

a: (left) Charge
b: (right) Peak current

Clearly the fit is not perfect. A natural sequel to this three-parameter model for $Q(i)$ would be to allow $Q(i)$ to be specified at many more values of $i$.

According to [95], it is very hard to measure parameters concerning reverse recovery precisely. Therefore, we should expect some measurement artifacts to be present in the data in [83]. Without knowledge concerning the precision of the measured data it is tricky, to say the least, to use many model parameters.

As an example a test was made with models specifying up to 42 parameters for $Q(i)$. The fit of the reverse-recovery charge of these models to the data here was better than in fig. 5.11. However, to arrive at this better fit, we needed specifications of $Q(i)$ which held little resemblance to physical reality, where we would expect $Q(i)$ to be a monotonously rising function of $i$.

We conclude that it makes no sense to fit a highly parametrized model on these data. Therefore we have decided to use the simple model of equations 5.6 and 5.7 for simulation purposes.
5.4 Discussion

Snubber networks for current and voltage serve to protect power semiconductors against unfriendly wave shapes. The power dissipated in snubbers can be a substantial fraction of the total power loss in a converter. Therefore it is worthwhile to minimize the snubber losses.

Passive snubber networks are easy to implement, simple in construction, and therefore highly fail-safe. The use of nonlinear (saturable) inductances allows the functions of current- and voltage snubbers to be designed independently. The use of separate voltage snubbers for thyristors which are connected in antiparallel takes care of the interference caused by the reverse-recovery of the off-switching thyristors.

A converter with snubbers included is a high-dimensional, nonlinear dynamical circuit. A classical analytical approach to snubber design is therefore not possible. However, present-day computer tools allow for an easy simulation of the operation of such a circuit. For this simulation representative models of the crucial parts of the circuit are needed.

For the purpose of this work models with a simple topology, whose parameters can be measured or estimated in the field, are preferred. The data which is needed to compute the model parameters can be obtained by measurements on the actual components, or extracted from the manufacturers' data sheet. In all cases a least-squares method is used to fit a model to the data.
Chapter 6

Power Circuit Design

The design of the power circuit of an SR converter in general is a complicated task. For a DC-DC converter the final design depends on a large number of parameters, such as the output power, the desired spectral purity of the input and outputs, the temperature of the environment, and the cooling method. For multiphase applications we need to add to this list the number of input and output phases, the frequency of the supply and of the output, and their wave shapes.

For the simplified model of the single-phase DC-DC SR converter explicit design rules are readily available (see for example [45, 46]). If transient phenomena, such as commutation and snubbing, need to be incorporated the only tool available to the designer is simulation, and in most cases the design process will be of an iterative nature.

In the case of the multiphase SR converter, even for the simplified model of the circuit no explicit analysis appears to be possible. Therefore we have decided to use simulation as our primary design tool. However, in order not to lose the connection to physics completely, we will use a very simple rule-of-thumb method to obtain initial values for some major parameters. Only after this step we will use simulation for fine tuning of the design.

We will illustrate this method with the design of two 3-phase to 3-phase SR power converter prototypes which have been constructed in the course of this work. Both prototypes use one common switch matrix to serve both inputs and outputs. The first model features 15 kW output power and has served as a test bed for the basic concept of multiphase SR power conversion. The second model, designed for an output power of approximately 6 kW, uses the same basic concept for control, implemented in different electronic hardware however. The latter system, as an additional feature, carries the possibility to perform phase-staggering if a number of power modules are paralleled.

The simplified schematic of both prototypes has been shown in figure 2.11c. The complete schematic of the 15 kW model has been depicted in
Figure 6.1: Schematic of the power part of the experimental 15 kW converter

For practical reasons, for the 6 kW converter a slightly modified configuration of the commutation inductances has been used. The complete schematic
for that power circuit will be shown in figure 8.1.

The design of the control electronics will be dealt with in chapter 7. Here we will focus on the major steps needed to design the power circuit.

6.1 Main Specifications

A first step in any power circuit design consists in establishing the specifications in terms of voltages, processing power, etc. of the circuit. Table 6.1 lists the key specifications of both converters:

<table>
<thead>
<tr>
<th></th>
<th>15 kW</th>
<th>6 kW</th>
</tr>
</thead>
<tbody>
<tr>
<td>Maximum input line voltage (rms)</td>
<td>380 V</td>
<td>380 V</td>
</tr>
<tr>
<td>Maximum output line voltage (rms)</td>
<td>380 V</td>
<td>380 V</td>
</tr>
<tr>
<td>Input frequency range</td>
<td>DC .. 50 Hz</td>
<td>DC .. 50 Hz</td>
</tr>
<tr>
<td>Output frequency range</td>
<td>DC .. 50 Hz</td>
<td>DC .. 50 Hz</td>
</tr>
<tr>
<td>Phase staggering</td>
<td>No</td>
<td>Possible</td>
</tr>
<tr>
<td>Number of input Phases</td>
<td>3</td>
<td>3</td>
</tr>
<tr>
<td>Number of output Phases</td>
<td>3</td>
<td>3</td>
</tr>
<tr>
<td>Input wave shape</td>
<td>sine</td>
<td>sine</td>
</tr>
<tr>
<td>Output wave shape</td>
<td>sine</td>
<td>sine</td>
</tr>
</tbody>
</table>

Table 6.1: Key specifications of the two multiphase converters

From the specifications in table 6.1 some important design parameters can be extracted. One of the most important ones is the peak capacitor voltage $V_{C_2}$, which needs to obey equations 2.26...2.30.

6.2 Initial selection of $V_{C_2}$ and $C_{res}$

The line selection algorithm we use (see section 3.5) connects the resonant circuit such that the following condition needs to be fulfilled:

$$V_{C_2} > \text{maximum voltage between any two terminals} \quad (6.1)$$

In passing, we like to note that this value for $V_{C_2}$ is substantially lower than the value needed in the two-matrix topology. For that power circuit, the peak capacitor voltage needs to be larger than twice the highest input- or output voltage.

In the limiting case (maximum input voltage, maximum output voltage) we obtain:

$$V_{C_2} > 2 \frac{\sqrt{2}}{\sqrt{3}} \times 380 \text{ V} = 620.5 \text{ V} \quad (6.2)$$
This is an absolute minimum for the capacitor voltage. As will be shown in section 6.8, a safety margin is needed to obtain some robustness against adverse operating conditions and unmodelled phenomena. After some simulation experiments it was found that a value of $V_{C2} = 800 \text{ V}$ provides an adequate margin.

On the other side, the peak capacitor voltage is limited by the voltage range allowed by the thyristors. If we assume that the voltages applied to the power circuit divide symmetrically over the thyristors, the highest voltage applied to a non-conducting thyristor is one of the following:

a) The maximum voltage difference between any two terminals, or

b) the peak capacitor voltage.

Dynamically, the voltages applied to the thyristors can be (much) higher than the values a) or b) above. The exact values can not be derived analytically, however. Therefore we have decided to continue the design with the lowest workable value for $V_{C2}$, i.e. 800 V, and use simulations to find out the maximum voltage applied to each thyristor.

If we were to build a DC-DC converter, we could continue here with the computation of the resonant circuit. For the DC-DC converter, the output power and voltage allow to compute an average output current. With a given average output pulse frequency $f_{av}$, peak capacitor voltage $V_{C2}$, and mean output current $I_{av}$, the value of the resonant capacitor $C_{res}$ could be found from:

$$C_{res} = \frac{I_{av}}{2f_{av}V_{C2}} \quad (6.3)$$

For the multiphase converter, an exact computation of $C_{res}$ is not possible. As a first approximation, we will consider the situation where the (resistively loaded) converter supplies power to a DC grid. If we select the voltages of this DC grid to be a snapshot of the situation in a symmetrical AC grid, it is reasonable to expect that we will obtain at least the right order of magnitude for $C_{res}$. We will consider two such situations here:

1. One of the output voltages zero, the other two at $\pm \cos(\pi/6) \frac{\sqrt{2}}{\sqrt{3}} \times 380 \text{ V}$. This results in a voltage difference of 537.4 V.

2. One of the output voltages at maximum, the other two equal. This results in a voltage difference between the output terminals of $\frac{3}{2} \frac{\sqrt{2}}{\sqrt{3}} \times 380 = 465.4 \text{ V}$

The highest output current corresponds to the lower voltage, i.e. to situation 2 above. For an initial estimate, this situation has been worked out, for a resonant frequency of 10 kHz (i.e. a minimum pulse width of 50μs), assuming

$$f_{av} = 2f_{res} \quad (6.4)$$
in table 6.2.
<table>
<thead>
<tr>
<th></th>
<th>15 kW</th>
<th>6 kW</th>
</tr>
</thead>
<tbody>
<tr>
<td>Output voltage difference</td>
<td>465.4 V</td>
<td>465.4 V</td>
</tr>
<tr>
<td>Output power</td>
<td>15 kW</td>
<td>6 kW</td>
</tr>
<tr>
<td>Average output current</td>
<td>32.23 A</td>
<td>12.89 A</td>
</tr>
<tr>
<td>$V_{C2}$</td>
<td>800 V</td>
<td>800 V</td>
</tr>
<tr>
<td>$C_{res}$</td>
<td>1.01 µF</td>
<td>403 nF</td>
</tr>
</tbody>
</table>

Table 6.2: Approximate computation of $C_{res}$

We may expect that the values for $C_{res}$ in table 6.2 are optimistic, i.e. rather low, for the following reasons:

1. In the computation, we have implicitly assumed that the resonant circuit caters exclusively to the three outputs. Of course, in a practical situation this will not be the case. The inputs of the converter need to be serviced as well.

2. We have neglected the current which, for AC operation, is needed to charge the filter capacitors.

3. We have neglected the turn-off time $t_q$ of the thyristors in equation 6.4.

4. As the shape of the resonant current pulses varies considerably with the voltages applied to the resonant circuit, the average pulse width is higher than $0.5/f_{res}$.

We can roughly assign weights to these four reasons, as follows:

1. If we assume the inputs to be serviced just as often as the outputs, we need twice as much current.

2. For a specific value of the power factor ($\cos(\phi)$) at the output, we need $1/\cos(\phi)$ times as much current.

3. For a turn-off time $t_q$ we need $(50\mu s + t_q)/50\mu s$ times more current.

4. The value for $C_{res}$ has been computed using the minimum pulse width of the resonant current. However, this width varies between this minimum and twice that value. If we take the average, we need another 1.5 times more current.

We can now compute adjusted values for $C_{res}$, which are shown in table 6.3. The values for $t_q$, $f_{res}$, and $\cos(\phi)$ anticipate the design of the other components of the power circuit somewhat. In fact, the design of the whole power circuit is of an iterative nature. For brevity, we will skip that aspect of the design, however.

With the values in table 6.3 as a first start, it is now possible to verify the power output of the two converters by simulation. We will return to that matter after a choice for some other circuit elements has been made.
<table>
<thead>
<tr>
<th></th>
<th>15 kW</th>
<th>6 kW</th>
</tr>
</thead>
<tbody>
<tr>
<td>$t_q$</td>
<td>15 $\mu$s</td>
<td>20 $\mu$s</td>
</tr>
<tr>
<td>$f_{res}$</td>
<td>10 kHz</td>
<td>8 kHz</td>
</tr>
<tr>
<td>$\cos(\phi)$</td>
<td>0.88</td>
<td>0.83</td>
</tr>
<tr>
<td>$C_{res(adjusted)}$</td>
<td>4.47 $\mu$F</td>
<td>2.41 $\mu$F</td>
</tr>
</tbody>
</table>

Table 6.3: Values for $C_{res}$, adjusted.

6.3 Filters

Both at the input and the output of the power converter capacitive filters are needed in order to minimize the high-frequency impedance of the source and load as 'seen' by the converter (see section 2.1.2). These capacitive filters are subject to two conflicting requirements. On the one hand, they present a low-impedance path for high frequencies, which implies that the converter 'sees' an environment with the characteristics of a voltage source. The same low-impedance property limits the amount of ripple voltage which is experienced by the environment. On the other hand, the filters should present a high impedance for the spectrum of the waveforms we like to generate with the converter. Otherwise we would spend an appreciable portion of the generated current only to charge and discharge the filters. We will try to find a compromise between these two requirements for the case of sinewave output voltages and maximum (resistive) load.

The worst case peak-to-peak ripple voltage $V_{rip}$ across a filter capacitor with value $C_o$ can be approximated by:

$$V_{rip} = 2VC_2 \frac{C_{res}}{C_o}$$ (6.5)

so the relative ripple $Ripp$ can be expressed as:

$$Ripp = \frac{V_{rip}}{2U_o} = \frac{VC_2}{U_o} \frac{C_{res}}{C_o} = \frac{VC_2C_{res}}{\tau_o I_o} = \frac{VC_2C_{res}}{\frac{2P_{out}}{3}U_o}$$ (6.6)

where $U_o$ indicates the amplitude of the sinewave output voltage. The amplitude $I_o$ of the total current supplied by the converter can be expressed as:

$$I_o = U_o \sqrt{\left(\frac{1}{R_o}\right)^2 + (\omega C_o)^2}$$ (6.7)

which implies that the ratio $\rho$ between the actual output current and its value without filter capacitor is given by:

$$\rho = \frac{I_o}{I_o(\text{no } C_o)} = \sqrt{1 + (\omega \tau_o)^2}$$ (6.8)
From equation 6.6 we obtain that the relative ripple is inversely proportional to the load time constant $\tau_o$. A large value for $\tau_o$ (i.e. a large filter capacitor) evidently lowers the ripple. Equation 6.8 shows that the total current rises with $\tau_o$. The compromise we have used for both converter types (using the values for $C_{res}$ from table 6.3) is shown in table 6.4.

<table>
<thead>
<tr>
<th></th>
<th>15 kW</th>
<th>6 kW</th>
</tr>
</thead>
<tbody>
<tr>
<td>$C_o$</td>
<td>180 $\mu$F</td>
<td>90 $\mu$F</td>
</tr>
<tr>
<td>$R_o$</td>
<td>9.6 $\Omega$</td>
<td>24.1 $\Omega$</td>
</tr>
<tr>
<td>$\tau_o$</td>
<td>1.7 ms</td>
<td>2.2 ms</td>
</tr>
<tr>
<td>Ripple</td>
<td>7.85 %</td>
<td>8.46 %</td>
</tr>
<tr>
<td>$\rho$</td>
<td>1.14</td>
<td>1.21</td>
</tr>
</tbody>
</table>

Table 6.4: Values for $C_o$, ripple, and excess current factor $\rho$

### 6.4 Final selection of $C_{res}$

With the values for $C_{res}$ from table 6.3 and for $C_o$ from table 6.4 simulation studies can be conducted in order to verify the power capacity of the converter. The results of the first set of these studies, for the 15 kW converter, have been depicted in figure 6.2.

The waveforms show the operation of the converter directly after turn-on. Especially the two lower traces, corresponding to the output power and estimated input power, show that with a value for $C_{res}$ of 3.0 $\mu$F the converter will not be able to supply the desired power. For $C_{res} = 3.5\mu F$ operation is only barely satisfactory (see the ripple on the output power signal during the first cycle of the output voltage). The difference in signals between $C_{res} = 4.0\mu F$ and $C_{res} = 4.5\mu F$ is only small. Therefore we have chosen to use $C_{res} = 4.0\mu F$.

Similarly, the startup of the 6 kW converter has been depicted for several values of $C_{res}$ in figure 6.3.

Anticipating somewhat with regard to the thyristors we will use for this design, we have used a resonant frequency of 8 kHz for this converter. The situations depicted in figure 6.3 show that the optimal value for $C_{res}$ here lies between 2.00 and 2.25 $\mu F$. Because of the components we had at our disposal, we have chosen to use the value of $C_{res} = 2.0\mu F$.

It is interesting to note that for both converters the optimum value for $C_{res}$ differs only little from the value given in table 6.3. This suggests that the common-sense approximations we have used to compute the values in table 6.3 can serve as good first estimates for the value of $C_{res}$ for a new design.
Figure 6.2: 15 kW converter: Simulated waveforms for four choices of $C_{res}$

\( t = 50\text{ms} \)

a) (Upper left): $C_{res} = 3.0\mu F$

b) (Upper right): $C_{res} = 3.5\mu F$

c) (Lower left): $C_{res} = 4.0\mu F$

d) (Lower right): $C_{res} = 4.5\mu F$

Traces:
Upper three: Output voltages
Middle six: In- and output currents
Lower two: Output power and estimated input power

6.5 Selection of thyristors

With the values for $C_{res}$ and $V_{C2}$ available, it is possible to compute the average and effective (rms) currents applied to the semiconductors. For normal operation, these values can easily be supplied by the simulation. We prefer to design the converter such that it will survive in a worst-case situation, however.

The (average, rms) current applied to a particular thyristor will be the highest if the following two conditions are satisfied:

- The resonant current has its highest (average and/or rms) value, and
- the sharing of the resonant current between multiple terminals is min-
Figure 6.3: 6 kW converter: Simulated waveforms for four choices of $C_{\text{res}}$
($t = 50\,\text{ms}$)

a) (Upper left): $C_{\text{res}} = 1.50\,\mu\text{F}$
b) (Upper right): $C_{\text{res}} = 1.75\,\mu\text{F}$
c) (Lower left): $C_{\text{res}} = 2.00\,\mu\text{F}$
d) (Lower right): $C_{\text{res}} = 2.25\,\mu\text{F}$
Traces as in fig. 6.2

imal, i.e. the full resonant current flows into this particular terminal.

These two conditions imply that the converter operates in a maximally unbalanced DC-DC context, i.e. all current flowing into one particular terminal is flowing out of one other terminal. Consequently, the voltage difference between these two terminals should approach zero. This kind of operation is possible if, with a DC source, maximum 'reactive' current is demanded at the converter inputs. The wave shapes of the resonant and thyristor currents in the mentioned worst-case situation have been depicted in fig. 6.4.

The effective and average values for the worst-case resonant current, $I_{\text{eff}}$ and $I_{\text{av}}$ respectively, can now be computed from the values for $t_q$, $C_{\text{res}}$, and the resonant angular frequency $\omega_{\text{res}}$ given before, as follows:

$$I_{\text{eff}} = \frac{1}{2} \sqrt{2 \omega_{\text{res}} C_{\text{res}} V C} \sqrt{\frac{\pi}{\pi + \omega_{\text{res}} t_q}}$$  \hspace{1cm} (6.9)
Figure 6.4: Worst-case currents in the resonant circuit and in the most heavily loaded thyristors

\[ I_{av} = \frac{2}{\pi} \omega_{res} C_{res} V_{C2} \frac{\pi}{\pi + \omega_{res} t_q} \]  \hspace{1cm} (6.10)

The values for the effective and average current in the most heavily loaded thyristors lie a factor $\sqrt{2}$ resp. 2 below these values.

Table 6.5 summarizes these and some other values for currents in the power circuit.

<table>
<thead>
<tr>
<th></th>
<th>15 kW</th>
<th>6 kW</th>
</tr>
</thead>
<tbody>
<tr>
<td>$I_{peak}$</td>
<td>201.1 A</td>
<td>80.42 A</td>
</tr>
<tr>
<td>$I_{eff}$ (simulated, full load)</td>
<td>100.6 A</td>
<td>40.65 A</td>
</tr>
<tr>
<td>$I_{av}$ (simulated, full load)</td>
<td>66.1 A</td>
<td>27.26 A</td>
</tr>
<tr>
<td>$I_{eff}$ (computed, worst case)</td>
<td>124.7 A</td>
<td>49.5 A</td>
</tr>
<tr>
<td>$I_{av}$ (computed, worst case)</td>
<td>98.5 A</td>
<td>38.8 A</td>
</tr>
<tr>
<td>$I_{theff}$ (simulated, full load)</td>
<td>29.2 A</td>
<td>12.0 A</td>
</tr>
<tr>
<td>$I_{thav}$ (simulated, full load)</td>
<td>5.9 A</td>
<td>2.0 A</td>
</tr>
<tr>
<td>$I_{theff}$ (computed, worst case)</td>
<td>88.2 A</td>
<td>35.0 A</td>
</tr>
<tr>
<td>$I_{thav}$ (computed, worst case)</td>
<td>49.2 A</td>
<td>19.4 A</td>
</tr>
</tbody>
</table>

Table 6.5: Values for currents in the resonant circuit and thyristors

The values in Table 6.5 show that the simulated current at full load in the resonant circuit is quite close to its computed worst-case value. The values for the thyristor current show a large difference, which is due to the fact that during normal (AC) operation the individual thyristors connected to a terminal each supply an equal part of the total current.

The problem which surfaces here is, that when we design the circuit for
sustained worst-case conditions, the thyristors and their cooling equipment will be vastly oversized for normal operation.

6.5.1 Thermal design

A partial solution to the problem mentioned above was devised as follows. The topology of the power circuit (see figure 6.1) shows that the resonant current is shared between the thyristors of all terminals. Therefore it might be expected that, whereas the power dissipated in a single thyristor may differ enormously between worst-case and normal operation, the power which is dissipated in the full stack of thyristors differs much less between these two conditions.

If we then use a common heat sink for the corresponding thyristors of each terminal (i.e. the thyristors connected to either the upper or the lower rail in fig. 6.1), this heat sink will have to drain more or less the same total heat both in the steady-state and in the worst-case, i.e. unbalanced situation.

A common heat sink implies the necessity to isolate the individual thyristors from the heat sink. For simplicity of the setup, we have used isolated thyristor modules. These modules each consist of two equal thyristors, with the anode of one thyristor connected to the cathode of the other. Both thyristors are isolated from the base plate of the module. Inspection of figure 6.1 shows that it is convenient to use one module for the thyristors with indexes 1 and 2 corresponding to one terminal, and another for the thyristors with indexes 0 and 3.

Two separate large heatsinks were used, one for the ‘upper’ 12 thyristors in fig. 6.1 and one for the ‘lower’ 12 thyristors. With these choices, the equivalent thermal network for one of these heatsinks becomes as indicated in figure 6.5.

In the worst-case situation, currents as shown in fig. 6.4 flow in two thyristors (not in the same module) per heat sink. Assuming a total dissipation per heat sink of $P_{tot}$ watts, i.e. $P_{th} = \frac{1}{2} P_{tot}$ watts per thyristor, the steady-state temperature difference between junction and ambient ($T_{ja}$) for this case follows from:

$$ T_{ja} = P_{tot} R_{thja} + \frac{1}{2} P_{tot} R_{thjc} + \frac{1}{2} P_{tot} R_{thch} $$

$$ = P_{tot} (R_{thja} + \frac{1}{2} R_{thjc} + \frac{1}{2} R_{thch}) $$

(6.11)

In the balanced situation, approximately the same power is dissipated in 12 instead of 2 thyristors. The temperature rise for this situation is given by:

$$ T_{ja} = P_{tot} R_{thha} + \frac{1}{12} P_{tot} R_{thjc} + \frac{1}{6} P_{tot} R_{thch} $$

$$ = P_{tot} (R_{thha} + \frac{1}{12} R_{thjc} + \frac{1}{6} R_{thch}) $$

(6.12)

6.5.2 Final thyristor selection

After some iterations, for both converters an isolated thyristor module was selected. The thyristor type and some important specifications are given in
Figure 6.5: Equivalent network for the heat flow from the thyristor junctions to the ambient

<table>
<thead>
<tr>
<th>Manufacturer</th>
<th>Semikron</th>
<th>Semikron</th>
</tr>
</thead>
<tbody>
<tr>
<td>Type</td>
<td>SKFT110/10DS</td>
<td>SKFT60/12DT</td>
</tr>
<tr>
<td>$t_g$</td>
<td>15 $\mu$s</td>
<td>20 $\mu$s</td>
</tr>
<tr>
<td>$R_{thjc}$ per thyristor</td>
<td>0.20 $K/W$</td>
<td>0.38 $K/W$</td>
</tr>
<tr>
<td>$R_{thch}$ per module</td>
<td>0.03 $K/W$</td>
<td>0.10 $K/W$</td>
</tr>
<tr>
<td>$W_p$ (worst case sine)</td>
<td>50 mJ</td>
<td>6 mJ</td>
</tr>
<tr>
<td>$P_{tot}$</td>
<td>769 W</td>
<td>72.7 W</td>
</tr>
<tr>
<td>$T_{jh}$ (worst case)</td>
<td>88.5 K</td>
<td>17.5 K</td>
</tr>
<tr>
<td>$T_{jh}$ (balanced)</td>
<td>14.7 K</td>
<td>2.9 K</td>
</tr>
<tr>
<td>$T_{jmax}$</td>
<td>125 C</td>
<td>125 C</td>
</tr>
<tr>
<td>Capacitance: parameter $n$</td>
<td>3.349</td>
<td>3.151</td>
</tr>
<tr>
<td>Capacitance: parameter $C_0$</td>
<td>1.646 nF</td>
<td>5.522 nF</td>
</tr>
<tr>
<td>Capacitance: parameter $V_0$</td>
<td>0.609 V</td>
<td>0.522 V</td>
</tr>
</tbody>
</table>

Table 6.6: Data for the two selected thyristor modules

The worst case value for the temperature difference between junction and heat sink ($T_{jh}$) for the SKFT110/10 thyristor indicates that, with the maximum junction temperature specified, only a (too) small temperature rise
of the common heat sink is allowed. This implies that this design cannot be used for extended periods in the worst-case situation, and the use of a larger thyristor would be appropriate. Nevertheless, as at the time of construction of this prototype the SKFT110/10 thyristor was the largest isolated module available, we have used this design as a test vehicle, taking care of not using it too long in an unbalanced situation. For the 15 kW prototype two force cooled heatsinks with a thermal resistance \( R_{thha} \) of approx. 0.05 \( K/W \) were used. The temperature rise of the heat sink \( T_{ha} \) then becomes 0.05 \( \times 769 = 38.5 \) \( K \). With an ambient temperature \( T_a \) of 25 C, and a maximum junction temperature \( T_j \) of 125 C, the maximum allowable power loss in a thyristor \( P_{th} \) then becomes

\[
P_{th} = \frac{T_j - T_{ha} - T_a}{R_{thj}c + 2 \times R_{thch}} = 237 \text{ W} \tag{6.13}
\]

Comparing this value for \( P_{th} \) with the total worst-case dissipation \( P_{tot} \) as given in table 6.6 shows that, even though a full asymmetry can not be applied for too long, the 15 kW power circuit can be subjected to rather large asymmetries for extended times.

Contrary to the above, the computation of the thermal resistance of the heat sink for the 6 kW prototype was a straightforward matter. Again using the values in table 6.6 and an ambient temperature of 25 C, the maximum thermal resistance \( R_{thha} \) can be computed from:

\[
R_{thha} = \frac{T_j}{P_{tot}} - \frac{1}{2}(R_{thj}c + R_{thch})
= \frac{100}{72.7} - \frac{1}{2}(0.38 + 0.10) = 1.15 K/W \tag{6.14}
\]

The length of heat sink which was needed to house the thyristors and snubbers already implied a lower value for \( R_{thha} \). No forced cooling was necessary here.

### 6.6 The resonant and commutating inductors

The value for the resonant inductance follows from:

\[
L = \frac{1}{\omega_{res}^2 C_{res}} \tag{6.15}
\]

If we assume that commutation takes a relatively small time compared to the complete resonant pulse, the value for \( L \) in equation 6.15 covers the sum of the resonant inductor \( L_{res} \) and two commutating inductances \( L_c \).

According to the analysis in section 5.2.2 a value of \( \sigma \) around 0.35 is to be preferred. The values for \( L_{res} \) and \( L_c \) can then be found from:

\[
\sigma = \frac{L_c}{L_c + L_{res}} \tag{6.16}
\]

\[
2L_c + L_{res} = L \text{ (from eq. 6.15)} \tag{6.17}
\]
which yields:

\[ L_c = \frac{\sigma}{1 + \sigma} L = 0.26L \quad (6.18) \]

\[ L_{res} = \frac{1 - \sigma}{1 + \sigma} L = 0.48L \quad (6.19) \]

A disadvantage of using these values for \( L_c \) and \( L_{res} \) is that commutation can, contrary to the assumption above, take a considerable amount of time. This implies that the operation of the Vpeak prediction circuit, which is based on a model of the power circuit without commutation at all, will be hampered somewhat. Furthermore the effective resonant frequency will be somewhat higher than predicted.

A low value for \( L_c \), on the other hand, gives rise to large values for \( di/dt \) around commutation. A relatively high value for \( L_c \) leads to smooth commutation waveforms, which implies that switching losses can remain low.

In view of the above we have used a relatively large value for \( \sigma \) in the 15 kW converter, which has rather high switching losses (compare the losses per pulse \( W_p \) for both converters in table 6.6), and a smaller value for the 6 kW prototype. The values used in the construction have been summarized in table 6.7.

<table>
<thead>
<tr>
<th></th>
<th>15 kW</th>
<th>6 kW</th>
</tr>
</thead>
<tbody>
<tr>
<td>( L )</td>
<td>63.3 μH</td>
<td>198 μH</td>
</tr>
<tr>
<td>( L_c )</td>
<td>15.0 μH</td>
<td>20 μH</td>
</tr>
<tr>
<td>( L_{res} )</td>
<td>33.3 μH</td>
<td>148 μH</td>
</tr>
<tr>
<td>( \sigma )</td>
<td>0.450</td>
<td>0.135</td>
</tr>
</tbody>
</table>

Table 6.7: Data for the commutation and resonant inductors

With the values of \( L_c \) and \( L_{res} \) and the associated rms currents the inductors can be designed. With regard to total cost, and to avoid saturation, toroid aircore inductors were used for both inductor types in both converters. Litz wire was used for most inductors to lower the copper losses due to skin-and proximity effects (see [86]).

For the design of the inductors two computer programs have been used. The first program, AIROC, which has been described in [10], computes the dimensions of an aircore inductor for given values of the inductance, the rms current, and the maximum temperature rise. It was found that the program gave good results for the value of the inductance. Using this program for the design of the inductors for the 15 kW prototype, we obtained the results of table 6.8.

For this converter, the resonant inductor has been built up from four parallel parts. The commutation inductances are shared between the four thyristors of every branch. The rms current has been chosen somewhat lower
Table 6.8: Design data for the commutation and resonant inductors for the 15 kVA converter

<table>
<thead>
<tr>
<th></th>
<th>$L_C$</th>
<th>$L_{res}$</th>
</tr>
</thead>
<tbody>
<tr>
<td>inductance</td>
<td>15.0 $\mu H$</td>
<td>132 $\mu H$</td>
</tr>
<tr>
<td>rms current</td>
<td>110 A</td>
<td>27.5 A</td>
</tr>
<tr>
<td>DC resistance</td>
<td>4.0 m$\Omega$</td>
<td>59.6 m$\Omega$</td>
</tr>
<tr>
<td>Quality</td>
<td>236</td>
<td>139</td>
</tr>
<tr>
<td>$P_{loss}$</td>
<td>48.4 W</td>
<td>45.1 W</td>
</tr>
</tbody>
</table>

than the worst-case value of table 6.5 because this converter will not be used at worst-case conditions for extended periods.

With the values of table 6.8, we obtain a total power loss (for the worst-case situation) in the inductors of $2 \times 48.4 + 4 \times 45.1 = 277$ Watt. For an output power of 15 kW this would indicate a relative loss of 1.85%.

A disadvantage of the program AIRC is that for every new design a new air-core (usually plastic material) needs to be manufactured. Also, the winding configuration cannot be chosen freely. Often the program outputs a rather thick winding, which implies that proximity losses will be relatively large, and that large variations between inductances may exist depending on who made the winding.

For the design of the inductors for the 6 kW converter we have therefore set up a new computer program LTORUS. This program uses a given core size, and tries to obtain a desired inductance with a winding consisting of two layers inside the toroid, and one layer outside. As the windings are very close to the core, hardly any freedom for the windings remains, which implies that variations between different makers will be small. An example of this configuration is given in figure 6.6.

The results of LTORUS for the inductors of the 6 kW converter are reported in table 6.9.

<table>
<thead>
<tr>
<th></th>
<th>$L_C$</th>
<th>$L_{res}$</th>
</tr>
</thead>
<tbody>
<tr>
<td>inductance</td>
<td>20.0 $\mu H$</td>
<td>148 $\mu H$</td>
</tr>
<tr>
<td>rms current</td>
<td>25 A</td>
<td>49.5 A</td>
</tr>
<tr>
<td>DC resistance</td>
<td>63.0 m$\Omega$</td>
<td>59 m$\Omega$</td>
</tr>
<tr>
<td>Quality</td>
<td>16</td>
<td>126</td>
</tr>
<tr>
<td>$P_{loss}$</td>
<td>39.4 W</td>
<td>144.6 W</td>
</tr>
</tbody>
</table>

Table 6.9: Design data for the commutation and resonant inductors for the 6 kVA converter

For this converter, a single resonant inductor has been used. Each thyris-
Figure 6.6: Example of the winding configuration of a toroidal aircore

tor has its own commutation inductances.

With the values of table 6.9, we obtain a total power loss (for the worst-case situation) in the inductors of $4 \times 39.4 + 144.6 = 302$ Watt. For an output power of 6 kW this would indicate a relative loss of 5.0%.

6.7 Snubbers

For both converters, the snubber configuration of figure 5.7 has been used. The values of the commutation inductances have already been given in tables 6.8 and 6.9.

The saturating inductors for the 15 kW converter have been built using medium-size ferrite toroids, by just shifting them on the appropriate connecting wires. This setup ensures minimal losses in the wiring, if wire lengths are used which are needed anyway. However, the restriction to a one-turn winding leads to a relatively large number of toroids per inductor, in order to obtain a reasonable value for the (unsaturated) inductance.

For the 6 kW converter again ferrite toroids were used, this time in a configuration with several turns per toroid. Using several turns, it is easy to obtain a large value for the unsaturated inductance. However, the inductor saturates at a proportionally lower current as well.

The design of the snubbers was tuned with the program DWDTH15, which has been described in section 4.5. For a number of combinations of $V_{LC1}$ and $V_{LC2}$ in the area defined in figure 2.9 the maximum values for the $dv/dt$ and the peak voltage applied to the thyristors were evaluated. It was found that
the highest values for both these variables occurred at the sharp corners of the triangle in figure 2.9, i.e. in situations where either $V_{LC1}$ or $V_{LC2}$ were close to zero. After some iterations the values in table 6.10 were obtained.

<table>
<thead>
<tr>
<th></th>
<th>15 kW</th>
<th>6 kW</th>
</tr>
</thead>
<tbody>
<tr>
<td>$L_e$</td>
<td>15.0 $\mu$H</td>
<td>20 $\mu$H</td>
</tr>
<tr>
<td>$C_d$</td>
<td>15 nF</td>
<td>10 nF</td>
</tr>
<tr>
<td>$R_d$</td>
<td>47 $\Omega$</td>
<td>100 $\Omega$</td>
</tr>
<tr>
<td>$L_s$: parameter $L_0$</td>
<td>87.1 $\mu$H</td>
<td>131 $\mu$H</td>
</tr>
<tr>
<td>$L_s$: parameter $k_0$</td>
<td>4.125 A</td>
<td>0.82 A</td>
</tr>
<tr>
<td>$L_s$: parameter $n$</td>
<td>1.69</td>
<td>1.75</td>
</tr>
<tr>
<td>$L_s$: number of turns</td>
<td>1</td>
<td>5</td>
</tr>
</tbody>
</table>

Table 6.10: Data for the snubbers

6.8 Consequences for the Vcpeak predictor

The designs up to here have been based primarily on the simplified model, which was presented in chapter 2. It has been argued there that several physical phenomena are not included in that model.

In this section we like to evaluate the consequences of some of these un-modelled phenomena for the operation of the Vcpeak predictor. For this purpose, we have used the most detailed simulation program DVDTH15, which carries the possibility to turn some of the phenomena on or off at will. The following phenomena can be studied individually:

- The non-linear thyristor junction capacitance (see section 5.3.2),
- the non-linear part of the snubber inductances (see section 5.3.1),
- the model for the stored charge in the thyristor junction (see section 5.3.3),

The snubber resistors and -capacitors ($R_d$ and $C_d$), and the nonsaturating part of the snubber inductances ($L_e$) are always present.

In the simulations, we have used both Vcpeak predictor types #1 and #2 (see sections 3.3.2 and 3.3.3 respectively).

With the three parameters which we can turn on or off, two different power modules, and two predictor types, we obtain 32 different situations to study. For brevity, we have restricted the presentation to a subset, as follows:

- Because we are interested mainly in trends, we will only consider the 6 kW power module,
• It was found that the behaviour of the predictor types #1 and #2 is almost identical, so we will only show the results for type #2.

The performance of the Vcpeak predictor circuits under realistic circumstances will be shown as contour plots, i.e., a 2-dimensional representation of a function of two variables. The values along the horizontal and vertical axes are the voltages applied to the resonant circuit (\(V_{LC1}\) and \(V_{LC2}\)). The plots are shown with the same orientation as figures 2.9 and 4.3.

The difference between \(V_{LC1}\) and \(V_{LC2}\) is limited on the one hand by equation 2.30, on the other hand by the applied grid voltages. It has been shown in figure 4.3 that the triangle defined by the grid voltages is used almost completely. Therefore we have decided to evaluate the performance of the predictors over a triangle which encompasses the area shown in fig. 4.3, but which lies inside the area shown in figure 2.9. A triangle with sides of 700 V proved adequate. The contours show the value of the capacitor voltage (in volts) after the simulation of one resonant halfcycle (\(V_{C2}\)), where the capacitor voltage at the start of the simulation (\(V_{C0}\)) was set to its nominal value (-800 V).

Due to the parasitic effects which we will incorporate one by one, the final capacitor voltage \(V_{C2}\) will not reach its intended value, which is 800 Volts here. The minimal value for \(V_{C2}\) computed over the triangle mentioned before can serve as a figure of merit for the performance of the Vcpeak predictor, and indicates roughly which safety margin on the peak capacitor voltage will be needed. Note that this figure of merit in principle does not predict what happens if the operation of the resonant circuit is initiated with a different value for \(V_{C0}\). However, we will assume in the following that the deviations on \(V_{C2}\) in those situations will be of more or less the same magnitude as the deviations computed here.

Figure 6.7 shows the performance of the predictor on the circuit with only linear (nonsaturating) commutation inductances and R-C snubbers present. In the worst situation, (lower right corner), the final capacitor voltage drops 71 Volts. As could be expected, this situation corresponds to very low values of \(V_{LC1}\) and \(V_{LC2}\). For these values, the commutation from the first to the second current segment takes relatively long.

The performance of the predictor drops even more if we incorporate the thyristor junction charge model in our simulation. As is shown in figure 6.8, in the worst-case situation the final capacitor voltage \(V_{C2}\) falls short of its intended value by ca. 83 Volts.

In the presence of saturable inductors, the final capacitor voltage \(V_{C2}\) drops only by about 8 Volts more than in the situation depicted in figure 6.7. This implies that the inductances we have used in the 6 kW converter, which saturate at a relatively low current (see table 6.10), have only a minor influence on the performance of this predictor type.

Figure 6.10 shows the performance of this predictor if the non linear thyristor junction capacitance is incorporated in the simulation. The minimum value for \(V_{C2}\) here again lies at 729 Volts. If we compare figure 6.10 with
Figure 6.7: Values for $V_{C2}$ (in volts) with predictor type #2, linear commutation inductances and R-C snubbers

Figure 6.8: Values for $V_{C2}$ (in volts) with predictor type #2, linear commutation inductances, R-C snubbers, and thyristor junction charge model

figure 6.7, then it becomes clear that the junction capacitance only influences
Figure 6.9: Values for $V_{C2}$ (in volts) with predictor type #2, linear commutation inductances, R-C snubbers, and saturating inductors

...the shape of the contours in a minor fashion.

Figure 6.10: Values for $V_{C2}$ (in volts) with predictor type #2, linear commutation inductances, R-C snubbers, and nonlinear thyristor junction capacitance
Figure 6.11: Values for $V_{C2}$ (in volts) with predictor type #2, linear commutation inductances, R-C snubbers, thyristor junction charge model, saturating inductors, and nonlinear thyristor junction capacitance.

To finish up the presentation of the predictor performance, figure 6.11 shows the consequence of the combined effect of the four parasitics. Combined, the parasitics cause the prediction of $V_{C2}$ to go wrong for 89 volts, which equals ca. 11%.

6.9 Discussion

Contrary to the situation with the DC-DC series-resonant converter, explicit design rules for the multiphase series-resonant converter are not available. Therefore we must rely on a rough approximation in order to find initial parameters for the circuit elements with the correct order of magnitude. It has been shown that the common-sense approach which we have applied supplies a value for the resonant capacitor which is correct within ca. 10%.

This value is then used to design the filters in a first approximation. Both the values for the resonant and filter capacitors can be fine tuned using more or less detailed simulation programs. The detailed simulation is also needed for the design of the snubber circuits.

After a final selection for the parameters of the resonant circuit has been made, values for currents in the resonant circuit and the individual thyristors can be computed. Here a large difference shows up between the current stresses during normal operation of the converter and in a worst-case, maxi-
mally unbalanced situation. For the construction of our prototype, we prefer to design the circuit such that it can withstand even the worst-case situation. With the components available at the time of construction, this was not possible for the 15 kW converter.

An important aspect of the design of the whole converter system is the performance of the innermost control loop, i.e. the \( V_{\text{cpeak}} \) predictor circuit. As the model which was used to design the predictor does not include parasitics, we may expect that the peak capacitor voltage will not be kept as constant as we would like. Simulations, which cover the full operating range of the converter, show that in the worst-case situation the peak capacitor voltage drops about 11%. This value falls within the safety margin of 20% which we have used for the determination of the peak capacitor voltage.

**Another approach to the \( V_{\text{cpeak}} \) predictor**

The simulation results presented in figures 6.7...6.11 show that under certain circumstances (voltages applied to the resonant circuit) the peak capacitor voltage can drop considerably below its intended value. The reason for this behaviour lies in physical phenomena concerning the thyristor charge control model and the commutation. These phenomena were not incorporated in the simplified model which has been used for the design of the \( V_{\text{cpeak}} \) predictor.

An important aspect of the observed behaviour with respect to the peak capacitor voltage of the converter is that it, even though the circuit is non-linear and complex, is almost completely deterministic. The only disturbances are the output current and the (slopes of the) input voltages (see figure 3.2), which both can be estimated fairly accurately. This observation suggests that it might be possible to compute the 'ideal' control action for a certain combination of \( (V_{L_{C1}},V_{L_{C2}}) \) off-line, using a model as detailed as we would care to. The operation and design of such a predictor is further discussed in appendix B.
Chapter 7

Design and Realization of the Control Electronics

The function of the control electronics is to perform measurements of setpoints, actual values and the internal state of the power converter, in order to generate signals which will drive the converter according to the control objectives which have been formulated in section 3.1.

The algorithms which the control electronics should perform have been described in chapter 3. These algorithms show a high degree of symmetry with regard to the treatment of in- and outputs (see for example figure 3.9), to the number of terminals of the converter (see figure 2.10), and to the number of power modules (see section 3.7) in a paralleled system. One of the basic problems we have tried to attack in this work (see section 1.3) is how to exploit this symmetry. In principle, the symmetry allows us to design hardware which can control a converter with any number of terminals and any number of paralleled modules.

The actual realization of the control electronics can be performed in many ways. The most important choice to be made is how the signals will be presented in the control circuit: as analog or digital (discretized) quantities. An attractive feature of the latter implementation, using a digital signal processor (DSP), would be that the control algorithms can be implemented in software, and therefore easily changed if the need arises. However, the use of digital signal processing also has some distinct disadvantages:

- At the time the first (15 kW) prototype was constructed, digital hardware still was rather expensive. Especially fast A/D converters were costly components.

- For the implementation of a control structure in software, tools (like hardware debuggers and logic analyzers) and experience with this kind of setup are needed. Neither the experience nor the tools were available in our laboratory when the construction of the prototype was started.
Using a DSP solution would therefore need the setting up of a completely new laboratory environment for this kind of hardware. However, the goal of this research project was to develop a new power circuit and new control algorithms. As it promised to be feasible to implement the control concepts in “classical” hardware, we have opted for that solution in order to save time.

The considerations above are dependent on time: hardware prices have been changing considerably, and tools for software development are much more available now than seven years ago. Probably, a new design of the control circuit would look very different from the circuit we are going to present here. Still, the “classical” design which we have adopted gets the job done, and that is what was and is our greatest concern.

The control concepts have been implemented in two versions: a first one which has served for the control of the 15 kW converter, and a second implementation for the 6 kW converter. Although the basic concepts for current-, voltage-, and Vpeak control are essentially the same between these two versions, the implementations are quite different. Also, in the electronics for the 6 kW converter the possibility to perform phase-staggering control has been added.

In the following, we will concentrate on the ‘newest’ version of the control electronics, i.e. for the 6 kW converter, and only refer to the older implementation to illustrate some specific changes.

Outline

The scalability in two dimensions (number of terminals and number of modules) of the power circuit allows us to view the converter as a sort of matrix. This matrix structure allows a rather direct mapping of the control concepts onto the control hardware, which will be discussed in section 7.1.

The column index of the matrix structure indicates a particular input or output terminal of the converter. The tasks which are specific to one column are discussed in section 7.2. Similarly, the tasks which are specific to a row, i.e. to one single module, will be treated in section 7.3.

Section 7.4 discusses the electronics which is specific to both one module and one terminal. This concerns mainly the decoding and bookkeeping associated with four thyristors.

Where possible, we will try to implement the control hardware in a distributed manner, in such a way that as little as possible difference needs to exist between the control circuits for the individual terminals and modules. If this desire is implemented in rigor, the central (supervising) controller, which is presented in section 7.5, can perform its task without knowledge of the number of modules and the number of terminals actually implemented (or switched on).

To finish up the presentation of the electronics, some waveforms appearing in the circuit are shown in section 7.7.
A word on scaling and notation

The control electronics has been implemented using analog and digital circuitry running of supplies of \( \pm 15 \) and \(+5\) volts respectively. Clearly, the voltage ranges indicated here are too low to use the signals which occur in the power circuit of the converter directly. Therefore, the electronics uses scaled versions of the measured voltages and currents.

With this scaling, every voltage and current in the circuit occurs twice: the ‘true’ and the scaled version. For the simplicity of notation, we have used the same symbol for both values. In most cases, the formulas concerning the scaled quantities are equal to the formulas with the true values, as the scaling factors divide out on both sides. Only for the scaling factors for currents vs. voltages care needs to be taken: this matter is discussed in section 7.3.2, starting at equation 7.9.

7.1 Matrix structure

The multiphase multimodule converter system which we like to control has been depicted schematically in fig. 7.1.

![Diagram of a converter system consisting of multiple paralleled power modules](image)

Figure 7.1: Converter system consisting of multiple paralleled power modules

We assume the individual power modules to be exact copies of each other. Both the number of modules and the number of terminals (6 in fig. 7.1) can vary. The structure of the control electronics for this ‘flexible’ power circuit will therefore need a similar freedom. For this purpose, we like to see the control circuit as a matrix, where the number of rows equals the number of paralleled modules, and the number of columns equals the number of (input- and output) terminals. The control matrix which would correspond to the power circuit of figure 7.1 for 3 modules has been depicted with the boxes marked c in fig. 7.2.

The indexes of the matrix are the module number (1...3) and the input/output number (we will use either r...w or 1...6), respectively. In figure...
Figure 7.2: Matrix representation of control electronics for a three-input, three-output, three module converter

7.2 we have added both a row (boxes with a) and a column (boxes with b) to the control structure. The box which is common to both the extra row and column has been marked with d. The tasks which the control electronics should perform can now be distinguished as follows (the letters correspond to the boxes in figure 7.2):

a) Tasks which are local to one input or output terminal of the converter,

b) Tasks which are local to one converter module,

c) Tasks which are subject to both a) and b),

d) Tasks which apply to the complete converter system.

For the implementation we would like to view the entries (boxes) in the matrix as individual printed circuit boards (PCB’s), which are identical for identical marks in fig. 7.2. The following PCB’s can then be distinguished:

a) Terminal board

b) Module board

c) Thyristor board

d) Central control board.

The more detailed treatment of the implementation in sections 7.2 ... 7.5 will show that it is not practical to use exactly one PCB per function. However, we will try to come as close as possible to this situation, because it will greatly simplify an expandable implementation. The structure in fig. 7.2 also shows the communication between the circuit boards.
7.2 Tasks local to a terminal (a)

7.2.1 Measurements of voltage and current

Measurement circuits are used to generate a scaled copy of a certain quantity for use in the control electronics. For convenience of processing the values of the measured voltages and currents are brought into the range of ±10 Volts. The terminal voltage is scaled with a simple differential amplifier. The voltage scaling factor will be further denoted by $A_u$, so for the scaled version $U_{x,sc}$ of any measured voltage $U_x$ the following holds:

$$U_{x,sc} = A_u U_x$$  \hspace{1cm} (7.1)

Because of the relatively low amount of common-mode noise an instrumentation amplifier setup was not needed.

The unfiltered terminal currents were measured using commercial 'DC-transformers' [58], which internally use a feedback configuration to balance a magnetic circuit. The bandwidth of these devices is specified to lie at 100 kHz. This implies that these devices should not be used for timing purposes, as an appreciable phase lag could already be present at the resonant frequency. The output current of these devices is converted to a voltage by a terminating resistor $R_{tr}$, such that for the scaled version $I_{x,sc}$ of a measured current $I_x$ the following holds:

$$I_{x,sc} = R_{tr} \frac{I_x}{N_{tr}}$$  \hspace{1cm} (7.2)

with $N_{tr}$ the winding ratio of the transformer. Note that $I_{x,sc}$ has the dimension of a voltage.

7.2.2 Voltage and current control

As has been described in section 3.4 the individual terminals can be either current or voltage-controlled. In the following we will assume the outputs of the converter to be subject to voltage control, and the inputs to be current-controlled. For convenience, we will try to use a circuit which is able to perform both functions, and configure the circuit board according to the place (input or output) where it is used.

As has been shown in section 3.4, for the control of current an integrator circuit is used to generate the time integral of the difference between the (unfiltered) terminal current and its reference value. For voltage control an operational amplifier is used to obtain the difference between the terminal voltage and its setpoint. Depending on the particular control mode desired, one of these signals is processed further. A simplified schematic of the setup we have used is depicted in figure 7.3.

The choice for voltage or current control is made by means of a digital signal (U/I ctrl), emanating from a hand-operated switch. This signal is processed by some logic in order to select either switch SW1 or switch SW2 in the schematic.
The lower part of the circuit is used to solve a special problem which may arise both in the current- or voltage controlled situation. If under current control the load would be disconnected, then the output voltage could possibly become very high. Alternatively, for example due to malfunctioning of another part of the circuit, the first control stage could be supplied with an unsafely large value for the voltage reference. The lower two branches in the circuit of figure 7.3 compute the difference of the actual voltage with precribed upper- and lower bounds. The signs of these signals, which are produced by the two comparators Comp1 and Comp2, indicate whether the terminal voltage is still within bounds. If the voltage goes out of bounds, then switch SW1 or SW2 is opened and the appropriate switch (SW3 or SW4) is closed. This implies that the terminal effectively becomes voltage-controlled, with reference either $U_{max}$ or $U_{min}$. As soon as the voltage gets within bounds again, normal current or voltage control is resumed.

### 7.2.3 P-I controllers and bounds check

In figures 3.5 and 4.5 it has been shown that the actual error signal which has been obtained from the voltage- or current controller gets more or less
Tasks local to a terminal (a) 115

confined to a range between an upper and a lower bound. For smooth operation of the complete system the distance between these bounds needs to be larger than the equivalent of the maximum charge displaced by one resonant halfcycle. The traces of the error signal in figures 3.5 and 4.5 show that, for a particular type of loading of the converter, the actual error signals tend to remain close to one of the two bounds. This implies that a steady-state difference will occur between the generated quantity and its setpoint. In order to remedy this the error signal, before further processing, is shaped by a proportional-integral (P-I) section, which has been shown in figure 7.4.

![Diagram](image)

Figure 7.4: Setup of the PI-controller for the current or voltage error signal

The integral part of this section will force the mean value of the error signal to become zero. The modified error signal will, under normal operating conditions, only deviate from zero by approximately half the distance between the upper and lower bounds. Therefore the range of the integral action of the P-I controller can be limited to this amount, which is useful to prevent large control actions to take place directly after startup of the converter or after an overload condition. In fact, in order to prevent wind-up, the state of the integrator should be limited.

7.2.4 In-phase references

We will define in-phase current references as references which when acting alone would give rise to a power factor of unity at the input of the converter. We will define the input power factor $P_f$ using the multiphase approach of Buchholz (see [18, 19]) in a time-local setting (see [1, 38]):

$$P_f = \frac{\sum_{j=1}^{n} i_j u_j}{\sqrt{\sum_{j=1}^{n} u_j^2 \sum_{j=1}^{n} i_j^2}}$$  \hspace{1cm} (7.3)

Using this definition, in-phase references can be easily generated:

$$i_{refk} = \frac{P u_k}{\sum_{j=1}^{n} u_j^2}$$  \hspace{1cm} (7.4)
where $\mathcal{P}$ is an estimate for the input power which we will assume here to be available. If we want to implement this equation for several terminals of the converter in a modular fashion, both the multiplication in $\mathcal{P}u_t$ and the evaluation of the $u_j^2$ can be done at the terminal level. The summation of the $u_j^2$ and the division in equation 7.4 need to be performed over all input terminals. We have used an analog summing junction with one operational amplifier and an analog multiplier to perform this task. These components are situated on the central control board. The setup has been depicted in figure 7.5.

\[ P \]

\[ U_r \quad I_{refr} \]

\[ U_s \quad I_{refs} \]

\[ U_t \quad I_{reft} \]

Figure 7.5: Circuit for the computation of the in-phase current references

### 7.2.5 Quadrature references

For a three-phase to three-phase converter four degrees of freedom are left over of the initial six after the constraints on current (see section 3.6.1) and power flow (see section 3.6.2) have been catered to. Normally three of these four degrees of freedom are used to specify the three output voltages or currents. The one degree which is left over can be used to advantage to generate or consume a controlled amount of 'reactive' power. For a converter with three inputs $r$, $s$, and $t$ a set of reactive current references can be defined as follows:

\[ i_{refr} = \mathcal{G}(U_s - U_t) \]  
\[ i_{refs} = \mathcal{G}(U_t - U_r) \]  
\[ i_{reft} = \mathcal{G}(U_r - U_s) \]

where $\mathcal{G}$ signifies the desired 'admittance' of the converter input for reactive current. We have applied the concepts of reactive current and power somewhat loosely here: with the definitions of equations 7.5...7.7 we could even obtain 'reactive' DC currents. The reference currents as defined in equations
7.5 ... 7.7 are reactive in the sense that the sum of the powers associated with these currents is zero:

\[
P_{refr} + P_{refs} + P_{refl} = U_r i_{refr} + U_s i_{refs} + U_t i_{refl} \\
= U_r G(U_s - U_t) + U_s G(U_t - U_r) + U_t G(U_r - U_s) \\
= G(U_r U_s - U_r U_t + U_s U_t - U_s U_r + U_t U_r - U_t U_s) \\
= 0 \quad (7.8)
\]

In the case of a symmetric three-phase AC source our 'reactive' current references represent the well-known out-of-phase currents. Note however, that the sign of \( G \) corresponds to 'inductive' or 'capacitive' behaviour only for a certain phase sequence. Also, contrary to, say, a load composed of three star-connected inductors, the reactive admittance \( G \) is independent of the frequency of the source.

For the electronic implementation of equations 7.5 ... 7.7 the scaled 'neighbour' voltages of a particular terminal are fed to its circuit board, and an analog multiplier is used to compute the reactive reference. The setup has been depicted in figure 7.6.

![Circuit for the computation of the quadrature current references](image)

Figure 7.6: Circuit for the computation of the quadrature current references

### 7.2.6 Power and offset control processing

For the implementation of the power controller we need to compute the excess energy \( E_{ex} \) which has been defined in equation 3.17:

\[
E_{ex} = \sum_{k=1}^{n} \text{ASD}_k u_k
\]

The product \( \text{ASD}_k u_k \) can be computed for every terminal individually, and like before summed by means of an analog summing junction with an operational amplifier on the central control board. The setup has been depicted in figure 7.7.
The offset control processing is implemented similarly. However, no multiplying action is needed here. The individual error signals are fed to one more operational amplifier summing junction. The output of this operational amplifier, which is situated on the central control board, is fed back to extra inputs on the terminal control boards in order to close the control loop.

### 7.2.7 Sum of errors

The central control board watches the sum of absolute errors of the terminal boards in order to decide when to initiate a new current pulse. The errors of the individual terminals are rectified and fed to a summing junction. The resulting signal is further processed on the central control board. The setup has been depicted in figure 7.8.

Figure 7.7: Circuits for the power- and offset control

![Circuits for the power- and offset control](image)

Figure 7.8: Circuit for the computation of the sum of absolute errors

![Circuit for the computation of the sum of absolute errors](image)
7.2.8 Voltage and error signal switch matrix

For the terminal selection process which has been described in section 3.5 it is necessary that the voltages and error signals of the individual terminals can be compared against each other. At least two basic setups are possible here:

a) At the start of the selection process, compare all of the \((n + m)\) signals against the \((n + m - 1)\) others. The digital results of the comparisons can then be stored in a memory bank, and used when needed. This approach uses at least \(\frac{1}{2}(n + m)(n + m - 1)\) comparators and memory cells.

b) Compare only those signals which are needed during the selection process. Only one comparator per comparison is needed, plus a bus structure which allows the individual voltage or error signals to be fed to the comparator.

Both setups have been built and used in the two subsequent versions of the control electronics. For simplicity of decoding and wiring the first variant has been implemented with a full \((n + m) \times (n + m)\) matrix of comparators and memory cells. The simplified schematics of both setups have been depicted in figures 7.9 and 7.10, respectively.

![Figure 7.9: Setup of selector with a comparator matrix. The arrows indicate signals which are used in the digital controller](image)

We found that a disadvantage of a) is that a lot of backplane wiring is needed. The circuit in b) uses very little wiring (the control signals for the switches can be generated on the circuit board itself), but is sensitive to the settling time of the switched analog signals on the buses and needs a fast
comparator. As circuit a) communicates with the selection arbiter on the central control board by means of a digital bus, the settling time restraints are much less severe here.

Another difference between the circuits is that the comparator/memory bank in a) restricts the total number of terminals \((n + m)\) to a maximum. The particular bus structure of implementation b) allows in principle any number of terminals to be added.

It was found that the highest clock frequency attainable with both implementations was almost equal, ca. 2 MHz.

7.3 Tasks local to a module (b)

7.3.1 Measurements in the resonant circuit

The resonant circuit is the core of the whole conversion system. For proper operation of the control circuit the state of the resonant circuit, i.e. the pair \((I_{res}, V_C)\) needs to be measured. The setup is similar to the measurements of the terminal voltage and -current. However, the value of \(I_{res}\), which contrary to the terminal currents is a high-frequency pure AC current, can be measured with a small current transformer. The terminating resistors and the winding arrangement are again chosen such that the scaled value lies in the range of \(\pm 10V\).
7.3.2 Predictor circuit

Two basic types of predictor have been built and used in two versions of the control electronics.

Predictor type #1

The first type, whose principle has been discussed in section 3.3.2, computes the distance from the trajectory of the state of the resonant circuit during the first current segment to the centre of the trajectory of the second current segment. The condition to test for has been given in equations 3.5 and 3.6. These equations are mathematically equivalent, but have some different consequences for an implementation. The implementation of equation 3.5 needs one more analog multiplier than the implementation of equation 3.6. However, close inspection of the signal levels involved in the latter reveals that the dynamic range of this implementation can be only half as large as in the former. A trade-off needs to be made here between component count and cost versus signal to noise ratio. The implementation according to equation 3.6 has been discussed in detail in [29, 26, 37], and will not be covered here.

The derivation which led to equation 3.5 is valid only for positive values of the current in the resonant circuit \( I_{res} \). However, it is easy to ‘fool’ the predictor into believing that \( I_{res} \) is always positive, if we feed it with \( +I_{res} \) during the positive resonant halfcycles, and with \( -I_{res} \) during the negative resonant halfcycles. This setup corresponds to ‘turning around’ the resonant circuit, which implies that the values of \( V_C \) and \( V_{LC2} \) need to be treated similarly.

For the implementation according to equation 3.5 we want to derive a condition for turnover to the second current segment specified in the signals which are present in the control electronics. Starting with equation 3.5 the following derivation applies:

\[
\frac{(Z_{res} I_{res})^2}{(Z_{res} I_{resc} N_{tr})^2} < \left( \frac{V_{C2} - V_{LC2}}{V_{C2sc} - V_{LC2sc}} \right)^2 - \left( \frac{V_C - V_{LC2}}{V_{Csc} - V_{LC2sc}} \right)^2 \Rightarrow \frac{A_u^2}{(Z_{res} N_{tr} A_u)^2} \tag{7.9}
\]

\[
\frac{I_{resc}^2}{R_{tr}^2} < \left( \frac{V_{C2sc} - V_{LC2sc}}{V_{Csc} - V_{LC2sc}} \right)^2 \left( \frac{Z_{res} N_{tr} A_u}{(Z_{res} N_{tr} A_u)^2} \right)^2 \tag{7.10}
\]

Here the signals with the subindex \( sc \) represent the scaled (measured) values of the corresponding non-indexed signals. Comparing equations 7.9 and 7.11 it can be concluded that for the computation of the switchover condition we can use the scaled versions of voltages and currents instead of the unscaled versions if the following equation holds:

\[
R_{tr} = Z_{res} N_{tr} A_u \tag{7.12}
\]

In this equation, \( Z_{res} \) is determined by the desired power level and frequency of the converter. The voltage scaling factor \( A_u \) depends on the maximum
value of the capacitor voltage \(V_C\) and the signal range in the analog electronics (in our implementation \(\pm 10V\)). The value of \(N_{tr}\) can be chosen as large as is considered practical (several hundred turns typically) and \(R_{tr}\) can then be computed.

Besides the scaled values of \(V_C\) and \(I_{res}\), the predictor circuit also needs the final value of the capacitor voltage \(V_{C2}\) and the voltage which will be applied to the resonant circuit during the second current segment \(V_{LC2}\). The former can be set to any desired value as long as equation 2.25 is satisfied. The latter can be constructed, assuming the switching algorithm is known, from a combination of the terminal voltages.

**Predictor type #2**

As has been discussed in chapter 3, a second predictor implementation could rely on the condition given in equation 3.8. However, the assumption that \(V_{C0}\) (the capacitor voltage at the beginning of the resonant pulse) is exactly minus \(V_{C2}\) (the capacitor voltage at the end of the pulse), which was used in the derivation of that equation will in general not be valid in a practical circuit. Therefore we have made a more complete derivation of the value of \(V_{C1}\), without assuming that \((V_{C0} + V_{C2}) = 0\). The derivation results in a value for \(V_{C1}\) given by:

\[
V_{C1} = \frac{V_{C2}(V_{C2} - 2V_{LC2}) - V_{C0}(V_{C0} - 2V_{LC1})}{2(V_{LC1} - V_{LC2})} \tag{7.13}
\]

In this equation only voltages are used to derive the condition for turnover, which implies that scaling problems like those discussed for predictor type #1 need not occur here. As was the case for predictor type #1, the circuit is fooled into believing that \(I_{res}\) is always positive. For this purpose both \(V_C\) and \(-V_C\) are measured, and the appropriate value is connected to the predictor circuit. As before, \(V_{LC1}\) and \(V_{LC2}\) can be constructed from a combination of the terminal voltages. The setup of the circuit for positive \(I_{res}\) has been depicted in figure 7.11.

The value of \(V_C\) at the beginning of the current pulse, \(V_{C0}\), is stored in a sample and hold circuit which is governed by the digital controller. A small (negative) offset is added to the values of \(V_{LC1}\) and \(V_{LC2}\) in order to compensate for resistive damping in the resonant circuit and voltage losses in the thyristors (see section 3.8.1). The two products in the denominator of the right hand side of equation 7.13 are computed by the two analog multipliers. A third analog multiplier, which is configured as a two-quadrant divider, is used to compute \(V_{C1}\), the assumed value of the capacitor voltage at the instant of turnover to the second current segment. Finally, the value of \(V_{C1}\) is compared against the actual value of the capacitor voltage. The result of this comparison is used in the digital controller to indicate when the turnover to the second current segment should be initiated.
7.3.3 Compensation signals for phase-staggering

In section 3.7 it has been shown that parasitic synchronization of paralleled power modules under ASDTIC control can be avoided if an adequate compensation is added to the real error signal. Three shapes of this compensation are needed:

- For a terminal which receives the full resonant pulse,
- for a terminal which receives only the first current segment, and
- for a terminal which receives only the second current segment.

As the currents in the latter two terminals flow in a direction opposite to the current in the first terminal, inspection of figure 3.14 shows that the sum of the compensation signals will be zero. The circuit implementation has been shown in figure 7.12.

In the circuit, first the compensation signal \( \text{comp}_0 \) for the full positive resonant pulse is computed as

\[
\text{comp}_0 = V_{C2} - V_C
\]
Inspection of figure 3.14 shows that during the second current segment, the compensation signal $\text{comp}_2$ for the terminal receiving only the second current segment is (apart from the sign) equal to $\text{comp}_0$. The value for this signal during the first current segment is constant, and is given by

$$\text{comp}_2 = V_{C_2} - V_{C_1} \quad (7.15)$$

An analog toggle switch, whose position is governed by the module state machine (either first or second current segment), selects between the two possibilities.

The values for $\text{comp}_0$ and $\text{comp}_2$ computed here are only valid for positive current flowing into the respective terminal. For negative current both signals need to be inverted. This function is indicated symbolically with the two multipliers, which are governed by a signal which indicates whether the current in the terminal receiving the complete resonant current pulse is positive or negative.

Finally, the value for $\text{comp}_1$ is computed from the values of $\text{comp}_0$ and $\text{comp}_2$.

The three compensation signals are wired to the boards which connect to the four thyristors of one terminal of one single power module (c in figure 7.2). On these boards, the appropriate one of the three compensation signals, or zero for a non-active terminal, is switched through to the current control board, where it is fed into an extra input (analog summing junction) of the PI-controller.

### 7.3.4 Predictor state machine

Local to a power module, some bookkeeping is needed to indicate the phase (first or second current segment, or no current) of its operation. For this purpose, we have used a state machine with four states (two bits), assigned as indicated in table 7.1.

<table>
<thead>
<tr>
<th>State</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>00</td>
<td>No current flow, and all thyristors safe</td>
</tr>
<tr>
<td>01</td>
<td>First current segment active</td>
</tr>
<tr>
<td>10</td>
<td>Second current segment active</td>
</tr>
<tr>
<td>11</td>
<td>No current flow, and not all thyristors safe</td>
</tr>
</tbody>
</table>

Table 7.1: State assignment for the predictor state machine

The most important state transitions are indicated in the diagram in figure 7.13.

Essentially the module receives the command to start a new current pulse from the central control (to be discussed in section 7.5), then runs on its own until the pulse is finished. For the next pulse, it supplies a signal to the
Figure 7.13: State transition diagram for one module

central control which indicates whether it is ready to start a new pulse (i.e. whether the state is equal to 00) or not.

7.4 Tasks local to both module and terminal (c)

7.4.1 Thyristor decoding

Of the four thyristors connected to one terminal of one power module, either one or none is conducting. Which thyristor needs to be turned on depends on a variety of parameters. These include:

- Will the terminal be used (for this particular resonant halfcycle) at all?
- The direction of the resonant current
- The desired direction of the current in the terminal
- Are we considering the first or the second current segment?
- To which of the three nodes (a, b, or c in figure 3.8) is the terminal connected?
- What is the sign of the voltage difference between this node and the central node (a)?

For every combination of answers to the questions above, it can be derived which (if any) thyristor of the four needs to be turned on. We have used a programmable device (EPLD, see [2]) to store the tables for the four thyristors.
7.4.2 Thyristor memory

In section 3.3 it has been pointed out that the state (on or off) of a thyristor can not be measured directly, but must be estimated using an observer structure. This structure, usually denoted as the 'Thyristor memory', is implemented as follows. The one-bit memory cell is set as soon as the thyristor in question receives a gate pulse. After the current through a thyristor has become zero, a certain time, the turn-off time \( t_q \), needs to elapse before the device can withstand a forward voltage again. For a specific device, the value of \( t_q \) is given by the manufacturer.

In our circuit, we have used an analog timer device to check for this time interval. If a reverse voltage (back-bias) has been applied to the thyristor for a time longer than \( t_q \), then the thyristor is considered to be able to sustain forward voltage again, so the memory cell can be reset. For this purpose, the voltage across the anode-cathode terminals of the thyristor is measured with a special floating amplifier (back-bias detector), and its polarity transferred to the control circuit through an isolating opto-coupler or glass fibre link.

If, for whatever reason (such as during start-up), insufficient reverse voltage is applied to the thyristors, the control circuit would be waiting indefinitely. Therefore we have added a second timer, which, if needed, resets the thyristor memories after the time equivalent of ca. 10 resonant halfcycles.

7.4.3 Pulse amplifiers

The control signal which indicates that a particular thyristor needs to be fired, needs to be isolated, amplified, and shaped before it can be fed into the gate of the thyristor.

The isolation has been performed using opto-couplers or glass fibre links. The power to the isolated (floating) part is supplied by means of a small high-frequency transformer, which on the primary side is connected to a square-wave power inverter. Experience has shown that such transformers can be constructed with interwinding capacitances as low as 5 \( pF \), which implies that the common-mode currents through this path can be kept acceptably low. The power consumption of the combination of memory and pulse amplifier lies in the range of 2-4 Watt.

Especially at the start of the resonant pulse, simultaneous triggering of the two thyristors involved in the current flow needs to be ensured. For simultaneous triggering a steep firing pulse is advantageous. The shape of the current flowing into the thyristor gate has been depicted in figure 7.14.

The first sharply rising part of the pulse is due to the discharging of an RC-series circuit. The tail is supplied by a higher resistance value connected to a positive supply. The voltage and impedance of the supply have been chosen such that during both the first and the second part of the gate pulse adequate triggering conditions for the thyristor are ensured, and that the gate dissipation remains below its allowable maximum.
If the thyristor needs to be in the off condition, a negative voltage bias of several volts is applied to the gate. Under this condition, turn-off of the thyristor can be performed in a shorter time and sensitivity to forward $dv/dt$ is lowered.

7.5 The central digital controller (d)

Now that the individual tasks have been discussed, the question naturally arises how these can be made to cooperate in an orderly fashion. It has already been pointed out that, ideally, the central coordinator should not need to ‘know’ how many terminals or how many modules the converter consists of.

For the implementation of this idea we have resorted to a daisy-chain architecture, both for the terminals and the modules. At the start of an operation, the central controller supplies a token to the first terminal (or module), which, after it is ready with processing, hands it over to its neighbour. The last terminal (or module) returns the token to the coordinator, which then continues with its next step. As long as the token does not get lost, this scheme runs fine.

At every instant, two tokens are in the game: one which is carried through the terminals, and one which is carried through the modules. In the following we will use the terms active terminal and active module to point at the terminal or module which contains the token at a particular moment.

Both daisy-chains consist basically of D-flipflops connected in series, i.e. a shift register divided over several circuit boards. The D-flipflops are implemented as a part of the programmable logic already present on the circuit boards.

7.5.1 Line selector

The line selection algorithm has been described in section 3.5. As has been discussed there, the selection is performed in two subsequent passes:
• First the terminals with the most negative and most positive error signals need to be selected,

• then one more terminal needs to be found such that Rule 2 (see page 41) is complied to.

First pass

With the daisy-chain architecture, we can compare the error of the active terminal to the worst error found as yet. For this purpose, the error signal switch matrix (see section 7.2.8) is used such that the error of the active terminal is connected to a (three-state) bus line leading to one side of a comparator residing on the central controller. Similarly, the other side of the comparator is connected to the error signal of the worst error found. If the error of the active terminal is found to be worse than the former worst error, then the active terminal becomes the ‘worst’, and the former ‘worst’ terminal is deselected.

Actually, the process is more complicated than described above because we need to track both the most positive and the most negative error. With adequate bookkeeping both terminals can be found with one passage of the token through the terminals. We will not go into that much detail here.

Second pass

During the second pass, a procedure similar to the first pass is executed to select a terminal which, together with the two already selected, complies to Rule 2. For this purpose, we need to compare the voltages between the unique and the other two terminals. If these voltages oppose each other, we have found a valid candidate.

The hardware needed for the selection during the second pass can be simplified somewhat by remarking that one of the voltage differences we need is between the two terminals which have been selected during the first pass. The sign of this voltage difference can therefore be stored already during the first pass.

After the two passes have been completed, three terminals have been selected which will be involved in the current flow in the active module for the next resonant halfcycle. The information needed to select the thyristors which will be fired is therefore transferred to the boards containing the thyristor decoding logic (c in figure 7.2). After this transfer, a signal can be given to the active module that a new current pulse can be started. After receiving this signal, the active module starts its current flow, and hands over the token to its neighbour module.

The whole operation of the central controller can be presented as the cooperation of two state machines. One serves to govern the line selection process, the other manages the selection of modules.
7.5.2 The terminal selection state machine

The coding of the first state machine has been chosen as indicated in table 7.2.

<table>
<thead>
<tr>
<th>Code</th>
<th>State</th>
</tr>
</thead>
<tbody>
<tr>
<td>000</td>
<td>Idle</td>
</tr>
<tr>
<td>010</td>
<td>Intermediate</td>
</tr>
<tr>
<td>100</td>
<td>First pass</td>
</tr>
<tr>
<td>101</td>
<td>Intermediate</td>
</tr>
<tr>
<td>110</td>
<td>Second pass</td>
</tr>
<tr>
<td>111</td>
<td>Intermediate</td>
</tr>
</tbody>
</table>

Table 7.2: State assignment for the terminal selection state machine

The corresponding transition diagram has been depicted in figure 7.15.

Figure 7.15: State transition diagram for the central line-selector state machine. Only transitions which indicate a change of state have been indicated

The transition from the idle to the active state is made on instigation of the module state machine, which we will come to shortly. At the transition from state 010 to state 100 (first pass) the token is fed into the chain of terminal circuits, and when it returns a check is made whether both a 'positive' and a 'negative' terminal have been found. If so, we continue through an intermediate state with the second pass (state 110). If not, the search starts over again. The second pass finishes when once again the token is returned to the central controller. In intermediate state 111 it is checked whether a third terminal has indeed been selected. If so, the terminal selector indicates
to the module state machine that a new current flow can be initiated. If not, the complete search will be performed again.

7.5.3 The module state machine

The second state machine on the central controller uses four separate states. The coding of these states is shown in table 7.3.

<table>
<thead>
<tr>
<th>Code</th>
<th>State Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>00</td>
<td>Idle (converter turned off)</td>
</tr>
<tr>
<td>01</td>
<td>Wait for current needed, or for thyristors to become safe</td>
</tr>
<tr>
<td>10</td>
<td>Select terminal</td>
</tr>
<tr>
<td>11</td>
<td>Wait for a certain time</td>
</tr>
</tbody>
</table>

Table 7.3: State assignment for the module state machine

The corresponding transition diagram has been depicted in figure 7.16.

Figure 7.16: State transition diagram for the central module state machine. Only transitions which indicate a change of state have been indicated.

When a need for current flow is reported, and the active module is found to be ready for a new current pulse, the module state machine commands the terminal selector to perform a selection. If the terminal selection succeeds, an appropriate signal is given to the active module, and after a certain time delay the next module is activated. The time delay is of influence only when the complete converter system is overloaded. In that case it takes care of a minimal phase shift in the case the phase-staggering algorithm can no longer perform its task.
Both state machines on the central controller have been implemented using one programmable logic device.

7.6 The central power and offset controllers (d)

7.6.1 The analog summing junction

Like the digital part of the central controller, the analog part relies on a particular bus structure. The structure used most often is the analog summing junction, which, because it is used several times, we will treat in some detail here.

For several computations in the analog electronics (see for example equations 3.14, 3.16 and 3.17) we need to compute the sum of analog quantities originating on different circuit boards. Like before, we want to use a modular setup, in which the different boards performing an equivalent task can be identical. Two structures come to mind for this purpose:

- A daisy-chain structure, where every next circuit board adds its contribution to a signal with an operational amplifier, and

- an analog summing junction, i.e. the signal is represented as a current which is fed into the inverting input (virtual ground) of an operational amplifier.

We have chosen the latter structure because of its simplicity: assuming that the signals are initially represented as a voltage, we need only a resistor for every board involved and only one central operational amplifier. A clear disadvantage of the structure is that the inverting input of this amplifier is directly connected to the bus, i.e. to a long trace on a backplane, which is generally considered bad practice. Because of the capacitive loading of this trace, the circuit can easily become unstable. Also, any kind of noise from the environment which can be picked up capacitively will be amplified.

We found that the stability of the circuit could be guaranteed by using some capacitive feedback around the operational amplifier, i.e. introducing what is called in [67] a 'phantom zero'. The bandwidth of the circuit will diminish with this method, however the bandwidth needed for these circuits generally lies only at a few kHz, so this needs not be a problem.

If special care is taken with regard to the surrounding traces on the backplane (preferably ground), capacitive coupling of disturbances can be kept at an acceptably low level.

7.6.2 The controllers

In section 3.6 it has been discussed that, due to Kirchhoff’s current law and the law of conservation of energy, restrictions apply to the current or
voltage references for the converter. Two control loops serve to cater to these restrictions. Both loops use a PI-controller to stabilize the loop and to achieve zero steady-state error. These PI-controllers are implemented as operational amplifiers with appropriate feedback, and differ only in the signal they are supplied with.

The first one, which has been discussed in section 3.6.2, receives as its input the sum-of-products as defined in equation 3.17. The individual products are computed on the terminal boards, and fed into an analog summing junction.

The second loop, which serves to comply with Kirchhoff's current law, is fed with the modified error signals originating in the PI-controllers on the terminal boards (see figure 7.4).

### 7.7 Simulation

To demonstrate the implementation of the control structure which has been presented above, we will in the following present some signals taken from simulations (using the program Simphs which has been presented in section 4.6) of the converter with its controller. In order to obtain some feeling for the time scales involved, we will present the same signals on three different time scales. All signals have been taken from a simulation of a three-phase to three-phase converter, consisting of three paralleled 6 kW modules. The starting point of the simulation is the same in all cases.

For clarity of the presentation of the digital state machine signals, we have used composite traces. Each trace is composed of the weighted state bits in question, such that the binary equivalent of the state is shown as one analog signal. The following traces are shown:

- **MS** The combined bits (MS1, MS0) of the module state machine, ranging from 0 to 3.
- **LS** The combined bits (LS2, LS1, LS0) of the terminal selector state machine, ranging from 0 to 7.
- **VS** The combined bits (VS1, VS0) of the predictor state machine, ranging from 0 to 3.

With this coding, each of these signals shows up as a rising staircase under normal operation. We will use a similar combination of the bits in chapter 8 to show the operation of the state machines in the prototype.

Figure 7.17 shows the development of three state machines during 25 μs operation of the converter. The predictor state has been shown for only one of the three modules. The simulation starts in the situation where the module under consideration is in the idle state. At a certain time, indicated by t₁, the combined error signal Err crosses the detection level. At this moment the terminal selector starts operating, first scanning 6 terminals, and after an
intermediate state 4 more. After finishing these scans, the terminal selector indicates to the module state machine that a new working set has been found. Subsequently, the current flow in the module (see lower trace) is initiated.

Figures 7.18 and 7.19 show the operation on two different time scales of a converter consisting of three paralleled power modules. The particular sequencing of the three resonant circuits is visible in figure 7.18. At the moment the error signal crosses its bound, a new module is started even though one or two of the other modules are still busy. The predictor state machines, indicated by VS, clearly indicate the phase of the corresponding resonant current.

Figure 7.19 shows the behaviour of the three paralleled modules on a 10 times larger time scale. This simulation especially shows the operation of the terminal selector circuit in the case when no terminals are selected. In the area indicated with a circle, the terminal selector repeats its operation for two subsequent pulses until a valid terminal set is found. This particular behaviour typically occurs close to the zero crossing of a terminal voltage or current. During the search normal operation of the converter is suspended. However, the simulation shows that the searches last only for the equivalent of ca. one resonant pulse. After a valid working set has been found, the error signal is quickly restored to its normal range.

To finish the presentation of the control electronics, figure 7.20 shows the operation of the three paralleled modules during 25 ms. On this time scale the operation of the complete converter system is visible during several cycles of both the input and the output grid. For clarity, relatively high grid frequencies have been chosen. The simulated input grid supplies sinewave voltages at 150 Hz, the output of the converter is voltage controlled at a frequency of 100 Hz.
The distribution of current pulses of the three individual modules over both in- and outputs of the converter takes care of these unrelated in- and output frequencies.

The input of the converter is set to a power factor of 1, i.e. \( p \) equals zero. The three upper pairs of traces in figure 7.20 show that indeed the input current pulses flow neatly in phase with the input voltages. Because of the mixed capacitive/resistive load, the output current leads the output voltage.

### 7.8 Discussion

In this chapter a realization in hardware of the control concepts which have been introduced in chapter 3 has been shown. A relatively straightforward implementation, using mixed analog and digital signal processing, has been
chosen. This realization is based on a scalable architecture with regard to the total number of paralleled modules and the number of terminals. It has been shown that the control hardware can be viewed as a matrix structure, whose column entries indicate a particular power module and whose row entries correspond to a particular input or output of the converter.

One of the elegant properties of the architecture we have used is that it allows an almost complete one-to-one mapping between control tasks and circuit boards. The control tasks can be divided into tasks which are local to a power module, to a terminal, or to both. Communication between these tasks and the associated circuit boards is performed by means of token-passing, summing junctions, and both digital and analog three-state buses. The data flow in both the analog and digital part of the circuit is governed by a central digital controller. The operation of this digital circuit is based on two state machines. On the highest hierarchical level, the module state machine takes
Figure 7.20: Simulation of 25 ms operation of a 3-phase to 3-phase converter consisting of three power modules

care of the selection of one module from those which are available for the next current pulse which will be initiated. On the next level, the terminal selector state machine governs the selection of three terminals for the next current pulse out of all terminals which are available.

The operation of the control system is illustrated with simulations on four different time scales.
Chapter 8

Measurements

In chapters 6 and 7 the design of the power circuit and control electronics for both a 15 kW and 6 kW power converter have been discussed. Following the design, both converters have been realized as prototypes (see [32, 34, 35]). In this chapter we intend to show some of the results obtained with these two converter setups. In the presentation we have limited ourselves to some of the most salient features of these converters.

We will start in section 8.1 with the 6 kW converter. This setup will be used specifically to demonstrate the operation of the control circuit. Basic to the control circuit is the operation of the state machines which have been discussed in sections 7.3.4, 7.5.2, and 7.5.3. The signals occurring in these circuits are shown together with signals taken from the power circuit.

In section 8.2, which deals with the 15 kW prototype, we will show some measurements concerning this power circuit. In particular, we will discuss power losses occurring in the converter. The measured losses are compared to their predicted values.

8.1 The 6 kW converter

The 6 kW power module has been especially designed in order to test the concept for phase staggering control. Therefore, compared to the (earlier) 15 kW converter, the control system has been expanded to perform the extra bookkeeping and (compensation) signal generation which is needed for this purpose. For reference, this section starts with the schematic of the complete power circuit, together with the component values.

8.1.1 The experimental set-up

The layout of the three-phase to three-phase power circuit we have used for our experiments has been depicted in figure 8.1.
The most important parameters concerning this power circuit are given in table 8.1.

This power circuit is connected to the control system through an interfac-
\[ \begin{array}{|c|c|} \hline C_{res} & 2 \mu F \\ \hline L_{res} & 148 \mu H \\ \hline L_c & 20 \mu H \\ \hline L_s \text{ parameters} & \text{see table 6.10} \\ \hline C_o & 90 \mu F \\ \hline \text{Thyristor type} & \text{SKFT 60/12DT} \\ \hline C_{th} \text{ parameters} & \text{see table 6.6} \\ \hline C_d & 10 \mu F \\ \hline R_d & 100 \Omega \\ \hline \end{array} \]

Table 8.1: Key specifications of the 6 kW prototype converter

\[ \text{ing unit. This interface part consists of gate pulse amplifiers (24, see section 7.4.3), back-bias detectors (24, section 7.4.2), current measurements (7, see sections 7.2.1 and 7.3.1), and voltage measurements (7, see also sections 7.2.1 and 7.3.1).} \]

The control circuit consists of the following printed circuit boards (the letters correspond to those in figure 7.2):

a) Central controller (1),

b) Current and voltage control boards (6),

c) Module control boards (1 or 2), and

d) Thyristor decoding logic (6).

The reference signals for the outputs are supplied by a three-phase sine wave generator.

In the following, the operation of the electronic control circuit is presented starting with single-phase DC-DC operation at relatively low input- and output voltages.

### 8.1.2 Measurement equipment

For the presentation of the operation of the 6 kW converter, two types of measurements are used:

a) \textit{Scaled} quantities (subscript \textit{sc}) in the control electronics, using either a straightforward connection or 10x voltage probes, and

b) unscaled voltages directly in the power circuit using 100x voltage probes.

All signals have been stored electronically using a Nicolet model 4094C digital oscilloscope, and transferred to the typesetting system using custom software. The Nicolet oscilloscope was equipped with plugin types 4175 and
4570. The 4175 is a 2-channel unit featuring 8 bits precision and a minimum sampling time of 2 ns; the 4570 features 12 bits and a minimum sampling time of 100 ns.

For a convenient presentation of the state machines, the two or three bits representing the state have been combined with a weighted resistor network to one analog signal. This setup provides signals shapes similar to those in figure 7.17.

8.1.3 The module- and terminal selection process

![Figure 8.2: Signals relevant to the terminal selection process.](image)

**MS**: state of the module state machine  
**LS**: state of the terminal selection state machine  
**VS**: state of the predictor state machine  
sampling interval: 2 ns

The module- and terminal selection process, which lies at the root of the converter operation, is shown in figure 8.2. In the figure the combined error signal crosses its bound at \( t = 0 \).

Right after this event the selection mechanism starts searching for a valid set of three terminals. During the time span where **LS** equals 100, which takes six consecutive clock cycles, the two terminals with the largest positive and negative error signals are selected. After an intermediate stage, where **LS** equals 101, a second search over the remaining four terminals is performed.
During this search LS equals 110. Finally, when a valid set of three terminals has been found, the terminal selection finishes and the thyristors in the appropriate power module are fired. The firing of the thyristors for the first current segment is indicated by $v_S$ becoming equal to 01. The reader may want to compare the measured signals with the simulation as presented in figure 7.17.

One of the results of the terminal selection process is that two terminal voltages are selected to be applied to the resonant circuit during the first and second current segment respectively. In figure 4.3 simulation results were shown for the choices of the pairs $(V_{LC1}, V_{LC2})$ which occur during three-phase to three-phase operation. In order to compare the simulation to measured results, the Nicolet oscilloscope was set up for external triggering, in such a way that at every transition from the first to the second current segment the actual values of $V_{LC1_{sc}}$ and $V_{LC2_{sc}}$ were stored in the oscilloscope memory. The results of this measurement are depicted in figure 8.3.

![Graph](image)

Figure 8.3: Measured values for $V_{LC1}$ and $V_{LC2}$ shown in a plane
The converter operates from three-phase AC 220V rms 50 Hz to three-phase 175V rms 100 Hz, without load.

Due to ripple and noise on the terminal voltages the distribution of the measurements over the plane is less sharp than in figure 4.3. Also, the measurement shows that in some cases voltages are used from a wrong section of the plane, i.e. where $V_{LC1} > 0$ or $V_{LC2} < 0$. One of the reasons for this
anomalous behaviour is that the voltages are selected at the beginning of the resonant pulse, however we sample them here at the cross over point. Again due to the ripple, a voltage which at the beginning of a pulse is still slightly positive may become negative during the pulse and vice versa.

![Graph](image)

Figure 8.4: One resonant cycle

Err: negative sum of absolute terminal errors

**VS**: state of the predictor state machine

**$V_{C_{sc}}$**: capacitor voltage

**$I_{t_{resc}}$**: resonant current.

Sampling interval: 100 ns

Figure 8.4 shows the measured values of the state variables of the resonant circuit together with the digital state of the module state machine. The figure shows that the current flow is initiated a short time (used for the terminal selection process, see figure 8.2) after the combined error signal crosses its bound. As the resonant current flows, the capacitor voltage $V_C$ changes until it crosses the value $V_{C_1}$ (not shown here for practical reasons, see figure 8.5). Right after this cross over has taken place, the state machine VS changes to 10,
and the appropriate thyristor for the second current segment is fired. After
termination of the current flow, the state machine remains in the position \textbf{VS} = 11 for the duration of the turn-off time \( t_q \). Note that at the end of the
resonant halfcycle some distortion is present on \( V_{C_{sc}} \). This distortion can be
traced back to the operation of the sample-and-hold circuit which is used to
store the value of \( V_{C0} \) (see figure 7.11). The reader may want to compare the
measured signals with the simulation as presented in figure 7.18.

Contrary to the situation presented in that figure, the measured error
signal Err here does not jump immediately to its "sawtooth" value. The
reason for this behaviour is that we performed these measurements at rather
low (± 36 V) terminal voltages, which implies that the ripple on these voltages
will be relatively large. This ripple leads to a changing value of the computed
value of \( V_{C1} \) (see figure 8.5), which on its turn influences the shape of the
compensation signals.

### 8.1.4 \( V_{cpeak} \) control

Figure 8.5 zooms in on the operation of the \( V_{cpeak} \) controller of one power
module. In the figure trace \( V_{C1} \) indicates the computed value of the capacitor
voltage at switchover for assumed positive resonant current. As soon as the
measured capacitor voltage \( V_{C} \) crosses this value, the second current segment
is initiated (indicated with circles and arrows in the figure). As has been
noted before, due to the relatively large ripple on the terminal voltages the
computed value for \( V_{C1} \) is not completely constant for the duration of the
resonant pulse.

In figure 8.6 we show the measured trajectories of the pair \((V_{C},I_{res})\) of
one power module in the state plane for four values of \( V_{C2} \). The trajectories
were recorded for single phase DC-DC operation, with terminal voltages of +36/0/-36 V respectively. Ideally, in this operating mode the trajectories
should be completely equal for every full resonant cycle. However, the
"fattening" of the trajectories as displayed in the figure indicates that slight
deviations do occur for subsequent resonant pulses. As might be expected,
the trajectories show a more pronounced "two-circle" appearance for low
values of the peak capacitor voltage \( V_{C2} \).

Figure 8.7 again shows the trajectory of \((V_{C},I_{res})\) of one power module in
the state plane. However, here the converter is operating as a three phase to
three phase DC-AC or AC-AC converter. In these operating modes, a variety
of voltage combinations for the first and second current segment (\( V_{LC1} \) and
\( V_{LC2} \) respectively) is applied to the resonant circuit. In the figure these
differing voltage pairs show up as different trajectory shapes. The operation
of the \( V_{cpeak} \) predictor shows up in the accuracy with which every trajectory
passes through the points \((±V_{C},0)\) in the state plane.
Figure 8.5: Operation of the $V_c$ peak predictor for DC-DC operation

$VS$: state of the predictor state machine

$I_{resc}$: resonant current

$V_{C_sc}$: capacitor voltage

$V_{C_{1sc}}$: computed value for the capacitor voltage (related to a positive value of $I_{res}$) at switchover

Sampling interval: 100 ns

8.1.5 Waveform synthesis

Figure 8.8 shows how an individual waveform, in this case an output voltage, is composed. The voltage on the output filter capacitor ($U_v$) is adjusted in tiny steps by the individual current pulses ($I_n$). In this way the desired output voltage (upper trace) can be approximated.

Figure 8.9 shows how multiple waveforms, in this case an input current and an output voltage, are synthesized. The individual current pulses flowing in the resonant circuit are redirected by the switching matrix to either an input of the converter, an output, or both. As the operating frequency of the resonant circuit (ca. 4.5 kHz) is much higher than the desired input- or output frequencies (50 resp. 115 Hz.), this intermodulation process allows the simultaneous generation of multiple low frequency currents with different wave shapes and/or frequencies.
Figure 8.6: State variables of the resonant circuit in the phase plane for DC-DC operation at four different values of $V_{C2}$

$V_C$: capacitor voltage

$I_{res sc}$: resonant current

sampling interval: 1 $\mu$s

upper left: $V_{C2} = 320$ V

lower left: $V_{C2} = 160$ V

upper right: $V_{C2} = 240$ V

lower right: $V_{C2} = 80$ V

8.1.6 The terminal PI control loops

In section 7.2.3 it has been pointed out that for accurate generation of input and output signals a PI control circuit is used for every terminal of the converter. The operation of this controller for one output terminal is shown in figure 8.10.

The upper traces in figure 8.10 show the actual error (difference between terminal voltage and reference) and the output of the PI controller for output terminal V. The actual error ($Err_a$) is rather small, and contains only high-frequency components, because the integrating part of the PI controller
Figure 8.7: State variables of the resonant circuit in the phase plane for multiphase DC-AC and AC-AC operation

a) (left) DC-AC operation. Input voltages (DC): +36/0/-36 V. Output: sinewave 80 V peak, 50 Hz.
b) (right) AC-AC operation. Input line voltage (AC, three phase): 300 V rms, 50 Hz. Output: sinewave 310 V peak, 55 Hz.

$V_C$: capacitor voltage
$I_{res_c}$: resonant current

Sampling interval: 1 $\mu$s

emphasizes the steady-state (i.e. low-frequency) part of the error. Without this PI-controller the real error signal would be almost as large as trace $Err_vPI$ in the figure.

8.1.7 Phase staggering

Originally two 6 kW power modules have been constructed in order to demonstrate the feasibility of phase staggering in the context of a multiphase to multiphase resonant converter. Unfortunately, because the second module is no longer available for measurements, we will not be able to demonstrate this complete functionality here. However, by reconstructing the 6-terminal thyristor bridge such that two 3-terminal bridges result, we are able to show the capability for phase staggering for a reactive power compensator or single phase converter (see table 2.1). This modification has been drawn schematically in figure 8.11.

Figure 8.12 shows the operation of the phase staggering control algorithm in the context of a single phase DC-DC converter under current control. The $\text{ASDTIC}$ error signal, which equals the time integral of the total current flowing in the terminal minus its reference value, shows the typical ripple which
Figure 8.8: AC output waveform synthesis.

- $U_{\text{ref}_SC}$: reference voltage of terminal V
- $U_{\text{usc}}$: output voltage of terminal V
- $\text{Err}_v$: difference between output voltage and reference (amplified 6.6 times)
- $I_{\text{usc}}$: unfiltered output current in terminal V
- Sampling interval: 2 $\mu$s

is usual in this application. When no current flows, the error ramps up or down, until a predefined border is exceeded. At that moment, current flow is initiated, in this case alternatingly in two power modules. As a consequence of the current flow, after a while the error signal reverses direction. However, as trace $\text{Err}_v$ in figure 8.12 shows, the reversal is not immediate. In order to make the reversal immediate, a compensation signal is added to the error signal. The result (after the PI controller) is shown in trace $\text{Err}_v, PI$. This signal shows an almost instantaneous response to the current flow, thus preventing the other module to be fired immediately.

Figure 8.13 shows the operation of two paralleled power modules which
Figure 8.9: Waveform synthesis for in- and outputs

$I_{ressc}$: resonant current
$I_{asc}$: unfiltered input current in terminal $S$
$I_{usc}$: unfiltered output current in terminal $V$
$U_{usc}$: output voltage of terminal $V$
sampling interval: 5 $\mu$s

together act as a single phase current-controlled DC-AC converter. The figure shows that the individual output current pulses have a phase shift of approximately 180 degrees, thus lowering the ripple on the output voltage substantially.

Figure 8.14 shows the operation of the three-terminal converter functioning as a three phase reactive current compensator. As in the two cases before, the figure shows that the current pulses are divided evenly between the two power modules. At $t = 0.5$ ms a disturbance in the operation of the converter is visible. This disturbance can be traced back to the operation of the terminal selection circuit: at this particular instant two of the three terminal voltages ($U_s$ and $U_t$) are approximately equal. If the power balance
Figure 8.10: The terminal PI controllers

\( \text{Err}_v \): difference between output voltage and reference (amplified 6.6 times)
\( \text{Err}_{v,PI} \): idem, after PI controller stage
\( U_{\text{refsc}} \): voltage reference of terminal V
\( U_{\text{usc}} \): voltage of terminal V

Sampling interval: 10 \( \mu s \)

in the converter is right, then the reference current for the third terminal (\( I_{\text{ref}} \)) should cross through zero at exactly the same moment. However, due to noise and component tolerances, the crossing of the voltages and of the current reference do not coincide exactly, which implies that the terminal selector will not find a valid set of three terminals. Therefore the generation of the current pulse is delayed for a short time. The reader may want to compare this event with the simulation results in figure 7.19.
Figure 8.11: Modification of a three-phase to three-phase converter to a two-module three-terminal converter

a) (left) original situation
b) (right) two modules

8.1.8 Static and dynamic characteristics

When operating under voltage control, the three-phase to three-phase power converter would ideally show zero output impedance. In order to test this behaviour, we have measured the output voltage of the converter under conditions of (slowly) varying load. The shapes of the generated output voltages at full load are shown in figure 8.15.

The generated output voltages show some ripple, similar to the ripple which shows up in the simulation (see figure 4.2).

Figures 8.16 and 8.17 show the operation of the PI controller which serves to estimate the input power. To give a first impression of the speed of response of this control circuit, the converter was set up for three-phase to three-phase conversion, and the amplitude of the output voltage was modulated with a square wave. The resulting voltage reference for output $V$ is shown in the uppermost trace of the figure. The individual output voltages, which are shown in the lower traces, show an almost immediate response to the change of reference.

In order to get a close view on the speed of response of the power circuit, figure 8.17 depicts the experiment on a shorter time scale. For clarity, the three output wave shapes were set to DC for this experiment, and only one output is shown. The trace in the figure shows that the rise and fall times of the output voltage both are ca. 1.1 ms.

8.1.9 Commutation

Figure 8.18 shows the commutation of current from one thyristor branch to another. For this measurement the converter was used as a DC-DC single phase converter and the three terminals ($R, S, T$) connected to $-57/0/+172$ V DC voltages respectively. The lower trace in figure 8.18 was computed from the measured values of $I_r$ and $I_l$. According to the analysis in appendix A the slope of this trace, i.e. $dI_{csc}/dt$, should be constant during commutation.
Figure 8.12: Phase staggering control: signal flow

$\text{Err}_s$: ASDTIC error signal

$\text{Err}_{s,PI}$: error signal after the PI controller, with compensation added

$I_{s1sc}$: unfiltered current in terminal S of module #1

$I_{s2sc}$: unfiltered current in terminal S of module #2

sampling interval: 500 ns

From the measurements, we obtain $dI_{csc}/dt = 1.65V/\mu s$. From this value, using equations 7.2 and 7.12, we can compute the corresponding $di/dt$ in the power circuit:

$$\frac{dI_c}{dt} = \frac{1}{Z_{res}A_u} \frac{dI_{csc}}{dt} = \sqrt{\frac{2\mu F}{198\mu H} \cdot \frac{80 \times 1.65 V}{\mu s}} = 13.3 \frac{A}{\mu s}$$

(8.1)

This value, which is higher than any $di/dt$ actually occurring in the circuit, shows that the transient current stresses to which the semiconductors are subjected are properly limited.
Figure 8.13: Phase staggering control: DC-AC operation
   Err: Error signal
   $I_{s1ac}$: output current of module #1
   $I_{s2ac}$: output current of module #2
   $U_{sr}$: voltage between terminals $S$ and $R$ of the converter
   sampling interval: 5 $\mu$s.

8.1.10 Fast transients

In order to compare the transient values of voltages and currents in the power circuit with simulations, we performed some measurements for which the power circuit was used as a single input, single output DC-DC converter. Terminals $s$, $r$, and $t$ of the power circuit (see figure 8.1) were used as input, neutral, and output, respectively.

Figure 8.19 shows the wave shapes of voltage and current at the moment of turnoff of a thyristor. Initially, thyristor $Th_{r1}$ conducts, and the voltage drop is too small to be visible here. After the firing of another thyristor ($Th_{r1}$), the current through thyristor $Th_{r1}$ starts to slope down, and after
Figure 8.14: Phase staggering control: AC reactive current compensator

Err: Error signal

$I_{s1sc}$: Unfiltered current of module #1, terminal S
$I_{s2sc}$: Unfiltered current of module #2, terminal S
$U_{ssc}$: voltage of terminal S
sampling interval: 5 $\mu$s

A short time crosses through zero. Around this zero crossing the saturable inductances get out of saturation, which shows up here in the lower slope of $I_{ssc}$ around zero. For larger negative values of $I_{ssc}$ the saturable cores saturate again.

Already during the sloping down of current $I_{ssc}$ a forward voltage starts to develop across the antiparallel thyristor $Th_{r2}$. From the measurements we obtain a value for the $dV/dt$ applied to this thyristor of 44V/$\mu$s. The reverse voltage across thyristor $Th_{r1}$ builds up much faster. The measured value of $dV/dt$ for this thyristor is 317V/$\mu$s. The measurement shows the proper operation of the snubber of thyristor $Th_{r2}$, whose core is unsaturated at the instant thyristor $Th_{r1}$ turns off.
Figure 8.15: Static operation: shape of the generated voltages.

- $U_{usc}$: Voltage on output terminal U
- $U_{wsc}$: Voltage on output terminal V
- $U_{wsc}$: Voltage on output terminal W

Sampling interval: 5 $\mu$s

Figure 8.20 shows a simulation of the same events with the models which have been derived in chapter 5. Comparison of the results in figures 8.19 and 8.20 shows good agreement. Differences between the measurement and the simulation occur at two main points:

- The off state voltage applied to the thyristors at the start of the measurement, and

- the value of the reverse recovery peak current and -charge.

In the simulation the off state voltage of the thyristors is computed by assuming that every thyristor in the off state can be represented by a high resistance. In the simulation these resistances are equal for every thyristor. However, in reality the off state voltage applied to the thyristors depends heavily on the actual leakage current of the respective thyristor junctions. These leakage currents show large differences between different thyristors of the same type, and are dependent on the junction temperature [22].

The values for $dV/dt$ for thyristors $Th_{r1}$ and $Th_{r2}$ were computed to be 1322 and 47V/$\mu$s, respectively. The former value is rather large compared to
Figure 8.16: Dynamic operation: shape of the generated voltages.

- $U_{vrefsc}$: Reference voltage for output terminal V
- $U_{usc}$: Voltage on output terminal U
- $U_{usc}$: Voltage on output terminal V
- $U_{wsc}$: Voltage on output terminal W

sampling interval: 20 $\mu$s

The measurement. The latter value is in good agreement with our practical results.

The differences between the experiment and the simulation show that the model we have used for the reverse recovery current- and charge is rather conservative: the model predicts much larger values for the reverse charge and peak current than were actually measured. As a consequence the thyristor voltage traces in the measurement are not as articulated around turn off events as are the simulated traces.

The larger reverse recovery parameters in our model compared to reality can be explained as follows. The model is based on worst-case data sheet values, valid for the worst possible device at the highest allowed junction
Figure 8.17: Dynamic operation: shape of the generated voltages.
Mod: Amplitude modulating signal
$U_{vsc}$: Voltage on output terminal V
sampling interval: 5 µs

temperature (125°C). Therefore we may expect that in our experiment, which was not performed at full load, the recovery phenomena do not show up as strongly.

The experiment suggests that a more sophisticated model for the reverse-recovery charge and current may be needed in order to obtain accurate simulation results in this respect. According to [95], especially the junction temperature could be an important parameter.

8.2 The 15 kW converter

The topology of the 15 kW power converter (see figure 6.1) is almost the same as the 6 kW converter, which has been given in figure 8.1. The only difference is that one commutation inductance is used in common for 4 thyristors connected to a terminal, instead of 4 separate inductors. The most important parameters concerning this power circuit are given in table 8.2.

In this section we concentrate on the power losses and therefore the efficiency of this converter. For this purpose measurements of the total input and output power have been performed. The results presented here have also been reported in [33, 34]. For these measurements we have used six wide band wattmeters, three of which (Marek) were connected to the inputs of the converter, and the other three (Norma) to the outputs. With this setup, the measurement error for the in- and output powers is ca. 1%.

The input- and output power have been measured at several output voltages and different loads. From the measured power we can compute the
efficiency $\eta$:

$$\eta = \frac{P_{out}}{P_{in}} \quad (8.2)$$

The computed values for $\eta$ have been plotted against the output power in
Figure 8.19: Voltages and current applied to an antiparallel thyristor pair close to turn-off

$I_{rsc}$: Current in terminal $r$

$I_{tsc}$: Current in terminal $t$

$V_{ac1}$: Voltage across thyristor $Th_{r1}$

$V_{ac2}$: Voltage across antiparallel thyristor $Th_{r2}$

sampling interval: 40 ns

The plotted traces in figure 8.21 show that the efficiency of the converter at rated output voltage and power (380 V, 15 kW) is quite high: 92%. The efficiency at rated voltage drops to low values (below 80%) only if we draw less than 16% of rated power. For reduced values of the output voltage, the maximum efficiency (and the maximum power which can be delivered to the output) drop somewhat. However, the traces show that even at an output of 110 V the percentual efficiency remains in the eighties over the major part of the operating range. This large high-efficiency range is important for applications which are expected to run in partial load for extended periods.
The 15 kW converter

\[ I_r \]  
\[ I_t \]  
\[ V_{ac1} \]  
\[ V_{ac2} \]  

Figure 8.20: Numerical simulation of figure 8.19

- \( I_r \): Current in terminal \( r \)
- \( I_t \): Current in terminal \( t \)
- \( V_{ac1} \): Voltage across thyristor \( Th_{r1} \)
- \( V_{ac2} \): Voltage across antiparallel thyristor \( Th_{r2} \)

8.2.1 Power losses

The difference between the measured input- and output power yields the power loss \( P_{loss} \) in the converter:

\[ P_{loss} = P_{in} - P_{out} \]  \( (8.3) \)

This power loss depends on a myriad of variables. If we assume the converter to be powered from a symmetrical three-phase grid, and to deliver symmetrical voltages to a symmetrical load, the most important components determining \( P_{loss} \) are the following:

- The input voltage \( U_i \),
### Key specifications of the 15 kW prototype converter

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>$C_{\text{res}}$</td>
<td>4 $\mu F$</td>
</tr>
<tr>
<td>$L_{\text{res}}$</td>
<td>33 $\mu H$</td>
</tr>
<tr>
<td>$L_c$</td>
<td>15 $\mu H$</td>
</tr>
<tr>
<td>$L_x$ parameters</td>
<td>see table 6.10</td>
</tr>
<tr>
<td>$C_o$</td>
<td>180 $\mu F$</td>
</tr>
<tr>
<td>Thyristor type</td>
<td>SKFT 110/10DS</td>
</tr>
<tr>
<td>$C_{\text{th}}$ parameters</td>
<td>see table 6.6</td>
</tr>
<tr>
<td>$C_d$</td>
<td>15 nF</td>
</tr>
<tr>
<td>$R_d$</td>
<td>47 $\Omega$</td>
</tr>
</tbody>
</table>

Table 8.2: Key specifications of the 15 kW prototype converter

**Figure 8.21:** Measured efficiency $\eta$ versus output power $P_{\text{out}}$ for four values of the rms line output voltage

- the output voltage $U_o$,
- the input frequency $f_i$,
- the output frequency $f_o$,
• the output current \( I_o \), and

• the reactive input current \( I_{io} \).

All these parameters have their own particular influence on the voltage and current wave shapes in the converter, and therefore on the power losses. In principle it is possible to construct a mathematical model for the power losses, using a least-squares fit to the measurement data. This method has been described in [23]. However, if we want to obtain accurate coefficients in such a model (with six parameters and possibly combinations thereof), a tremendous number of measurements needs to be performed. Furthermore, the practical use of a mathematical model is rather limited.

For the designer, the maximum power loss in the power circuit is of interest for the thermal design of the converter. In Chapter 6 we have computed some relevant values for circuit components, currents, and voltages. Here we will compare these values to the measurements in the rated operating point, i.e. at \( P = 15 \, kW \) and \( U_o = 380 \, V_{rms} \). A problem arises because the losses in the thyristors depend in an unknown way on the values of the rms and average resonant current. As an approximation, we will use the thyristor losses corresponding to the worst case currents from Table 6.5 (because these losses can be computed), and scale them with the ratio between the simulated average resonant current and its worst case value. From Table 6.5 we obtain the following scaling factor \( K \):

\[
K = \frac{66.1}{98.5} = 0.671
\]

The power loss for the snubbers is estimated similarly. From Table 6.7, using equation 6.16, we obtain \( \sigma = 0.45 \). Inspection of Figure 5.4 then shows an average energy loss of 54 mJ/pulse. In the worst-case situation, this energy loss appears every 65\( \mu \)s. We will assume that the same derating factor \( K \) can be applied here.

For the other relevant circuit elements, we can compute the losses directly from the current values given in Table 6.5 and the component values in tables 6.8 and 6.9. Thus we find the following values for the total losses:

<table>
<thead>
<tr>
<th>Element</th>
<th>Power Loss</th>
</tr>
</thead>
<tbody>
<tr>
<td>Thyristors</td>
<td>( P = 2K \times 769 , W )</td>
</tr>
<tr>
<td>Snubbers</td>
<td>( P = K \times 54mJ/65\mu s )</td>
</tr>
<tr>
<td>( L_{res} )</td>
<td>( P = R \times I_{rms}^2 )</td>
</tr>
<tr>
<td>( L_c (2) )</td>
<td>( P = 2R \times I_{rms}^2 )</td>
</tr>
<tr>
<td>other elements</td>
<td>assumed negligible</td>
</tr>
<tr>
<td>Total loss</td>
<td></td>
</tr>
</tbody>
</table>

The total loss as measured at rated output voltage and power is 1440 \( W \). This implies that we have been somewhat pessimistic in the computation above. This might be expected, because the largest contribution to the computed losses, i.e. the power loss in the thyristors, is based on a worst-case data sheet value (as no other was available).
8.3 Discussion

The experimental setups of both the 6 kW and the 15 kW converters which were discussed in the chapters before have been used to perform measurements. The measured waveforms were used to verify the validity of the designs and the underlying theory. Furthermore, measurements were presented in order to demonstrate some of the capabilities of this kind of equipment.

The signals occurring both in the control electronics and in the power part of the converters have been shown to agree satisfactorily with the shapes and values predicted by simulation. This observation supports the models we have used for the various components of both the power circuit and the control electronics. An exception needs to be made here for the models of the stored charge in the thyristor junction, and for the losses occurring in the thyristors. However, both models were shown to yield conservative data.

The close agreement of the measured data to the simulated design also indicates the proper operation of our hardware architecture. Signals taken both for different numbers of input and output terminals and for one or two power modules support the scalability of the system in both these dimensions.

Summarizing we may therefore state that:

- The module- and terminal selection processes perform their tasks as predicted,
- the designed Vcpeak controller is indeed able to restrict the peak capacitor voltage to narrow margins,
- the in- and output waveforms both appear as nearly pure sine waves,
- the algorithm for phase staggering works as predicted, both under DC-DC and AC operation of the converter,
- the models which were derived for saturating inductors and the thyristor junction capacitance show good agreement with the measurement data,
- the models describing the stored junction charge and the thyristor losses are too conservative, and need refinement. However, the models in their present state can be used safely for design,
- limitation of both dv/dt and di/dt applied to the thyristors has been reached.
Chapter 9

Conclusion

In chapter 1 we have formulated the problems we wanted to solve in the course of this research project. Now the time has come for an evaluation of the work which has been done, to state which goals have been achieved, and what remains to be done in the future.

In section 9.1 we will address the results of this work, and discuss the most salient features of the type of equipment which we have developed. Section 9.2 is concerned with developments which have been taking place during the last decade in the field of power electronics. To finish up, section 9.3 lists some recommendations for further research and development.

9.1 Results

The results obtained in this work can be subdivided in several categories. First, we will return to the problem statement which we have put forward in chapter 1. The following sections deal with methodology, i.e. the way we have attacked a design problem, and with the specific features of the implementation.

9.1.1 The problem statement revisited

Our problem statement was concerned with three main topics: input current control, scalability with regard to the (total) number of terminals, and parallel operation (phase staggering).

The theory and practical design we have shown in the foregoing chapters show that for the one-matrix topology all three goals have been reached. Therefore we may state that, for that topology, it is now possible to:

- Achieve load sharing between the input terminals of an SR power converter with an adjustable input power factor in such a way that the input power factor range includes unity;
• Construct series-resonant power converter modules with any number of input- and output terminals, as long as the total number of terminals is greater than 2;

• Parallel any number of these modules in such a way that the load is shared equally between them, even under transient conditions, and that the effective inverter frequency rises linearly with the number of modules.

9.1.2 Model based design and control

A large part of the work which has been reported in this thesis is concerned with models. We have used a simplified model in order to obtain some insight in the operation of the power circuit, and more complex models for the detailed design. The simplified model suggested the structure of the Vcpeak controller. Even though a simplified model in general will not provide an accurate description of the behaviour of the real circuit, we found that the description was “close enough” for the controller to work satisfactorily. Also, measurements have shown that in most respects the more detailed model, which is composed of more accurate descriptions of the components of the power circuit, shows close agreement with reality.

Summarizing we may state that this model-based approach of both control and circuit design has borne fruit. The combined use of models for the power and the control circuit makes it possible to verify the operation of a design with adequate accuracy before it is built.

9.1.3 State based control

It is well known in the theory of linear systems that tight control of such a system is possible if full state information is available. Even though the SR power converters considered here are strongly nonlinear systems, the work reported in this thesis indicates that the availability of state information is of major importance for the control of these converters as well. A nonlinear model based control law is used to tame the relatively fast dynamics in the resonant circuit. Once this has been achieved, control of input- and output currents becomes relatively easy.

9.1.4 Further features of the multiphase series-resonant converter

The power circuit topology and control system we have devised make it possible to:

• Generate smooth waveforms at both the input- and output terminals of a multiphase SR converter;

• Perform both step-up and step-down voltage scaling;
• Transfer electrical power in a controlled manner in both directions between two mutually asynchronous electrical multiphase grids;

• Generate output voltages of programmable shape, including nonsinusoidal, instantaneous phase reversal, and almost instantaneous amplitude modulation;

• Generate or absorb reactive power independently at both input and output terminals;

• Transfer electrical power from a multiphase grid to another multiphase grid or load with high efficiency over a large part of the operating area;

Every nice feature has its price. In the case of the SR converter we pay for them mainly in the following way:

• The power output of an SR converter is rather low compared to the total VA rating of the power semiconductors needed;

• The control circuit of a multiphase SR converter is a highly complex system, thus possibly hampering the reliability of the system;

• The power circuit of these converters contains many active semiconductors, with the associated need for driving circuits and measurements. Consequently the ratio of price to performance of these power circuits is rather high.

Whether an SR converter is an attractive way to implement a desired system function ultimately depends on the alternatives which are available for the task. The developments in the alternative technologies are the subject of the following section.

9.2 Developments

In section 1.3 a view has been given regarding the market developments of power semiconductor devices. As we know now, this view was rather optimistic as far as the developments in fast thyristors, the primary work-horse for multiphase resonant converters, are concerned. Also, for large power ratings several new device types, with low switching losses compared to thyristors, have been developed in the last decade. GTO thyristors, IGBT's, and normal bipolar transistors can operate up to several kHz switching frequency for tens of kW power ratings [27, 66, 84], and up to several hundred hertz in the MegaWatt power range [61]. Power MosFet's are reported [20] to switch several kW's at frequencies in the 10 to 100 kHz range, and allow relatively easy load sharing.

These new devices have forced a shift of the borderline between the areas where SR techniques can be reasonably applied and where other switching techniques show better performance. Several reasons can be put forward for not using resonant techniques:
Conclusion

- The semiconductor switches are generally subject to (sometimes much) higher rms and peak voltages and/or currents than devices in a PWM context for the same power rating [64],

- Often more semiconductor switches are needed to perform the same task,

- Resonant power converters are often (assumed to be) harder to control than PWM converters,

- Design rules are hard to extract from the open literature.

As an example, in the bulk of medium-power applications, i.e. variable speed drives, the field has been taken by the newer devices mentioned before. The squirrel-cage induction machine, which is the work-horse in electrical drive technology, can be driven to satisfactory performance using relatively crude waveforms generated by circuits with a much simpler architecture than the circuits described in this thesis.

This implies that quite a few applications, which fell in the scope of the multiphase series-resonant converter when the research described here started, are no longer there. Still, the series-resonant converter has applications where in some respects other circuits still lag behind. As with any technique, SR converters should be used where the advantages of the technique show up and the disadvantages can be minimized.

The field of applications of multiphase power converters seems to be dominated by electrical drives, where Pulse Width Modulation (PWM) appears to be a cheap and reliable technique. Only if smooth output voltage waveforms are needed for the application, it may be worthwhile to use an SR converter. An example of such an application is an Uninterruptible Power Supply (UPS), which is generally expected to supply clean sinewave voltages to a nonlinear load.

Contrary to the outlook for multiphase applications, a whole new field is currently being developed for DC-DC conversion using so-called quasi-resonant techniques [69, 74, 75]. The application of resonant techniques there appears to be shifting towards frequencies in the MHz range, which is the range where the newer power semiconductors experience the same type of problems as did the thyristors for which the series-resonant technique was originally conceptualized for the kHz range over 20 years ago.

9.3 Topics for future research

The work reported in this thesis has shown that it is feasible to design and construct multiphase series-resonant power converters. In principle, due to the soft switching waveforms applied to the active semiconductors, this type of converter could be used for applications up to several hundred kW at internal frequencies of several tens of kHz.
9.3.1 Reduction of the number of active devices

As has been noted before, whether such a converter is an attractive candidate to perform a certain system function depends on a large number of parameters. Due to the price and vulnerability of the power semiconductors, one of the most important parameters appears to be the number of active devices needed. It seems to be worthwhile to investigate power circuits which carry with them the advantages of the resonant technique, but which use fewer components.

9.3.2 More accurate predictor

Using a predictor circuit in order to control the state of the resonant circuit has proven to be a successful technique. However, the present implementation is based on a much simplified model of the power circuit, and is therefore not able to control the state of the LC circuit with high accuracy. A more accurate implementation appears to be possible (see appendix B), and waits to be tested in a practical circuit.

9.3.3 Better model for the stored charge in the thyristor junction

The way the power semiconductors switch on or off can have large consequences for the voltages applied to these devices. For an accurate computation of these voltages, more accurate models for the internal operation of thyristors are needed.
Appendix A

Analysis of Commutation

In chapter 6 it has been shown that the presence of commutation inductances and snubbers causes unwanted deviations of the peak capacitor voltage from its intended value. For the 6 kW converter, deviations from 1 to 9% were computed. Of the phenomena which remained unmodelled in the simplified power circuit, commutation appears to have the largest influence on the operation of the Vcpeak predictor. It is therefore worthwhile to analyze which aspects of the operation of the power circuit change due to the commutation inductances. We will discuss this matter referring to the network in fig. A.1.

Figure A.1 shows the part of a resonant converter which is relevant for the current flow during commutation of the current from one branch (1) to another (2). Saturating inductors have been left out. The thyristors are modeled as ideal switches. For the analysis, all voltages in the circuit are referred to the node between the two independent sources $V_{LC1}$ and $V_{LC2}$. This node has therefore been grounded symbolically.

A.1 Description

We will assume that the impedance of the snubber components is high compared to the rest of the circuit, and ignore their influence. We will furthermore assume that the magnitude of the initial capacitor voltage $V_{C0}$ is large enough to overcome the voltage in branch 1, i.e. $V_{C0} < V_{LC1}$, and that the voltages $V_{LC1}$ and $V_{LC2}$ have the proper polarity for commutation to be possible, i.e. $V_{LC1} < V_{LC2}$. The normal operation is as follows.

After firing thyristor $Th_1$ at $t = t_0$ a sinewave current starts to flow in the resonant circuit. After some time, depending on the control circuit, thyristor $Th_2$ is fired at $t = t_{1a}$ in order to take over the current flow from $Th_1$. As from this moment, all three thyristors in the circuit conduct. Due to the voltage difference between $V_{LC2}$ and $V_{LC1}$ $I_1$ will decrease gradually, while $I_2$ will rise. The commutation is finished at the instant ($t_{1b}$) when $I_1$ becomes zero. After this moment only $Th_2$ and $Th_3$ conduct, until the moment when
the resonant current $I_{res}$ becomes zero. Then all thyristors turn off.

The state plane trajectory and the time response of the currents are depicted in figure A.2.

Figure A.2: Description of commutation phenomena, without snubbers

a: (left) State plane trajectory
b: (right) Waveforms versus time
The figure clearly shows the intended effect of the commutation inductances, i.e. the $di/dt$'s of the currents through the thyristors are reduced. Furthermore, the presence of a new current segment between $t = t_{1a}$ and $t = t_{1b}$ shows that the "effective" takeover of the current from branch 1 to branch 2 does not take place at the instant thyristor $Th_2$ is fired, but somewhere along the interval $[t_{1a}, t_{1b}]$.

We like to note here that the waveforms as depicted in figure A.2 show a more or less intended behaviour. However, the presence of commutation inductances can, in certain situations, give rise to rather peculiar waveforms. We will come back to that matter after the more formal analysis.

A.2 Analysis

For an approximate analysis of the simplified process as described in section A.1 we will introduce an additional variable $I_d$, being the difference between the currents in branches 2 and 1. Therefore before the commutation $I_d$ equals $-I_1$, and after the commutation $I_d$ equals $I_2$. If for simplicity we assume $L_{c1} = L_{c2} = L_{c3} = L_c$, then for the processes during the commutation the following derivation applies:

\[ L_c \frac{d}{dt} I_1 = V_{LC1} - U_k \]  \hspace{1cm} (A.1)

\[ L_c \frac{d}{dt} I_2 = V_{LC2} - U_k \]  \hspace{1cm} (A.2)

\[ (L_{res} + L_c) \frac{d}{dt}(I_1 + I_2) = U_k - V_C \]  \hspace{1cm} (A.3)

\[ C_{res} \frac{d}{dt} V_C = I_{res} \]  \hspace{1cm} (A.4)

Adding equations A.1, A.2, and A.3 (2x) and dividing by two we obtain for the sum of the two branch currents:

\[ (L_{res} + \frac{3}{2} L_c) \frac{d}{dt} I_{res} = \frac{1}{2}(V_{LC1} + V_{LC2}) - V_C \]  \hspace{1cm} (A.5)

and subtracting equation A.1 from equation A.2 yields:

\[ L_c \frac{d}{dt} I_d = V_{LC2} - V_{LC1} \]  \hspace{1cm} (A.6)

In this way we have performed a change of base quantities ($I_1, I_2$) to ($I_{res}, I_d$). The equations concerning these quantities (A.5 and A.6 respectively) look relatively simple. Equation A.5 shows that in the commutation interval the resonant current will still be a sinewave. During the commutation interval $I_d$ develops linearly with time (equation A.6). This behaviour is visible in the lower trace of figure A.2b.

During the commutation the frequency of $I_{res}$ and the impedance of the resonant circuit change by a small amount. These values are now given by:

\[ \omega_{res} = \sqrt{\frac{1}{C_{res}(L_{res} + \frac{3}{2} L_c)}} \]  \hspace{1cm} (A.7)
\[ Z_{\text{res}} = \sqrt{\frac{L_{\text{res}} + \frac{3}{2}L_c}{C_{\text{res}}}} \]  

(A.8)

Outside the commutation interval the factors \(3/2\) appearing in equations A.7 and A.8 should be replaced by 2. A consequence of the changing impedance is that (with the usual scaling) the state plane trajectory of the commutation interval will be presented as an ellipse. The centre of this ellipse is situated at \((\frac{1}{2}(V_{LC1} + V_{LC2}), 0)\), and its eccentricity is \(\sqrt{(L_{\text{res}} + 2L_c)/(L_{\text{res}} + \frac{3}{2}L_c)}\). This ellipse has already been shown in figure A.2.

In order to obtain steady-state formulas we would like to follow a path similar to the derivation which has been presented for the simplified power circuit in section 2.3. The trajectories corresponding to the first and last current segments can be described by the following equations respectively:

\[ C_{\text{res}}(V_C - V_{LC1})^2 + (L_{\text{res}} + 2L_c)(I_{\text{res}})^2 = C_{\text{res}}(V_{C0} - V_{LC1})^2 \]  

(A.9)

\[ C_{\text{res}}(V_C - V_{LC2})^2 + (L_{\text{res}} + 2L_c)(I_{\text{res}})^2 = C_{\text{res}}(V_{C2} - V_{LC2})^2 \]  

(A.10)

and the trajectory during commutation is described by:

\[ C_{\text{res}}(V_C - \frac{V_{LC1} + V_{LC2}}{2})^2 + (L_{\text{res}} + \frac{3}{2}L_c)(I_{\text{res}})^2 = \text{constant} \]  

(A.11)

and by equation A.6.

The next step in the derivation à la section 2.3 would be to introduce the continuity of the state variables at the interval borders. Thus we obtain the following set of equations:

\[ C_{\text{res}}(V_{C1a} - V_{LC1})^2 + (L_{\text{res}} + 2L_c)(I_{\text{res1a}})^2 = C_{\text{res}}(V_{C0} - V_{LC1})^2 \]  

(A.12)

\[ C_{\text{res}}(V_{C1a} - \frac{V_{LC1} + V_{LC2}}{2})^2 + (L_{\text{res}} + \frac{3}{2}L_c)(I_{\text{res1a}})^2 = C_{\text{res}}(V_{C1b} - \frac{V_{LC1} + V_{LC2}}{2})^2 + (L_{\text{res}} + \frac{3}{2}L_c)(I_{\text{res1b}})^2 \]  

(A.13)

\[ \frac{V_{LC2} - V_{LC1}}{L_c} = \frac{I_{\text{res1b}} - I_{\text{res1a}}}{t_{1b} - t_{1a}} \]  

(A.14)

\[ C_{\text{res}}(V_{C1b} - V_{LC2})^2 + (L_{\text{res}} + 2L_c)(I_{\text{res1b}})^2 = C_{\text{res}}(V_{C2} - V_{LC2})^2 \]  

(A.15)

And this is where the derivation grinds to a halt. We have obtained four equations with four unknowns: \(I_{\text{res1a}}, V_{C1a}, I_{\text{res1b}},\) and \(V_{C1b}\). The values of \(t_{1a}\) and \(t_{1b}\) can in principle be derived from the state of the circuit. However, the relation between the state and these values is a goniometric function, and an explicit solution to the system of equations A.12 ... A.15 is not known. As has been suggested in section 3.8.3, it is still possible to obtain a solution to the equations by numerical iteration. We will not go into that matter any further here.
A.3 Interpretation

A mathematical solution to equations A.12 ... A.15 is not possible. Still, in order to understand the phenomena which appear in the circuit, we may try to apply some common sense to the equations derived so far. As has been noted before, we are most interested in the consequences of the commutation to the operation of the $V_{\text{cpeak}}$ predictor.

The predictor has been devised for the limiting case of a power circuit without commutation inductances, i.e. where $\sigma = 0$. If, starting from this situation, we gradually "turn up" the value of $\sigma$, the commutation interval will gradually widen. Examples of the corresponding waveforms have been depicted for three values of $\sigma$ in figure A.3.

![Waveforms](image)

Figure A.3: Shapes of the three branch currents and the capacitor voltage in the circuit of fig. A.1 for $\sigma \in [0.1, 0.5, 0.9]$ and $(V_{LC1}, V_{LC2})=(-400 \, V, 250 \, V)$. The arrows indicate rising values of $\sigma$.

In the simulations which produced figure A.3 the component values cor-
responding to the 6 kW converter were used. Contrary to the simplified situation in section A.1 the effects of snubbers were taken into account as well. Only the values of the main inductor \( L_{res} \) and the commutation inductances \( L_c \) were changed, as shown in table A.1.

<table>
<thead>
<tr>
<th>( \sigma )</th>
<th>( L_{res} ) ( \mu H )</th>
<th>( L_c ) ( \mu H )</th>
</tr>
</thead>
<tbody>
<tr>
<td>0.1</td>
<td>154</td>
<td>17</td>
</tr>
<tr>
<td>0.5</td>
<td>62</td>
<td>63</td>
</tr>
<tr>
<td>1.0</td>
<td>0</td>
<td>94</td>
</tr>
</tbody>
</table>

Table A.1: Inductor values for three values of \( \sigma \)

We see that due to the commutation the effective takeover of the current is delayed with respect to the instant that thyristor \( Th_2 \) is fired. This implies that less (too little) energy can be supplied to the resonant circuit during the second current segment, and consequently the peak capacitor voltage \( (V_{C2}) \) will drop, as is visible in the lower trace. It will be clear that if we fire thyristor \( Th_2 \) somewhat earlier, the peak capacitor voltage will rise, and that in this way we can, in principle, obtain the right value for \( V_{C2} \). That matter will be discussed further in appendix B.

To finish this section, we like to address the question in which areas of the \( (V_{LC1}, V_{LC2}) \) plane the influence of the commutation on the peak capacitor voltage will be the largest. The following reasoning can be applied:

- When either \( V_{LC2} \) or \( V_{LC1} \) is almost zero, the commutation occurs at the very beginning or end of the current pulse, respectively. As the value of the current to be commutated is rather small there, we may expect the influence to be relatively small as well.

- When the commutation voltage \( (V_{LC2} - V_{LC1}) \) is large, the commutation takes relatively little time (see equation A.14). This effect is marked even more because for large values of \( (V_{LC2} - V_{LC1}) \), approaching the peak capacitor voltage, the current in the resonant circuit is relatively small (the numerator in equation 2.20 approaches zero).

Consequently, the largest deviations of \( V_{C2} \) may be expected for relatively small, but not too small, values of \( V_{LC1} \) and \( V_{LC2} \). For these values, the commutation takes relatively long.

It is interesting to note here, that in the two-matrix topology, which is often used for DC-DC conversion, the commutation voltage is always large, twice the supply voltage. This may explain why commutation phenomena have until now received relatively little attention.
A.4 Examples

The shapes of the resonant and branch currents can change significantly compared to the simplified model when the commutation of current from the first to the second current segment takes a significant time. In the following figures we will present the waveforms of the currents in the three branches of figure A.1 for different values of $\sigma$ (as shown in table A.1), $V_{LC1}$ and $V_{LC2}$. The traces have been computed assuming that an (almost) ideal predictor (see appendix B) is present.

![Graph showing waveforms of currents](image)

Figure A.4: Traces of the currents $I_1$ (a), $I_2$ (b), and $I_{res}$ (c) in the three branches of figure A.1 for $\sigma = 0.1$. In every subfigure the simulation time ranges from 0 to 100 $\mu$s, the currents from $-10$ A to $+100$ A. The thyristors for the first current segment are fired at $t = 5\mu$s.

Figure A.4 shows the circuit behaviour at $\sigma = 0.1$, which comes close to the simplified model as has been presented in chapter 2. For most combinations of $V_{LC1}$ and $V_{LC2}$ the takeover of current from the first to the last
segment is almost immediate. A distortion of the current waves is visible which is due to the presence of snubbers in the simulated circuit. Only for very low values of the voltages applied to the circuit (lower right corner) the commutation takes a significant amount of time.

![Graph showing current vs. voltage](image)

**Figure A.5:** Traces of the currents $I_1$, $I_2$, and $I_{res}$ in the three branches of figure A.1 for $\sigma = 0.5$. Scaling as in figure A.4.

Comparison of the simulation results for $\sigma = 0.5$ in figure A.5 to the results for $\sigma = 0.1$ shows only slight differences. As might be expected, the commutation takes somewhat longer. For the low-voltage case in the lower right corner the commutation time is extended further, and now covers almost the complete resonant half wave. The large differences between the wave shapes in the lower right corner in figure A.5 and the idealized wave shapes (see for example figure 2.7) indicate why especially for low terminal voltages the $V_{cpeak}$ predictor will generate relatively large errors (see figure 6.7).

A further increase in $\sigma$ generates the traces as depicted in figure A.6. Here the main inductor is reduced to zero. Compared to figure A.5, in all
Figure A.6: Traces of the currents $I_1$, $I_2$, and $I_{res}$ in the three branches of figure A.1 for $\sigma = 1.0$. Scaling as in figure A.4.

cases the commutation takes longer.

For the lowest voltage combination, in the lower right corner of figure A.6, a peculiar wave shape can be seen. The second current segment, which is initiated at $t = 13\mu s$, crosses through zero before the resonant current (outer trace). Again, this particular wave shape was not taken into account when the $V_c$peak predictor we have used for the experiments was designed.

Even though the sequence of switching actions for this low voltage combination might appear to be somewhat counterintuitive, the simulation indicates that - in principle - control of the peak capacitor voltage is still possible. Furthermore, the current wave shapes for this case show low values for the $di/dt$, both at turn-on and turn-off, applied to every active thyristor in the circuit. This is a distinctive advantage with regard to switching losses.
A.5 Discussion

Virtually every series-resonant converter using thyristors as active elements needs to limit the $di/dt$ applied to these devices. For this purpose, commutation inductors are used. The presence of these inductors leads to the introduction of a commutation interval, where three thyristors are conducting simultaneously. Due to the time it takes for the current to commutate between the two branches involved, the operation of a "normal" Vcpeak predictor will be hampered.

In the situation without commutation inductances, an explicit analytical solution for the capacitor voltage at turnover is available. When commutation inductances are present, this is no longer the case. The formal analysis of the circuit leads to an implicit equation, and an explicit solution for $V_{C1}$ can not be found.

A straightforward interpretation of the equations which describe the behaviour of the circuit shows that the influence of the commutation might be expected to be the largest for relatively small values of the voltage difference $(V_{LC2} - V_{LC1})$. However, if either of these voltages is approaching zero, the influence of commutation reduces again. This observation is in good agreement with the simulation results as shown in figure 6.7.

For relatively low values of $(V_{LC2} - V_{LC1})$ and large values of the commutation inductances, the second current segment may actually be terminated before the first. The current waveforms associated with this situation are very smooth, but the "normal" predictor will not be able to provide adequate control of the peak capacitor voltage in this situation. However, the simulation results, which were obtained using a new optimal predictor algorithm (see appendix B), indicate that Vcpeak control is still possible.
Appendix B

A Digital Implementation of a Vcpeak Predictor

B.1 Introduction

The tight control of the state of the resonant circuit is of paramount importance for reliable operation of any series resonant converter. In a DC-DC SR converter the magnitudes of currents and voltages applied to the power semiconductors, which are the most vulnerable elements of the power circuit, are directly related to the state of the resonant circuit. The same can be said concerning the worst-case values of these variables in a multiphase SR configuration.

In chapter 3 a technique, Vcpeak prediction, has been introduced to control the state of the resonant circuit. In section 3.3.1 the basic operation of the Vcpeak predictor circuit has been treated. The operation of the predictor relies on an analytical model of the simplified power circuit of the converter. It has been suggested in section 3.8 that some phenomena which have not been included in this simplified power circuit could be included in the basic setup of the predictor. However, the predictor circuit would become much more complex, and the elegance of the design would be lost.

In section 6.8 we have shown that the phenomena which remained unmodelled in the simplified description of the converter do have a significant influence on the performance of the Vcpeak predictor. Therefore we were forced to use a margin on the peak capacitor voltage \((V_{C2})\) in order to guarantee sustained oscillation in the resonant circuit and proper turn off conditions for the thyristors.

In this appendix we would like to introduce a predictor setup which is able to cope with the complete converter circuit, including nonlinearities, commutation, thyristor voltage drops, resistive losses, snubbers, and reverse recovery. With this setup it is possible to control the peak capacitor voltage, and therefore the state of the resonant circuit, with a much higher accuracy.
than with the circuit we have used for the experiments.

The higher accuracy allows us to reduce the safety margin on $V_{C2}$. Therefore we can use a lower value for $V_{C2}$ than before, which allows us to use semiconductors with a lower voltage rating.

For reference, section B.2 presents the operating area in the $(V_{LC1},V_{LC2})$ plane of our original predictor (type #2). Section B.3 of this appendix introduces the basical idea behind the new predictor circuit, and in section B.4 we show the outcome of some simulation experiments with the new predictor circuit.

### B.2 Predictor type #2

The operation of predictor type #2 has been described in detail in section 7.3.2. Based on the initial state of the resonant circuit and the voltages to be applied to it, the value of the capacitor voltage at switchover is computed (see equation 7.13). A comparison of this value with the actual measured capacitor voltage indicates when the turnover to the second current segment should be initiated.

The operation of this circuit for one value of the initial capacitor voltage $V_{C0}$ and one value of the final capacitor voltage $V_{C2}$ can be presented with contours for $V_{C1}$ in the $(V_{LC1},V_{LC2})$ plane. These contours are shown for three values of $V_{C0}$ in figures B.1, B.2, and B.3.

![Diagram](image)

**Figure B.1:** Contours for $V_{C1}$ (in volts) for $V_{C0} = -750$ V

The contours for $V_{C1}$ show up as straight lines in the $(V_{LC1},V_{LC2})$ plane. The exact relation between $V_{LC1}$ and $V_{LC2}$ can be derived after rewriting...
Figure B.2: Contours for $V_{C1}$ (in volts) for $V_{C0} = -800 \, V$

Figure B.3: Contours for $V_{C1}$ (in volts) for $V_{C0} = -850 \, V$

equation 7.13 as follows:

$$V_{LC1}(2V_{C1} - 2V_{C0}) + V_{LC2}(-2V_{C1} + 2V_{C2}) = V_{C2}^2 - V_{C0}^2 \quad (B.1)$$

For given values of $V_{C1}$, $V_{C0}$ and $V_{C2}$ equation B.1 defines straight lines in the
(V_{LC1}, V_{LC2}) plane. If V_{C2} = -V_{C0}, then the lines pass through the origin. This is the situation which is described by equation 2.16.

B.3 Background of the new circuit

For the real power circuit, including the unmodelled phenomena which were mentioned in the introduction, an analytical derivation for V_{C1} is not possible. However, for a fixed topology of the power circuit, assuming time-independent values for the circuit elements, the value for V_{C2} is completely fixed if the values for V_{C0}, V_{LC1}, V_{LC2}, and V_{C1} are known. In other words, the circuit is fully deterministic. Furthermore, the physical operation of the circuit indicates that, for given values for V_{C0}, V_{LC1}, and V_{LC2} the relation between V_{C1} and V_{C2} is monotonous. Roughly said: the longer we wait to start the second current segment, the lower the value of V_{C2} will become.

We can view the inverse of this V_{C1}-V_{C2} relation (which, due to the monotonicity, exists) as the desired behaviour of an optimal Vcpeak predictor circuit. Even though an analytical expression of this behaviour can not be derived, it is possible to tabulate the values of V_{C1} for the ranges of V_{C0}, V_{LC1}, and V_{LC2} of interest.

A practical problem associated with the use of a table is the total size needed in an implementation. If we would like to specify the three inputs to the table (V_{C0}, V_{LC1}, V_{LC2}) with an accuracy of ca. 1%, i.e. represented each by 7 bits, we would need a table with 2^{21} = 2M entries. With the present-day availability of 2 Mbit Eproms, and higher densities available in the near future, this table could therefore be implemented straightforward in hardware. It is possible to obtain a huge reduction of the table size if we consider that, once the system runs, the peak capacitor voltage will be confined to a small margin around the intended value for V_{C2}. Using this, we need to implement the table only for this range of V_{C0}, which can be done with only, say, 4 bits resolution. Also, we need to fill the table only for half of all possible combinations of V_{LC1} and V_{LC2}. Using these two techniques, the table would reduce to 128k bytes. Still another significant reduction of the needed table size may be obtained if interpolation techniques are used.

Two methods for obtaining the table with values for V_{C1} will be discussed in the following.

B.3.1 Filling the table by simulation

A first approach to filling the table would be to use the detailed models which we have presented in chapter 5 in a simulation context. Using the value for V_{C1} given in equation 7.13 as a starting point, the correct value for V_{C1} can be iteratively found after only a few simulation runs for each triple of (V_{C0}, V_{LC1}, V_{LC2}). This is the approach we have used to obtain the table for the simulation experiments in section B.4. It must be noted that this method has two shortcomings:
Background of the new circuit

- It takes a large amount of computer time, and
- it relies heavily on the precision of the model.

Both shortcomings can be solved by using the following method.

B.3.2 Filling the table by experiment

The iterative method can be applied much faster by using the hardware of the converter directly. If we use a computerized setup to perform measurements of the values of \( V_{C2} \), \( V_{LC1} \), and \( V_{LC2} \), and to control the value of \( V_{C1} \), it is feasible to obtain a new table entry after 10 to 100 resonant halfcycles, so every 1 to 10 milliseconds. With this method, a complete 2 megabyte table can therefore be filled in a few hours, and the filling of a 128k byte table can be a matter of minutes.

B.3.3 Contours of the optimized predictor circuit

With either approach, we obtain a table with values for \( V_{C1} \) as a function of \( V_{LC1} \), \( V_{LC2} \), and \( V_{C0} \). For a specific value for \( V_{C0} \), the table can again be represented with a contour plot in the \((V_{LC1}, V_{LC2})\) plane. An example of this plot, obtained by the simulation approach, is shown in figure B.4.

![Figure B.4](image-url)

Figure B.4: Contours for \( V_{C1a} \) (in volts) for \( V_{C0} = -800 \) V, with thyristor junction capacitance, reverse recovery, and saturating inductors taken into account

Comparison of the contours in figure B.4 with those in figure B.2 shows that the optimal operation of a predictor differs significantly from the op-
eration of the predictor which has been used in the experimental setup as reported in chapter 8.

B.4 Performance of the new predictor

For the evaluation of our concept, the operation of the new table-oriented predictor needs to be compared to the performance of the old analytic setup. For the comparison, we have computed the table values for the 6 kW power circuit by simulation. In order to obtain some resemblance to a practical implementation, the values of $V_{LC1}$ and $V_{LC2}$ were discretized with 6 bits (64 values) over the range of interest, which was chosen to be $0 \pm 700\, V$. The computed value for $V_{C1}$ was discretized with 8 bits (256 values), over the range of $-800 \pm 800\, V$.

For brevity, we will only show the performance of the new predictor assuming that the initial value of the capacitor voltage ($V_{C0}$) equals $-800\, V$.

![Figure B.5: Operation of the new table-oriented predictor. Contours for the peak capacitor voltage $V_{C2}$ (in volts) for $V_{C0} = -800\, V$](image)

Figure B.5 shows the operation of the new predictor. In order to show the effects of the discretization of the table, we have evaluated the predictor operation over a grid of 70 times 70 points, i.e. with steps for both $V_{LC1}$ and $V_{LC2}$ of 10 $V$. As the table is implemented on a 64 times 64 grid (6 bits for both $V_{LC1}$ and $V_{LC2}$), the actual values for $V_{LC1}$ and $V_{LC2}$ need to be rounded to the nearest table entry. The result is that the value for $V_{C1}$ used in the evaluation has a periodic error, which leads to peculiar contours for $V_{C2}$. Nevertheless, comparison of the contours in figure B.5 with those in
figure 6.11 shows that the peak capacitor voltage here is confined to a much smaller range.

B.5 Discussion

The resonant $L - C$ circuit is the very heart of a series-resonant converter. Tight control of the state of this circuit is very important for the proper operation of the whole converter. For this purpose a circuit, the Vcpeak predictor, has been introduced in chapter 3. The intended operation of this circuit was derived analytically from a simplified model of the power circuit.

It has been shown by simulation in chapter 6 and by measurement in chapter 8 that, due to several unmodelled phenomena, the operation of the simplified model of the power circuit and the real setup differ to some extent. Consequently, the control of the state of the resonant circuit is not as tight as we would like it to be.

In this appendix we have shown that, starting from a somewhat different viewpoint, it is in principle possible to obtain tighter control of the state of the resonant circuit than with the approach which we have used in the experiments. The control of the state of the circuit is model-based, as it was before. However, a much more complete model was used, and the analytical problems associated with this high-order model solved using iteration. An even more appealing approach could be to use the power circuit itself, the best model there is, for the iterations. Using measurements taken from the circuit in operation, the table could be adapted in order to take care of aging of components and relatively slow thermal phenomena.

The Vcpeak control method we have described here makes it possible to use large values for the commutation inductances ($L_c$) without losing accuracy in the Vcpeak controller. With these large values, snubber losses can be reduced, and due to the resulting reduction in the $di/dt$ it might be expected that switching losses in the thyristors are reduced as well.

In the limiting situation we could even leave out the resonant inductor completely ($\sigma = 1$). This setup allows a somewhat simpler construction of the power circuit. However, the consequences for the efficiency of the circuit should be evaluated with care.
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Notation

$\text{ASD}_i$ ........ Output of current ASDTIC controller
$\text{ASD}_s$ ........ Sum of all individual ASDTIC signals
$\text{ASD}_u$ ........ Output of voltage ASDTIC controller
$A_u$ .......... Voltage scaling factor in measuring circuits
$C_b$ .......... See fig. 5.9
$C_d$ .......... Snubber capacitor
$C_f$ .......... Filter capacitor
$C_{f1}$ .......... Input filter capacitor
$C_{f2}$ .......... Output filter capacitor
$C_i$ .......... Input filter capacitor
$C_o$ .......... Output filter capacitor
$C_0$ .......... See formula 5.4
$C_{res}$ ........ Capacitance in the resonant circuit
$C_{th}$ ........ Capacitance of thyristor junction
$D$ .......... See equation 2.2
$E_{ex}$ ........ Excess energy (see eq. 3.17)
$\eta$ .......... Efficiency of the converter
$\text{Err}$ .......... Error signal
$E_c$ .......... Energy absorbed by the resonant circuit
$E_s$ .......... Supply voltage
$f_{av}$ .......... Average frequency
$f_{res}$ .......... Undamped resonant frequency
$G$ .......... Admittance for reactive power at input of converter
$I_{av}$ .......... Average of rectified resonant current
$I_{eff}$ .......... Effective value of resonant current
$I_{th}$ .......... Thyristor current
$I_{thav}$ .......... Average of thyristor current
$I_{theff}$ .......... Effective value of thyristor current
\( I_d \) . . . . . . . . . . . . . . Difference of currents in two commutating branches
\( I_1 \) . . . . . . . . . . . . . . . Current in first branch of commutating circuit
\( I_2 \) . . . . . . . . . . . . . . . Current in second branch of commutating circuit
\( I_{peak} \) . . . . . . . . . . . . . Peak value of resonant current
\( I_i \) . . . . . . . . . . . . . . . Input current
\( I_{io} \) . . . . . . . . . . . . . . Reactive part of input current
\( I_o \) . . . . . . . . . . . . . . . Output current
\( \dot{I}_o \) . . . . . . . . . . . . . Peak output current
\( I_{res} \) . . . . . . . . . . . . . Value of resonant current
\( I_{res0} \) . . . . . . . . . . . . . Initial value of resonant current
\( I_{res1a} \) . . . . . . . . . . . . . Value of resonant current at \( t = t_{1a} \)
\( I_{res1b} \) . . . . . . . . . . . . . Value of resonant current at \( t = t_{1b} \)
\( I_{RR} \) . . . . . . . . . . . . . . Peak of reverse-recovery current
\( I_s \) . . . . . . . . . . . . . . . Treshold value in junction charge model (see equation 5.6)
\( I_{res,sc} \) . . . . . . . . . . . . Scaled version of \( I_{res} \)
\( I_{TM} \) . . . . . . . . . . . . . . . Peak value of current for \( Q_{RR} \) test
\( K_i \) . . . . . . . . . . . . . . . Scaling factor in current measurements
\( K_u \) . . . . . . . . . . . . . . . Scaling factor in voltage measurements
\( k_0 \) . . . . . . . . . . . . . . . See formula 5.3
\( L_c \) . . . . . . . . . . . . . . . Non-saturating part of snubber inductance
\( L_d \) . . . . . . . . . . . . . . . Total snubber inductance
\( L_{res} \) . . . . . . . . . . . . . Inductance in the resonant circuit
\( L_s \) . . . . . . . . . . . . . . . Saturating part of snubber inductance
\( L_0 \) . . . . . . . . . . . . . . . See formula 5.3
\( N_{TR} \) . . . . . . . . . . . . . . . Winding ratio of current measuring transformer
\( \omega_{res} \) . . . . . . . . . . . . . Undamped angular resonance frequency
\( \Phi \) . . . . . . . . . . . . . . . . . . . . . . Estimate for input power of converter
\( P_f \) . . . . . . . . . . . . . . . . . . . . . . Power factor
\( P_{in} \) . . . . . . . . . . . . . . . . . Input power of converter
\( P_{loss} \) . . . . . . . . . . . . . . . Power loss in converter
\( P_{out} \) . . . . . . . . . . . . . . . Output power of converter
\( \psi_{r} \) . . . . . . . . . . . . . . . Delay angle
\( P_{snub} \) . . . . . . . . . . . . . . . Power loss in snubbers
\( P_{th} \) . . . . . . . . . . . . . . . Power loss in one thyristor
\( P_{tot} \) . . . . . . . . . . . . . . . . Total power dissipation
\( Q \) . . . . . . . . . . . . . . . . . . . . . . Quality factor of resonant circuit
\( Q_{junc} \) Junction charge in charge-control model
\( Q_{rr} \) Reverse-recovery charge
Ripp Relative ripple
\( R_o \) Load resistance
\( R_1 \) Distance from trajectory to \((V_{L,C2}, 0)\)
\( R_2 \) Radius of trajectory for second current segment
\( R_b \) See fig. 5.9
\( R_d \) Snubber resistance
\( R_{tr} \) Equivalent terminating resistor of current measuring transformer
\( R_{thj} \) Thermal resistance between junction and case
\( R_{thc} \) Thermal resistance between case and heatsink
\( R_{thha} \) Thermal resistance between heatsink and ambient
\( R_{thja} \) Thermal resistance between junction and ambient
\( S_1 \) Semiconductor switch
\( S_2 \) Semiconductor switch
\( S_3 \) Semiconductor switch
\( S_4 \) Semiconductor switch
\( t_0 \) Time at start of first current segment
\( t_1 \) Time at boundary between first and second current segments
\( t_{1a} \) Time at boundary between first and commutation current segments
\( t_{1b} \) Time at boundary between commutation and last current segments
\( t_2 \) Time at end of second current segment
\( T_{sw} \) Matrix of switch positions
\( T_{swl} \) Matrix of switch positions for left bridge
\( T_{swr} \) Matrix of switch positions for right bridge
\( t_p \) Duration of a resonant halfcycle
\( t_q \) Turn-off time of thyristor
\( T_a \) Ambient temperature
\( T_{ch} \) Temperature difference between case and heatsink
\( T_{ha} \) Temperature difference between heatsink and ambient
\( T_j \) Junction temperature
\( T_{ja} \) Temperature difference between junction and ambient
\( T_{jc} \) Temperature difference between junction and case
\( T_{jh} \) Temperature difference between junction and heatsink
\( T_{jmax} \) Maximum allowed junction temperature
$U_k \ldots \ldots \text{See figure A.1}$
$U_1 \ldots \ldots \text{See figure 5.6}$
$U_i \ldots \ldots \text{Input voltage}$
$U_o \ldots \ldots \text{Output voltage}$
$\bar{U}_o \ldots \ldots \text{Peak output voltage}$
$\mu s \ldots \ldots \text{Microsecond}$
$U_2 \ldots \ldots \text{See figure 5.6}$
$V_{ak} \ldots \ldots \text{Voltage across an SCR}$
$V_C \ldots \ldots \text{Value of capacitor voltage}$
$V_{C_{se}} \ldots \ldots \text{Scaled version of } V_C$
$V_{C_0} \ldots \ldots \text{Initial value of capacitor voltage (at } t = t_0)$
$V_{C_{1\ldots \ldots \text{Value of capacitor voltage at } t = t_1)}$
$V_{C_{1a}} \ldots \ldots \text{Value of capacitor voltage at the beginning of the commutation interval (} t = t_{1a})$
$V_{C_{1b}} \ldots \ldots \text{Value of capacitor voltage at the end of the commutation interval (} t = t_{1b})$
$V_{C_2} \ldots \ldots \text{Final value of capacitor voltage (at } t = t_2)$
$V_{C_{2se}} \ldots \ldots \text{Scaled version of } V_{C_2}$
$V_{ext} \ldots \ldots \text{Voltage external to the resonant converter}$
$\bar{V}_{in} \ldots \ldots \text{Vector of input voltages of the converter}$
$V_{LC} \ldots \ldots \text{Voltage across resonant circuit}$
$V_{LC1} \ldots \ldots \text{Voltage across resonant circuit during first current segment}$
$V_{LC2} \ldots \ldots \text{Voltage across resonant circuit during second current segment}$
$V_{LC_{2se}} \ldots \ldots \text{Scaled version of } V_{LC_2}$
$\bar{V}_{out} \ldots \ldots \text{Vector of output voltages of the converter}$
$V_{rip} \ldots \ldots \text{Ripple voltage (peak-peak)}$
$V_0 \ldots \ldots \text{See formula 5.4}$
$W_{snub} \ldots \ldots \text{Energy loss in snubbers}$
$W_p \ldots \ldots \text{Energy dissipation during one resonant pulse}$
$Y_{res} \ldots \ldots \text{Admittance of the resonant circuit}$
$Z_{res} \ldots \ldots \text{Impedance of the resonant circuit}$
Summary

Starting in the early sixties, resonant power converters have been developed in order to overcome the restrictions caused by switching losses in power semiconductors. Due to the presence of a resonant circuit, values for the \( \frac{di}{dt} \) applied to the semiconductors can be limited. Consequently, switching losses are reduced, and higher operating frequencies can be reached.

Initially, resonant converters were used mainly to generate high-frequency AC power from a DC source. Addition of a rectifier makes it possible to supply DC power to a load. However, with this addition the control of the converter becomes more complex.

The topology of the power circuit of the DC-DC resonant converter can easily be extended to cater to multiphase applications. Another extension, phase-staggering, makes it possible to operate several converter modules in parallel. In this way the maximum power of a converter can be raised substantially, while at the same time increasing the effective inverter frequency.

In multiphase applications, the resonant \( L - C \) circuit is time shared by all phases. The control circuit needs to ascertain that every phase is serviced adequately, while maintaining the integrity of the power circuit. A problem arises here because the voltages applied to the resonant circuit, which are taken from different phases for subsequent cycles of the resonant current, do - contrary to the single-phase DC-DC converter - not necessarily balance over time. This may cause the oscillation in the resonant circuit to die out, or worse, to become unbounded, leading to destruction of the components of the power circuit.

The integrity of the power circuit can be assured if maximum voltages and currents in the resonant circuit, which lies at the very heart of the converter, can be kept below a predefined maximum. An important measure for both the maximum voltage and the maximum current in the resonant tank is the peak capacitor voltage \( V_{\text{peak}} \). Control of the value of \( V_{\text{peak}} \) implies control of the maximum voltages and currents applied to every element of the power circuit. The structure of a simplified, idealized model of the power circuit suggests a way to control the value of \( V_{\text{peak}} \), independent of the magnitude of the phase voltages which are used.

Under classic current control, paralleled converter modules tend to become synchronized. The purpose of phase-staggering control is to counteract
this behaviour, in order to obtain equal load-sharing between the paralleled modules and a higher effective inverter frequency. For this purpose, a prediction of the total charge displaced by every current pulse is computed, and injected in the current controller.

Before construction of a prototype converter equipped with the new control system, the design of the converter hardware and the operation of the control algorithm need to be checked by means of simulations. For use in the simulations simple models are derived. Parameters for these models can be obtained either from easy to perform experiments, or from manufacturer's data sheets. The actual simulations are performed using several dedicated computer programs.

Two converter systems are constructed and tested. The first converter is a 15 kW system, converting power from the three-phase 380 V utility grid to a three-phase output. Measurements show that the system features high efficiency over a large section of the operating area, and very fast control.

With the experience gained from the 15 kW setup, another system was constructed for 6 kW operation. This system was conceived especially to demonstrate the possibility of phase-staggering control. Measurements on this converter are shown to illustrate a variety of features, the most important being the operation of the Vcpeak controller, and phase-staggering control under AC conditions.
Samenvatting

Vanaf de zestiger jaren worden resonante technieken toegepast in elektronische vermogensomzetters. Dankzij de aanwezigheid van een resonant circuit kan de steilheid van de stromen in de halfgeleiders (di/dt) worden beperkt. Door de hiermee samenhangende lage schakelverliezen in deze vermogenshalfgeleiders kunnen hogere schakelfrequenties dan gebruikelijk worden toegepast.

De eerste toepassingen van resonante omzetters lagen op het gebied van hoogfrequente verwarming van materialen. De resonante omzetter maakt het mogelijk om met de beschikbare halfgeleiderschakelaars met hoog rendement energie uit een gelijkspanningsbron om te zetten naar de gewenste hoge uitgangsfrequentie. Toevoeging van een gelijkrichtbrug maakt het ook mogelijk om gelijkstroom te genereren. Door deze toevoeging wordt de omzetter echter lastiger om te regelen.

De topologie van een gelijkstroom-gelijkstroom omzetter, welke voornamelijk is opgebouwd rond twee éénfase bruggen van vermogenshalfgeleiders, kan eenvoudig worden uitgebreid naar meerdere fasen aan in- en/of uitgang. Een tweede uitbreiding van het concept bestaat uit het parallel schakelen van meerdere omzettermodule. Hiermee kan een hoger vermogensniveau worden bereikt, terwijl tegelijkertijd de effectieve omzetterfrequentie toeneemt.

In meerfasenomzetters wordt de resonante $L - C$ kring gedeeld door alle in- en uitgangfasen. Een regelaar zorgt er voor dat elke fase naar behoefte wordt bediend, zodanig dat de gewenste stroom- en spanningsvormen worden gegeneereerd en overbelasting van het vermogensdeel wordt voorkomen. Ten opzichte van de éénfasecircuit ontstaat een extra probleem, doordat de spanningen die worden toegevoegd aan de resonante kring, welke voor opeenvolgende stroompulsen afkomstig zijn van telkens verschillende fasen, niet noodzakelijkerwijs in balans zijn. Zonder extra maatregelen zou hierdoor de slingerigheid in de resonante kring uit kunnen dement of, erger, ongeremd kunnen toenemen. Dit kan leiden tot beschadiging van de onderdelen van het vermogenscircuit.

Beschadiging van het vermogensdeel van de omzetter kan worden voorkomen wanneer de spanningen en stromen in de resonante kring, het ‘hart’ van de vermogensomzetter, onder een maximum gehouden kunnen worden. Een belangrijke maat voor zowel de maximum spanningen als -stromen in de
Samenvatting

resonante kring is de topspanning over de resonante condensator (Vcpeak). Beheersing van deze waarde leidt automatisch ook tot beheersing van spanningen en stromen in de overige componenten van het vermogensdeel. Uit een vereenvoudigd model van het gedrag van het vermogensdeel wordt een regelaar met een niet-lineaire structuur afgeleid, die in staat is om, onafhankelijk van de spanningen welke extern worden toegevoerd, de waarde van Vcpeak binnen nauwe marges vast te leggen.

Wanneer een ‘klassieke’ stroomregeling wordt toegepast vertonen parallel geschakelde omzettermodulen de neiging om te synchroniseren. Door een aanpassing van de regeling, met gebruik van niet-lineaire voorwaartskoppeling, wordt deze ongewenste synchronisatie voorkomen. In de voorwaartskoppeling wordt een voorspelling berekend van de totale verplaatste lading in de desbetreffende resonante stroompuls, en deze waarde wordt geïnjecteerd in de ‘klassieke’ stroomregeling. Deze methode leidt tot een hogere effectieve omzetterfrequentie, en tot gelijke verdeling van het te bewerken vermogen over de parallel geschakelde modulen.

Vóór de bouw van een prototype van een omzetter uitgerust met de nieuwe regelingen is het zinvol om de werking van het gehele systeem te verifiëren met behulp van simulatie. Voor gebruik in deze simulaties worden een aantal eenvoudige modellen afgeleid. De parameters voor deze modellen kunnen worden bepaald aan de hand van eenvoudig uit te voeren metingen, of worden afgeleid uit gegevens die verstrekt worden door de fabrikanten van de onderdelen van het vermogenscircuit. Voor de eigenlijke simulaties wordt een aantal verschillende programma’s toegepast, welke ieder een eigen aspect van de werking van de omzetter en de regeling benadrukken.

Twee omzettes zijn daadwerkelijk gebouwd en getest. De eerste omzetter is in staat om 15 kW om te zetten tussen twee 380 V driefasensystemen. Met metingen wordt aangetoond dat deze omzetter een hoog rendement haalt over een groot deel van het werkgebied.

Aan de hand van de ervaringen opgedaan met de 15 kW omzetter is een tweede omzetter, ditmaal voor een vermogen van 6 kW, gebouwd. De nadruk bij dit ontwerp ligt op de mogelijkheid om meerdere modulen parallel te schakelen. Met metingen aan deze omzetter wordt de werking van de besturingselektronica gedemonstreerd. Speciaal wordt aandacht gegeven aan de regeling van de topspanning op de resonante condensator, en aan het parallel schakelen van twee omzettermodulen. De metingen geven aan dat de methode die gebruikt wordt om ongewenste synchronisatie van de modulen tegen te gaan ook bij het genereren van wisselstroom uit een gelijkstroombron haar taak naar behoren vervult.
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