OLFAR: DESIGN OF LOW FREQUENCY RECEIVER

This document is a master thesis work done by Edwin Wiek for the Delft University of Technology. OLFAR will be the first cube sat array which makes it possible to receive signals from the early space.
Introduction

In this thesis work an OLFAR chip has been designed. This thesis is written by Edwin Wiek, Master student of the micro-electronics department of the TU Delft. First of all I will give you a short introduction in what OLFAR is about:

During the big bang, 13 billion years ago, a lot of hydrogen was blown into the universe. This hydrogen has a well-known frequency (1420.40575 MHz) can be received still now. With this data we can retrieve information about things like: how much hydrogen was there, how stars form and lots more scientific questions. How can it be that we can still measure those signals, which are generated such long ago? That is easy: as proven by HUBBLE, the universe is expanding. Things that happened in the beginning of the universe are on the boundary of our universe, what we thus know is that everything moves. Hubble has proven that the further away, the faster the speed. When moving with a higher speed, a higher Doppler shift can be found. Thus the signals which are generated by the hydrogen during and after the big-bang are still in the sky, only with a lower frequency and signal strength. These signals are now such that they are in the galactic noise, by receiving this noise and using convolution techniques, we can retrieve this H1 line. More about OLFAR can be found at [13].

Some of these signals are already received by LOFAR, which is a very large antenna array which receives frequencies with a minimum of 20 MHz, and that is where OLFAR gets interesting. OLFAR will do the same as LOFAR but there will be measured from space, and not from the earth. Due to ionosphere blockage it is impossible to receive signals lower as 20 MHz on earth. OLFAR however will be in space, and thus these signals can be received. For this reason we are interested in the signals from 30 kHz till 30 MHz. These signals will be sent to earth, where the calculation can be done and so trying to retrieve the HI-line which gives us all the information about the past.

OLFAR will consist of several cube-sats, which will probably fly in formation, such that they form a large antenna, to receive all the signals of interest. OLFAR will fly around the moon to prevent the problem that too much terrestrial noise will be received, but OLFAR will probably first fly with the delfi-n3Xt (a student satellite of the TU-Delft). This will only be a proof-of-concept, before the entire OLFAR mission will be started, and will be in a kind of transponder. For the antenna system just one system will be used for both receiving and transmitting, this is because OLFAR will be a cube-sat, so there is no place for more antennas.

This thesis is about the low frequency receiver, which translates the signal to such a frequency that it can be sent to earth. The measured frequency is adjustable between 30 kHz and 30 MHz.

I have had a great time on the 18th floor of the EEMCS building of the TU-Delft, for this I want to thank: Robin Kearey, Robin van Eijk, Sheng Li, Ronald de Bock, Christiaan Hartman, Maurits Schaap, Wolter van der Kant for their help and good and funny time on our room. I would also like to thank Marion de Vlieger for her help with everything I needed. Special thanks are there for dr. ir. C.J.M. Verhoeven (Associate Professor TU Delft) and dr. ir. G.L.E. Monna (Systematic) which where my direct supervisors, and helped me during the entire project. Also I would like to thank everyone at home: my parents, my girlfriend, my brothers and their partners, for their support during this graduation period.
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Summary

An entire chip, in AMS 0.35 µm technology, has been designed in this thesis. This chip contains the entire front-end for delfi-n3Xt to receive the red-shifted H1 signal, in the frequency band of: 0.03 MHz till 30 MHz. This signal has been generated such long ago that it is covered by the galactic noise. This noise should be received and amplified so that it could be sent back to earth; the level of this signal is expected to be about -120 dB. The red-shifted H1 line is a correlated signal, thus by using convolution techniques it could be retrieved.

The OLFAR chip will fly with delfi-n3Xt as a proof of concept, when it showed its successful operation it will be converted to a cube-sat. The antenna system of delfi-n3Xt has been fully characterized, with this information the input, a LNA, has been constructed. For the OLFAR satellite an antenna configuration has been chosen: a tripole gave the best results. For delfi-n3Xt two antennas are used and for OLFAR three antennas are used, the reason for this is that the transmitted signal had to be canceled. By using the phase shifted transmitting signals; they could suppress itself on the input of the LNA.

The LNA has a gain of 28 dB nominal and an equivalent input noise of -146 dB. After this amplification a buffer has been added to provide low output impedance for the next stages. The input range is said to be 30 kHz till 30 MHz, so two frequency steps has been used. First an up-conversion to 50.7 MHz has been made. Second a down-conversion to 10.7 MHz has been made, since delfi-n3Xt requires the output of the OLFAR chip to be at this frequency. To do these conversions two mixers are added, one of them is driven by a PLL, the other by a crystal oscillator (40 MHz).

The range of the PLL equals 0 MHz till at least 55.6 MHz. The output frequency of this PLL can be set by a user-defined division number. A differential to single-ended conversion has been made since the output of the mixer is a differential signal, and the output of the mixer should be combined to suppress the RF signal.

A crystal filter has been added after the second mixer, to keep between the bandwidth as specified by delfi-n3Xt (50 kHz). At the output an AGC has been added to use as much as possible of the dynamic range.

The total gain can be varied between at least -19.45 dB and 123.38 dB. This means that we can handle input signals of: -161.17 dB till -2.45 dB. The output level can be set with a maximum of 1.0 V swing.

The entire design has been tested and simulated. Also the chip-layout has been designed and fully checked. The AMS technology has been used for this device. The total area of the chip is 2015 µm X 2015 µm. Also ESD problems play a great role; also this has been taken into account while designing the chip. The chip has 28 pins; most of them are there for testing purposes.

The testing of the chip has not been done jet, but a test circuit has been added. An entire test-plan has been proposed to test each sub-circuit.

For the OLFAR project the chip has to be changed a little: there has to be added another input for the third antenna, compared to the delfi-n3Xt antenna system, which only has two inputs. This input can be easily connected with a resistor to the input of the LNA.
1. Design Procedure

In this thesis work a receiver for receiving at low frequencies (0.03 MHz-30 MHz) in space will be designed. This receiver will be tested on the student satellite of the TU Delft, called delfi-n3Xt (the successor of the delfi-c3). When this receiver seems to be stable and proven its functionality in space it will be converted to a cube-sat. OLFAR is a project where several of these cube-sats will fly around the moon to retrieve as much information as possible about the Early Universe. The used receiver can be used in both cases; only the antenna structure needs to be redesigned for the OLFAR case.

Two different receiving networks will be designed, for delfi-n3Xt we are restricted to the antennas which are already there, for OLFAR a new antenna design has to be made. Delfi-n3Xt has two sets of antennas, one for transmitting at 435 MHz and one for receiving at 145.9 MHz. There is the desire to use only one antenna set for both receiving and transmitting. For this reason we use the 145.9 MHz antenna set.

![Diagram of OLFAR and delfi-n3Xt implementation](image)

For OLFAR we are free to design the entire antenna set. This gives us the opportunity to look at different antenna setups.

A look at the characteristics of the delfi-n3Xt antennas will be taken. For OLFAR several antenna configurations are characterized and the most suitable has been chosen. Both satellites are dealing with a 12 V transmitting signal, which should not be seen at the input of the Amplifier. All these parts are dealt with in chapter 2.

To determine which parts are required on the OLFAR chip a short look has been taken on the functionality of the chip. A look at the frequency steps which need to be taken is done in 1.1. In 1.2 a decision at the gain, which should be met by entire configuration, has been taken. With this information a configuration has been proposed (1.3), and some properties for each part are specified in 1.4.
1.1. Frequency steps
We know that the input frequency range equals 0.03 MHz till 30 MHz. The output frequency needs to be 10.7 MHz, since this is the frequency which has been used internally on the delfi-n3Xt transmitter. So the only question is which steps need to be taken to get there. The following is proposed: first we step up to 50.7 MHz, after this we can easily step down to 10.7 MHz. The reason that we took this conversion is because otherwise we would have the problem that the 10.7 MHz input signal is in the middle of the required input range. In that case it would be hard to separate information for example from 20.7 MHz and 0.7 MHz. The proposed frequency steps are shown below:

![Diagram showing frequency steps](image)

1.2. Required Gain
The input signal is very small, since its information is correlated in the galactic noise. In chapter 2 the level of this galactic noise will be reviewed more, but a global calculation can be made. Assuming a 1 µV input signal (-120 dB) and an output signal of at least (-20 dB), a gain of at least 100 dB is required. For the large input signals we see that we should have much less gain, assuming an input signal of -40 dB, a gain of maximal 40 dB is required, taking 0 dB as the maximum output. Summarizing this:

<table>
<thead>
<tr>
<th>Table 1 - gain properties</th>
</tr>
</thead>
<tbody>
<tr>
<td>Min</td>
</tr>
<tr>
<td>Input range</td>
</tr>
<tr>
<td>Required gain</td>
</tr>
<tr>
<td>Output range</td>
</tr>
</tbody>
</table>
1.3. Proposed configuration

Figure 3 shows the proposed configuration. At first a Low-Pass filter can be found, which is used to suppress the transmitting signals. A Low-Noise-Amplifier has been added for amplifying the input signal and adds as less noise as possible. A buffer has been added to have low output impedance. A mixer and phase-locked-loop are there to realize the first frequency step, to 50.7 MHz. The mixer will have a differential output, and the same will be used later, so we have to convert this output to a single ended signal. After this conversion the signal will be converted to 10.7 MHz by another mixer, with a local-oscillator of 40 MHz. To filter out all the unwanted signals a crystal filter has been added, since it is known to have a high Q-factor. At the output an automatic-gain-control block has been used to obtain the gain range as discussed before.

This figure also shows which part will be discussed in which chapter.

1.4. Properties for each block

The properties which should be met by each block are defined in this chapter. All the schematics of the blocks can be found in Appendix G.

1.4.1. Low Noise Amplifier

The LNA should have a gain of 28 dB with ranges between 20 dB and 40 dB over all corners over the entire frequency range. The reason that this gain is between quite some large limits is because we will have to deal with large resistors, due to the high ohmic antennas, and this can cause several problems. The noise of the LNA should be well known and be as low as possible. The signal of interest can be filtered of the galactic noise and the noise added by the system, by using convolution techniques, which are beyond the scope of this thesis. The frequency range needs to be 0.03 MHz till 30 MHz. The distortion levels should be below 40 dB, because in that case we are sure that the distortion signals are below the noise floor. This part will be discussed in Chapter 3.
1.4.2. Buffer
A buffer is required since the LNA will have a small loop-gain, for this reason it would have large output impedance. To overcome this problem a buffer has been added. Since this is a buffer it should have a gain of 0 dB. For the noise the same restriction holds. The frequency range of this amplifier should be 0.03 MHz till 30 MHz. Also a low output resistance is required. For the distortion levels have the same requirements as for the LNA. This part will be discussed in Chapter 4.

1.4.3. PLL
The only requirement for this part is that we need an output voltage range of 20.7 MHz till 50.67 MHz. The settling time should not be too large, but it has no exact maximum. This part will be discussed in Chapter 6.

1.4.4. Differential-to-single-ended
For this amplifier the following requirements hold: the working frequency is 50.7 MHz. For the noise again the same level holds, thus -120dB. We want here \(\frac{\pi^2}{4}\) gain, thus 7.84 dB. This is because we will have some loss at the mixers, which equals \(\frac{\pi}{2}\) per mixer, so to compensate for this loss we want this converter to have some gain. The Harmonic distortion at this point is of less importance, because it will be filtered out, for the IM\(_3\) distortion we keep the same requirements as for the LNA. This part will be discussed in Chapter 0.

1.4.5. Filter
The used filter should be a 10.7 MHz filter. A crystal filter is proposed, since it provides a very precisely defined center frequency and very steep band-pass characteristics, that is a very high Q-factor: far higher than can be obtained with conventional lumped circuits.

1.4.6. Local Oscillator
The only requirement for this part is that it should have an output frequency of 40 MHz. This part will be discussed in Chapter 5.

1.4.7. Automatic Gain Control
The working frequency for this part will be 10.7 MHz. The wanted gain can be simply calculated by taking a look at the gain of the LNA and the required gain as explained in 1.2. A gain less than 0 dB gain and more than 80dB should be obtained, because this 80 dB with the minimal 20 dB of the LNA equals the 100 dB required, and the < 0 dB with the 40 dB equals a gain of <40 dB. For the noise holds the same requirement. If we take the lower gain below 0 dB, we can handle much larger input signals, which can be an advantage if the input signals are much larger. As explained in 1.2, the output signal must reach 1.0 V swing. The distortion levels of the AGC should be higher as 30 dB. For the intermodulation distortion this will also be enough, since there is a crystal filter before the AGC, so not much signals close to 10.7 MHz are there and 30 dB will be enough to distinguish these signals. This part will be discussed in Chapter 8.
1.4.8. Overall properties

Properties for each block are:

- Biasing current between 7 µA and 13 µA
- $V_{dd}$ range of 3.0 V till 3.6 V
- Temperature variations of -40 °C till 125 °C
- The noise added by each block should not exceed -120 dB, with a bandwidth of 50 kHz; this is in the same order as the Galactic noise. The entire design will be constructed such that it can handle this noise, thus the noise added by the system should not exceed the noise level of the galactic noise.
- The entire design will be made in AMS 0.35 µm technology
- Minimal size of 0.7 µm for transistors, since there will be designed for an environment with large temperature variations. This is given by the AMS technology
- Matching parameters should be taken for $3\sigma$, in that case 99.7 % of the produced chips will operate as they should
- Rpolyh should be used for resistors, since it has the highest sheet resistance and the least parameter spread
- For the same reason Cpoly will be used for the capacitors
- For each block all the process variations are tested, this includes:
  - Resistor variations
  - Cmos variations
  - Capacitor variations
  - Bipolar variations
  - $V_{dd}$ between 3.0 V and 3.6 V
  - Temperature between -40 °C and 125 °C

The mixers are discussed in Chapter 5. The Voltage Reference in Chapter 9, and the biasing currents in Chapter 10. Also a small look has been taken on the layout design in chapter 0. Also ESD protection has been taken into account; this is discussed in chapter 12. At the end a testing circuitry has been added and a test program has been proposed in chapter 13. For simulation and lay-outing of the circuits Cadence has been used. ADS has been used to investigate the gain from the antenna to the input of the LNA.
2. Antenna Modeling

An antenna model is required to determine the input of the chip. There are two different configurations: one is the delfi-n3Xt case which cannot be changed and the other is the OLFAR case where the configuration of the antennas still needs to be determined. In 2.1 an overview of the possible antenna configurations for OLFAR will be given. These configurations are simulated and these results are discussed in 2.2. With these results a decision will be made on which configuration to use for OLFAR. The filter network, which is required to suppress the transmitting signal, will be discussed in 2.3. A summary is given in 2.4.

2.1. Antenna Configurations

A turnstile configuration has been used in delfi-n3Xt. The frequency range of interest for receiving signals is 145.8 MHz – 146 MHz. With this information the antenna length can be optimized. The configuration of delfi-n3Xt is shown in figure 6.

For OLFAR several configurations are proposed, which are shown in figure 8. Other configurations are already done in [1], from these simulations the turnstile configuration seemed to give the best results. Seven antenna configurations are proposed:

- Configuration 1: a tripole antenna with the antennas 90° bowed, to have the least possible coupling between the antennas and between the antennas and the body.
- Configuration 2: a tripole antenna with the antennas in such way that there is the most probable distance between the antennas to reduce coupling between these antennas. In this setup there is more coupling between the antennas and the body, but this is expected to be much less of importance.
- Configuration 3: also a tripole antenna, but with a stick. This configuration is more or less only defined for taking a look at the influence of this stick. (because this stick is also added at configuration 2)
- Configuration 4: the turnstile antenna as used on the delfi-c3 satellite. For comparison with the setup in configuration 5.
- Configuration 5: the turnstile antenna with the antennas starting at the center, this model is generated to make a useful comparison between the turnstile and the tripole (number 1).
- Configuration 6: same case as configuration 2, setup to decrease coupling between the antennas.
- Configuration 7: tripole antenna like configuration 1, but in this case the antennas are mounted on the edge of the body, to reduce the coupling between the antennas.

For the body of both the delfi-N3XT and the OLFAR satellites we used the $\lambda/6$ rule in the simulator 4nec2, this means that the body must have a grid density larger as $\lambda/6$ of the used frequency. This must be done so that the body is approaching the real body of the satellites.

![figure 5 - tripole antenna](image)

To send circular polarized waves (this is preferred because of the fact that circular polarized waves are known to have less problems with penetrating through the ionosphere) we have to transmit with at least three sources which are 120 degrees out of phase, as shown in figure 5. The maximum angle between the antennas is 120°. This corner has some influences on the coupling between the antennas, which has some effect on the frequency shift.

![figure 6 - tripole source phases](image)
Chapter: Antenna Modeling

Figure 7 - delfi-n3xt simulation model

Figure 8 - antenna configurations
For simulation the 4nec2\(^1\) antenna simulation software has been used, which uses .pg and .nec files, which are reported in Appendix B.

### 2.2. Simulation results

For both OLFAR and delfi-n3Xt the simulation results are discussed in this chapter. For delfi-n3Xt the used configuration has been modeled in 2.2.1. For OLFAR the results of the proposed configurations are discussed and the best configuration has been chosen.

#### 2.2.1. Delfi-n3Xt antenna modeling

For delfi-n3Xt, the simulation results are given in Figure 9 till Figure 12. The gain is shown in dBi, which is the gain in comparison to the gain of an ideal isotropic antenna. The optimal antenna length is 47.97 cm. It is not exactly \(\frac{\lambda}{4}\) due to coupling between the antennas.

![Figure 9 - Optimized Delfi-N3XT impedance and gain](image)

![Figure 10 - Optimized delfi-N3XT swr](image)

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\(^1\) http://home.ict.nl/~arivoors/
Figure 11 - Optimized delfi-N3XT smith-chart

Figure 12 - Pattern for optimized delfi-n3Xt antennas @ 15MHz
2.2.2. OLFAR antenna modeling

For OLFAR the proposed configurations need to be reviewed to decide which configuration to use. The simulation results are given in Appendix A. A weight table has been used to determine the best possible configuration. The five main parameters of the antennas are:

- **Gain**, which is the gain at low frequencies (0.03 MHz-30 MHz).
- **Mechanism**, the easiness of designing the given configuration and deploying in space.
- **Omni directionality**, how omni-directional the pattern of a given configuration is, compared to each other. We look at the pattern at 15 MHz; this is because of the fact that the pattern is quite similar for each configuration at the transmitted frequency. We take 15 MHz because this is in the middle of the band of interest, so it is good to make a valid comparison between the configurations.
- **Filtering**, since the antennas are used for transmitting at 145.9 MHz with 12 V, we need to filter out these signals. This can be done in several ways, some are easier as others. Like some configurations only need a 3rd order filter and some need a 7th order filter.
- **Gain flatness**, this is preferable since this keeps the design of the total circuit comparable for each frequency.

The mechanism is the most important one, since it must be as simple as possible to deploy the chosen antenna configuration in space (40%). The gain and gain flatness are of equal importance since they both make the design of a receiver circuit easier (20%). Of less importance are the filtering (5%) and the Omni-directionality (15%), since they can be both solved with external components like a better filter.

| table 2 - weight table for OLFAR antennas |
|----------------|----------------|----------------|----------------|----------------|----------------|----------------|----------------|
| **Parameter**  | **weight**     | **Conf 1**     | **Conf 2**     | **Conf 3**     | **Conf 4**     | **Conf 5**     | **Conf 6**     | **Conf 7**     |
| Gain [dB]      | 20%            | 7              | 8              | 7              | 3              | 4              | 8              | 7              |
| Mechanism      | 40%            | 7              | 4              | 3              | 9              | 7              | 2              | 7              |
| Omni-directional| 15%            | 7              | 8              | 7              | 3              | 4              | 8              | 7.5            |
| Filtering      | 5%             | 6              | 6              | 6              | 8              | 8              | 8              | 6              |
| Gain flatness  | 20%            | 8              | 7              | 8              | 3              | 5              | 8              | 8              |
| **Total**      | **7.15**       | **6.10**       | **5.55**       | **5.45**       | **5.40**       | **5.60**       | **7.23**       |

If we take a look table 2 we can see that configuration 7 gives the best results. So we prefer configuration 7.

Some of the points given in table 2 are explained:

Taking a look at the gain at 0.03 MHz-30 MHz, since this is the band of interest, it is shown that configuration 2 and 6 gave the highest gain at low frequencies. The mechanism has been graded such that the deployment structure will not use much space of the cube-sat and that there are as least as possible movements needed to get the antennas in place. As example: taking a look at the configurations with a stick, they give nice results for the gain, but they are hard to realize. The omni-directionality is in most cases quite equal but differs a bit. For the filtering a turnstile scores better, because of the fact that in this case we can use the 180° phase shifted transmitting signals, which could cancel each other out (or at least give a lot of suppression). This is not the case for the tripole antenna.
When we look at configuration 4 we can see a frequency shift of the optimum point. We should expect that the optimum should be at +/- 146 MHz, but the optimum seems to be around 137 MHz. This is a result of coupling between the antennas. In the tripole case we also have coupling, but much less, because the antennas are separated with an angle of 120 degrees, instead of 90 degrees. We can model this by looking at Figure 13; at point b we have to insert Z, which can be complex, as a result of coupling. This complex number can cause the given frequency shift. We can compensate for this by decreasing the antenna length, because in that case we move to higher frequencies because of the fact that the wavelengths are smaller at higher frequencies.

![Figure 13 - antenna model](image)

For this reason the antenna lengths are changed a bit to get the optimum at 145.9 MHz. The final results are shown below. The optimum antenna length is 48 cm.

![Figure 14 - Gain and impedance for optimized OLFAR antennas](image)

2 The simulator is not good enough to make a good simulation at very low frequencies (1 MHz) with this model, due to this fact we see a non-useful result at 1 MHz. This is no problem, because we expect the antenna to behave approximately equal at 1 MHz to the 2 MHz behavior.
Figure 15 - SWR for optimized OLFAR antennas

Figure 16 - Smith-chart for the optimized OLFAR antennas

Figure 17 - Pattern for optimized OLFAR antenna
2.3. Filtering

A filter is required to suppress the transmitting signal of 146 MHz (3 V). The required suppression has been calculated so that it does not overdrive the LNA (Chapter 3). The expected signal strength will be discussed in 2.3.1; in this paragraph also the terrestrial noise will be discussed. In 2.3.2 the phasing network will be discussed, because the phase-shifted transmitting signal will be used to get some suppression of this signal at the input of the LNA. With all this information a filter will be added to be sure that the LNA will not be overdriven, this is done in 2.3.3.

2.3.1. Noise Temperature

The wanted H1 signal is fully covered by the Galactic noise, the approximately expected antenna temperature which is caused by galactic noise is given in Figure 18. By pointing to the galactic center, we would obtain an antenna temperature between $5 \times 10^4$ K and $6 \times 10^5$ K. What this means is explained below. It must be kept in mind that the given antenna temperature is not the physical temperature, this is a part which is misunderstood in many cases.

![Figure 18 - expected antenna temperature in space, determined by Kraus\textsuperscript{3}.](image)

We assume that we have a beam angle of less than a few degrees and 100% beam efficiency.

Figure 19 shows us a model of the receiving antenna network. There are no transmission lines (the wavelength is much larger than the used wire length) so \( l \) is equal to 0.

The effective antenna temperature of this system is given by:

$$T_a = T_A e^{-2\alpha l} + T_{AP} e^{-2\alpha l} + T_0 \left(1 - e^{-2\alpha l}\right)$$

$T_0$ is the physical temperature of the transmission line, $T_A$ is the antenna temperature and $T_{AP}$ is given by:

$$T_{AP} = \left(\frac{1}{e_A} - 1\right) T_P$$

$T_P$ is the physical temperature of the antenna, and $e_A$ is the thermal conductivity of the system. For $T_a$ we know that $l$ equals 0. So the term $e^{-2\alpha l} = 1$, which leaves us with:

$$T_a = T_A + T_{AP}$$

We can estimate $T_A$ using Figure 18. $e_A$ is expected to be large (in the range of 380 for copper), since it is known that electrical good conductors are also good thermal conductors. This tells us that $T_{AP}$ is fully determined by $T_P$. If the antenna is fully in the range of the sun, it will be heaten up, but it is known that $T_A$ is about $10^5$ K, so even when the sun heats the antenna up to 300 K, this will not have a significant effect on the received power.

This power can thus be given by, assuming no losses between the antennas and the receiver:

$$P_N = kT_a \Delta_f$$

With these formulas the following can be obtained: there cannot be done much about $T_P$, which is the physical temperature of the antenna, the only thing what can be done is mounting the antennas on the side which is not directed to the sun. We can also make the decision to only measure when on the shadow side if this does seems to have a significant effect on the performance of the system.

2.3.1.1. Estimated galactic noise

Taking the antenna gain in mind and using the formulas of the previous chapter the following estimations on the input are made:

$$U = \sqrt{(P_N \ast R)}$$
Since $P_N$ is dependent on $T_a$ and $\Delta f$ we have to set these. $T_a$ is determined by using Figure 18; we can see that this is between approximately 50,000 K and 600,000 K, depending on the frequency. For the bandwidth 50 kHz has been used, since it is determined by J. BASART [2] that this bandwidth is the best trade-off between the sensitivity and the level of interference. Table 3 gives the expected input signal in $\mu$V at the input of the antennas.

<table>
<thead>
<tr>
<th>$\Delta f$ @ 50 kHz</th>
<th>$T=50000$ K</th>
<th>$T=600000$ K</th>
</tr>
</thead>
<tbody>
<tr>
<td>Input signal (uV)</td>
<td><img src="image1.png" alt="Graph 1" /></td>
<td><img src="image2.png" alt="Graph 2" /></td>
</tr>
<tr>
<td>Input signal (uV)</td>
<td><img src="image3.png" alt="Graph 3" /></td>
<td><img src="image4.png" alt="Graph 4" /></td>
</tr>
</tbody>
</table>

Table 3 - Estimated input signal, frequencies are in MHz

### 2.3.1.2. Estimated terrestrial noise

A problem is the following: delf-n3Xt is going to fly in an orbit around earth. Due to this fact we have to consider noise from earth, since this seems to have a considerable impact on the performance of the low frequency sensing.

The part below is quoted from [3] written by W. C. Erickson.

“...In the 1 to 10 MHz range ionospheric effects make high-angular resolution (=arc-minute) observations from the Earth’s surface virtually impossible and it is necessary to go to space. At satellite altitudes near the Earth, terrestrial sources generate noise levels millions of times above the level of interference harmful to observations with a low-frequency space array. This interference is both narrow band and broad band noise. It is essentially impossible to filter or excise interference to such levels. Near solar minimum, sensitive observations up to a few MHz may be possible from Earth orbit on the sunlit side of the Earth where the ionosphere should provide sufficient shielding from terrestrial interference. Near solar maximum it may be possible to work up to 10 MHz from the sunlit side, at least during selected periods. In the 10 to 30 MHz range sensitive observations from space near the Earth are probably impossible because ionospheric shielding will be ineffective. In this case, Earth-based observations utilizing terrain...
shielding are far more practical. The problems associated with ionospheric refraction in Earth-based observations can be attacked with modern self-calibration techniques that have proven to be highly effective at higher frequencies. This approach is far more feasible than an attempt to cope with the interference levels at satellite altitudes. The interference levels at the near side of the Moon will be about a thousand times lower than those at typical satellite altitudes. This reduction in levels may make relatively sensitive observations possible if effective interference rejection techniques are developed. The far side of the Moon appears to be the only location near the Earth that is sufficiently shielded from terrestrial interference to permit observations without interference rejection systems. In the distant future, when the severe communication and logistical problems associated with the lunar far side are solved, it is the most promising site for low-frequency radio astronomy.”

From this we can conclude that we have to take a careful look at when and what we want to measure, but flying with delfi-n3Xt will just be a proof of concept. What we do know is that the frequency bands: 13.36-13.41 MHz and 25.55-25.67 MHz are protected because of this fact. The OLFAR satellite will fly in an orbit around the moon. For that reason we will design a receiver that can receive up to 30 MHz. In that case we can also measure the terrestrial noise ourselves.

2.3.2. Phasing network

For both delfi-n3Xt and OLFAR the same idea has been used. To send a polarized wave, the transmitted signal has to be phase shifted. For delfi-n3Xt these signals are shifted with steps of 90 degrees. For OLFAR the transmitted signals will be phase shifted with steps of 120°. This concept is shown in Figure 20. This gives the phasing circuit of delfi-n3Xt. For OLFAR such a phasing circuit still has to be designed. The input signal will be around 12 V. This is divided over the 4 antennas, thus 3 V each. The reason that we keep on calculating with 12 V is because of the fact in the case if something goes wrong in the phasing circuit. In that case we do not want the OLFAR chip to fail.

2.3.3. Filter Solutions

By using the 180° phase shifted an ideal suppression can be obtained, but this is not realistic due to some parameter spread of the 180° couplers. To prevent the situation where the transmitted signal does reach the LNA a filter has been added. For both delfi-n3Xt and OLFAR such filters are discussed in 2.3.3.1 and 2.3.3.2.
2.3.3.1. Filter solution for delfi-n3Xt

Figure 21 shows a schematic overview of the entire receiving and transmitting network of delfi-n3Xt. There are two sources. This is due to the fact that if one fails, that there is a back-up, so one of both is transmitting at the same moment. The first 90 degrees phasing part is done by a coax network, after there are two SBTCJ’s. These SBTCJ’s are off-the-shelf 180 degrees phase shifters. There is only one shown, because only one of them will be used. The antennas are mounted after this phase shifter. After this the filters are added. This are 2nd order filters, because they will give about 30 dB suppression, which will be enough, and we want to use as less as possible components in this stage to have a minimal influence on the OLFAR signal. A low-pass filter has been used because keeping in mind component spread; we see that a band-stop filter seems to be much more dependent on this component spread. (Which will be there, the temperature can fluctuate quite much)

Figure 21 - schematic overview of the OLFAR receiving circuit

Figure 22 is the ADS model of the same circuit. This model has been used to determine the expected suppression at the output of this circuit. There can be some parameter spread of the SBTCJ and of the filter; these will influence the amount of suppression. These parameters are:

- SBTCJ phase error: max +/- 7 degrees (from datasheet)
- SBTCJ amplitude error: max +/- 0.4 Volt (from datasheet)
- Parameter spread in the filters L and C (5%)
Some simulations are done on this circuit to determine the suppression, since as stated before we have to deal with some parameter spread. The results are shown in Figure 23 till Figure 26. The numbers at the top of each figure is the worst case scenario.

Figure 22 - Schematic for simulations in ADS, without 90 degrees, because this has no influence. (L=.259uH, C=113pF)

Figure 23 - suppression for 173-180 degrees phase shifting
Figure 24 - suppression for amplitude shifting of 11.6 to 12.4.

Figure 25 - dependence on $L$ of filter max 5% up and down, thus $L=0.48\times L_{dep}$. The ideal case $L_{dep}=1$, is around $-137$ dB.

Figure 26 - dependence on $C$ of filter max 5% up and down. Thus $72.68\times C_{dep}$. The ideal case $C_{dep}=1$ is around $-137$ dB.

A suppression of approximately $-100$ dB is obtained; this will be more than enough to prevent overdriving of the LNA.
2.3.3.2. Filter solution OLFAR
For OLFAR the same principle as for delfi-n3Xt will be used. If all the three 120 degrees phase shifted signals are added we can obtain almost the same suppression as we can for the 180 degrees phase shifted signals. This principle is shown in Figure 27.

![Figure 27 - vectors of 120 degrees phase shifted signals](image)

From this figure it is clear that by adding these vectors that we end in the center, which is in theory 0.00 V. In reality some spread in parameters will be there, so that they will not be shifted exactly 120 degrees, which will result in a not optimal suppression. The filters which will be used are the same as used for the Delfi-N3XT design.

2.4. Summary
A tripole configuration will be used for the OLFAR satellite. For delfi-n3Xt the antennas are fully characterized, with this information the LNA can be designed. The antenna length of the antennas for delfi-n3Xt are 47.97 cm and for OLFAR 48 cm. For both cases the same type of filter will be used, a 2nd order low-pass filter with C equals 72.68 pF and L equals 0.48 µH. The expected Galactic noise is in the range of several micro-volts. It is also discussed that OLFAR needs to fly around the moon to prevent receiving terrestrial noise, for this reason we can state the mission of delfi-n3Xt to be a proof-of-concept.
3. LNA Design

A low-noise amplifier is required to add as less as possible noise in the first stage. This amplifier will be optimized for noise. This LNA should be capable to be used for both OLFAR and delfi-n3 Xt. A structural design method will be used to design the LNA. The basic properties of amplifiers will be discussed in 3.1. The feedback network which is required to get the required gain will be discussed in 3.2. When those two are known, a look at the noise performance will be taken in 3.3. This noise performance is mostly set by the input stage of the LNA. The second stage which is required to get enough gain will be discussed in 3.4. In 3.5 the stability of the LNA will be determined and improved. Combining all this information will give a complete LNA, which properties will be shown in 3.6. Conclusions are made in 3.7. The requirements which should be met by the LNA are shown in Table 4.

<table>
<thead>
<tr>
<th>Table 4 - LNA requirements</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
</tr>
</thead>
<tbody>
<tr>
<td>Frequency Range</td>
<td>30 kHz</td>
<td>30 MHz</td>
<td></td>
</tr>
<tr>
<td>Temperature Range</td>
<td>-40 °C</td>
<td>27 °C</td>
<td>125 °C</td>
</tr>
<tr>
<td>Gain</td>
<td>20 dB</td>
<td>28 dB</td>
<td>40 dB</td>
</tr>
<tr>
<td>Noise @50kHz BW</td>
<td>&lt; -120 dB</td>
<td></td>
<td></td>
</tr>
<tr>
<td>HD and IM3 @50kHz</td>
<td>40 dB</td>
<td></td>
<td></td>
</tr>
<tr>
<td>I_ref range</td>
<td>7 μA</td>
<td>13 μA</td>
<td></td>
</tr>
<tr>
<td>V_dd range</td>
<td>3.0 V</td>
<td>3.3 V</td>
<td>3.6 V</td>
</tr>
</tbody>
</table>

3.1. Amplifier Basics

For the design of a Low-Noise Amplifier a structural design method has been followed as explained in [4]. The design of an amplifier contains two stages, first the design of the feedback network and second the design of the nullor. The nullor is an ideal amplifying stage, and the feedback is used to set the amplifier with a certain gain. The feedback only determines the gain in the case if the loop-gain (L=Aβ) is high enough, because the gain can be expressed by:

\[ A_t = A_{t\infty} \frac{-L}{1 - L} \], thus if L = \infty the transfer of the amplifier is

\[ A_t = A_{t\infty} \frac{-1}{\beta} \]

in which \( \beta \) is the negative feedback. For this reason a nullor has to be designed such that it gives enough gain, so that it approximates \( L = \infty \).
3.2. Feedback Network

The feedback for the LNA which has been chosen is shown below. The reason for this type of feedback is because it is capable of added several input voltages, and a third input can be easily added.

![Configuration for summing voltages](image)

Figure 29 - configuration for summing voltages

The output voltage is given by:

$$-V_{out} = \frac{R_3}{R_1} \cdot V_{input1} + \frac{R_3}{R_2} \cdot V_{input2}$$

$R_1$ and $R_2$ should be equal to make a symmetrical summation; this is required to suppress the transmitting signal as much as possible. The values of $R_1$, $R_2$ and $R_3$ will be determined in the next paragraph, since they are influencing the noise behavior of the LNA. As shown by Table 4 a gain of 28 dB is required. From this it is known that:

$$R_1 = R_2 = \frac{R_3}{25}$$

This has one major disadvantage, since a high resistive load is required, due to the antenna; the feedback resistor has a large parasitic capacitance. This capacitance causes some problems in the gain of the amplifier. For this reason the LNA is chosen to be divided in two parts with both a gain of 14 dB.
3.3. Input stage LNA
The input stage of an amplifier is known to be the most important concerning noise properties, because this is the place where the signal is the smallest. Thus this noise has been optimized for noise. A mosfet has been used since its noise behavior is much better compared to a bipolar transistor. The theoretical noise performance of the LNA will be discussed in paragraph 3.3.1. This noise will be compared to the real noise as simulated by cadence in paragraph 3.3.2.

3.3.1. Theoretical approach of the noise
The theoretical input noise of the LNA can be calculated by using equivalent noise models for all the used objects, and using shifting techniques to transform them to an equivalent input noise. These calculations are done in Appendix I. From these calculations the following values can be obtained:

- $W = 10 \mu m$
- $L = 3 \mu m$
- $I_d = 100 \mu A$

The only thing left is to determine $R_4$, since $R_4$ also has some influence on the signal which will be received from the antennas.

Figure 31 – transfer of the input signal to the amplifier

Figure 31 is the transfer of the signal from the antenna to the LNA. The antennas seemed to be high ohmic for low frequencies, which require a high ohmic input impedance of the LNA. Figure 32 is a zoomed version of Figure 31, at low frequencies.

Figure 32 – transfer for low frequencies
The information from Figure 32 can also be found in Table 5. It can be found that from about 40 kΩ there is not much improvement anymore, and the losses which are dealt with here, will be compromised by the AGC. The figure below shows the noise depending on the resistance value.

![Graph showing noise as a function of R4](image)

Figure 33 – noise [V²/Hz] as a function of R4

Figure 33 shows the input noise as a function of R₄. What we see is that R₄ has a significant influence on the total noise. This is not strange, because of the fact that the equivalent noise voltage of R₄ is directly on the input. R₄ has been taken equal to 20 kΩ. Which means that R₁ = R₂ = 40 kΩ.

Since the gain is given by $\frac{R₂}{R₁} and \frac{R₃}{R₂}$, also the influence of R₃ on the noise should be taken into account.
Figure 34 shows the noise as a function of R3 and R4. What we see is that there is no significant influence on the noise by R3. Thus R3 can be chosen freely to set the gain of the amplifier.

R3 will be $5 \times 40 \, \text{k}\Omega = 200 \, \text{k}\Omega$.

3.3.2. Practical noise LNA

Figure 35 shows the input noise of the LNA as simulated in cadence. It is shown that the input noise of the LNA suffers more noise than calculated in the previous paragraph. This is due to the fact that the previous paragraph only concerned of one amplifier, but two are used. It should not make sense to do the calculation with both the amplifier, since the outcome will be the same, because an optimum had been found.

3.4. Second stage LNA

The second stage should provide enough gain to obtain a loop-gain high enough. For this a look has to be taken onto the loop-gain. Two stages should be enough to get enough loop-gain. This has the advantage that no third stage is required, which has the advantage that the stabilization will be much easier. Negative feedback is required to provide the given gain, thus a differential pair has been used for the second stage. The loop gain can be calculated by the following:
Loop gain:
The source will be simplified, because of the fact that it is expected to have no important poles. For this the source is just modeled as a resistor of 50 Ω. In that case the amplifier can be reduced to the following:

\[ L(0) = -g_{m1}r_{ds1}g_{m2} \frac{r_{ds2}}{R_3 + R_4 + r_{ds2}} \cdot R_4 \]

Adding for both stages the gate-source capacitors the following loop gain can be found:

\[ L(s) = \frac{r_{ds1} g_{m2}}{1 + s r_{ds1} C_{gs2}} \frac{r_{ds2}}{R_4 (1 + s r_{ds2} C_1) + R_3 (1 + s r_{ds2} C_1)(1 + s R_4 C_{gs1}) + r_{ds2} (1 + s R_4 C_{gs1}) R_4} \]

The poles of this transfer seemed to be very hard to determine by hand. These poles and the stabilization will be discussed in the next paragraph. The second stage has been chosen to be 50 µm/0.7 µm, with a biasing current of 200 µA.

3.5. Poles
For the pole simulations LINDA has been used, these simulations and stabilization are done in Appendix H. The figure below shows the root-locus of the LNA after stabilization using phantom zeros and pole splitting techniques. Figure 38 show the poles as simulated by cadence.

---

4 The poles are calculated using the equation:

\[ \rho_s = -1.25 \times 10^{-11} \left( 1001 \nu_{gs1} C_1 + 4 \times 10^4 \nu_{gs1} C_1 + \nu_{gs1} C_{gs1} - (1.02 \times 10^3 \nu_{gs1} C_1^2 - 8.098 \times 10^4 \nu_{gs1} C_{gs1}^2 - 3.99 \times 10^3 \nu_{gs1} C_{gs1}^2 + 1.6 \times 10^4 \nu_{gs1} C_{gs1}^2 + 8 \times 10^4 \nu_{gs1} C_{gs1}^2)^2 + \right) \]

5 Software written by TU-Delft and Catena, Linear Dynamic Circuit analyzer, manager: Th. Hamoen, 1999
3.6. Entire LNA
Some important properties for this amplifier are:

- Distortion
- Biasing
- Influence of the load capacitance

These will be discussed in 3.6.1. Another important aspect: the suppression of the transmitted signal, this will be discussed in 3.6.2.

3.6.1. Properties of the LNA

3.6.1.1. Distortion
Harmonic distortion is a result of the non-ideality of the LNA, which is shown in the next equation:

\[ \frac{V_{\text{out}}}{V_{\text{in}}} = -\frac{1}{\beta} \frac{1}{1 + \frac{1}{A_\beta}} \]

If \( A_\beta = \infty \) than a gain is equal to \( \frac{1}{\beta} \) can be found, but since this is not the case, some non-idealities can be found. Thus to improve distortion levels the loop-gain could be increased. With this knowledge, a look at the inter-modulation and harmonic distortion has been taken. The reason that these specifications matter for OLFAR are the following: it is unwanted to get a signal at a certain frequency to be visible at other frequencies, because in that case a ‘double’ star can be obtained. The results are shown below.

![Figure 39 - Harmonic distortion of a 2 MHz signal](image)
The harmonic of a 2 MHz signal is below the noise floor, and thus it is good enough. The inter-modulation is shown in figure 40. The IM₃ is very low and thus will not be seen at different frequencies, thus no more loop-gain is required for reducing the distortion levels.

3.6.1.2. Influence of C_L
Figure 41 shows the root-locus for a changing load capacitor; from this it can be found that the load capacitor should not exceed 1 pF.

3.6.1.3. Differential pair biasing
The second input of the differential pair still has to be biased. For this a bias currents of 10 µA through a 100 kΩ resistor had been taken, causing a bias voltage of 1.0 V. Even at the worst process corner, this will be enough to have all the transistors saturated. Taking the V_{gs} of the mirror close to V_{th}, V_{ds,sat} would be low and thus the voltage drop, with a 1.0 V bias voltage,
across this mirror will be enough. A decoupling capacitor between the input of the LNA and the phasing circuit should be added. This capacitor should be taken at least 0.5 µF to obtain not much loss at low frequencies.

3.6.1.4. Gain LNA
The figures below show the gain of the entire LNA, they are shown with and without parasitic capacitances. A ‘bubble’ around 30 MHz can be found, caused by these capacitances. This is not a real problem, since the LNA keeps between its requirements.

![Gain LNA, without and with parasitic capacitance](image)

3.6.2. 146MHz signal suppression
The suppression of the transmitted signal which has been obtained by this configuration is shown in figure 43. A suppression of about -100 dB can be found, which will be enough.

![Suppression of 146MHz signal at the output of the LNA](image)
3.7. Conclusion

By approaching the amplifier on the structural way an amplifier with a dc-gain of 28 dB has been constructed. This amplifier and the filters will suppress the 146 MHz signal with about 100 dB. The LNA has been implemented by a two stage amplifier and a resistive feedback network. The following characteristics are obtained:

<table>
<thead>
<tr>
<th>Characteristic</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
</tr>
</thead>
<tbody>
<tr>
<td>Total Power</td>
<td>1.245 mW</td>
<td>1.75 mW</td>
<td>2.37 mW</td>
</tr>
<tr>
<td>Output Impedance</td>
<td>8.43 kΩ</td>
<td>9.19 kΩ</td>
<td>10.1 kΩ</td>
</tr>
<tr>
<td>Distortion HD IM3</td>
<td>63 dB</td>
<td>71.3 dB</td>
<td>84 dB</td>
</tr>
<tr>
<td>Max Load</td>
<td></td>
<td>1 pF</td>
<td></td>
</tr>
<tr>
<td>Noise @ BW 50kHz</td>
<td>-145.9 dB</td>
<td>-151.9 dB</td>
<td>-160.95 dB</td>
</tr>
<tr>
<td>Gain @ 30 MHz</td>
<td>22.55 dB</td>
<td>28 dB</td>
<td>34.38 dB</td>
</tr>
</tbody>
</table>
4. Buffer

A buffer is required to get low output impedance, which is required to drive the mixer and the differential to single ended converter. The requirements for this buffer are discussed in 4.1. The gain and the stability are reviewed in 4.2, and at the end a summary will be given in 4.3.

<table>
<thead>
<tr>
<th>Requirement</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
</tr>
</thead>
<tbody>
<tr>
<td>Max input capacitance</td>
<td></td>
<td>1 pF</td>
<td></td>
</tr>
<tr>
<td>Wanted Gain</td>
<td>0 dB</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Wanted output Impedance</td>
<td>2 kΩ</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Max distortion</td>
<td>40 dB</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Frequency range</td>
<td>30 kHz</td>
<td>30 MHz</td>
<td></td>
</tr>
<tr>
<td>Max noise (@ BW=50kHz)</td>
<td>-120 dB</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Driving voltage range</td>
<td>3.0 V</td>
<td>3.3 V</td>
<td>3.6 V</td>
</tr>
<tr>
<td>Current reference range</td>
<td>7 µA</td>
<td>13 µA</td>
<td></td>
</tr>
</tbody>
</table>

There will not be any loss of loop-gain, thus a single stage amplifier will be enough, concerning the gain. The noise produced by the buffer should not be more than produced by the LNA. The input capacitance should not exceed its maximum value of 1 pF, but they are taken such that they do form low output impedance. The biasing current has been chosen such that there is enough gain so that low output impedance is observed.
The mirror dimensions are chosen such that the output impedance is low enough and they do not use too much space. Matching is not of interest now, since the input offset will not cause a significant problem.

4.2. Gain and Stability

As the figures below show, enough loop gain is obtained. This results in a well behavior of the closed loop gain as shown in Figure 47.

A zero can be found at 500 MHz, causing the gain to be not completely equal to 0 dB. This zero is caused by the upper mirror of the amplifier. The plots below show us the stability of the amplifier at all process corners. A stable buffer is obtained, even with a large load capacitance the buffer seems to be stable. The only disadvantage of a large load is its added pole, which influences the gain.
4.3. Output Characteristics

Table 9 gives a summary of the output characteristics of this buffer; also the noise, PSRR and the distortion are shown in the figures below.
Table 9 - output characteristics Buffer

<table>
<thead>
<tr>
<th></th>
<th>min</th>
<th>typ</th>
<th>Max</th>
</tr>
</thead>
<tbody>
<tr>
<td>Distortion IM3 @30kHz HD</td>
<td>106 dB</td>
<td>113 dB</td>
<td>121 dB</td>
</tr>
<tr>
<td></td>
<td>51.7 dB</td>
<td>54.4 dB</td>
<td>77.2 dB</td>
</tr>
<tr>
<td>Open loop gain</td>
<td>29.86 dB @ 30kHz</td>
<td>33.03 dB @ 30kHz</td>
<td>36.6 dB @ 30kHz</td>
</tr>
<tr>
<td></td>
<td>29.36 dB @ 30MHz</td>
<td>32.06 dB @ 30MHz</td>
<td>34.59 dB @ 30MHz</td>
</tr>
<tr>
<td>Closed loop gain</td>
<td>-104 mDB @ 30kHz</td>
<td>-157 mDB @ 30kHz</td>
<td>-251 mDB @ 30kHz</td>
</tr>
<tr>
<td></td>
<td>-87.81 mDB @ 30MHz</td>
<td>-154 mDB @ 30MHz</td>
<td>-270 mDB @ 30MHz</td>
</tr>
<tr>
<td>Noise @ BW 50kHz</td>
<td>-184.3 dB</td>
<td>-207.8 dB</td>
<td>-214.2 dB</td>
</tr>
<tr>
<td>Output resistance</td>
<td>643 Ω</td>
<td>815 Ω</td>
<td>992 Ω</td>
</tr>
<tr>
<td>Input impedance</td>
<td>47.7 fF</td>
<td>52.65 fF</td>
<td>57.67 fF</td>
</tr>
<tr>
<td>Power</td>
<td>2.11 mW</td>
<td>3.3 mW</td>
<td>4.63 mW</td>
</tr>
<tr>
<td>Max load</td>
<td>1 pF</td>
<td></td>
<td></td>
</tr>
<tr>
<td>PSRR @ 50MHz</td>
<td>-30.5 dB</td>
<td>-34.27 dB</td>
<td>-37.06 dB</td>
</tr>
</tbody>
</table>
5. Mixer and LO Design

A Mixer is required to make the frequency steps. Two mixers are required as shown by figure 53. One is used for the UP-conversion to 50.7 MHz, the other has been used for down-conversion to 10.7 MHz. To make these conversions a mixer has been designed and discussed in 5.1. Also a Local oscillator of 40 MHz is required; this will be discussed in 5.2.

5.1. Mixer Design

A brief review of the used mixer is given in this chapter. The basics of a mixer are discussed in 5.1.1, with this knowledge the mixer has been designed and discussed in 5.1.2.

5.1.1. Mixer Properties

The purpose of a mixer is to convert a base band or intermediate frequency to the higher RF frequency (up-conversion mixer) or to translate an RF frequency to a lower frequency base band or intermediate frequency (down-conversion mixer) by multiplying the input signal two signal with a Local Oscillator signal taken from the PLL. When signals with two different frequencies are multiplied; the output frequencies consist of an additive term plus the subtractive term (Figure 54).

\[ V_{out}(t) = \cos \omega_1 t \times \cos \omega_2 t = \frac{1}{2}(\cos(\omega_1 - \omega_2)t + \cos(\omega_1 + \omega_2)t) \]

If the additive term is used as output, it is called an up-conversion mixer. On the other hand, if the subtractive term is used as the output, it is called a down-conversion mixer. This mixer will be used...
for both cases. The first mixer will be used to convert the input frequencies up to 50.7 MHz; here it is very important that the RF signal is suppressed very well, since this signal should not be seen at the output of the OLFAR, to prevent incorrect information. For the second mixer it is less important, this one is used to convert the 50.7 MHz signal down to 10.7 MHz, after this mixer a crystal filter has been added to filter out all the other signals. This is also explained in chapter 1. Thus to suppress the RF signal, we will need to combine the mixer output signals, otherwise it is not a full multiplication with a square wave. This principle is shown in the figures below.

Figure 55 - Output without and with differential to single ended conversion

The LO frequency is 5 MHz and the RF frequency is 1 MHz. The first figure shows the case with combining the outputs. There is almost no RF signal on the output. The second figure shows a single output, where the RF signal can be seen around -25dB. For this reason a differential to single ended conversion is required. This amplifier will be discussed in Chapter 0. Also a lot of other ‘peaks’ can be seen, these are results of a non-ideal dft conversion, which is also over a small time interval. The only reason for these figures is to show the difference at the RF frequency.

5.1.1.1. Capacitive Coupling
Capacitive coupling is not a problem for this application of the mixer, since both the PLL and LO frequencies are not near the signal of interest.

5.1.1.2. Conversion gain
One of the main specifications of a mixer is conversion gain. The two basic types are conversion voltage gain and conversion power gain. Conversion voltage gain is the gain from the RF input voltage to IF output voltage. So if the mixer consists of perfect switches, the conversion voltage gain of the mixer equals:

\[
V_{rf} = A \cos \omega_{rf} t, V_{lo} = \frac{4}{\pi} \left[ \cos \omega_{lo} t + \frac{1}{3} \cos 3\omega_{lo} t + \frac{1}{5} \cos 5\omega_{lo} t \right]
\]

\[
V_{rf} * V_{lo} = \frac{2A}{\pi} \cos (\omega_{lo} - \omega_{RF}) + \frac{2A}{3\pi} \cos (3\omega_{lo} + \omega_{RF}) + \frac{2A}{5\pi} \cos (5\omega_{lo} - \omega_{RF}) + \ldots
\]

\[
V_{if} = \frac{2A}{\pi} \cos \omega_{if} t
\]
5.1.2. Mixer final

The load of this mixer will be an AGC or an amplifier. The resistance should be as low as possible, but the input capacitance should not be too high, otherwise the PLL will not be able to drive the mixer at the wanted frequency.

The mixer consists of two of these simple switching stages, and a switch between the output of the voltage mixer and a dc point has been added, so that we indeed have a mixer and not a sample and hold stage. This switch has to be driven with the opposite LO signal. This switch has to deal with some non-idealities. The two most important ones are: charge-injection and capacitive coupling. Some charge-injection can be expected, but this is not a problem, since the output of the mixer is always defined; ‘grounded’ or following the RF signal. Thus the signal will only face problems of capacitive coupling during the switching time. By making the switches as fast as possible, this problem will be reduced. The LO frequency for both mixers is also far outside the region of interest and thus can be filtered out. The width of these ‘grounding’ switches should have the same value as that of the mixing switches, since when we make them larger we are facing more charge-injection, and it does not make our system faster, so that is useless.

5.1.2.1. DC point

A DC-point is required otherwise the output signal has to switch between ground and the RF signal. A biasing current through a resistor is used to get this DC-point. A capacitor has been added to keep this voltage at the wanted 1.5 V (half of $V_{dd}$). It is known that the lowest frequency is about 30 kHz, a filter below this frequency should be used. Taking 5 kHz:

$$freq = \frac{1}{2 \pi \times RC}$$

By taking a biasing current and converting this to a voltage we need a resistor of 158 kΩ. With this value it can be found that a $C = 172 \text{ pF}$ is required.

<table>
<thead>
<tr>
<th>Table 10 - Mixer Characteristics</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Gate capacitance</strong></td>
</tr>
<tr>
<td>22.95 fF</td>
</tr>
<tr>
<td><strong>Power</strong></td>
</tr>
<tr>
<td><strong>On resistance</strong></td>
</tr>
<tr>
<td><strong>Gain</strong></td>
</tr>
</tbody>
</table>
5.2. LO Design

One of the mixers will be driven by the PLL of Chapter 6. For the other mixer we need a LO of 40 MHz, and also for the PLL we will need a 25 kHz clk (6.1). A Crystal Oscillator will be used, since they are known to have a very stable frequency. The figure below shows the proposed Crystal Oscillator circuit diagram. This type of setup gives a parallel resonant mode of the crystal. The internal inverter acts as a class AB amplifier and provides approximately 180° phase shift from input to output and the π network formed by the crystal, $R_1$, $C_1$ and $C_2$ provides additional 180° phase shift.

So the total phase shift is 360° around the loop. This is one of the conditions, which is required to sustain oscillation. The other condition, for proper startup and sustaining oscillation is the closed loop gain should be $\geq 1$. $C_1$ and $C_2$ form together the load capacitance of the crystal, also the stray capacitance of the printed circuit board needs to be taken into account. By combining all these values we obtain a load capacitance of:

$$C_l = \frac{C_1 \cdot C_2}{C_1 + C_2} + C_s$$

Usually $C_1$ and $C_2$ are chosen to be quite equal. Large values of $C_1$ and/or $C_2$ increases frequency stability but decreases loop gain and may cause start-up problems. The resistors should be chosen such that:

$R_1$ us the drive limiting resistor, its function is to limit the output of the inverter so that the crystal is not over driven. $R_1$ and $C_1$ form a voltage dividing circuit, the values of these components are chosen in such way that the output of the inverter goes close to rail-to-rail and the input of the crystal is 60% rail-to-rail, usually resistance $R_1$ and reactance $C_1$ are chosen equal at the operating frequency, $R_1 \approx XC_1$. In this way the input of the crystal is half that of the inverter output.

$R_f$ is there to provide negative feedback, this value is high, in the range of 500 kΩ -> 2 MΩ.
A Phase-Locked-Loop is required to have an adjustable output frequency, to switch between several frequencies. The required frequency range is given by:

**Frequency Range**  20MHz till 50.67MHz

This frequency should be stable over all the time. The schematic of a PLL is shown below. Since we want to set the frequency, a frequency divider has been added with an adjustable division (6.1). The output of this divider will be compared to a well-known frequency, by the phase-frequency detector (6.2). With this signal a charge-pump(6.3) can be driven, this charge pump increases or decreases (6.4) the control voltage of the Voltage Controlled Oscillator (6.5). A loop-filter (6.6) has been added to stabilize the PLL-loop. The entire PLL will be reviewed in paragraph 6.7.
6.1. Frequency Divider

A frequency divider is required to compare the output signal of the VCO with a stable input clock signal. This division has to be adjustable, because in that case it is possible to change the output frequency, and thus set the output of OLFAR. The frequency divider consists of a standard frequency division by D-Flip-Flops. Each output is a division by two of the input.

The outputs have to be compared to a value which can be set by the user. For this XOR-ports and inverters are added. Taking all the outputs of the inverted OUT, and combining them in an AND-port, we will see a ‘1’ output when all the values of the counter are equal to the preset division value. This generates a reset pulse, which starts the division all over again. This pulse can also be used for switching a D-Flip-Flop, and thus creating a divided square wave.

This way gives one limitation, and that is that it is forbidden to divide by ‘1111’, thus 0.

6.1.1. Peak protection

To protect the frequency divider from unwanted signals; like a peak out of the comparison circuit, in this case the division can be reset and thus give a wrong division, the reset has been synchronized with the input. So if an a-synchronous pulse has been given, nothing happens.

6.1.2. Jitter

Jitter is a time-varying type of noise, which can at the end lead to a large phase noise, as shown in Figure 62. The solid line is the wanted output, the dotted lines are caused by Jitter, this means that when this happens the signal is faster or slower. Normally this Jitter is Gaussian, it can for example be caused by temperature effects, so in a larger time period the average division will be correct, but there still will be phase noise.
Jitter can occur in every Flip-flop. This means that the Jitter in the total circuit can cause a quite large deviation of the output frequency. The clock also produces some Jitter, but by taking a crystal as clock reference, this is negligible, since the Jitter of a crystal is very low.

The total Jitter in an a-synchronous counter equals:

\[ T_j = T_{j,clk} + \sum_{i=1}^{N} T_{j,i} \]

Where \( N \) is the number of divider units, and \( T_{j,clk} \) is the clock jitter. Looking at the variance of the Jitter we see:

\[ \sigma_j^2(t) = \sigma_{j,clk}^2 + (N \cdot \sigma_{j,div})^2 \]

When looking at a synchronized output of the divider, which looks like the figure below, the following can be obtained:

\[ T_j(t) = T_{j,clk} + T_{j,FF}(t) \]

Which implies:

\[ \sigma_j^2(t) = \sigma_{j,clk}^2 + \sigma_{j,FF}^2(t) \]

From which we can see that it is much lower than that of an a-synchronous counter. For this reason a DFF has been used, which uses IN as the clock signal.
6.1.3. Division Ratio

This output synchronization has an influence on the division ratio, because a pulse should be given before the pulse is shown on the output. The division without this synchronization block equals SET+2, this 2 comes from the fact that we get 1 from the first counter (which is always a division by 2) and by the reset delay. Multiplying this by 2 we get:

\[ N = 2 \cdot SET + 4 \]

In which is SET the value which can be set by the user.

From this formula it can be seen that a clock of 25 kHz is required, to make steps of 50 kHz. Also the ‘forbidden’ state problem has been solved, since N cannot be equal to 0.

6.2. Phase-Frequency Detector

A phase-frequency detector is a special type of a phase detector. A phase detector has to detect the phase difference of its two inputs. A very simple form of a phase detector is a XOR gate, but due to its symmetric operation, it’s not capable of detecting phase differences greater than 180 degrees. A phase-frequency detector is capable of detecting phase differences larger as 180 degrees. An often used circuit has been shown in the figure below.

Input R is the signal from the frequency divider and V is the reference signal. If V lags behind of R, which means that the VCO frequency is too high, the DN signal would be high. In the other case, when R lags behind of V, UP will be high. With these signals we are able to drive a charge pump, which is able to increase or decrease the VCO voltage, to influence its output frequency. This circuit
has a problem, which is that it has four states. The situation where UP and DN are high should be prevented, because in that case we will short the Charge pump. To prevent this, the circuit in the middle has been added. When both get high, both the flip-flops will get a reset. By eliminating this stage we are left with the following states.

<table>
<thead>
<tr>
<th>State</th>
<th>Output</th>
<th>Reason</th>
</tr>
</thead>
<tbody>
<tr>
<td>-1</td>
<td>DN=1, UP=0</td>
<td>VCO frequency too high</td>
</tr>
<tr>
<td>0</td>
<td>DN=0, UP=0</td>
<td>In phase lock</td>
</tr>
<tr>
<td>1</td>
<td>DN=0, UP=1</td>
<td>VCO frequency too low</td>
</tr>
</tbody>
</table>

The operation of the PFD is now 360 degrees. One another important issue is the phase resolution that the PFD is able to detect. If the phase detector is able to detect only phase differences larger as 100 ps, then the gain drops dramatically below these differences. In this region the PFD becomes useless; this is called the dead-zone band. In this region the PFD no longer behaves as a linear system and the noise performance of the PLL will be degraded. The PFD will be phase locked in that case, since it does not measure a phase difference. A well-known method to prevent this problem is by using a type-4 PFD. In this PFD a delay has been added in the feedback path. When the PLL is in lock, the PFD will always send two short UP and DN pulses simultaneously at every positive edge of R and V. When a small differential phase can be seen on R and V, the fall times of the two pulses may be less than one gate delay. By using this technique a smaller timing resolution can be achieved. The working of this PFD is shown in the figures below, net3 is the output DN.

![Figure 66 - output PFD, with 100ns lagging V](image)

In this case R is lagging 100 ns on V, and thus the pulse width equals 100 ns, as shown below.

![Figure 67 - zoomed in](image)
6.3. Charge Pump
A charge pump is a simple device. Its only function is translating the UP and DN pulses of the PFD to a current. This current will be used to increase or decrease the voltage across a capacitor, which is used to drive the VCO. This capacitor can be found in the Loop Filter. So the only goal of the charge pump is to switch between current pulling and pushing. This can be simply done by two switches, which switch between these two modes. This is implemented by the following:

When the frequency is too high, DN will be high, so S2 will be switched on. In this case voltage across the capacitor decreases and thus the frequency of the VCO will be lowered. The switches are chosen somewhat larger than the standard values, because we wanted to reduce its on-resistance to have the voltage drop as low as possible.

6.4. Gain of Charge Pump and PFD
The gain of these two parts together is important for calculating the loop gain in a later stage. This is required for determining the loop filter component values. An ideal phase-frequency detector compares a reference phase $\theta_r$ to the output phase $\theta_o$ of the closed-loop-PLL VCO. Ideally, the PFD outputs an error voltage proportional to the phase error $\theta_e = \theta_r - \theta_o$, at least for some range of $\theta_e$. If the proportionality constant is given by $K_d$ (volts/rad), then the error voltage is given by $V_e = K_d \theta_e$. The value of $K_d$ can be found from the slope of $V_e$ vs. $\theta_e$.
It is known that with a given phase difference DN or UP will be enabled. When one of these is enabled, the current \( I_p \) will charge the capacitor, and since we know that a capacitor charges linear as a function of the current the curve above is achieved. The slope of this curve is thus equal to \( I_p \).

\[
K_D = I_p
\]

### 6.4.1. Corners

The following figures show the variation of the output current at all process corners. Table 12 is a summary of these figures.

![Figure 70 - UP](image)

![Figure 71 - DN](image)

<table>
<thead>
<tr>
<th>Table 12 Charge-Pump</th>
</tr>
</thead>
<tbody>
<tr>
<td>Min</td>
</tr>
<tr>
<td>Gain</td>
</tr>
</tbody>
</table>

### 6.4.2. Matching

In 6.4.1 the influence of process corners on the output of the charge-pump has been shown. The only thing left is to calculate the additional matching to get the entire output swing. For this circuit we obtain the following results:

<table>
<thead>
<tr>
<th>Table 13 - Charge-Pump output Characteristics</th>
</tr>
</thead>
<tbody>
<tr>
<td>Gain variation</td>
</tr>
<tr>
<td>-29.2 %</td>
</tr>
<tr>
<td>Matching (3(\sigma))</td>
</tr>
<tr>
<td>Current Reference Variation</td>
</tr>
<tr>
<td>Output Variation total</td>
</tr>
</tbody>
</table>
6.5. Voltage Controlled Oscillator

A Voltage Controlled Oscillator is a device which must be capable of translating an input voltage into a output frequency. So the gain is given in [MHz/V]. The requirements which should be met by the VCO are given in Table 14.

<table>
<thead>
<tr>
<th></th>
<th>Min</th>
<th>Max</th>
</tr>
</thead>
<tbody>
<tr>
<td>Input Voltage Range</td>
<td>0.0 V</td>
<td>3.0 V</td>
</tr>
<tr>
<td>Output frequency Range</td>
<td>20 MHz</td>
<td>50.67 MHz</td>
</tr>
</tbody>
</table>

A Voltage Controlled Oscillator can be split up into three parts. The first part is the integrator, which should integrate the input voltage over time; this part is explained in 6.5.3. The second part is the comparator, this part compares the integrated voltage to a static voltage and gives a pulse when they are equal (6.5.2), and in 6.5.1 something will be explained about the memory which reminds in which state we are.

6.5.1. Memory

The used memory can be simply implemented by a Toggle Flip Flop. By generating a pulse on the input pin, the output will change from symbol. So each time when the integrator reaches a value above the dc value, this pulse will be given and a switch will be put ‘on’ to discharge the integrator to set this output again to ‘zero’. The output impedance of INV6 (a standard AMS inverter cell), which has been used to drive larger loads equals 586 Ω, this means that a maximum load of 5 pF for 50.7 MHz.

6.5.2. Comparator

The comparator will compare the signal of the integrator with a preset voltage. This comparator should provide a rail-to-rail output to be sure that its output voltage crosses the operating voltage of the used digital parts. It should be fast enough to follow at least a 50.67 MHz signal, this holds that the pulses are 19.7 ns wide, resulting in a maximum rise and fall time of 4.9 ns. To reach this the transistor sizes has been chosen such that the output is able to reach easily rail-to-rail and that the comparator is saturated at all corners. The error due to mismatch should not cause a large problem, since this is not dominant on the frequency selection. The chosen comparator is shown in the figure below; this setup has been chosen because of its large output swing capability and its differential input. A current of 50 µA will do the job seemed to be enough. All the outputs of the comparator are shown below.

<table>
<thead>
<tr>
<th></th>
<th>Min</th>
<th>Max</th>
</tr>
</thead>
<tbody>
<tr>
<td>Output voltage range</td>
<td>0.5 V</td>
<td>2.5 V</td>
</tr>
<tr>
<td>Frequency Range</td>
<td>20 MHz</td>
<td>50.67 MHz</td>
</tr>
<tr>
<td>Max output delay</td>
<td></td>
<td>4.9 ns</td>
</tr>
</tbody>
</table>
Figure 73 - Comparator

Figure 74 - step up response

Figure 75 - step down response
There is gain at 50.67 MHz and it thus still operates as it should. The characteristics are given in the table below.

<table>
<thead>
<tr>
<th></th>
<th>Min</th>
<th>Typ</th>
<th>max</th>
</tr>
</thead>
<tbody>
<tr>
<td>Max delay</td>
<td>0 ns</td>
<td>3.5 ns</td>
<td></td>
</tr>
<tr>
<td>Output range</td>
<td>0</td>
<td>&gt; 2.5 V</td>
<td></td>
</tr>
<tr>
<td>Load</td>
<td></td>
<td>8 fF</td>
<td></td>
</tr>
</tbody>
</table>

What we see in the table above is that the comparator reaches the upper or down limit within 4.9 ns, which was required to be sure of a correct operation.

6.5.3. Integrator

For the integrator it is important that the charging time is constant, otherwise we can get duty-cycles which differ from 0.5. The input signal is a voltage from the loop filter. This should be converted to a voltage which charges constant over the time, and can be discharged. For this reason a configuration with one current source is preferred, which takes care of the charging of a capacitor. A RC combination has been used to ensure the discharging of the capacitor. For this reason the structure as shown below has been chosen.
The integrator of above has been chosen, because in this case almost the entire input range can be used. If instead a voltage to current amplifier would have been used, a limited input range would have been obtained, due to biasing of the amplifier. The only disadvantage of this integrator is that it suffers more from process corners since also the gate-source voltage of the input varies with this. This shall result in some more deviation in the output frequency. The integration can be obtained by the voltage across the capacitor, caused by the constant current $I$:

$$I = C \frac{dU}{dt}$$

This equals:

$$dt = \frac{dU \times C}{I}$$

dU is given by $V_{ss}$ and the dc value at the other input of the comparator. The switch is chosen to be 50 µm/0.7 µm, in that case its gate capacitance does not cause too much delay, so that the frequency of interest can be obtained, and its on resistance is low so that a fast discharging of the capacitor has been obtained.
6.5.4. Entire VCO

The frequency of the VCO can be expressed by the following:

\[ f = \frac{1}{2 \cdot \left( \frac{dU}{t} \cdot C + \text{delay} \right)} \]

The maximum delay of all of the components equals 9.5 ns. This is shown by the figure below.

![Figure 78 - VCO outputs, transient response](image)

With this delay it should be possible to reach an output frequency of at least 52.6 MHz. The figure above shows the output and the integration. A difference in delay can be found, due to process corners. The point of switching changes due to a changing dc-voltage on the other input of the comparator. This dc point has been established by a bias current through a 100 kΩ resistor, resulting in a typical dc-voltage of 1.0 V. The figure and table below show the output characteristics of the VCO. In which \( K_0 \) is the derivative of the Voltage to frequency relation, taken from 20 MHz till 50.67 MHz.

<table>
<thead>
<tr>
<th>Table 17 - VCO output characteristics</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
</tr>
</thead>
<tbody>
<tr>
<td>Max Output frequency Range</td>
<td>55.6 MHz</td>
<td>99.7 MHz</td>
<td>158 MHz</td>
</tr>
<tr>
<td>Max Load</td>
<td>5 pF</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Power (depending on freq)</td>
<td>0.77 mW</td>
<td>18 mW</td>
<td></td>
</tr>
<tr>
<td>Input Voltage Range</td>
<td>0.0 V</td>
<td>3.0 V</td>
<td></td>
</tr>
<tr>
<td>Temperature Range</td>
<td>-40 °C</td>
<td>27 °C</td>
<td>125 °C</td>
</tr>
<tr>
<td>( K_0 )</td>
<td>27.2 MHz</td>
<td>88.2 MHz</td>
<td>159 MHz</td>
</tr>
<tr>
<td>Vdd range</td>
<td>3 V</td>
<td>3.3 V</td>
<td>3.6 V</td>
</tr>
<tr>
<td>Iref range</td>
<td>7 µA</td>
<td>13 µA</td>
<td></td>
</tr>
</tbody>
</table>
A lot of variation of the output frequency has been obtained; this is due to variations at all process corners, like:

- Parasitic capacitors
- Variations in resistor values
- Variations in capacitor values
- Difference of $V_{gs}$ of the input

### 6.6. Loop filter

The loop filter in a PLL has an important function. The loop filter will set some of the performance parameters of the PLL. Parameters like phase noise, spurious outputs and the settling time. The loop-transfer needs to be calculated, to determine the loop filter parameters.

A simple RC filter will be used for first approximation; this will introduce an additional pole. The transfer of this filter equals:

$$F(s) = R + \frac{1}{sC}$$

The total transfer function of the PLL is given by:

$$H(s) = \frac{K_d K_0 F(s)}{s^2 + K_d K_0 F(s) + \frac{1}{N}}$$

In which $K_d$ is the gain of the PFD and charge pump, $K_0$ is the voltage to frequency gain of the VCO and $F(s)$ is the transfer of the loop filter.
This can be rewritten as:

$$H(s) = \frac{K_d K_0 \left( R + \frac{1}{sC} \right)}{s + \frac{K_d K_0 \left( R + \frac{1}{sC} \right)}{N}}$$

$$H(s) = \frac{sK_d K_0 R + \frac{K_d K_0}{C}}{s^2 + s \left( R K_d K_0 \right) + \frac{K_d K_0}{N C}}$$

The denominator of a classic harmonic oscillator transfer can be described as:

$$s^2 + 2s\xi\omega_n + \omega_n^2$$

Solving this for the PLL loop results:

$$\omega_n = \sqrt{\frac{K_0 K_d}{N C}}$$

This is the frequency of the signal, which is providing the lock of the frequency.

$$\xi = \frac{\omega_n RC}{2}$$

This is the damping of this signal.

In both cases the poles are complex when $\xi < 1$, a high peaking transfer is unwanted because in that case the VCO driving voltage will also have a large peek, and this can be annoying. So by choosing $\xi$ the following should be taken into account:

- Overshoot
- Effective integration noise
- Catch behavior

The PLL properties are discussed below.

- Static phase difference:
  Assuming $\Delta \omega_0$ to be the difference between the frequency of the oscillator and the outer frequency, then the VCO input signal has to be returned by $\frac{\Delta \omega_0}{K_0}$, this has to be delivered by the phase-frequency detector via the loop filter: $F(0)K_d \Delta \theta = \frac{\Delta \omega_0}{K_0}$, which gives us:

$$\Delta \theta = \frac{\Delta \omega_0}{K_0 K_d F(0)}$$

In the case of a passive filter $F(0) = 1$. So the phase difference is set by $K_0 K_d$. When this gives poor results, an active filter can be used, so that: $F(0) = A$. 
Noise properties:
The goal of the PLL is to remove the unwanted signals as much as possible. These unwanted signals will be minimized by averaging over a given time: \( T_{\text{avg}} = \frac{1}{B_L} \). \( B_L \) is the noise bandwidth of the PLL. By increasing the averaging time, we decrease the noise at the output. Assuming Gaussian noise, the noise bandwidth follows per definition from:

\[
B_L = \frac{\int_0^\infty |H(j\omega)|^2 df}{|H(0)|^2}
\]

Working this out gives us:

\[
B_L = \frac{\omega_n}{2} \left( \xi + \frac{1}{4\xi} \right)
\]

This noise can cause a “cycle-slip”, this is when the output signal does not follow the input signal for 1 or more periods, as a consequence of the noise. \( \xi = 0.5 \) seems to give the best results, but considering the overshoot \( \xi = 1 \) would be better. The bandwidth is not much more than when \( \xi = 0.5 \). It is considered that the input noise of the clock signal is negligible, since a crystal oscillator has been used.

Figure 80 – noise Bandwidth versus the chosen \( \xi \)
Catch behavior:
The catching behavior is mostly determined by the settling time. The settling time is the time which is required to get to the wanted frequency, and the lock time is the time which is required to get to the final value without cycle slipping. By taking a look at the following equation, which is an example of a typical 2nd order system (adopted from 6)

$$v_{cont}(t) = 1 - \frac{1}{\sqrt{1-\xi^2}} e^{-\xi \omega_n t} \sin\left(\frac{\omega_n t}{\sqrt{1-\xi^2}}\right)$$

It can be seen that the factor $e^{-\xi \omega_n}$ defines the envelope of the dying oscillation. If we want to be in a given band of the total frequency range, given by:

$$\frac{f_a}{f_{step}}$$

It can be found that the factor $e^{-\xi \omega_n}$ has to be lower than this value, to settle in a given time into this frequency range.

$$e^{-\xi \omega_n} < \frac{f_a}{f_{step}}$$

Writing this out gives:

$$\omega_n = \frac{-1}{2\pi \xi} \ln\left(\frac{f_a}{f_{step}}\right)$$

The loop filter can be calculated with these formulas, for this a few parameters have been determined:

<table>
<thead>
<tr>
<th>Table 18- PLL parameters</th>
</tr>
</thead>
<tbody>
<tr>
<td>$f_{step}$</td>
</tr>
<tr>
<td>$t_s$</td>
</tr>
<tr>
<td>$f_a$</td>
</tr>
<tr>
<td>$K_d$</td>
</tr>
<tr>
<td>$K_0$</td>
</tr>
<tr>
<td>$\xi$</td>
</tr>
</tbody>
</table>

These values can be explained by the following:
- $f_{step}$: The maximum frequency change within one hop. So from 50.7 MHz to 20 MHz
- $t_s$: The maximum time which is required to step to a new frequency
- $f_a$: The frequency variation of the carrier within the desired time
- $K_d$: Gain of the PFD
- $K_0$: Gain of the VCO
- $\xi$: Damping factor

---

Now we can start calculating:

- The required division equals:
  \[ N = \frac{\text{Max VCO freq}}{\text{Channel Spacing}} = \frac{50.7 \text{ MHz}}{50 \text{ kHz}} = 1014 \]

- The wanted natural frequency:
  \[ \omega_n = -\frac{1}{2\pi \tau_s \xi} \ln \left( \frac{f_a}{f_{\text{step}}} \right) \]

- This can be met by setting \( C \) equal to:
  \[ C = \frac{I_p K_0}{N \omega_n^2} \]

- This leaves for \( R \):
  \[ R = 2 \xi \sqrt{\frac{N}{I_p K_0 C}} \]

- The capacitor for reducing the ripples
  \[ C_2 = \frac{C}{10} \]

The last part is to take spurious outputs into account, which can be caused by: leakage of the charge pump or mismatched currents of the charge pump.

It is known that these spurs will get smaller for narrower loop bandwidths and by better filtering. These spurs will appear at a spacing of \( f_{\text{clk}} \) from the carrier. So by minimizing these spurs, the phase noise will be increased significantly.

The following can be found: by increasing the bandwidth, the lock time will be decreased, but the spur gain will increase, which will result in larger spurs. The table below gives an overview of points of operations of the PLL. It can be found that a value of approximately 30 (\( f_{\text{clk}}/\text{LBW} \)) will give the best results. The loop-bandwidth can be given by:

\[ \text{LBW} = \frac{\omega_n}{2} \left( \xi + \frac{1}{4\xi} \right) \]

From the frequency divider it is known that the clock frequency has to be 25 kHz, to take steps of 50 kHz.

<table>
<thead>
<tr>
<th>Very likely Instability</th>
<th>Slight instability</th>
<th>Optimal Stability</th>
<th>Slight Cycle Slipping</th>
<th>Severe Cycle Slipping</th>
</tr>
</thead>
<tbody>
<tr>
<td>PLL will probably not lock at all.</td>
<td>Lock time may be increased.</td>
<td>Analog lock time models serve as a good approximation.</td>
<td>Cycle slipping may be visible. If so, lock time will be increased a little.</td>
<td>Lock time is likely to be severely degraded.</td>
</tr>
<tr>
<td>0</td>
<td>5</td>
<td>10</td>
<td>50</td>
<td>400</td>
</tr>
</tbody>
</table>

\(^7\) Can be found at [6]
To reduce the spurs somewhat further, another filter has been added, which reduces the spur gain. This product will be 1/10 of the product of the first filter; in this case it does not add a dominant pole. All these values are simulated in matlab, and by sweeping the settling time, the following results were observed:

- R = 47.5 Ω
- C = 31.205 µF
- LBW = 843 Hz
- Division = 29.6, which is close to 30
- C_ripple = 3.12 µF
- R_spurs = 47.5 Ω
- C_spurs = 3.12 µF

These C’s are chosen to put outside the chip, otherwise they would take too much space on the chip.

### 6.6.1. Corners

Due to process corners it is possible that certain parameters are different than the nominal case. These variations can be found in the previous paragraphs. They can be used to determine the overshoot and the settling time. These variations are given in

<table>
<thead>
<tr>
<th>table 20 - input values PLL calculation</th>
<th>min</th>
<th>nom</th>
<th>max</th>
</tr>
</thead>
<tbody>
<tr>
<td>R</td>
<td>39.9</td>
<td>47.5</td>
<td>55.1</td>
</tr>
<tr>
<td>C</td>
<td>31.205</td>
<td>31.205</td>
<td>31.205</td>
</tr>
<tr>
<td>K₀</td>
<td>27.2 MHz</td>
<td>88.2 MHz</td>
<td>159 MHz</td>
</tr>
<tr>
<td>K_d</td>
<td>670 µA</td>
<td>1000 µA</td>
<td>1337 µA</td>
</tr>
</tbody>
</table>

Putting these values into MATLAB, the following results are obtained:

<table>
<thead>
<tr>
<th>Table 21 - output values</th>
<th>min</th>
<th>nom</th>
<th>max</th>
</tr>
</thead>
<tbody>
<tr>
<td>ξ</td>
<td>0.53</td>
<td>1</td>
<td>1.58</td>
</tr>
<tr>
<td>Clk/BW</td>
<td>15.48</td>
<td>29.6</td>
<td>57.6</td>
</tr>
</tbody>
</table>

![Figure 81 - matlab output root-locus PLL, (upper left: nominal, bottom left: min, bottom right: max)](image)
6.7. PLL characteristics

By taking the calculated values, the PLL has been simulated. The results are shown below. One adjustment has been made: the resistor value has been changed into 270 Ω.

The reason for this adjustment is because the simulation results did not match the calculated results, this can be caused by a difference in $K_0$, which is much higher at local places. Due to\(^8\) a phase noise of around -100 dBC can be obtained with this type of PLL.

---

\(^8\) [14] Noise Analysis of Phase-Locked Loops, Amit Mehrotra, Department of Electrical and Computer Engineering, University of Illinois at Urbana-Champaign
Figure 84 - PLL-Filter output signal at worst-case process corner

Table 22 - output values PLL

<table>
<thead>
<tr>
<th></th>
<th>Min</th>
<th>Max</th>
</tr>
</thead>
<tbody>
<tr>
<td>Power</td>
<td>0.82 mW</td>
<td>21.4 mW</td>
</tr>
<tr>
<td>Frequency range</td>
<td>0 MHz</td>
<td>&gt; 55.6 MHz</td>
</tr>
</tbody>
</table>
7. Differential to Single-Ended

The next amplifier is used for a differential to single ended conversion. This is required as discussed in Chapter 5. Some loss at the mixers is introduced, to overcome that loss, some gain has been added here. The table below gives the wanted properties which have to be met by this amplifier.

<table>
<thead>
<tr>
<th>Property</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
</tr>
</thead>
<tbody>
<tr>
<td>Working frequency</td>
<td>50.7 MHz</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Gain @ 50.7 MHz</td>
<td>$\pi^2$</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Current working range</td>
<td>7 µA</td>
<td>13 µA</td>
<td></td>
</tr>
<tr>
<td>Voltage working range</td>
<td>3.0 V</td>
<td>3.3 V</td>
<td>3.6 V</td>
</tr>
<tr>
<td>Max input source impedance</td>
<td>2 kΩ</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Temperature Range</td>
<td>-40 °C</td>
<td>27 °C</td>
<td>125 °C</td>
</tr>
<tr>
<td>Noise @ 50kHz BW</td>
<td>-120 dB</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Distortion IM3 @ 50kHz</td>
<td>40 dB</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

First of all we will start to determine our feedback network in 7.1. After that the ‘nullor’ can be designed in 7.2. After that the stability of this amplifier will be discussed in 7.3. The properties of the amplifier are given in 7.4. In 7.5, resistor matching will be taken into account, because when they do not match they can differ a bit, this has some influence on the gain.

7.1. Feedback Amplifier

The chosen network is not the best of all, since the gain is depending on the input impedance. The reason that this network has been used is because of the fact that only one amplifier is required and that an AGC is used as output stage. The gain is set by four resistors. With the values of: 20 kΩ and 49.35 kΩ. The reason for these values is because of the fact that the input impedance had to be as high as possible to get the entire signal out of the buffer into this amplifier, due to the output impedance of the buffer.
7.2. Amplifier Design

A two stage amplifier has been used to get enough gain. Both stages are 50 \( \mu \text{m}/0.7 \text{ \( \mu \text{m} \)). The mirror above has the same dimensions as the output stage. In that case both transistors of the input stage are loaded the same and thus their drain voltage will be the same and thus the distortion will be lowered, due to symmetrical operations. For this reason also the current of the 2\textsuperscript{nd} stage is half of the 1\textsuperscript{st} stage. In this case all the transistors have the same bias current.

The figure below shows the gain of the amplifier without any compensation or feedback. Enough gain is obtained.
7.3. Stability

The amplifier is not stable of itself, so stabilization needs to be done. The same approach as explained in chapter 3.4 has been used. So a capacitor has been added over the feedback, functioning as a phantom zero, and a capacitor has been added over the output stage. The plots below show us the pole positions before and after compensation. It is shown that the system is stable now (Figure 89).

7.4. Properties

Some properties of the Amplifier are of interest. These are:

- Noise Properties
- Distortion Properties
- Open Loop Gain
- Closed Loop Gain
- PSRR

First of all the open- and closed-loop gain is shown. There is still open-loop gain at 50.7 MHz, this holds that the closed-loop gain is still determined by the feedback, as explained in 3.1. This is also shown in the second figure below.
Distortion is shown in Figure 92. Both harmonic distortion and IM3-distortion can be found. These parameters are given in Table 24.

The next two plots are the noise and PSRR behavior of the system. All these parameters are given in Table 24.
7.5. Resistor Matching

Both resistors are implemented on-chip and thus there has to be dealt with resistor matching. The matching is given by:

\[
\sigma \left( \frac{\Delta R}{R} \right) = \frac{A_R}{\sqrt{W \cdot L}}
\]

For rpolyh $A_R=6.5\%$. Thus the matching is $(3\sigma)$: 3.19%, because $W/L$ equals $1.6 \mu m/23.35 \mu m$. The table below gives all the properties of this amplifier.

<table>
<thead>
<tr>
<th>Property</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
</tr>
</thead>
<tbody>
<tr>
<td>Input impedance</td>
<td>121.1 fF</td>
<td>133 fF</td>
<td>144.4 fF</td>
</tr>
<tr>
<td>Power</td>
<td>1.59 mW</td>
<td>2.56 mW</td>
<td>3.617 mW</td>
</tr>
<tr>
<td>Gain @ 50.7MHz</td>
<td>6.812 dB</td>
<td>7.889 dB</td>
<td>8.644 dB</td>
</tr>
<tr>
<td>Open Loop Gain @ 50.7MHz</td>
<td>20.29 dB</td>
<td>22.78 dB</td>
<td>25.77 dB</td>
</tr>
<tr>
<td>Output impedance</td>
<td>40.3 Ω</td>
<td>58.9 Ω</td>
<td>79.2 Ω</td>
</tr>
<tr>
<td>Max load</td>
<td>250 fF</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Distortion IM3 HD</td>
<td>73 dB</td>
<td>101 dB</td>
<td>101 dB</td>
</tr>
<tr>
<td>Noise @ 50.7MHz BW 50kHz</td>
<td>-186.7 dB</td>
<td>-189.1 dB</td>
<td>-192.3 dB</td>
</tr>
<tr>
<td>Current working range</td>
<td>7 µA</td>
<td>10 µA</td>
<td>13 µA</td>
</tr>
<tr>
<td>Voltage working range</td>
<td>3.0 V</td>
<td>3.3 V</td>
<td>3.6 V</td>
</tr>
<tr>
<td>PSRR @ 50.7MHz</td>
<td>12.9 dB</td>
<td>15.36 dB</td>
<td>16.6 dB</td>
</tr>
</tbody>
</table>

7.6. Biasing

For biasing purpose a resistor has been added to the positive input of the amplifier. This is required because the dc voltage of the mixer cannot be used, because in that case the amplifier will not be biased properly during half of the time. This resistor is connected to a bias current to obtain a voltage of approximately 1.5 V. This value can change somewhat over the corners, since $I_{bias}$ will change and the resistor value can change. With this value as gate voltage we will have enough voltage headroom for the biasing mirror, which is thus at every corner saturated.
8. Automatic Gain Control

An AGC is required to keep the dynamic range as large as possible. An AGC consists of the following parts:

- A Variable Gain Amplifier: its gain can be adjusted by adjusting its control signal
- A Peak detector: This device will track the peak of the output signal
- An Amplifier: which compare this peak signal to a well-known $V_{top}$
- A loop filter: required to delay the loop, to minimize the problem of unwanted signals

In 8.1 the peak detector will be discussed. In 8.2 and 8.3 the amplifier and VGA are discussed respectively. All these parts will be combined and the filter will be determined in 8.4. In 8.5 a final look will be taken at the total gain which is produced by the entire design.
8.1. Peak Detector

The input shape of the signal is not known, for this a peak detector has been chosen. For the peak detector a simple Peak Detect and Hold has been used. The configuration is demonstrated below.

![Peak Detector Configuration](image)

This amplifier with current-mirror compensation is proposed by Kruiskamp and Leenaerst\(^9\). A current-mirror has been used as the rectifying element. The current mirror is driven by an operational amplifier \(G_0\). The stability of this configuration is easy to achieve, as has been explained in Appendix C of [12]. The current of the mirror charges the capacitor, which can discharge itself via the resistor. The output buffer has been added to provide driving capability. It is known that the input signal is at 10.7 MHz, and keeping in mind a parameter deviation, a bandwidth equal to 4 kHz has been taken. In that case the output signal does not respond immediately to signals on higher frequencies, and at the worst corners we still observe a bandwidth large enough. The bandwidth is chosen such that output is nearly to dc, in that case a stable output voltage can be obtained, which does not respond on a down-going flank of the input signal. \(C\) is chosen to be 20 pF, since the speed is determined by the output current. As addition for the discharging of the cap, a 2 M resistor has been added. The implementation of the buffer has been shortly discussed in 8.1.1. In 8.1.2 the properties of the peak detector will be discussed.

### 8.1.1. Amplifier Peak Detector

The task of this buffer is to amplify the difference of its inputs as good as possible. The input is chosen to be 30 \(\mu\)m/0.7 \(\mu\)m, with a current of 300 \(\mu\)A, in that case there is enough gain to keep the error of the output as low as possible. To be sure the circuit is saturated at every corner and to keep the matching error limited: the mirror above has been chosen to be equal to 50 \(\mu\)m/0.7 \(\mu\)m.

An important parameter of this amplifier is its input offset, which comes from the differential pair mismatching and the current mismatch in the upper mirror. This can be calculated \(3\sigma\): 7.11 mV.

<table>
<thead>
<tr>
<th></th>
<th>Min</th>
<th>Max</th>
</tr>
</thead>
<tbody>
<tr>
<td>Matching error (3\sigma)</td>
<td>7.11 mV</td>
<td></td>
</tr>
<tr>
<td>Open loop gain</td>
<td>32.6 dB</td>
<td>41.9 dB</td>
</tr>
<tr>
<td>Working frequency</td>
<td>10.7 MHz</td>
<td></td>
</tr>
</tbody>
</table>
8.1.2. Peak-Detector Properties

The most important property of this peak detector is the output error. This is caused by: the finite DC-gain, the finite DC common mode rejection ratio, the input-to-input capacitive coupling. It is undesired that the output responds to power supply changes, for this reason we take a look at the PSRR. It is known that the information is at almost DC, thus these higher frequency power supply changes will be filtered out by the loop-filter, and thus no problems are expected. These both plots are given below. The output characteristics are given in Table 28.

<table>
<thead>
<tr>
<th>Table 26 - Properties Peak Detector</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Min</strong></td>
</tr>
<tr>
<td>Output Error</td>
</tr>
</tbody>
</table>
8.2. Amplifier

This amplifier only has the task to amplify the difference between the output of the peak detector and a constant voltage. This output will be used to drive the VGA. A single stage amplifier will be enough. By taking matching errors in account, while designing the amplifier, the following results are obtained:

![Figure 101 - Gain of the Amplifier](image)

Also for this amplifier it is important that the PSRR is not too high. The PSRR is shown in the figure below.

![Figure 102 - PSRR of the Amplifier](image)

These properties are summed up in table 27.

<table>
<thead>
<tr>
<th>table 27 - Output Properties Amplifier</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
</tr>
</thead>
<tbody>
<tr>
<td>Power</td>
<td>0.105 mW</td>
<td>0.166 mW</td>
<td>0.237 mW</td>
</tr>
<tr>
<td>PSRR</td>
<td>-44.15 dB</td>
<td>-46.4 dB</td>
<td>-50.3 dB</td>
</tr>
<tr>
<td>Gain</td>
<td>34.9 dB</td>
<td>37.6 dB</td>
<td>41.9 dB</td>
</tr>
<tr>
<td>Matching 3σ</td>
<td>11.28 mV</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
The third part of the AGC is the VGA, which is a variable gain amplifier. Its name implies its function. This is the main part of the AGC, since it determines the dynamic range of the AGC. Its input is a differential signal and the output needs to be single ended so that it can be connected to the internal delfi-n3Xt transmitter. The following structure has been chosen:

![VGA set-up](image)

### Table 28 - requirements of the VGA

<table>
<thead>
<tr>
<th>Requirement</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
</tr>
</thead>
<tbody>
<tr>
<td>required Gain</td>
<td>&lt;0  dB</td>
<td></td>
<td>&gt;80 dB</td>
</tr>
<tr>
<td>$V_{control}$</td>
<td>0 V</td>
<td>3.0 V</td>
<td></td>
</tr>
<tr>
<td>$V_{dd}$ range</td>
<td>3.0 V</td>
<td>3.3 V</td>
<td>3.6 V</td>
</tr>
<tr>
<td>Freq Range</td>
<td>10.7 MHz</td>
<td></td>
<td></td>
</tr>
<tr>
<td>$I_{ref}$ Range</td>
<td>7 µA</td>
<td>13 µA</td>
<td></td>
</tr>
<tr>
<td>Temperature Range</td>
<td>-40 °C</td>
<td>27 °C</td>
<td>125 °C</td>
</tr>
<tr>
<td>Noise @ BW=50kHz</td>
<td></td>
<td>-120 dB</td>
<td></td>
</tr>
<tr>
<td>Distortion IM3 @ 50kHz</td>
<td>30 dB</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

The gain of this amplifier is given by:

$$ \left( \frac{R_2}{R_1} \right) \left( \frac{R_3}{R_4} \right) $$

In which $R_1$ is a variable resistance, implemented by a mosfet. A disadvantage of this amplifier is that the gain is depending on the input impedance, this is not a real problem, since this is part of an AGC and thus the gain will be set depending of its output value. In 8.3.1 the first part of the amplifier will be discussed. The second part will be discussed in 8.3.2. These parts will be connected together in 8.3.3. One important aspect of the amplifiers is their matching error. This cannot be too large, since a large output swing is desired, thus the dc voltage should be as much as possible in the middle of the $V_{dd}$ and $V_{ss}$. 

---

**TU Delft**

Delft University of Technology
8.3.1. **VGA 1st stage**

<table>
<thead>
<tr>
<th>Requirement</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
</tr>
</thead>
<tbody>
<tr>
<td>Required Gain</td>
<td>&lt;0 dB</td>
<td>&gt;50 dB</td>
<td></td>
</tr>
<tr>
<td>Vcontrol</td>
<td>0 V</td>
<td></td>
<td>3.0 V</td>
</tr>
<tr>
<td>Vdd range</td>
<td>3.0 V</td>
<td>3.3 V</td>
<td>3.6 V</td>
</tr>
<tr>
<td>Freq range</td>
<td></td>
<td>10.7 MHz</td>
<td></td>
</tr>
<tr>
<td>Iref Range</td>
<td>7 µA</td>
<td>13 µA</td>
<td></td>
</tr>
<tr>
<td>Temperature Range</td>
<td>-40 °C</td>
<td>27 °C</td>
<td>125 °C</td>
</tr>
</tbody>
</table>

It has been already explained which kind of type the amplifier will be. The only thing left for us is implementing the feedback and the amplifier part.

**8.3.1.1. Feedback**

The feedback of this amplifier will be, as mentioned before, a mosfet with a resistor. By taking the size of the mosfet equal to: 50 µm/0.7 µm, a small on resistance is obtained, thus a large gain. With this value it is shown that there is enough gain at all the process corners. It cannot be taken too large, since in that case it would introduce a dominant pole. The resistor has been taken 4 MΩ.

**8.3.1.2. Amplifier Implementation**

This amplifier is a two stage amplifier, which should be enough to give enough gain to meet the required gain for this amplifier. The first stage is a differential input stage, so the second stage has to be a single amplifier stage to get negative feedback. The values are chosen such that the input capacitance is quite high and that there is enough gain to provide the required closed-loop gain.

**8.3.1.3. Stability**

For the stability a capacitor has been added over the input stage of 100 fF, to obtain some pole splitting. In the feedback a phantom zero has been introduced by adding a capacitor of 20 fF across the feedback resistor.

**8.3.1.4. Input Matching:**

The matching error at the input of the amplifier equals $3\sigma$: 3.69 mV. This matching should be as low as possible to keep the output range as large as possible.

**8.3.1.5. Characteristics**

With all this information the outputs of this amplifier can be discussed. The figures below show the bode-plots of the closed-loop gain at all the process corners. What can be seen is that the amplifier operates between the given requirements.
In 8.3.1.3 two capacitors are added to get the amplifier stable. The fact that this is true is shown in the figure below.
The other characteristics of the amplifier like intermodulation- and harmonic distortion are shown in the figures below.

![Figure 107 - IM3 distortion](image)

![Figure 108 - harmonic distortion](image)

All these outcomes are summarized in Table 30.

<table>
<thead>
<tr>
<th>Table 30 - VGA 1st stage properties</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
</tr>
</thead>
<tbody>
<tr>
<td>Gain @ Vcntrl =3</td>
<td>55.2 dB</td>
<td>60.1 dB</td>
<td>68.4 dB</td>
</tr>
<tr>
<td>Gain @ Vcntrl =0</td>
<td>-76.3 dB</td>
<td></td>
<td>-123.6 dB</td>
</tr>
<tr>
<td>Distortion HD</td>
<td>32.1 dB</td>
<td>34 dB</td>
<td>36.3 dB</td>
</tr>
<tr>
<td>Distortion IM3</td>
<td>48.5 dB</td>
<td>51 dB</td>
<td>53.6 dB</td>
</tr>
<tr>
<td>Power</td>
<td>1.61 mW</td>
<td>2.33 mW</td>
<td>3.55 mW</td>
</tr>
<tr>
<td>Noise @ BW 50kHz</td>
<td>-150 dB</td>
<td>-159.3 dB</td>
<td>-166.8 dB</td>
</tr>
<tr>
<td>Max load</td>
<td>0.5 pF</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Output impedance</td>
<td>44.9 kΩ</td>
<td>50.3 kΩ</td>
<td>55.4 kΩ</td>
</tr>
<tr>
<td>Input impedance</td>
<td>448.6 fF</td>
<td>539.1 fF</td>
<td>622.7 fF</td>
</tr>
<tr>
<td>PSRR</td>
<td>-24.6 dB</td>
<td>-25.3 dB</td>
<td>-28.1 dB</td>
</tr>
</tbody>
</table>
8.3.2. VGA 2nd stage

Table 31 - requirements of VGA 2nd stage

<table>
<thead>
<tr>
<th></th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
</tr>
</thead>
<tbody>
<tr>
<td>Maximum input capacitance</td>
<td></td>
<td></td>
<td>0.5 pF</td>
</tr>
<tr>
<td>Gain</td>
<td></td>
<td>34 dB</td>
<td></td>
</tr>
<tr>
<td>Output Swing</td>
<td>0.1 V</td>
<td>1.0 V</td>
<td></td>
</tr>
<tr>
<td>I range</td>
<td>7 µA</td>
<td>13 µA</td>
<td></td>
</tr>
<tr>
<td>Temperature Range</td>
<td>-40 °C</td>
<td>27 °C</td>
<td>125 °C</td>
</tr>
<tr>
<td>V&lt;sub&gt;dd&lt;/sub&gt; range</td>
<td>3.0 V</td>
<td>3.3 V</td>
<td>3.6 V</td>
</tr>
</tbody>
</table>

The second stage is quite similar to the first stage, only in this case a larger output swing and a constant gain should be obtained. The input transistors are chosen such that the output has a lower saturation voltage, by placing the gate-source voltage of the output nearly equal to the threshold voltage, since \( V_{gs} \approx V_{gs} - V_{th} \). The second stage and upper mirror are chosen to be equal. The figures and table below shows that the amplifier is between its boundaries and operates as it should be.
8.3.2.1. Matching

The matching of this amplifier equals \( (3\sigma) \): 7.44 mV

8.3.3. Entire VGA

By combining these two stages, the entire VGA is constructed. Simulating this VGA gives the following results:

<table>
<thead>
<tr>
<th>Table 33 - VGA characteristics</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Min</strong></td>
</tr>
<tr>
<td><strong>Gain</strong></td>
</tr>
<tr>
<td><strong>Power</strong></td>
</tr>
<tr>
<td><strong>Output Swing</strong></td>
</tr>
</tbody>
</table>

A capacitor has been added to de-couple the dc voltage of the input signal. A 50 pF capacitor has been chosen. This added zero is far enough from the wanted 10.7 MHz. As shown in the figures below.
8.3.3.1. DC-Point Corners

A dc voltage of 1.5 V is required for proper biasing of the VGA. 1.5 V has been chosen since it is half of the power supply (at the worst case). In this case an output swing of 1.0 V should still be obtained. This 1.5 V is constructed by taking a biasing current and a 160 kΩ resistor. This dc point can vary at all the process corners, as shown in the figure below.
8.3.3.2. Matching error entire VGA

The total matching error of the biasing point of the VGA can be easy calculated. This is important as explained before. We care about the DC output biasing voltage of the VGA. So that is both the matching errors summed up. Since we are talking about stochastic values we have to square them. This gives a total matching error of $(3\sigma)$: $8.31 \text{ mV}$.

8.3.3.3. Additional capacitor

A capacitor of 1 fF has been added between the lower resistor of the first amplifier and ground. This is to ground the signal for AC signals, but not for DC. 1 fF is enough since we only want ‘ground’ the AC signal. Taking this C larger, it can cause a dominant pole, which should not be there.

8.4. Entire AGC

Now that all the parts of the AGC are determined, the only thing left to do is combining all these parts, and determining the Filter. This filter will be discussed in 8.4.1. Also the entire matching error of the AGC is important, because this error reduces the maximum swing we can make at the output of the amplifier. A look at this matching error will be taken in 8.4.2. At last the entire AGC properties are discussed in 8.4.3.

8.4.1. Loop Filter

A simple first order filter will be enough, so one R and C combination is enough. Taking a bandwidth of 50 kHz we obtained the following values for R and C: 40 MΩ and 70 pF, taking this bandwidth very low, makes the loop stable, because the control signal of the VGA will not vary at each change in the loop.

8.4.2. Total Matching Error

All the numbers on matching errors and output variations are known, so the total error of the biasing dc voltage can be calculated and a look at the total output swing can be taken. This can be easy calculated; first the total $\sigma$ error of the DC point at the VGA should be calculated. By adding the dc-biasing error and the peak detector error, the entire error can be found. These values have to be between the requirements as given in Table 33.

The total $\sigma$ of the AGC can be calculated the following:

$$
\sigma_{total} = \sqrt{\sigma_{VGAtotal}^2 + \sigma_{Peak}^2 + \sigma_{Amp}^2}
$$

$$
\sigma_{total} = 5.23 \text{ mV}
$$

$$
3\sigma = 15.71 \text{ mV}
$$

In addition to this matching error, the peak detector error and the dc-bias point error can be added.

$$
3\sigma_{total} + \Delta_{peak, error} + \Delta_{dc, bias\ error}
$$

This gives a total error of:

| Total Error (3\sigma) | -118.55 mV | 152.51 mV |

This is the error of the 1.5 V biasing voltage, adding a 1 V swing, a voltage swing can be found at: $0.38\text{V}-2.65\text{V}$. This is between the limits for the output swing of the VGA 2nd stage.
8.4.3. AGC Properties

The table below shows the properties of the AGC. To prove its working also its transient response has been shown.

<table>
<thead>
<tr>
<th>Table 34 - AGC properties</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Output swing</strong></td>
</tr>
<tr>
<td><strong>Power</strong></td>
</tr>
<tr>
<td><strong>Gain</strong></td>
</tr>
<tr>
<td><strong>V_{top} range</strong></td>
</tr>
</tbody>
</table>

8.5. Entire Gain OLFAR

The total gain of the AGC is known, so the total range of the input signals of the OLFAR chip can be calculated. A gain of at least -19.45 dB till 123.38 dB is obtained; this is the case at the worst process corner.

Taking in mind the loss at the antennas, as shown in 3.3.1, the minimum and maximum input signal can be calculated:

\[
Max, In = 21.658dB + (\log (\text{output swing}) \times 20)
\]

\[
Min, In = -121.17dB + (\log (\text{output swing}) \times 20)
\]

Table 35 - Input range of the entire chip

<table>
<thead>
<tr>
<th>Input signal</th>
<th>Output signal</th>
<th>0.01V</th>
<th>0.1V</th>
<th>1V</th>
</tr>
</thead>
<tbody>
<tr>
<td>Minimum</td>
<td>-161.17dB</td>
<td>-141.17dB</td>
<td>-121.17dB</td>
<td></td>
</tr>
<tr>
<td>Maximum</td>
<td>-18.342dB</td>
<td>-2.5dB</td>
<td>-2.5dB</td>
<td></td>
</tr>
</tbody>
</table>

We see that for the maximum input signal we are limited due to the LNA and its biasing.
9. Band-Gap Reference

A stable voltage reference is required to keep the biasing currents constant; therefore a band-gap reference has been designed. A band-gap reference makes use of the fact that a diode has a negative temperature coefficient, and the voltage difference between two differently driven diodes has a positive temperature coefficient. By combining these two effects in the right way, the temperature dependency of the reference voltage cancels. The working range of the band-gap is shown in the table below.

<table>
<thead>
<tr>
<th>Table 36 - operating range band-gap</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
</tr>
</thead>
<tbody>
<tr>
<td>Output Voltage</td>
<td>1.20 V</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Temperature Range</td>
<td>-40 °C</td>
<td>27 °C</td>
<td>125 °C</td>
</tr>
<tr>
<td>Vdd range</td>
<td>3.0 V</td>
<td>3.3 V</td>
<td>3.6 V</td>
</tr>
<tr>
<td>Frequency Range</td>
<td>DC</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

A temperature derivative of 0 is required; in that case a constant voltage over the entire temperature range can be found. In formula:

\[
\alpha_1 \frac{\partial V_1}{\partial T} + \alpha_2 \frac{\partial V_2}{\partial T} = 0,
\]

\(\alpha_1\) and \(\alpha_2\) are parameters which are free to choose. \(V_1\) and \(V_2\) are the voltage across bipolar transistors. If this formula can be met, we obtain a reference voltage of:

\[
V_{\text{Ref}} = \alpha_1 V_1 + \alpha_2 V_2,
\]

with a zero Temperature Coefficient.

1.20V is wanted, since this is known to be close to the theoretical 1.22 eV band-gap of silicon at 0 K. In paragraph 9.1 the used bipolar devices are discussed. In 9.2 and 9.3 a look at the temperature coefficients of these bipolar devices has been reviewed. They will be combined to a band-gap reference in 9.4. Since the band-gap is the most important part of the IC, we have to be sure that it works in all conditions. To guarantee its working a look at forbidden states has been made in 9.5. In the remaining paragraphs matching (9.6), enabling circuit (9.7) and the overall characteristics of this band-gap (9.8) are discussed.
9.1. Used Bipolar devices
The bipolar devices which have been used are vert10 devices, which are vertical bipolar transistors. They use the substrate as the collector, the well as the base and diffusion as the emitter. The reason that we took this bipolar device is because it has a smaller deviation of $V_{be}$. This is a result of the fact that vertical bipolar transistors can be made more exact since implantation is more precise compared to lithography.

9.2. Negative TC
The forward voltage of a pn junction has a negative TC. Explained below, it is known that:

$$I_C = I_S e^{v_{be}/V_T}, \text{with } V_T = \frac{kT}{q}$$

We can write this as:

$$V_{be} = V_T \ln \left( \frac{I_C}{I_S} \right)$$

To simplify the analysis, it is assumed that $I_c$ is kept constant. Thus it can be seen that:

$$\frac{\partial V_{be}}{\partial T} = \frac{\partial V_T}{\partial T} \ln \left( \frac{I_C}{I_S} \right) - \frac{V_T}{I_S} \frac{\partial I_S}{\partial T}$$

The dependence of $V_T$ on the temperature and that of $I_s$ should be known. That is a more complex formula, from which it is known that it is proportional to $\mu kT n_i^2$, in which $\mu$ and $n_i^2$ are temperature dependent. Completing this formula:

$$\frac{\partial V_{be}}{\partial T} = \frac{V_{be} - (4 + m)V_T - E_g}{T}$$

This gives a negative TC, as also can be seen in the figure below:

![Figure 117 - negative Temperature Coefficient](image-url)
From the figure, we see that \( \frac{\partial V_{be}}{\partial T} = -\frac{2.07mV}{K} \). This coefficient depends itself on the temperature. This creates an error in the reference voltage.

### 9.3 Positive TC

Taking two bipolar transistors operating at unequal current densities, the difference in their base-emitter voltages is positive depending on the temperature.

\[
\Delta V_{be} = V_{be1} - V_{be2} = V_T \ln \left( \frac{n I_0}{I_{S1}} \right) - V_T \ln \left( \frac{I_0}{I_{S2}} \right) = V_T \ln(n)
\]

In which \( n \) is the factor of the difference in current densities. Thus:

\[
\frac{\partial \Delta V_{be}}{\partial T} = \frac{k}{q} \ln(n)
\]

This is not temperature dependent, compared to the negative TC which is temperature dependent.

A positive TC can be found in figure 118.

### 9.4 BandGap reference

Combining these two properties, and implementing the weight factors \( \alpha_1 \) and \( \alpha_2 \), we get the wanted band-gap reference. This is done by the figure shown below, which can be explained as the following: MN0, MN1 and MP0, MP1 are identical. Thus \( I_{D1} = I_{D2} \), and we see that \( V_X = V_Y \). By varying the transistor sizes we can obtain the currents equal to:

\[ I_{D1} = 0.578 \mu A \text{ and } I_{D2} = 0.577 \mu A \]
Over the resistor $R_1$, we obtain the voltage difference between the base-emitter voltages of $Q_0$ and $Q_1$. It is assumed that $V_x = V_y$. Thus $V_{R1} = \Delta V_{BE} = V_1 \ln(n)$, in this case $n = 10$, and so the current through $R_1$ equals $I_{R1} = \frac{V_T \ln(10)}{R_1}$ and thus $I_{DS} \approx 4 \cdot I_{R1} = \frac{4V_T \ln(10)}{R_1}$.

This gives us a reference voltage of:

$$V_{ref} = V_{BE2} + \frac{4V_T \ln(10)}{R_1} \frac{R_2}{R_2}$$

Differentiating this to the temperature gives us:

$$\frac{\partial V_{ref}}{\partial T} = \frac{\partial V_{BE2}}{\partial T} + R_2 \frac{\partial I_{DS}}{\partial T}$$

Assuming temperature coefficient of $R2$ is zero.

What we now want is a zero TC, so:

$$\frac{\partial V_{BE2}}{\partial T} + R_2 \frac{\partial I_{DS}}{\partial T} = 0$$

We already know that the first factor equals $-2.07\text{mV}$. Thus solving this equation, we see that:

$$R_2 \frac{\partial I_{DS}}{\partial T} = \frac{4k \ln(10)}{q} \frac{R_2}{R_1}$$

$$= (7.934 \times 10^{-4}) \left(\frac{R_2}{R_1}\right) \left[\frac{V}{k}\right]$$
Thus:

\[
\frac{R_2}{R_1} = \frac{2.07 \times 10^{-3}}{7.934 \times 10^{-4}} = 2.61
\]

Taking the output equal to 1.20 Volts:

\[
V_{\text{Ref}} = 0.446 + 2.308 \times 10^{-6} \times R_2 = 1.20 V
\]

Resulting:

\[
R_2 \approx 331 \, k\Omega \Rightarrow R_1 \approx 127 \, k\Omega
\]

This did not show the exact wanted output reference voltage; this can be due to simplifying equations, like the temperature dependence of the negative TC. By taking \( R_2 = 338 \, k\Omega \) and \( R_1 = 144.4 \, k\Omega \). We see the following result:

The reason that we still see a curvature and not a constant line may be due to many reasons like:

1. Temperature variations of base-emitter voltages.
2. Temperature variations of collector currents.
3. Temperature variations of offset voltages.
9.5. Guarantee of operation

9.5.1. Forbidden stages

To guarantee a correct operation in all conditions of this the states in which the voltage reference can be should be reviewed. The state in which \( V_x = V_y = V_{md3,d} = 0 \) V and \( V_{md4,d} = 3.3 \) V, it seems that in that state the voltage reference is incapable of getting out of this stage. To prevent the voltage reference to get into this state the output can be measured, which will be equal to 0 volts in that case, and when this output approaches 0 V, \( V_{md4,d} \) can be pulled down. There needs to be measured at the output and not at \( V_{md4,d} \), because that could influence the operation of the band-gap reference.

9.5.2. Startup Circuit

A start-up circuit is required, because this device cannot start itself when going from ‘off’ to ‘on’. In this case it may come in one of the forbidden stages, so no voltage at the output would be there. So this problem is solved already. This is shown at Figure 122.

![Figure 122 - start-up of band-gap circuit](image)

9.6. Matching

Due to current mismatches in the upper mirror and voltage mismatch in the lower mirror a total mismatch at the input can be obtained:

Mismatch \((3\sigma) = 8.35 \) mV

The lower mirror gives a voltage difference in \( V_x \) and \( V_y \). In that case \( V_{R1} = \Delta V_{be} \). Also a mismatch in the current mirrors could be found. This results also in a difference, which cause a different output voltage.

9.7. Enable

The lower enable switch has been made 20 µm/0.35 µm to be sure that we have low impedance, and all the current will flow through this switch, to make the output voltage equal to 0 Volt. The plots below show the difference:
9.8. Characteristics

Due to parameter spread, as discussed in 1.4.8, it is possible that the output varies. Figure 125 shows the output voltage due to this parameter spread.

<table>
<thead>
<tr>
<th>Table 37 - output characteristics Band-Gap</th>
</tr>
</thead>
<tbody>
<tr>
<td>Min</td>
</tr>
<tr>
<td>--------------------------------------------</td>
</tr>
<tr>
<td>Output Voltage</td>
</tr>
<tr>
<td>Power</td>
</tr>
</tbody>
</table>

Figure 123 - response with a small switch (0.4 µm / 0.35 µm)

Figure 124 - response with a large switch (20 µm / 0.35 µm)

Figure 125 – Output voltage over all the process corners
10. Current Reference

For the bias currents a voltage to current translation is required. This can be simply done by taking an amplifier. The feedback network for this amplifier has been discussed in 10.1. In 10.2 a closer look at the outputs of the amplifier has been taken. Matching plays a significant role in this amplifier, since there are restrictions to the output current. This matching is discussed in 10.3. In 10.4 a summary of the output characteristics has been given.

### Table 38 - bias current output characteristics

<table>
<thead>
<tr>
<th></th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
</tr>
</thead>
<tbody>
<tr>
<td>Input Voltage</td>
<td>1.163 V</td>
<td>1.202 V</td>
<td>1.327 V</td>
</tr>
<tr>
<td>Output current</td>
<td>7 μA</td>
<td>13 μA</td>
<td></td>
</tr>
<tr>
<td>Driving voltage</td>
<td>3.0 V</td>
<td>3.3 V</td>
<td>3.6 V</td>
</tr>
<tr>
<td>Frequency Range</td>
<td>DC</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Temperature Range</td>
<td>-40 °C</td>
<td>27 °C</td>
<td>125 °C</td>
</tr>
<tr>
<td>required bias outputs</td>
<td>20</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

#### 10.1. Feedback

As a feedback circuit the circuit of the figure below has been chosen. This is an ideal setup, since it is easy to mirror the output current to several outputs. 20 outputs are required to bias all the blocks of OLFAR. The gain of this amplifier equals:

$$I_{out} = \frac{U_{in}}{R}$$

The input voltage is known to be 1.202 V. Taking $R = 130$ kΩ, an output current of 9.3 μA is obtained. This is done since it is known that the variations over the process corners vary somewhat less down than up. This is also shown in table 40. This is caused by the negative temperature coefficient of $r_{polyh}$ and the fact that we look at the temperature range of -40 °C till 125 °C with 27°C nominal, so more variation up than down.
10.1.1. Nullor Implementation

Not much gain is required, for this reason a single stage amplifier has been chosen. There is no biasing current available jet, so a resistor of 1.5 kΩ has been used for biasing. This result in a not constant biasing current, but this should not introduce too much problems. The voltage drop across the resistor equals 400 mV, resulting in a bias current of 266 µA for this amplifier. The amplifier is saturated at all the process corners.

10.2. Outputs

The figures below show the open loop gain of this amplifier at all process corners. This amplifier seems to be stable of its own, so no compensation is required. To prove this the poles of the amplifier are shown in Figure 129.

The output current at all the process corners are shown in the figure below. This shows that the output currents are between the given output range.
10.3. Matching

Matching plays a significant role in this amplifier. The output currents vary a lot as shown in the previous paragraph. To keep these currents between the given limits, the matching should be reduced as much as possible. There are here three types which can cause an error in the output current. The first is by mismatching of the input transistors, the second one is caused by the upper mirror and the last one is caused by all the output mirrors. All these mismatches and the deviation of the output current, leads to the choice to take the output mirrors equal to 10 µm/10 µm. The calculations are done below:

<table>
<thead>
<tr>
<th></th>
<th>V_{gt} [V]</th>
<th>W/L [µm/µm]</th>
<th>g_{m} [S]</th>
<th>type</th>
</tr>
</thead>
<tbody>
<tr>
<td>Input</td>
<td>0.117</td>
<td>100/0.7</td>
<td>2.4m</td>
<td>nmos</td>
</tr>
<tr>
<td>Upper mirror</td>
<td>0.73</td>
<td>10/0.7</td>
<td>184.9u</td>
<td>pmos</td>
</tr>
</tbody>
</table>

\[
A_{V_{gs}}^2 = A_{V_{th}}^2 + \frac{1}{4} V_{gt}^2 \cdot A_{V_{th}}^2
\]

With the values above and from table E.1 results in:

\[
A_{V_{gs}}^2 = 9.04 \times 10^{-5}
\]

\[
\sigma_{\text{input}} = \frac{A_{V_{gs}}}{\sqrt{W \cdot L}}
\]

This is the \( \sigma \) of the input transistors. Also the upper mirror can cause a static input offset by mismatch in currents, which are translated to an input offset by the \( g_m \) of the input transistor, as shown below.

\[
A_{I_{th}}^2 = A_{I_{th}}^2 + \frac{4}{V_{gt}^2} \cdot A_{I_{th}}^2
\]

\[
A_{I_{id}}^2 = 1.58 \times 10^{-3}
\]

\[
\sigma = \frac{A_{I_{id}}}{\sqrt{W \cdot L}} = 0.015
\]

\[
\sigma \cdot I = 2.8 \mu A
\]

\[
\sigma_{\text{total}} = \sqrt{\sigma_{\text{input}}^2 + \left(\frac{2.8 \mu}{g_m}\right)^2}
\]

This gives results in a total matching error at the input of:
\[ \sigma = 1.62 \text{ mV} \]

Combining this \( \sigma \) with that one of the Voltage reference of 9.6, resulting in an input \( \sigma \) of:

\[ \sqrt{1.62^2 + 2.78^2} = 3.22 \text{ mV (1}\sigma) \]

The output at all the process corners results in a maximum deviation of 1\% at the output (@3\sigma), so a maximum of 0.33 \%, which equals 0.00336 \( \sigma_{\text{max}} \).

The \( \sigma_{\text{input}} \) equals: 3.22 mV of 1.202 V => 0.00268 \( \sigma \).
So:

\[ \sigma_{\text{out, max}} = \sqrt{\sigma_{\text{max}}^2 - 0.00268^2} = 0.002027 \]

By taking the output mirrors equal to 10 \( \mu \)m/10 \( \mu \)m, we obtain a \( \sigma_{\text{out}} \) of 0.0014. This is below \( \sigma_{\text{out, max}} \), so we are in the range of the 1\% max.

A maximum matching error at the output can be found:

\[ \sigma_{\text{out}} = \sqrt{0.00268^2 + 0.0014^2} = 0.00249 \]
\[ 3\sigma = 0.0075 \equiv 0.75\% \]

### 10.4. Characteristics

The output characteristics of this amplifier are shown in Table 39. Also the PSRR is shown in the figure below.

<table>
<thead>
<tr>
<th>Open Loop Gain</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>41.3 dB</td>
<td>50.2 dB</td>
<td>66.8 dB</td>
</tr>
<tr>
<td>PSRR @ low freq</td>
<td>-47.29 dB</td>
<td>-57.5 dB</td>
<td>-59.74 dB</td>
</tr>
<tr>
<td>Power</td>
<td>0.755 mW</td>
<td>1.357 mW</td>
<td>2.811 mW</td>
</tr>
<tr>
<td>Output current Range(without matching)</td>
<td>7.253 ( \mu )A</td>
<td>9.3 ( \mu )A</td>
<td>12.83 ( \mu )A</td>
</tr>
<tr>
<td>Matching</td>
<td></td>
<td></td>
<td>0.75 %</td>
</tr>
</tbody>
</table>
11. Layout

In this chapter a brief look at the lay-outing of the entire chip will be taken. There are a few important layout problems. These problems are:

- Differential pair matching
- Resistor matching
- Dummy structure
- Current density
- Die ratio’s

It is important to keep these problems in mind, because the previous calculated matching errors are based on the fact that these layout techniques are used. By using these techniques the matching cannot be worse as the calculated values. All the above listed problems are discussed in the chapters: 11.1 till 11.6.

11.1. Differential pair matching

By taking a large transistor over a large area of chip, matching problems can be found, due to thermal differences and local variations. For this reason a common centroid technique has been used to match differential pairs as much as possible. This idea has been demonstrated in the figures below.

This has been implemented for all the differential pairs. How this looks like in the OLFAR layout is shown in Figure 134. This technique has the advantage that we use less space since the sources are combined and the drain-to-bulk capacitance is minimized.
11.2. Resistor Matching
For resistor matching the same problem holds. The resistors which have to be matched must be laid next to each other so that the matching error is as small as possible.

What we see in Figure 135 are three resistors which determine the gain of a certain amplifier. These are positioned like this: A A B A C A A. The outer resistors are there as dummy structure, which will be explained in 11.4.
11.3. Current Mirror matching

Also the current mirrors need to be matched. There are two types of current mirrors:

- A one-to-one mirror, usually used above a differential pair
- A one-to-more mirror, usually used for biasing currents

Usual structures for these kinds of mirrors are the ABBA technique, or the BBBABBB technique.

Figure 136 shows us a multiple ABBA structure as has been used for a 1:1 mirror.

Figure 137 is another example of a current mirror of 1 : 100. They are constructed such that they use the least possible area. On the bottom of the figure we see the input transistor, which is situated in the middle of the other transistors.

11.4. Dummy structure

During processing of the chip, some spread of the layers could be found. This can cause discontinuities in the entire design of a structure. To prevent this situation dummies are added. These dummies are
shorted so that they do not influence the circuitry. Again we have two types, one for the transistors and one for the resistors. The case of the resistors is shown below.

Figure 138 shows a resistor dummy example. There are two dummies added at the border of the design, this is done so that the outer resistors have the same shape as the inner resistors. Also for this reason five small resistors are added (shown in the top of the figure) to make all the resistors as large as each other, without getting a different resistance value.

Figure 136 already shows us some dummies for transistors, they are placed at the border of the active transistors and they are also shorted.
11.5. **Current density**

The used metals all have a maximum current density which they can handle. All the lines are chosen such that they can handle the required current. Table 40 shows these current densities for every layer. An example is the V<sub>dd</sub> line where all the currents flow through. For this line metal 4 has been used with a width of 50 µm. In this case this line can handle: 167.5 mA, which is more than enough. Also two V<sub>dd</sub> and V<sub>ss</sub> pads have been used to split the current through these layers.

<table>
<thead>
<tr>
<th>Layer</th>
<th>Maximum current density</th>
</tr>
</thead>
<tbody>
<tr>
<td>Poly1</td>
<td>0.34 mA/µm</td>
</tr>
<tr>
<td>Poly2</td>
<td>0.20 mA/µm</td>
</tr>
<tr>
<td>Met1</td>
<td>0.67 mA/µm</td>
</tr>
<tr>
<td>Met2</td>
<td>0.67 mA/µm</td>
</tr>
<tr>
<td>Met3</td>
<td>0.67 mA/µm</td>
</tr>
<tr>
<td>Met4</td>
<td>3.35 mA/µm</td>
</tr>
</tbody>
</table>

While placing vias, the current density had been taken into account. Multiple vias are placed where more current flows.

11.6. **Die ratio**

The AMS process needs a DIE ratio for almost all layers. For this reason a lot of floating dummies are added. These dummies are not placed above active parts, since they can cause extra capacitances. Appendix F shows us the entire layout for this chip.
12. ESD Protection

For ESD a protection ring has been added. While placing this ring some rules must be followed. These rules are shortly explained in this chapter.

12.1. Types of Pads

There are several types of pads. The pads that are required for this design are the: digital-, analog- and power pads. Between these pads peri-spacers cells are added. These are just connections of the internal nodes of these pads. All these pads have some important properties. First we will take a look at the digital pads.

12.1.1. Digital Pads

These pads are used for all the digital inputs. For all the inputs the ICDP version has been used. This pad is a CMOS Input Buffer with pull down.

12.1.2. Analog Pad

For the analog in- and outputs we used the APRIO1K5P_3B pad. This kind of pad is a protected analog pad which is illustrated in Figure 140. We took for RBLOCK a resistor of 1500 Ω, in that case we are maximal protected for ESD problems. In that case the in- and outputs can handle at least 2 kV as stated by AMS.

12.1.3. Power pads

For the power inputs another type of pad has been used. The AVDDALLP and AGNDALLP pads are used. These are analog power supply pads. They have a very large path from the pad to the circuitry. In this case they can handle a lot of current. Both for $V_{dd}$ and $V_{ss}$ two pads are used, they are placed such that the distance between a $V_{dd}$ and $V_{ss}$ is small from every pad seen. In that case when an ESD problem occurs, the distance which has to be travelled is small and so the resistance is small and thus no large problems are seen. The entire ESD protection ring can be found in Appendix F. The largest resistance between a $V_{dd}$ and $V_{ss}$ is about 0.3 Ω. This is small enough to have no problems with handling some ESD pulses.
13. Recommendations and testing

Testing of the chip is beyond the scope of this thesis, but a test circuitry has been added. All the controls are discussed in this chapter and important situations are highlighted. For the frequency control a shift register has been used (13.1). Also all the separate devices can be tested by using the control circuit (13.2), an example of useful situations are discussed in 13.3. An overview of the chip can be found in 13.4, with pin assignment. Recommendations are done in 13.5.

13.1. Frequency Control

In 6.1.3 it has been explained that the division ratio had to be controlled by a 10 bit SET signal. Since we do not want to use 10 pads for this a control circuitry has been added. This circuitry is shown below:

![Frequency Control Circuit](image1)

A 10 bits shift-register is shown, with a set-circuitry. This set-circuitry is there to prevent that while switching the frequency, this will be directly seen by the frequency divider. A reset has been added to set the output equal to “0000000000”. The inputs are summarized in the table below. A shift-register has been used instead of a frequency divider because in this case it takes less time to set the wanted division ratio.

<table>
<thead>
<tr>
<th>Input</th>
<th>Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>clkFreq</td>
<td>Clock pulse for frequency Control</td>
</tr>
<tr>
<td>setFreq</td>
<td>Sets the output equal to the wanted frequency</td>
</tr>
<tr>
<td>freqInput</td>
<td>Input data to set the division ratio</td>
</tr>
<tr>
<td>resetFreq</td>
<td>Reset the output</td>
</tr>
</tbody>
</table>

![Table 41 - inputs of frequency divider](image2)
13.2. Function Control

The entire chip has a lot of interesting points. To measure a certain point or test a certain device, all the other devices need to be turned off. For this a control circuitry has been added, and a lot of switches are added to measure the points of interest. First the positions of these switches are shown, after that a look at the circuitry which has been used to drive these switches has been reviewed.

13.2.1. Added switches

The figure below shows all the positions of the switches and their numbers. Also the devices are numbered; this is to get a clear overview which data signal influences which part.

Two global lines are added: “inTest” and “outTest”. These lines can be used to put a signal on, or read out a signal. As shown in the figure these lines are connected to the points of interest. All the numbers are related to the outputs of the control circuit: D<0> -> D<19>

13.2.2. Control Circuitry

The control circuitry needs to have 20 data signals as shown in the previous paragraph. For this we made a similar circuit as the frequency control, as can be seen below.
The difference is that when a reset has been given, the data signals are such that the chip is in its ‘on’ situation. Important data signals are discussed in 13.3.

<table>
<thead>
<tr>
<th>Input</th>
<th>Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>set</td>
<td>Set data to output</td>
</tr>
<tr>
<td>reset</td>
<td>Reset the output to ‘on’</td>
</tr>
<tr>
<td>data</td>
<td>Data input</td>
</tr>
<tr>
<td>clk</td>
<td>Clock input to shift data</td>
</tr>
</tbody>
</table>

For the reset a Power-On-Reset has been used. This power-on-reset is a standard block of AMS.

### 13.3. Test examples

For testing it is useful to use the table below, since it defines some data signals which can be used to test several devices. It also gives what kind of signal has to be put on the “inTest” line, and what can be read out on the “outTest” line.

<table>
<thead>
<tr>
<th>Data signal</th>
<th>What to test?</th>
<th>inTest</th>
<th>outTest</th>
</tr>
</thead>
<tbody>
<tr>
<td>“01010000010001111111”</td>
<td>Everything on</td>
<td>nothing</td>
<td>nothing</td>
</tr>
<tr>
<td>“01001000000001110000”</td>
<td>LNA</td>
<td>Pads can be used for input Sinusoidal</td>
<td>Amplified signal</td>
</tr>
<tr>
<td>“01000001000001100010”</td>
<td>PLL</td>
<td>nothing</td>
<td>Block signal with frequency set</td>
</tr>
<tr>
<td>“10000000000001000000”</td>
<td>Voltage Reference</td>
<td>nothing</td>
<td>Voltage of 1.2V</td>
</tr>
<tr>
<td>“00100000001100100000”</td>
<td>Current Reference</td>
<td>1.2V&lt;sub&gt;dc&lt;/sub&gt;</td>
<td>High ohmic load, about 1.5V&lt;sub&gt;dc&lt;/sub&gt;</td>
</tr>
<tr>
<td>“01001100000001101000”</td>
<td>Buffer</td>
<td>Sinusoidal signal with dc offset</td>
<td>Same as input</td>
</tr>
<tr>
<td>“01000000100010110001”</td>
<td>Differential to Single ended</td>
<td>Sinusoidal signal with dc offset</td>
<td>Amplified input signal</td>
</tr>
<tr>
<td>“01000000000001111000”</td>
<td>AGC</td>
<td>Pads can be used for input Sinusoidal</td>
<td>Output pad can be used for output signal</td>
</tr>
</tbody>
</table>
13.4. In- and Outputs of the entire Chip

A clear overview of these pads is shown below.

Table 44 - numbers connected to pins

<table>
<thead>
<tr>
<th>Pad number</th>
<th>Signal</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>VDD</td>
</tr>
<tr>
<td>2</td>
<td>VDD</td>
</tr>
<tr>
<td>3</td>
<td>VSS</td>
</tr>
<tr>
<td>4</td>
<td>VSS</td>
</tr>
<tr>
<td>5</td>
<td>inOverall</td>
</tr>
<tr>
<td>6</td>
<td>inOverall2</td>
</tr>
<tr>
<td>7</td>
<td>Out</td>
</tr>
<tr>
<td>8</td>
<td>outCrFilter_1</td>
</tr>
<tr>
<td>9</td>
<td>outCrFilter_2</td>
</tr>
<tr>
<td>10</td>
<td>LO+40M</td>
</tr>
<tr>
<td>11</td>
<td>LO-40M</td>
</tr>
<tr>
<td>12</td>
<td>25kHz</td>
</tr>
<tr>
<td>13</td>
<td>25kHz_2</td>
</tr>
<tr>
<td>14</td>
<td>inTest</td>
</tr>
<tr>
<td>15</td>
<td>outTest</td>
</tr>
<tr>
<td>16</td>
<td>3_1uCapPLL_1</td>
</tr>
<tr>
<td>17</td>
<td>3_1uCapPLL_2</td>
</tr>
<tr>
<td>18</td>
<td>inCrFilter_1</td>
</tr>
<tr>
<td>19</td>
<td>inCrFilter_2</td>
</tr>
<tr>
<td>20</td>
<td>31uCapPLL</td>
</tr>
<tr>
<td>21</td>
<td>Vtop</td>
</tr>
<tr>
<td>22</td>
<td>Set (Control)</td>
</tr>
<tr>
<td>23</td>
<td>Data (Control)</td>
</tr>
<tr>
<td>24</td>
<td>Clk (Control)</td>
</tr>
<tr>
<td>25</td>
<td>clkFreq</td>
</tr>
<tr>
<td>26</td>
<td>setFreq</td>
</tr>
<tr>
<td>27</td>
<td>freqInput</td>
</tr>
<tr>
<td>28</td>
<td>resetFreq</td>
</tr>
</tbody>
</table>

13.5. Recommendations

The chip needs to be fabricated and tested as is explained before. This testing will give information about each part of the chip, if needed they can be optimized. The chip as constructed above will be for delfi-n3Xt which means there are only two antenna inputs. For the OLFAR project an extra pin needs to be added to provide a three antenna input. Also a 40 kΩ has to be added between this pad and the input of the LNA.
14. References

[1] delfi-n3Xt document, DNx-TUD-TN-0036, 05-09-2008 by M.J. de Milliano, Tu Delft


[3] RADIO NOISE NEAR THE EARTH IN THE 1-30 MHZ FREQUENCY RANGE, 1990, W.C. Erickson, Dept. of Physics and Astronomy, Univ. of Maryland, College Park, MD 20742, pag: 60-69


A. Appendix: OLFAR antenna setup simulation results

Configuration 1:

- Figure A.1 - Impedances for configuration 1
- Figure A.2 - SWR and Reflection Coefficient for configuration 1
- Figure A.3 - Gain for configuration 1, shown in dBi
Configuration 2:
Configuration 3:

Figure A. 9 Impedances for configuration 3

Figure A. 7 SWR and Reflection Coefficient for configuration 2

Figure A. 8 Pattern for configuration 2
figure A. 10 SWR and Reflection Coefficient for configuration 3

figure A. 11 Gain for configuration 3, shown in dBi

figure A. 12 Pattern for configuration 3
Configuration 4:

Figure A. 13 Gain for configuration 4, shown in dBi

Figure A. 14 Impedances for configuration 4

Figure A. 15 SWR and Reflection Coefficient for configuration 4
Configuration 5:

![Diagram of antenna gain and impedances for configuration 5]

**Figure A. 16 Pattern for configuration 4**

**Figure A. 17 Gain for configuration 5, shown in dBi**

**Figure A. 18 Impedances for configuration 5**
Configuration 6:

figure A. 21 Gain for configuration 6, shown in dBi
Appendix: OLFAR antenna setup simulation results

1

5

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figure A. 22 Impedances for configuration 6

figure A. 23 SWR and Reflection Coefficient for configuration 6

figure A. 24 Pattern for configuration 6
Configuration 7:

**figure A. 25 Gain for configuration 7, shown in dBi**

**figure A. 26 Impedances for configuration 7**

**figure A. 27 SWR and Reflection Coefficient for configuration 7**
Figure A. 28 Pattern for configuration 7
### B. Appendix: Files for antenna simulation

**DELFI-N3XT**

<table>
<thead>
<tr>
<th>Global files</th>
<th>comment</th>
</tr>
</thead>
<tbody>
<tr>
<td>Body.pg</td>
<td>Body of delfi-n3xt including solar cells</td>
</tr>
<tr>
<td>Antennas_four.pg</td>
<td>Four voltage sources</td>
</tr>
<tr>
<td>Geom._end.pg</td>
<td>required file for generating nec file</td>
</tr>
<tr>
<td>UHF.pg</td>
<td>required file for generating nec file</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Simulation files</th>
<th>comments</th>
<th>Nec file</th>
</tr>
</thead>
<tbody>
<tr>
<td>DelfiOLFARVHFantenna514cm.pg</td>
<td>Antenna length 51.4cm</td>
<td>Delfiolfar514cm.nec</td>
</tr>
</tbody>
</table>

**OLFAR**

<table>
<thead>
<tr>
<th>Global files</th>
<th>comment</th>
</tr>
</thead>
<tbody>
<tr>
<td>BodyOLFAR.pg</td>
<td>Body of a cube sat (10x10x10) including solar cells</td>
</tr>
<tr>
<td>Antennas_four.pg</td>
<td>Four voltage sources</td>
</tr>
<tr>
<td>Antennas_tripole.pg</td>
<td>Three voltage sources for tripole simulations</td>
</tr>
<tr>
<td>Geom._end.pg</td>
<td>required file for generating nec file</td>
</tr>
<tr>
<td>UHF.pg</td>
<td>required file for generating nec file</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Simulation files</th>
<th>comments</th>
<th>Nec file</th>
</tr>
</thead>
<tbody>
<tr>
<td>OLFARvhfantennaTRIPOLE.pg</td>
<td>Tripole antenna</td>
<td>Olfartripole.nec</td>
</tr>
<tr>
<td>OLFARvhfantennaTRIPOLEflat.pg</td>
<td>Flat tripole antenna</td>
<td>Olfarvhftripoleflat.nec</td>
</tr>
<tr>
<td>OLFARvhfantennaTRIPOLEstick.pg</td>
<td>Tripole antenna with stick</td>
<td>Olfarsticktripole.nec</td>
</tr>
<tr>
<td>OLFARvhfantennaTurnstile.pg</td>
<td>Turnstile antenna</td>
<td>OLFARvhfTurnstile.nec</td>
</tr>
<tr>
<td>OLFARvhfantennaTurnstileflat.pg</td>
<td>Turnstile flat</td>
<td>OLFARturnstileflat.nec</td>
</tr>
<tr>
<td>OLFARvhfantennaTurnstileCenter.pg</td>
<td>Turnstile at center</td>
<td>OLFARturnstileCenter.nec</td>
</tr>
<tr>
<td>OLFARvhfantennaTRIPOLEedge.pg</td>
<td>Tripole at edge</td>
<td>OLFAREdge.nec</td>
</tr>
<tr>
<td>OUTPUT FILES</td>
<td>Description</td>
<td></td>
</tr>
<tr>
<td>----------------------------------------------------------------------------</td>
<td>-------------------------------------------------------</td>
<td></td>
</tr>
<tr>
<td>Delfiolfarvhfantenna514cm.out</td>
<td>Delfi-n3xt 51.4cm antenna</td>
<td></td>
</tr>
<tr>
<td>OLFARstickTRIPOLE.out</td>
<td>Olfar with tripole antenna on stick</td>
<td></td>
</tr>
<tr>
<td>OLFARTRIPOLE.out</td>
<td>Olfar with tripole antenna</td>
<td></td>
</tr>
<tr>
<td>OLFARTRIPOLEflat.out</td>
<td>Olfar with flat tripole antenna</td>
<td></td>
</tr>
<tr>
<td>OLFARTURNSTILE.out</td>
<td>Olfar with turnstile antenna</td>
<td></td>
</tr>
<tr>
<td>OLFARturnstileCenter.out</td>
<td>Olfar turnstile antenna at center</td>
<td></td>
</tr>
<tr>
<td>OLFARTurnstileFlat.out</td>
<td>Olfar turnstile flat at center</td>
<td></td>
</tr>
<tr>
<td>OLFARTRIPOLEedge.out</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
C. Appendix: Antenna Parameters

In this Appendix we will explain some parameters which are important to characterize antennas.

C.1. Reflection Coefficient

Due to no impedance matching some reflection can occur. This means that a part of the signal is reflected back into the signal line. This signal line has characteristic impedance called: $Z_0$. The impedance of the load is defined by $Z_L$. When the reflection of an antenna is measured, this is done by knowing it is connected to a 50Ω environment. The reflection coefficient is given by:

$$\Gamma = \frac{V_{0-}}{V_{0+}} = \frac{(Z_L-Z_0)}{(Z_L+Z_0)}$$

In which $V_{0-}$ is the wave going back from the load, and $V_{0+}$ is the incident wave going to the load.

C.2. Standing Wave Ratio

The standing wave ratio is defined as the ratio of $V_{\text{max}}$ to $V_{\text{min}}$, so it is a measure of the mismatch of a line. It is known that when the reflection coefficient increases, the SWR increases too. The ratio can be defined as:

$$\text{SWR} = \frac{V_{\text{max}}}{V_{\text{min}}} = \frac{(1 + |\Gamma|)}{(1 - |\Gamma|)}$$

C.3. Scattering-Parameters

$S$-parameters do not use open or short circuit conditions to characterize a linear electrical network; instead matched and unmatched loads are used. These terminations are much easier to use at high signal frequencies than open-circuit and short-circuit terminations. Moreover, the quantities are measured in terms of power.

$$S_{11} = \frac{b_1}{a_1} = \frac{V_1^-}{V_1^+} \text{ and } S_{21} = \frac{b_2}{a_1} = \frac{V_2^-}{V_1^+}$$

$$S_{12} = \frac{b_1}{a_2} = \frac{V_1^-}{V_2^+} \text{ and } S_{22} = \frac{b_2}{a_2} = \frac{V_2^-}{V_2^+}$$

C.4. Insertion Loss

Insertion Loss (IL), usually also represented in dB, is given by:

$$\text{IL} = -10 \log_{10} \frac{|S_{21}|^2}{1 - |S_{11}|^2}$$
Since insertion loss is, by definition, a loss, the leading negative sign is often neglected. Insertion loss is not a function of the input or source impedances. This can be further expressed as:

\[ IL = \frac{P_{out}}{P_{in}} \]

where \( P_{in} \) is the power that makes it into port 1 of the network.

C.5. Input return loss
Input return loss (\( RL_{in} \)) is a scalar measure of how close the actual input impedance of the network is to the nominal system impedance value and, expressed in logarithmic magnitude, is given by:

\[ RL_{in} = 20 \log_{10} |S_{11}| \ [dB] \]

By definition, return loss is a positive scalar quantity implying the 2 pairs of magnitude (|) symbols. The linear part, \( |S_{11}| \) is equivalent to the reflected voltage magnitude divided by the incident voltage magnitude.

C.6. Z-Parameters
The Z-parameter matrix for the two-port network is probably the most common. In this case the relationship between the input currents, output voltages and the Z-parameter matrix is given by:

\[
\begin{pmatrix}
V_1 \\
V_2
\end{pmatrix} =
\begin{pmatrix}
Z_{11} & Z_{12} \\
Z_{21} & Z_{22}
\end{pmatrix}
\begin{pmatrix}
I_1 \\
I_2
\end{pmatrix}
\]

Where

\[
Z_{11} = \frac{V_1}{I_1} \bigg|_{I_2=0} \quad \text{and} \quad Z_{12} = \frac{V_1}{I_2} \bigg|_{I_1=0}
\]

\[
Z_{21} = \frac{V_2}{I_1} \bigg|_{I_2=0} \quad \text{and} \quad Z_{22} = \frac{V_2}{I_2} \bigg|_{I_1=0}
\]

C.7. Polarization
Electromagnetic waves can have several kinds of polarization. These are given in figure C.144. It is preferred to receive as much kinds of polarization as possible. There are two types of circular polarization, left-handed (LHCP) and right-handed (RHCP). It is preferred to get a high as possible gain for both types of circular polarization. For this we use multiple antennas, like the turnstile or the tripole antennas.
C.8. Omni-directionality
An omni-directional antenna is an antenna system which radiates power uniformly in one plane with a directive pattern shape in a perpendicular plane. This pattern is often described as "donut shaped". For OLFAR this is preferred, since we do not want any direction selectivity, because the satellite cannot stay at one position. This direction selectivity will be retrieved after correlating the signals.

C.9. F/B ratio
The F/B ratio is the power ratio (in dB) between the power transmitted in (or received from) the favored direction (front) of an antenna compared to the power transmitted in (or received from) the back of the antenna. A vertical good directional antenna will have an F/B ratio of 30 dB or more.
D. Small signal parameters differential stage

Figure D.1 shows us a differential stage. For this we can make the following equations: with \( +V_{in} = +0.5V_{in} \), \( -V_{in} = -0.5V_{in} \). In that case we can see:

\[
I_{out} = I_{Q3} - I_{Q4}
\]

With the inputs of above we see:

\[
I_{Q3} = +0.5g_mV_{in} \quad \text{and} \quad I_{Q4} = -0.5g_mV_{in}
\]

\[
I_{out} = g_mV_{in}
\]

Thus when assuming Q1 and Q2 to be biased exactly the same we would see just 1 equal \( g_m \) at the output. If we take a look at the small signal circuit (for now letting the current mirror out) we see the following:

We can make this simplification because: for the case that both base currents are equal in the differential pair, no current flows through the branch in the middle of the left figure. So, it can be removed from the diagram. The circuit that remains is easily reduced to the diagram at the right side. Thus we see series combinations of the \( C_{gs} \) and \( r_{ds} \).

From this we can conclude:

\[
C_{gs,eq} = \frac{C_{gs1} \cdot C_{gs2}}{C_{gs1} + C_{gs2}} = \frac{C_{gs}}{2} \quad \text{(assumed equal biasing and thus} \ C_{gs1}=C_{gs2})
\]

\[
r_{ds,eq} = r_{ds1} + r_{ds2} = 2 \cdot r_{ds1} \quad \text{(assumed equal biasing and thus} \ r_{ds1}=r_{ds2})
\]

\[
g_{m,eq} = \frac{g_m}{2}
\]
The matching of transistor parameters between two identically designed devices are described by the Pelgrom model [ref]. This states that the variance of a parameter $P$ consists of a term inversely proportional to the area of the devices and a term proportional to the square of the distance between them.

$$\sigma^2 \sim \frac{A_P}{WL} + S_P D_x^2$$

In which $A_P$ is an empirically determined constant specific to the parameter in question, $WL$ is the area of the device, $S_P$ is an empirically determined constant that describes the mismatch as a function of the distance between two devices, and $D_x$ is the distance between the devices. For closely spaced devices this simplifies to

$$\sigma^2 \sim \frac{A_P}{WL}$$

which are used in the austria microsystems design manual, i.e. the parameter $S_P$ is not given and devices to be matched are expected to be located closely together. For MOS devices, the constants $A_P$ are given for the threshold voltage $V_{th}$ and for the current gain factor $k$. These values are shown in Table E.1.

In designing a circuit however, these values are not directly useable. As shown in [Hastings], circuits can be optimized for either precisely matched gate-source voltages, or precisely matched drain currents.

The difference in gate-source voltage between two transistors is given by

$$\Delta V_{gs} = \Delta V_{th} - \frac{1}{2} V_{gs} \left( \frac{\Delta k}{k} \right)$$

If the variances of $V_{th}$ and $k$ are known, then it is possible to find the variance of $\Delta V_{gs}$ from

$$\sigma^2 \sim \sigma^2 \sim \sigma^2 \sim + \frac{1}{4} V_{gs}^2 \cdot \sigma^2 \left( \frac{\Delta k}{k} \right)$$

Because both $\sigma^2 \sim$ and $\sigma^2 \left( \frac{\Delta k}{k} \right)$ are of the form $\frac{A_P^2}{WL}$, also $\sigma^2 \sim$ can be written in this form, and we can therefore define a constant $A_{V_{gs}}$ equal to

$$A_{V_{gs}}^2 = A_{V_{th}}^2 + \frac{1}{4} V_{gs}^2 \cdot A_k^2$$

Similarly, if the drain currents are to be matched, then we can use the equation
\[
\frac{I_{D1}}{I_{D2}} = k_2 \left( 1 + \frac{2\Delta V_{th}}{V_{gt}} \right)
\]

Which can be written as

\[
\frac{\Delta I_D}{I_{D1}} = \left( \frac{\Delta k}{k_1} + 1 \right) \left( 1 + \frac{2\Delta V_{th}}{V_{gt}} \right) - 1 = \frac{\Delta k}{k_1} + \left( \frac{\Delta k}{k_1} \frac{2\Delta V_{th}}{V_{gt}} \right) + \frac{2\Delta V_{th}}{V_{gt}}
\]

so that

\[
\sigma^2 \left( \frac{\Delta I_D}{I_{D1}} \right) = \sigma^2 \left( \frac{\Delta k}{k_1} \right) + \sigma^2 \left( \frac{\Delta k}{k_1} \frac{2\Delta V_{th}}{V_{gt}} \right) + 4 \frac{\Delta V_{th}}{V_{gt}} \sigma^2 \Delta V_{th}
\]

However, in this equation there is a term that cannot directly be derived from the two known parameters. If we assume this term to be negligible, we end up with an expression for \( A_{I_o} \) that looks very similar to (5).

\[
A_{I_o}^2 = A_k^2 + 4 \frac{\Delta V_{th}}{V_{gt}} \cdot A_{V_{th}}^2
\]

If we compare (5) and (9), we find that for good voltage matching \( V_{gt} \) should be small, while for good current matching \( V_{gt} \) should be large. From (2) it is clear that in either case the gate area should be large for good matching (and that the transistors should be close together).

When designing a differential amplifier, it therefore makes sense to use transistors with a large \( W/L \) ratio, because these have a lower \( V_{gt} \) than transistors with a small \( W/L \) biased at the same drain current. There is however a practical limit, following from (5), at which reducing \( V_{gt} \) provides little additional benefit: if the term containing \( V_{gt} \) becomes much smaller than \( 2 \Delta V_{th} \), then it makes no sense to reduce \( V_{gt} \) any further.

Conversely, when designing a current mirror, it is better to use transistors with a small \( W/L \), to ensure a relatively large \( V_{gt} \). Because the second term in (9) becomes negligible only for very large voltages, it is advisable to design current mirrors with as high a \( V_{gt} \) as possible. Table E.1 contains \( A_{id} \) for two values of \( V_{gt} \).

<table>
<thead>
<tr>
<th>Device</th>
<th>( A_{V_{th}} ) (mV( \mu )m)</th>
<th>( A_k ) (%( \mu )m)</th>
<th>( A_{V_{th}} ) (mV( \mu )m) @ ( V_{gt} = 0.4 ) V</th>
<th>( A_{id} ) (%( \mu )m) @ ( V_{gt} = 0.5 ) V</th>
<th>( A_{id} ) (%( \mu )m) @ ( V_{gt} = 1.0 ) V</th>
</tr>
</thead>
<tbody>
<tr>
<td>NMOS4</td>
<td>9.5</td>
<td>0.7</td>
<td>9.6</td>
<td>3.86</td>
<td>2.02</td>
</tr>
<tr>
<td>PMOS4</td>
<td>14.5</td>
<td>1.0</td>
<td>14.6</td>
<td>5.89</td>
<td>3.07</td>
</tr>
</tbody>
</table>
F. Entire Layout
G. Circuits
<table>
<thead>
<tr>
<th>Field</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Work No.</td>
<td>569 21 153.24 2000</td>
</tr>
<tr>
<td>Model</td>
<td>H8524+</td>
</tr>
<tr>
<td>Output</td>
<td>RX</td>
</tr>
<tr>
<td>Receiver</td>
<td>OLFAR</td>
</tr>
</tbody>
</table>

**Diagram:**

A detailed schematic diagram of the OLFAR receiver is shown, illustrating various components and connections. The diagram includes labels for each part, indicating its function and position within the circuit. The layout is complex, with multiple paths and nodes connecting different circuit elements.

**Text:**

OLFAR: A Low Frequency Receiver by Edwin Wiek
Chapter: Circuits
OLFAR: A Low Frequency Receiver by Edwin Wiek
OLFAR: A Low Frequency Receiver by Edwin Wiek
Control
H. Pole Simulation

H.1. Poles simulation

For simulating the pole positions LINDA has been used. The table below shows the parameters which are used for calculating the pole positions of the LNA.

<table>
<thead>
<tr>
<th>table H.1 - small signal parameters</th>
</tr>
</thead>
<tbody>
<tr>
<td>Stage 1</td>
</tr>
<tr>
<td>C\textsubscript{gs}</td>
</tr>
<tr>
<td>C\textsubscript{gd}</td>
</tr>
<tr>
<td>g\textsubscript{m}</td>
</tr>
<tr>
<td>r\textsubscript{ds}</td>
</tr>
</tbody>
</table>

![Figure H.1 - bode-plot of the LNA](image)

Figure H.1 shows the root-locus of this LNA. What can be found is that the system is unstable, since the poles are moving to the right half plane. The pole on the left is caused by the load capacitance, and is shown to be non-dominant.

![Figure H.2 - root locus of the LNA](image)
H.2. Improving LNA
Also the improvement of the LNA will be done by a structured method. The following steps will be taken:

- Stabilize the system, by using pole splitting
- Stabilize the system, by using a phantom zero

H.2.1. Stabilizing the system
To prevent the poles going to the right half plane we can use the technique of adding a phantom zero. This is a zero which is visible in the loop of the system, but not in the system transfer. To realize a phantom zero in the feedback network, the feedback network has to introduce a reasonable reduction of the loop-gain, which is the case in this design. As the feedback is realized with accurate components, frequency compensation using a phantom zero is often more accurate to design than the other methods (like pole/zero cancellation). More about phantom zeros can be found in [4]11. It seems that the poles are too close to each other to get the system stable in an easy way. When we took $C_{\text{phantom}}$ too large the poles seems to go in a same way to the right half plane, and when taking $C_{\text{phantom}}$ too small the poles seem to have a bended way to the right half plane. Thus we need to do an additional step to get those poles away from each other. This can be done by pole splitting, which can be done by adding a capacitor across the gate-drain of the second stage (at the output because the local feedback causes the output impedance of the transistor to lower and the output pole shifts). The results of adding a capacitor across the gate-drain shows the following result. $C_{\text{split}}$ equals 20fF.

---

We can see that the poles have been split up, but the root-locus is still heading for the right half plane. In reality we can put this capacitance between the input of the differential stage and his output because that gives us the desired effect for the entire amplifier. We have to solve this, which can be done by a phantom zero as told before. $C_{\text{phantom}}$ equals 30fF.

![Figure H.4 – bode-plot of LNA including phantom zero](image)

![Figure H.5 - root-locus of LNA including phantom zero](image)

Above we see that the root-locus is now bending to the left, and thus the system can be assumed stable.
I. Noise calculations input stage LNA

To do the noise calculation of the LNA a lot of steps need to be taken. These are done and illustrated below. The input is a parallel combination, thus an equivalent of these could be taken, thus $R_4 = R_1//R_2$, and $Z_s = Z_{s1}//Z_{s2}$. These first order approximations will be enough to determine the input stage.

Figure I.1 is a noise model of the entire design. We can see a noise voltage source of $R_4$ ($V_{n,R4}$) and of the LNA ($V_n$), and we see the noise current sources of $R_3$ ($I_{n,R3}$) and one of the LNA ($I_n$). All of these sources are shifted to the antenna, so that the equivalent input noise could be calculated. These shifts are shown in the figures below.

\[ I_{nR3} = I_{nR3} + \frac{V_n}{R3} \]
What has not determined yet are the noise sources $I_n$ and $V_n$. For these sources we have to take a closer look at the first stage of the LNA. These calculations are done below.

Thus: 

$$V_{\text{neq}} = V_{nR4} + I_n * R_4 - V_n - I_{nR3} * R_4 - \frac{V_n * R_4}{R_3}$$

In which:
This gives us for \( V_n \) and \( I_n \) the following:

\[
V_n = -V_{ng} + \left[ \frac{1}{g_m} - \frac{j2\pi f R_g (C_{gs} + C_{gd})}{g_m} \right] (I_d + I_{df})
\]

\[
I_n = -\frac{j2\pi f (C_{gs} + C_{gd})}{g_m} (I_d + I_{df})
\]

If we fill this in, we get a total noise at the antenna equal to:

\[
V_{\text{neq}} = V_{nr4} - \frac{j2\pi f R_4 (C_{gs} + C_{gd})}{g_m} (I_d + I_{df}) + V_{ng} - \left[ \frac{1}{g_m} - \frac{j2\pi f R_g (C_{gs} + C_{gd})}{g_m} \right] (I_d + I_{df})
\]

\[
- I_{n,R3} * R_4 + \left( \frac{R_4}{R_3} \right) V_{ng} - \left( \frac{R_4}{R_3} \right) \frac{1}{g_m} - \frac{j2\pi f R_g (C_{gs} + C_{gd})}{g_m} (I_d + I_{df})
\]

And thus an equal noise voltage power:

\[
S_{Vn,eq} = S_{v,n,R4} + \left( 1 + \frac{R_4}{R_3} \right)^2 S_{v,n,g} + S_{I,n,R3} * R_4
\]

\[
+ \left[ \left( R_g + R_4 + \frac{R_4}{R_3} R_g \right)^2 \frac{2\pi f^2 (C_{gs} + C_{gd})^2}{g_m^2} + \left( 1 + \frac{R_4}{R_3} \right)^2 \frac{1}{g_m^2} \right] (S_{I_d} + S_{I_{df}})
\]

With:

\[
g_m = \sqrt{\frac{2\mu C_{ox} W L}{l}}
\]

\[
S_{I_{df}} = \frac{1}{g_m} KF \cdot \frac{I_d}{f} \quad S_{I_d} = \frac{8kT}{3} g_m \quad S_{v,n,R4} = 4kT R_4 \quad \text{and} \quad S_{I,n,R3} = \frac{4kT}{R_3}
\]

In this formula \( KF, AF, C_{ox}, C_{gd} \) and \( C_{gs} \) are given by the process. With these equations an optimization can be made. If the values of above are filled in and assuming \( R_4 = 40 \, \text{k}\Omega \):
This formula is dependent on $I_d$, $L$, $W$ and $f$. Which are the parameters which have to be designed by us, we will first start optimizing $I_d$.

$$S_{vneq} = 8.288 \times 10^{-20} + \frac{1.17 \times 10^{-19}L}{W} + \left( \frac{6.66 \times 10^{-15}}{I_d} \left( \frac{1407}{200} \frac{L}{W} + 5 \right)^2 f^2 W L + \frac{2958.4 L}{W I_d} \right) \left( 2.04 \times 10^{-22} \right) \left( \frac{W I_d}{L} + \frac{K F R^4}{L^2 f} \right) \left[ \frac{V^2}{Hz} \right]$$

Figure I.10 – noise $[V^2/Hz]$ depending of $I_d$ at 30kHz

Figure I.10 gives us the noise depending on $I_d$. In this figure $W=100 \ \mu m$, $L=10 \ \mu m$ and $R=40000$. We can see that the noise is increasing with increasing $I_d$. Two cases should be considered: the noise at low frequencies ($\approx 30 \ kHz$) and the noise at higher frequencies ($\approx 30 \ MHz$). In the case of low frequencies the noise is mostly caused by flicker noise, for high frequencies the noise is mostly caused by shot-noise. The figure below illustrates this phenomenon, for this reason it has been chosen to optimize for low frequencies.

Figure I.11 - noise $[V^2/Hz]$ as function of the frequency

---

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To confirm our model we have plotted also the noise as function of frequency and compared it to Figure I.11. Figure shows the results; they seem to have the same shape.

![Figure I.12 – noise [V^2/Hz] as function of the frequency, Id =100 µA, L=10 µm, W=100 µm](image)

Conclusion is that a drain current of 100 µA will give optimal noise results. The next step to take is to optimize W and L. What must be considered is that in an earlier stage we did not consider R_s and C_p, this is because of the fact that their contributions are negligible in the first order approximation. From now we have included them, to get a complete as possible first order approximation.

![Figure I.13 – noise [V^2/Hz] as function of W and L @ 30 kHz](image)

Figure I.13 is a 3D plot of the noise as a function of W and L @ 30 kHz. What we see, is that L should not be too small. (Figure)
Figure I.14 – noise \([V^2/\text{Hz}]\) as function of \(L\) @ 30 kHz, \(W=100 \, \mu\text{m}\)

Figure shows that from \(L = 3 \, \mu\text{m}\) there is no significant difference in noise. We have plotted the same figure at higher frequencies, to study its behavior at 3 MHz (Figure ). What we see is that in that case the optimum is around 1 \(\mu\text{m}\), but in that case the noise is even smaller as for the lower frequencies, as explained before. Thus we will take 3 \(\mu\text{m}\), to get an optimization for both frequencies and not to get an useless large transistor.

Figure I.15 – noise \([V^2/\text{Hz}]\) as a function of \(L\) @ 3 MHz, \(W=100 \, \mu\text{m}\)

The only thing left for now is to determine \(W\):

Figure is the same plot as Figure I.13, but this time on a higher frequency. If we take a closer look at \(W\) (Figure ) we can see that we have to take \(W\) as large as possible. This is what we concluded before, so it is plausible for both low and high frequencies.
We will take $W$ equal to 10 $\mu$m, since the scale of figure 180 is quite small. The following results of these calculations can be obtained:

- $W = 10 \mu$m
- $L = 3 \mu$m
- $I_d = 100 \mu$A