Modelling of RF High Power Bipolar Transistors

Koen Mouthaan
Stellingen
behorende bij het proefschrift
"Modelling of RF High Power Bipolar Transistors"
K. Mouthaan, Delft, 22 januari 2001

1. Voor het ontwikkelen van nieuwe RF vermogenstransistoren met hogere vermogensdichtheden zijn nieuwe technieken nodig om de warmte af te voeren.

For realisation of new RF power transistors with higher power densities, new techniques are required for the removal of heat.

2. Het accuraat meten van de temperatuurverdeling in en rond de pn-overgangen van een RF vermogenstransistor is niet mogelijk.

The accurate measurement of the temperature distribution in and around the junctions of a RF power transistor is impossible.

3. Vaak worden verkeerde conclusies getrokken over de kwaliteit van electromagnetische programma's, zoals HFSS, door onoordeelkundig gebruik van deze programma's.

Incorrect conclusions are often drawn about the quality of electromagnetic software packages, like HFSS, due to injudicious use of these packages.

4. Door culturele vervlakking gaat het geluid van folklore verloren.

The sound of folklore is being lost due to cultural indifference.

http://www.si.edu

5. Internationale klimaatconferenties blijven mislukken totdat het water aan de lippen staat.

International Climate Conferences continue to fail until we are up to our neck in water.
6. De Nederlandse architectuur vertoont steeds meer gaten.

Dutch architecture is more and more concerned with emptiness.

7. De toenemende snelheid van processoren voor computers verdoezelt de kwaliteit van bepaalde besturingssystemen.

The increasing speed of computer processors obscures the quality of certain operating systems.

8. De Nederlandse Spoorwegen zijn het spoor bijster.

Dutch Railways have lost their way.


Similarities between proposition and reality are most often accidental.
Modelling of RF High Power Bipolar Transistors

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Modelling of RF High Power Bipolar Transistors

Proefschrift

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door Koenraad MOUTHAAAN

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Preface

This thesis describes work performed in the Microwave Components Group at the Delft University of Technology from 1993 to 1999. The subject of the work is the modelling and measurement of RF high power bipolar transistors.

In 1993 extensive discussions with the discrete semiconductor group of Philips Semiconductors led to the definition of a PhD research project in the area of modelling and measurement of RF power transistors. Philips Semiconductors provided the start up funding for the project and additional funding for measurement gear. The Dutch Technology Foundation (STW) funded the project starting in November 1993. Hewlett-Packard (now Agilent Technologies) provided significant financial support as well.

Koen Mouthaan joined the project in August 1993 after performing a feasibility study at Philips Semiconductors. His work focussed on the compact electrical and thermal modelling of RF power transistors.

Roberto Tinti, a second PhD student joined the team in January 1995. His main focus has been on the isothermal and non-isothermal characterisation of RF power transistors. The combined efforts of Mouthaan and Tinti resulted in an experimentally verified, accurate, predictive electro-thermal model for RF bipolar power transistors.

In chapter 5 the final results of this combined work are presented in brief. A more detailed discussion of these results and on the characterisation of power transistors will be given in Roberto Tinti’s thesis, which is to appear in the near future.
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## 3 Electrical modelling of bondwires, matching capacitors and packages

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## 4 Electro-thermal modelling and measurement

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## 5 Modelling and measurement of RF high power bipolar transistors

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Chapter 1

Introduction

1.1 RF high power amplifiers

Wireless communication has emerged as a mass communication medium and is growing rapidly. The combination of new services, advanced technologies and free market price competition has made wireless communication attractive for virtually everyone. Wireless communication is in essence the bidirectional link between a mobile telephone on one hand and a base station on the other. Common frequency bands used for wireless communication are around 900 Mhz and 1800 MHz which will in the context of this thesis be referred to as radio frequencies (RF). Older communication systems operate at lower frequencies such as 450 MHz. A mobile telephone consists of a transmitter to send signals to the base station and a receiver to receive signals from the base station. An example of a mobile telephone is displayed in figure 1.1. Additional circuitry processes the received signals and the information to be sent to the base station. The base station also has a transmitter and a receiver and is in general connected to the wired telephone network. It is also possible that the base station uses a microwave radio link to connect to another station. A photo of the antenna of a base station is shown in figure 1.1 on the right.

Consider the signal transmitted by the mobile telephone. To ensure the quality of the signal received by the base station, various measures are taken: the output power of the mobile phone is made sufficiently high, the antenna of the base station is located at an elevated position and low noise receivers are used in the base station. Next consider the signal transmitted by the base station which is received by the mobile telephone. To ensure a good connection again several measures are taken: the antenna of the base station is positioned at a high and line-of-sight location, the output power of the base station is high and the sensitivity of the receiver in the mobile phone is chosen appropriately. Additionally, sophisticated methods of digital transmission and reception increase the quality of the connection. It is noted that for the mobile telephone, which is produced in high volumes, several trade-offs must be made. A high transmitted power consumes considerable battery power and a high quality receiver introduces high costs. For the base stations high power is achieved using high power amplifiers (HPA). The subject of this thesis is the modelling of a part of the power amplifiers: the RF high power transistors. The transistors are used to amplify the RF signals to power levels of a few Watts or more. A schematic of a single stage power amplifier is shown in figure 1.2.
1.2 RF high power bipolar transistors

Roughly speaking, RF high power transistors are devices designed to amplify RF signals to high powers. The terms "low power", "medium power" and "high power" are loosely used and depend on frequency, technology and application. Normally "low power" indicates output power levels up to a few hundred milliWatts, "medium power" indicates levels up to a few Watts and "high power" refers to power levels above a few Watts. In the context of base sta-
tion amplifiers "low power" refers to levels of a few Watts, "medium power" indicates levels of tens of Watts and "high power" means levels in the range of one hundred Watts or more. Throughout this work a power level of 10 Watts is considered "high power". Because this work concentrates on high power transistors sometimes the words "high" or "high power" are omitted.

RF power transistors are manufactured for different applications and different types of operation. Presently a number of companies produce power transistors in high volumes such as Motorola, Philips, Ericsson, NEC and Mitsubishi. Different materials exist for power transistors such as silicon (Si), silicon germanium (SiGe), silicon carbide (SiC), gallium arsenide (GaAs). In these materials different types of transistors can be made. Well known types in silicon are the Bipolar Junction Transistors (BJT), the Metal Oxide Semiconductor Field Effect Transistor (MOSFET), the Laterally Diffused MOS (LDMOS) transistor. In GaAs well known types are the High Electron Mobility Transistor (HEMT), Metal Semiconductor FET (MESFET) and Heterojunction Bipolar Transistor (HBT). Although this thesis deals with silicon bipolar transistors, the modelling methods can also be applied to modelling of power transistors using other materials and other devices. As an example Motorola's ultra high frequency (UHF) MOSFET power transistor MRF 166W is shown in figure 1.3 on the left. This power transistor is used in power amplifiers in the range of 30-512 MHz with a typical output power of 40 Watts. In the photo the packaged power transistors are visible showing the white cap with "MRF 166W" printed on it, four leads and the mounting base. Normally the mounting base of a power transistor is firmly attached to a cooling block. The leads are soldered to the input and output printed circuit boards. In the same figure a photograph of Ericsson’s LDMOS power transistor PTF 10031 is shown. The PTF 10031 transistor is able to deliver 50 Watts at a frequency of 1 GHz. In this photo once again the white cap, the mounting base with two holes and two leads are visible. The size of these transistors is in the order of a few centimeters.

Figure 1.3: Examples of power transistors. On the left Motorola’s UHF power transistor MRF 166W (MOSFET) and on the right Ericsson’s PTF 10031 LDMOS transistor is shown.

In general a power transistor contains four types of components. Although the silicon bipolar power transistor will be considered in-depth, the four components are also found in other types of power transistors. Photos of these internals of a specific transistor are shown in the
following chapter in figure 2.2.

- The transistor die. The die is the part of the power transistor where the amplification takes place. The die consists of a block of silicon with a number of active areas at the top. These active areas are also referred to as active cells. The actual amplification of the power transistor is in these active areas. Throughout this thesis silicon bipolar technology is considered for the die. In this particular case each cell consists of an interdigitated structure of base and emitter fingers. The bipolar junctions are located less than a micrometer under the emitter fingers. Emitter and base bondpads are located between the active areas. The collector is on the bottom of the die and is directly connected to the package. It is noted that in the literature the term "transistor", "intrinsic transistor", "device" or "chip" may be used to indicate the "die" or "transistor die". In power transistors of up to a few Watts normally one die is used, in transistors for higher powers multiple dies are found. Device technologists constantly improve and optimize the performance of the die by changing doping profiles and geometries of the die.

- The matching capacitor. Normally the matching capacitor consists of a highly conducting block of silicon. On the top surface two different metallic contacts are formed. The first contact has a thin oxide layer between the metal and the silicon forming a MOS capacitor. The second contact is a metal strip directly attached to the silicon forming an ohmic contact. The prematch capacitor has been introduced to match the low impedance of the die to a somewhat higher impedance at the input of the transistor. Similarly the postmatch capacitor has been introduced to transform the output impedance of a power transistor to a higher impedance. This matching is achieved by using the combination of the inductive behaviour of the bondwires in combination with the capacitor. The ohmic contact serves as an electrical path to the package for current flowing from the die through the bondwires.

- The bondwires. Bondwires are wires with a diameter in the order of 25-50 μm. The wires interconnect the die, the prematch capacitor and the package. Furthermore, they also provide matching of the low input impedance of the die to a higher impedance at the input of the power transistor.

- The package. The main function of the package is to provide a good, reproducible and solderable interface to the relatively small internal components. Additionally, the package protects the internal components. The die and prematch capacitor are attached to the package and bondwires are placed to interconnect the components. The package itself consists of a metal block (the mounting base) with a ceramic substrate attached to it. On top of the ceramic substrate a leadframe is placed. Components are attached to the leadframe and a ceramic or metallic cap is placed on top of the package to protect the components. In figure 1.3 the white caps are easily visible with the manufacturers partnumbers printed on them. In both photos the mounting base and the leads are also visible.

As an example, an internal view of the Ericsson PTB 20105 transistor is shown in figure 1.4. This transistor is capable of delivering 20 Watts in the 925-960 MHz frequency range. The prematch capacitor and two dies are visible in the SEM photo as well as the leadframe and bondwires.

As another example the top view of the Philips BLV 950 bipolar high power transistor is shown in figure 1.5. On the lower side two base leads are shown and on the upper side two collector leads are visible, the emitter being connected to the mounting base. The heart of the
transistor consists of six dies. Twelve capacitors are used at the input and four at the output to transform the low input and output impedance respectively of the dies to higher impedance levels at the leads of the transistor. The transistor can deliver 150 Watts of output power and is used in base station transmitters in the 800 to 960 MHz range. For reasons of clarity the steps in building up a power transistor are roughly shown in figure 1.6.

The first part of the package is the mounting base shown in (a): a brick shaped block of metal with two mounting holes in it. Using screws through these holes the power transistor is firmly attached to a cooling block. Next a ceramic is attached to the mounting base (b). The purpose of the ceramic is to provide electrical isolation between the mounting base and the circuitry on top of the ceramic. A prerequisite of the ceramic is a good thermal conductivity thus providing a good heat flow from the die to the mounting base. A thin metallisation pattern can be present on the ceramic with a typical thickness in the order of 10 μm. Next a leadframe is attached to the ceramic as shown in (c). The leadframe provides the required interconnections and isolations between the leads. The prematch capacitor and a die are placed on top of the leadframe as shown in (d). In larger transistors multiple capacitors and dies are placed. Using bondwires the prematch capacitor, the die and the package are interconnected as shown in (e). Finally a ceramic cap is placed over the components protecting the bondwires, die and prematch capacitor as shown in (f).

The (external) leads of silicon bipolar power transistor are usually termed "emitter", "col-
lector" or "base" depending on their internal association with the emitter, collector and base respectively of the die. Using these names for the die and for the external leads may confuse the reader. In this thesis it should be clear from the context whether the external leads or the die is being considered. Whenever there is a chance of confusion "external emitter" refers to the emitter lead and "internal emitter" refers to the emitter of the die. This convention is also used for the base and collector.

In practice, designs of a power transistor are not started from scratch. Instead, variation to proven designs are used to meet new requirements. Designers can vary the prematch capacitor, the bonding wires or they can choose a different package. Variations in the die, such as using more active areas, are also available to the designer.

The design of a power transistor is a matter of trial and error, because standard models for the components are either grossly inaccurate or do not exist at all. The availability in recent years of electromagnetic simulators which are able to accurately analyse power transistor constituent components, is a considerable step forward. The automation of the design process is nonetheless still in its infancy with substantial time being required, especially when new designs are needed. Computer Aided Design (CAD) can reduce the time if accurate electrical and thermal models for the components of the power transistor are available in the simulator.
Figure 1.6: Building a power transistor starting with a mounting base (a), placing a ceramic (b), adding a leadframe (c), placing capacitor and die (d), connecting bondwires (e) and finally placing the cap (f).

1.3 Statement of the problem and solution strategy

Designers of power transistors and power amplifiers are primarily interested in the electrical behaviour of a power transistor. More specifically they are interested in the large signal behaviour where the signal at the input and the signal at the output are no longer linearly related. Several parameters are of importance to the designers in this large signal regime. These parameters are normally referred to as ”large signal parameters”, and are discussed in more detail in the following chapter.

The problem is that in the CAD tools used by designers of power transistors a general modelling method or a general model for power transistors is not available. In this situation development time is dependent on the time needed for trial and error designs hampering short time-to-market introduction of new transistors. Some designers build their own model using lumped components, fitting the simulated performance to the measured performance of the power transistor. The model then serves as a starting point for further improvements. Unfortunately, this approach gives little insight into the actual working of the device nor does it help in solving practical problems.
The main question addressed in this thesis is whether it is possible to find a general modelling strategy for power transistors, where the resulting model is able to predict the large signal parameters of a power transistor. The model should include the electrical effects of the prematch capacitor, the bondwires, the package and the die. Additionally, the effect of self-heating must be accounted for. And last but not least the model should be incorporable in an existing CAD tool with limited simulation times. The time required to extract the large signal parameters for the model should be as short as possible.

In 1993 extensive discussions with the discrete semiconductor group of Philips Discrete Semiconductors Nijmegen led to the definition of a PhD research project in this area. Koen Mouthaan joined the project in August 1993. The Dutch Technology Foundation (STW) founded the project starting in November 1993. A second PhD student, Roberto Tinti, joined the project in January 1995. Philips Semiconductors and Agilent Technologies have provided substantial technical and financial support.

Although the project was driven by a request from Philips, it is most likely that other companies manufacturing power transistors, like Motorola and Ericsson, face similar problems.

It is important to note that for a correct description of the electrical behaviour the thermal behaviour must also be considered since a substantial amount of electrical power is dissipated, introducing an increase in temperature. The increased temperature in turn changes the electrical behaviour of the transistor and can, under certain conditions, even destroy the transistor. The interaction between electrical behaviour and temperature is referred to as electrothermal interaction.

**Short survey of reference literature for power transistor modelling**

A survey is given below of relevant publications discussing the modelling of RF power transistors at various levels of detail.

Numerous studies have been made on parts of power transistors. A good introduction to small signal transistors is given by Cooke [1]. An example of approximate calculations of (germanium) microwave transistor parameters are given in [2] for example. The interdigitated structure of base and emitter fingers introduces distributed effects which can not be neglected in some cases as shown in theory and by simulations by Wahl [3]. Shacklé confirmed Wahl’s conclusions by experiment [4]. In the first generations of interdigitated transistors distributed effects where also present in the base emitter area due to the relatively large distance between the fingers and the large width of the fingers. These current crowding effects were studied for example by Archer [5] and by Kakihana and Wang [6]. The currents and voltages at the terminals of the transistor were studied by Bailey [7]. These computer simulations indicated large distortion in the output signals under certain conditions. In these simulations compact transistor models were used to model the die. Graham et. al. [8] replaced these compact models by a one-dimensional device simulator to study the intrinsic behaviour of the transistor under working conditions. The behaviour of a power transistor was analysed by Lange and Carr [9] with a distributed model for the die and a relatively simple model for the package. In these references the main focus was on the modelling of the intrinsic transistor, the die. Harrison studied a complete transistor with a more complicated model for the package and a compact model for the die [10]. Chapman designed a series of high-efficiency broadband power transistors for S-band applications [11]. In the CAD of these transistors he used lumped models for the bondwires, the capacitors and the package.
In the past decades a vast amount of articles and books have appeared on the theory, modelling and technology for the intrinsic transistor. It is noteworthy, however, that throughout this period very few articles have appeared on the modelling of full power transistors with inclusion of bondwires, package and thermal effects. In 1979 in an invited paper Allison gave an overview of Silicon bipolar microwave power transistors. Unfortunately no impression is given of the state of the art of CAD of power transistors at that time. He noted an interconnection technique other than wire bonding to avoid "the costly time-consuming wire bonding". In the 1997 Microwave Symposium, Ping Li et al. approached this problem differently and used monolithically fabricated impedance matching circuits reducing the number of bondwires substantially [12].

For base station applications LDMOS transistors have been proposed in recent years by various manufacturers including Motorola [13], Philips [14] and Ericsson [15]. Northrop Grumman also reported the use of Silicon Carbide for high power transistors [16]. In most of these publications the issue of CAD of the power transistors is not dealt with. A good exception, worth mentioning, is the work of Ted Johansson of Ericsson [15]. In his thesis some CAD issues are addressed. An integrated approach, including thermal modelling and the modelling of self heating, is however not treated.

Looking at all this work it is worth looking from the perspective of a designer of RF power amplifiers. To that end an extensive quotation is given from a book that appeared in 1999 by Steve Cripps: "RF Power Amplifiers for Wireless Communications" [17].

The central issue in modeling an RF power transistor is scaling. Almost always, the detailed modeling and curve fitting are done on a small periphery sample device and may be quite accurate. [...] The PA designer has to take that small cell and scale it by tens, even hundreds to "build" a power transistor. The large periphery device will display a range of secondary phenomena that may have been quite negligible in the model cell. Nonuniform thermal effects, for example can play havoc with the customary assumptions made about equal currents and voltages across an array of "identical" circuit elements. The typically very low impedances obtained by multiple parallel connections also can cause other effects to come into play that would normally be neglected, including current spreading at bondwire contacts, electro-acoustic coupling in the semiconductor crystal, and mutual coupling between bondwires. [...] More and more, we are driven to the conclusion that the best of deriving accurate models for RF power transistors is to build amplifiers, even nonoptimized ones, and fit the combined circuit and device models to the measured results. [...] Undoubtedly, some individual groups of workers with the time and facilities have managed to get on top of most of the modelling issues for the successful simulation of PA products, but the full results are not always available to the general public in the form of easily implemented library files in commercially available CAD products. [...] Packaged RF power transistors seem to be poorly represented in commercial model databases.

In conclusion, it is found that in none of the publications a consistent modelling strategy is applied to the modelling of power transistors. Additionally, most of the publications consider low power transistors or medium power transistors at best.
Electrical modelling strategies

Several strategies are available for modelling power transistors. Three strategies are discussed in brief below.

Modelling by measurement

One strategy might be to brute force characterise power transistors by measuring all electrical parameters and thermal parameters at a (large) set of points in the area where the transistor operates. Interpolation and extrapolation routines are used to predict characteristics at points not measured. The method is relatively easy to implement yielding relevant parameters, such as output power and transistor impedance, in a short time. There are, however, drawbacks. The approach does not give full insight into the dynamic nonlinear behaviour of the transistor particularly in the case of bipolar devices. Further, it is difficult to optimize the transistor. Apart from not having a good idea which part or parameter to optimize, the complete cycle of producing and measuring the modified transistor must be followed. Consequently, modification and measurement time should be as short as possible in order to ensure short development times.

Modelling by rigorous calculation

Another strategy is to write down the governing electromagnetic equations, charge-transport equations and heat equations for a full power transistor and solve these equations for relevant parameters for the problem at hand. It is not possible to solve these equations exactly in the case of power transistors and numerical methods must be employed to find an approximate answer. These procedures normally break the problem down into a set of equations to be solved for the unknowns. Several questions arise at this point such as: "Is it feasible to solve the set of equations in a reasonable time with the computing power available?" and "If a solution of the set of equations is computed is the solution good enough or should the problem be further discretised into a larger set of equations?" and "Does the solution supply useful information? Does it give insight into dominant mechanisms?" At present several researchers are dealing with these problems for relatively simple structures. For high power transistors this approach is not feasible due to the range in dimensions. Dimensions of emitter and base fingers are in the order of micrometers and dimensions of the package are in the order of millimeters.

Modelling by segmentation

A third strategy for modelling the transistor is to consider dominant effects. Although not all effects and their respective order of relevance are known in great detail, some knowledge is available from practice. For each component a separate model, having a limited number of parameters and a number of ports is built. These models can be based on measurements, rigorous calculations or approximations. Models are connected together in an electrical simulator and the resultant network is solved for currents and voltages. An example of this segmentation approach is shown in figure 1.7. In fact this figure represents the model derived in this thesis for a specific power transistor: the Philips BLV 910. (cf. section 2.5).

In this schematic five constituent models are connected together. One model represents the
die. This model is connected on one side to the package model and on the other sides to the model for bondwires. This bondwire model is partly connected to the package model and partly to the model for the prematch capacitor. The capacitor model is connected to the package model and the bondwire models. The last bondwire model is connected to the prematch capacitor model and to the package model. If all bondwires have electromagnetic coupling, the two separate models are replaced by a single model.

Thermal modelling strategy

Similar methods as described above are applicable for the thermal modelling of power transistors. To be able to analyse the electro-thermal behaviour in an electrical simulator temperature is represented by voltage and heat fluxes and power dissipation are represented by currents. In other words the thermal impedance is represented by an electrical anlogon.

Before the main body of the research started a 3 month feasibility study was carried out at Philips Semiconductors Nijmegen by the author in 1993. The main bottleneck in the CAD of power transistors at that time was the availability of a compact model for bondwires. The simulator used by the Philips group in Nijmegen was Agilent’s Microwave Design System (MDS). At the end of this study it was concluded that the segmentation strategy was the most viable option. This was natural in that the segmentation strategy is similar to the way microwave circuits are designed using CAD tools. Additionally, building models of separate components yields compact models relatively quickly. Independent of the success of the project, models of separate components would become available in the course of the project. Furthermore, the segmentation approach allows for flexible modelling of the power transistor. If for example one model fails to describe the behaviour of bondwires correctly, this model can be replaced by another model without changing the whole model for the power transistor. Considering these points the segmentation approach is followed in this thesis.
1.4 The Philips BLV 910 high power transistor

To assess the modelling approach an existing power transistor is chosen as a test vehicle: the Philips BLV 910 transistor. The BLV 910 is a bipolar power transistor with externally one base lead, one collector lead and four emitter leads. A top view photo and a side view photo are shown in figure 1.8.

Figure 1.8: Photos of the Philips BLV 910 power transistor. On the left a top view photo and a side view photo on the right.

In the photo on the left the mounting base with two holes is clearly visible as well as the six leads. To give an idea of the dimensions the length of the mounting base is 25 mm, the width 6 mm and the height 2.5 mm. The bottom three leads are for emitter, base and emitter respectively and the top three leads are emitter, collector and emitter. The cap with the text imprinted is also visible. In the photo on the right the mounting base, the beryllium oxide ceramic, the leadframe and the cap are visible. The transistor is used in base stations operating in the 820 to 960 Mhz range and produces 10 Watts of output power at 800 mW of input power. The transistor is described in detail in section 2.5.

1.5 Outline of this thesis

In chapter 2 the statement of the problem, the governing equations and the solution method are outlined in more detail. A particular device, the Philips BLV 910 power transistor, is used to demonstrate the modelling approach. The implementation of models in MDS is considered and followed by a discussion of implementation issues of a resistance model as a demonstrator.

In chapter 3 the electrical models for the four components are discussed in more detail. First the modelling of the bondwires is considered and as an introduction the modelling of straight wires above a ground plane is discussed. This model is often used to model the behaviour of bondwires. A model for curved wires is introduced. This model computes the inductance matrix for a set of coupled bondwires including ohmic losses. This model is compared with rigorous simulations in Agilent’s 3D finite element simulator HFSS. The model is also compared with measurements for setups with one wire, to compare the self inductances, and setups with two coupled wires, to compare self- and mutual inductances.

Secondly the prematch capacitors are considered. Dominant effects are found using Sonnet’s Em planar simulator. Again the model is compared with rigorous simulations in HFSS.
Measurements of combinations of bondwires and prematch capacitors are compared with simulations. Thirdly the modelling of the die is studied. For the electrical model the Mextram compact transistor model is used. Due to the inhomogeneous temperature distribution several of these compact models, each having its own temperature are placed in parallel. Finally the modelling of the package is considered. The package model is based on electromagnetic simulations in Sonnet’s Em and Agilent’s Momentum.

In chapter 4 the thermal modelling of power transistors is considered. Starting point is the one-dimensional thermal conduction equation. The one-dimensional model is extended with heat spreading. Although this model fits measured data well, it doesn’t give full insight in the three-dimensional heat distribution. Several methods for measuring the thermal impedance of the power transistor are discussed in brief. Special attention is given to the electrothermal measurement of the thermal impedance. A full three-dimensional heat conduction model is introduced to account for all couplings between heat areas and the heat spread in the die and the package.

In chapter 5 the electrical models and thermal models are combined together to form a complete model for the BLV 910 power transistor. The full model is compared with measurements of the DC traces, small signal scattering-parameters and large signal parameters. Finally this thesis ends with conclusions and recommendations for further research.

1.6 Scope of this work

Previously it was stated that designers of power transistors need predictive models for power transistors in existing CAD tools like Agilent’s MDS. In a feasibility study the segmentation approach was found to be the most viable approach. For the electrical modelling this approach is used to derive the electrical model for a power transistor. The four components of a power transistor (die, prematch capacitor, bondwires and package) are modelled separately. Physical parameters obtained from measurements, such as dimensions of bondwires, should be the basis for all models.

The segmentation approach is also pursued to model the conduction of heat through the die and the ceramic to the mounting base. The first important question is whether it is possible to derive separate models which are able to describe the behaviour with sufficient accuracy. In the process of finding the models various important questions arise. Some of them are addressed in detail and others remain for further research.

All models are implemented in Agilent’s MDS allowing designers to directly apply the models and the modelling techniques. The models can also be used to find answers to specific questions without using them in the context of a full power transistor model. The thermal models for example can be used separately to make temperature estimates. The bondwire model can be applied to find the equivalent inductances of a set of coupled bondwires. The use of the models by designers should produce enough feedback for their improvement in a later stage. Some of the models are being transferred to Agilent’s new microwave simulator ADS and become commercially available. To test the approach chosen the modelling is applied to a 10 Watt power transistor.

The main question is if the segmentation approach in combination with the implemented models is able to predict the DC behaviour, the small signal RF behaviour and the large signal RF behaviour of a power transistor correctly.
Chapter 2

Statement of the problem

2.1 Introduction

This chapter states the problem and also serves as an introduction into the modelling approaches applied. Traditionally in the design of power transistors trial and error methods are used. First power transistor is build and measured and based on experience the transistor is modified and measured. This process is iterated until the target specifications are achieved. This was more or less the situation in 1993 when this project started. Fortunately, in recent years the situation has changed due to increased computing power and the notice among most designers for the usability of CAD tools. Nevertheless, there is a stronger need then ever for predictive models of high power transistors. The models must be able to predict the DC behaviour, the RF small signal behaviour, the RF large signal behaviour and the thermal behaviour. A strong requirement is that the models must be easily available to designers in an electrical simulator and the models also must be easy usable by designers. The principle aim of this thesis is to derive and implement these models. Prior to this work, a feasibility study was performed for Philips Semiconductors Nijmegen and it was found that the segmentation approach is the most viable approach for modelling power transistors. Some of the characteristics, advantages and disadvantages of this approach are outlined in section. In this approach, the components of a power transistor are modelled separately and represented by multiports (N-ports). In MDS several methods for implementing models are available. The options and requirements for implementing models in MDS are reviewed in section 2.3. Because the models presented in this work are based on physics equations, the solution to these equations must be translated into N-port parameters. For reasons of completeness linear N-port parameters are described in section 2.4.

The Philips BLV 910 serves as a test vehicle for the segmentation approach. This transistor is described in detail in section 2.5. By placing a power transistor in an amplifier transistor quantities such as gain and output power can be measured or calculated. These quantities are given in section 2.6.

The electrical behaviour of the active component of the power transistor, the die, is governed by complex non-linear equations. Device simulators can solve these equations by discretising the problem using physical parameters such as dimensions and doping profiles as input. Most device simulators are two dimensional solvers i.e. the problem is only solved in two
directions under the assumption that the structure is invariant in the third direction. Due to the complexity of the problem these device simulators are able to solve only a very small part of the die. Instead of attempting to solve these equations, the die is modelled using a so called "compact transistor model". More specifically in this work the Mextram compact transistor model [18] is used. This is a model available in MDS being able to represent the electrical behaviour of (parts of) the die rather accurately once the compact model parameters are known. In section 2.8 the compact modelling of the die is reviewed. The remaining components of the power transistors are all passive components. In section 2.7 the governing equations and elements used in the electrical modelling are discussed. Because temperature is of significant importance for the electrical behaviour, mechanisms of heat flow and governing equations are discussed in section 2.9. In building the electrical models and the thermal models extensive use is made of integral equations and Green's function. For reasons of completeness these are discussed in section 2.10.

2.2 Advantages and disadvantages of segmentation modelling

Before the research started a feasibility study of 3 months was performed at Philips Semiconductors Nijmegen by the author in 1993. At the end of this study it was concluded that the segmentation strategy was the most viable option at that time. The reason is that the segmentation strategy is close to the way microwave circuits are being designed using CAD tools. Additionally, building models of separate components yields compact models relatively fast. Even if the project would fail, models of separate components would still be available. Additionally, the segmentation approach allows a flexible modelling of the power transistor. If for example one model fails to describe the behaviour of bondwires correctly, this model can be replaced by another model without changing the whole model for the power transistor. The characteristics, advantages and disadvantages associated with this approach are discussed in the following.

- Parts of the transistor are represented by models with a number of ports and a number of parameters. In some cases parts may even be modelled with discrete elements such as inductors, resistors, capacitors and transmission lines.
- Optimisation of a transistor reduces to optimization of subcircuits although the full model is used during the optimization.
- Implementation of a model for a transistor reduces to the implementation of models for the components (die, bondwires, package and prematch capacitor). The implementation of each model can be fully optimized for maximum computational speed and minimum memory usage.
- Only dominant effects are modelled, and some couplings are neglected. The exact accuracy of the model is hard to estimate. In principle it should be possible to estimate the accuracy of the model for each component by performing rigorous calculations. By comparing the complete model of a power transistor with for example measurements it should be possible to find the error introduced by the neglected couplings.

Each characteristic is reviewed briefly below. Modelling each component of the transistor separately follows intuition. The user of the model does not need to understand the underlying theory in great detail. In case of the bondwires for example one would expect a set
of coupled inductances with resistors being added to model losses. It is noted however that representing physical situations by circuit elements should be done with care. Bonding wires for example behave capacitively in some cases. Additionally, modelling each component separately might ignore important couplings.

The optimization of the modelled performance of a power transistor can be rather difficult due to the large number of parameters involved and the influence each parameter has on the overall performance of the power transistor. If the desired response of each model is known, it is in principle possible to optimize the parameters associated with that model for the desired response. For example, if a bondwire inductance of 0.6 nH is required it is possible to optimize the bondwire geometry for that inductance. It may occur however that during the optimization a model is used in a parameter range where underlying assumptions for the model do not hold anymore. A solution to this problem is to determine in which parameter range a model is valid. But in many cases this is difficult and sometimes even possible.

The third point is the implementation of models into an electrical simulator. For every component a model is implemented having its own function. For example the thermal model implemented computes the conductance of heat in the substrate, but it does not model thermal radiation or convection. To include radiation either this effect must be added to the model or an additional model must be implemented.

All models discussed in this thesis are implemented in Agilent's Microwave Design System (MDS). On the one hand this gives a well defined method for implementing linear models and non-linear models. On the other hand it puts some restrictions on the capabilities of the model. In the thermal modelling for example the spatial distribution of the power dissipation must be known. In transistors this distribution depends strongly on the electrical state of the junction. The die is modelled using so called compact transistor models. It is not feasible however in MDS to let a compact transistor model tell the thermal model the shape of the power dissipation, even if this shape is known.

An advantage of implementing separate models is that each model can be fully optimized for computational speed and memory usage. In many cases however, the optimization does not improve the overall speed and memory requirements for a full model of a transistor. In for example the electrothermal modelling compact transistor models are used in combination with thermal models, simulation times are mainly dominated by the number of iterations used for the solution of the non-linear equations.

The last point to consider is the accuracy of the model. Due to the various approximations made, there can be a considerable error in the results. In some cases these errors can be traced by comparing the model with measurements or rigorous calculations. For example the measurement of the DC traces of a transistor is relatively simple and can be performed with little error. These traces can be compared with simulated DC traces of the model. It should be kept in mind however that in all parameters practical process variations exist. For example the current gain of a transistor can vary within a few percent from sample to sample if the samples are from one batch, but it can vary much more from batch to batch. Another point is that in some measurements the errors can be large making a solid comparison difficult. Each submodel should therefore be tested by doing careful experiments on simplified structures with a well understood behaviour.
2.3 Implementation of models in MDS

Agilent's Microwave Design System (MDS) is used to simulate the electrical circuits representing the electrical behaviour and the thermal behaviour. The simulator offers a wide range of analysis options such as DC analysis, transient analysis, small signal and Harmonic Balance analysis. To simulate circuits models and their current-voltage relations are available in libraries. The libraries of MDS include a variety of compact models for interconnects and active devices. A distinction can be made between linear models and non-linear models. All models discussed in this work are implemented in MDS. The methods available for implementing of models in MDS are discussed below.

Data collection methods. Data is generated by (external) software packages or by measurement subsequently the data is read into datasets. This method is normally used for linear models. An example are the measured scattering parameters of a transmission line. The datasets are then used in the simulations. Interpolation and extrapolation methods are used for points not included in the dataset. This option is quite often used to generate microwave libraries for fixed components such as SMD components and the small signal response of transistors at a specific bias point.

Equivalent circuit methods. An equivalent circuit model is made for the problem at hand. The element values are defined by analytical functions or extracted from other data such as fitting a measured response to the response of the equivalent model. This method has some disadvantages. First of all the model must be capable of representing the behaviour of the structure under consideration. A second problem is in the estimation of equivalent circuit parameters from external data. Quite often parameters can not be estimated uniquely from the data available and optimization routines must be used. If measured data is used the parameters extracted may be sensitive to measurement error.

Symbolically Defined Device (SDD). The Symbolically Defined Device (SDD) is used to define non-linear multiport devices. This option is often used in the initial development of non-linear models in MDS. A main advantage is that an implementation of a non-linear model is achieved very fast in principle because there is no need for software coding. There are some drawbacks however. First of all it is not possible to interface with external computer programmes. SDD's could be much more flexible if such external function calls were supported at the SDD level. Models implemented in SDD are computationally slower than models coded directly into the simulator.

User Compiled Linear Models. Another method to implement models in MDS is through the use of User Compiled Linear models. In this method only linear models can be implemented. At this level a computer programme is written by the user describing the linear behaviour of a device to the simulator in terms of either scattering parameters or admittance parameters. These programmes can be written in for example Pascal, Fortran and C++. This option has been used extensively in this work to implement models in MDS. The main advantage is that user written software can be included into the model. A detailed knowledge of the coding of models into the simulator is not required however. The main task for the user is to define a evaluation routine having input parameters and returning scattering or admittance parameters.

This method has a number of disadvantages. Non-linearities can not be included in the models. In most cases however this is not necessary. Generic models can not be handled. For example, we have implemented a computer programme which computes the Y-parameters for any number of bondwires. Unfortunately, separate models must be implemented for one
wire, two wires, three wires etc. This drawback comes into play if models are needed up to 100 or more bondwires. Compilation time and memory requirement of the MDS executable grow with the number of models implemented. The standard simulator executable is around 6 Mb but the same executable with 100 bondwire models is around 11 Mb. Another point that could be improved is the access to library functions in MDS. For example matrix solve routines and eigenvalue routines should be made available to the user.

Compiled Non-linear models The last method is the most complete method. With compiled non-linear models the non-linear model is coded directly into the simulator. The simulator passes a guess for the terminal voltages to the model and the model returns the currents and charges and their respective voltage derivatives to the simulator. Some 30 functions specify the device behaviour. Not all these functions need to be defined. There are a number of disadvantages. First of all, this option is not available to the user and is not documented. Second, the implementation requires a substantial amount of coding and debugging time. A large part of the code is dedicated to book keeping. Thirdly, it is not possible to let the model control the simulator. Normally the simulator passes a guess of the voltages to the model and the model returns currents and derivatives. This can be viewed as a master/slave situation where the model acts as a slave. After the simulator has found convergency the model is not called anymore. In some cases however we want to tell the simulator that after convergency is found, the model must be evaluated once more.

2.4 Network parameters

Network parameters relate the electromagnetic behaviour and thermal behaviour with network theory. To characterise a N-port network several parameters exist, such as scattering parameters, transmission parameters, admittance parameters. These three parameters are reviewed here for several reasons. The implementation of linear models with an "User Compiled Linear Model" in MDS requires the use of either admittance parameters or scattering parameters. In section 2.10 it is shown that the determination of the impedance matrix is easy using Green's functions. In these cases the admittance matrix is found by inverting the impedance matrix. Additionally, in the microwave measurements discussed in this work scattering parameters are used.

Before reviewing the parameters there are points to consider:

- In network theory current flows into ports or out of ports. To model these ports electromagnetically they must have physical dimensions where current is injected in volumes or areas. In many models used in this work, the current is injected in brick shaped volumes. And in the case of thermal models it is assumed that heat is generated uniformly in these volumes.
- Voltages are defined at ports. In practice ports have physical dimensions and in the models a point must be specified at which the potential is computed. In many models used in this work voltage is computed at the center of brick shaped injection volumes. A similar approach is used in the thermal modelling.

For reasons of completeness three network parameters are discussed briefly: impedance parameters, admittance parameters and scattering parameters. Several good textbooks about
network parameters are available. For example Dobrowolski [19], chapter 2 deals with Y-, Z- and S-parameters and their interrelations and Kurokawa [20] discusses S-parameters and their properties in detail. Consider a linear N-terminal device with the ground node as reference node. The elements of the impedance matrix are given by:

\[ Z_{ij} = \frac{U_i}{I_j} \quad I_k = 0, k = 1 \ldots N, k \neq j \quad (2.1) \]

The way to compute or measure these parameters is to inject a current \( I_j \) into port \( j \) and the voltage is observed at port \( i \) under the condition that all other ports are open-circuited. The ratio between the voltage and the current defines the impedance parameter. Note that it must be possible for a current to flow into the port. This method will be used to calculate the resistance matrix in case of electrical conduction modelling and to calculate the thermal resistance matrix in case of steady-state heat conduction. The requirement that all currents \( I_k \), except \( I_j \), must be zero in equation (2.1), results in simple expressions for the matrix elements in these cases. The admittance matrix is computed by inverting the impedance matrix.

The elements of the admittance matrix are given by:

\[ Y_{ij} = \frac{I_i}{U_j} \quad U_k = 0, k = 1 \ldots N, k \neq j \quad (2.2) \]

The way to compute or measure these parameters is to apply a voltage \( U_j \) to port \( j \) and to measure the current \( I_i \) at port \( i \). Note that it must be possible to apply a voltage to the port. This method is difficult to apply in modelling, since short circuiting ports is normally not possible as is shown later. The impedance matrix is computed by inverting the admittance matrix.

Finally scattering parameters are introduced. These parameters are of special importance in microwave engineering. In characterising networks it is very difficult to make open or short circuits without introducing unwanted parasitics. Additionally, in some cases terminating a network is highly undesirable. Some amplifiers for example are damaged when terminated with an open or a short. With scattering parameters the ports are connected to a known impedance, usually 50 \( \Omega \). The elements of the scattering matrix are defined in terms of transmitted and reflected power waves:

\[ S_{ij} = \frac{b_i}{a_j} \quad a_k = 0, k = 1 \ldots N, k \neq j \quad (2.3) \]

where \( a_j \) is the incident wave at port \( j \) and \( b_i \) is the scattered wave at port \( i \). Note that incident and scattered waves are defined in terms of complex normalisation constants associated with each port. These are most often the characteristic impedances of connecting lines at these ports. General conversion equations exist between scattering parameters and the Z- and Y-parameters (cf. [19], page 51).

### 2.5 The BLV 910 power transistor

The Philips BLV 910 power transistor is used as a demonstrator for the modelling approach. Once again it is noted that the approach described in this work is applicable to almost any other solid state RF power transistor.
The BLV 910 is used in the driver amplifier or in the final amplifier stage of base stations operating at frequencies around 900 MHz. With an input power of around 800 mW, the output power is 10 Watts under class-AB operation. Three photos of the BLV 910 are shown in figure 2.1.

![Image of BLV 910 power transistor](image)

Figure 2.1: The BLV 910 power transistor. In the top left the packaged device is shown and in the top right the ceramic cap is removed from the device. In the bottom photo a side view is given.

In the photos the mounting base, with two holes in it, is clearly visible. In practical applications the transistor is firmly attached to a heat sink with screws through the two holes. In the top left photo the six leads of the transistor are also visible. The bottom three leads are emitter, base and emitter respectively. And the top leads are emitter, collector and an emitter. Normally these leads are soldered to the input and output printed circuit boards. The leads are a part of the leadframe. This leadframe is clearly visible in the top right photo. The leadframe is glued on a substrate of beryllium oxide (BeO). The BeO substrate is attached to the mounting base and provides electrical isolation between the components on the leadframe and the mounting base. The main reason to use the highly poisonous beryllium oxide is its high thermal conductivity thus providing a good conduction of heat from the die to the mounting base. To protect the die, prematch capacitor and bondwires a ceramic cap is placed over the components. The mounting base, beryllium oxide, leadframe and the cap are visible in the bottom photo.

In the top right photo of figure 2.1 the cap is removed and the interior of the transistor is visible. In figure 2.2 scanning electron microscope (SEM) photos of the interior transistor are shown.

In the top left photo the die, the prematch capacitor, the bondwires and the main part of the
Figure 2.2: SEM photographs of the BLV 910 power transistor. In the top left photo the four main components are visible. These components are the die, the prematch capacitor, the bondwires and the package. In the top right photo the prematch capacitor is shown. The left bottom photo displays a top view photo of the die with eight active areas. And finally in the bottom right photo the interdigitated structure of base and emitter fingers are shown. The emitter ballasting resistors are also visible.

The leadframe of the package are visible. The input of the transistor, the base lead, is on the left and the output, the collector lead, is on the right in this photo. In the top right photo a close-up of the prematch capacitor is shown. The capacitor consists of a block of conducting silicon (Si) with two different contacts. The contact on the left is a metal line, mainly gold, on top of a thin layer of silicon dioxide (SiO₂) forming a metal-oxide-semiconductor (MOS) capacitor. The contact on the right is a metal deposited directly on the silicon forming a low ohmic contact. In combination with the bondwires the prematch capacitor transforms the low input impedance of the die to a higher impedance at the input of the transistor.

In the bottom left photo a top view of the die is shown. The bonding wires and eight active areas, where the actual RF amplification takes place, are visible. The last photo on the bottom right displays an active area. The interdigitated structure of base and emitter fingers is visible as well as the emitter ballasting resistors in the emitter lines. These resistors suppress high local currents to diminish local heating. In silicon bipolar transistors local heating increases the local currents which eventually may lead to thermal runaway.

The objective of this work is to define a descriptive and a predictive model for the electri-
cal behaviour of the power transistor. The input parameters of this model must be physical and measurable parameters such as geometrical dimensions, conductivities and compact transistor model parameters.

In the approach used, the transistor is divided into four constituent parts: the die, the prematch capacitor, the bondwires and the package. Separate electrical models are made for each of these components.

A thermal model is built for the die and the package only because the effect of the bondwires and the prematch capacitor on the thermal behaviour is assumed negligible. A complete model of the power transistor is obtained by connecting the models together. Agilent's Microwave Design System (MDS) is used as the simulator in this work, although any other simulator offering the same capabilities could have been used. There are several reasons for this choice. First of all, the group where this work was performed has a strong working knowledge of this software tool. MDS also offers an extensive library of predefined elements, including transmission lines, microstrip lines and a variety of non-linear models. One of the drawbacks is the rather limited information detailing model implementation and which effects are accounted for. A good point of MDS is the availability of a number of solvers, including a non-linear DC solver, an AC solver and a Harmonic Balance (HB) solver. Another good point is the possibility of implementing both linear and non-linear models in a variety of ways. In section 2.3 the possibilities of implementing models in MDS are discussed in more detail.

**Material parameters**

Throughout this work various physical calculations are made. These calculations not only require dimensions, such as the heights of substrates, but also the material parameters. In fact, the accurate determination of the values of the material parameters is a study in itself. Therefore we have used data commonly available. It is noted however that variations in the order of 5-10% can be found from reference to reference for some of the parameters. The values of the material parameters used in this work are reported in table 2.1. The relevance of the electrical parameters and the thermal parameters becomes clear in section 2.7 and section 2.9 respectively. The electrical parameters (\(\varepsilon, \mu, \sigma\)) are assumed to be independent of temperature and frequency. The thermal parameters are assumed independent of the voltage and the current flowing through the material involved. It is noted however that from the thermal parameters both \(k\) and \(c\) depend strongly on temperature. For this work the temperature dependence of \(k\) is of importance as discussed in section 4.2.

It is strongly recommended for future work in this area to derive measurement methods for the determination of the material parameters. Special attention should be given to the temperature dependency of the thermal conductivity of the silicon of the die.

**2.6 Definition of power transistor quantities**

To review power transistor quantities such as gain, efficiency, input power, output power a common emitter power transistor circuit is shown in figure 2.3.

In the center the BLV 910 power transistor is shown with the emitter grounded. The transistor is driven by a source with available power \(P_S\) at angular frequency \(\omega\) and input impedance \(R_S + jX_S\) and is terminated with a load impedance \(Z_L = R_L + jX_L\). The angular frequency is \(2\pi f\) where \(f\) is the frequency of operation. The transistor is biased at the base with the
<table>
<thead>
<tr>
<th>Material</th>
<th>Component</th>
<th>$\varepsilon_r$</th>
<th>$\mu_r$</th>
<th>$\sigma$ (S/m)</th>
<th>$\kappa$ (W/m·K)</th>
<th>$c$ (J/kg·K)</th>
<th>$\rho$ (kg/m$^3$)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Si</td>
<td>die</td>
<td>11.7</td>
<td>-</td>
<td>156</td>
<td>650</td>
<td>2330</td>
<td></td>
</tr>
<tr>
<td>BeO</td>
<td>package</td>
<td>6.4</td>
<td>1</td>
<td>0</td>
<td>270</td>
<td>1300</td>
<td>3000</td>
</tr>
<tr>
<td>Cu</td>
<td>package</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>400</td>
<td>400</td>
<td>8800</td>
</tr>
<tr>
<td>Si</td>
<td>capacitor</td>
<td>3.9</td>
<td>1</td>
<td>0</td>
<td>-</td>
<td>-</td>
<td>-</td>
</tr>
<tr>
<td>SiO$_2$</td>
<td>capacitor</td>
<td>11.7</td>
<td>1</td>
<td>$5 \cdot 10^4$</td>
<td>-</td>
<td>-</td>
<td>-</td>
</tr>
<tr>
<td>Au</td>
<td>bondwires</td>
<td>-</td>
<td>-</td>
<td>$4.1 \cdot 10^7$</td>
<td>-</td>
<td>-</td>
<td>-</td>
</tr>
<tr>
<td>Au</td>
<td>leadframe</td>
<td>-</td>
<td>-</td>
<td>$4.1 \cdot 10^7$</td>
<td>-</td>
<td>-</td>
<td>-</td>
</tr>
</tbody>
</table>

Table 2.1: Values of material parameters used throughout this work.

**Figure 2.3:** The BLV 910 power transistor is driven by a power source with available power $P_S$ and impedance $R_S + jX_S$. The transistor output is terminated with a load impedance $R_L + jX_L$. To separate the DC bias from the RF signals, the ideal capacitor $C$ acts as a DC block and the inductor $L$ acts as a DC feed.

bias voltage $V_{BE}$ and the bias current is $I_B$. At the base the transistor is in practical situations biased with a voltage source but in some special cases a current source is used. The bias voltage at the collector is $V_{CE}$ and the current is $I_C$. Normally a voltage source biases the collector, but in some cases a current source is used.

The biasing depends on the class of RF operation of the transistor. For example in class-A, used for linear amplification, the bias levels are relatively high. In class AB the biasing is reduced to increase the efficiency of the transistor with the drawback of a less linear amplification. In class-C, a strong non-linear amplification, the transistor is not biased. The capacitor $C$ represents an ideal connection for RF signals blocking the DC voltage. The inductor $L$ represents an ideal connection for the bias voltages and it blocks the RF signals. The power flowing into the transistor at the base is denoted by $P_{in} = \frac{1}{2}\Re(V_{in}I_{in})$ and the input impedance of the power transistor is given by $Z_{in} = R_{in} + jX_{in} = V_{in}/I_{in}$. The power flowing out of the transistor is denoted by $P_{out} = \frac{1}{2}\Re(V_{out}I_{out}^*)$ and the output impedance of the transistor is $-V_{out}/I_{out}$.

Since the transistor is driven by a time-harmonic source with angular frequency $\omega$ the current and voltage at both input and output are decomposable in time-harmonic values with frequencies being integer values of $\omega$. Harmonic Balance (HB) algorithms use this property to solve non-linear networks driven by time-harmonic sources.
In the following, values of quantities specified by the transistor manufacturer (Philips) in the datasheets are given. To understand these numbers, the definitions of these quantities are given briefly. The definitions of some of these quantities differ from the definitions given above.

**DC quantities**

The quiescent current at the collector $I_{CQ}$ is defined as the current $I_C$ with zero power at the RF source. The DC power flowing into the transistor $P_{DC}$ is defined as: $P_{DC} = V_{BE}I_B + V_{CE}I_C$. The DC current gain is defined as the ratio between collector and base current with zero power of the power source: $h_{FE} = I_C/I_B$.

**RF quantities**

The input power $P_{in}$ is defined as the component of the input power with angular frequency $\omega$ and the power delivered to the load $P_L$ is defined as the component of the output power with angular frequency $\omega$. The input impedance $Z_{in}$ and load impedance $Z_L$ are defined as the component with angular frequency $\omega$ of the ratio between the voltage and the current at the input and output respectively. The power gain of the transistor is defined as the ratio between the power delivered to the load and the input power: $G_P = P_L/P_{in}$. The efficiency of the transistor is defined as the ratio between the power delivered to the load and the DC power: $\eta = P_L/P_{DC}$. The same definition is used for the power added efficiency (PAE) with the input power being subtracted from the load power: $\text{PAE} = (P_L - P_{in}) / P_{DC}$. The values published in the datasheets are obtained by optimizing input impedance and output impedance for maximum power gain or maximum PAE.

**Thermal quantities**

The temperature at the junction of the transistor is denoted by $T_j$ and the temperature of the heatsink is denoted by $T_h$. The thermal resistance from junction to mounting base is denoted by $R_{thj-mb}$ and it is defined as the ratio between the temperature difference from junction to mounting base and the power dissipated. The thermal resistance from mounting base to heatsink, denoted by $R_{thmb-h}$, is defined as the ratio between the temperature difference from the top of the mounting base to the heat sink and the dissipated power. The total dissipated power is denoted by $P_{tot}$. In principle the junction temperature is computed from the above quantities as follows:

$$T_j = P_{tot}(R_{thj-mb} + R_{thmb-h}) + T_h$$

(2.4)

In chapter 4 it is shown that these concepts must be used with care in the case of power transistor with large active areas. In large power active areas not a single junction temperature is present but a temperature profile is found instead.

**Datasheets**

For reasons of convenience data as published by Philips in the datasheets is listed in the four tables shown below.
### Table 2.2: Quick reference data. RF performance at $T_{mb} = 25 \, ^\circ\text{C}$ in a common emitter test circuit.

<table>
<thead>
<tr>
<th>Mode of operation</th>
<th>Frequency (MHz)</th>
<th>$V_{CE}$ (V)</th>
<th>$P_L$ (W)</th>
<th>$G_P$ (dB)</th>
<th>$\eta$ (%)</th>
</tr>
</thead>
<tbody>
<tr>
<td>CW, class-AB</td>
<td>960</td>
<td>26</td>
<td>10</td>
<td>$\geq 11$</td>
<td>$\geq 55$</td>
</tr>
</tbody>
</table>

### Table 2.3: Limiting values.

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Conditions</th>
<th>Min</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>$I_C$</td>
<td>collector current (DC)</td>
<td></td>
<td>-</td>
<td>1.5</td>
<td>A</td>
</tr>
<tr>
<td>$I_{C(AV)}$</td>
<td>average collector current</td>
<td></td>
<td>-</td>
<td>1.5</td>
<td>A</td>
</tr>
<tr>
<td>$P_{tot}$</td>
<td>total power dissipation</td>
<td>up to $T_{mb} = 25 , ^\circ\text{C}$</td>
<td>-</td>
<td>30</td>
<td>W</td>
</tr>
<tr>
<td>$T_j$</td>
<td>operating junction temperature</td>
<td></td>
<td>-</td>
<td>200</td>
<td>$^\circ\text{C}$</td>
</tr>
</tbody>
</table>

### Table 2.4: Thermal characteristics.

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Conditions</th>
<th>Value</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>$R_{thj-mb}$</td>
<td>thermal resistance from</td>
<td>$P_{tot} = 30 , \text{W}; \ T_{mb} = 25 , ^\circ\text{C}$</td>
<td>5.85</td>
<td>K/W</td>
</tr>
<tr>
<td></td>
<td>junction to mounting base</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$R_{thmb-h}$</td>
<td>thermal resistance from</td>
<td>$P_{tot} = 30 , \text{W}; \ T_{mb} = 25 , ^\circ\text{C}$</td>
<td>0.4</td>
<td>K/W</td>
</tr>
<tr>
<td></td>
<td>mounting base to heatsink</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

### 2.7 Electrical Modelling

The electrical behaviour of the power transistor is governed by Maxwell’s equations. These equations are discussed in brief, detailed descriptions are found in for example references [21], [22] and [23]. The emphasis is on the “passive” parts: package, bondwires and prematch capacitor. Two software packages are considered for solving the discretised Maxwell’s equations: Agilent’s HFSS and Sonnet’s Em. The limited applicability of these solvers for some of the problems at hand and the relatively low frequency justifies a reduction of Maxwell’s equations to the quasi-static equations for a number of cases. The circuit concepts of resistance, conductance, capacitance and inductance are based on the quasi-static equations. For

### Table 2.5: Characteristics. $T_j = 25 \, ^\circ\text{C}$.

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Conditions</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{(BR)CBO}$</td>
<td>collector-base</td>
<td>open emitter; $I_C = 5 , \text{mA}$</td>
<td>70</td>
<td>-</td>
<td>-</td>
<td>V</td>
</tr>
<tr>
<td></td>
<td>breakdown voltage</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$V_{(BR)CEO}$</td>
<td>collector-emitter</td>
<td>open base; $I_C = 15 , \text{mA}$</td>
<td>30</td>
<td>-</td>
<td>-</td>
<td>V</td>
</tr>
<tr>
<td></td>
<td>breakdown voltage</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$V_{(BR)EBO}$</td>
<td>emitter base</td>
<td>open collector; $I_E = 0.3 , \text{mA}$</td>
<td>3</td>
<td>-</td>
<td>-</td>
<td>V</td>
</tr>
<tr>
<td></td>
<td>breakdown voltage</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$h_{FE}$</td>
<td>DC current gain</td>
<td>$V_{CE} = 10 , \text{V}; \ I_C = 0.5 , \text{A}$</td>
<td>30</td>
<td>-</td>
<td>120</td>
<td></td>
</tr>
</tbody>
</table>


reasons of convenience the concept of resistance and conductance -in lumped form and in matrix form- is discussed in some detail because a direct relationship between physics and the implementation of physical models in a circuit simulator becomes apparent. The use of the resistance matrix in the thermal modelling of power transistors is another reason to discuss it to some extent. For reasons of completeness the concept of a transmission line is also described, mainly because transmission lines return in the modelling of the prematch capacitor, the package and in the simplified thermal modelling.

2.7.1 Maxwell’s equations

Maxwell’s first and second equation governing the electromagnetic behaviour in matter are introduced. A detailed discussion of these equations is found in for example [21]. For reasons of simplicity a small overview is given starting with Maxwell’s equations in matter:

\begin{align}
-\nabla \times \mathbf{H} + \mathbf{J} + \partial_t \mathbf{D} & = -\mathbf{J}^e \\
\nabla \times \mathbf{E} + \partial_t \mathbf{B} & = -\mathbf{K}^e
\end{align}

where

\begin{align}
\mathbf{E} & \quad \text{the electric field strength} \\
\mathbf{H} & \quad \text{the magnetic field strength} \\
\mathbf{B} & \quad \text{the magnetic flux density} \\
\mathbf{D} & \quad \text{the electric flux density} \\
\mathbf{J} & \quad \text{the volume density of electric current} \\
\mathbf{J}^e & \quad \text{the volume density of external electric current} \\
\mathbf{K}^e & \quad \text{the volume density of external magnetic current}
\end{align}

(V/m) \quad (A/m) \quad (T) \quad (C/m^2) \quad (A/m^2) \quad (A/m^2) \quad (V/m^2)

The compatibility relations are obtained by taking the divergence of Maxwell’s equations and using the rule \(\nabla \cdot \nabla \times \mathbf{F} = 0\):

\begin{align}
\nabla \cdot (\mathbf{J} + \partial_t \mathbf{D}) & = -\nabla \cdot \mathbf{J}^e \\
\nabla \cdot (\partial_t \mathbf{B}) & = -\nabla \cdot \mathbf{K}^e
\end{align}

Additionally, the volume density of unpaired electric charge \((C/m^3)\) is given by:

\[ \rho = \nabla \cdot \mathbf{D} \]

The constitutive relations for a linear, homogeneous, isotropic, time-invariant, instantaneously reacting and locally reacting medium are given by:

\begin{align}
\mathbf{J} & = \sigma \mathbf{E} \\
\mathbf{D} & = \varepsilon \mathbf{E} \\
\mathbf{B} & = \mu \mathbf{H}
\end{align}

The medium parameters are given in these equations by the permittivity \(\varepsilon = \varepsilon_0 \varepsilon_r \ (F/m)\), the conductivity \(\sigma \ (S/m)\) and the permeability \(\mu = \mu_0 \mu_r \ (H/m)\).
Boundary conditions

There are boundary conditions at the (source free) interface of two materials. Denoting the normal to that interface by $\mathbf{n}$, continuity of the tangential components of the electric and magnetic field is required:

$$\begin{align*}
  \mathbf{n} \times \mathbf{E} \\
  \mathbf{n} \times \mathbf{H}
\end{align*}$$

continuous across an interface \hspace{1cm} (2.13)

Additionally, the compatibility relations at the interface require the continuity of the normal component of the electric and magnetic flux through an interface:

$$\begin{align*}
  \mathbf{n} \cdot (\partial_t \mathbf{D} + \mathbf{J}) + \mathbf{n} \cdot \mathbf{J}' \\
  \mathbf{n} \cdot \partial_t \mathbf{B} + \mathbf{n} \cdot \mathbf{K}'
\end{align*}$$

continuous across an interface \hspace{1cm} (2.14)

In section 2.10.3 it is shown how these interface conditions can be enforced.

2.7.2 Electromagnetic software packages

In modelling components or in verifying models often electromagnetic software based on numerical methods are used. Also in this work electromagnetic software is used and therefore it is worthwhile reviewing these packages in brief.

Generally numerical methods discretise Maxwell’s equations into a finite set of equations. Various numerical procedures exist to solve Maxwell’s discretised equations for electromagnetic fields in media using local methods and global methods. Examples of local methods are the Finite Element Method (FEM), the Finite Difference Method (FDM), the Finite Integration Method (FIM) and the Transmission Line Matrix method (TLM). An example of a global method is the Method of Moments (MoM).

The Finite Element Method discretises the structure under consideration in subdomains. At the boundaries of each subdomain weighted conditions are applied. The Finite Element Method normally produces large sparse matrices to be solved for field quantities.

In Finite Difference Methods the differential form of Maxwell’s equations is replaced by the finite difference form. These equations are applied to a grid of points with field values computed at these points. This method, as in FEM, normally results in large sparse matrices. In a particular version of the method, the Finite Difference Time Domain Method (FDTD), a marching-on-in-time scheme is used to compute the response to an excitation in the time-domain. In combination with (Fast-) Fourier Techniques this method can compute a wide-band frequency response from a single time domain simulation.

In Finite Integration Methods the structure under consideration is discretised to a grid. Instead of applying finite differences, integrals are applied on the grid.

In the Method of Moments (MoM) normally unknown charge and current densities act as a source for the electric- and magnetic field. By enforcing weighted forms of boundary conditions for the electromagnetic field, the unknown discretised charge and current densities are computed. This method normally results in dense matrices. This poses serious limitations in case of a large number of unknowns where solve times and memory usage increase dramatically. It is however very well suited for the analysis of microwave circuits with strip-type connections.

In the Transmission Line Method (TLM) the structure is again discretised in a grid of nodes. Neighbouring nodes are connected with each other by transmission lines, based on the equivalence of Maxwell’s equations and the equations for wave propagation on transmission lines.
In this thesis two software packages are considered for solving Maxwell's equations. The first package is Agilent's High Frequency Structure Simulator HFSS (version A.04.06). A structure is represented by a collection of solids created by a solid modeller. The finite element method is used to solve for the electric field and the magnetic field in the structure. A post-processor is applied to manipulate the field solutions. Although this package has several capabilities, there are serious drawbacks. The major drawback found are the large memory usage and the long computation times, even for relatively simple structures. It is noted however that in later versions serious improvements have been made both in computation time and memory usage.

The second package is Em from Sonnet Software (version 4.0a). A metallisation pattern in a boxed structure with multiple dielectric layers is defined using the a modeller (xgeom). A Method of Moments (MoM) approach (cf. [24], [25]) is used to compute current densities and the charge density on the metallic pattern. The metallisation is assumed infinitely thin, losses are accounted for in an approximate manner. The programme can also account for dielectric bricks, but using this option in cases relevant to this work led either to unsatisfactory results or failures due to insufficient RAM memory. Within MDS a package similar to Sonnet's Em is available under the name Momentum also using the Method of Moments.

2.7.3 Static fields

The dimensions of the power transistor are on the order of millimeters. For larger power transistor dimensions can go up to a few centimeters. The frequency of operation in case of base station amplifiers is around 900 Mhz and 1800 Mhz. The electrical wavelength in free space $\lambda$ is found from dividing the speed of light in free space by the frequency. Doing this the corresponding wavelengths are around 33 and 17 centimeter respectively. In other words the physical dimensions of the power transistor are small compared to the wavelength. This allows a simplification of Maxwell's equation to static equations [22]. In the limit of static fields Maxwell's equations reduce to:

$$-\nabla \times \mathbf{H} + \mathbf{J} = -\mathbf{J}^e \quad (2.15)$$

$$\nabla \times \mathbf{E} = 0 \quad (2.16)$$

and the compatibility relations are now given by:

$$\nabla \cdot \mathbf{J} = -\nabla \cdot \mathbf{J}^e \quad (2.17)$$

$$\nabla \cdot \mathbf{E} = 0 \quad (2.18)$$

The electric field is irrotational and the gradient of a potential function $\Phi$ ($V$) is introduced:

$$\nabla \times \mathbf{E} = 0 \Leftrightarrow \mathbf{E} = -\nabla \Phi \quad (2.19)$$

Substituting the constitutive relation for the volume density of electric current, equation (2.10), in the compatibility relation, equation (2.17), it follows that:

$$\nabla \cdot \sigma \mathbf{E} = -\nabla \cdot \mathbf{J}^e \quad (2.20)$$

In regions of uniform conductivity this equation reduces to:

$$\sigma \nabla^2 \Phi = -\nabla \cdot \mathbf{J}^e \quad (2.21)$$
By introducing an external volume distribution of current sources \( \nabla \cdot \mathbf{J}^e = s^e \) (A/m\(^3\)) (see also [22], section 7.3) it follows that:

\[
\sigma \nabla^2 \Phi = -s^e
\]  

(2.22)

This is Poisson's equation for electrical conduction. If a volume density of unpaired electric charge exists in a medium filled with a perfect dielectric, having permittivity \( \varepsilon \), equation (2.9) is given by:

\[
\varepsilon \nabla^2 \Phi = -\rho
\]  

(2.23)

This is Poisson's equation for electrical charge. It is observed that Poisson's equation for electrical conduction, equation (2.22), has the same form as Poisson's equation for charge, eq. (2.23). In Poisson's equation for charge the volume density of electrically unpaired charge is the source for the electric field. In equation (2.22) the external volume distribution of current sources is the source for the electric field and the volume density of electric charge is computed from equations (2.11) and (2.9)

From the photos of the power transistor (figure 2.2) it is observed that most parts are decomposable in a number of rectangular blocks. Both the die and the prematch capacitor are rectangular blocks. The leadframe of the package can be viewed as a set of conductive blocks mounted on a rectangular block of beryllium oxide. Prescribed boundary conditions can often be formulated for these blocks. For example the current flow through a number of sides of the prematch capacitor is zero. Two types of conditions at a boundary are used in this work:

1. Dirichlet boundary condition.
   - The value of the potential is specified on the boundary or zero by default.
2. Neumann boundary condition.
   - The value of the normal derivative of the potential is specified on the boundary or zero by default.

It follows from the uniqueness theorem [26] for the solution of Poisson's equation that the potential function \( \Phi \) can be fully determined aside from a constant. This constant is zero if a Dirichlet boundary condition is used.

### 2.7.4 Modelling elements

Passive circuit elements can be defined in terms of the solution of Maxwell's equations using low frequency approximations to these equations. These elements are the resistor, the capacitor and the inductor. They form the building blocks for more complex models. Below the concept of resistance and conductance is discussed and additionally transmission line elements are introduced. The discussion of the concept of capacitance and inductance follows the same lines. Please note that this section does not give a full coverage of the subject, the reader should refer to textbooks such as [22] for an in-depth treatment.

### Resistance and conductance

The definition of the resistor is based on the solution of Poisson's equation for electrical conduction, eq. (2.22). Consider the configuration of figure 2.4.
Two domains are located in homogeneous medium with conductivity $\sigma$. In the first volume a distribution of current sources $s_1^e$ exists and in the second volume a volume distribution of current sources $s_2^e$ is present. Integration over the first volume of $s_1^e$ yields the current $i$ and it is assumed that integration of $s_2^e$ over the second volume yields the current $-i$. With the volume distribution of current sources $s^e = s_1^e + s_2^e$ equation (2.22) is solved, aside from a constant, for the potential distribution. Next the potential difference between the two domains is computed. Note however that in general the potential is not constant inside the two domains. Several options are available to compute a voltage difference. The first option is to pick a point inside each volume and to use the difference of these two potentials as the potential difference of the two domains. In case of spheres and bricks for example it is customary to use the potential at the center of the domains. As shown in section 2.10 it is possible, through the use of Green's functions, to compute the voltage directly at specified points without computing the potential distribution in the whole domain first. A second option is to compute a weighted form of the potential, such as integrating the potential over the volume and dividing the result by the volume. Normally the drawback with this option in the implementation of models is the additional computational effort needed to integrate the potential distribution over the volume. Once the potential difference $(\Phi_1 - \Phi_2)$ between the two domains is defined, the resistance follows as $R = (\Phi_1 - \Phi_2) / i$. The conductance is the inverse of the resistance: $G = 1/R$.

In case more than two current injection domains are present (cf. figure 2.4), resistance- and conductance matrices are introduced. The definitions of these matrices for an N-terminal system are:

$$\mathbf{v} = \mathbf{R} \mathbf{i} \quad \mathbf{i} = \mathbf{G} \mathbf{v} \quad \mathbf{R} = \mathbf{G}^{-1} \quad (2.24)$$

where $\mathbf{v}$ is an array of voltages associated with each volume and $\mathbf{i}$ is an array of currents associated with current leaving each volume. In principle each element of the resistance matrix is computed by setting the current flowing from a domain to the surrounding to 1
Ampere and observing the potentials in the other domain:

\[ R_{ij} = \frac{U_i}{I_j} \quad I_k = 0, k = 1 \ldots N, k \neq j \quad (2.25) \]

Please note that a reference potential must be defined in case a unique solution for the potential from equation (2.22) and the additional boundary conditions does not exist. This is achieved for example by specifying that the potential at a point in one of the domains is 0 Volts. A detailed description of this procedure is given in section 2.10 (cf. eq. 2.38).

Please note that it is also possible to define a net of \( N \times (N - 1)/2 \) lumped resistances between the domains. The direct computation of these resistances however is cumbersome since the procedure outlined in figure 2.4.a can not be used to compute each component of this net separately. With Green’s functions however it is possible to compute each element of the resistance matrix separately.

**Transmission lines**

A single transmission line is characterised by a complex impedance \( Z_L \), a complex propagation constant \( \gamma \) and the line length \( l \) [27]. These quantities are normally found by solving a two-dimensional Helmholtz equation for the propagation constant. The propagation constant is then back substituted to find the electric and magnetic field distributions. The impedance is computed from these field distributions. Note that, in general, several definitions for the impedance exist based on power, voltage and current (cf. [28]). The propagation constant is split into an attenuation constant \( \alpha \) (Np/m) and a phase constant \( \beta \) (rad/m). It is further customary to introduce a longitudinal impedance per unit length \( Z \) (\( \Omega/m \)) and a transversal admittance per unit length \( Y \) (S/m) as shown in figure 2.5.

![Diagram of a transmission line](image)

Figure 2.5: A transmission line with characteristic impedance \( Z_L \), propagation constant \( \gamma \) and length \( l \) (left). An equivalent circuit for a small piece of line \( \Delta z \) with an impedance \( Z \) and admittance \( Y \) per unit length. The equivalent circuit is further refined with a resistance \( R \), inductance \( L \), capacitance \( C \) and conductance \( G \) per unit length.

The transmission line impedance and propagation constant are related through these quantities through \( Z_L = \sqrt{Z/Y} \) and \( \gamma = \sqrt{ZY} \) respectively. For many (quasi-)TEM transmission lines, the model can be further refined by introducing an inductance \( L \), resistance \( R \), capacitance \( C \) and conductance \( G \) per unit length. The equivalent circuit for a small piece of transmission line is shown in figure 2.5. The impedance per unit length is found as \( Z = R + j\omega L \) and the admittance per unit length as \( Y = G + j\omega C \). Transmission line equations are used in this thesis for the electrical modelling of a single line above a ground plane (cf. section 3.2.1) and to model one dimensional heat transfer in solids (cf. section 4.3).

In case of multiple coupled lines the situation is more complex. For all aforementioned
quantities matrix representations are used. In the implementation of transmission line models in MDS the method outlined in [29] is used. First the inductance-, capacitance, resistance- and conductance matrix are computed. Next the impedance- and admittance-matrices are computed. Eigenvalue and eigenvectors are computed using the software package EISPACK available in the netlib repository [30]. Please note that EISPACK has been superseded for the most part by LAPACK, also available at the netlib repository. Lossless cases should be treated with care since they can give numerical problems which may be avoided by introducing small losses i.e. for both the resistance and conductance matrix the diagonal elements are made slightly positive.

### 2.8 Modelling of the die

Key components in power transistors are the active areas i.e. the die. The main focus of this thesis is on the modelling of the passive elements of power transistors however. The thesis of R. Tinti gives an in-depth treatment of modelling of the active part [31]. Nevertheless, a brief overview of the modelling of the die is given here for reasons of completeness.

In this work the active element is considered as a blackbox with given relations between the external nodes of the blackbox. In other words, this work does not concentrate on finding correct models for the active device. It is noted however that in the electrical simulator a model must be available for the active element. The model must fulfill two requirements however:

- Electrical relations between the currents and voltages at the nodes must be known and computable.
- In active elements where temperature is of importance a thermal node must be available to connect to a thermal model.

The main idea is that the models of the passive elements introduced in this work can be used for any given technology. Then for each technology a model for the die must be derived. Combining the model of the die with the passive and thermal models results in a full model of the power transistor.

It is noted that once a technology is chosen, the model for the active element must be available. This model can be based on measurements, compact model equations or device simulations. In the first case, a representative transistor is measured at different bias levels and at different input power levels with various loads. All measured data is stored in a dataset which is used by the electrical simulator to retrieve relevant currents and voltages. This is the dataset approach discussed in section 2.3. In the second approach, a model is used or derived describing the electrical behaviour of (a part of) an active area as function of several parameters. These parameters are found from for example measurements or from process parameters (doping profile, dimensions etc.). These models are collectively referred to as "compact transistor models". In the third approach the process parameters form the input for a device simulator. The device simulator solves for voltages and currents. Normally a device simulator can handle a very small part of an active area only, say one or two emitter fingers. A prerequisite for this approach is that the device dimensions and the process parameters are available. In case of the BLV 910, the process info available was not accurate enough to achieve reliable device simulations results. Additionally, going from device simulations of a small part of the die to a full model of the die is not a trivial task because simply upscaling the
results ignores mutual effects and the effects at the boundaries of the active areas. This approach is not pursued here. Nevertheless, it is strongly recommended to explore possibilities of twodimensional and threedimensional device simulations in an MDS like environment.

In this work a compact transistor model is employed to model the active element. For reasons of completeness, a brief discussion of the compact model employed in this work is given in the next few pages. Once again it is noted that the principle aim of this work is to find a modelling strategy for the passive elements of power transistors. Building a good compact model of active elements is a task in itself.

Compact bipolar transistor models

The active element of the BLV 910 is a single silicon die with eight active areas. Various compact models are able to model the behaviour of silicon bipolar transistors. The most commonly used models are:

- The Ebers-Moll model [32]
- The Gummel-Poon model [33]
- The VBIC95 model [34]
- The HICUM model [35], [36]
- The Mextram model [18]

The Ebers-Moll model is generally considered as the first standard model used in common. The main advantages are the simplicity of the model and short calculation times. The drawback is that various effects important for power transistors are not included in the model.

The Gummel-Poon model is widely used in the present industrial environment. The model accounts for various important effects combined with a moderate model complexity. The major drawback related to power transistors are the poor temperature scaling and the incomplete modelling of quasi-saturation effects.

The last two models are considered advanced models in terms of accurate modelling of complicated physical phenomena. An advantage of the VBIC95 model is that it reduces to the Gummel-Poon model when some parameters are omitted. Compared to the Mextram model there are some shortcomings however (cf. [37] and [38]).

The Mextram compact transistor model

In this work the Mextram model is used because a long list of physical phenomena is modelled using a physics-based formulation. Additionally, the model incorporates a set of temperature scaling rules. These rules are a prerequisite for the electro-thermal modelling of the power transistors employed in this work. Also the equations, the C-code and a parameter extraction procedure for the model are available in the public domain [39], [40]. Finally, the Mextram model was implemented successfully in MDS by Delft University of Technology. Consequently, a lot of knowledge about the model and about adding a thermal node to the model is available there. Additionally, debugging the model and solving convergency problems is directly possible as the source code of the model in MDS is available. For reasons of completeness the equivalent circuit of the Mextram compact model is shown in figure 2.6.

In the figure four external nodes are shown: Emitter (E), Base (B), Collector (C) and Substrate (S). Additionally, five internal nodes are visible: E1, C1, C2, B1 and B2. Implementing this model in MDS basically requires the charges and the currents as function of the node voltages and their derivates with respect to the voltages. All these equations are freely available [39].
Using the C-code available in the public domain [39] the model can be implemented without too much effort in any MDS type of simulator.

**Mextram parameter extraction of the BLV 910**

For reasons of completeness the extraction of the Mextram parameters for the BLV 910 is discussed in brief here. For an in-depth treatment the reader should refer to [31]. Two sets of parameters are required:

1. Electrical parameters.
   These parameters interrelate electrical quantities such as charge, capacitance, voltage and current. These parameters are normally extracted under small signal conditions at a single temperature.

2. Thermal parameters.
   These parameters interrelate temperature and the electrical quantities i.e. these parameters “scale” the electrical parameters for temperature. The thermal scaling parameters are found by measuring electrical parameters at differing temperatures.
In principle the parameters should be extracted for a set of transistors having different areas. From the results the area scaling rules are verified i.e. it is concluded whether the parameters scale correctly with the area.
In case of the BLV 910 the smallest cell available is one active area. On a die with 8 active areas connections from the bonding pads to seven active areas are lasered away. One cell is left connected to the bondpads. The die is placed on a ceramic substrate and bondwires are properly connected.
Using this setup it is possible to extract both the electrical parameters of a single cell. By placing the ceramic substrate on a thermal chuck and extracting relevant electrical parameters at differing temperatures, the temperature scaling parameters are found. An in-depth treatment of the parameter extraction of the BLV 910 parameters is given in the thesis of R. Tinti [31].

**Problem statement**

Given the fact that a compact transistor model is used in the modelling of the die, several problems arise. First of all a temperature node must be added to the compact transistor model to allow a fully dynamic electro-thermal simulation. In other words, at every iteration made by the simulator the temperature and all temperature related equations are evaluated on top of the normal evaluations. Fortunately, this implementation proved successful [31].
The second question is how to perform the parameter extraction. In principle this extraction should be performed on a small part of an active areas. The extraction should then be repeated on a larger part to check the correctness of the area scaling.
Then the question is how to model all the active areas of a power transistor, like the BLV 910, using a compact bipolar transistor model such as Mextram. Is one compact transistor model enough to model the full die? Considering temperature effects and the temperature profiles within an active area it is not likely that one compact model suffices. Then the question comes up how many compact models, each having it's own temperature node, are needed to represent an active area.
The remaining question is whether the model for the die in combination with the passive models and the temperature models is able to correctly describe the DC-, RF small signal and RF large signal behaviour.

### 2.9 Thermal modelling

The electrical behaviour of a power transistor is substantially affected by temperature, so that a good thermal model for the transistor is imperative. The main portion of the heat is generated at the junctions of the transistor in the active areas and transferred through the silicon of the die and the beryllium oxide to the mounting base. In this section a short discussion of mechanisms of heat transfer in power transistors is given, followed by the heat conduction equation. This section ends with a review of methods reported in the literature for modelling the thermal behaviour of electronic devices.

#### 2.9.1 Mechanisms of heat flow

The heat generated in the active areas must be transferred to the surroundings. There are three mechanisms of heat transport:

The thermal modelling in this work focuses on heat conduction since the main portion of heat is conducted from the junctions through the silicon to the package. It is further conducted through the package to the mounting base. The mounting base is mounted on a cooling block, the heat sink, which is normally cooled with water or by forced air flow. The final aim of the temperature study is to build a thermal model needed for the electrothermal modelling and to compute the temperature distribution within the active areas, because the temperature of these areas affects the electrical behaviour.

2. Heat convection.

Within the power transistor there is a small amount of heat convection, but this effect is assumed negligible in this work. Another place where convection takes place is in the cooling of the power amplifier heat sink. In the models introduced in this work, the reference temperature is defined at this heat sink. If forced water cooling with temperature control is used to keep the heat sink at a specified temperature, that temperature is the reference temperature. If the mounting base is mounted on a cooling block, cooled by forced air, heat is transferred through convection. In that particular case the reference temperature is the temperature of the surrounding air and the temperature of the heat sink should be calculated with the aid of convection equations.


A small amount of heat is radiated by power transistors, but the effect of radiation on the temperature is assumed negligible. Note however that heat radiation is used to measure temperature distributions at the surface of a transistor with infrared camera’s.

Initial rule of thumb calculations indicate that less than 5% of the heat is transferred through convection and radiation and the remaining 95% is transferred through heat conduction.

2.9.2 The heat conduction equation

The thermal modelling starts with the introduction of the governing differential equation which is based on the application of Fourier’s law of heat conduction to the energy equation (cf. [41], [42]):

\[
\frac{\partial}{\partial x} \left( \kappa \frac{\partial T}{\partial x} \right) + \frac{\partial}{\partial y} \left( \kappa \frac{\partial T}{\partial y} \right) + \frac{\partial}{\partial z} \left( \kappa \frac{\partial T}{\partial z} \right) + g(x, y, z, t) = \rho c \frac{\partial T}{\partial t} \tag{2.26}
\]

where \(x, y, z\) are the Cartesian coordinates (m) and \(T\) is the temperature (K). The parameters of the body are the thermal conductivity \(\kappa\) (W/m·K), the specific heat \(c\) (J/kg·K) and the material density \(\rho\) with units kg/m\(^3\). The rate of energy generation per unit volume is given by \(g(x, y, z, t)\) (W/m\(^3\)).

The thermal conductivity and the specific heat are of particular interest since for the materials involved the values are strongly dependent on temperature. In this work, the effect of the temperature dependent thermal conductivity is accounted for by transforming equation (2.26) to an almost linear equation using Kirchhoff’s transformation (cf. section 4.2). In the case of steady state conduction this equation becomes a linear equation. The solution of this linear equation is then transformed back to the non-linear solution. Please note that the value of the specific heat increases with temperature for both silicon and beryllium oxide. To simplify the discussion these values are now assumed independent of temperature.
Since the non-linearity of the thermal conductivity is taken into account using Kirchhoff's equation, the problem of a temperature independent thermal conductivity remains. In this case equation (2.26) is rewritten as:

\[
\frac{\partial^2 T}{\partial x^2} + \frac{\partial^2 T}{\partial y^2} + \frac{\partial^2 T}{\partial z^2} + \frac{g(x, y, z, t)}{\kappa} = \frac{1}{\alpha} \frac{\partial T}{\partial t}
\]

(2.27)

where \(\alpha = \kappa / \rho \cdot c\) is the thermal diffusivity (m\(^2\)/s). Although not discussed in this thesis, a model is implemented solving equation (2.27) for an array of heat generating volumes with the assumption of uniform heat generation in each of these volumes.

If heat flow takes place in one direction, e.g. the \(z\)-direction, this equation reduces to a one-dimensional differential equation:

\[
\frac{\partial^2 T}{\partial z^2} + \frac{g(z, t)}{\kappa} = \frac{1}{\alpha} \frac{\partial T}{\partial t}
\]

(2.28)

The solution of this particular case in the frequency domain is considered in section 4.3. An RC transmission line is used to model the one dimensional heat flow.

Since the thermal time constants are much larger than the cycle time of the RF signal the variation of temperature in time is negligible i.e. in the \(\partial T / \partial t \approx 0\). The heat conduction equation, equation (2.27), reduces to the Poisson equation:

\[
\frac{\partial^2 T}{\partial x^2} + \frac{\partial^2 T}{\partial y^2} + \frac{\partial^2 T}{\partial z^2} = -\frac{g(x, y, z, t)}{\kappa}
\]

(2.29)

In this case changes of the source distribution in time are followed instantaneously by temperature. Note the equivalence between Poisson's equation for heat and the equations for electrical conduction, equation (2.22) and the equation for charge, equation (2.23). This equivalence can be used to implement a model for electrical conduction and use this model in the modelling of heat conduction.

### 2.9.3 Literature survey

Before going into detail how the thermal modelling is set up, first a brief overview is given of references available in this area. The amount of literature related to (electro-)thermal modelling for electronic devices and integrated circuits is rather extensive. Because it is a difficult task to discuss all available references a brief selection is reviewed. The first important article is by Joy and Schlig [43]. Their starting equation is the time-dependent heat conduction equation, equation (2.27). The temperature dependency of the thermal diffusivity \(\kappa\) is not considered. A brick shaped heat source is assumed and located either in a homogeneous medium or above an adiabatic surface (surface without heat flow through the surface). Green's function in the time domain is introduced representing the temperature as function of time due to an instantaneous point source. More details of this method are given in section 2.10. This Green's function is integrated over the volume of the heat source resulting in an expression for the temperature as function of place and time. The expression contains a convolution integral involving the time dependency of the heat generated in the heat source. The convolution equation is then applied to a broad range of cases. Although this article
is not directly applicable to the problem at hand it gives a good introduction to the thermal modelling of electronic devices.

In the second article by Gao et. al. a thermal design study of high-power heterojunction bipolar transistors is presented [44]. In this article several heat sources are located at the surface of a block of material. An expression is given for the temperature at this surface where the temperature dependent thermal conductivity is included in the equation in an approximate fashion. More important, the effect of temperature is included in the electrical equations. Unfortunately both the thermal modelling approach and the electrothermal modelling can not be applied directly to the problem at hand. Nevertheless, it shows the direction of investigation required for this type of modelling.

The third article discussed here is by Zweidinger et. al. where the compact modelling of BJT self-heating in SPICE is considered [45]. The article starts with the solution of the time-dependent heat conduction equation, equation (2.27), given by Joy and Schlie. The solution is transformed to the frequency domain and the special case of zero frequency is considered. Based on this equation an approximate equation is introduced for the thermal resistance of a brick shaped heat source. The electrical equations of the Gummel-Poon model containing temperature are reviewed followed by a discussion of the modelling algorithm implemented in SPICE. The modelling is applied to some circuit examples but unfortunately the presented results are very brief and a bit difficult to follow. Nevertheless, the article shows what is needed to implement electro-thermal modelling in a simulator like SPICE.

The last article considered is by Snowden [46]. In this article a large-signal microwave characterisation of AlGaAs/GaAs HBT's is made based on a physics-based electro-thermal model. First a compact electrical model is derived. This model is coupled to a thermal model which is based on a "new thermal resistance matrix scheme". Basically, a thermal resistance matrix is computed relating temperature at a point to the dissipations in the bounded volumes of the junctions. Reported calculation times for a thermal matrix are in the order of 30 minutes. The method is also used in this thesis (cf. section 4.6), but calculation times are in the order of seconds.

The electrothermal model is applied to the large-signal modelling of AlGaAs/GaAs HBT's going to RF powers of around 500 mW. Although package effects are not included in the analysis and the RF power is less than a Watt, is clearly shows that physics-based electro-thermal modelling is a viable option.

This thesis brings the electro-thermal modelling further:

1. The thermal models derived in this work use analytic expressions which can be evaluated very rapidly. Thermal matrices are evaluated in the order of milliseconds where the expressions given by Gao et. al. involve more difficult to evaluate summations.
2. Instead of the Gummel Poon model, used by Zweidinger et. al. [45] a much more advanced compact model is used, the Mextram model. The Mextram model has an elaborate set of better temperature scaling rules. Additionally, the model has a good modelling of distortion behaviour.
3. Instead of implementing the non-linearity of the thermal conductivity in the thermal model itself, this effect is separated from the linear thermal modelling using Kirch-
hoff’s transformation.

4. All three articles discussed above only consider an heat source in a homogeneous medium. In this work a considerable amount of work is devoted to modelling of the effect of a multilayered substrate.

5. The thermal modelling is not only applied to a more or less theoretical circuit example as in [45], but it is applied in full to a power transistor.

2.10 Integral equation, Green’s functions and Matrix Methods

In previous sections it is shown that the equations governing the electrical and the thermal behaviour reduce to Poisson’s equation in specific cases. There are several methods to solve Poisson’s equations: local methods such as finite difference and finite element methods, and global methods such as the integral equation method. Although local methods offer several advantages, such as ease of implementation of numerical schemes and the ability to account for strongly inhomogeneous media, a global method is used in this thesis for several reasons. First of all, the structures under consideration are simple homogeneous structures, in many cases they are brick shaped. Secondly, an integral equations leads to models with short computation times in the case of simple structures with a limited number of ports. Thirdly, the models require only a small amount of memory. In the thermal modelling of transistors in [47] for example a net of thermal resistors and capacitors is build to model a low frequency power transistor. For larger structures and fine discretisations, excessive memory usage is reported. Similar observations are made in this work (cf. section 4.6.2). In the following the implementation of a model for electrical conduction, based on integral equations, and the treatment of interface and boundary conditions is considered. Note that this model is also used to model the thermal behaviour of the power transistor.

2.10.1 Integral equation

In power transistors several brick shaped structures are found. As an example, consider the structure of figure 2.7 on the left.

![Figure 2.7](image)

Figure 2.7: On the left a rectangular block with four areas where current is injected into the block. Boundary conditions are applied to all six faces of the block. This is a particular case of the general case shown on the right: a domain with volume $V$ with boundary $S$ and normal to the surface $n$ pointing outward.

In this figure a rectangular block of conducting material with four current injection domains is shown. Models for situations similar to this example are used to model current flow in the
die, in the prematch capacitor and in the package. It is also used to model heat transfer in the
power transistor.

The general case is shown in the same figure on the right: electrical conduction in a domain $D$
with volume $V$ bounded by a surface $S$ with a normal $\mathbf{n}$ pointing outward. The electrical
conduction is governed by Poisson’s equation, eq. (2.22). This equation is converted to an
integral equation by introducing a Green’s function satisfying:

$$
\nabla^2 G(x,y,z|x',y',z') = -\delta(x-x')\delta(y-y')\delta(z-z')
$$

(2.30)

Applying Green’s second identity to the volume $V$ and using equations (2.22) and (2.30), the
potential at a point $(x,y,z)$ is given by:

$$
\Phi(x,y,z) = \frac{1}{\sigma} \int_V G(x,y,z|x',y',z') s^e(x',y',z') dV' 
+ \oint_S \left( G(x,y,z|x',y',z') \frac{\partial \Phi(x',y',z')}{\partial \mathbf{n}} \right) dS' 
- \oint_S \left( \Phi(x',y',z') \frac{\partial G(x,y,z|x',y',z')}{\partial \mathbf{n}} \right) dS'
$$

(2.31)

The voltage at a point $(x,y,z)$ is the sum of an integral over the volume $V$ and two integrals
over the surface bounding the volume.

Throughout this work the main focus is on situations as depicted in figure 2.7 on the left,
where on all six faces a Neumann boundary condition is applied or on one face a Dirichlet
condition and on the other faces Neumann conditions. For these cases Green’s functions are
easily derived. The important point to note is that in these cases it can be easily shown and
envisaged that the two surface integrals in equation (2.32) vanish. Therefore it is assumed in
the following that the two surface integrals vanish, reducing equation (2.31) to:

$$
\Phi(x,y,z) = \frac{1}{\sigma} \int_V G(x,y,z|x',y',z') s^e(x',y',z') dV
$$

(2.32)

stating that the potential is a convolutional volume integral of Green’s function and the source
distribution. The volume distribution is expanded into a set of known expansion functions $E$:

$$
s^e(x,y,z) = \sum_{j=1}^{l} M_j E_j(x,y,z)
$$

(2.33)

By substituting eq. (2.33) in eq. (2.32) the following integral is obtained for the potential
distribution:

$$
\Phi(x,y,z) = \frac{1}{\sigma} \sum_{j=1}^{l} M_j \int_V G(x,y,z|x',y',z') E_j(x',y',z') dV'
$$

(2.34)

With this equation the potential anywhere in the volume $V$ is computable provided that the
Green’s function is known, the expansion (equation (2.33)) correctly represents the source
distribution and the integral is solvable. In some specific cases a weighted form of the poten-
tial is required and not the potential function itself. By introducing the weighting function
$W(x,y,z)$ and integrating the potential multiplied by the weighting function, the weighted potential is given by

$$\int_V W(x,y,z)\Phi(x,y,z)dV = \int_V W(x,y,z)$$

$$\sum_{j=1}^J \frac{1}{\sigma} \int_V G(x,y,z|x',y',z')E_j(x',y',z')dV'dV$$

(2.35)

This equation is used to compute the resistance matrix of a structure with $N$ current injection volumes in a brick of conducting material. The case with four brick shaped injection volumes is depicted in figure 2.7. The volume and the surface of the block are denoted by $V$ and $S$ respectively and Neumann boundary conditions are applied at all six faces by introduction of the appropriate Green’s function. A uniform volume distribution of current sources is assumed for each injection volume $V_i$ and the voltage is computed at the centers $(x_i,y_i,z_i)$ of the injection volumes i.e. a Dirac delta function is the weighting function in equation (2.35). Although the second surface integral of equation (2.31) vanishes in this specific case, the normal component of the potential is unknown. To avoid this problem, a reference volume is selected and all potentials are referenced to this volume. Suppose volume $N$ is chosen as the reference volume. If a current is injected in a volume $j$ it returns through the conducting medium into the reference volume $N$. If a current of 1 A is injected in a volume $j$ and returns through the reference the source distributions are given by:

$$s_j^x(x,y,z) = \begin{cases} 1/V_j & \text{if } (x,y,z) \text{ in } V_j \\ 0 & \text{other cases} \end{cases}$$

$$s_j^z(x,y,z) = \begin{cases} -1/V_N & \text{if } (x,y,z) \text{ in } V_N \\ 0 & \text{other cases} \end{cases}$$

(2.36)

An element of the resistance matrix $R_{ij}$ is found by first computing the voltage at the center $(x_i,y_i,z_i)$ of observation volume $V_i$ due to the source distributions in the volume $V_j$ and the reference volume $V_N$. The voltage at the center $(x_N,y_N,z_N)$ due to the same current distributions is subtracted from this voltage:

$$R_{ij} = \frac{1}{\sigma} \int_V G(x_i,y_i,z_i|x',y',z') \left[ s_j^x(x',y',z') + s_j^z(x',y',z') \right] dV'$$

$$-\frac{1}{\sigma} \int_V G(x_N,y_N,z_N|x',y',z') \left[ s_j^x(x',y',z') + s_j^z(x',y',z') \right] dV'$$

(2.37)

Substituting the source distribution (2.36) in equation (2.37) an element of the resistance matrix is given by:

$$R_{ij} = \frac{1}{\sigma V_j} \int_{V_j} G(x_i,y_i,z_i|x',y',z')dV' - \frac{1}{\sigma V_N} \int_{V_N} G(x_i,y_i,z_i|x',y',z')dV'$$

$$-\frac{1}{\sigma V_j} \int_{V_j} G(x_N,y_N,z_N|x',y',z')dV' + \frac{1}{\sigma V_N} \int_{V_N} G(x_N,y_N,z_N|x',y',z')dV'$$

(2.38)

Note that the surface integrals vanish, the integration constant in Green’s function vanishes and the resistance elements are computed from four volume integrals.
Consider again a block of material with \((N - 1)\) brick shaped current injection volumes. At five faces Neumann boundary conditions are applied and at the sixth face a Dirichlet boundary condition is applied. This face is the \(N\)-th reference terminal. First the appropriate Green’s function is found with the Dirichlet condition \(\Phi = 0\) at the sixth face. In this particular case elements of the resistance matrix, are directly computable:

\[
R_{ij} = \frac{1}{\sigma V_j} \int_{V_j} G(x_i, y_i, z_i; x', y', z') dV'
\]  
(2.39)

The above derivation and discussion clearly demonstrates how a physics based model can be derived and defined in a form suitable for implementation in an electrical simulator.

To allow for changes in voltage of the reference terminal the \((N-1)\times(N-1)\) resistance matrix is inverted to obtain a \((N-1)\times(N-1)\) definite admittance matrix. To include the reference node in the admittance matrix the relation for an indefinite \(N\) terminal network is used:

\[
\sum_{i=1}^{N} Y_{ij} = 0 \quad j = 1, \ldots, N \quad \text{and} \quad \sum_{j=1}^{N} Y_{ij} = 0 \quad i = 1, \ldots, N
\]  
(2.40)

to compute the last row and last column of the admittance matrix. There is an additional point to note. In MDS quite often parameter sweeps are performed. One parameter is swept while the other parameters remain constant. For example the \(x\)-coordinate of the center of a volume is swept to compute the potential distribution along a line. If a volume has changed only one row and one column in the impedance matrix, corresponding with the changed volume, need to be recomputed. Implementing this option reduces computation times considerably.

### 2.10.2 Green’s functions

As stated above Green’s functions play an important role in integral equations. Quite a problem is solved elegantly once the Green’s function is derived for the problem at hand. For reasons of completeness below a brief discussion is given of the Green’s functions used in this work. Starting point is equation (2.30):

\[
\nabla^2 G(x, y, z; x', y', z') = -\delta(x - x')\delta(y - y')\delta(z - z')
\]  
(2.41)

The Green’s function for this problem is given by:

\[
G(x, y, z; x', y', z') = \frac{1}{\sqrt{(x-x')^2 + (y-y')^2 + (z-z')^2}}
\]  
(2.42)

This Green’s function describes how the static potential is distributed in a homogeneous medium with a Dirac delta source located at \((x', y', z')\) (see previous section). The same Green’s function describes in case of static heat conduction temperature is distributed. The above Green’s function applies to the case of an infinite homogeneous medium.

In practical situations boundary or interface conditions are present however. Examples of these conditions are a plane at constant temperature, a plane without heat transfer through it or a plane forming the interface between two materials. Several methods exist to include these conditions in the Green’s function i.e. the Green’s function satisfies also the additional boundary or interface conditions. Two of these methods are illustrated in figure 2.8 because they are used throughout this work: imaging and series expansion.
Figure 2.8: On the left the principle of imaging is shown. A source is shown and at a plane zero potential is required. The plane is removed and replaced by an opposite source located at the other side of the plane.

Shown on the right zero potential is required at two planes located a certain distance apart. To satisfy these conditions a series expansion in sine terms is applied for the Green’s function. Three of these terms are shown in the figure.

In the imaging method, the boundary condition is replaced by imaging the source in the boundary plane. One can imagine that in the Green’s function for this problem two terms similar to eq. (2.42) enter: one for the source and one for its image.

In the second example two boundary conditions are applied. One can imagine that to satisfy these two conditions an infinite series of sines enters the Green’s function. This method is used to derive the Green’s function for heat conduction through a multilayer substrate (cf. equation (4.34)).

2.10.3 Interface conditions

At the interface between two media the interface conditions must be satisfied (cf. equations (2.13) and (2.14)). In case of conduction problems these interface conditions are equality of the potential and continuity of the normal component of the flux. As an example consider the block with four injection volumes shown in figure 2.7 on the left. This block is placed on top of a second block as shown in figure 2.9 on the left. For the upper block at all six faces a Neumann boundary condition is used, current can only enter or leave the block through the injection volumes. At five faces of the bottom block a Neumann boundary condition is used and at the bottom face a Dirichlet boundary is used to satisfy a potential. To enforce the boundary conditions in the area where the two blocks are joined, a grid of current volumes with a very small thickness (panels) is defined at the bottom of the upper block and the top of the lower block. If current flows uniformly into each panel, it can be shown that this current represents the normal component of the flux. The grids at two different blocks are connected together to enforce the flux continuity in an area and the temperature equality at the points of the nodes. In other words, current leaving one block through a panel enters the second block through a panel.

For each block a multiport model must be created, the number of ports being equal to the number of current injection volumes plus the number of panels used to enforce the boundary conditions. As an example consider the case where current is injected into 25 injection volumes and the interface conditions are enforced on a grid of 7 × 7 panels. The model has 74 ports, with a full resistance matrix with with 5476 (74^2) elements.
2.10.4 Method of Moments

This section ends with a short discussion of a method that does not compute the response of a system (e.g., the potential) to a source (the volume distribution of electric sources). Instead the response of the system is known and the sources must be computed. This method is collectively known as the "method of moments" [24]. This method is applied in this work to derive a model for multiple coupled lines (cf. section 3.2.2). The method is also used in Sonnet's Em and Agilent's Momentum (cf. section 2.7.2).

Consider again an unknown volume distribution of current sources $s^e$ in a bounded volume. If the potential is known, the source distribution is directly found from equation (2.22). Two reasons limit the practical use of this approach. First, the potential distribution is not known in the entire volume but only in a part of it. And secondly, from a computational point of view, even if the potential distribution is known, applying the Laplace operator can cause serious numerical problems.

A second method to compute the source distribution is by the "Method of Moments" [24]. First the volume distribution is expanded into a set of known expansion functions (cf. equation (2.33)), with the expansion coefficients $M_N$ to be computed. In a (part of the) volume where the potential function is known, equation (2.34) must be satisfied. This equation normally is not solvable apart from a few trivial cases for several reasons. The first reason is that the potential distribution is not known exactly. The second reason is that the convolution integral of the Green's function with the chosen expansion functions cannot represent the potential exactly. To avoid these problems the potential is weighted and an integral equation (2.35) in $N$ unknowns is obtained. The $N$ expansion coefficients can be found by setting up $N$ linear independent equations. These equations are then solved for the $N$ unknowns.

Examples of the method can be found in [22] and [24]. In this work the method is used to compute the capacitance and inductance matrix of straight coupled lines above a ground plane in sections 3.2.1 and 3.2.2. Sonnet's Em and Agilent's Momentum also employ this method and these packages are used here to compute S-parameter data of the package. The method is further used to compute transmission line parameters of the strips in a multilayered medium to analyse interdigitated capacitors with 40 fingers (48, page 76). The same model
is used in this work in the analysis of the package of the BLV 910 transistor.

2.11 Conclusions

In a feasibility study performed prior to this work it was concluded that the segmentation approach is the most viable approach in modelling power transistors. In this approach the constituent components of a power transistor are modelled separately. The models are then properly connected together to form the full model. The approach is tested using the Philips BLV 910 power transistor. The four components of this transistor are a die, a prematch capacitor, bondwires and a package. To electrically model the passive parts electromagnetic software and private software based on quasi-static equations will be employed. The latter software employs integral equations with the appropriate Green’s function. To model the die the Mextram compact transistor model is used. A thermal node is added to this model to allow for electrothermal interaction. The main heat transfer is through heat conduction from the active areas to the mounting base. Heat convection and heat radiation are found negligible. The heat conduction is modelled using an integral equation with a Green’s function for the problem at hand.
Chapter 3

Electrical modelling of bondwires, matching capacitors and packages

3.1 Introduction

The common components of power transistors are die’s, bondwires, matching capacitors and a package. As stated in the first chapter the modelling approach chosen is to model each component separately and to connect all submodels together to form a full electrical model. The unavailability of electrical models for each of the components in standard microwave simulators is, however, one of the main limitations for computer aided design (CAD) of RF power transistors. In this chapter separate models for the components are introduced. The models are implemented in Agilent’s Microwave Design System (MDS). All models have as input physical constants, spatial dimensions, material permittivities and material conductivities.

In section 3.2, modelling starts with the bondwires. The initial modelling of bondwires is based on the propagation of a TEM wave along a cylindrical transmission line above a perfectly conducting groundplane. Using this initial case it is shown that a line’s inductive or capacitive behaviour is dependent on the terminating impedance. The model of the single line is extended to a model for multiple parallel lines. With the implementation of this model in MDS it is easy to make a zero order estimate of the mutual coupling effect and the effect of terminating impedances. The main advantage of these two models is their accuracy. The main limitation is their inability to model curved wires.

In the third model implemented in MDS the wires are approximated by a set of straight segments whose end coordinates are entered into the model. The model computes the inductance matrix of the coupled wires using Neumann’s inductance equation [49]. This model is verified using rigorous finite element analysis using HFSS and by measurement on single wires and on coupled wires.

The modelling of the prematch capacitors is considered in section 3.3 focussing on relatively long prematch capacitors i.e. capacitors with the length of the contact being substantially larger than the width. The initial model assumes a wave propagation along the length of the capacitor. Based on the results of electromagnetic simulations using Sonnet’s Em, it is shown that the skin effect resistance of the highly conducting silicon effects the model substantially.
This effect is accounted for by modifying the model slightly. Because of the subtle effects it is rather difficult to measure these phenomena directly. It is possible however to compare the model with rigorous electromagnetic field simulations made in Agilent’s HFSS.

In the section 3.4, the electrical modelling of the power transistor package is discussed. The package of the BLV 910 transistor is a SOT 171. Two approaches are pursued: building a model using circuit elements found in the microwave simulator MDS and building a model using electromagnetic software.

Finally several combinations of bondwires and prematch capacitors are placed in the SOT package and small signal S-parameters are measured. To obtain actual geometrical data for the bondwires in the package SEM photos are made of all structures. The measured S-parameters of four different configurations is compared with simulations in the last section.

### 3.2 Modelling of bondwires

Several approaches are used by engineers to model the electrical behaviour of bondwires. In this thesis a few of the approaches are discussed. In the first approach a nearly rigorous model is made by solving Maxwell’s discretised equations. The geometry of the wires is entered in a full 3 dimensional solver and the fields inside the structure are calculated. This principle is illustrated on the left side of figure 3.1 where the geometry of coupled bonding wires in HFSS is shown. This approach is discussed in detail in section 3.2.4.

In the second approach the wires are represented by a set of parallel coupled transmission lines accounting for capacitive and inductive effects. An equivalent circuit for this approach is shown in the middle of figure 3.1. Although this model is not a predictive model for curved wires, it is used to understand the dominant behaviour of the wires and it is used to make analytical calculations. Based on the results of the transmission line model capacitive effects are neglected and only inductive effects are considered in the third modelling approach. Although this model neglects certain effects, it models the dominant inductive effect with short calculation times and low memory usage. This makes the method amendable to the CAD of power transistors.

![Figure 3.1: Modelling of ten bondwires:](image)

(a) with the Finite Element package HFSS, (b) with coupled transmission lines and accounting for capacitive and inductive coupling and (c) coupled inductances accounting for inductive coupling only.

In this section the following consecutive steps are made:

1. A TEM wave propagating along a single round wire above a perfectly conducting groundplane is considered first. This specific case allows the analytical investigation of the behaviour of the line as function of all parameters.
2. This approach is extended to the case of coupled round transmission lines above a ground plane under TEM wave propagation. This model does not account for the curvature of the wires, but it does account for inductive and capacitive coupling. It is shown that if the terminating impedances are sufficiently low, capacitive effects are negligible and the bondwires behave inductively.

3. In the bondwire model introduced next, the capacitive effects are ignored and inductive effects are considered only. Results are computed quickly making the method amendable to application in CAD.

4. To investigate the applicability of the model a comparison is made with full wave electromagnetic simulations performed with Agilent’s High Frequency Structure Simulator (HFSS). Although this simulator gives accurate results, both simulation time and memory usage are prohibitively large for design fast CAD. HFSS can be used however, to benchmark models developed. Limitations to this approach are demonstrated.

5. Finally measurements on a number of bondwire configurations are performed and the inductance extracted is compared with the bondwire model.

### 3.2.1 Single line over a ground plane

An analysis is made of a TEM wave propagating along a single round wire above a perfectly conducting groundplane. The single line model is often used as a model for a single bondwire. This specific case allows the analytical investigation of the behaviour of the line as function of all parameters (wire radius \(r\), wire length \(l\) and height above the groundplane \(H\)).

In figure 3.2 a drawing is shown of the cross section of a cylindrical conductor with radius \(r\) located a distance \(H\) above a ground plane. The line is invariant in the \(z\)-direction.

![Cross sectional view of a round wire above a ground plane](image)

Figure 3.2: Cross sectional view of a round wire above a ground plane. TEM wave propagation is assumed in the \(z\)-direction.

In the analysis of the wire the assumptions are made that the wire and the groundplane are lossless and that a pure TEM wave propagates in the \(z\)-direction along the line. Under these conditions the line is characterised by an inductance per unit length \(L\) (H/m) and a capacitance per unit length \(C\) (F/m). The impedance \(Z_0\) (\(\Omega\)) of the line is \(Z_0 = \sqrt{L/C}\) and the propagation constant is given by \(\gamma = j\omega\sqrt{LC}\).

The determination of the inductance and capacitance per unit length is carried out analytically using conformal mapping techniques ([50], page 444):

\[
C = \frac{2\pi \varepsilon_0}{\text{arccosh}(H/r)} \\
L = \frac{1}{\varepsilon_0 C} = \frac{\mu_0}{2\pi} \text{arccosh}(H/r) \tag{3.1}
\]
For a transmission line with a wire diameter of 50 $\mu$m located 500 $\mu$m above the ground plane the inductance and capacitance per unit length are $L = 0.7377 \cdot 10^{-6}$ H/m $\approx 0.7$ nH/mm and $C = 0.1508 \cdot 10^{-10}$ F/m $\approx 15$ fF/mm respectively, the impedance of the line is 221.1 $\Omega$ and the phase constant is $0.3336 \cdot 10^{-8} \cdot \omega$ rad/m.

The question arises when the line behaves inductively and when it behaves capacitively. The answer to this question is important for our application because ignoring the capacitive effects will simplify the bondwire modelling substantially. To answer the question the wire is short circuit at one end and the input impedance is measured at the other. The input impedance is given by:

$$Z_{in} = Z_0 \tanh(\gamma l) = \sqrt{\frac{L}{C}} \tanh(j \omega \sqrt{LC}l) = j \sqrt{\frac{L}{C}} \tan(\omega \sqrt{LC}l) \tag{3.2}$$

The input impedance of an inductor with inductance $L_{eq}$ is given by $Z_{in} = j \omega L_{eq}$. Comparing this expression with the input impedance of the short circuit transmission line, equation (3.2), shows that the line behaves inductively up to the first resonance frequency where $\omega \sqrt{LC}l = \pi/2$.

This inductive behaviour is independent of the capacitance per unit length. As an example consider the line with $L = 0.7$ $\mu$H/m, $C = 15$ pF/m and $l = 1$ mm. In this particular case the resonance frequency is 77 GHz. Note that the inductance seen at the input of the short circuit line is a function of frequency. Making the small argument approximation $\tan(\omega \sqrt{LC}l) \approx \omega \sqrt{LC}l$, the input impedance of the line is $Z_{in} = j \omega L I$. In this case the equivalent inductance is given by $L_{eq} = L I$. The result of this analysis is unsatisfactory since it shows that the line behaves inductively up to the first resonance independent of the capacitance per unit length. Measuring the line in a two port configuration and considering either the impedance parameters or admittance parameters does not solve this problem since:

- A shunt capacitor can not be represented with two-port admittance parameters. For that reason it is not possible to conclude that the line behaves as a (shunt) capacitance.
- A series inductor can not be represented with two-port impedance parameters and therefore it is not possible to demonstrate series inductive behaviour.

This problem is solved with scattering parameters. These parameters do not use shorts or opens as terminating impedances but terminating impedances $Z_N$ with $\Re(Z_N) > 0$ are used instead. Consider the scattering parameters of a transmission line with equal port impedances $Z_N$:

$$S_{11} = S_{22} = \frac{j (Z_0 - 1/Z_0) \sin(\beta l)}{2 \cos(\beta l) + j (Z + 1/Z_0) \sin(\beta l)} \approx \frac{j (Z_0 - 1/Z_0) \beta l}{2 + j (Z_0 + 1/Z_0) \beta l} \tag{3.3}$$

where $\overline{Z_0}$ is the normalised transmission line impedance $\overline{Z_0} = Z_0/Z_N$ and $\beta$ is the phase constant $\beta = \omega \sqrt{LC}$ and the small argument approximations $\sin(\beta l) \approx \beta l$ and $\cos(\beta l) \approx 1.0$ have been used. Comparing these scattering parameters with the scattering parameters of a series inductor $L_{eq}$ and a shunt capacitor $C_{eq}$ respectively:

$$S_{11} = S_{22} = \frac{j \omega L_{eq}/Z_N}{2 + j \omega L_{eq}/Z_N} \quad S_{11} = S_{22} = \frac{-j \omega C_{eq}/Y_N}{2 + j \omega C_{eq}/Y_N} \tag{3.4}$$

shows that the line is inductive if $\overline{Z_0} \gg 1$ and capacitive if $\overline{Z_0} \ll 1$. In other words: if the impedance of the line is much greater than the impedance of the termination the line behaves
inductively and if the line impedance is much smaller than the reference impedance the line behaves capacitively.

Based on the previous analysis we conclude that to determine whether a single line above a ground behaves inductively scattering parameters should be used. Then determination of inductive behaviour depends on terminating impedances.

3.2.2 Coupled lines above a ground plane

The case of a single line is extended to the case of multiple wires over a ground plane. In figure 3.3 four lines above a ground plane are shown and in the same figure a cross sectional view is shown of multiple coupled lines above a perfectly conducting groundplane. A TEM wave is assumed to propagate in the longitudinal z-direction.

![Figure 3.3: Straight coupled lines above a ground plane. On the right a cross sectional view of coupled round lines above a ground plane. TEM wave propagation is assumed in the z-direction.](image)

In the single line case the capacitance and inductance per unit length are computed analytically. In case of multiple coupled lines the inductance matrix \( L \) and capacitance matrix \( C \) per unit length matrices must be computed (cf. the transmission lines in section 2.7.4). In the following the accurate and efficient computation of these matrices is considered. Assuming vacuum the capacitance matrix \( C \) is computed first and the inductance matrix is computed using the relation: \( L = C^{-1} / \epsilon_0^2 \). This relation is derived from the fact that the velocity of TEM wave propagation in vacuum equals the speed of light in vacuum \( c_0 \). The method of moments as discussed in section 2.10.4 is employed to compute the capacitance matrix. For reasons of simplicity the full mathematical treatment is not given here.

To compute all elements of the capacitance matrix a Fourier expansion is made of the unknown surface charge density, with Fourier coefficients to be computed. This expansion represents the surface charge density in a large number of cases with only a few terms. Since for each element of the capacitance matrix the potential of each wire is known, a set of integral equations can be set for the unknown expansion coefficients. These equations are similar to the equation set up for the weighted potential in case of current conduction, equation (2.35). The Green’s function in two dimensions is found by image techniques [51] and is represented in cylindrical coordinates. The potential is point matched at a number of points on each wire. The number of matching points on each wire is chosen equal to the number of expansion functions for that particular wire. With the Green’s function in cylindrical coordinates, the chosen Fourier expansion and the point matching scheme, all convolution integrals are calculated analytically. To have an accurately computed capacitance matrix the number of Fourier terms must be 2-5 per wire for the structures under consideration. More terms are needed
if the wire is brought close to the ground plane or if wires are brought close together. One
drawback is that the resulting matrix equation is badly conditioned, causing numerical
problems and loss of accuracy if no specific actions are taken. By using a pivoting scheme in the
solution process of the matrix equation these problems were solved. Another method to avoid
problems is to use a Fourier expansion for the surface charge density and to weight the poten-
tial with the same function. This method is collectively referred to as the Galerkin Method.
For the case under consideration the Galerkin method has one major drawback. Only a part
of the resulting convolution integrals can be solved analytically, the remainder must be solved
by numerical integration. One option in this case is to expand the function, obtained after the
first integration, again in Fourier functions. This expansion must be based on a finite number
of function evaluation points on the observation wire. The remaining convolution integral
is then solved analytically again. This option is open for further research. In any case, a
Galerkin type method gives a better conditioned matrix, but in our case this approach is not
necessary.
To treat the perfectly conducting ground plane it is also possible to use image charges. Con-
sequently, the Fourier coefficients also enter the remaining matrix equation and make the
matrix twice as large as necessary. Since the charge density distribution of the direct wire
and the image wire are interrelated, the effect of the image wire can be directly accounted for.
This approach can also be used in the case of a round wire above a grounded dielectric slab
in which case an infinite number of images arises.

In section 3.2.3 the bondwires are modelled using a lumped inductance matrix ignoring ca-
capacitive effects. Several methods can be used to investigate whether this approximation is
valid. Although the coupled lines model can only be used in very specific cases, the model
offers possibilities to quantify the capacitive effects. In the first method the scattering ma-
trix is written in terms of the capacitance matrix, the inductance matrix and the length of the
lines. Next the capacitance matrix is multiplied by a factor much smaller than 1, reducing the
capacitive effects, and the scattering parameters are recalculated. Comparing the scattering
matrix for this case and the previous case gives an indication under which circumstances the
capacitive effects can be ignored in terms of the capacitance matrix, the inductance matrix,
the length of the lines, the frequency and the terminating impedances. Another approach, fol-
lowed here, is to implement the transmission line model in MDS and to simulate wires with
practical terminations. Then the capacitance matrix is scaled by a factor much smaller than
one, and the simulation with the specific terminations is repeated. If the scattering parameters
have not changed very much, it is concluded that the capacitive effect is negligible.

This strategy is applied to the example of 10 parallel coupled wires connected to port 1 on
one side and to port 2 on the other side as shown in figure 3.4.
The wires are placed 500 \( \mu \text{m} \) above the groundplane with a spacing between the wires of 100
\( \mu \text{m} \). The length of the wires is 1 mm and the radius of each wire is 25 \( \mu \text{m} \). First a relatively
large impedance is chosen for the terminations: \( Z_1 = Z_2 = 100 \text{ Ohms} \). The scattering para-
eters are calculated from 1 - 20 GHz and plotted in the top row of figure 3.5. The scattering
parameters are normalised to the terminating impedances. Shown on the left is the magnitude
of \( S_{11} \) and shown on the right is the magnitude of \( S_{21} \). In each plot one trace displays the
result if both inductive and capacitive effects are taken into account, the other trace represents
inductive effects only.
A large difference is observed between these two cases. In the case that both the inductive
and capacitive effect are accounted for a TEM wave propagates along the line. This example demonstrates that the TEM wave guiding property of the transmission line is used to transfer energy from one port to the other. In the case of a single line above a ground plane it was already shown that the behaviour of the lines depends on the terminating impedances. Since the lines are coupled in parallel in a homogeneous medium, it can be modelled by one equivalent transmission line. It is found that this equivalent transmission line has a line impedance of 87 \, \Omega with an inductance per unit length of 0.291 \, \mu H/m and a capacitance per unit length of 38.18 \, pF/m. Because the line impedance is close to the terminating impedance, both capacitive and inductive effects come into play.

The terminating impedances are reduced to 10 \, \Omega and the scattering parameters are recalculated and shown in the second row of figure 3.5. Small differences between the case with both inductive and capacitive effects and the case with inductive effects only are found from these pictures. These differences increase with frequency. The equivalent inductance is extracted from the scattering parameters as 291 \, pH, which compares very well with the product of the inductance per unit length and the length of the lines. It is concluded that approximating the wires only with inductances is justified in this case.

Finally the wires are terminated with an impedance of \( Z = 10 - j10 \, \Omega \). The reflection parameters and the transmission parameters are shown in the two bottom pictures of figure 3.5. A resonance around 11 \, GHz is observed in the scattering parameters. Note the difference in the reflection parameters for the two cases at this frequency. Although not shown in the picture, this difference is due to a shift in the resonance frequency of around 100 \, Mhz for the case with the inductances only.

In this section the calculation of the capacitance matrix per unit length and the inductance matrix per unit length for coupled round wires above a perfect groundplane is considered. These matrices are calculated in a short time with a high accuracy. Although curved bond-wires can not be modelled, this coupled line model may serve as a simplified model to make (rough) estimations of the electrical behaviour of bondwires. The impact of ignoring capacitive effects on the behaviour can be estimated in a relatively easy way. One other point not considered here is the modelling of losses due to the finite conductivity of the metallisations involved. The implementation of skin effect losses under the TEM-approximation is straightforward and these losses can be computed with good accuracy, since the charge density distribution is computed with high accuracy. In section 3.2.4 the modelling of wires with a rigorous solver is considered. Unfortunately this solver can not model losses rigorously, making a good evaluation of a lossy model rather difficult. The correct and accurate modelling of loss in curved wires is a subject for further research.
Figure 3.5: Simulation of ten parallel coupled lines with different impedance terminations $Z_1=Z_2$ accounting for capacitive and inductive effects ($L$ and $C$) and inductive effects only $L$. The magnitude of $S_{11}$ is shown on the left, and the magnitude of $S_{21}$ on the right. The scattering parameters shown are normalised to the terminating impedances.
3.2.3 Modelling of curved wires

In this section the modelling of curved wires, as implemented in MDS, is discussed. The modelling starts with the computation of the inductance matrix and the computation of the resistance matrix. These two matrices are appropriately combined to form the impedance matrix. The impedance matrix is then inverted to obtain the admittance matrix and finally the $N$-port admittance matrix is converted to a $2N$-port admittance matrix. This process is illustrated in figure 3.6.

![Diagram of bondwires in MDS as a multiport network.](image)

Figure 3.6: Modelling of bondwires in MDS as a multiport network. Shown on the left the initial $N$-port model for $N$ coupled bondwires. Inductive coupling is modelled by the inductance matrix $\mathbf{L}$ and resistive losses are modelled by a resistance matrix $\mathbf{R}$. Shown on the right the $2N$-port model implemented in MDS. The $2N$-port admittance parameters are obtained from the $N$-port model.

In a subsequent section a more rigorous tool, Agilent’s Finite Element Solver HFSS, is used to compute the scattering parameters of a single wire. Inductances are extracted from the calculated scattering parameters and compared with the model. Comparison with measurements concludes the modelling part of the wires.

Computation of the inductance matrix

Computation of the inductance matrix is based on the definition of the mutual inductance $L_{ij}$ between two loops as the ratio between the magnetic flux $\Phi_i$ induced in loop $i$ and the current $I_j$ flowing in loop $j$. In the case of bondwires forming loops with constant cross section along the loop and under the assumption of a uniform current density in each loop Neumann’s inductance equation is used to compute the mutual inductances $L_{ij}$ [49], [52]:

$$L_{ij} = \frac{\text{flux linking } C_j \text{ due to a current in } C_i \text{ current in } C_i}{4\pi \int_{C_i} \int_{C_j} \frac{dl_i \cdot dl_j}{r}}$$

(3.5)

with the contour $C_i$ defining the center of the current carrying wire $i$ and the contour $C_j$ defining the interior edge of closed loop $j$ and $r$ is the distance between the points on the contours $C_i$ and $C_j$. This situation is illustrated in figure 3.7, where two circular loops are depicted with the mutual inductance defined as the ratio of the induced magnetic flux and the current.

In practice, however, ideal loops as shown in figure 3.7 are not encountered. Normally a current carrying loop is formed by a set of network elements connected together as shown in figure 3.8 on the left. Each loop consists of a series connection of lumped elements such as a
Figure 3.7: Definition of the mutual inductance between two current carrying loops as the ratio of the magnetic flux in contour $C_j$ and the current in loop $i$.

voltage source, a resistor or a capacitor and a bondwire. Because only the mutual inductance between the two wires is of interest, the concept of partial inductances is introduced.

Figure 3.8: Current carrying loops formed with network elements. On the top closed loops are shown using elements such as a capacitor, a resistor and a voltage source. Each loop also has a bondwire. If only the mutual inductance between the wires is of interest, the concept of partial inductance is used [52] where for reasons of simplicity the mutual coupling between the wires and the remaining network elements is assumed negligible. In this case Neumann's inductance equation is not applied to the closed contours, but to the open contours of the wires only.

The mutual effect between the circuit and the wire is assumed negligible and Neumann's inductance equation is considered for the wires alone instead of for the full loops.

In the implementation in MDS each wire is represented by a number of segments and the contour integral is evaluated along the segments. The contour $C_i$ is taken at the heart of the wire and the contour $C_j$ is at the outer surface of the wire [49].

To illustrate the procedure behind the model implemented in MDS, consider the circuit of 3.9.

A straight bondwire is located above a perfectly conducting groundplane. The bondwire is connected to a voltage source and is terminated by a resistor. The model assumes an equivalent circuit as shown in the middle of the same figure i.e. the bondwire is represented by an inductor with inductance $L$. To account for the effect of the perfectly conducting ground plane, the method of images is used: the wire is "mirrored" in the ground plane. To compute the inductance, three lines are defined: $l_1$ is the center axis of the bondwire, $l'_1$ is the line on
Figure 3.9: Example illustration of inductance calculation using the concept of partial inductance [52]. On the left a straight bondwire located above a perfectly conducting ground plane. In the center the equivalent circuit is shown. On the right the method of images is used to compute the partial inductance.

the edge of the wire and \( l_2 \) is the center axis of the imaged wire. The distance between a point on line \( l_1 \) or line \( l_2 \) and a point on line \( l'_1 \) is represented by \( r \). The inductance \( L \) is computed from:

\[
L = \frac{\mu_0}{4\pi} \int_{l_1} \int_{l'_1} \frac{dl_1 \cdot dl'_1}{r} + \frac{\mu_0}{4\pi} \int_{l_2} \int_{l'_1} \frac{dl_2 \cdot dl'_1}{r}
\]  

(3.6)

The approach described here requires accurate drawings or photos of the wires to be modelled. Throughout this work SEM photos were made of the top-view and the side-view of the bondwires. The Cartesian coordinates of the beginning and end of the segments are found from these photos. This approach is illustrated in figure 3.10. On the left a SEM photo of bondwires is shown. On the right the bondwire is discretised into five segments.

Figure 3.10: Piecewise approximation of bondwires. Left: SEM photos are made of the bondwires. Right: using the photos the wire is approximated by straight segments.

**Computation of the resistance matrix**

In general the full resistance matrix needs to be computed. If the bondwires are not placed very close to each other the "proximity effect" is rather low and all off-diagonal elements of the resistance matrix are small. In power transistors the spacing between wires may be on the order of the radius if the wires, making this assumption questionable. On the other hand it is noted that this approximation simplifies the computations substantially since the accurate computation of the resistance matrix requires the current distribution in the wire be known with high accuracy. Rather difficult computations must be employed to find this
current distribution. Therefore, the crude assumption of a uniform current distribution in the wires has been maintained and the accurate computation of the resistance elements remains a point for future work.

Modelling of the diagonal elements of the resistance matrix includes the DC resistance and the skin resistance. The DC resistance is computed for each wire using:

$$R_{DC,i} = \frac{l_i}{(\sigma \pi r^2)}$$  \hspace{1cm} (3.7)

where \( r \) is the radius of the wire. And the skin effect resistance is computed after ([27], pp. 43-45):

$$R_{AC,i} = \frac{l_i}{(\sigma 2\pi r \delta_s)} \hspace{1cm} \delta_s = \frac{1}{\sqrt{\pi f \mu \sigma}}$$  \hspace{1cm} (3.8)

These two resistances intersect at the frequency \( f = 4/(\pi r^2 \mu \sigma) \). Far below this frequency the DC resistance dominates and far above this frequency the skin resistance dominates. In our implementation in MDS of the model a Spline interpolation is applied around the intersection of the two resistances. This allows for a "smooth" function avoiding possible numerical problems in the simulator.

As an example consider a 1 mm long bondwire of gold \((\sigma = 4.1 \cdot 10^7 \text{ S/m})\) with a radius of 19 \(\mu\text{m}\). The DC resistance is 0.022 \(\Omega\) and the AC resistance at 1 \(\text{GHz}\) is 0.082 \(\Omega\). Although these resistances may seem small they affect the behaviour of the transistor. In principle the inductance of the bondwires should also be modified for the skin effect behaviour but its effect is found negligible for the frequencies used.

**Computation of the impedance- and admittance matrices**

For the implementation of the model in MDS the \(2N\)-port admittance matrix is required, with \(N\) being the number of wires. This matrix is computed as follows. Once the resistance matrix \(R\) and the inductance matrix \(L\) are available the \(N\)-port impedance matrix \(Z\) is formed:

$$Z = R + j\omega L$$  \hspace{1cm} (3.9)

This impedance matrix is inverted and the admittance of the \(N\)-port model is obtained (cf. left of figure 3.6).

$$Y_N = Z^{-1} = (R + j\omega L)^{-1}$$  \hspace{1cm} (3.10)

From the admittance matrix \(Y_N\) the \(2N\)-port admittance matrix is easily computed (cf. right of figure 3.6).

$$Y_{2N} = \begin{bmatrix} Y_N & -Y_N \\ -Y_N & Y_N \end{bmatrix}$$  \hspace{1cm} (3.11)

The computations for the model are now complete. There is an important point to note however. In equation (3.10) the inversion of an \(N \times N\) complex matrix is required. Under normal conditions this doesn't pose any problems. It was found however that during DC analysis in MDS this operation is performed for each iteration in solving the set of non-linear equations. Consequently, the same matrix inversion is repeated unnecessarily slowing the simulations. Note that hundreds of iterations are not abnormal when analysing the electro-thermal behaviour of power transistor models. This problem is solved in the implementation in Agilent's ADS.
Example instance of the bondwiremodel

For reasons of completeness an example of the instance of the model for 3 coupled wires is shown in figure 3.11.

Figure 3.11: Instance of the model for 3 wires as implemented in MDS. Each wire is discretised in 5 segments and the Cartesian coordinates of the begin- and endpoints must be entered.

The first two parameters required are the radius of the wire and the conductivity of the metallisation of the wires. The remaining parameters are the Cartesian coordinates of the begin- and endpoints of the segments (3×6×3). Models for any reasonable number of wires are created easily. Additionally, the number of segments per wire is changed easily.

3.2.4 Full wave modelling of bondwires with HFSS

There are two reasons to model curved wires in a 3-dimensional FEM simulator like HFSS. First of all it is important to know typical simulation times and memory usage. This allows one to make a well-founded decision to use HFSS in specific complex situation or to use a simplified model as presented in section 3.2.3. Secondly the results produced by HFSS are used to verify the computations made using the model presented in section 3.2.3.

This section starts with a discussion of the simulation of multiple bondwires in HFSS (version A.04.01). The principle aim is to compare the inductance computed by the model of section 3.2.3 with the inductance computed by HFSS. Note however that HFSS computes fields and scattering parameters. To extract the inductance matrix from the scattering parameters an equivalent circuit is assumed. An analytical procedure is used for the extraction of the inductance matrix. Several parameters, such as wire discretisation and box dimensions, affect the accuracy of the HFSS computations. By varying these parameters their relative effect is estimated or reduced. The method is demonstrated for simple structures such as a single wire above a ground plane and a curved wire above a ground plane. It is found that for accurate HFSS results a considerable amount of memory and solution time is required. Maximum differences in the inductance computed by the model and computed by HFSS in the order of a few percent are reported.
Modelling of bondwires with HFSS

The modelling starts with the definition of the geometry. A solid modeller is used to define a collection of connected objects and medium parameters are assigned to the objects. Boundary conditions and port definitions are applied to faces or parts of the faces. In figure 3.12 a setup with six bondwires in a rectangular box is shown.

![Figure 3.12: Six wires in a rectangular box defined in HFSS are shown on the left. Each wire is connected to ground on one side and excited by a coaxial line on the other side. In the middle the coaxial ports are shown. The equivalent circuit for the bondwires, a shunt capacitance matrix and a shunt inductance matrix, is shown on the right.](image)

In this picture a box with six coupled bondwires is shown. At all six faces of the box Dirichlet boundary conditions are applied, forcing the tangential electric field to zero. The bondwires are assumed perfectly conducting and at the surface of the wires Dirichlet boundary conditions are also applied. Each bondwire is connected to ground on one side and excited by a coaxial line on the other side. In the center of figure 3.12 the coaxial lines forming the connection between the coaxial ports and the wires are shown. These coaxial lines are required by HFSS to excite the wires correctly.

HFSS starts by defining a mesh in the structure. To excite the structure a 2D solver computes the TEM modes at the coaxial ports. These modes are the excitation of the 3D structure. The 3D solver computes the fields in the structure and the scattering parameters of the structure in a first pass. At the second pass the mesh is refined automatically based on an error criterion, and fields and scattering parameters are recomputed. This process is repeated until the \( S_{11} \) has stabilised. To obtain the scattering parameters of the wires, the data is de-embedded for the length of the coaxial lines and renormalised to 50 Ohms.

For the extraction of the inductance matrix the equivalent circuit shown in figure 3.12 on the right is used. This is the equivalent circuit after de-embedding for the coaxial lines. On one side of the ports a capacitance matrix \( C \) is assumed and on the other side a grounded inductance matrix \( L \). The capacitance matrix consists mainly of the stray capacitance to ground at the transition from coaxial line to the wire, the capacitance from the wire to ground and the capacitance from wire to wire. The admittance matrix of the configuration is given by:

\[
Y = j\omega C + \frac{1}{j\omega} L^{-1}
\]  

(3.12)

First the Scattering parameters are converted to admittance parameters and then the capacitance matrix \( C \) is extracted from the admittance matrix:

\[
C = \frac{1}{2} \left[ \frac{\Im(Y)}{\omega} + \frac{\partial \Im(Y)}{\partial \omega} \right]
\]  

(3.13)
Once the capacitance matrix is known the inductance matrix is found from equation (3.12). There are a number of parameters affecting the $L$ and $C$ matrices. First of all to make a good comparison between the model and HFSS, the box surrounding the wires should be made as large as possible. If the box dimensions are too small, the inductance computed by HFSS is too low. If the box is made too large the problem can not be handled by the solver due to limited memory or box resonances may occur. The strategy to follow is to start with a reasonably small box and to increase the dimensions step by step until the computed inductance does not depend on the box dimensions. Because in HFSS a circle must be approximated by straight segments the second point is the discretisation of the circumference of the wires. If the discretisation is too rough, the computed inductance is too high and if the discretisation is too fine the mesh generator may encounter problems or the generated matrix system is too large. The strategy in this case is to start with a rough discretisation and to increase it until the computed inductance matrix does not depend on the discretisation.

Modelling of a straight wire

The first comparison between HFSS and the model is for a single grounded wire above a ground plane. For reasons of symmetry only half the structure is simulated. The setup in HFSS is shown in figure 3.13.

Figure 3.13: Modelling of a wire in HFSS. Shown on the left the box enclosing the wire. The wire is excited at a coaxial port on one side and is grounded on the other side as shown on the right. Note that only one half of the wire is simulated.

On the left the boxed structure is shown. On five faces Dirichlet boundary conditions are defined and on the plane of symmetry a Neumann boundary condition is applied. This symmetry plane cuts the structure in two halves and only half the structure need to be solved. In the same figure a close up of the wire is shown. The radius of the wire is 25 $\mu$m and the length of the horizontal part of the wire above the ground is 1 mm. The axis of the horizontal part of the wire is located 100 $\mu$m above the groundplane. A better view for a similar setup is shown in figure 3.17. On one side the wire is excited by a coaxial port. To ensure a correct port definition the coaxial port is connected through a coaxial line of 100 $\mu$m with the bondwire. The coaxial line lies below the ground surface. On the other side the wire is shorted to ground. HFSS starts with finding the dominant mode at the coaxial port. The dominant mode for
the coaxial port is a TEM mode. The structure is excited with this mode and resulting fields and the $S_{11}$ (the ratio between the incident wave and the reflected wave) is computed. The simulator adaptively refines the finite element mesh at each pass and recomputes the fields in the structure and the $S_{11}$.

To extract the inductance from the computed scattering parameter, the equivalent circuit of figure 3.14 is used.

![Inductance vs Pass](image)

Figure 3.14: Top: equivalent model of the structure under consideration. The transmission line models the coaxial line of 100 $\mu$m, the capacitor models the capacitance to ground and the inductor represents the inductance of the wire. Shown on the bottom: the computed inductance versus the number of passes in HFSS and the inductance computed with the model.

In the circuit the transmission line represents the coaxial line of 100 $\mu$m, the capacitor represents the stray capacitance at the transition from coaxial line to the wire and the capacitance from the wire to ground. The inductor represents the inductance of the wire. First the computed $S_{11}$ is de-embedded in HFSS for the coaxial line. After de-embedding, the $S_{11}$ is renormalised to 50 $\Omega$ in HFSS and the new $S'_{11}$ results. The capacitance is extracted from $S'_{11}$ by applying equation (3.13) and a value of 13 fF is found. The $S''_{11}$ is de-embedded for this capacitance. From the resulting $S''_{11}$ the inductance is computed. In figure 3.14 the inductance versus the number of passes is shown at 1 GHz. At the first pass an inductance of 365 pH is found, increasing to 443 pH at the last pass. The inductance computed with the bondwire model is 432 pH giving a relative difference of less than 3 percent. In this particular case 4 to
5 passes are enough to obtain an inductance within 1 percent of the answer at the eighth pass. There are two issues affecting the computed inductance: the size of the surrounding box and the angular discretisation of the wire. These issues are discussed later in this section.

The memory usage and the solution time per frequency point is displayed in figure 3.15. At the first pass the RAM usage is 12.5 Mb and increases to 50 Mb at the last pass. During the solve process the solution is written to disk. This file steadily increases until the solution process is completed. The disk usage at the first pass is 14 Mb and increases to 72 Mb at the last pass. The simulation time as reported by the solver on an HP 735 workstation (45 MFlops) is around 2 minutes per frequency point at the first pass and increases to 19 minutes at the last pass. To show improvements in simulator technology the solve times for a previous version of HFSS (A.02.06) is also plotted in the figure.

![Graph](image)

Figure 3.15: Simulation statistics of the straight wire above the ground plane for HFSS version A.02.06. On the left the memory usage in Mb versus the number of passes and on the right the solution time per frequency point is displayed.

To study its influence the circumference discretisation of the wire is doubled from 20 segments to 40 segments, and the extraction procedure outlined above is repeated. The computed inductance versus the number of passes is displayed in figure 3.16. The results from figure 3.14 are also displayed in this figure.

At the first pass an inductance of 420 pH is computed with 40 segments compared to 365 pH with the 20 segments discretisation. With the increased number of segments the results of the first pass are closer to the final result mainly due to the finer meshing in the surroundings of the wire, enforced by the increased discretisation of the circumference of the wire. The cost is higher memory usage. With the 20 segments discretisation memory usage is at pass 5 less than 35 Mb, with 40 segments the memory usage is around 95 Mb at the start and at the fifth pass 150 Mb. For this reason only the results of five passes are reported. It is concluded from this picture that the discretisation of 20 segments is enough to compute the inductance correctly.

The influence of the radius of the wire on the inductance is also studied with HFSS. The radius of the wire is varied from 5 μm to 25 μm in steps of 2.5 μm. The circumference of the wire is approximated by 20 segments and for reasons of symmetry only half the structure is
considered. In all simulations eight passes are used to compute the scattering parameter. The inductance versus the wire radius is shown in 3.16 on the right. If the wire radius is 5 μm the inductance computed by HFSS is 820 pH, the model computes an inductance of 837 pH. The inductance decreases as the wire radius increases to a value of 443 pH (HFSS) and 432 pH (model) for a wire radius of 25 μm. The maximum difference is around 2.5 percent for the wire with 25 μm radius.

From these results it is concluded that the inductance computed with the model differs only a few percent from the inductance computed by HFSS. Simulation times of HFSS are in the order of minutes per frequency point were the bondwire model takes only a few seconds to evaluate the admittance matrix. A similar observation is made with respect to RAM memory usage: HFSS uses several Mb up to more than 100 Mb, and the bondwire model uses less than 1 Mb. The observed simulation times prohibit the use of HFSS during the iterative design of power transistors. The software can be used however to generate scattering parameters of bondwire geometries at certain intermediate points in time during the design. Additionally, the bondwire model is directly used within MDS, allowing the design and optimization of the bondwire geometry without much effort.

Modelling of a curved wire

The modelling of a curved wire follows the same guidelines as the straight line. A curved wire with five segments is defined in a box of 2 × 3 × 3 mm³. For reasons of symmetry only half the structure is simulated. In figure 3.17 the setup of half the structure is shown. In the same figure on the right the setup of the wire is displayed. A coaxial line of 100 μm connects the coaxial port with the wire. The wire has a radius of 25 μm and a horizontal length of 1000 μm. The axis of the wire approximates with 5 segments a circle with a radius of 500 μm. The inductance is computed with the inductance model of section 3.2.3 using five
straight segments in the model. The inductance computed by the model and the inductance computed by HFSS versus the number of passes is shown in figure 3.18 on the left.

The inductance computed by the model is 941 pH. The inductance at the first HFSS pass is 771 pH and increases to 916 pH at the eighth pass. The relative difference between the HFSS inductance and the model is around 3 percent. An important parameter in this particular case is the size of the surrounding box. For the straight wire above a plane little differences were found for larger boxes, mainly because the main part of that wire is parallel to the ground plane, with the top cover far above it. In case of the curved wire the side walls are relatively close to the wire and may affect the magnetic field substantially compared to the case without side walls. To investigate the effect of the box dimensions, two other cases are investigated. One structure has box dimensions $5 \times 5 \times 5$ mm$^3$ and the other has dimensions $10 \times 10 \times 10$ mm$^3$. The procedure of simulating and extracting the inductance is repeated for these two
cases and the inductance is plotted against the number of passes. In figure 3.18 the results of the model and the HFSS results for the three structures are plotted. It is observed that the inductance at the eighth pass is 931 for the box of $5 \times 5 \times 5 \text{ mm}^3$. This is around 15 pH higher than the 916 pH found for the box of $2 \times 5 \times 5 \text{ mm}^3$. Finally it is observed that the inductance for the largest box ($10 \times 10 \times 10 \text{ mm}^3$) is 933 pF, a relative difference of around 1 percent.

Concluding remarks

The results presented in this section indicate that the bondwire model computes the self inductance of wires with reasonable accuracy. The HFSS calculations take in the order of minutes with a substantial memory usage. Calculation times of the bondwire model are in the order of seconds with very low memory usage. Due to limited time and limited computing power at the time the HFSS computations were carried out, only single wires have been studied. The approach presented here should be extended to coupled bondwires and bondwire arrays. Solving these complex structures seems now feasible with the software and hardware available for desktop CAD. Additional studies with rigorous software like HFSS should be carried out to investigate the modelling of conductor losses and radiation losses.

3.2.5 Measurement of coplanar transmission lines

Transmission lines are often used in microwave circuits either for their transforming properties or for the connection of two components separated spatially. In this thesis transmission lines are mainly used for connecting a component under investigation with microwave probes. More specifically, in this section the coplanar lines are used as an interconnection between microwave probes and bondwires. To remove the line effects from the measurements, accurate characterisation of the lines is a prerequisite. This section focuses on the experimental characterisation of the coplanar transmission lines. These lines are used in the experimental setups for the characterisation of bondwires, prematch capacitors and more complex situations.

Transmission lines are characterised by a complex transmission line impedance and a complex propagation constant. If these parameters are known, the scattering parameters are computed easily for any given length $l$. The line parameters are obtained by measuring the scattering parameters of the line and converting these parameters to ABCD-parameters. Both complex transmission line parameters are computed from these chain parameters. In this section the method is used to extract line parameters for coplanar lines. These coplanar lines are used to connect for example a coplanar probe to a bondwire i.e. the accurate characterisation of the bondwire depends on the characterisation of the interconnecting line. A top view drawing of the measurement set up of the coplanar line is shown in figure 3.19.

In this figure a ground plane with a coplanar line is shown. The coplanar lines have a width of approximately 50 µm and the line to ground spacing is also 50 µm. Microwave GSG probes are connected to both ends of the lines and the scattering parameters are measured in the range of 45 MHz - 10 GHz. The transmission line with a total length $L_T$ is divided in three parts. In the first and third part the probes are placed and each probe is moved 40 µm inwards. The middle part represents the actual transmission line with length $l$. Lines with the following lengths $L_T$ are fabricated in an industrial thin film process using 25 mil alumina
substrate: 100, 200, 300, 400, 500, 1000, 2000, 3000, 4000 and 5000 μm. Although for a symmetrical and reciprocal transmission line \( S_{11} = S_{22} \) and \( S_{21} = S_{21} \), differences are found in the measured scattering parameters. For a 5000 μm line differences between \( S_{11} \) and \( S_{22} \) of 0.3 dB and 5° are observed for the magnitude and phase respectively. For the transmission parameters these differences are 0.01 dB and 0.1° respectively. These differences are larger for smaller line lengths. The transmission line parameters are extracted from the ABCD parameters after conversion from Scattering parameters. Nevertheless, the extracted transmission line parameters are stored in a dataset. These transmission line parameters facilitate a transmission line model with the length of the line as a variable.

In the measurements it was found that the extracted imaginary part of the impedance and the real part of the propagation are noisy, the results of the real part of the impedance and the imaginary part of propagation constant having much less noise. Note that, in the first order approximation, a line length of 0.2 mm, with an impedance of 60 Ω and β = 70 rad/m at 1 Ghz has an equivalent series inductance of \( L_{eq} = (Zβl)/ω \approx 130 \text{ pH} \).

Sensitivities

The LRM calibration does not contain a method to obtain absolute numbers for the measurement accuracy. The differences between the measured scattering parameters however gives an indication of the accuracy with which the transmission line is measured. In the following the sensitivity is studied of the line parameters of the 5000 μm line for errors in the S-parameters at 1 GHz and at 5 GHz.

The results of the sensitivity analysis are shown in table 3.1.

In the table the relative sensitivity of \( R(\gamma) \), \( Z(\gamma) \), \( R(Z) \) and \( Z(Z) \) with respect to the \( S_{11} \) and the \( S_{22} \) are shown at two different frequencies. For example a change of 0.01 dB in \( |S_{21}| \) causes a a change of 12.3 % in \( R(\gamma) \) at 1 Ghz and 5.8 % at 5 GHz. Although no general conclusions can be made from this table, we can make some observations. First of all, an error in the magnitude of the reflection parameters has a significant effect on the attenuation constant (\( R(\gamma) \)) and the imaginary part of the impedance. The same observation can be made for an error in the phase of the reflection parameters. In this case a very large variation in the
Table 3.1: Relative errors in the extracted transmission line parameters due to errors in the scattering parameters at 1 Ghz (columns 1 G) and at 5 GHz (columns 5 G). The length of the coplanar line is 5 mm.

| Par. | $\Delta$ | $|S|_{11}$ | $\angle S_{11}$ | $|S|_{21}$ | $\angle S_{21}$ |
|------|----------|-----------|----------------|-----------|----------------|
|      |          | 1 G       | 5 G            | 1 G       | 5 G            |
|      |          | 1.0       | 1.9            | 0.03      | 0.02           |
|      |          | 0.37      | 0.37           | 3.4       | 1.8            |
|      |          | 2.6       | 2.3            | 0.12      | 0.10           |
|      |          | 0.38      | 0.05           | 26.8      | 115.           |
|      |          | 12.3      | 5.8            | 0.0       | 0.0            |
|      |          | 0.04      | 0.01           | 1.4       | 5.0            |
|      |          | 0.15      | 0.05           | 0.77      | 0.16           |
|      |          | 0.09      | 0.01           | 1.3       | 2.3            |

imaginary part of the impedance is found. Note that at 1 Ghz the imaginary part is around 3.5 $\Omega$ and at 5 Ghz less than 1.0 $\Omega$.

It is further observed that an error in the magnitude of the transmission parameters mainly effects the attenuation constant and the imaginary part of the impedance. Finally an error in the phase of the transmission parameters causes the largest change in the imaginary part of the propagation constant.

### 3.2.6 Measurement of single bondwires

Previously a model for coupled bondwires was introduced. Several assumptions were made in the computation of the inductance matrix and the computation of the resistance matrix. In this section the self inductance of one wire computed with the model is compared with measurements. In the following section the self- and mutual inductance of two coupled wires is considered. A coplanar measurement set-up is used to eliminate parasitic effects present in for example microstrip measurements. The characterisation of the coplanar line is discussed in section 3.2.5. The scattering parameters of the bondwires are measured on the coplanar substrate with a wafer probe. The length of the coplanar transmission line is de-embedded from the data using the transmission line parameters extracted previously and the self inductance is extracted from the reduced dataset. Top view and side view photos of the bondwires are used to obtain the geometrical data as input for the model. A maximum relative difference of less than 10 percent between model and measurement are observed. A discussion of sensitivities of the inductance for several parameters concludes this section.

In figure 3.20 on the left a drawing of a top view of the measurement set-up is shown. A coplanar measurement set-up is used to measure the bondwires. This configuration allows for a good contact between the microwave probe and the interconnecting coplanar line. It also provides a good grounding and eliminates the need for via holes as compared to a microstrip set-up. In the figure a coplanar line with total length $L_T$, width $W$ and spacing $S$ between ground and line is shown on an Alumina substrate. The substrates are fabricated in a thin film process with a width $W$ of approximately 50 $\mu$m and the same spacing. The length $L_T$ is varied between 100 and 500 $\mu$m. The lines are probed with Ground-Signal-Ground probes from Cascade (WPH-205-100).

Bondwires with a diameter of $2r \approx 38 \mu$m and an x-axis length $LH_w$ are connected on one side to the coplanar line and on the other side to ground. The coplanar probe is moved ap-
proximately 40 μm inwards, leaving a transmission line with length \( l \) between probe and bondwire. A set of 18 samples with a length \( LH_w \) of 1000 μm and a set of 12 samples with a length 2000 μm are considered in this section. To obtain the geometrical data two photos are made from each configuration: a top view photo to obtain the x-axis length \( LH_w \) and the transmission line length \( l \) and a side-view photo to obtain the geometry of the wire. In figure 3.21 an example of these photos is shown.

Figure 3.21: Photos of a bond wire with an x-axis projection of approximately 1 mm. Shown on the left is a top view photo and on the right a view in perspective.

One-port scattering parameters are measured in a frequency range of 45 MHz to 10 GHz with 201 points and an averaging factor of 128. The system is calibrated using a Cascade LRM substrate.

**Extraction of the inductance**

To compare the measurements with the inductance computed by the model several steps must be taken:

- Choose an equivalent model for the measurements. The equivalent model for the measurements is shown in figure 3.20 on the right. The interconnecting transmission line
between probe and wire is modelled by a transmission line $TL$. The additional capacitance from probe to ground and the capacitance of the end of the line to ground is modelled by the capacitor $C_{pg}$. The capacitance from the line end where the wire is mounted and the additional capacitance from the wire to ground is modelled by the capacitor $C_{wg}$. The bondwire is modelled by a series connection of an inductor $L$ and a resistor $R$. The values of all components may vary with frequency.

- De-embed the measured scattering parameters for the interconnection. In section 3.2.5 and appendix A the extraction of the transmission line parameters of the coplanar lines and the capacitance $C_{pg}$ is discussed. With these parameters and the length $l$ (cf. figure 3.20), measured from the photographs, the measured $S_{11}$ is de-embedded for the capacitance $C_{pg}$ and the transmission line $TL$.

- Extract the inductance from the de-embedded data. To extract the inductance from the measured $S_{11}$ the input impedance $Z_{in}$ and its inverse $Y_{in}$ are computed. First assume that the capacitance $C_{wg}$ is zero. In this case the inductance and resistance are computable from the input impedance: $R = \Re(Z_{in})$ and $L = \Im(Z_{in})/\omega$. This leaves the problem of finding the capacitance $C_{wg}$. Using the derivative of $Y_{in}$ an expression is found for $C_{wg}$. Unfortunately the extracted capacitance is very sensitive to measurement error. Under the assumption $\omega L \gg R$ an alternative expression can be found:

$$C_{wg} \approx \frac{1}{2} \left[ \frac{\Im(Y_{in})}{\omega} + \frac{\partial \Im(Y_{in})}{\partial \omega} \right]$$

(3.14)

After extracting this capacitance and de-embedding the data, the inductance and resistance are directly found from the new input impedance.

The difference in the extracted inductance between the case where $C_{wg}$ is assumed zero and the case where the data is de-embedded for this capacitance, obtained using equation (3.14) is less than 10 pH for the samples with a length $LH_w$ of 1000 $\mu$m and less than 21 pH for the samples with a length of 2000 $\mu$m.

**Measurement results**

The inductance is extracted as function of frequency and maximum variations of a few percent were found in the range of 1-10 GHz. In figure 3.22 the measured and modelled self inductance for a wire with a length of 1000 $\mu$m and 2000 $\mu$m respectively are shown. The values shown are extracted at 2 GHz.

The inductance of the 1000 $\mu$m samples is around 0.58 nH. A reasonable agreement between model and measurement is observed, especially for the samples 10-18. A maximum relative difference of 8 percent occurs for sample 3.

The inductance of the 2000 $\mu$m samples is around 0.87 nH. Again reasonable agreement between model and measurement is observed, especially for the samples 6-12. A maximum relative difference of 7 percent occurs for samples 3 and 5.

Note that a rule of thumb for the inductance (e.g. 0.8 nH per mm wirelength) does not give the correct inductance for these samples. This is due to the ground plane close to the wire and the bending of the wire, effectively reducing the inductance.

**Discussion**

Above differences less than 10 percent between model and measurement are reported. A point of concern however is the sensitivity of the inductance for various parameters such as
the wire radius, the geometry of the wire, the de-embedding length etc. In the following an attempt is made to get a feeling for these sensitivities. To that end sample number 16 of the bondwires with a horizontal length of 1000 $\mu$m is considered. The six $(x,z)$ pairs (in $\mu$m) for this wire are given by: (0.0,15), (232,195), (316,221), (391,232), (502,219) and (1099,19).
The inductance of this wire is computed as 0.594 nH.

- **The wire radius.**
The radius of the wire is specified by the manufacturer to be 19 $\mu$m. Changing the wire radius to 18 $\mu$m, which is a rather large change, results in an inductance of 0.608 nH, a relative increase of 2.3 %. Increasing the wire radius to 20 $\mu$m decreases the inductance to 0.581 nH, a relative change of 2.2 %.

- **The de-embedding length.**
Although all de-embedding lengths are measured from the photographs, an error in this length is made easily. Suppose that the correct de-embedding distance is 248 $\mu$m but a length of 228 $\mu$m is used instead, then the extracted bondwire inductance increases to 0.602 nH, an error of 1.3 %.

- **The mounting of the wire.**
Another point of concern is the way the bondwire is mounted on the coplanar transmission line. At the end the wire is pressed on the coplanar line and cut off. This can be seen from the side view photographs. Over a distance of approximately 100 $\mu$m pieces of the wire are found, disturbing the transmission line behaviour. The assessment of the introduced error is quite difficult.

- **The extraction of the reference length.**
The reference length is obtained by making a top view photo of a known length. This reference length is used as a scaling factor in all photographs. If an error is made in the reference length, all $x,z$ values in the model and the de-embedding length are in error. If for example all $x,z$ values are made 2 % smaller, then the inductance decreases from
0.594 nH to 0.577 nH (≈ 2.9 %). If all lengths are made 2 % larger, the inductance increases to 0.611 nH (≈ 2.9 %).

- Substrate tilt.
  Suppose that for some reason the substrates were not completely inline with the microscope, i.e. the substrates were photographed under a small angle. In that case the x-values remain the same but all z values should be multiplied by \( \cos(\theta) \), where \( \theta \) represents the tilt angle. If this tilt angle is 5 degrees the inductance decreases to 0.593 nH. This is a relatively small change in inductance.

- Shift of ground plane.
  The definition of the coplanar ground plane is another cause of errors. From the photos it is not always clear where the ground plane is. Another limiting factor in this respect is the number of pixels in the top view and side view photos. As an example, suppose that all z values are made 10 \( \mu \)m larger (except for the begin and end-points). In that case the inductance increases to 0.609 nH, an increase of approximately 2.5 %.

- Phase error in \( S_{11} \).
  The extracted inductance mainly depends on the phase of \( S_{11} \), the magnitude of \( S_{11} \) has less effect on the inductance. An error of 0.1 degrees at 1 GHz results in a relative error of 1.2 % in the inductance. At 10 GHz the same phase error gives an error in the inductance of 0.2 %. If the phase error is 0.5 degrees these values are approximately 5 times larger (5.9 % and 0.9 % respectively).

- The bond wire discretisation.
  The measured bondwires are modelled with 5 straight wire segments in the model. There are two points to consider in this discretisation process. The first point is the number of wire segments. If the number of segments is increased the curvature of the wire is better approximated. Another point is the choice of the discretisation points. The wire is sampled with 1 begin- and 1 end-point and 3 points along the curvature of the wire. The last of these is put at the longest straight part of the wire. It is anticipated that the discretisation error can give a maximum difference of 5 % in the modelled inductance.

Considering these points a least squares estimate of the introduced difference is on the order of 6 %.

### 3.2.7 Measurement of coupled bondwires

In the previous section the measurement of the self-inductance of bondwires is discussed. The modelling and measurement of coupled wires is discussed in this section. The principle aim is to measure the self and mutual inductance of coupled bondwires and to compare these values with computed values. First the measurement set-up is discussed, followed by a description of the extraction procedure. Measurement results are given and this section concludes with a discussion of the measurements. Parts of the work discussed in this chapter are taken from [53].

The measurements of the coupled wires is an extension of the single wire case. In figure 3.23 a top view drawing of the coplanar set-up is shown.

Two coplanar lines with width \( W \) and spacing \( S \) (both 50 \( \mu \)m) are used to connect the wafer probes with the wires. The coplanar line length \( L_T \) of 200 \( \mu \)m is a compromise between the shortest line possible and a minimum length for correct bonding. The coplanar probes are placed on the beginning of the coplanar line and "travel" a distance of approximately 40
μm over the line. Variations in the order of 10 μm occur. Two bondwires are mounted on a coplanar substrate. The diameter of each wire is \(2r \approx 38 \mu m\), the horizontal length of the wires is denoted by \(LH_w\) and the spacing between the wires is \(S_w\). Each wire is connected to a coplanar transmission line on one side and grounded on the other side. The wires are placed in parallel and the self and mutual inductances are extracted from the two-port scattering parameters.

To calculate the self and mutual inductance of the coupled wires the exact geometry of the wires must be known. In the previous section a microscope in combination with a digitising camera was used to make the photographs. To increase the resolution and to get better pictures of the wires a SEM was used to photograph the coupled bondwires. To obtain the geometry of the wires and the lengths of the interconnecting lines a top view photo and two side view photos are made of each pair of wires. Examples of these photos are shown in figure 3.24.

![Figure 3.24: SEM photos of coupled wires with a horizontal length of approximately 500 μm. Shown on the left is a side view and on the right a top view.](image)

The side view photo shows a wire with a horizontal length of 500 μm and the top view photo shows two parallel wires separated by 700 μm. The de-embedding varies from wire to wire, since the wires are not mounted exactly on the same place on the coplanar strip. Variations
in the order of 10-40 \( \mu \text{m} \) occur.

Two sets of bondwires are considered in this section. The first set of five bondwires have an x-axis projection length \( LH_w \) of approximately 500 \( \mu \text{m} \). The separation of the wires, \( S_w \) is 1000 \( \mu \text{m} \), 1000 \( \mu \text{m} \), 900 \( \mu \text{m} \), 800 \( \mu \text{m} \) and 700 \( \mu \text{m} \) respectively. The exact dimensions are measured from the SEM-photographs. The second set of four wires has a horizontal length \( LH_w \) of approximately 1000 \( \mu \text{m} \). The spacing between the wires is 600 \( \mu \text{m} \), 500 \( \mu \text{m} \), 400 \( \mu \text{m} \) and 200 \( \mu \text{m} \) respectively. In both sets of wires the maximum height above the ground plane is approximately 250 \( \mu \text{m} \) and the wire radius is 19 \( \mu \text{m} \) for all wires. Measurements are carried out using Ground-Signal-Ground microwave wafer probes from Cascade (WPH-205-100) in the frequency range of 45 MHz to 10 GHz with 201 points and an averaging factor of 128. LRM calibration is used to calibrate the system.

The inductance is extracted from the measured scattering parameters as follows:

- Choose an equivalent circuit for the measurement set-up. The equivalent circuit of the measurement set-up is shown in figure 3.25. As in the case of the single bondwires, the model includes probe to ground capacitor \( C_{pg} \), line end to ground capacitor \( C_{wg1} \) and \( C_{wg2} \) and two transmission lines with differing lengths \( TL_1 \) and \( TL_2 \). The bondwires are modelled by an inductance matrix with self-inductance \( L_{11} \) and \( L_{22} \) and a mutual inductance \( L_{12} = L_{21} \). Losses in the wires are modelled by the resistances \( R_1 \) and \( R_2 \).

- Extract the values of the circuit components. The extraction scheme starts with the determination of the capacitor \( C_{pg} \) and the transmission line parameters. As before these values are obtained from the measurement of transmission lines with differing lengths. The measurement data is de-embedded for \( C_{pg} \) and the various line lengths. As a next step the capacitors \( C_{wg1} \) and \( C_{wg2} \) are extracted. For the single wire case an expression for these capacitances was given but this equation is particularly sensitive to measurement errors in the case of coupled wires compared with the single wire case. A different strategy must be followed. Suppose that the capacitors \( C_{wg1} \) and \( C_{wg2} \) are known. In that case the resistance and inductance are extracted from the \( Z \)-parameters: \( R_i = \Re(Z_{ii}) \) and \( L_{ij} = \Im(Z_{ij})/\omega \), with \( i = 1,2 \) and \( j = 1,2 \). Now the capacitor \( C_{wg} \) is chosen such that the extracted inductance does not change with frequency, i.e. the derivative of the extracted inductance with respect to frequency must be as small as possible: \( \partial L_{ij} / \partial \omega \approx 0 \).

![Figure 3.25](image)

Figure 3.25: Equivalent model for the measurement set-up of figure 3.23. The measurements are de-embedded for the capacitors \( C_{pg} \) and the transmission lines \( TL_1 \) and \( TL_2 \). The coupled bondwires are modelled by an inductance matrix and two additional resistances represent loss.
Measurement results

Below the measurement results of the two sets of wires are given. Although both the self and mutual inductances were extracted, the emphasis is on the mutual inductance.

Bondwire $L H_w = 500 \mu m$

The measured and modelled inductance of the five samples with a nominal length of 500 $\mu m$ are shown in figure 3.26.

Figure 3.26: Self inductances $L_{11}$ (shown on the left) and $L_{22}$ (right) and mutual inductance $L_{21}$ (bottom) for five sets of coupled wires with a horizontal length $L H_w$ of approximately 500 $\mu m$. The spacing between the wires $S_w$ is 1000, 1000, 900, 800 and 700 $\mu m$ for samples 1-5 respectively.

The extracted inductance $L_{11}$ is between 0.33 nH and 0.36 nH and $L_{22}$ is between 0.34 and 0.38 nH. The difference between these inductances is due to the longer length of the second wire compared to the first wire. A maximum relative difference between the model and the measurements in the order of 6-8 % is observed for the self inductances.

The mutual inductance is between 2 and 7 pH. Note that the spacing between the wires is 1000 $\mu m$ for samples 1 and 2, 900 $\mu m$ for sample 3, 800 $\mu m$ for sample 4 and 700 $\mu m$ for
sample 5. Although both calculation and measurement show the same trend, a maximum difference of 30 % is found for sample 3.

**Bondwire \( LH_w = 1000 \, \mu m \)**

The measured and modelled inductance of 4 samples with a length of 1000 \( \mu m \) are shown in figure 3.27.

![Graphs showing inductance comparison](image)

Figure 3.27: Self inductances \( L_{11} \) (shown on the left) and \( L_{22} \) (right) and mutual inductance \( L_{21} \) (bottom) for four sets of coupled wires with a length \( LH_w \) of approximately 1000 \( \mu m \). The spacing between the wires \( S_w \) is 600, 500, 400 and 200 \( \mu m \) for samples 1-4 respectively.

The self inductance is between 0.52 nH and 0.56 nH. The maximum difference between the measured and modelled self inductance is 3 %. The mutual inductance is between 15 pH and 115 pH. Again we find that both the calculation and the measurement show the same trend and in this case the difference between the measured and modelled mutual inductance is much smaller compared with the wires of 500 \( \mu m \) length.
Discussion

In this section the sensitivity of the extracted inductances to errors in the geometrical and the microwave measurements is considered. As an example the sensitivities of a wire (sample number 3 in figure 3.26) with a horizontal length of 500 \(\mu\text{m}\) and a spacing between the wires of 900 \(\mu\text{m}\) are considered. First the main sensitivities of the self inductances and then the main sensitivities of the mutual inductance are discussed.

First of all a change of the wire radius of 1 \(\mu\text{m}\) gives a change in the inductance of around 2 \%. Secondly, an error of 20 \(\mu\text{m}\) in the de-embedding length results in an error of 3 \% in the inductance. A third cause of error is due to measurement of the geometrical data. If an error of 2 \% is made in these lengths, an error of 3 \% in inductance is obtained. Finally an error in the phase of the reflection coefficient \(S_{11}\) contributes to the error in the measured inductance. If a constant phase error with respect to frequency is assumed, the error in extracted inductance depends on frequency. For example, a phase error of 0.5 degrees at 1 GHz results in an error of 10 \% in the inductance. The same phase error at 10 GHz gives an error of 1 \% in inductance.

The mutual inductance is less sensitive to changes in the wire radius; a change of 1 \(\mu\text{m}\) in the radius gives a change of 0.5 \% in the inductance. The mutual inductance is also less sensitive to errors in the de-embedding distance. An error of 20 \(\mu\text{m}\) in this length results in an error of 0.25 \% in the extracted inductance. A more important cause of error is in the measurement of the geometrical data. An error of 2 \% introduces an error of 2 \% in the extracted inductance. Finally we consider errors in the scattering parameters. An error of 0.2 dB in the magnitude of the reflection parameters gives an error of 2.5 \% in the extracted inductance. The magnitude of the transmission parameters \(S_{12}\) and \(S_{21}\) is around -50 dB for the 500 \(\mu\text{m}\) wires. If an error of 0.5 dB is made in these parameters an error of 6 \% in the mutual inductance results. Please note that the wires with a length of 1000 \(\mu\text{m}\) have a much higher coupling and, consequently, have a much lower error in the transmission parameters. This explains the relatively small difference between measured and modelled mutual inductance in figure 3.27.

3.3 Modelling of prematch capacitors

In this section the modelling of prematch capacitors is discussed. First a description of prematch capacitors is given followed by a discussion of a transmission line model for the capacitors. In principle parameters for the model must be extracted from rigorous simulations or, if possible, from measurements. It is found that the simulation of the capacitors both in the finite element package HFSS and Sonnet’s Em poses serious problems. By simplifying the geometry important phenomena can be demonstrated and these phenomena can be described by a transmission line model. Measured resonance frequencies of a series combination of a bondwire and a prematch capacitor are compared with simulated resonance frequencies.

A SEM photograph of the prematch capacitor of the BLV 910 transistor, the CAPV910 capacitor, is shown in figure 3.28. This example is illustrative for prematch capacitors found in power transistors, although variations in the geometry are possible. The capacitor shown has a length of approximately 2 mm, a width of 0.95 mm and the height is around 200 \(\mu\text{m}\).
The prematch capacitor consists of a block of silicon with two types of contacts on the top side. In case of the CAPV910 the silicon has a relatively high conductivity of approximately $5 \times 10^4$ S/m (data supplied by Philips Semiconductors). The first contact is gold on a dielectric layer (SiO$_2$ or Si$_3$N$_4$) forming the capacitor. The dielectric layer is on the silicon block, and this type of contact is referred to as Metal-Oxide-Semiconductor (MOS) contact. The second type of contact is a gold deposited on the silicon forming a low ohmic contact. This contact is used to connect bondwires directly to ground. The metal contacts consist of gold with additional metals to avoid diffusion of the gold into the silicon. The MOS contact and the ohmic contact are excited via bondwires and prematch capacitor is connected to the package using the bottom contact.

The modelling of this type of system is closely related to the modelling of interconnects on silicon-silicon dioxide due to the presence of the conducting silicon substrate makes the modelling difficult [54].

In figure 3.28 relatively long contacts in the $x$-direction are found compared to the width of the contacts and the height of the substrate. From this point of view the model introduced in this work for prematch capacitors uses transmission lines assuming quasi-TEM wave propagating in the $\pm x$-direction. Each contact is modelled with a transmission line with a series impedance and a shunt admittance per unit length. To model the coupling between the two lines a coupling series impedance and a coupling admittance per unit length are used. Note that in principle this model can not be used for cases where the width of the metal contact is comparable to the length of the contact. In that case either more elaborate models or simpler lumped element models should be used. In high power transistors however the length of the contact is normally larger than the width. Consider the cross-sectional view of the capacitance as shown in figure 3.29 on the left.

The MOS contact and the ohmic contact are displayed in this figure as well as the transversal model. The transversal model for the MOS contact consists of a capacitor modelling the dioxide capacitance and a parallel combination of a resistor and a capacitor modelling the silicon. The transversal model for the ohmic contact consists of a parallel combination of a resistor and a capacitor modelling the silicon. The model for the MOS contact and the ohmic contact are connected together through a parallel combination of a resistor and a capacitor.
Figure 3.29: Transmission line modelling of a prematch capacitor. On the left (a) a transversal view of a prematch capacitor showing the MOS contact and the ohmic contact. The equivalent transversal models for the two contacts is also indicated. A top view for an incremental piece $\Delta x$ of the two contacts is shown on the right in (b). The longitudinal model is also shown in this figure. Both models assume the return current to flow in the ground contact. Due to the high conductivity of the silicon this assumption fails at higher frequencies where substrate currents due to the skin effect play an important role. Throughout this work modelling will focus on the MOS contact.

Modelling coupling in the substrate. Additionally, a capacitor models the coupling in the air between the two contacts. With quasi-static calculations low frequency values for the per unit length resistances and capacitances can be calculated. The longitudinal model of each contact consists of a series inductance and a series resistance as shown in figure 3.29 on the right. The coupling between the two contacts is through a mutual inductance and, if required, a mutual resistance per unit length. For higher frequencies however skin effect comes into play, mainly because the conductivity of the silicon is relatively high. As stated before the conductivity of the silicon for the BLV 910 prematch capacitor is $5 \times 10^4$ S/m. At 1 GHz the skin depth is in this case approximately 70 $\mu$m. Also note that all quantities are expressed in unit per length allowing for length scaling of the model.

Assuming quasi-TEM wave propagation the two contacts can be modelled as a system of two coupled lines or, if the bottom contact is also considered a line, as a set of three coupled lines. Note that the assumption of quasi-TEM wave propagation is mainly made to get a physical understanding of the electrical behaviour of the capacitors. This assumption is disputable in many cases, but in the absence of rigorous simulations the transmission line model seems a good choice since it models the distributed behaviour in a compact form.

It is anticipated however that due to three-dimensional current spreading occurring in the ohmic contact and in the substrate under the ohmic contact the assumption of quasi-TEM wave propagation in the ohmic contact is not valid. This contact however mainly represents a very low resistance between the bondwires connected to the ohmic contact and the bottom contact of the capacitor and the package. The D.C. resistance being in the order of a few milliohms. From this point of view the modelling of the prematch capacitor only considers the modelling of the MOS contact.
Modelling of the MOS contact

The MOS contact, acting as a capacitor, is the most important contact to model. A transmission line with line parameters $Z_L$, $\gamma$ and length $l$ is used to model the quasi-TEM wave propagation in the $x$ direction of the MOS contact. The model for the MOS contact only is taken from figure 3.29. The ground contact is also considered as a separate line for the time being. The complete model for an incremental piece of line $\Delta z$ of the contact is shown in figure 3.30 in the middle.

![Diagram of MOS contact model](image)

Figure 3.30: Modelling of the MOS contact with a transmission line with line parameters $Z_L$, $\gamma$ and length $l$. Shown in the middle the model accounting for return current flow in the substrate. Modelling of the current flow in the metal and the return current in the substrate is combined in one inductance and a resistance if required. If the effect of the substrate is small compared to the silicon dioxide the model is further simplified as shown on the right.

In this figure the transverse model consists of a silicon dioxide capacitance per unit length $C_{SiO_2}$, a silicon resistance $R_{Si}$ and a silicon capacitance $C_{Si}$. These three elements are also found in the model for the MOS contact shown in figure 3.29 (a). The current flow in the metal is modelled by an inductance $L_m$ and a resistance $R_m$. These two elements are also indicated in the longitudinal model for a short section $\Delta x$ of the contact shown in figure 3.29 (b). It is anticipated that at frequencies where skin effect comes into play, return current flows in the substrate under the metal contact and not in the bottom contact or the ground-plane. This return current in the substrate is modelled by an inductance $L_s$ and a resistance $R_s$. Coupling between the current in the metal and the return current in the substrate should also be accounted for. The inductive coupling between these currents is indicated in the figure with $M_L$. If required, the current flow in the metal and the substrate is modelled with one inductance $L_{pm}$ and one resistance $R_s$ as shown in figure 3.30 in the middle. Note that the substrate capacitor $C_{Si}$ is almost short circuited by the substrate resistor $R_{Si}$ up to very high frequencies since the conductivity is relatively high. This effect is quantified in a first approximation, ignoring skin effects, by the substrate relaxation frequency $f_e$. By noting the similarity between Poisson’s equation for conduction and Poisson’s equation for capacitance, the substrate relaxation frequency is given by:

$$f_e = \frac{1}{2\pi R_{Si}C_{Si}} \approx \frac{\sigma_{Si}}{2\pi \varepsilon_0 \varepsilon_{Si}}$$  \hspace{1cm} (3.15)

Above this frequency the substrate behaviour is dominated by the silicon capacitance and below this frequency the behaviour is dominated by the silicon substrate resistance. In case of a silicon conductivity of $5 \cdot 10^4$ S/m the substrate relaxation frequency is $8 \cdot 10^{13}$ Hz. Additionally, note that the transverse behaviour is mainly dominated by the silicon dioxide. This is quantified using a parallel plate approximation, by the interfacial polarisation
frequency $f_s$:

$$f_s = \frac{1}{2\pi R_{Si} C_{SiO_2}} \approx \frac{t_{SiO_2} \sigma_{Si}}{2\pi \varepsilon_0 \varepsilon_{SiO_2} t_{Si}} \quad (3.16)$$

where $t_{SiO_2}$ and $t_{Si}$ are the thickness of the silicon dioxide and silicon respectively. Above this frequency the transverse behaviour is dominated by the silicon resistance and below this frequency the transverse behaviour is governed by the silicon dioxide capacitance. In case of $t_{SiO_2} = 0.35 \, \mu m$, $t_{Si} = 200 \, \mu m$ and $\sigma_{Si} = 5 \cdot 10^4 \, S/m$ the interfacial polarisation frequency is given by $4 \cdot 10^{11} \, Hz$. Finally it is also noted that the skin effect becomes important in the microwave region. The frequency where the skin effect in the silicon substrate comes into play is the substrate skin effect frequency. This frequency is defined as the frequency where the skin depth of the substrate equals the height of the substrate:

$$f_\delta = \frac{1}{\pi \mu_0 \sigma_{Si} t_{Si}^2} \quad (3.17)$$

Below this frequency return currents mainly flow in the bottom contact. Above this frequency return currents flow in the substrate and both the resistive and the internal reactance should be accounted for. In the specific case of $t_{Si} = 200 \, \mu m$ and $\sigma_{Si} = 5 \cdot 10^4 \, S/m$ the substrate skin effect frequency is 130 MHz.

Based on these considerations one concludes that the high conductivity of the silicon is so dominant that the influence of the transverse silicon resistance and the transverse silicon capacitance is negligible i.e. $R_{Si}$ and $C_{Si}$ in figure 3.30 are negligible. Additionally, the return current flows for frequencies in the microwave region mainly in the silicon and in this case the internal impedance of the substrate (the resistive and the reactive component) is of relevance. The initial transmission line model shown in figure 3.30 in the middle is reduced to the transmission line model shown in the same figure on the right. In this model the inductance of the current flowing in the metal, the inductance of the return current in the substrate and the coupling between these two inductances is modeled by one prematch inductance $L_{pm}$. The same approach is used for the resistance resulting in one prematch resistance $R_{pm}$. The silicon dioxide capacitor $C_{SiO_2}$ is also shown in the figure.

**Parameter calculations of the MOS contact model**

There are several approaches possible to calculate the transmission line parameters for the transmission line model of the MOS contact. The first approach is to make a two dimensional transmission line analysis by solving the Helmholtz equation for a cross section of the capacitor. The per unit length parameters are then extracted from the transmission line parameters $Z_L$ and $\gamma$. First attempts to follow this approach in HFSS failed primarily due to the fact that HFSS finds a waveguide mode far below cut-off instead of the quasi-TEM mode. The second approach is to excite a piece of line with a TEM mode and to compute the transmission line parameters from the scattering parameters computed for that line. This approach also failed in HFSS, the exact reason being not completely clear. The same approach was also used in Sonnet’s Em. A cross sectional view of the MOS contact of interest is shown in figure 3.31 on the left. This example is based on the prematch capacitor of the BLV 910 power transistor, the CAPV910.
In this picture a 200 $\mu$m thick silicon block is placed in a rectangular box. On top of the silicon a thin layer SiO$_2$ of 350 nm is placed. A metal plate of 550 $\mu$m in width is on top of the SiO$_2$ forming the MOS capacitor. The 1-D parallel plate capacitance of the MOS capacitor is 54.26 nF/m. The length of the prematch capacitor in the BLV 910 is 1.7 mm resulting in a parallel plate capacitance of 92.2 pF. The LF capacitance specified by Philips is around 87 pF with a specified maximum variation of $\pm$ 5 pF. The difference between the computed parallel plate capacitance and the actual capacitance is negligible and may be due to a difference between the assumed height and the actual height of the SiO$_2$.

In principle Em can handle brick shaped objects. If these objects are used, the sidewalls of the bricks are also discretised. The number of subsections of the sidewalls in the z-direction is controlled by the z-subsectioning parameter in Em. The default number of 2 z-subsections is enough for the silicon dioxide since this layer is relatively thin and the electric field is mainly directed from the metal to the silicon substrate in this layer. By increasing the number of z-subsections for the sidewalls of the silicon from 2 (default) to 4, it is found that a higher number of z-subsections on the sidewalls is required. But RAM memory requirement is excessive (over 1 Gb) if the z-subsectioning is set to 10. This high RAM requirement makes the solution of the problem shown in figure 3.31 on the left impossible. As a compromise, the structure shown in the same figure on the right is simulated. In this case the bricks are removed and replaced by layers. This structure is solved efficiently by Em. In the simulations the conductivity and the relative permittivity of the silicon are set to $5 \times 10^4$ S/m and 11.7 respectively. The thickness of the SiO$_2$ is adjusted to match at low frequencies the LF capacitance measured by Philips. This choice should guarantee that the calculated low frequency capacitance is close to the actual low frequency capacitance. Initially the losses in the upper metallisation are ignored. Lines with varying lengths are calculated in Em and the inductance per unit length $L_{pm}$, the resistance per unit length $R_{pm}$ and the dioxide capacitance $C_{SiO_2}$ are extracted from the computed scattering parameters. The effect of the line length on these parameters was found negligible. Typical results are displayed in figure 3.32. The prematch inductance $L_{pm}$ is plotted in the top left corner as function of frequency. In this picture a relatively high inductance for low frequencies is found, decreasing as frequency
Figure 3.32: Per unit length quantities versus frequency extracted from the Sonnet Em simulation results. The prematch inductance $L_{pm}$ is shown in the top left picture. In the top right the SiO$_2$ capacitance is plotted. The series resistance $R_{pm}$ is shown in the bottom left corner. Because in this case the upper metal is assumed lossless, the losses are due to the substrate. In the bottom right corner the series resistance due to the substrate ($R_s$) only and the combined series resistance due to loss in the substrate and the upper metal ($R_s + R_{DC}$) are shown.

increases. A reasonable physical explanation for this behaviour is given in the discussion of the resistance. In the next picture the SiO$_2$ capacitance is plotted as function of frequency. Within 1 percent the capacitance per unit length is constant over the complete frequency range of interest. In the picture in the bottom left corner the series resistance per unit length is plotted. Because in the simulations the top metal is assumed perfectly conducting, these losses are due to the silicon substrate. By setting the values for the conductivity of the upper metal to the actual values DC losses are also accounted for. Skin effect losses are ignored since the thickness of the metallisation is much smaller than the skin depth. The results are plotted in the picture in the lower right corner. One trace represents the resistance due to the
substrate only \(R_s\) and the other trace represents the resistance due to the substrate and the DC resistance of the metallisation \(R_s+R_{DC}\). The trace of \(R_s\) is the same trace as \(R_{pm}\) in the left picture. From the last two pictures it is concluded that the resistive losses are mainly due to the skin effect in the substrate. Referring to the case of the internal impedance of a plane conductor in the skin effect regime \([50]\), it is interesting to know the internal impedance of the substrate. Note that the resistance and the reactance of the internal impedance are equal to each other at any frequency in the case of a plane conductor. The series resistance \(R_s\) of figure 3.32 is due to skin losses in the substrate and we define this resistance as the real part of the internal impedance of the substrate. The internal inductance of the substrate \(L_i\) is then computed as \(R_s/\omega\). This internal inductance is plotted against frequency in figure 3.33.

![Graphs showing inductance per unit length versus frequency](image)

Figure 3.33: Per unit length internal inductance \(L_i\) versus frequency computed from the substrate resistance (left). Difference between the total inductance and the internal inductance versus frequency (right).

Comparing this figure with the series inductance of the prematch capacitor \(L_{pm}\) it is concluded that this inductance is primarily dominated by the internal inductance of the substrate. The difference between the prematch inductance and the internal inductance is plotted in figure 3.33. From the previous discussions the following conclusions are made:

- If the quasi-TEM approximation is valid, the transmission line parameters can be extracted from Em simulations.
- Capacitive effects in the silicon substrate are negligible since they are short circuited by resistive effects.
- The transversal behaviour is mainly dominated by the silicon dioxide capacitance because the interfacial polarisation frequency is rather high.
- The extracted prematch inductance per unit length decreases as frequency increases if the skin effect in the substrate dominates.
- In case the height of the substrate is larger than the skin depth the internal impedance of the silicon dominates both the resistance and the inductance.
It is stressed that these conclusions are based on the calculations in Em of the layered structure shown in figure 3.31 on the right. Although no large differences are anticipated, it is recommended to repeat the calculations for the structure shown in the same figure on the left. Rigorous solvers based on the finite difference method seem a good candidate for these structures.

**Compact modelling of prematch capacitors**

The compact modelling of prematch capacitors is based on the transmission line model shown in the middle of figure 3.30. Two modifications are made to this model. First the effect of the silicon shunt resistance and capacitance is ignored. The internal inductance and resistance due to current flow in the silicon substrate are accounted for. The model for a small piece of transmission line Δx is shown on the left in figure 3.34.

![Diagram of prematch capacitor](image)

Figure 3.34: Compact modelling of a prematch capacitor as two coupled lines. Current flow in the metal is modelled by the inductance $L_m$ and the resistance $R_m$. Current flow in the substrate is modelled by the inductance $L_s$ and the resistance $R_s$. The internal inductance is modelled by the inductance $L_i$. For reasons of simplicity the model shown on the right is used.

The inductive effect and loss due to the current flow in the metal contact are modelled by the inductance $L_m$ and the resistance $R_m$. The MOS capacitance is modelled by the capacitance $C_{SiO_2}$. The effect of the return current flow in the substrate is modelled by an inductance $L_s$ and a resistance $R_s$. The coupling between the current flows is modelled by the inductance $M_L$ and the internal inductance is modelled by the inductance $L_i$. Note that it is difficult to compute the inductances $L_m$, $L_s$, and $M_L$, because the current in the substrate is a volume density of electrical current. Additionally, these inductances also depend on the surrounding. These two inductances and the coupling between them, are not too important since the overall inductance is dominated by the internal inductance of the silicon substrate.

The model is reduced to the transmission line model shown in figure 3.34 on the right. The substrate inductance $L_s$ and the coupling inductance $M_L$ are removed from the model. The inductance $L_m$ is replaced by the inductance $L_{pm} - L_i$ to ensure that the total inductance is equal to the previously extracted inductance $L_{pm}$. The resistance $R_m$ is the DC resistance of the metal, since the thickness of the metal is much smaller than the skin depth in the metal for frequencies of interest. The resistance $R_s$ is the internal resistance of the substrate and the internal inductance $L_i$ is computed from $L_i = R_s/\omega$.

To use the model in MDS a coupled two line model is used. The first line models the metal contact and the second line models the current flow in the substrate. The following TEM
matrices are used:

\[ R = \begin{bmatrix} R_{DC} + R_{RF} & 0 \\ 0 & R_s \end{bmatrix} \quad L = \begin{bmatrix} L_{pm} - L_i & 0 \\ 0 & L_i \end{bmatrix} \quad C = \begin{bmatrix} C_{SiO_2} & -C_{SiO_2} \\ -C_{SiO_2} & C_{SiO_2} \end{bmatrix} \]  

(3.18)

The diagonal elements of the resistance matrix \( R \) describe loss in the metal and the substrate respectively. The diagonal elements of the inductance matrix \( L \) describe the inductive effect due to current flow in the metal and in the substrate respectively. And the capacitance matrix \( C \) represents the MOS capacitance between the two lines. The conductance matrix is set to zero since current flow between the two lines and current flow from the lines to the groundplane is assumed negligible. The values of the elements of the matrices should be extracted from rigorous simulations or, if possible, from measurements. They can also be computed from simplified expressions.

**Compact model verification**

The compact model is verified by comparing it with rigorous electromagnetic calculations. The values presented in figures 3.32 and 3.33 are used in the transmission line model. The first structure under consideration is shown in figure 3.35.

![Figure 3.35: Verification of the prematch capacitor model in HFSS version 5. The capacitor consists of a block of silicon and a thin dielectric representing the silicon dioxide. The metal contact extends 1 mm on both sides of the capacitor to form the microstrip ports.](image)

The structure consists of three materials in a box of dimensions \( 5 \times 5 \times 2 \) mm\(^3\). The first material is a conducting block with a length of 3 mm, width 950 \( \mu \)m and height 200 \( \mu \)m representing the silicon. On top of this block a thin dielectric (350 nm) with permittivity 3.7 is defined, representing the silicon dioxide. A metal strip, 5 mm in length and 550 \( \mu \)m in width with zero thickness, is placed on top of the silicon and the silicon dioxide. This structure represents a prematch capacitor excited on two sides by microstrip transmission lines. Agilent's HFSS (version 5) is used to compute scattering parameters of the structure. First the TEM mode of the microstrip transmission line at the ports is computed and the structure is excited with this mode. The computed scattering parameters are de-embedded in HFSS for
the connection lines of 1 mm. The de-embedded S-parameters are renormalised to 50 Ω and plotted in figure 3.36 versus frequency.

![Graphs showing S11 and S21 parameters](image)

<table>
<thead>
<tr>
<th>HFSS</th>
<th>pass 1</th>
<th>pass 2</th>
<th>pass 3</th>
<th>pass 4</th>
<th>pass 5</th>
</tr>
</thead>
<tbody>
<tr>
<td>Memory (Mb)</td>
<td>50</td>
<td>75</td>
<td>115</td>
<td>162</td>
<td>211</td>
</tr>
<tr>
<td>CPU time (s)</td>
<td>69</td>
<td>125</td>
<td>237</td>
<td>395</td>
<td>644</td>
</tr>
</tbody>
</table>

Figure 3.36: Scattering parameters of a prematch capacitor computed with Agilent's HFSS version 5, the transmission line model and a lumped shunt capacitor of 154 pF. The two pictures on the top display the magnitude of the reflection and transmission line parameter respectively and the bottom two pictures display the phase versus frequency. Typical RAM usage and solve time per frequency point of HFSS are shown in the table.

For reasons of comparison the magnitude and phase data of an ideal shunt capacitor is also shown in these plots. From these pictures it is concluded that the transmission model models the behaviour of the prematch capacitor in this situation reasonably well. It is also found that
above $\approx 400$ Mhz the capacitor does not behave as an ideal capacitor anymore. Please note that the results presented are not de-embedded for the transition from the microstrip transmission line to the capacitor. It is found that these effects are small however. For reasons of completeness the HFSS memory usage and solve time per frequency point are also tabulated in the figure. Note that the initial mesh (the mesh at the first pass) is kept as small as possible by setting the mesh parameters to their minimum values.

In the next verification example a series combination of a bondwire and a prematch capacitor is considered. Two different configurations as shown in figure 3.37 are studied.

![Figure 3.37: Verification of the prematch capacitor model in HFSS version 5 with a series combination of a bondwire and a prematch capacitor.](image)

In both cases the prematch capacitor consist of a block of silicon, 3 mm in length. A block of silicon dioxide, 350 nm in thickness, is placed on top of the silicon. A metal plate, 3 mm in length and 550 $\mu$m in width, is defined on top of the dioxide forming the MOS capacitor. The parallel plate capacitance is computed as 154.4 pF. Note that this configuration may pose problems for the simulator due to the relatively thin silicon dioxide layer. In the picture on the left the prematch capacitor is connected in the center to the bondwire and in the picture on the right the capacitor is excited at the end by the bondwire. Also note the different orientations of the capacitors. The transmission line model mainly models $x$ directed currents (currents along the length of the capacitor) in the metal contact and the silicon substrate. It is anticipated however that in the configuration of the left picture significant $y$ and $z$ directed currents are present. These currents and the currents at the sidewalls of the capacitor are not modelled by the transmission line model.

Both structures are simulated in Agilent’s HFSS version 5. The structure on the left has electromagnetic symmetry so that simulating only one half of the structure is sufficient. The computed scattering parameters are de-embedded for the 0.1 mm coaxial lines and the resulting scattering parameters are renormalised to 50 $\Omega$ in HFSS. The inductance of the bondwire is computed with the bondwire model as 0.80 nH. To model the configurations this inductance is used in series with two transmission line models for the prematch capacitor. To model the first configuration the length in each model is set to 1.5 mm. For the second configuration one length is set to 0.2 mm and the other length is 2.8 mm. The series combination of an ideal inductor of 0.8 nH and a capacitor of 154.4 pF resonates at 453 MHz. The resonance frequency of the two configurations is affected by the distributed behaviour of the prematch capacitance and the (internal) inductance of the capacitor. At this resonance frequency the resistive component of the input impedance determines the $S_{11}$. From these considerations it is useful to study the resonance frequency and the equivalent resistance at resonance.
With 50 Ω terminations the reflection is relatively high for the two configurations under study and for clarity the magnitude of the reflection coefficient with 1 Ω termination is displayed in figure 3.38.

![Graph showing reflection magnitude](image)

Figure 3.38: Comparison of modelled and simulated (HFSS) magnitude of $S_{11}$ versus frequency for two different configurations with a 1 Ω termination. The scattering parameters are normalised to the 1 Ω termination.

For the first situation a resonance frequency of 430 MHz and 440 MHz is computed with HFSS and the model respectively. The equivalent series resistance at resonance is 0.045 Ω and 0.067 Ω respectively. The resonance frequency of the second situation is computed as 430 MHz and 420 MHz with HFSS and the model respectively. The series resistance at resonance is 0.2 Ω and 0.3 Ω respectively.

First of all note that the resonance frequency of the second configuration is lower than for the first configuration. This is mainly due to the relatively longer current path in the substrate of the second configuration. Also note the difference in equivalent resistance between the two situations. In the first situation this resistance is predicted reasonably well and for the second configuration a relatively large error is made. In both cases the model predicts a higher resistance than computed with HFSS. However the ratio between the simulated and modelled resistance of the two situations is roughly the same: 0.2/0.045 and 0.3/0.067 respectively. Finally note that the per unit length values of the capacitor model are taken from the EM simulations (cf. figure 3.31). The effect of the sidewalls and the finite width of the substrate are not accounted for in these simulations.

**Measurement of prematch capacitors**

Unfortunately it is not possible to measure the RF properties of prematch capacitors directly. A coplanar setup in combination with a bondwire has been used to measure the capacitor. In figure 3.39 a sketch of the measurement setup is shown.

A bondwire connects the MOS contact of the prematch capacitor with the coplanar line. The bottom contact of the capacitor is mounted on the groundplane. With this setup it is possible
to measure one-port scattering parameters. To compare the measured scattering parameters a model for the measured situation is assumed as shown in Figure 3.39. The capacitor $C_{pg}$ represents the probe to ground capacitance, $C_{wg}$ represents the wire to ground capacitance and the coplanar line is indicated by the line parameters $Z_L$, $\gamma$, $l$. The bondwire is modelled by a resistor $R_{bw}$, modelling DC and skin losses, and an inductor $L_{bw}$. The prematch capacitor is modelled by a series connection of three lumped elements: an inductor $L_p$, a resistor $R_p$ and a capacitor $C_p$. At this point several options are available to compare the models with measurement. In the first option the measured data is de-embedded for the transmission line, the $C_{pg}$ and $C_{wg}$ capacitances and the bondwire. The resultant dataset should represent the one-port scattering parameters of the prematch capacitor. In principle it should be possible to extract the parameters $L_p$, $R_p$ and $C_p$ from the de-embedded data. It is noted however that the inductance of the prematch is much smaller than the bondwire inductance and the series resistance is small compared to the system impedance. It should be possible however to extract the capacitance of the prematch from the low frequency scattering parameters with reasonable accuracy.

In the second option the measured data is de-embedded for the coplanar line and the capacitors $C_{pg}$ and $C_{wg}$. The transmission line parameters and the capacitances $C_{pg}$ and $C_{wg}$ are known from previous sections. The de-embedded scattering parameter is compared with the simulated scattering parameter. To model the bondwire inductance and resistance the bondwire model of section 3.2.3 is used. The prematch capacitor is modelled with a lumped capacitor and a resistor in series, neglecting the series inductor. The capacitance value is taken from the datasheets and the resistance value is assumed unknown. Only the bondwire geometry and the length of the coplanar transmission line are needed to compare scattering parameters of the model with the measured scattering parameters leaving the frequency dependent resistance of the prematch capacitor as a fitting parameter. Although the configuration chosen is not the best option for the measurement of resonance frequencies, the measured resonance frequencies can be compared to simulated resonance frequencies.

In the third option the measured data is de-embedded for the coplanar line and the capacitances $C_{pg}$ and $C_{wg}$. The geometry of the bondwire is measured and by using the bondwire
model, the data is also de-embedded for the inductance and the resistance of the bondwire. From the resultant data the prematch parameters $C_p$, $L_p$ and $R_p$ are extracted. Note however that in this option all errors in the de-embedding and the modelling of the bondwire return as errors in the extracted prematch parameters.

**Measurement results**

A set of samples with a 10 pF prematch capacitor and a second set with a 6.4 pF capacitor has been fabricated. From each sample a top view and a side view photo has been made to obtain the bondwire geometry and the length of the coplanar transmission line. First the capacitance values are extracted from the low frequency scattering parameters after de-embedding the data for the capacitances $C_{pq}$ and $C_{wq}$ and the coplanar line. A plot of these values versus the sample number is shown in figure 3.40. Variations less than a percent are observed from this figure. Second the resonance frequencies of the model and the measurements are compared in figure 3.40. From this figure a difference less than 30 MHz is observed for the resonance frequencies. Similar results are found for the 6.4 pF capacitors.

![Figure 3.40](image)

Figure 3.40: Results of the prematch measurements. Extracted low frequency (45 MHz) capacitance values of seven samples are shown on the left. Measured and modelled resonance frequencies are shown in the right picture for a capacitor of 10 pF.

Main limitations in the comparison of the resonance frequencies is the low resolution of the photographs used, since it was not possible to make SEM photos.

**Final remarks**

The modelling and measurements of prematch capacitors are considered in this section. The focus is on the MOS contact of the capacitors. First simulations with Em indicate that the skin effect in the silicon substrate plays an important role in the electrical behaviour. Unfortunately it is not possible with Sonnet’s Em to calculate the effects of the sidewalls of the silicon on the electrical behaviour. It would appear that these effects are non-negligible. For a clear picture of the behaviour of the capacitors it is recommended that the two- and three-dimensional simulations be repeated with a software package better suited to this problem.
Additionally, on wafer measurements of dedicated two port structures should be used to verify the model. In the upper metallisation a GSG contact is formed with the signal contact connected to the capacitor contact and the ground contacts are connected to the substrate. With this setup the capacitor is measured as a transmission line. The results can also be used for extraction purposes.

For an accurate comparison of measured and modelled resonance frequencies it is recommended that a two-port measurement setup with a shunt connection of the capacitor and the bondwire be used. An example of this setup is shown in figure 3.41.

![Figure 3.41: Prematch capacitor measurement setups. A two-port measurement is used for accurately determining the resonance frequency (a). An opening in the groundplane around the capacitor forces the current to flow in the longitudinal direction. Similar ground openings in (b) are used as a modification to the measurement setup shown in figure 3.39.](image)

A series combination of the bondwire inductance and the prematch capacitor resonates as a shunt element to ground. On three sides around the capacitor an opening in the groundplane is created forcing the current to flow in one direction only. In the actual situation, shown in the SEM photograph of figure 3.28, current in the capacitor also flows more or less in one direction. A similar opening in the groundplane is used to modify the setup, described in figure 3.39, to the structure of figure 3.41 on the right.

### 3.4 Modelling of power transistor packages

A large variety of packages are available for power transistors ranging from plastic packages for low power transistors to large ceramic packages for high power transistors. Several possibilities exist for modelling packages such as measurement-based curve-fitting procedures and rigorous electromagnetic field simulations. In all cases the general idea in this study is to represent a package as a multiport dataset (cf. figure 3.42).

The dataset has external ports to allow for connections to external circuitry and internal ports for connections to the bondwires, the prematch capacitor(s) and the die(s). A library of package models based on multiport datasets is feasible as long as the position of the internal ports does not change. If, for example, the mounting point of a bondwire changes, the position of the internal port changes accordingly and a new dataset must be built. Once a model is created it is tested by performing microwave measurements on elementary circuits mounted
in the package.
To obtain the multiport S-parameters for the package at hand, the SOT 171, two different approaches are used in this work. First the package is simulated in Sonnet’s electromagnetic simulator Em. Six external ports allow the connection of external circuitry such as sources, grounds etc. Six internal ports facilitate connections for the bondwires, the prematch capacitor and the die. The result of this simulation is a 12-port S-parameter dataset. This model is then compared to a model built with library elements directly available or implemented in MDS such as coupled transmission lines and capacitors. Finally the electromagnetic model is compared to measurements of differing combinations of bondwires and prematch capacitors mounted in the SOT 171 package.

3.4.1 Modelling of the SOT 171 package
Two independent approaches are considered for modelling the SOT 171 package. In the first approach an equivalent circuit model is created in the simulator with circuit elements found in the libraries of MDS. Examples of these circuit elements are lumped capacitors and coupled transmission lines. This equivalent circuit is used for comparison with the following method. In the second approach the package is simulated in Sonnet’s commercially available electromagnetic simulator Em. Although in principle an electromagnetic simulator gives good results, computed results must be viewed with some scepticism as the produced results are just numbers. Therefore if a method is available to verify the electromagnetic results or to make them plausible, that method should be employed. In the problem at hand the circuit model serves this purpose.

Modelling with circuit elements
The first model is built in MDS with coupled transmission line models and lumped capacitor models available in the standard components library. The effect of the ceramic cap is not accounted for. In figure 3.43 in the top left corner a scaled top view drawing of the package is shown as well as a cross-section along the line A-A’. The size of the package is 9 × 5.8 mm². In the figure on the right, internal and external ports are indicated in the SEM photograph of the BLV transistor. In the next figure the chosen equivalent circuit is superimposed on the drawing of the package.
Figure 3.43: Modelling of the SOT package with library elements. Shown on the top left a scaled top view drawing of the package. In the top right picture the SEM photo of the transistor is shown with the external and internal ports indicated. On the bottom picture the package is subdivided into nine regions each modelled with library elements available in the microwave components library of MDS. Three different metals are found: a 100 μm thick leadframe, a 3 μm gold layer for the collector and a 100 μm thick bridge.

In modelling the package three modelling elements are used: lumped capacitor models, microstrip transmission line components and coupled line models. The package is divided into nine regions and each region is modelled separately.
1. The first region represents the base connection and part of the emitter leads. The model for this region consist of three coupled lines on a BeO substrate.

2. The second region represents the open end effect of the base to the metal line of the leadframe in between the base and the collector. It is modelled by a lumped capacitor. The value of the capacitor is extracted as 120 pF from separate simulations of the open end.

3. The metal line of the leadframe to which the prematch capacitor is mounted is the third region. It is modelled by six separate microstrip transmission lines. Current flowing out of the end walls of the prematch capacitor are injected into the internal ports 8 and 9.

4. The open end effect between the metal line of region 3 and the collector is modelled by a lumped capacitor. The value of this capacitor is extracted as 210 pF from separate Em simulations of the open end effect. Because both base and collector metal are relatively wide it is expected that representing this distributed capacitance by a single lumped capacitor can introduce significant errors.

5. The fifth region represents the area from the edge of the collector metal to the internal collector port 10. This region is modelled by three coupled transmission lines on a BeO substrate.

6. The region from the internal collector port to the change in line width of the collector is the sixth region. This region is also modelled by three coupled lines.

7. From the change in width to the point under the center of the emitter bridge is modelled by three coupled lines.

8. The region of the emitter bridge is modelled by two microstrip transmission lines with the internal port 13 at the interconnection of these two lines.

9. The ninth region represents the area from the point under the center of the emitter bridge to the external collector port 5. This area is modelled by three coupled lines on a BeO Substrate.

All the parameters for the transmission lines, such as strip width and strip spacing, are taken from the technical drawings of the package. For the definition of the substrate parameters the parameters of the BeO are used. In the model 13 ports, six external and seven internal, are defined. The external ports allow the connection of the package model to external models such as grounds, transmission lines or sources. The internal ports allows the connection of the models for the bondwires, the prematch capacitor and the die to the package model. The following external and internal ports are defined:

- The external emitter ports: 1, 3, 4 and 6. These four ports are normally connected to the ground of the external printed circuit board. In the simulator they are grounded directly, ignoring pcb effects.
- The external base port: 2. This port is connected to the base line of the printed circuit board.
- The external collector port: 5. This port is connected to the collector line of the printed circuit board.
• The internal base port: \(7\). Bondwires connect this port to the prematch capacitor. In principle the number of internal base ports should be equal to the number of these base bondwires i.e. two base bondwires in the problem at hand, see figure 3.43. For reasons of simplicity only one port is used i.e. both bondwires are connected to this port.

• The internal prematch capacitor ports: \(8\) and \(9\). In the prematch capacitor model introduced previously current flows out of the capacitor at the end walls. These two currents are injected into the package at the internal prematch capacitor ports.

• The internal collector port: \(10\). Current is flowing from the external collector into the collector of the die. The transition from package to the die is at the internal collector port. In practice this current is distributed over an area with the size of the bottom of the die.

• The internal bridge connection ports: \(11\) and \(12\). A metal strip 1 mm wide and 4 mm in length bridges the one emitter lead to the other lead crossing over the collector. The points where this bridge is connected to the leadframe are the bridge connection points with associated ports.

• The internal emitter bridge port: \(13\). In the BLV 910 transistor four emitter bondwires are mounted from the die to the ohmic contact on the prematch capacitor and four bondwires are mounted to the emitter bridge.

It is noted that in some cases the coupled transmission line models could not handle the large ratio’s between strip width, strip spacing and the substrate height. For these cases own models were created. These models are based on the modelling of the quasi-TEM wave propagating along the line using Poisson’s equation (cf. section 2.10). The numerical method used is the method of moments in combination with a Green’s function for a multilayered substrate.

**Electromagnetic simulation of the package**

In the second approach the package is simulated in Sonnet’s Em. First the BeO substrate is defined with a thick layer of air on top of it. A grid is chosen on which the metallisation is defined. In the electromagnetic simulation the metallisation is represented by subsections where certain boundary conditions are applied. On each subsection a current density in \(x\) and \(y\) direction and a charge density represent the actual \(x\) and \(y\) current densities and charge densities in that subsection. By enforcing boundary conditions on the subsections the values of current- and charge densities are computed through a numerical procedure. The grid size controls the size of these subsections. If the grid is made smaller, i.e. the size of the subsections is reduced, the actual current- and charge densities are better represented. Note however that calculation time increases if the grid size is decreased. Throughout the calculations the thickness of the metallisation is assumed zero. The simulation setup is shown in figure 3.44. In the picture on the left the package is shown in the center with interconnecting lines on the left and on the right of the package. The interconnecting lines serve two purposes. In the electromagnetic simulations metal side walls are assumed on all six sides of the box. By introducing the interconnection lines the effect of these metallic side-walls on the package is reduced.

Secondly the lines allow a quasi-TEM wave to start propagating at the box-walls. These waves excite the package and mimic the way the package is excited in practical situations. In calculating the scattering parameters the effect of these transmission lines is removed by a de-embedding procedure.

In figure 3.44 on the right a closeup of the package is shown. All the numbered internal
ports are autogrounded internal ports. Autogrounded ports are connected on one side to the edge of a metallisation and on the other side to ground. Additional metallisation between the metal edge and ground is not allowed in the simulator. Therefore it is not possible to define the emitter bridge with an internal port. The effect of the emitter bridge is accounted for by connecting two microstrip transmission line elements to the internal ports 11 and 12 on one side. On the other side the microstrip lines are connected together forming the internal port 13. Each microstrip line is 1 mm wide and 2 mm in length defined in air 100 µm above ground.

With a grid size of 200 × 200 µm² the number of subsections used for the structure of figure 3.44 is 2268. Simulation times on an HP-735 with this grid is 520 seconds per frequency point.

A number of effects are neglected in the electromagnetic simulations:

- Thickness of the leadframe. The leadframe has a thickness of 100µm while in the simulations zero thickness is assumed. This mainly effects edge capacitances in the package from base lead to emitter leads and from the collector to the emitter leads. The thickness is taken account of in the loss calculations by including it in the DC and RF resistance of the metal.
- Ceramic cap. The ceramic cap is placed on the leadframe to protect bondwires, die and prematch capacitor. By representing the cap by five dielectric bricks it should be possible in principle, to simulate this effect with Sonnet’s Em. In practice this proved impracticable due to limited computing power.
- Transition from PCB to package. The power transistor is soldered to two PCB’s. The effect of the transition from PCB to package is not accounted for in the simulations. If for example a narrow air gap is present between substrate and package a substantial
characteristic impedance discontinuity is introduced.

- Emitter bridge. Due to limitations in the autogrounded ports it is in principle not possible to simulate the emitter bridge, and its associated internal port (13) with autogrounded ports. The alternative is to use two microstrip transmission line models in series connected to port (11) and port (12) respectively. Port (13) is located at the series connection of the two transmission line model.

- Representation of areas by single ports. In several places current is injected in (large) areas. For reasons of simplicity these areas are represented by a single internal port. For example the collector current of the die is injected in an area of approximately $1 \times 1.1 \text{ mm}^2$.

Comparison of circuit elements model and electromagnetic model

The electromagnetic simulation model and the circuit element based model are compared for two cases. In the first case the internal base port (7) and the internal collector port (10) are grounded. The results of this comparison are shown in figure 3.45. Reasonable agreement up to 3 GHz is found in the magnitude of $S_{11}$ but a significant difference in the magnitude of $S_{21}$ is observed. Significant differences are also found in the phase of the reflection parameters. The phase of $S_{11}$ and $S_{22}$ in this configuration are related to the transmission line effect at the input and output respectively. In a practical situation this effect transforms the low impedance at the input and the output respectively to another impedance. Consequently, this phase must be modelled with good accuracy by the electromagnetic simulator because any length effect not accounted for substantially affects the accuracy of the input and output impedance modelling.

The phase of both $S_{11}$ and $S_{22}$ is substantially affected by the current crowding in the base and collector respectively. This effect is illustrated in figure 3.46. In the circuit model the leadframe on the base side is modelled by three coupled transmission lines with the center line connected to ground. The associated current flow in the circuit model is shown in figure 3.46 on the left. In practice however the current crowds to the grounded internal base port as shown in the same figure on the right, increasing the phase change of $S_{11}$. A similar effect occurs on the collector side.

The difference in the magnitude of the transmission parameters is mainly due to the distributed nature of the coupling between base, the metal strip where the prematch capacitor is mounted and the collector. In the circuit model both base and collector are fully grounded while in the electromagnetic model only the part of the internal ports of base and collector is grounded.

In the second example the circuit of figure 3.47 is connected to the internal ports (7), (8), (9) and (10).

This example represents the situation of a 80 pF prematch capacitor mounted in the package with bondwires, with a 1 nH inductance, connected from base to the prematch capacitor and from the collector to the prematch capacitor. The magnitude of $S_{11}$ and $S_{21}$ and the phase of $S_{11}$ and $S_{22}$ are plotted in figure 3.48 as function of frequency.

For reasons of completeness the results without package effects are also plotted in the figure. In this case port (7) and (10) in figure 3.48 are the input- and output respectively and ports (8) and (9) are directly grounded.
Figure 3.45: Comparison of the electromagnetic model with the circuit elements model with the internal base and the internal collector grounded. The solid lines represent the electromagnetic model and the dashed lines represent the circuit element based model. The internal base port and the internal collector port are short circuited. Shown on the top the magnitude of $S_{11}$ and $S_{21}$ and plotted on the bottom the phase of $S_{11}$ and $S_{22}$.

Figure 3.46: Modelling of current flow on the base side of the package with a grounded internal base. In the middle picture the package is shown. Shown on the left the assumed current flow in the circuit model. The actual current flow crowds to the short circuited internal port as indicated in the figure on the right. This crowding effect affects the phase of $S_{11}$ substantially.
Figure 3.47: Circuit for comparing the electromagnetic model with the circuit model representing a prematch capacitor connected to the base and collector by bondwires.

A substantial difference between the model without package effects and the two models with package effects included is observed for frequencies above a few hundred MHz. Additionally, reasonable agreement between electromagnetic simulations and the circuit model is found up to 3 GHz. Above 3 GHz significant differences are found.

In conclusion an electromagnetic model based on simulations in Sonnet’s Em is created. This model has six external ports and six internal ports. Since it is not possible to define an internal port at the emitter bridge, this bridge and the seventh internal node are introduced separately by connecting a series of two microstrip transmission line models to two internal ports of the package model. To make a first verification of the model S-parameters are compared with the S-parameters of a circuit model. Results indicate that the S-parameters computed by the electromagnetic simulator can be used to model the package. However, further comparison with measurements is necessary. Parts of this comparison are discussed in section 3.5.

### 3.4.2 Discussion of electromagnetic simulation with internal ports

An important issue is the use of internal ports in electromagnetic simulations. This problem is encountered in the problem at hand in the modelling of the bondwire from the die to the emitter bridge.

At the internal collector an autogrounded port is used. It is not possible to create such a port on the emitter bridge because there may not be any additional metallisation between the port and ground. Two different types of internal ports are available in Sonnet’s Em.

- Autogrounded internal ports are connected on one side to the edge of a metallisation and on the other side they are connected to the bottom ground plane. A metallisation between the top side of the port and the ground plane is not allowed. Additionally, the distance between the top side of the port and the ground plane should not be too large to avoid de-embedding problems.
- Ungrounded internal ports are connected on both sides to edges of metallisation. This type of "floating" port is used to allow for the connection of for example SMD components.

Although trivial, it is important to note that in both cases current flowing into one side of the port leaves the port on the other side. There are two drawbacks in using autogrounded
Figure 3.48: Results of the second comparison of the electromagnetic model with the circuit elements based model. The solid lines represent the electromagnetic model, dashed lines represent the circuit element based model and the dotted line represents the results of the ideal circuit. The circuit of figure 3.47 is placed in the 12 port dataset. Shown on the top the magnitude of $S_{11}$ and $S_{21}$ and plotted on the bottom the phase of $S_{11}$ and $S_{22}$.

Figure 3.49: Cross sectional view of the package with an internal port at the collector and an internal port at the emitter bridge.
ports for the problem at hand. Firstly it is not possible to use an autogrounded internal port to access the point in the center of the airbridge (port 13 in the SEM photo of figure 3.43). Secondly the "length" of the autogrounded ports is relatively long compared to the dimensions of the package. Both problems are avoided with ungrounded internal ports. Therefore it is worthwhile to explore the use of these ports further.

As an example consider the simulation setup of two grounded microstrip lines shown in figure 3.50.

Figure 3.50: Internal ports in Sonnet's Em. Shown on the left two auto-grounded ports on the edge of two shortcircuited pieces of transmission lines. Both top- and side view are shown. One side of the port is connected to a metal edge and the other side is automatically grounded. As a major drawback of these ports there may be no metallisation between the top side of the port and the ground. Shown in the middle an ungrounded internal port on the edges of the microstrip lines. Both sides of the port are connected to an edge of metallisation. It is important to note that for any dataset used in a simulation the current flowing out of the port ($I_{out}$) is made equal to the current flowing into the port ($I_{in}$).

A small gap is located between the two adjacent line ends. In the figure on the left autogrounded ports are connected to each side of the port. In the next figure an ungrounded port is connected to each edge of the metallisation. Both cases can be simulated in Sonnet's Em and the resulting data is read into a MDS dataset. Circuitry, such as passive- and active elements and sources, is connected to these datasets. As an example consider the case of a current source connected to the dataset as shown in figure 3.51.

Figure 3.51: Circuits with datasets obtained from for example electromagnetic field simulations with internal ports (cf. figure 3.50). On the left the circuit with a two-port dataset. Forcing a current in the first port, doesn't affect the current in the second port. On the right a circuit with a one-port dataset. Forcing a current into one side of the port results in an opposite current in the other side of the port.

First the case of autogrounded ports is considered. In the electrical simulator a current source
is connected to the first port and the second port is short circuited. Simulating this circuit results in zero current flow in the short circuited port. Next the case of the one-port dataset is considered. A current source is connected between one side of the port and ground and the second side of the port is connected to ground. Forcing a current $I_{\text{source}}$ into one side of the port results in the opposite current in the second side of the port because the relation $I_{\text{in}} = I_{\text{out}}$ holds (cf. figure 3.50).

From the previous discussion it is evident that the use of ungrounded ports, although potentially desirable, is rather limited in our specific case.

At this point the idea is as follows: the package is simulated with ungrounded internal ports at the positions where ports are needed for bondwires, prematch capacitor and die. These internal ports are connected with each other through known interconnections. Then the sides with the known interconnections of the internal ports are short circuited and desired components such as bondwires, prematch capacitor and die are connected to the other side of the internal port. This idea is illustrated in figure 3.52 for the case of two internal ports.

![Diagram](image)

Figure 3.52: Attempt to connect a desired component, an inductor $L$ to a dataset with ungrounded internal ports. For reasons of simplicity only the two ungrounded internal ports are shown in the figures. The package structure is simulated with a standard between the plus sides of the internal ports (a). The dataset of the structure is simulated with the plus sides grounded and the desired component $L$ connected to the minus sides as shown in (b). Unfortunately this principle does not work because the S-parameters of the structures shown in (c), (d) and (e) are equal and indistinguishable.

The other internal and external ports are not indicated for reasons of simplicity. The package is simulated with the standard between the plus (+) side of the two internal ports as shown in figure (a). The results of the electromagnetic simulation are read into a dataset and in the circuit simulator the plus sides of the dataset, with the standard in between them, are both grounded and the desired structure is connected to the minus (-) sides of the dataset as shown in figure 3.52.b. Unfortunately this principle does not work as is demonstrated in the pictures (c), (d) and (e). Suppose, for example, that the standard is connected to the plus sides of the internal ports and a resistor is connected to the minus sides as shown in figure (c). The S-parameters of this structure are equivalent to and indistinguishable from the S-parameters of the structures shown in figures (d) and (e). It is concluded that if internal
ports are used with a sophisticated interconnection scheme between them, the resultant data must be de-embedded for this interconnection scheme. It is not possible to ground or leave open one side of the internal port and connect the desired structure to the other side of the internal port.

In the following a candidate de-embedding scheme is discussed: series de-embedding. First a structure is simulated electromagnetically with a standard connected between the two plus (+) sides of the internal ports shown in figure 3.53.a.

![Diagram](image)

Figure 3.53: Series de-embedding of a dataset. A known standard is connected between the plus (+) sides of two internal ports (a). To de-embed the opposite of this standard is connected externally to the internal ports (b). In principle after this de-embedding step the two plus (+) sides are connected together (c). It should be possible to connect external components such as an inductor by short circuiting one internal port and inserting the component in the other internal port (d). Unfortunately shunt de-embedding does not work because the S-parameters of the dataset with the internal structure shown in (e) are the same as the S-parameters of the structure in (f). (cf. 3.52). Shunt de-embedding both datasets with the negative standard, as shown in (b), produces differing results.

In the second step the opposite of the standard is connected between the plus and minus side of one internal port (b). This series de-embedding yields a dataset with two internal ports with one side of an internal port connected to one side of the other internal port as shown in (c). Desired components, such as an inductor is insertable by connecting it to one of the internal ports and short circuiting the other internal port (d). It is noted that although the S-parameters of the datasets of figures (e) and (f) are equal, series de-embedding both datasets for the standard yields the same results, as opposed to shunt de-embedding. It is noted that in the above examples the interaction between package and standard is assumed negligible. Although the effect of the standard itself is removed by series de-embedding, the interaction between standard and package is still present in the dataset. If there is interaction, it is recommended that the standard be chosen as close as possible to the desired structure that is to be inserted later. In that particular case the interaction between package and standard is roughly the same as the interaction between the desired structure and the package. Suppose for example that a dataset is needed with internal ports to allow for the connection of the bondwire model for one bondwire to the package dataset. As a standard the bondwire, or a structure as close as possible to that bondwire, should be used. Using this standard will approximately include the
coupling between the desired structure and the package.

From the previous examples two conclusions may be drawn:

1. Simulating a package with internal ports, grounding one side of the internal ports and connecting desired circuitry to the other side of the internal ports is not possible. This is illustrated in figure 3.52.

2. Simulating a package with a known standard between one side of the internal ports and series de-embedding for this standard is, in principle, possible. This is shown in figure 3.53.

Although the series de-embedding technique is not further explored in this work, it may prove a valuable option to generate datasets with internal ports at critical positions where it may not be possible to use autogrounded ports.

3.4.3 Assessment of package emitter inductance

The assessment of the effects of the package on the overall behaviour of the transistor is a complicated task. At this stage of the work only the separate components are modelled electrically, the complete RF electro-thermal behaviour is still to be considered. To study the effect of the package, the power transistor must be analysed using Harmonic Balance algorithm and the computed currents and voltages at the internal and external ports must be studied in detail. On the other hand, in common emitter bipolar power stages the emitter inductance has a very large impact on the electrical performance of the device. The gain of such devices decreases rapidly with increasing emitter inductance. From this point of view it is worthwhile to estimate the emitter inductance introduced by the package under practical conditions without going into a full Harmonic Balance simulation.

To make an estimation of this effect, the following simulation setup is chosen: the external collector (cf. figure 3.43. port 5) is excited by an AC voltage source and all other external ports are short circuited (ports 1, 2, 3, 4 and 6). Current flowing from the external collector to the internal collector port (port 10) is injected into the internal ports while the emitter current of the die is injected into the package i.e. into the prematch capacitor grounding ports 8 and 9 and the internal emitter bridge port 13. With this setup, shown in figure 3.54, the mutual effect of the collector current on the emitter currents is included in the simulation.

The voltage at the internal collector port and the total current injected into the ports 8, 9 and 13 are calculated. The ratio between these two quantities gives a first impression of the impedance seen at the emitter of the die in the direction of the package. The imaginary part of this impedance divided by the angular frequency ($\Im(Z)/\omega$) is the inductance seen by the emitter of the die in the direction of the package. The observed imaginary part of this impedance is shown in figure 3.54 as function of frequency. It is noted that the trace is a linear function of frequency indicating a $\\omega L$ behaviour with an inductance of around 0.17 nH. Although a number of effects are not accounted for in this simplified situation, it gives an estimate of the inductance introduced by the package in the emitter of the transistor.
Figure 3.54: Assessment of package induced emitter inductance. A voltage source is connected to the external collector with the other external ports grounded. Current flows from the external collector to the internal collector. In the circuit simulator the internal collector is connected to the prematch capacitor ports and the emitter bridge port. The current flows from these ports to ground. By calculating the ratio between the voltage and the current at the internal collector port, a first impression is obtained of the impedance seen from the emitter of the die into the package. On the right the imaginary part of the impedance is plotted as function of frequency.

3.5 Measurement of packaged structures

Unfortunately two factors make it rather difficult to verify the package modelling directly by measurement. First of all measuring scattering parameters of low impedance packages in a 50 Ω environment can introduce significant errors, especially for larger packages. Secondly, in an (electromagnetic) simulator it is possible to introduce internal ports but in scattering parameter measurements this is rather complicated.

In this work several combinations of bondwires and prematch capacitors are mounted inside the SOT package. Two-port scattering parameters of these packages are measured with the external emitters grounded, the external base is connected to port 1 and the external collector is connected to port 2 of the network analyser and all other external ports are grounded (cf. figure 3.43). Although not all measured samples are discussed here, a good impression of relevant samples is given:

- An empty package.
- A sample with two bondwires from base to the prematch capacitor.
- A sample with two bondwires from the base to the prematch capacitor and two wires from this capacitor to the collector.
- A sample with two bondwires from the base to the prematch capacitor and two wires from this capacitor to the emitter bridge.

All samples are measured in a home made microstrip testfixture in the range of 500 Mhz and 3 Ghz. The measurement system is calibrated using a TRL (thru-reflect-line) calibration.
Empty package

The first sample under consideration is an empty package. A number of scattering parameters are of interest. First of all the phase of $S_{11}$ more or less describes the electrical length of the path from the external base to the internal base. The measured and modelled phase is shown in figure 3.55.

![Graphs showing phase and magnitude of S-parameters](image)

Figure 3.55: Comparison of modelled and measured S-parameters of an empty package. Three dashed lines indicate measured data of three separate measurements and the solid line represents the model.

A significant difference between modelled and measured phase is observed. This difference is mainly due to the inaccurate modelling of the capacitance from the base lead to the emitter. In the electromagnetic simulations the thickness of the leadframe and the ceramic cap are not taken into account. Simulations using HFSS indicate that these two effects increase this capacitance in the order of 80-100 fF. The second parameter of interest is the magnitude and phase of the transmission coefficient $S_{21}$. From the figure a substantial difference between model and measurement is observed. Additionally, the electromagnetic model computes a resonance around 2.6 GHz. Further investigation shows that adding a capacitance of 30 fF between the internal base and the internal collector reduces the difference between the model
and the measurement substantially. Note that in practice the additional circuitry of bondwires, prematch capacitor and die increase the transmission loss to much higher levels. Finally the phase of $S_{22}$ is, roughly speaking, related to the electrical length of the path from the external collector to the internal collector. Note that this phase is very well modelled.

In the following discussions of measured samples the extra capacitance from the base lead to the emitter (90 fF) and the extra capacitance from the internal base to the internal emitter (30 fF) are added to the model.

### 3.5.1 Two base bondwires and a prematch capacitor

In this example two bondwires are connected in parallel from the base to the prematch capacitor. A top- and a side-view SEM photo are shown in figure 3.57. The internal port on the base lead is indicated with $\textcircled{7}$ and the prematch capacitor ports are indicated by $\textcircled{8}$ and $\textcircled{9}$. The resulting measured and modelled scattering parameters are also shown in the figure. First the magnitude of $S_{11}$ is plotted versus frequency. Significant differences are found between model and measurement but it is noted that measuring this parameter accurately is rather difficult in this situation with connection problems between the sample and the test fixture proving particularly troublesome. The second plot shows the phase of the reflection parameter. Although model and measurement correspond well, the difference is about 8 degrees at 3 GHz. Another parameter of interest is the magnitude of $S_{21}$. Because nothing is connected to the collector the same behaviour is expected as in the case of the empty package. By comparing the two results substantial differences are found however. For example the measured magnitude of $S_{21}$ at low frequencies in the empty package is -40 dB where in the current sample this value decreases to -55 dB. And at 3 GHz $|S_{21}|$ is -34 dB for the empty package and -24 dB for the sample under consideration.

Two explanations are possible for this behaviour. First of all, the signal going from the base through the bondwires and the prematch capacitor is injected in the package at the ports $\textcircled{8}$ and $\textcircled{9}$. Compared to the empty package at lower frequencies more signal is reflected and at higher frequencies more signal is transmitted to the collector area. This is further illustrated in figure 3.56.

Shown on the left is the modelled $|S_{21}|$ of the empty package and the sample under consideration and shown on the right are the measured results for both cases. Both measurement and model predict significant differences between the two cases. Additionally, the model for the sample under consideration predicts a $|S_{21}|$ roughly 6 dB lower than the measured $|S_{21}|$. The second explanation for the difference between the empty package and the packaged structure of is the presence of the prematch capacitor and the bondwires. The addition of these two elements changes the coupling between base lead, emitter lead and collector lead.

### 3.5.2 Two base bondwires, a prematch capacitor and two collector bondwires

The third sample under consideration contains one prematch capacitor, two bondwires from the base lead to this capacitor and two bondwires from capacitor to the collector lead. A top- and side view are shown in figure 3.58. It is observed that all parameters are well modelled, especially the important resonance at 950 MHz in $|S_{21}|$ is as predicted, $|S_{21}|$ is not modelled
correctly around 2.1 GHz, however. The difference is due to some additional capacitance between base and collector not accounted for in the model.

### 3.5.3 Two base bondwires, a prematch capacitor and two emitter bondwires

In the last packaged structure discussed here two bondwires are mounted from the base lead to the prematch capacitor and two wires are connected from the capacitor to the emitter bridge of the package. A sideview and a topview SEM photo are shown in figure 3.59. Measured and modelled reflection and transmission parameters are shown in the same figure. A significant difference in the magnitude of $S_{11}$ is observed although it is noted that it is rather difficult to measure this parameter with high accuracy in this case. The phase of $S_{11}$ is modelled quite well, with a maximum difference of 10 degrees at 3 GHz. Once again significant differences are found in the magnitude of $S_{21}$.

### 3.5.4 Conclusions and discussion

The modelling of the SOT 171 package is considered in this section. The modelling is based on electromagnetic simulations with Sonnet’s Em allowing the definition of both external and internal ports. Although the programme makes a rigorous electromagnetic analysis, four effects are not taken into account in the simulations: the effect of the ceramic cap, the thickness of the metallisation, the transition from the printed circuit board to the package and finally the current flow at high frequencies (skin effect) is accounted for in an approximate sense. Based on a circuit element model the electromagnetic results are made plausible. An important issue in the electromagnetic analysis is the use of (un)grounded internal ports to facilitate internal nodes for the connection of bondwires, prematch capacitor and die. In this work it is shown how these ports can be used to create internal nodes.

Finally the electromagnetic model is compared with measured results of combinations of a prematch capacitor and bondwires mounted in a SOT 171 package.
Due to the relatively high frequencies the electrical behaviour has a substantial influence on the performance of RF power transistors. Therefore on the one hand it is important to know this behaviour either through calculation or through measurement. On the other hand the degrading electrical effects of the package should be reduced to the minimum. Unfortunately it happens too often that a designer is given a particular package and then the design of the shape of the bondwires and the choice of the prematch capacitor are optimized for maximum performance. In other words, the package is usually not a variable in the optimization process. The BLV 910 transistor is a good example in this respect as the package introduces significant parasitics reducing the performance of the transistor substantially. The collector lead of the package is much too large for the small die and the emitter path introduces too much parasitic emitter inductance reducing the gain of the transistor substantially. If for example the collector lead is reduced the emitter bridge in the SOT package can be made smaller reducing the parasitic emitter inductance.
Two base bondwires and a prematch capacitor

Figure 3.57: Comparison of modelled and measured scattering parameters of the structure shown in the top SEM photos.
Two base bondwires, a prematch capacitor and two collector bondwires

Figure 3.58: Packaged structure with two bondwires from the base lead to the prematch capacitor and two bondwires from the capacitor to the collector lead. The measured (dashed lines) and modelled (solid line) magnitude and phase of $S_{21}$ is plotted as function of frequency.
Two base bondwires, a capacitor and two emitter bondwires

Figure 3.59: Packaged structure with two bondwires from the base lead to the prematch capacitor and two bondwires from the capacitor to the emitter bridge. The measured (dashed lines) and modelled (solid line) magnitude and phase of $S_{21}$ is plotted as function of frequency.
Chapter 4

Electro-thermal modelling and measurement

4.1 Introduction

In RF silicon bipolar power transistors temperature significantly affects the electrical behaviour of the transistor. Additionally, extreme temperatures may damage the transistor. Consequently, in the modelling of power transistors the thermal behaviour should be accounted for in electrical simulations of the power transistor. In the following a brief outline is given of the electro-thermal modelling implemented in MDS within the framework of this project.

To be able to handle electro-thermal problems in an electrical simulator such as MDS, temperature is represented by voltage and heat dissipation is represented by current. This representation allows the straightforward computation in the electrical simulator of temperature, following Ohm’s law \((V = I R)\), as the product of dissipated power and thermal impedance: \(T = P_{\text{diss}} Z_{\text{TH}}\).

The electrical behaviour of the die is modelled by a compact transistor model. If temperature increases, e.g. due to power dissipation in the die, the electrical behaviour of the die changes must be reflected in the compact transistor model. In other words a compact transistor model is required with the correct temperature dependence of the compact model parameters. This scaling is commonly referred to as “temperature scaling”. The Mextram model used in this thesis is one of the few advanced models available in the public domain with a working set of temperature scaling rules.

To begin a temperature node must be added to the compact transistor model. This process is illustrated in figure 4.1. Shown on the left is a compact transistor model with three nodes: a collector, a base and an emitter. The dissipated power of the compact model is computed from terminal node voltages and currents: \(P_{\text{diss}} = (V_c - V_e) I_c + (V_b - V_e) I_b\). The dissipated power is represented by a current source with current flowing out of the transistor to the “temperature node” as shown in figure 4.1 in the middle. By connecting a thermal impedance \(Z_{\text{TH}}\) to the
temperature node, the temperature $T$ is computed as the product of dissipated power and the thermal impedance $T = P_{diss} Z_{TH}$. Note that thermal resistance ($R_{TH}$) is used in case of steady state heat conduction and thermal impedance ($Z_{TH}$) in other cases. The electrical parameters of the compact transistor model are then updated by applying the temperature scaling rules using the new temperature and also the dissipated power and the temperature are recomputed.

![Diagram of thermal model](image)

Figure 4.1: Adding a thermal node to a compact bipolar transistor model. Shown on the left a three terminal model with a collector, base, and emitter. In the middle: the dissipated power is computed as $P_{diss} = (V_c - V_e) I_c + (V_b - V_e) I_b$. In the compact model the dissipated power is represented as a current flowing out of the transistor model to a temperature node. The voltage at this node, the product of the current $P_{diss}$ and the thermal impedance $Z_{TH}$, represents temperature.

Of course, a compact transistor model with a thermal node and correct temperature scaling rules of the electrical parameters is not enough. A good thermal model of the environment of the transistor is essential to the computational process.

As discussed in section 2.9 the major portion of the heat flow in the power transistors is through heat conduction. Heat is generated in the active areas and flows into the silicon die. From the silicon it flows through the beryllium oxide (BeO) substrate to the solid mounting base. The governing heat conduction equation is given by equation (2.26) which is repeated here for reasons of convenience:

$$
\frac{\partial}{\partial x} \left( \kappa \frac{\partial T}{\partial x} \right) + \frac{\partial}{\partial y} \left( \kappa \frac{\partial T}{\partial y} \right) + \frac{\partial}{\partial z} \left( \kappa \frac{\partial T}{\partial z} \right) + g(x, y, z, t) = \rho c \frac{\partial T}{\partial t} \tag{4.1}
$$

The parameters of the body are the thermal conductivity $\kappa$ (W/m-K), the specific heat $c$ (J/kg-K) and the material density $\rho$ with units kg/m$^3$. The rate of energy generation per unit volume is given by $g(x, y, z, t)$ (W/m$^3$). For the materials involved the values of $\kappa$, $c$ and $\rho$ depend on temperature.

For the problem at hand the cycle-time of the RF signal is much shorter than the thermal time constants. Consequently, the right-hand side of equation (4.1) is negligible and the temperature dependencies of $c$ and $\rho$ are not considered. In the case of pulsed power transistors, however, where the pulse width and pulse repetition time are in the order of the thermal time constants these effects must be taken into account. In the study of the thermal transient of a power transistor the right-hand side of equation (4.1) of course may not be assumed zero (cf. section 4.4).

Throughout this work the temperature dependency of $\kappa$ is taken account of through the use of Kirchhoff's transformation (cf. section 4.2).
In order to gain insight into the thermal transient behaviour first a one-dimensional model is introduced in section 4.3 using temperature independent $c$ and $\rho$. Although this model is not of practical use since heat spreading is ignored, it does provide the opportunity for introducing analytic expressions and a building basic understanding of heat conduction. In section 4.4 the one-dimensional model is extended to include heat spreading. The resultant model can be used to accurately describe the transient thermal behaviour of a power transistor. Using this model, transient behaviour is studied by applying a pulse to the power transistor and monitoring transistor warming which follows the "heating up curve". This curve describes the temperature as function of time when a power pulse is applied.

Both of these models are one port models based on the assumption that the electro-thermal behaviour of the complete die can be modelled by a single compact transistor model. It is possible to use one such model per active area, but thermal interaction between active areas is then neglected. The underlying assumption in both these cases is that the temperature gradient within one active area does not have a significant effect on the electrical performance.

To investigate this issue further and before discussing more complex models, the measurement of the temperature distribution within an active area and the measurement of thermal impedance is considered in section 4.5. Four types of (electro-) thermal measurement are considered:

1. Infrared measurements
2. Contact probing measurements
3. Measurements using liquid crystals
4. Electro-thermal measurements

The first three are discussed in brief and the four is discussed in more detail since in the latter case these measurements the relation between the base-emitter voltage and temperature at low current levels is used to measure the thermal impedance of a transistor by measuring the external base-emitter voltage after applying a power pulse heating up the transistor. Because in an active area of the transistor a temperature profile is found, the measured base-emitter voltage can only be related to an equivalent temperature. A crucial question is how this equivalent temperature is related to the temperature profile in the active area.

Before investigating the electro-thermal interaction, the three-dimensional thermal resistance modelling of power transistors is discussed in section 4.6. Two modelling methods are discussed in brief: 1) using a net of resistors and capacitors to build a thermal model for the structures involved and 2) using Green's functions to compute the thermal resistance matrix directly. For implementation in MDS the second approach, using a Green's function, is found most suitable with respect to simulation times. Based on this method an attempt is made to further simplify the model by looking at the effect of the finiteness of substrates and the temperature at the interface of materials for the case of the BLV 910.

Finally to investigate the temperature gradient within an active area and its effect on the electrical behaviour of the die, a three dimensional thermal model is build for the BLV 910. The investigation considers the following: the die of the BLV 910 has eight active areas and each active area has its own temperature profile. Each active area is represented by multiple compact transistor models, each model having its own temperature node. These models are connected to a multiport thermal model representing the power transistor. In principle with
this full model it is possible to compute the temperature profile within an active area and the
temperature profile of the complete die. This process is illustrated in figure 4.2 where one
active area is modelled by 12 compact transistor models and a thermal matrix model with 12
ports. To model a full transistor with 8 active areas $8 \times 12$ compact models and a thermal
matrix model having $96 \times 96$ elements are needed.

Figure 4.2: Schematic overview of the thermal modelling of a power transistor using 12 compact models
per active area. Shown on the top left the die with eight active areas. Shown on the top right one active
area modelled by $2 \times 6$ compact models, each compact model having its own temperature node. The
total number of compact models used to model the power transistor is: $8 \times 2 \times 6 = 96$. To model
the thermal interaction within an active area a thermal matrix model is needed with $12 \times 12$ entries as
shown on the bottom. If also thermal interaction between active areas is modelled the thermal matrix
model has 96 elements in this particular case.

Important questions related to this problem are solved in this chapter:

- Is it possible to run a complete electro-thermal simulation in MDS with each active
  area being represented by multiple compact transistor models?
- How many compact models are needed per active area to ensure a good representation
  of the temperature profile and the electrical performance of the transistor?

4.2 The Kirchhoff transformation

The non-linearity in the heat conduction equation (2.26) is removed by introduction of Kirchhoff's transformation. The transformation relates the "linear" temperature $\theta$ to the actual
temperature $T$ through the relation [55], [56]:

$$
\theta(r) = T_0 + \frac{1}{\kappa(T_0)} \int_{T_0}^{T(r)} \kappa(T')dT'
$$

(4.2)
where \( T_0 \) denotes a reference temperature. Substituting equation (4.2) in the heat conduction equation transforms the non-linear equation to a linear heat equation:

\[
\kappa(T_0) \left( \frac{\partial^2 \theta}{\partial x^2} + \frac{\partial^2 \theta}{\partial y^2} + \frac{\partial^2 \theta}{\partial z^2} \right) + g(x, y, z, t) = \rho c \frac{\kappa(T_0)}{\kappa(T)} \frac{\partial \theta}{\partial t} \quad (4.3)
\]

As an illustration consider the circuit of a linear thermal resistance and two Kirchhoff transformations shown in figure 4.3 where thermal capacitance effects are neglected for reasons of simplicity.

![Kirchhoff's transformation diagram](image)

Figure 4.3: Illustration of Kirchhoff's transformation. The linear temperature \( \theta_1 \) and \( \theta_2 \) across the linear thermal resistance, are transformed to the actual temperatures \( T_1 \) and \( T_2 \) respectively using Kirchhoff temperature sources.

The resistance represents the steady state solution of equation (4.3). The linear temperatures \( \theta_1 \) and \( \theta_2 \) are transformed to the actual temperatures \( T_1 \) and \( T_2 \) respectively using the Kirchhoff transformation sources.

The integral in equation (4.2) is solved analytically by fitting the temperature dependence of the thermal conductivity to a power function:

\[
\kappa(T) = \kappa(T_0) \left( \frac{T}{T_0} \right)^n \quad (4.4)
\]

Substituting this equation into the Kirchhoff transformation, performing the integration and rearranging terms yields the actual temperature:

\[
T = T_0 \left( \frac{n(\theta - T_0) + \theta}{T_0} \right)^{\frac{1}{n+1}} \quad (4.5)
\]

This transformation is implemented in MDS as a Symbolically Defined Device (SDD) with two ports. One port represents the "linear" temperature \( \theta \) and the second port represents the actual temperature \( T \). For future work it is recommended that the transformation be directly implemented in the software instead of using a SDD. This will speed up computations considerably.

### 4.3 One-dimensional modelling

The one-dimensional thermal model is based on the similarity between the differential equation for the temperature under one-dimensional heat conduction and the differential equations for the voltage on a RC transmission line. The one-dimensional heat conduction equation is given by:

\[
\kappa \frac{\partial^2 T(z, t)}{\partial z^2} - \rho c \frac{\partial T(z, t)}{\partial t} = 0 \quad (4.6)
\]
where \( \kappa \) is the thermal conductivity (W/m·K), \( \rho \) is the material density (kg/m\(^3\)) and \( c \) is the specific heat (J/kg·K). In this equation the parameters \( \kappa \), \( \rho \), and \( c \) are assumed temperature independent. The one-dimensional differential equation for the voltage on an RC line is given by:

\[
\frac{1}{R} \frac{\partial^2 V(z,t)}{\partial z^2} - C \frac{\partial V(z,t)}{\partial t} = 0
\]  

(4.7)

where \( R \) is the resistance per unit length (\( \Omega/\text{m} \)) and \( C \) is the capacitance per unit length (\( \text{F/m} \)). Upon comparing equation (4.6) and equation (4.7) it is concluded that the one-dimensional linear thermal problem can be solved using a transmission line approach.

If the temperature and voltage are time-harmonic quantities, with radian frequency \( \omega \) (rad/s), the differential equations for the temperature and voltage are rewritten as:

\[
\kappa \frac{\partial^2 T(z,\omega)}{\partial z^2} - j \omega \rho c T(z,\omega) = 0
\]  

(4.8)

\[
\frac{1}{R} \frac{\partial^2 V(z,\omega)}{\partial z^2} - j \omega c V(z,\omega) = 0
\]  

(4.9)

It is interesting to note that the above differential equations have the same form as the differential equation of a plane wave in a good conductor (see for example [27] page 42-45):

\[
\frac{\partial^2 E_z(z,\omega)}{\partial z^2} - j \omega \mu \sigma E_z(z,\omega) = 0
\]  

(4.10)

where \( E_z \) is the \( z \)-component of the electric field (V/m), \( \mu \) is the permeability of the conductor (H/m) and \( \sigma \) is the conductivity of the conductor (S/m). Based on the solution of equation (4.10) the skin depth of a good conductor is defined as:

\[
\delta_s \equiv \sqrt{\frac{2}{\omega \mu \sigma}} = \sqrt{\frac{1}{\pi f \mu \sigma}}
\]  

(4.11)

The skin depth is the distance in the conductor at which the value of the electric field is \( e^{-1} \) (or 37 percent) of the value at the surface. Analogous to this skin depth, a thermal skin depth is introduced:

\[
\delta_{th} \equiv \sqrt{\frac{2\kappa}{\omega \rho c}} = \sqrt{\frac{\kappa}{\pi f \rho c}}
\]  

(4.12)

The thermal skin depth is the depth in a heat conducting material where the temperature is \( e^{-1} \) (or 37 percent) of its surface value. For e.g. silicon the thermal skin depth is around 56 \( \mu \text{m} \) at 100 MHz and drops to around 18 \( \mu \text{m} \) at 1 GHz. Consider a brick of material, as shown in figure 4.4 on the left. The planes \( z = 0 \) and \( z = L_z \) have a certain temperature i.e. heat flow takes place in the \( z \)-direction. This heat flow is modelled by a transmission line, as shown in the same figure on the right, with a thermal resistance per unit length \( R_{th} \) and a thermal capacitance per unit length \( C_{th} \):

\[
R_{th} = \frac{1}{\kappa \frac{L_z}{L_y}}
\]  

(4.13)

\[
C_{th} = \rho c \frac{L_z}{L_y}
\]  

(4.14)
Figure 4.4: Brick of heat conducting material. The temperatures at the planes \( z = 0 \) and \( z = L_z \) are assumed constant and heat conduction is in the \( z \)-direction. A transmission line with a thermal resistance \( R_{th} \) and capacitance \( C_{th} \) per unit length is used to model the one-dimensional heat conduction.

The voltage at one end of the line represents the temperature of one plane and the voltage at the other end of the line represents the temperature at the other plane. The impedance and propagation constant of the transmission line are given by:

\[
Z = \sqrt{\frac{R_{th}}{j\omega C_{th}}} = \frac{1}{L_x L_y} \sqrt{\frac{1}{j\omega \kappa c}}
\]

(4.15)

\[
\gamma = \sqrt{j\omega R_{th} C_{th}} = \sqrt{\frac{j\omega \kappa c}{\kappa}}
\]

(4.16)

The input impedance of a transmission line, short circuited at one side is given by:

\[
Z_{in}(\omega) = Z \tanh(\gamma L_z)
\]

(4.17)

where \( L_z \) is the length of the transmission line (m). Please note that the input impedance at DC is equal to the thermal resistance per unit length divided by the plate area and multiplied by the plate distance:

\[
Z_{in}(0) = \frac{L_z}{\kappa L_x L_y}
\]

(4.18)

As an example consider an active area of \( 50 \times 300 \, \mu m^2 \) on a silicon substrate of 120 \( \mu m \) in height with a thermal conductivity of 156 W/m·K. From these values the thermal resistance is computed using the above equation as 51 K/W.

It can also be shown that for very high frequencies the input impedance is zero:

\[
\lim_{\omega \to \infty} Z_{in}(\omega) = 0
\]

(4.19)

The transmission line can be approximated by a cascade of resistors and capacitors as shown in figure 4.5.

In this figure the resistors conduct the heat and the capacitors store the heat. Suppose the transmission line is approximated by \( N \) resistors and \( N - 1 \) capacitors. The values of the resistances and the capacitances are given by:

\[
R_{LE} = \frac{1}{\kappa} \frac{L_z}{L_x L_y N}
\]

\[
C_{LE} = \rho c \frac{L_x L_y L_z}{N - 1}
\]

(4.20)
It is noted that the input impedance of the lumped element circuit at DC is \( N \cdot R_{LE} \), and at high frequencies the input impedance is equal to \( R_{LE} \). If the number of elements \( N \) is taken large, the input impedance at high frequencies is small. The thermal transmission line model is implemented in MDS using a user defined model. Note that user defined models are implemented in the frequency domain. Simulations with this model in the time domain, to study the thermal transient, produce incorrect results. The reason for this incorrect behaviour is not known to the author. In these cases the lumped element approximation is found very useful.

### 4.4 Heat spreading

Before more complex thermal models are introduced, the effect of heat spreading is included in the transmission line model. The effect of spreading reduces the thermal resistance and increases the thermal capacitance. The one-dimensional model does not take into account heat spreading and can therefore not be used in practical problems. This approach can serve, however, as a first order model yielding insight into the temperature behaviour of a power transistor. Assume heat injection in a rectangular area with dimensions \( (L_x \times L_y) \). Heat is assumed to spread out under an angle as shown in figure 4.6.

![Diagram](image)

**Figure 4.6:** Approximation of heat spreading by a pyramid. Heat is flowing from the top plane to the bottom plane and spreads out under an angle.

This situation is modelled by a non-uniform transmission line. Equations (4.15) and (4.16) indicate that the propagation constant \( \gamma \) only depends on material parameters but the impedance
$Z$ now is a function of the distance from the top plane. The impedance is proportional to the inverse of the area \((L_x + 2z\tan(\alpha)) \times (L_y + 2z\tan(\alpha))\). If the thermal conductivity, the material density, the specific heat and the thickness of the layer \(H\) are known, this model has three unknown parameters: the spreading angle \(\alpha\) and the lengths \(L_x\) and \(L_y\). It is important to note that it is not possible to use the physical dimensions of an active area for the lengths \(L_x\) and \(L_y\) as is shown in the following.

Consider uniform heat injection in a rectangular heat area \((L \times L)\) at the top surface of a substrate. Zero heat flux is assumed at this plane (except for the active area) and a constant temperature is assumed at the bottom plane. A cross sectional view is shown in figure 4.7.

![Figure 4.7: Modelling of heat spreading shown in figure a. By adjusting the spreading angle (figure b) in the pyramid model, the steady state thermal resistance is modelled correctly. The short time transient behaviour can only be modelled correctly by increasing the spreading angle further (figure c). To model both the steady state thermal resistance and the short time transient behaviour, a spreading angle and an effective area must be used (figure d).](image)

As a first order model this situation is approximated by the heat spreading model discussed previously with a rectangular area \((L \times L)\) with a heat spreading angle \(\alpha_1\). This angle is chosen such that the total thermal resistance of the model is equal to the actual thermal resistance. Although this models thermal resistance correctly, the short-term thermal transient behaviour due to a heat pulse is not modelled correctly. This error is due to the incorrect modelling of the relatively large heat spreading close to the heat area resulting in a lower resistance and a higher capacitance. To lower the error the heat spreading angle could be increased to match the short-term behaviour. The model now predicts this behaviour correctly but does not predict the thermal behaviour after the pulse has been applied and certainly does not give the correct steady state thermal resistance. To solve these problems the dimensions of the active area are increased to \((L + \Delta L) \times (L + \Delta L)\) and the spreading angle is adjusted until both the short-term behaviour and the steady state thermal resistance are modelled correctly.

It is convenient to replace the non-uniform transmission line by a lumped circuit representation as shown in figure 4.8.

If an equidistant representation with \(N\) resistors and capacitors is used the element values are given by:

\[
R_{LE}(i) = \frac{L_z}{N} \frac{1}{kA(z(i))} \quad C_{LE}(i) = \frac{L_z}{N} \rho c A(z(i))
\]

(4.21)
Figure 4.8: Lumped element modelling of the heat spreading by a serie of cascaded resistor/capacitor sections. The assumed heat flow is from left to right, with the values of the lumped elements given by equation (4.21).

In these equations \( A(z(i)) \) represents the area at the position \( z(i) \) modelled by the \( i \)-th resistor/capacitor section:

\[
A(z) = (Lx + 2z\tan(\alpha))(Ly + 2z\tan(\alpha)) \quad z(i) = \frac{Lz}{N}(i - \frac{1}{2}) \quad (4.22)
\]

The lengths \( Lx \) and \( Ly \) represent the increased dimensions, and not the actual dimensions. The above equations are used directly in the design page in MDS to build a model for heat spreading. It is found that in practice 5-10 resistor/capacitor sections are needed to represent the thermal impedance of a power transistor.

**Modelling of thermal transient of the BLV 910**

The non-uniform transmission line model is used in the modelling of the BLV power transistor using the lumped element representation of figure 4.8 for each line. Three of these models are connected in series as shown in figure 4.9.

![Diagram](image)

Figure 4.9: One-dimensional thermal model of the BLV 910 power transistor. The model consists of a series connection of a model for the silicon die, the BeO package substrate and the mounting base respectively.

The models for the silicon die, the BeO and the mounting base are indicated by \( T_{LSi}, TL_{BeO} \) and \( TL_{mb} \) respectively. Each non-uniform transmission line is represented by twenty lumped resistors and capacitors. This number is enough to represent accurately the behaviour of the non-uniform transmission line. To model the non-linearity in the thermal conductivity six additional Kirchhoff transformations are placed in the circuit as shown in the same figure. Note that the non-linearity of the thermal capacitance is not accounted for in this set-up. The model is compared to thermal transient measurements as discussed in section 4.5. The principle of these measurements is basically that a power pulse is applied to the transistor and at the end of the pulse the base emitter voltage is measured. Using the relation between the
base-emitter voltage and temperature, the temperature at the end of the pulse is determined. The thermal impedance $Z_{th}$ is introduced as the ratio between the junction temperature and the power dissipation.

In modelling the BLV 910 transistor the parameters of table 4.1 are used.

<table>
<thead>
<tr>
<th>Layer</th>
<th>$L_x$ (m)</th>
<th>$\kappa$ (W/m-K)</th>
<th>$c$ (J/kg-K)</th>
<th>$\rho$ (kg/m$^3$)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Si</td>
<td>$120 \times 10^{-6}$</td>
<td>$8 \times 156$</td>
<td>650</td>
<td>$8 \times 2330$</td>
</tr>
<tr>
<td>BeO</td>
<td>$940 \times 10^{-6}$</td>
<td>270</td>
<td>1300</td>
<td>3000</td>
</tr>
<tr>
<td>Mb (Cu)</td>
<td>$5 \times 10^{-3}$</td>
<td>400</td>
<td>400</td>
<td>8800</td>
</tr>
</tbody>
</table>

Table 4.1: Parameters used in the modelling of the BLV 910 transistor.

Please note that to account for the 8 active areas the values of $\kappa$ and $\rho$ for the Si are multiplied by 8. To fit the measured thermal impedance, first the effective area and the heat spreading angle are adjusted until the first part of the thermal transient is matched. Next, the second part of the thermal transient is fitted by adjusting the parameters of the BeO layer and finally the parameters of the mounting base are adjusted to fit the measured thermal transient. In figure 4.10 a comparison is made between the model and the measurements.

![Graphs showing thermal impedance vs pulse width for Si, BeO, and Mb layers.](image)

Figure 4.10: Modelling the heating up curve of the BLV 910. Shown on the left the measured (solid line) and the simulated (dashed line) heating up curve of the BLV 910 as function of the pulse width. On the right the calculated thermal impedance of the silicon die, the BeO package and the mounting base versus time.

Note the small differences between the model and the measurements. The fitted parameters $L_x$, $L_y$ and $\alpha$ are shown in table 4.2.

An interesting point is the fitted size of an active area $L_x \times L_y = 0.15 \times 0.35$ mm$^2$. The actual size of an active area is $0.05 \times 0.3$ mm$^2$. This indicates a large spreading close to the active areas. Although this model is conceptually simple it is useful in investigating the thermal behaviour in the transistor. Thermal impedances are defined for the Si block, the BeO substrate and the mounting base as the ratio between the temperature drop over each layer and
<table>
<thead>
<tr>
<th></th>
<th>$L_x$ (mm)</th>
<th>$L_y$ (mm)</th>
<th>$\alpha$ ($^o$)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Si</td>
<td>0.15</td>
<td>0.35</td>
<td>10</td>
</tr>
<tr>
<td>BeO</td>
<td>0.7</td>
<td>0.7</td>
<td>45</td>
</tr>
<tr>
<td>Mb</td>
<td>2.5</td>
<td>2.5</td>
<td>45</td>
</tr>
</tbody>
</table>

Table 4.2: Parameters found for $L_x$, $L_y$ and $\alpha$ after fitting the modelled thermal transient to the measured thermal transient.

the dissipated power. Each thermal impedance is plotted as function of time after a power pulse is applied to the power transistor in figure 4.10 on the right. Although all three layers increase immediately in temperature as dissipation starts, a clear distinction is visible between the three layers. From the figure it is observed that the silicon is heated up until approximately 200 $\mu$s. After 200 $\mu$s the temperature drop across the silicon is almost constant and the BeO substrate is heated up until 2 ms. After 2 ms the temperature drop across the BeO is constant and the mounting base is heated up. Note that heating up the mounting base takes considerably longer due to the large metal volume. This time scheme is also used in fitting the parameters. Initially the transmission lines for the BeO and the Mb are removed from the model. The effective area and the spreading angle of the silicon are fitted for the first point at $10^{-5}$ s. and the corresponding slope. The model for the BeO is added next and once again the point at 200 $\mu$s and the slope are fitted. Finally the model for the Mb is added and the last part of the trace is fitted.

A major drawback is that the accuracy of the method depends heavily on the measurement accuracy of the first part of the heating up curve. In practice there is significant uncertainty as to the accuracy of the measured data for this part of the trace. Steady state resistances of 2.0 K/W, 2.2 K/W and 0.4 K/W for the Si, BeO and mounting base respectively have been found.

Using a rather simple model and only fit parameters (effective area and spreading angle) a reasonable fit between model and the measured heating up curve is obtained.

### 4.5 Thermal impedance measurements

Several methods exist to characterise the thermal behaviour of transistors by experiment. Some of these methods are:

- **Infrared measurements.** At the surface of the transistor heat is radiated into the surroundings. The wavelength of the radiation is related to the temperature of the surface and is detectable with infra-red cameras.
- **Probing methods.** When two metals are joined together a temperature related voltage drop exist across these metals. Using a probe, made of two dissimilar metals with different work functions. placed on the surface of the die, the voltage drop over the metals is a measure for the temperature.
- **Liquid Crystal methods.** A thin layer of liquid crystals is deposited on the top surface of the power transistor. These crystals change polarisation at a certain critical temperature. This change is observed by viewing the reflection of incoming light. By varying
the dissipation temperature contours are easily established.

- Electro-thermal characterisation. A transistor parameter with a measurable temperature relation is measured at different dissipation levels and at different reference temperatures. The junction temperature is deduced from the measurements.

The first three methods are discussed in brief in the following. The thermal characterisation of power transistors is normally carried out using electro-thermal measurements and this method is discussed in more detail.

**Infrared measurements**

In this method the energy radiated by the surface of the heated material is measured. This radiated power is related to the surface temperature $T_s$ (K), the surrounding temperature $T_{sur}$ (K) and the emissivity of the surface $\varepsilon$:

$$P_{rad} = \varepsilon\sigma A(T_s^4 - T_{sur}^4)$$  \hspace{1cm} (4.23)

The emissivity ($0 \leq \varepsilon \leq 1$) is and indicator of how efficiently the surface radiates heat when compared to an ideal radiator. The constant $\sigma$ is the Stefan-Boltzmann constant ($\sigma = 5.67 \times 10^{-8}$ W/m² K⁴). In the case of a power transistor the spectrum of the radiated energy is predominantly in the infrared region. The radiation is detectable with an infrared detector, which is used to scan and record the surface temperature. In the case of power transistors the ceramic cap is removed from the sample before it is placed under the scanner. Under DC or RF conditions power is dissipated in the junctions and the temperature at the surface of the die is scanned. In figure 4.11 typical DC results for a BLV 910 sample are shown. In this particular case the collector emitter voltage is set to 30 V and the base emitter voltage is adjusted to provide a collector current of 0.8 A. The corresponding dissipation is around 24 Watts.

In the top half of the figure the results of the infrared scan are shown. Light areas represent high temperatures and dark areas represent low temperatures. In this picture eight different areas with a high temperature are found, representing the eight active areas of the power transistor. The effect of the bondwires is also visible although these bondwires are bent slightly to the sides to allow a clear view of the surface where the active areas are located. Please note that this has no effect on the behaviour of the transistor under DC conditions. It does however have an effect under RF conditions. In the top figure a horizontal line (LI01) and a vertical line (LI02) are defined and the measured temperature along these lines is plotted in the bottom two figures. In the left figure the temperature along the line crossing four active areas is shown. The curve starts on the left close to a temperature of 27 degrees C. This temperature is not the mounting base temperature since the the base is watercooled down to 19 degrees Celsius. It is the temperature of the die at the outer edges. The temperature increases to around 120° C, representing the temperature of the first outer active area. Temperature drops to 110° C in between the two active areas and increases to 135° C maximum in the second active area. In between the two center areas the scanned temperature drops to around 70° C. Note, however, that this is not directly the surface temperature as two bondwires are located at this position. Temperature then shows a maximum of 135° C for the third active area and a maximum of 120° C for the fourth active area.

In the second picture the temperature along the vertical line (LI02) crossing two active areas is shown. It starts at 38° C and increases to 135° C representing the maximum temperature in
Figure 4.11: Results of an infrared measurement of a BLV 910 sample \( V_{ce} = 30 \text{ V}, I_c = 0.8 \text{ A}, P_{diss} = 24 \text{ W} \). In the top half the infrared image is shown with light areas representing high temperatures and dark areas representing low temperatures. In this image a horizontal line and a vertical line are drawn. The temperature profile along these lines are plotted in the bottom two figures. On the right a column is shown with absolute temperature values.

the active area. This maximum temperature (the "hot spot") is found at the intersection of the horizontal line and the vertical line. Temperature drops to 80° C and increases again to 115° C. To estimate the thermal resistance the temperature difference is divided by the dissipated power. In the particular case of the sample shown in figure 4.11 the thermal resistance is \( R_{th}(peak) = (135 - 19) / 24 = 4.8 \text{ K/W} \).

Advantages
There are a few major advantages of infrared scanning. The temperature of the surface is rather easily obtained. Also the temperature distribution of a large area is obtained in one scan within a relatively short time without moving the sample. Additionally, there is no need for direct contact with the sample as opposed to probing methods.

Disadvantages
There are also some drawbacks related to the infrared measurements. The surface temperature is measured and based on the fact that the junction is located close to the surface, the assumption is made that the junction temperature is close to the surface temperature. In RF power transistors, however, a portion of the power is dissipated in the epitaxial layer. This
layer extends a few microns into the die and the assumption of temperature equality of the surface and junction becomes questionable. Additionally, a relationship must be established between the surface temperature and the radiated energy. In practical cases this means that the emissivity of the surface (\( \varepsilon \) in equation (4.23)) must be found. Any error in determining this factor leads to an error in the temperature measurement. Calibration procedures reduce these errors. Another problem is the rather low spatial resolution of the measurements. The resolution of commercially available equipment is in the order of 5-10 microns.

**Probing measurements**

In direct contact methods two differing metals are joined together to form a probe (see figure 4.12). Heating up the metals introduces a voltage drop across the junction due to the differing workfunctions. By moving the probe over the surface of the heated material a temperature scan is made.

![Figure 4.12: Principle of the probing method. Two metals are joined together and placed on a heated surface. The temperature induces a voltage drop across the two metals.](image)

This type of equipment can be very powerful in combination with Scanning Tunneling Microscope (STM) equipment. By replacing the STM tip by a thermal probe it should be possible in principle to make high resolution temperature scans. First tests with such equipment performed on the BLV 910 have shown some significant drawbacks of this method. The STM equipment in the tests has a set of high resolution motors to position the probe with a high precision in a small area and a set of motors to move the probe over larger distances.

In high power transistors the probe must be manoeuvred in between the bondwires. In practice this limits the use of the scanner to areas completely free of bondwires. Additionally, STM equipment normally scans rather small areas (10 \( \mu \text{m} \times 10 \mu \text{m} \)) and moving the probe over such an area takes considerable time. The active area of the high power transistors under consideration is 50 \( \mu \text{m} \times 300 \mu \text{m} \). Consequently, several scans have to be made before the profile of one active area is obtained. Or the positioning system must be modified to cover a large area.

Nevertheless, this method may be very useful in thermal imaging of integrated circuits where bondwires are only located at the edge of the die. Further investigations should be made in this field.
Liquid crystal methods

Liquid crystal methods work differently from other methods in that a very thin artificial layer of liquid crystal material is deposited on the surface to be scanned. Below a certain temperature, which is determined by the specific liquid crystal material used, the crystals are polarised and incoming light is reflected back as in a normal mirror. The reflected light is observed by a standard camera. Above the specific temperature the crystals become unpolarised and light is absorbed by the liquid crystal material. The principle is illustrated in figure 4.13.

- Area above critical temperature
- Area below critical temperature

Figure 4.13: Principle of the liquid crystal method. At low dissipation levels there is no change of the liquid crystals. At higher dissipations the temperature in certain areas is higher than the critical temperature of the liquid crystal material. In these areas the reflection of light changes. As dissipation increases these areas become larger.

At low dissipation levels the temperature of the entire active area is below the critical temperature of the liquid crystal material. When the dissipation in the transistor increases the temperature in certain areas rises above the critical temperature so that the reflection of light by the liquid crystals changes. As dissipation increases further this area grows larger and larger. An advantage of this method is that it is possible to determine temperature contours for differing dissipation values rather easily. Each contour then encloses the area where the temperature is higher than the critical temperature of the liquid crystal. Appropriate software can facilitate the determination of these contours automatically. The peak thermal resistance at a single dissipation level is determined by increasing the dissipation until at a point the liquid crystals change states. The peak thermal resistance then is the ratio between the temperature increase and the dissipated power.

It is not possible, however, to draw a correct set of temperature contours at a single dissipation level unless the temperature increase is a linear function of dissipated power. In case the temperature increase is a known nonlinear function of dissipation, it is possible to determine temperature contours at a given dissipation level using Kirchhoff’s transformation.

Initial tests, performed with the help of Philips Research Laboratories, in determining temperature contours on the die of the BLV 910 were hindered by some practical problems. The liquid crystal material must be deposited in liquid form on the surface of the die. It was found that a great deal of the liquid crystal material pulled together just below the bondwires mounted on the die. This left the active areas without any liquid crystal material. Trying to spin more material onto the die resulted in an excessively thick layer of the material. Proper software to determine the temperature contours was not yet available making the determination of these contours cumbersome if not impossible. This method may be used however with
success in the thermal characterisation of flat surfaces, such as complete integrated circuits, without any bondwires mounted to central positions.
Hot spots are easily found by increasing dissipation until the state of the liquid crystal material changes. This method is very inexpensive as only a liquid crystal material and a normal camera are needed. In addition the resolution of this method is in principle higher than other methods.

**Electro-thermal measurements**

The previous three methods probe the temperature directly at the top surface. In the fourth method the junction temperature is probed using the (measured) relation between the base-emitter voltage and temperature at low current relation.

The circuit for measuring the thermal impedance is shown in figure 4.14.

![Circuit Diagram](image)

**Figure 4.14: Basic circuit for measuring the thermal resistance of bipolar transistors (the DUT is the device under test).**

A constant voltage is connected between the collector and base. At the emitter two current sources are placed: a constant current source $I_m$ and a pulsed high current source $I_p$. A volt meter measures the base-emitter voltage. This method is often referred to as the $V_{EBC}$ method. The method uses the relation between the base-emitter voltage and temperature for a given current level $I_m$. The current level is usually in the order of a few mA. To calibrate the thermal resistance measurements, the relation between $V_{be}$ versus temperature is measured at a low current level. This linear relationship has a slope of approximately -2 mV per Kelvin. Extrapolating to 0 K gives a value of approximately 1267 mV.

A typical plot of the emitter current versus time is plotted in figure 4.15 on the left. The plot of the base-emitter voltage is shown on the right.

At the start the emitter current is held at the low level of a few mA. At time $t_1$ the pulsed high current source is switched on and the emitter current is $I_m + I_p$. Because the collector-base voltage is set to a relatively high value, the power dissipation starts at $t_1$ and the device starts heating up. Between times $t_1$ and $t_2$ the device heats up. This is also found in the decrease of $V_{be}$ between $t_1$ and $t_2$. At $t_3$ the pulsed current is switched off and the emitter current is again equal to $I_m$. At this point the previously measured relationship between temperature and $V_{be}$ is applicable. By measuring $V_{be}$ directly after $t_2$ the temperature can in principle be found directly. In practice, however, it is difficult to measure $V_{be}$ at $t_2$. More practical is to measure the voltage at $t_3$ and $t_4$, the voltage at $t_2$ is found by extrapolation assuming a parabolic curve.
The dissipated power is equal to:

$$P_{\text{diss}} = V_c I_c + V_{be}(I_m + I_p - I_e)$$

(4.24)

By increasing the pulse width $t_2 - t_1$ and measuring the temperature for each pulse width the heating up curve is found. In figure 4.16 the temperature divided by the dissipated power is plotted versus the pulse width.

This figure shows the same as the measured results as in figure 4.10. For a pulse width of 10 $\mu$s the thermal impedance is 0.6 K/W increases to around 4.5 K/W for a pulse width of 10 ms. The thermal impedance does not increase much more for longer pulse widths.

**Relation between temperature and base-emitter voltage**

The $V_{EBC}$-method is used to measure the thermal resistance based on the electro-thermal relationship between base-emitter voltage and temperature. For small transistors the measured $V_{be}$ is related to the junction temperature. In large power transistors a temperature profile is present within an active area and consequently the measured $V_{be}$ is not related to the junction temperature. The main question then is which temperature is measured: the maximum temperature, the average temperature or something different. To start investigating this point two compact models are placed in parallel as shown in 4.17 on the left. The Mextram parameters for each compact model represent one active area of the BLV 910.

The idea is to keep one transistor at a fixed temperature $T_1$ and to vary the temperature $T_2$ of the second transistor. The resultant base-emitter voltage is compared with the base-emitter voltage of a transistor at an equivalent temperature $T_{eq}$. The equivalent temperature is
Figure 4.16: Heating-up curve of the BLV 910: Measured temperature divided by the dissipated power versus pulse width. Dissipation starts at time \( t_1 \) and stops at \( t_2 \) in figure 4.15.

Figure 4.17: Circuits for estimating the equivalent temperature. On the left two transistors in parallel having temperatures \( T_1 \) and \( T_2 \) respectively. Area factor is 1 for both transistors (A=1). On the right a single transistor having temperature \( T_{eq} \) and area factor 2 (A=2).

changed until the \( V_{be} \) of both situations is the same. In other words, the two transistors in parallel represent a transistor with a temperature gradient and the equivalent transistor gives the equivalent temperature of this transistor.

The temperature \( T_1 \) is held at 273 K and \( T_2 \) is swept from 273 K to 473 K. For each point the equivalent temperature is found by changing this temperature until the \( V_{be} \) is the same for both situations. The equivalent temperature is plotted versus the temperature difference \( T_2 - T_1 \) in figure 4.18 on the left.
The black dotted line represents the case where the equivalent temperature equals the max-
Figure 4.18: Left: Equivalent temperature of two transistors in parallel at differing temperatures (solid line). Two other cases are also indicated: equivalent temperature equal to the average ($T_{eq} = (T_1 + T_2)/2$) or equal to the maximum ($T_{eq} = T_2$). Shown on the right the current through the two transistors as function of the temperature difference with the total current being constant.

The equivalent temperature $T_{eq} = T_2$. The line with the open squares shows the situation where the equivalent temperature equals the average temperature: $T_{eq} = (T_1 + T_2)/2$. The solid line itself is the equivalent temperature versus the temperature difference.

Based on the figure two observations are made: for low temperature differences the equivalent temperature equals the average temperature and for larger differences the equivalent temperature is closer to the maximum temperature.

Next the currents of the two separate transistors are plotted versus the temperature difference in figure 4.18 on the right. At zero temperature difference the two currents are equal. Increasing the temperature difference decreases the current through the transistor at the reference temperature and increases the current through the other transistor. This is in agreement with the conclusions in [57]. The explanation for this phenomenon is the fact that the increasing temperature decreases the base emitter voltage of the transistor with temperature $T_2$ with around 2 mV/K. The first transistor is held at constant temperature and the base-emitter voltage drops. Consequently, the current through that transistor decreases rapidly with increasing temperature. For high temperature differences the current through the first transistor is negligible and all current flows through the second transistor having area equal to one (A=1). This situation is represented by the equivalent transistor having an area factor equal to two (A=2). Although not performed in this work, it is strongly recommended to verify the above results by experiment.

**Electro-thermal determination of the thermal resistance of an active area of the BLV 910**

The observation that the equivalent temperature equals the average temperature at low temperature differences and tends more towards the maximum temperature at higher differences
is tested for one active area of the BLV 910. Once again simulation tools are used to investigate this point. The circuit setup is similar to that in figure 4.17. An active area is no longer represented by a single compact model, but by a set of compact models. In figure 4.19 on the left a sketch of an active area between a base and an emitter line is shown (cf. the bottom right SEM photo of figure 2.2).

Figure 4.19: Left: Subdivision of an active area of the BLV 910 into $3 \times 18$ subareas. Each subarea is modelled by a compact transistor model having its own temperature node. All 54 compact models are placed in parallel as shown in the middle for 3 models representing a column of 3 subareas. In the BLV 910 in such a column the emitter resistors are mainly lumped however (cf. the ballasting resistors at the bottom right SEM photo of figure 2.2). To mimic this situation the emitter resistor is set to zero in the compact model and one "lumped" emitter resistor is added per 3 models as shown on the right. Eighteen of these models are then placed in parallel to model an active area.

The active area itself is subdivided into $3 \times 18$ rectangular subareas. Each subarea is represented by a Mextram model with the Mextram parameters given in appendix B and the area factor of each model set to $1/(3 \times 18)$. In total 54 Mextram models are placed in parallel each having it's own temperature node. Each temperature node is connected to a multiport thermal model. The full thermal model includes all thermal couplings and is further discussed in section 4.6. the non-linear behaviour of the thermal conductivities involved is included in the model.

In the simulator the transistor is heated up with a fixed collector-base voltage of 26 V and a variable emitter current. Two results are calculated:

- The maximum temperature $T_{\text{max}}$ in the center of the active area versus the dissipated power.
- The average temperature $T_{\text{ave}}$ of the 54 subarea temperatures versus the dissipated power.

For each point the temperature profile is then fixed and the emitter current is switched back to a value of $I_m = 1$ mA (cf. figure 4.15). From the base-emitter voltage the equivalent temperature $T_{\text{eqv}}$ is found by comparing the voltage with an equivalent transistor. The three temperatures ($T_{\text{max}}$, $T_{\text{ave}}$ and $T_{\text{eqv}}$) are divided by the dissipated power and plotted against the dissipated power. Initial results are shown in figure 4.20 on the left.

It is observed that the thermal resistance increases substantially with dissipated power due to the decreasing thermal conductivities. Additionally, it is also observed that the equivalent thermal resistance $T_{\text{eqv}}/P_{\text{diss}}$ is almost equal to the average thermal resistance at low dissipations and starts to deviate at dissipation levels of a few Watts. In fact these results are similar to the first part of the plot shown in figure 4.18. Temperature differences are, however, too small to lead to large differences of the equivalent temperature from the average temperature.

Please note that under normal operation the power dissipation in the BLV 910 is on the order
Figure 4.20: On the left the average, maximum and equivalent thermal resistance versus dissipated power for the case with $3 \times 18$ compact models in parallel. On the right the same resistances with a better approximation for the emitter ballasting resistors in the BLV 910.

of 1 Watt per active area.

An important point is not considered in the analysis: the effect of the lumped emitter ballasting resistor. As shown in the bottom right SEM photo of figure 2.2 a ”lumped” ballasting resistor is placed at the end of each two emitter fingers. The extracted emitter resistance for one active area is 4.42 $\Omega$. In the model with $3 \times 18$ compact models the value of the emitter resistor of each compact model is simply a scaled value of $3 \times 18 \times 4.42 \Omega$. This situation is shown in the center of figure 4.19 where each model has its own emitter resistor. A more realistic approach is to set the emitter resistance of the the compact mode itself to zero and connect the emitters of a column of transistors together. From there a single emitter resistor ($18 \times 4.42 \Omega$) is connected to the external emitter as shown on the right of figure 4.19. Eighteen of these models are connected together to represent the active area. The procedure of finding the three temperatures $T_{\text{max}}$, $T_{\text{ave}}$ and $T_{\text{eqv}}$ is repeated and the thermal resistances are plotted against the dissipated power in figure 4.20 on the right. For dissipations up to 2 Watts the results are similar to the previous results shown in the same figure on the left. For higher dissipations the maximum temperature increases rapidly. The average temperature doesn’t show this sharp increase however. These results therefore indicate a serious hot spot at high dissipation levels. The equivalent temperature also increases at the levels of 2.5 Watts or more.

Two important conclusions may be drawn from these calculations:

- For low dissipation levels the equivalent temperature follows the average temperature i.e. when measuring the thermal impedance at low dissipations using the electro-thermal method the measured impedance represents the average impedance.
- At higher dissipations (above 2 Watts) the equivalent temperature deviated substantially from the average temperature. Additionally, the maximum temperature increases rapidly indicating a hot spot.
Extrapolating these conclusions to the complete BLV 910 transistor it is concluded that up to dissipation levels of around 16 Watts the measured thermal impedance represents the average temperature. For higher dissipation levels the thermal impedance tends to the maximum impedance.

From figure 4.20 it is observed that the effect of the emitter ballasting resistance on the maximum temperature is rather large. Consequently, it is important to study the effect of the value of this resistance on the maximum temperature. In the simulator the maximum temperature is calculated as function of the dissipated power for various emitter resistance values. The results are plotted in figure 4.21.

![Graph showing thermal resistance vs. dissipated power for different emitter resistances](image)

**Figure 4.21:** Maximum thermal resistance ($T_{\text{max}}/P_{\text{diss}}$) as function of the dissipated power for various active area emitter resistances. The extracted value for the BLV 910 is $R_e = 4.42 \, \Omega$.

From this figure it is observed that the active area is capable of handling powers up till 3 or 4 Watts for emitter resistance values of 5 $\Omega$. If this resistance is decreased the power handling capability degrades rapidly to around 2.4 W for $R_e = 1 \, \Omega$ and 1 Watt for $R_e = 0 \, \Omega$. Please note that the extracted thermal resistance of the active area is 4.4 $\Omega$.

### 4.6 Three-dimensional thermal modelling

In this section the three-dimensional thermal modelling of power transistors is considered. In figure 4.22 a typical problem encountered in the thermal analysis of RF power transistors is shown.

A silicon die with 4 active areas is located on top of a beryllium oxide block. The active areas are located below the top surface of the silicon block. Heat is generated in these active areas and conducted to the Si-BeO interface. The BeO block is mounted on the mounting base, a block of metal. The heights of the Si, BeO and mounting base are in the order of 100 $\mu$m, 1 mm and 3 mm respectively. In practice a thin gold layer with a thickness of a few microns is
Figure 4.22: Typical problem encountered in the thermal analysis of power transistors: a silicon die with 4 heat generating volumes, placed on top of a BeO block and a mounting base. Heat is conducted from the active areas through the silicon and the BeO to the mounting base.

located between the Si die and the BeO substrate. The effect of this layer on the total thermal resistance is normally negligible. There are a few other points which are more difficult to investigate. The first point is the effect of voids created during the mounting of the die on a thin gold layer on top of the beryllium oxide. These voids increase the thermal resistance. The second point concerns the diffusion of gold into the silicon. This diffused gold lowers the local thermal conductivity and increases the thermal resistance.

The main interest in thermal modelling is the relation between the heat generated in the heat volumes and the temperature in the heat volumes. As an example, suppose each heat volume represents one active area and each active area is represented by one compact transistor model. In each active area power is dissipated and heat is generated. Electrically this is represented by a current, equal to the dissipated power, flowing out of the temperature node of the compact transistor model. This current is injected in the corresponding heat volume of the thermal model and the simulator needs to solve for the corresponding temperature in the active area. This temperature is then used to update the temperature dependent electrical parameters of the compact transistor model. The thermal model must, therefore, relate the dissipated powers in the active areas and the temperature in the active area:

$$\mathbf{T} = \mathbf{R}_{TH} \mathbf{P}_{diss}$$  \hspace{1cm} (4.25)

where $\mathbf{P}_{diss}$ is a vector of dissipated powers, $\mathbf{T}$ is a vector of temperatures and $\mathbf{R}_{TH}$ is the thermal matrix relating $\mathbf{P}_{diss}$ and $\mathbf{T}$.

$$R_{TH,ij} = \frac{T_i}{P_{diss,j}} \hspace{1cm} P_{diss,k} = 0, k = 1 \ldots N, k \neq j$$  \hspace{1cm} (4.26)

The main issue in this section is finding a computationally fast and accurate method for determining the coefficients of the matrix $\mathbf{R}_{TH}$.

### 4.6.1 Problem reduction

From figure 4.22 it is observed that a rectangular block of uniform heat conduction with brick shaped heat generation volumes may serve as an elementary building block for the thermal model of RF power transistors. One such block is shown in figure 4.23 on the left. To enforce
continuity conditions at the interface between Si and BeO and the interface between the BeO and the mounting base it is convenient to introduce heat panels. These panels are heat generation volumes with zero thickness placed at the interface. An example of such a block with heat panels is shown in figure 4.23 on the right.

Figure 4.23: Shown on the left four brick shaped heat injection volumed in a block of conducting material. Each heat injection volume can represent an active area or a part of an active area. By setting the thickness of the volumes to zero, heat injection panels result. These heat panels can also be used at the bottom plane to enforce boundary conditions as shown on the right.

In the case of the thermal model for the BLV 910 three elementary blocks are needed. One block for the silicon die, one for the beryllium oxide and finally one block for the mounting base.
For each block it is assumed that heat is generated or absorbed uniformly in the heat generating volumes or the panels and a node is defined in the center of each volume or panel. Additionally, at all six boundary planes zero heat flow is assumed. Heat only enters or leaves the block of material through the heat volumes or the panels. A thermal resistance matrix is generated for each block and the blocks are then connected together in MDS.

Interface conditions
At the interfaces, continuity of the normal component of the heat flux and equality of the temperature must be enforced. At interfaces where these conditions must be met, a grid of heat panels is defined. Under the aforementioned conditions it can be shown that the flux entering/leaving the block through a panel is the normal component of the flux. The grids at two different blocks are connected together to enforce the flux continuity in an area and the temperature equality at the points of the nodes. In other words, heat leaving one block through a panel enters the second block through the connected panel. An example of this approach is shown in figure 4.24.

Figure 4.24: Shown on the left the silicon die on top of the BeO block. To enforce heat flux continuity and temperature equality at the Si-BeO interface, heat panels are defined at the bottom of the Si substrate and at the top of the BeO substrate. The panels are connected properly in the simulator.
For each block a $N$-port model must be generated where $N$ equals the number of heat volumes used to represent the active areas plus the number of heat panels used to enforce the boundary conditions. Suppose for example that a thermal model for a transistor with one active area is required. This active area is modelled with say 25 heat volumes and the interface conditions are enforced with 49 heat panels. The number of ports in the model then must be 74. In this $N$-port model a full matrix is required. In the example a $74 \times 74$ thermal matrix, with 5476 elements must be computed.

### 4.6.2 Solution methods

Two approaches are compared:

- Modelling using equivalent RC networks. In this approach the heat conduction differential equation is discretised in an electrical simulator using resistors and capacitors. The resistors model heat conduction and the capacitors model heat storage. The resulting electrical network is simulated and the calculated voltage and current are interpreted as temperature and heat flux respectively. It is shown that this approach is time consuming if not impossible using the DC- or AC-simulator of MDS.

- Modelling using Green's functions. In this approach the heat conduction differential equation is replaced by an integral relation relating the volume distribution of dissipated power to the temperature. Analytical Green's functions are used to generate a thermal impedance matrix including thermal conduction and heat storage. In the particular case of heat transport in RF power transistors under CW conditions, only the heat conduction is of importance and consequently only the thermal resistance matrix is required. It is shown that this approach is feasible for the high power transistor under consideration.

Another approach, which is not pursued here, is to compute the thermal matrix with commercially available software packages and to import the output dataset into MDS. An advantage of this method is that a reliable thermal resistance matrix is computed and more complex geometries can be taken into account if desired. A major drawback of this method is for every geometry a new dataset must be generated. Furthermore, it is not possible to follow temperature and heat flux inside the geometry under dynamic conditions.

### Thermal RC networks

In the first approach a model is built by replacing the differential operators in the heat equation by their finite difference approximations. These equations are then represented in an electrical simulator by a three dimensional net of thermal resistances as shown in figure 4.25 on the left. In this figure the central node is interconnected to six surrounding nodes using resistances. The current flowing from one node to another node through the resistor models heat conduction.

If the thermal capacitance must be accounted for, a thermal capacitor is connected from every node to ground as depicted in figure 4.25 on the right. Heat conduction is modelled by the resistors and heat storage is modelled by the capacitors.

In this section the feasibility of this approach in MDS is studied based on three criteria:
Figure 4.25: Network representations of a finite difference approximation of the heat conduction equation around a point. Shown on the left is a circuit with only resistances and shown on the right a circuit with an added capacitor to model heat storage.

1. Feasibility of defining the circuit in MDS. Schematics are entered into MDS using two-dimensional drawings. The representation of a three-dimensional network introduces practical problems.

2. Solution time for the network. Once the solver starts solving for node voltages the solve time is an important factor.

3. RAM memory usage. Not only solve time but also the required computer memory is important.

Defining thermal RC networks in MDS

First of all it is noted that defining the three-dimensional RC network in the schematic bench of MDS is already a difficult task. The main problem being the connection of the elements in the third dimension. To avoid this problem wire labels, representing nodes, can be used in MDS to connect elements together without the necessity for wires. A major drawback is that the voltage of the wire label (the node) is saved in the dataset, making the dataset unnecessarily large.

A different approach has been chosen. A small external computer programme generates a netlist, representing the thermal network. This netlist is then directly fed to the simulator solver. After the simulation has completed the solution, the solve time and the memory usage are found in the output files of MDS.

Solution time and memory usage

Networks of $n \times n \times n$ resistors in the $x$, $y$ and $z$-direction respectively are considered. The number $n$ is varied from 1 to 20 and consequently the number of nodes is varied from 8 to 9261 nodes. Two types of networks are generated. The first type only has resistances and the second type has additional capacitors from each node to ground. In these networks the elements are assumed linear i.e. non-linear effects are not included in this analysis.

Two different network solvers of MDS have been used to solve the networks. The first solver is the DC-solver. This engine solves non-linear networks at DC iteratively, and is normally used to solve for DC operating conditions of circuits. The second solver is the AC-solver, which solves linear network equations in the frequency domain. This solver is normally used
to compute the small signal AC behaviour of circuits. Consequently, the simulation time and the memory usage of three simulations are available:

1. The DC-solution of the resistors network
2. The AC-solution of the resistor network
3. The AC-solution of the resistor/capacitor network

The solve time and the memory usage are the numbers reported in the output logfile of MDS. The results of the simulations are shown in figure 4.26.

![Graph showing solve time and memory usage](image)

Figure 4.26: Simulation time in seconds (shown on the left) and memory usage in Mb (shown on the right). In both figures the normalised number of nodes in the circuit \(((n+1)/21)^3\) is shown on the horizontal axis.

The following observations are made. First of all, the solution of the resistance network by the DC-solver takes more time than by the AC-solver. The network of \(21^3 = 9261\) nodes consumes 3500 seconds using the DC-solver and 2300 seconds using the linear AC-solver. This is mainly caused by the fact that the DC-solver solves iteratively for the node voltages where the AC-solver solves the linear problem directly. Note that the AC-solver was not able to complete the last circuit with capacitors and resistors.

The second observation is that both simulation time and memory usage are almost the same for the network with and without the capacitors. This is due to the fact that the solvers solve for the node voltages. Since the number of nodes is not increased, the solution time and memory usage are almost the same.

Thirdly it is noted that memory usage of all three methods is nearly the same and is moderate. The fourth and most important conclusion is that this simulation approach is impracticable for our type of problems, since both simulation times and memory usage become excessive for larger networks. It is anticipated that for our type of problems the number of nodes is much larger than 10,000 nodes. The method works quite well however for smaller problems.
Conclusions
Representing the thermal problem by a RC-network in MDS did not prove very successful mainly due to long simulation times. The method offers a number of advantages however. Non-linearities and inhomogeneities in the materials involved are easily accounted for. It is expected that further research into the implementation of this method in MDS can improve the results substantially. More specialised solvers should be used to solve the RC-type networks. One such a set of programmes, dedicated to the solution of Helmholtz’s equations, is FISHPACK available in the public domain [30].

Green’s function methods
An alternative approach to compute the thermal matrix is the use of Green’s functions. In section 2.10 Green’s functions are used to relate a volume distribution of current sources to the resultant potential distribution. Similarly it is possible to relate a volume distribution of heat generation to the resultant temperature using Green’s function. Consider the case of a brick shaped volume $V'$ where 1 Watt of heat is generated uniformly. Following a similar reasoning as in section 2.10 the temperature distribution follows as:

$$T(x,y,z) = \frac{1}{kV'} \int_{V'} G(x,y,z|x',y',z')dV'$$

(4.27)

where $G(x,y,z|x',y',z')$ is the Green’s function satisfying the appropriate boundary conditions. Two problems arise: finding the Green’s function and integrating this function. Once these two problems are solved it is easy to compute the thermal matrix elements.

Two methods have been investigated to obtain a suitable Green’s function for the rectangular block with on each face either a Dirichlet boundary condition or a Neumann boundary condition.

In the first method an eigenfunction expansion is constructed resulting in a a triple summation of sine terms and cosine terms (depending on the applied boundary conditions). The convolution integral (equation (4.27)) of the Green’s function and the rectangular heat volume is solved analytically. The resulting function, with a triple summation, is simplified to a double summation. Note that this function must be evaluated eight times, due to the triple integration. Highly optimized algorithms are then used, based on the recurrence relations for the sines and cosines, to compute the summations. Although the method works well, it is found that the number of terms in the summations can be high for reliable results, making calculation times relatively long. Although the algorithm was not improved any further, it should be noted that the calculation times can be reduced further if techniques based on Fast Fourier Transforms (FFT’s) are used.

The second method to compute the Green’s function is based on imaging technique ([51], [58]). In this case a Green’s function for a homogeneous medium without boundaries is used. To take into account the boundary conditions, the source is imaged in the boundaries and again a triple summation results. The convolution integral is solved analytically, but the triple summation remains. For practical cases however the number of terms in the summation is relatively low making this approach more suitable for implementation in CAD tools.
Advantages and disadvantages

An advantage of the method based on Green’s functions for the problem at hand is that the thermal resistance matrix is computed (nearly) exactly. Additionally, a direct relationship between the geometry and the thermal matrix in MDS is maintained. A disadvantage of this method is that only simple geometries are treated since derivation of the Green’s function is impracticable for more complex geometries without discretising the boundary.

Nevertheless, in the remainder of this work Green’s functions are used to build several thermal models into MDS.

4.7 Modelling of one active area

Before continuing with the thermal modelling of the BLV 910, the modelling of one heat generating volume is considered. The model uses Green’s function (equation (2.42)) in combination with imaging technique. The model was implemented in MDS by the author with the structure under consideration in figure 4.27.

Figure 4.27: Calculation setup of a brick shaped substrate with dimensions \((LSUB_x, LSUB_y, LSUB_z)\) and a brick shaped heat generating volume with dimensions \((LH_x, LH_y, LH_z)\). One the bottom plane temperature is assumed zero and on all other faces zero heat flux is assumed.

In this figure a brick shaped substrate is shown with dimensions \(LSUB_x \times LSUB_y \times LSUB_z\). On the bottom face of this substrate temperature is assumed zero and on all five other faces
zero heat flux is assumed. A heat generating volume with dimensions $LH_x \times LH_y \times LH_z$ is located in the substrate. The bottom of this volume is placed a distance $HH$ from the bottom plane. The spacing between the heat volume and the side walls is $S_x$ and $S_y$ in the x- and y-direction respectively.

There are two reasons to investigate this structure:

- In the modelling of the BLV 910 several simplifications are made. These simplifications are based on this section. The motivation for these simplifications is given later (cf. section 4.8).
- Parameters, such as the substrate height, vary in practice. The effect of this variation is studied in this section.

For the heat volume the dimensions of one active area of the BLV910 are chosen as a starting point, i.e. $LH_x = 50 \mu m$ and $LH_y = 300 \mu m$. The thickness of this volume is made negligibly small: $LH_z = 0$. Sidewall spacings $S_x$ and $S_y$ are both set to $0 \mu m$ initially. The substrate height is set to the height of the die: $L_{SUB_z} = 120 \mu m$ and the heat generating volume is placed on the top of the substrate: $HH = L_{SUB_z}$. The thermal conductivity of the substrate is set to 150 W/m-K. This situation represents the one dimensional case where heat spreading does not take place because the sidewall spacings $S_x$ and $S_y$ are 0. This allows the computation of the upper limit of the thermal resistance as $HH/(xLH_x LH_y) = 53.33 K/W$.

In the following the main focus is on the temperature in the center of the heat generating volume with the bottom plane at $T = 0$. Power dissipation is set to 1 Watt and the temperature in the center then represents the (maximum) thermal impedance.

Sidewall spacing

The effect of the sidewall spacing is investigated by changing the spacing between the edge of the heat area and the sidewall in the x-direction and y-direction respectively. First the spacing $S_x$ is varied between 0 and 100 $\mu m$. In the BLV 910 die this distance is slightly larger than 100 $\mu m$. The results of the computations are shown in figure 4.28 on the left.

At zero distance the computed thermal resistance equals the one-dimensional resistance of 53.33 K/W. Note that the one-dimensional case also serves as a test for the numerical software. As the spacing $S_x$ increases the thermal resistance decreases to 47 K/W, a relative effect of about 12 percent. From a practical point of view it is advisable to keep the sidewall more than 50-100 $\mu m$ away from the active area.

In the next computation the spacing $S_x$ is reset to zero and the spacing $S_y$ is swept from 0 to 200 $\mu m$. In the BLV 910 this spacing is a little above 200 $\mu m$ for the outer 4 active areas. For the inner four areas this spacing is larger. The results are shown in figure 4.28 on the right. With a spacing of 0 the thermal resistance equals the one-dimensional resistance. Increasing the spacing lowers the thermal resistance substantially to around 19 K/W at a spacing of 200 $\mu m$. Once again from a practical point of view the spacing should be in the order of 100-200 $\mu m$ to keep the thermal resistance low.

In the last computation the spacings $S_x$ and $S_y$ are set to 100 $\mu m$ and 200 $\mu m$ respectively. These are the values used in the BLV 910 die. The computed thermal resistance for this
Figure 4.28: Thermal resistance as function of the spacing between the heat area and the sidewall in the x-direction (shown on the left) and the y-direction (shown on the right) respectively.

case is 19.1 K/W. The thermal resistance with the sidewalls completely removed is 19.0 K/W Upon comparing these two values it is concluded that ignoring the effect of the sidewalls introduces an error of less than one percent. Consequently, and for reasons of simplicity, the sidewall effect is removed from the remaining computations of this section.

Substrate thickness

In practice the height of the substrate varies and consequently the thermal resistance changes. To investigate the effect of these variations, the substrate height is varied. With the results it is also possible to investigate how much the substrate thickness must be thinned down to reduce the thermal resistance substantially. results of the computations are shown in figure 4.29.

The computed thermal resistance as function of the substrate height (solid line) is shown on the left. The one-dimensional thermal resistance is also plotted (dashed line). On the right the first part is replotted. From these pictures it is concluded that for substrate heights up to $\approx 20 \mu m$ the thermal resistance follows the one-dimensional behaviour. For thicker substrates heat spreading comes into play. A typical variation of the substrate height is in the order of 10-20 $\mu m$ at a substrate height of 120 $\mu m$. At this height of 120 $\mu m$ the resistance is 19.0 K/W increasing to 19.7 K/W at 140 $\mu m$ and decreasing to 18 K/W at a height of 100 $\mu m$ representing a relative change of 6%.

Location of heat generation

In [47] the location and the volume where heat is injected in the thermal model is made dependent on the applied base collector voltage. This approach accounts for the dependency of the thickness of the collector-base depletion region, the region where the main portion of the heat is generated, on the applied voltage. Although this approach is not applied in this work,
for reasons to be discussed later (cf. section 4.10), it is useful to investigate the effect of the location of the heat generation on the total thermal resistance.

Two cases are considered. In the first case the thickness of the heat region is kept zero \((LH_z = 0)\) and the location is varied \((HH, \text{ cf. figure 4.27})\). In the second case the heat volume is extended to the top of the surface, representing the case where heat is generated uniformly in a heat volume starting at \(HH\) and ending at the top surface at \(LSUB_z\), i.e. \(LH_z = LSUB_z - HH\). The results of the computations are shown in figure 4.30. On the left results are shown for the range from 0 - 120 \(\mu m\) and on the right the scale from 100 - 120 \(\mu m\) is expanded.

In figure 4.30 the solid line represents the case of a heat region with zero thickness and the dashed line is for the case with thickness. Please note that the solid line represents the lower limit of the two. Significant differences are observed between the two cases for heights \(HH\) close to the bottom.

In the BLV 910, die the transition from emitter to base to collector is located just below the surface. From there on the epilayer extends about 6 \(\mu m\) into the surface measured from the top. Suppose that all heat is generated at the bottom of the epilayer \((HH = 114 \mu m)\). The thermal resistance is 16.7 K/W compared to 19 K/W for heat generation at the surface, a relative change of 12%.

If heat is generated uniformly in the volume of 6 \(\mu m\) the thermal resistance is 17.4 K/W, a relative change of 8%.

Similarly suppose it is possible to deposit an extra layer of a few micrometers with a thermal conductivity similar to silicon, on top of the surface. It is found from additional computations that such a layer lowers the thermal resistance with approximately 0.3 K/\(\mu m\) In practice such a layer is more or less found in the form of the metallisation of the base and emitter fingers. These metallic fingers provide some additional heat spreading.
Figure 4.30: Computed thermal resistance as function of the location of the bottom of the heat generating volume $HH$. The solid line represents a heat volume with zero thickness ($LH_z = 0$). The dashed line represents a heat volume extending to the top surface ($LH_z = LSUB_z - HH$).

**Temperature profile**

Finally the temperature profile of one heat area on top of a 120 $\mu$m substrate is studied. On the bottom of the substrate temperature is set to zero and on the top surface zero heat flux is enforced. Side-walls are not present. The simulation setup is shown in figure 4.31 on the left.

A rectangle of $1 \times 1$ mm$^2$ is defined and the heat area of $50 \times 300$ $\mu$m$^2$ is placed in the center. The thickness of the heat area is set to zero and 1 Watt of heat is uniformly injected in the heat panel. A horizontal line (H-H') and a vertical line (V-V') are defined at the top surface, crossing each other in the center of the heat area. The temperature increase along these two lines is plotted in figure 4.31 on the right. The dashed line represents the temperature along the horizontal line and the solid line is for the temperature along the vertical line. In the figure the shaded areas indicate positions within the heat panel. For both cases the maximum temperature is 19 K. From the figure it is observed that the temperature drops sharply along the horizontal line to around 10% of its maximum value at 194 $\mu$m and to 1% at 300 $\mu$m from the center. The temperature has a broader behaviour along the vertical line. At a distance from the center of 215 $\mu$m the temperature has dropped to 10% of the maximum value and at 360 $\mu$m to 1% of the maximum.

These numbers become important when more active areas are placed on the die. In that case the areas must be separated by a certain distance to avoid mutual heating: if the distance between two active areas is small the heat generated in one area heats the other area up. Based on the numbers computed it is concluded that an initial guess for this spacing is around 300-350 $\mu$m. If the active areas are brought closer together, mutual heating must be modelled.
Conclusions

Based on the calculation on one active area the following initial conclusions can be drawn:

- In the BLV 910 the side-walls are far enough from the heat volumes. Consequently, the effect is ignored.
- Variations in the thickness of the substrate on the order of 20 μm increase or decrease the thermal resistance by 6%.
- The thermal resistance is significantly reduced if the substrate thickness is reduced to ≈ 30 μm or less.
- Because the position and the thickness of the heat generating volumes is not exactly known, these volumes are approximated by heat panels at the top surface. This approximation introduces an error of around 10%.
- To have negligible mutual heating between the active areas of the BLV 910, the center to center spacing should be in the order of 300-350 μm or more.

Please note that in these conclusions the effect of the non-linear thermal conductivity and the presence of additional thermal conductors (BeO and mounting base) is not accounted for.

Interface modelling

In power transistors heat is generated in the active areas of the transistors. The heat is conducted through several differing materials to the mounting base. Normally the mounting base is placed on a metal block and cooled by forced water or air flow.

In the BLV 910 power transistor the heat is conducted from the silicon die to the BeO ceramic substrate and then transported to the mounting base below it. The effect of these interfaces
must be accounted for in the thermal models. One way is to rigorously simulate the complete structure in a three dimensional simulator and import the computed thermal resistance matrix into MDS or directly include such a simulator into MDS. There are two major drawbacks to this approach. Firstly, non-linearities in the materials used are not accounted for. This problem is solved by including these non-linearities in the simulation. This made the computed data structure, to be used in the MDS model, is more complex. Additionally, if the reference temperature changes all computations must be repeated. The second drawback is that physical insight is lost. The contribution to the overall thermal resistance of each of the separate materials is of importance. This allows the optimization of e.g. the thickness and placement of materials.

In this work a different approach is used: each of the materials involved is modelled separately and all the separate models are then connected together. In the particular case of the BLV 910 power transistor a thermal model is made of the silicon die, a separate model for the thick BeO ceramic substrate and a model for the mounting base.

The main question is how to account for heat spreading. Consider the case of heat conduction from the silicon to the BeO. At the surface of the silicon heat is generated in the active areas. The actual dimensions of these areas are used in the thermal model. The heat is conducted from these areas to the interface between the silicon and the BeO. Along this path the heat is spread out i.e. the actual dimensions of the heat areas are projected, with a heat spreading factor, on the interface of the silicon and the BeO. If separate models are made for the Si and the BeO the dimensions of the projected active areas must be determined.

Assessment of the projection heat area

Consider the case of two substrates placed on top of each other as illustrated in figure 4.32.

![Diagram of thermal resistance modelling of a composite substrate.](attachment:image)

Figure 4.32: Thermal resistance modelling of a composite substrate. An active area with width $W$ is located at the surface of the top substrate. The total thermal resistance of the composite substrate is denoted by $R_{TH}$. This resistance is supposed to be the sum of the resistances of the separate layers ($R_{TH} = R_1 + R_2$). The thermal resistance $R_2$ of the upper layer is computed first using the actual value $W$. The problem is to find the projected width $W'$ such that $R_1 = R_{TH} - R_2$.

For reasons of simplicity two-dimensional heat spreading is considered here, allowing for a clear assessment of the projection due to heat spreading. A heat generating area is located at
the surface of the upper substrate. At the bottom of the lower substrate a plane of constant temperature is defined. The total thermal resistance of the composite substrate is denoted by $R_{TH}$. Going from the top to the bottom this resistance is supposed to be the sum of the separate resistances of each of the layers. The silicon resistance is computed using the actual width $W$ and the assumption of a constant temperature at the bottom. The BeO resistance is calculated using the projected width $W'$. The main question is to find the projected width $W'$ such that $R_{TH} = R_1 + R_2$.

Assuming zero temperature on the side walls and the bottom of each of the structures the thermal resistances are found as:

$$R_{TH} = \frac{1}{WL} \sum_{n=1}^{\infty} \frac{2}{n\pi Y} \sin \left( \frac{n\pi}{2} \right) \int_{c/2-W/2}^{c/2+W/2} \sin \left( \frac{n\pi x'}{c} \right) dx'$$  \hspace{1cm} (4.28)

$$R_1 = \frac{1}{WL} \sum_{n=1}^{\infty} \frac{2}{n\pi Y_1} \sin \left( \frac{n\pi}{2} \right) \int_{c/2-W'/2}^{c/2+W'/2} \sin \left( \frac{n\pi x'}{c} \right) dx'$$  \hspace{1cm} (4.29)

$$R_2 = \frac{1}{WL} \sum_{n=1}^{\infty} \frac{2}{n\pi Y_2} \sin \left( \frac{n\pi}{2} \right) \int_{c/2-W/2}^{c/2+W/2} \sin \left( \frac{n\pi x'}{c} \right) dx'$$  \hspace{1cm} (4.30)

where

$$Y = \frac{\kappa_2 Y_1 + \kappa_2 \tanh(n\pi h_2/c)}{\kappa_2 + Y_1 \tanh(n\pi h_2/c)}$$  \hspace{1cm} (4.31)

$$Y_1 = \kappa_1 \coth(n\pi h_1/c) \hspace{1cm} Y_2 = \kappa_2 \coth(n\pi h_2/c)$$  \hspace{1cm} (4.32)

The width of the substrate is denoted by $c$ and the length in the third dimension is denoted by $L$. Please note that heat spreading in this third dimension is not accounted for. With these equations it is possible to find the projected width $W'$ rather easily by first computing the total thermal resistance $R_{TH}$ and subtracting the resistance $R_2$. In the calculation of $R_1$ the projected width $W'$ is varied until $R_1 = R_{TH} - R_2$.

Based on the procedure outlined above the projected area of one active area of the BLV 910 transistor is computed. In figure 4.32 the bottom layer represents the BeO with parameters $\kappa_1 = 270$ (W/m·K) and $h_1 = 940$ µm and the top layer represents the silicon with parameters $\kappa_2 = 150$ (W/m·K) and $h_2 = 120$ µm. The width $c$ is set to 20 mm, large enough to make side wall effects negligible. An active area of the BLV 910 transistor measures approximately 50 × 300 µm². It was found (cf. figure 4.31) that the main portion of heat spreading is for the small side of 50 µm. This side is considered in the following and the other side of 300 µm is used as the length scaling factor $L$.

The total thermal resistance $R_{TH}$ is computed using equation (4.28) and plotted in figure 4.33 as function of the width $W$. Next, the thermal resistance of the silicon is computed using equation (4.30) and plotted in the same figure. The difference $R_{TH} - R_2$ between these two resistances is assumed to be the thermal resistance of the BeO layer. This difference is plotted both in the left picture and the right picture as a dotted line.

One very interesting point is noted from this trace: for small widths the resistance for the BeO is nearly independent of the width. For larger widths the resistance steadily decreases. Note, however, that the change is only from 9.3 K/W to 6.7 K/W. Finally the BeO resistance is computed as function of the width $W'$ using equation (4.29) and plotted as a solid line.
Figure 4.33: Thermal resistance modelling of a composite BeO and Si substrate. On the left the total resistance ($R_{TH}$) and the resistance of the upper Si layer ($R_{Si}$) are computed. The difference, plotted both in the left and right picture, is supposed to be due to the BeO. By comparing this difference with the BeO resistance as function of the heat area width, the equivalent width $W'$ is found. The case of a heat area width $W$ of 50 $\mu$m is shown. The corresponding heat area width on the BeO $W'$ is found as 620 $\mu$m.

in the picture on the right. It is now easy to find the projected width $W'$ giving the same thermal resistance as the difference $R_{TH} - R_2$. In the particular case of an area width of 50 $\mu$m the total thermal resistance and the silicon resistance are computed as 29 K/W and 19.8 K/W respectively, the difference being 9.2 K/W. From the right-hand side graph it is found that a BeO with an equivalent heat injection width of 620 $\mu$m has this resistance. Therefore the projected width of the 50 $\mu$m width is 620 $\mu$m, representing substantial heat spreading. The same reasoning is applied for the long side of the heat area of 300 $\mu$m. The associated thermal resistance difference is computed as 8.8 K/W and the corresponding projected width is 700 $\mu$m. Based on the two dimensional analysis the projected area is estimated as 620 $\times$ 700 $\mu$m$^2$.

Assessment of the 3D projection heat area

In the two-dimensional analysis only two-dimensional heat spreading is included. The projection based on the two-dimensional analysis is depicted in figure 4.34 on the left. The 50 $\mu$m side spreads out to 600 $\mu$m and the 300 $\mu$m side spreads out to 700 $\mu$m assuming a constant temperature of the active area. Continuing the analysis of the Si-BeO system discussed before and using the projected shape shown in the picture, with a total area of (50 $\times$ 700) + (300 $\times$ 620) - (50 $\times$ 300) = 0.2 mm$^2$, a value of 17 K/W is found for the thermal BeO resistance.

Due to three dimensional heat spreading a much larger projected area is however expected. A crude approximation is to define the projected area as 620 $\times$ 700 $\mu$m$^2$ resulting in a thermal BeO resistance of 2.7 K/W. An even better approximation is to use the ellipse shown in the same picture. Using rectangular heat injection areas, the lengths of the sides should be lowered compared to the 620 $\times$ 700 $\mu$m$^2$ case as shown in the figure on the right. In the
Figure 4.34: Heat projection of a $50 \times 300 \mu m^2$ heat area. On the left the heat projection using the two-dimensional approximation: the $50 \mu m$ and the $300 \mu m$ side project to $620 \mu m$ and $700 \mu m$ respectively. Due to spreading effects the two dimensional approximation may prove to be too crude. As a second approximation a rectangular area of $620 \times 700 \mu m^2$, as shown in the center, may yield a too low value for the BeO resistance. A more realistic approximation is the ellipsoid shown in the center figure. To approximate the ellipsoid the rectangular 700 area should shrink as shown on the right.

A following three dimensional assessment is made of the actual projection of the heat area.

The structure under consideration is shown in figure 4.35 on the left.

Figure 4.35: Three dimensional thermal analysis. Left: two substrates with the bottom plane at constant temperature and a heat panel located in the top plane. The situation represents the case of a silicon die on a BeO substrate. Right: cross sectional view in one direction showing the two substrates and a heat panel with width $W_x$.

Two substrates are placed on each other representing the silicon and the BeO from top to bottom. At the bottom a plane constant temperature is assumed and at the top plane a heat panel representing the active area is placed. A cross sectional view is shown in the picture.
on the right. The substrate has dimensions of $L_x \times L_y$ and the heat panel is $W_x \times W_y$. The substrate heights are $h_1$ and $h_2$ and the thermal conductivities are $\kappa_1$ and $\kappa_2$ respectively. For reasons of completeness the analysis made for the two dimensional case is repeated here for the three dimensional case using a square heat panel. The heat panel is centered in the rectangular area. In the case under consideration the values are for the BeO: $h_1 = 940 \mu m$ and $\kappa_1 = 270 \text{ K/W}$ and for the silicon $h_2 = 120 \mu m$ and $\kappa_2 = 150 \text{ K/W}$. The thermal resistance is derived by integrating Green’s function over the heat panel:

$$R_{TH} = \frac{1}{W_x W_y} \int_{(L_y-W_1)/2}^{(L_y+W_1)/2} \int_{(L_x-W_1)/2}^{(L_x+W_1)/2} G(\frac{L_x}{2}, \frac{L_y}{2}, x', y') dx' dy'$$

(4.33)

$$G(x, y|x', y') = \sum_{m=1}^{\infty} \sum_{n=1}^{\infty} \frac{4}{L_x L_y \xi_x \xi_y} \sin(\xi_{x'}y) \sin(\xi_{y'}x) \sin(\xi_{x}x) \sin(\xi_{y}y)$$

(4.34)

where

$$\xi = \sqrt{\xi_x^2 + \xi_y^2}$$

$$\xi_x = n \pi / L_x$$

$$\xi_y = m \pi / L_y$$

(4.35)

$$Y = \frac{\kappa_2 Y_1 + \kappa_2 \tanh(\xi h_2)}{\kappa_2 + Y_1 \tanh(\xi h_2)}$$

$$Y_1 = \frac{\kappa_1 \coth(\xi h_1)}{\kappa_2}$$

(4.36)

The two Green’s function summations are terminated after about 1000 terms have been evaluated for each summation. The side length of this panel is varied and the total thermal resistance $R_{TH}$ is computed. Then the BeO height is set to zero and the silicon thermal resistance is computed and subtracted from the total thermal resistance. The difference is then assumed to be due to the BeO: $R_{BeO} = R_{TH} - R_{Si}$. The results of the computation are shown in figure 4.36.

![Figure 4.36: Thermal resistance modelling of a composite BeO and Si substrate. On the left the total resistance ($R_{TH}$) and the resistance of the upper Si layer ($R_{Si}$) are shown. The difference, plotted both in the left and right picture, is supposed to be due to the BeO. By comparing this difference with the BeO resistance as function of the heat area width, the equivalent side length is found.](image)

Shown on the left is the composite thermal resistance $R_{TH}$ as function of the side length of
the square area. Also shown are the silicon resistance $R_{SI}$ and the difference $R_{TH} - R_{SI}$. This difference is assumed to be due to the BeO substrate. Shown in the right picture is the same thermal resistance difference and the thermal resistance of the BeO substrate. From the figures one may note that small heat areas project to heat areas of around $500 \times 500 \mu m^2$.

Finally the calculation is performed for a $50 \times 300 \mu m^2$ heat area of the BLV 910. The computed resistances are $R_{TH} = 21.9 \text{ K/W}$ and $R_{SI} = 19.0 \text{ K/W}$, the difference being 2.9 K/W. From figure 4.34 it is observed that a square heat panel of $620 \times 620 \mu m^2$ has a thermal resistance of 2.9 K/W. In the two-dimensional analysis the ratio between the sides of the projected area was 6:7. Using this ratio the sides of the heat panel are found to be 580 \mu m and 670 \mu m respectively. In conclusion: the total thermal resistance of one active area of $50 \times 300 \mu m^2$ from the top of the silicon to the bottom of the BeO is 21.9 K/W. This total thermal resistance is assumed to be the sum of thermal resistances of the silicon (19.0 K/W) and the BeO (2.9 K/W).

**Temperature profile**

In the previous section the thermal resistance of one active area was considered: the total thermal resistance is computed, then the silicon resistance is separately computed and finally the difference between the two is assumed to be due to the BeO. Subsequently the thermal resistance of one active area is build up of the sum of the BeO resistance and the Si resistance. Trivially, this works good for the modelling of the thermal resistance.

The remaining question is whether this approach also works for the modelling of the thermal resistance matrix of the complete die. In other words: is it possible to compute the thermal resistance matrix of the eight active areas of the silicon die separately and add the resistance of the BeO? Or is it not possible to separate the two and is it necessary to compute the full structure?

Before considering the thermal resistance modelling of the full BLV 910 die, the temperature profile is computed for the die with heat dissipation in only one active area. A top view of the die, measuring $1 \times 1.1 \text{ mm}^2$, with eight heat areas is shown in figure 4.37. The temperature profile is computed along three lines: two horizontal lines and a vertical line. The active area measures $50 \times 280 \mu m^2$ and the substrate heights and thermal conductivities remain as before. Heat of 1 Watt is generated uniformly in the active area. Two methods are used to compute the temperature profiles. The first method computes the temperature by integrating Green’s function (cf. equation (4.34)) over the active area.

\[
T(x,y) = \frac{1}{W_x W_y} \int \int G(x,y|x',y')dx'dy' \quad (4.37)
\]

This model yields the correct temperature profile and is shown in figure 4.37 using solid lines. The temperature along line 1 shows a relatively narrow peak where the temperature along line 2 is broader, the maximum being 23.4 K. Please note that these temperature profiles are similar to the profiles shown in 4.31. From the last picture it is clear that the temperature rise along line 3 is 5 % or less of the maximum value.

In the second method the temperature profile is first computed considering the silicon die only, assuming zero temperature (gradient) at the bottom of the silicon die. The temperature increase due to the BeO is then added separately. At 1 Watt of dissipation this is around 3.2
Figure 4.37: Temperature profile along three lines at the top surface of the BLV 910 die. Top view of the eight heat areas is shown at the top left. Heat is generated in the bottom left heat panel. Temperature profiles are shown in the subsequent three pictures with the solid line representing the computed profiles and the dashed lines representing the approximate calculations.

K. Please note that the effect for the BeO is for one active area only. If more active areas are involved it is likely that the projected area becomes larger and the BeO resistance becomes lower.

Results of the approximate method are shown in figure 4.37 using dashed lines. From the figures it is observed that the agreement between the computed profiles (solid lines) and the approximate method (dashed lines) is good in the vicinity of the active area. However, when the distance increases, larger discrepancies become apparent. At greater distances the temperature drops to zero while the approximate model decreases to the steady value of 3.2 K. This results from the use of the approximation that the temperature at the bottom of the silicon die is constant and equal to the temperature at the top of the BeO. In the particular case of the single active area this approximation apparently is valid for locations not too far away from the active area.
Thermal resistance matrix

Using the results of figure 4.37 the thermal resistance matrix for the case of the active areas on a composite substrate of Si and BeO is found by inspection. Please note that for reasons of simplicity the mounting base is not accounted for in the analysis. An element of the resistance matrix is defined here as the temperature in the center of an active area due to heating of 1 Watt in another section. These temperatures are found by inspecting the temperature plots shown in fig 4.37.

It appears that the approximate method always overestimates the mutual resistance i.e. the off-diagonal elements of the resistance matrix. Therefore the following question must be solved: is it possible to make a thermal model for the BLV 910 under normal operating conditions based on the approximate method? This question is addressed in the next section.

4.8 Thermal resistance modelling of the BLV 910

Previously for the single area structure first the total resistance and the Si resistance were computed. The difference between these was then attributed to the BeO die. This process is repeated under the condition that heat generation is equal for all eight areas (1 Watt). The structure under consideration has not changed: eight active areas on the composite substrate of Si and BeO as shown on the left in figure 4.38.

![Diagram of active areas and temperature profiles](image)

Figure 4.38: Left: Eight active areas with heat generation of 1 Watt in each area. Temperature profiles are computed along the dashed line. Right: computed temperature profiles for the composite Si+BeO substrate (solid line), the Si substrate (dashed line) and the difference between the two profiles (dotted line).

In the structure a horizontal line is defined and temperature profiles along this line are computed for the case of the composite substrate and the silicon substrate alone. Results are shown on the right in figure 4.38. The solid line represents the temperature for the composite...
substrate. From the figure large temperature gradients are observed. The temperature in the center of the middle two areas is 35 K and drops rapidly to 22 K just outside these areas. Temperature then increases to 32 K in the outer two areas. The temperature difference is thus around 3 K between the maximum of the outer two areas and the inner two areas. This difference is due to the mutual thermal coupling where the center two areas have two "close neighbours" and the outer two only have one "close neighbour".

The dashed line represents the temperature profile with the silicon substrate only. Once again large temperature gradients are found. The difference in the maxima is smaller i.e. the mutual effect is of less significance in this case.

Finally, the dotted line is the difference between the previous two traces. Main interest is in the difference for the maxima being around 10.6 K for the outer two maxima and 12.5 K for the inner maxima. Using the 12.5 K and adding the profile of the silicon substrate approximates the actual temperature profile within 2 degrees in the active areas.

**Thermal resistance modelling of the BLV 920**

For reasons of completeness the calculations made for the eight areas are repeated for the case of 16 active areas. This situation represents heating in the BLV 920, a transistor with double the size of the BLV 910. Instead of two rows of four active areas each, two rows of eight active areas are now considered. The temperature profile for the 16 active areas on the composite substrate is first computed. Then the profile is computed for silicon only with the bottom side of the silicon die connected to ground. These two results and their difference is plotted in figure 4.39.

![Temperature profiles](image)

**Figure 4.39:** Temperature profiles of 16 active areas for the composite Si+BeO substrate (solid line), the Si substrate (dashed line) and the difference between the two profiles (dotted line).

The temperature shows a maximum of 35 K for the outer two areas and a maximum of 40 K for the inner two areas. This difference of 5 K is due to asymmetric mutual heating. This
effect is not visible in the profile using the silicon substrate only. The difference between the two profiles again varies slowly along the line and has a maximum in the center of the area. By taking the maximum of the difference (17.6 K) and adding the silicon temperature profile the value of 40 K is approximated very well for the center areas. Temperature for the outer two areas is then overestimated by 5 K. Note that the total temperature increase is larger than was the case for the BLV 910 shown in figure 4.38.

From the above it is concluded approximating the actual temperature profile by adding the maximum of the temperature difference and the profile of the silicon only works reasonably well for the BLV 910. Larger differences are found, however, for increasing size (BLV 920), especially for the outer active areas.

Up till now the effect of the mounting base and the effect of the nonlinear thermal conductivities were ignored. Both effects are considered in the following.

**Effect of mounting base**

To investigate the effect of the mounting base, one layer is added to the structure shown in figure 4.35 and equations (4.36) are modified to account for the extra layer. The structure is calculated with and without the additional mounting base. The temperature profiles along the dashed line of figure 4.38 are plotted in figure 4.40.

![Temperature profiles and difference](image)

**Figure 4.40**: Left: Temperature profiles along the dashed line of figure 4.38. The solid line and the dashed line represent the profile with and without the mounting base respectively. Right: The difference between the two profiles.

The solid line represents results with the mounting base while the dashed line is for the case without mounting base. For reasons of convenience the difference is plotted in the same figure on the right. From these pictures a relatively small increase in temperature of 1.25 K is observed.

**Linear model of BLV 910**

Based on the previous results it is concluded that the three layers of the BLV 910 can be modelled separately i.e. for each layer a separate model is built and these models form the
complete thermal model. This process is illustrated in figure 4.41 where in the left picture the eight active areas are numbered.

![8 x 8 thermal matrix](image)

Figure 4.41: Linear model of the BLV 910. Shown on the left the numbering of the active areas. Shown on the right the linear model comprising an 8 x 8 resistance matrix for the 8 active areas, a resistance of 12.5/8 K/W for the BeO and resistance of 1.3/8 K/W for the mounting base.

First the 8 x 8 thermal matrix for the silicon is computed with the bottom side of the silicon assumed at constant temperature. Each elements specifies the temperature increase in the center of an area when heat is uniformly generated in an (other) area. The elements of the first column of this matrix (in K/W) are as follows:

\[
R_{TH,11} = 20.2 \quad R_{TH,21} = 1.1 \quad R_{TH,31} = 0.08 \quad R_{TH,41} = 6 \cdot 10^{-3}
\]
\[
R_{TH,51} = 4 \cdot 10^{-2} \quad R_{TH,61} = 2 \cdot 10^{-2} \quad R_{TH,71} = 5 \cdot 10^{-3} \quad R_{TH,81} = 8 \cdot 10^{-4}
\]

With these values and using symmetry (\(R_{TH,21} = R_{TH,32}\) etc.) the complete matrix is easily found. The model for the silicon has an additional node connected to the BeO model. This extra node is easily implemented in an electrical simulator using Kirchhoff’s current law. In figure 4.38 a maximum temperature difference of 12.5 K was found between the structure with and without BeO with a heat generation of 8 Watts. Assuming this difference is due only to the BeO only the layer may be modelled using one resistor of 12.5/8 K/W. Similarly in figure 4.40 a maximum temperature difference of 1.3 K was found between the structure with and without the mounting base with a heat generation of 8 Watts. Assuming this difference is due only to the mounting base this layer may be modelled using one resistor of 1.3/8 K/W.

### 4.9 Nonlinear thermal conductivity

In order to investigate the effect of the nonlinear thermal conductivity on the thermal resistance, Kirchhoff voltage sources are added to all nodes of the linear model shown in figure 4.41. As an illustration the block with the 8 x 8 matrix is shown again in figure 4.42 with voltage sources added to all nodes.
Figure 4.42: Nonlinear modelling of the BLV 910. Thermal resistances as function of dissipated power. The dotted trace displays the temperature drop over the thermal resistance modelling the BeO and the dashed trace models the maximum temperature drop over the Si. The total temperature drop is modelled by the solid line.

These voltage sources transform the linear temperatures at the matrix ports to the actual temperatures. Similarly two voltage sources are added to the thermal resistance of the BeO and two sources are added to the resistance of the mounting base similar to figure 4.3. The effect of the total dissipated power is studied by computing the thermal resistance i.e. the temperature drop over a layer divided by the total dissipated power. With the mounting base temperature set to a reference value of 300 K, the power dissipation is swept from 0 to 50 Watts. The computed thermal resistances of the BeO and the Si are plotted in figure 4.42 on the right. The dashed line represents the resistance of the BeO and the dotted line is for the Si. The thermal resistance of the mounting base is low and not plotted in the figure. The total thermal resistance, found by adding the three resistances (Mb+BeO+Si), is plotted in the figure using a solid line.

The total thermal resistance is around 4.5 K/W and increases to 6.3 K/W at 30 Watts of dissipation and increases further to 8.3 K/W at 50 K. Please note that under practical conditions dissipation will not go further than 30 Watts. The thermal resistance of the silicon follows the same trend: at low dissipation levels the resistance is 2.8 K/W and increases to 6.2 K/W at 50 Watts of dissipation. The explanation for this behaviour is that the temperature is maximum in the active areas at the top surface of the silicon. This large temperature increase reduces the thermal conductivity and increases the thermal resistance of the silicon layer. The BeO thermal resistance however is much less effected by the dissipation. At low dissipation the resistance is 1.6 K/W and increases to 2.0 K/W at 50 Watts of dissipation.

Summing up, it has been shown that the total resistance is strongly dependent on temperature and is mainly dominated by the thermal resistance of the silicon. The thermal resistance of silicon is temperature dependent and the maximum temperature is reached at the heat areas on the top surface of the silicon.
4.10 Electro-thermal modelling of one area

This section considers the electro-thermal modelling of one active area where all previous sections of this chapter are concerned with thermal modelling alone. Within an active area a temperature profile exists i.e. temperature varies with the position, and consequently, the electrical behaviour also depends on the position. Also note that the heat generation is no longer uniform within an active area. To study this effect on the DC behaviour one active area is gridded into a number of rectangular areas of approximately the same size. Each rectangular area is modelled using a single compact transistor model having its own temperature node. The following questions arise:

- How many grid elements are needed to represent the electrical behaviour of one active area correctly?
- How many transistor models, each having its own temperature, including significant thermal interaction between individual compact models can the simulator handle?

In figure 4.43 on the left four different griddings of an active area are shown.

![Electro-thermal modelling of one active area](image)

Figure 4.43: Electro-thermal modelling of one active area. Left: different griddings to study the effect of the temperature profile in the active area on DC traces. Right: linear thermal model of the active area. Kirchhoff transformations are added to account for the non-linear thermal conductivities.

The number of grid elements and the number of compact models are $1 \times 1$, $1 \times 6$, $2 \times 12$ and $3 \times 18$ respectively. For reasons of illustration the linear thermal model is shown in figure 4.43 on the right. To obtain the values of the resistors for the mounting base and the BeO the procedure outlined before is used. First the resistance of one active area on silicon is computed (20.2 K/W) and one active area on the composite substrate of Si and BeO is computed (23.4 K/W). The difference is assumed to be due to the BeO (3.2 K/W). Finally the resistance of the active area on Si, BeO and the mounting base is computed (23.6 K/W) and the mounting base resistance is found (0.2 K/W).

The thermal interaction within the active area is modelled by the thermal matrix computed for the silicon where the number of elements is equal to the square of the the number of grid elements. For example in case of the $3 \times 18$ gridding the number of grid elements is 54 and the thermal matrix contains $54 \times 54$ elements.
To complete the thermal model, Kirchhoff transformations are added to all nodes to account for the nonlinear thermal conductivities. For reasons of simplicity the bases of all compact models are connected together to form the base of the active area. A similar procedure is followed for the collector and the emitter.

Two cases are considered:

- Forced base current. The emitter is grounded and the collector is connected to a variable voltage source. The base current is forced to 1.5 mA introducing significant dissipation and self heating.
- Forced base voltage. Again the emitter is grounded and the collector is connected to a variable voltage source. The base voltage is set to 1.4 V introducing significant dissipation and self heating.

Prior to studying the effect of the gridding and the self heating, the effect of the temperature is first computed i.e. in the simulator the temperature at the temperature node of the compact model is forced to a certain temperature difference ($\Delta T$) with respect to the reference temperature. The two cases, forced base current and forced base voltage, are plotted for three different temperature differences in figure 4.44 on the left and the right respectively.

![Graphs showing collector current vs collector voltage for different temperatures](image)

**Figure 4.44:** Electro-thermal modelling of one active area for different temperatures. On the left the collector current versus the collector voltage with a forced base current of 1.5 mA. On the right the collector current versus the collector voltage with a forced base voltage of 1.4 V.

From these two figures, positive feedback of temperature on the collector current is observed i.e. if temperature increases the collector current also increases.

The collector current is plotted versus the collector voltage for these two cases in figure 4.45.

On the left the result for the forced base current is shown. The maximum temperature increase with respect to the reference temperature of 273 K is around 160 K at a collector voltage of 30 V. To establish a baseline the isothermal case is also plotted and significant differences are found between the isothermal and the non-isothermal case. Small differences are observed between the various gridded cases. A maximum difference of 10 % in the collector current is found between the $1 \times 1$ and the $3 \times 18$ case at a collector voltage of 30 V. On the right in figure 4.45 the result for the forced base voltage is shown. The maximum
temperature increase with respect to the reference temperature of 273 K was found to be 180 K at a collector voltage of 30 V. Once again comparison the isothermal case is also plotted and significant differences are found again between the isothermal and the non-isothermal case. Small differences are observed between the various gridded cases however. A maximum difference of 7% in the collector current is found between the $1 \times 1$ and the $3 \times 18$ case at a collector voltage of 30 V.

Please note that in both cases $1 \times 1$ gridding leads to the highest current. This is explained by the fact that in this case one compact model is at the maximum temperature. In all other griddings only a few compact models are at the maximum temperature and the others are at a lower temperature. Transistors at a lower temperature introduce less positive feedback of temperature on the total current and consequently lower the current in an area.

The comparison on the computations were performed using a $4 \times 24$ grid. The thermal matrix for the silicon die contains 9216 elements in this case. The results did not significantly vary from the $3 \times 18$ gridding however.

An important point to note is that the two examples given above represent worst cases, since under normal conditions the dissipation and the temperature increase are much less.

- The number of compact models to model the DC behaviour of an active area should be chosen between 1 and 24. Introducing more compact models results in longer computational times without changing the results significantly.
- The simulator was able to cope very well with all cases presented here. It is worthy of note that the thermal interaction between the subareas is relatively large. Although simulation times increase rapidly at finer grids the simulator handles a grid of $4 \times 24$ compact models and a $96 \times 96$ thermal matrix well.
- Modelling an active area with one compact model introduces a maximum error of 10% under extreme conditions.
4.11 Retrospective: interface modelling

In previous sections a considerable amount of attention was paid to the modelling of the interfaces. By separating the Si, BeO and Mb, a good idea is obtained about the relative effects. In addition nonlinearities in the respective thermal conductivities are easily accounted for by introduction of Kirchhoff's transformations at the interface nodes. The model derived for the BLV 910 is shown in figure 4.46 (a). The silicon is modelled by an $8 \times 8$ thermal matrix, the BeO and the Mb are both modelled by a single resistor.

![Diagram](image)

Figure 4.46: Different thermal modelling approaches for the BLV 910. (a) Division into a matrix for the silicon and resistors for BeO and Mb. (b) For a better treatment of the interface conditions the BeO resistor is replaced by a matrix. (c) One matrix for Si and BeO, with the interface condition correctly implemented. (d) One matrix for Si, BeO and Mb.

A major drawback of this model is its inability to model the coupling between the active areas correctly as illustrated in figure 4.38. To better approximate this coupling the interface between the Si and BeO must be modelled with great care. One option is to create heat panels at the bottom of the Si and to connect these with corresponding heat panels at the top surface of the BeO e.g. 8 heat panels at the bottom surface of the Si and 8 panels at the top surface of the BeO. The size of these panels is found by projecting the active areas to the bottom surface as discussed in figure 4.34. Using this method the silicon is modelled by an $16 \times 16$ matrix (8 active areas and 8 heat panels at the bottom) and the BeO is modelled by an $8 \times 8$ matrix as shown in figure 4.46 (a). This method may be extended by discretising the
complete interface with heat panels as discussed in figure 4.24. Although not shown here, this approximation was also used to model the BLV 910 with similar results as discussed in section 4.8. Although the thermal coupling between active areas is better approximated, the thermal matrices and the number of Kirchhoff transformations grows rapidly.

A third option is to treat the Si and BeO as a composite substrate and compute the $8 \times 8$ thermal matrix directly using the Green's function of equation (4.34). With this option the complexity of the model is kept low and the coupling between areas is modelled correctly (figure 4.46 (c)). It is, however, not possible to include the Kirchhoff transformation at the interface. In figure 4.42 it is shown that the effect of the nonlinearity in the BeO is negligible if the reference temperature is close to the actual temperature. Additionally, at that interface two Kirchhoff transformations are placed "head to head". One transformation transforms the linear BeO temperature up to the actual temperature and the second transformation transforms it down again to the linear Si temperature. Because the underlying shape of the transformation is almost the same for both transformations, these intermediate transformations can be left out without introducing much error.

Going one step further the Si, BeO and mounting base are treated as a three layer substrate and an $8 \times 8$ thermal matrix is computed using the Green's function method of equation (4.34). The resultant model in the simulator is the $8 \times 8$ matrix. Kirchhoff's transformations are added to the eight top nodes for the active areas.

### 4.12 Conclusions

This chapter is concerned with building thermal models of power transistors. Of the three methods of heat transportation (conduction, convection and radiation) the main portion of heat is conducted from the silicon to the beryllium oxide and to the mounting base. One-dimensional modelling of heat conduction is similar to modelling of currents and voltages on a RC transmission line (section 4.3). Additionally, it is possible to define a thermal skin depth similar to the electrical skin depth. The thermal skin depth forms the base for a rule of thumb approximation for the heat penetration as function of frequency. To account for heat spread the one-dimensional model is transformed into a non-uniform transmission line model. Using this model and using a measured heating up curve of the BLV 910, an accurate fit is obtained between the modelled and the measured heating up curve. Using the one-dimensional model it is shown that at the RF frequencies of interest for the BLV 910 the thermal impedance is almost zero. Consequently, under CW conditions only the DC component of the dissipation is considered.

Four different (electro-)thermal measurement methods are discussed in brief: infrared measurements, probing methods, Liquid Crystal methods and electro-thermal characterisation based on the relation between base emitter voltage and temperature. Infrared measurements give a good impression of temperature profiles. A major drawback is the limited spatial resolution and the fact that bondwires obscure the full picture. In principle probing methods should produce accurate temperature profiles with a rather high resolution. Due to technical difficulties it was not possible to apply this method with success to the power transistor under consideration. Profiling methods based on liquid crystal methods also should produce accurate plots with a high resolution. Again due to technical difficulties it was not possible to apply this method with success. Thermal characterisation of bipolar transistors using the
relation between base-emitter voltage and temperature is a commonly used method. This method allows a reasonable assessment of the thermal resistance. It is not easy however to make a temperature profile as is the case with infrared measurements.

Two methods are considered for the three-dimensional resistance modelling of power transistors. In the first method the thermal heat conduction equation is discretised in an electrical simulator using resistors (and capacitors if necessary). Only rather simple structures can be solved with this method when using the MDS simulator due to simulation time and memory size limitations. In the second method the thermal resistance matrix is directly computed using Green's functions. With models based on this method implemented in MDS first the effect of several parameters on the thermal resistance of an active area in the silicon die is computed. The effect of the sidewalls of the silicon die is found to be negligible. The exact location and thickness of the heat generating volumes has a significant effect on thermal resistance.

The initial thermal model of the BLV 910 consists of an $8 \times 8$ thermal matrix for the silicon, a single resistor for the BeO and a resistor for the mounting base. The values of the matrix and the resistors are computed using a procedure using physical parameters (dimensions and thermal conductivities) as input. Nonlinearities in the conductivities are accounted for using Kirchhoff transformations at all nodes.

Finally electro-thermal interaction in one active area is studied. The active area is gridded into a number of rectangular areas and each area is modelled by a compact transistor model having its own temperature node. All compact transistor models are connected to a thermal matrix model including all thermal interactions between the active areas. One active area is modelled well with one compact model. For higher accuracy the active area is modelled by $2 \times 12$ compact models, each model representing an area of approximately $25^2 \, \mu m^2$. 
Chapter 5

Modelling and measurement of RF high power bipolar transistors

5.1 Introduction

In the previous chapters modelling of the separate elements of the RF high power bipolar transistor are considered. In this chapter all these models are brought together to form the full model of the BLV 910 power transistor. The BLV 910 transistor is measured under DC, RF small signal and RF large signal conditions and the results are compared with model simulations. The results of the comparison is based on the work of R. Tinti and K. Mouthaan. A shortened version of this chapter can be found in the proceedings of the Essderc conference of 1999 [59]. The measurement results are discussed in greater detail in the thesis of R. Tinti [31]. For reasons of completeness in section 5.2 the electrical models for the bondwires, the prematch capacitor and the package are discussed in brief. The heat generated in the die is injected into the thermal model of the die, BeO and the mounting base. This thermal model is discussed in brief in section 5.3. The first test of the model is the modelling of the DC behaviour. The comparison of DC results is given in section 5.4. Next in section 5.5 the small signal RF behaviour is considered. Small signal S-parameters are compared at various biasing points. Finally the model is tested for the RF behaviour under large signal conditions in section 5.6. The accurate modelling of RF large signal parameters is the main drive for the research presented in this work. The large signal parameters include output power versus input power, efficiency versus input power and input- and output impedance. The chapter ends with conclusions and important recommendations.

5.2 Electrical models

Bondwires model

The modelling of the bondwires is based on Neumann’s inductance equation where the self- and mutual inductance of wires are computed. For the bondwire structure of the BLV 910 the model for 12 coupled wires is used. The Cartesian coordinates serving as input for the
model are obtained from top view and side view SEM photos of the BLV 910. To check the coordinates entered in the model a top view layout is generated automatically as shown in figure 5.1.

![Diagram of a semiconductor layout](image)

Figure 5.1: Top view of the automatically generated layout of the coupled bondwires. The two dashed boxed represent the position of the prematch capacitor and the die respectively.

**Prematch capacitor model**

The model for the prematch capacitor uses the model introduced in section 3.3 and shown on the right of figure 3.34. The capacitor is modelled using a transmission line and assumes quasi-TEM wave propagation along the length direction of the MOS contact as shown in figure 5.2.

Model parameters are extracted from electromagnetic simulations and the frequency dependent data is stored in a dataset. During electrical simulations of the capacitor relevant data is retrieved from the dataset. The model accounts for the skin effect behaviour of longitudinal currents in the substrate. The ohmic contact is assumed ideal, i.e. the current from the emitter bondwires directly flows into the package. Coupling between the MOS contact and the ohmic contact is also ignored.

To understand how the prematch model is connected to the other models, two sections of figure 3.34 are shown connected together in figure 5.3 representing the prematch capacitor. Please note that for reasons of simplicity only two sections are shown.

On the left and right connections are made to internal ports (8) and (9) respectively of the package model. In the center a connection is made to the bondwire model.

**Package model**

The package model is built using electromagnetic simulations. In section 3.4 Sonnet's Em is used to simulate the package with 6 external ports and 6 internal ports. In the final model presented in this chapter, the simulations are repeated in Agilent’s Momentum. This simulator
Figure 5.2: In the prematch capacitor model current is assumed flowing along the length direction of the MOS contact.

Figure 5.3: Illustration of connecting the prematch model to the internal ports of the package models and the bondwire model.

allows the definition of an internal port on the emitter bridge and therefore allows a more realistic representation of the emitter bridge. Computed S-parameters are stored in a dataset and retrieved during electrical simulations of the package.

**Die model**

The model of the die uses the Mextram compact transistor model. To account for the temperature a thermal node is added to the model. The electrical parameters of the compact model are extracted from pulsed iso-thermal measurements. The temperature scaling parameters are extracted from measurements of electrical parameters at differing reference temperatures. The number of compact models for the full die depends on the required accuracy in the electro-thermal interaction. In section 4.10 it is shown that for DC operation the number of compact models per active area can be kept low without introducing a large error in the areas of normal operation. Only at extreme voltages and currents the errors become significant.
Therefore in the model one compact model per active area is used. Because the die of the BLV 910 has two axes of symmetry only two compact models are needed for modelling the die instead of eight. This speeds up the simulations times significantly.

5.3 Thermal models

The thermal modelling uses the model discussed in section 4.10 i.e. the silicon die is modelled as an $8 \times 8$ thermal resistance matrix and the BeO and the mounting base are modelled with a single resistor. Values of the matrix and the resistors are computed from equation (4.34). The nonlinearity of the thermal conductivity of the silicon is accounted for using Kirchhoff voltage transformations at all the nodes of the $8 \times 8$ matrix.

Once again, due to symmetry the four nodes representing the temperature at the four outer active areas are connected together and the remaining four nodes are also connected together.

5.4 DC analysis

The first comparison of the model with measurement is for the DC behaviour. Two options are available: a forced current or a forced voltage to the base. The main disadvantage of a forced voltage to the base is the possibility of thermal runaway destroying the device. Therefore a forced current is applied to the base. The circuit setup is shown in figure 5.4 on the left including the BLV 910 transistor, a current source feeding the base and a voltage source applied between collector and emitter.

![Circuit Diagram](image)

Figure 5.4: Left: Circuit setup for finding $I_c-V_{ce}$ curves using a forced base current and a variable collector emitter voltage. Right: measured and calculated $I_c-V_{ce}$ curves for a base current $I_b$ of 1, 3, 5, 7, 9, 11, 12, 13, and 14 mA. The calculated results with- and without self heating are both plotted in the figure.

The major drawback of this setup is that the modelling of the current gain becomes important.
In power transistors, the current gain is of less importance. Devices show a large variation in current gain from device to device. One device can have a current gain of 50 while a second device has a current gain of 100. To compare measurements with the model, the value of the current gain is the parameter being optimized for a best fit between model and measurement. The results of the model and measurement are shown on the right in figure 5.4. Three types of lines are displayed, with thermal effects included in the first two traces: the solid lines represent the model, the dots represent measured values and the dashed lines represent the model without thermal effects. Although not shown in the figure, it is found that the results of the isothermal model correspond extremely well with measured isothermal results.

In figure 5.5 the low voltage region is zoomed in where once again the solid lines represents the model and the dots represent measured data.

![Figure 5.5: First part of figure 5.4 showing measured and calculated $I_c-V_{ce}$ curves for a base current of 1, 3, 5, 7, 9, 11, 12, 13, and 14 mA in the low voltage regime.](image)

From the above the following important observations and conclusions are made:

- In comparing the model with measurements with a forced base current the current gain is the parameter used as a fitting parameter. The measured current gain shows a large variation from device to device.

- Temperature significantly effects the DC behaviour of the power transistor and consequently thermal effects must be accounted for in modelling the power transistor.

- The measured and modelled $I_c-V_{ce}$ curves shown in figure 5.4 and 5.5 correspond extremely well.
5.5 Small signal analysis

The second comparison of the model of the BLV 910 with measurements is for the small signal S-parameters at fixed bias points. In this comparison the combined effect of package, bondwires, prematch capacitor and the bias dependency of various parameters of the compact transistor model and thermal effects come into play. This serves as a first test for the modelled RF behaviour. If the scattering parameters are far off it is most likely that the large signal behaviour is poorly modelled.

The standard setup for the measurement consists of a microwave test fixture in combination with two bias-T's. For the testfixture a special block is prepared where water can flow through a channelised system to remove the heat from the mounting base. The water is forced through the block using the water pump of a circulating cooling system. The temperature in the reservoir of this cooling system can be set to any reasonable value. In the case under consideration this temperature is set to 297 K. With this setup the scattering parameters as function of bias and reference temperature are measured with relative ease.

The results at the following two points are shown:

- $V_{ce} = 2.5$ V and $I_b = 5$ mA.
  The comparison between model and measurement is shown in figure 5.6.
- $V_{ce} = 10$ V and $I_b = 5$ mA.
  The results are shown in figure 5.7.

From these two figures and additional results not shown here, the following conclusions are drawn:

- The scattering parameters at the measured bias points are modelled very well especially in the area of interest around 1 GHz.
- The scattering parameters do not change dramatically as function of the biasing in the non-saturating area.
- When varying the bias the measured S-parameters change. The same change is also observed in the calculated S-parameters.
Figure 5.6: Modelled and measured scattering parameters as function of frequency at the bias point of \( V_{ce} = 2.5 \) V and \( I_b = 5 \) mA.
Figure 5.7: Modelled and measured scattering parameters as function of frequency at the bias point of $V_{ce} = 10 \text{ V}$ and $I_b = 5 \text{ mA}$.
5.6 Large signal analysis

The last test of the modelling is in the large signal behaviour. Under these conditions all nonlinearities of the transistor come into play. Designers of power transistors want to predict the following quantities using a model:

- The input and output impedance. The source impedance and load impedance are optimized to achieve maximum gain or maximum efficiency. The input and output impedance at these maxima are of importance.
- Efficiency. A high efficiency indicates a well optimized transistor as little power is dissipated. In general, power transistors are optimized for efficiency.
- Gain. The gain is the other important parameter that power transistors are optimized for. Having high gain reduces the need for many intermediate stages in amplifier design. The power gain of the BLV 910 is more than 10 dB.
- Output power versus input power (PiPo-curve). The output power versus input power is another way of representing the gain. A PiPo-curve clearly shows up till what input power the transistor behaves linear and at what input power the transistor starts to saturate.

Test circuit

To be able to make a good and honest comparison between simulation (the model) and measurement a test circuit and a test strategy must be chosen with care. In the following first the general idea of testing as used both in simulation and measurement, is discussed in brief. It is followed by a description of the setup for measurement and the setup for simulation respectively.

The basic setup for testing is shown in figure 5.8.

![Test circuit diagram](https://via.placeholder.com/150)

Figure 5.8: Large signal schematic. On the left side the source with available power $P_s$ and impedance $Z_s = R_s + jX_s$ is shown. On the right the load with impedance $Z_L = R_L + jX_L$ is shown. DC bias is supplied on the base with voltage $V_{BE}$ and on the collector side with $V_{CE}$.

In the center of the figure the device under test is shown: the BLV 910 in common emitter configuration. A power source, with available power $P_s$ and impedance $Z_s = R_s + jX_s$ is connected to the base of the device as shown on the left. If this source is terminated with an impedance equal to the complex conjugate of the source impedance then all available power flows into the terminating impedance. To bias the base of the transistor with the voltage $V_{BE}$ choke inductor is placed between the voltage input and the base. To avoid bias current flowing through the source a capacitor is placed between the base and the source.
A similar network is placed at the output where the bias voltage is $V_{CE}$ and the terminating impedance is $Z_L = R_L + jX_L$.

For setting the bias of the transistor the RF source is switched off. The collector voltage $V_{CE}$ is applied and the base voltage $V_{BE}$ is increased until the collector current $I_C$ reaches a desired level. For the BLV 910 a low level of 25 mA is chosen i.e. a small current flows through the transistor keeping the transistor open.

The power source is switched on to a level such that the output power at the expected maximum gain is equal to a specific output power. In case of the BLV 910 this specific output power is 40 dBm (10 Watts). Then the source is varied to maximise the power flowing into the transistor and the load impedance is varied until maximum gain is achieved or maximum efficiency is achieved. Consider the case of maximising for gain of the BLV 910. First the source impedance is optimized for maximum power flowing into the transistor. Next the output impedance is optimized for maximum gain. Most likely the desired output power is not achieved and the input power consequently must be increased or decreased. Additionally, by changing the load impedance the optimum source impedance might be changed. Then the source impedance and the output impedance are changed again for maximum gain. etc. This process is repeated until the desired output power is reached under maximum gain operation. Once the stable point is found the complex conjugates of the input and output impedances are the impedances sought for. In general the designers of the matching circuitry (the printed circuit boards in figure 1.2) need these impedances to design the matching networks. At that point various curves are measured keeping the source and load impedance fixed. This represents the practical situation where the drive level can vary with the input and output matching circuitry being fixed and tuned for drive level only.

- Collector current versus output power.
- Efficiency versus output power.
- Gain versus output power.
- Output power versus input power.

**Harmonic impedances**

An important factor not mentioned thus far are the input and output impedances at the harmonic frequencies. In nonlinear operation the output signal is a distorted sine when the transistor is driven by a sine wave. This distorted sine is a summation of pure sines with harmonic frequencies: if the BLV 910 is driven by a sine with a frequency of 900 MHz, signals with frequencies of 900 MHz, 1800 MHz, 2700 MHz etc. appear at the output. Consequently, the terminating impedance for these harmonics is of significant importance.

In the comparison between model and measurement discussed in this work, the impedance at the harmonics are set to the same value in both cases. This is achieved by measuring the harmonic impedance in the measurement setup and using the values found in the simulation setup. This procedure is not applied to the impedances at the fundamental frequency.

**Measurement test circuit**

The measurement setup is a bit different from the basic setup of figure 5.8. First of all the source is built using a general power generator with a fixed impedance followed by a tuner. These tuners transform the fixed impedance of the source to another, complex, impedance. At the output a load with a fixed impedance is used. Once again a tuner is used to transform
<table>
<thead>
<tr>
<th>Frequency (MHz)</th>
<th>Meas. $Z_s$ ($\Omega$)</th>
<th>Sim. $Z_s$ ($\Omega$)</th>
</tr>
</thead>
<tbody>
<tr>
<td>850</td>
<td>2.5 - $j$ 5.5</td>
<td>1.7 - $j$ 3.4</td>
</tr>
<tr>
<td>900</td>
<td>2.0 - $j$ 5.8</td>
<td>2.1 - $j$ 3.5</td>
</tr>
<tr>
<td>950</td>
<td>2.9 - $j$ 5.8</td>
<td>2.5 - $j$ 3.5</td>
</tr>
</tbody>
</table>

Table 5.1: Comparison of measured and simulated optimum source impedances for three frequencies.

the fixed load impedance to another impedance.
Secondly bias T's are used to bias the transistors. Within these bias T's the same principle
of a decoupling capacitor and a choke inductor as shown in figure 5.8 is found. These bias
T's are of course not perfect and they have a specified behaviour within a certain frequency
range.

**Simulation test circuit.**

The simulation setup is equal to the setup shown in figure 5.8. As mentioned before the
source impedance and the load impedance at harmonic frequencies are set to the respective
harmonic values as were measured in the measurement setup.
The simulation procedure is as follows:

1. The load impedance is set to starting values found in the measurements when optimiz-
ing for gain.
2. The available source power is varied until the desired output power is achieved. In the
   results considered here the desired output power is 10 Watts (40 dBm).
3. The source impedance $Z_s$ is set to the complex conjugate of the input impedance of the
   transistor ($Z_{in}$). The input impedance $Z_{in}$ is computed from the voltage at the input and
   the current flowing into the input of the transistor.
4. Steps 2 and 3 are repeated until the impedance doesn't change anymore. It is found
   that only two steps are sufficient.

After the optimum source impedance is found the output impedance for maximum gain or
maximum efficiency is found:

1. The output impedance $Z_L$ is varied for maximum gain or for maximum efficiency.
2. The source power is varied to achieve the desired output power (40 dBm).
3. Steps 1 and 2 are iterated until the impedance doesn't change anymore.

**Comparison of Simulation and measurement**

The model and measurement are compared for the case of 10 Watts output power at a col-
lector voltage $V_{CE}$ of 26 V. The quiescent current, the collector current with input power
switched off, is set to $I_{CO} = 25$ mA. The temperature of the mounting base is fixed at 293 K
using a watercooling system. As described previously a source pull is performed to find the
source impedance ($Z_s$) giving maximum input power matching.
The comparison of the source impedances achieving maximum power flowing into the tran-
sistor is displayed in table 5.1.
From the figure a good match is found between the measured and simulated real part of the
<table>
<thead>
<tr>
<th>Frequency (MHz)</th>
<th>$Z_L$ (Ω)</th>
<th>$\eta$ (%)</th>
</tr>
</thead>
<tbody>
<tr>
<td>850</td>
<td>4.9 + j 13.1</td>
<td></td>
</tr>
<tr>
<td>900</td>
<td>4.7 + j 12.4</td>
<td>4.7 + j 11.9</td>
</tr>
<tr>
<td>950</td>
<td>4.8 + j 11.4</td>
<td>4.4 + j 11.1</td>
</tr>
</tbody>
</table>

Table 5.2: Comparison of measured and simulated load impedances optimized for maximum efficiency at three frequencies.

<table>
<thead>
<tr>
<th>Frequency (MHz)</th>
<th>$Z_L$ (Ω)</th>
<th>Gain (dB)</th>
</tr>
</thead>
<tbody>
<tr>
<td>850</td>
<td>4.9 + j 11.3</td>
<td>5.9 + j 11.6</td>
</tr>
<tr>
<td>900</td>
<td>4.6 + j 10.8</td>
<td>5.5 + j 10.9</td>
</tr>
<tr>
<td>950</td>
<td>5.2 + j 10.4</td>
<td>5.0 + j 10.1</td>
</tr>
</tbody>
</table>

Table 5.3: Comparison of measured and simulated load impedances optimized for maximum gain at three frequencies.

source impedance. A rather high difference in the imaginary part of 1-2 Ω is found however. An error of 1.5 Ω corresponds to an equivalent series inductance of 1.5/ω = 0.25 nH at 950 MHz. At present the source of this error had not been identified.

**Maximum efficiency results**

After finding the source impedance a load pull for maximum efficiency is performed i.e. the output impedance is optimized for maximum efficiency with the prerequisite of 10 Watts output power. The impedances at three different frequencies are shown in table 5.2. The correspondence between measured and simulated optimum load impedance is good and the efficiency is also predicted well.

Using the impedances found, plots are made of various parameters versus output power. Relevant plots are shown in figure 5.9 for a frequency of 950 MHz. It is noted that an astonishing good agreement between model and measurement is found.

**Maximum gain results**

The same procedure as before is followed but now the impedance is optimized for maximum gain i.e. the output impedance is optimized for maximum gain with the prerequisite of 10 Watts output power. The impedances at three different frequencies are shown in table 5.3. Reasonable agreement is found for the real part of the load impedance and good agreement for the imaginary part of the impedance is found. Additionally, the gain is predicted very well.

Using the impedances found, plots are made again of various parameters versus power. Relevant plots are shown in figure 5.10 for a frequency of 950 MHz. Once again good agreement between model and measurement is found from the plots.
Conclusions

From the above results the following conclusions are made:

- The real part source impedance for maximum power flowing into the transistor is predicted well.
- A systematic difference is present in the imaginary part of the source impedance. The cause of this error has not been found.
- Both the real and imaginary part of the optimum load impedance are predicted well when optimizing for efficiency. The efficiency itself is also predicted very well.
- Also the real and imaginary part of the optimum load impedance are predicted well when optimizing for gain. The gain itself is also predicted very well.
- Gain versus power and efficiency versus power are also predicted very well.
Figure 5.9: Large signal parameters at 950 MHz with the load impedance optimized for maximum efficiency. Solid line represents the modelling and the dashed line represents measurements. Top left: collector current as function of output power, top right: gain, bottom left: efficiency and bottom right: output power versus input power.
Figure 5.10: Large signal parameters with source and load impedance optimized for maximum gain. Solid line represents the modelling and the dashed line represents measurements. Top left: collector current as function of output power, top right: gain, bottom left: efficiency and bottom right: output power versus input power.
5.7 Conclusions

In this last chapter the modelling is compared to measurements in three phases: DC curves, AC small signal curves and AC large signal curves. From these comparisons the following conclusions are made:

- The model represents the DC behaviour both isothermal and non-isothermal very well. In the non-isothermal results shown in figure 5.4, the electrothermal interaction is fully accounted for.
- The model represents the small signal scattering parameters very well around the area of interest (900 MHz). Two examples of the results are shown in figures 5.6 and 5.7. At higher frequencies differences between model and measurement occur. These can be due to both model inaccuracies as well as measurement errors.
- The most important behaviour, the large signal behaviour of the transistor, is modelled well. The modelling of input and output impedances shows significant errors. Especially the imaginary part of the input impedance shows a considerable error. Gain, efficiency and output power versus input power are modelled very well.
Chapter 6

Conclusions and recommendations

In this final chapter a very brief overview is given of the work presented in this thesis. Conclusions and recommendations for further theoretical and experimental work are given.

Review of the problem

In recent years mobile communications has grown explosively. These wireless networks are build up around base stations operating at frequencies around 900 Mhz and 1800 Mhz (RF, radio frequency). The base stations are connected to the "wired" telephone network. To be able to receive the base station with a mobile telephone, the RF power transmitted by the base station must be relatively large. To generate the power solid state RF power amplifiers are used. The heart of these amplifiers are high power RF transistors.

Generally four components are found in a high power transistor:

- The die.
  The die is the active part of the power transistor. On the die the low power levels at the input of the transistor are amplified to higher levels.

- The matching capacitor.
  Pre-match capacitors are used at the input of the transistor to transform, in combination with the bondwires, the impedance at the intrinsic transistor up to a higher value. Similarly postmatch capacitors are used at the output of the intrinsic transistor.

- The package.
  The prematch capacitor and the die are mounted in the package. The package forms the medium between these devices and its surroundings. Ceramic packages for bipolar power transistors are normally build up around a mounting base (a block of metal), a beryllium oxide ceramic (BeO) and a leadframe. A ceramic cap is placed on top of the package once the capacitor and die are mounted in the package to protect the components.

- Bonding wires.
  The bondwires connect the die, the package and the prematch capacitor together. The second function of the wires is to behave as an inductive element to transform, in combination with the capacitor, the low impedance of the die to higher values.

In the traditional way the procedure to make a new power transistor is by trial and error. An existing and proven design is modified and measured. Based on the measured results and
based on the knowledge of the designer the design is modified again and measured. This empirical process is repeated until the design meets the acceptance criteria. This approach has a few drawbacks. First of all the time needed to develop a new device is determined by the number of trial and error iterations. Consequently, the number of iterations and the time required per iteration should be kept as low as possible to guarantee a short time to market.

It is also possible in the trial and error method to end up with a sub optimal solution. Additionally, the success of a design heavily depends on the intelligence and knowledge of the designer. If, for example, an experienced designer decides to work somewhere else, an immediate problem exists.

A good and feasible solution to these problems is the use of Computer Aided Design (CAD) tools. These tools aid both the experienced and the less experienced designer in the design of the power transistor. The ultimate goal being the "first time right" design of power transistors using only CAD tools.

A major problem is the non-existence of electrical models and thermal models of the components found in power transistors. Although it is possible to fit models found in every commercially available microwave simulator to measured behaviour, this approach leaves too much room for error and misinterpretation. Additionally, it is rather difficult to optimize for example the shape bondwires for a better performance of the transistor. Consequently, physical models in the simulator of the bondwires, the capacitor, the package and the die are highly desired.

The principle aim of this work is to develop a consistent modelling strategy and to implement models required. The modelling work is applied to a particular transistor: the BLV 910. This transistor is a single silicon die transistor, able to produce around 10 Watts of RF power at 900 MHz in class AB with 800 mW of input power.

Modelling of bondwires

In the practical design of power transistors the shape of the bondwires is one of the few parameters a designer can change to optimize the transistor performance. This means that the modelling of the bondwires is of great importance. The modelling discussed in this work is based on Neumann's inductance equation. This approach facilitates a physical model where the shape of a bondwire is represented by a number of straight segments. The model implemented into MDS calculates within a reasonable amount of time the self and mutual inductance between bondwires.

In this work the model has been tested on basic structures such as single and coupled bondwires. Differences in inductance between model and measurement on the order of 5-10 percent are observed. In another work the model is tested on more intricate structures with good results [60].

Although the implemented model is adequate, the following recommendations are given:

- Modelling of capacitive effects. The present model accounts for inductive effects only and inclusion of capacitive couplings should increase the capabilities of the model.
- Modelling of mutual resistances. For reasons of simplicity analytic equations are used to model resistive losses in the wires in the present model. If wires are placed closely
together, mutual resistances come into play. Although difficult to model correctly, the inclusion of this effect into the model significantly improves the model.

- At higher frequencies the effect of radiation may become important. A rigourous investigation is strongly recommended.

Modelling of prematch capacitors

In the modelling applied in this work the prematch capacitors are treated as transmission lines with quasi-TEM wave propagation along the length of the capacitor. Rigorous electromagnetic simulations indicate significant skin effect currents in the highly conducting substrate. The model implemented for the prematch capacitor includes the dominant skin effect behaviour of the substrate. For completeness the following recommendations are given:

- Modelling of three dimensional current spreading. The model includes transmission line behaviour only, three dimensional effects are ignored. The modelling of three dimensional effects becomes important for capacitors where the width of the MOS contact is roughly the same as the length of the contact.

- Modelling of the ohmic contact. In this work modelling focussed on the MOS contact, assuming that the ohmic contact is lossless. An advanced compact model should include the effect of this ohmic contact.

- Experimental verification of the model. The prematch capacitor model is compared with electromagnetic simulations in HFSS showing reasonable to good results. The modelling of the skin effect behaviour in the substrate lacks, however, an experimental basis. Providing such a basis should contribute significantly to understanding of the substrate behaviour.

Modelling of the package

The package modelling discussed in this work makes use of the electromagnetic packages EM of Sonnet and Agilent's Momentum. In both packages a (multi-)layered substrate is defined and on the interfaces between these layers metallisation is defined. External ports and internal ports where capacitor, bondwires and die may be attached are defined. Both packages calculate the currents on the metallisation and generate scattering parameter datasets. The metallisation is considered infinitely thin, the thickness being ignored. The generated datasets seem reliable. Nonetheless, the following recommendations should be considered:

- Inclusion of three dimensional effects. The software packages used (Sonnet's Em and Agilent's Momentum) do not include the metallisation thickness. In the package of the BLV 910 the thickness of the leadframe is significant (≈ 100 μm). The influence of the thickness must be included in the analysis. Although a FEM package such as HFSS is capable of including this thickness, it appears to be impossible to define the required internal ports.

- Assessment of material constants. Throughout the simulations, the values for the relative dielectric constant found in the literature are used. An assessment of these constants, including the conductivity of the metal leadframe would contribute to the validity of the modelling.
- Measurement of multiport scattering parameters. At present the only reliable way to generate the multiport model including internal ports is through simulations. A thorough research programme should be defined for the development of a microwave measurement strategy for packages including the internal ports.

**Modelling of the die**

This thesis deals mainly with the modelling of the passive elements of the power transistor, an in-depth treatment of the modelling of the die will be given in the work of Roberto Tinti [31].

In the modelling of the BLV 910 the Mextram compact transistor model is used. Modelling of both DC and AC small- and large signal behaviour has proven successful. It is concluded that the inclusion in the modelling of thermal effects is a prerequisite for successful power transistor modelling. The thermal effects are included through the use of a thermal node in the compact model and isothermal parameter extraction. The following recommendations for the modelling of the die are given:

- Inclusion of a temperature coefficient in the emitter resistor in the compact model. In silicon power transistors an emitter ballasting resistor is added to reduce thermal runaway effects. The resistance value changes as function of temperature and this effect should be included in the modelling. Also an investigation into the emitter resistor should reveal how much of the contact resistance contributes to the total emitter resistance.
- Although not shown in this work, there are still significant difficulties in the simultaneous DC fitting and AC fitting during parameter extraction. To obtain a good DC fit, an error is introduced in the AC fit. Vice versa to obtain a good AC fit an error in the DC curves is found.
- Parameter extraction of small transistor active areas. Parameter extraction for the BLV 910 was performed on the smallest elementary cell available: a single cell. To study scaling rules the parameter extraction should be performed on a set of smaller transistors.
- Location and shape of the heat generating area. Heat is generated in the active areas of the die. In the modelling the heat generating area is located on the top of the silicon substrate. In practice this area is located just below the surface. Additionally, the location and the exact heat generation distribution depend heavily on the biasing of the transistor. A study should be made of the location and the distribution of the heat generation. Device simulations add substantially to such a study.

**Electro-thermal modelling**

For the electro-thermal modelling three essential ingredients proved necessary:

1. A thermal node has been added to the Mextram compact transistor model. The current flowing out of the port represents the power dissipated in the transistor. This current is injected into the thermal model and the voltage at the thermal node then represents temperature.
2. A thermal model. The thermal model implemented is a physical model i.e. physical parameters such as thermal conductivity and dimensions form the input for the model.
3. Kirchhoff's transformation. The thermal conductivity of the materials involved decreases with increasing temperature. To account for this, Kirchhoff's transformation is used.

The implemented thermal model computes the thermal resistance matrix of heat volumes in a block of heat conducting material. In power transistors the heat is generated in the junction area of the transistor. It is rather difficult to include the exact location and the distribution of the heat generation in the modelling. Therefore it was decided to place the heat areas on the top surface of the silicon. Consequently, the temperature used throughout the simulations is the maximum temperature. The electro-thermal modelling applied in this work has proven very successful. The following recommendation's for future work are given:

- Assessment of the location and distribution of the heat generation. In the modelling, the heat generation is assumed to take place on the top surface of the die. The exact location and distribution can be assessed using device simulations. This requires the availability of device data.
- Inclusion in the modelling of location and distribution of heat generation. As stated before these effects are not included in the model. Once the location and distribution of the heat generation are assessed, the models need to be adjusted to include this effect.
- Inclusion of heat transport through metallisation and bondwires. At present heat conduction is assumed through the die and package only. The effect of heat conduction through the metallisation pattern of the die and heat conduction through the bondwires is not accounted for. Although these effects are assumed quite small, they should be included in the model for reasons of completeness.
- Establishing a relation between the measured thermal impedance and the temperature distribution. Within the simulator a relation can be established between the measured thermal impedance, measured using electro-thermal measurements, and the temperature distribution. This relation should be experimentally verified and, where needed, be adjusted.

Modelling and measurement of power transistors

The above modelling approach is applied to the modelling of the BLV 910. Electrical models for the bondwires, prematch capacitor, die and the thermal models for die and package are all properly connected together. The resulting model is able to predict the DC behaviour of the power transistor quite accurately. Even at high dissipation levels and high voltages the DC behaviour is correctly predicted.

The small signal S-parameter behaviour is predicted very well up to 2 GHz at various biasing points. At higher frequencies significant differences are observed.

Finally, the model is well suited to predict the large signal behaviour of the BLV 910. Gain, efficiency and output impedance are found with small error. The input impedance is, however, not predicted correctly.

Based on the practical experience to date various recommendations are given.

- Investigation into differences in input impedance. As stated above significant differences are found in the input impedance. An investigation should reveal the cause of this error.
- Testing of the modelling approach on larger transistors. Thus far the modelling approach is tested on the BLV 910. Relatively small distributed effects are found for this
transistor. To explore the modelling approach further larger transistors should be modelled. Perfect candidates are the BLV 920, a 20 Watt power transistor, and the BLV 950, a 150 Watt transistor. These transistors use dies similar to the die of the BLV 910 i.e. there is no need to repeat the parameter extraction for the Mextram compact transistor model. Especially in the BLV 950 all distributed effects in temperature, the package and the bondwire come into play.

- Testing of the modelling approach on distortion behaviour. The comparison thus far is limited to DC, small signal and large signal behaviour at the fundamental behaviour. The merits of the model should be further explored by investigating the PiPo curve on the second and third harmonic and intermodulation behaviour.

Based on the results of the BLV 910 it is concluded that the approach to model each component of a power transistor separately and to combine these models together has proven successful.
Bibliography


Appendix A

Extraction of transmission line parameters

Introduction

In various cases extraction of transmission line parameters is required. For example in modern high speed integrated circuits and printed circuit boards (PCB’s) the effects of the interconnecting lines must be accounted for. Another example is found in the characterisation of components. Transmission lines are used to connect the components to measurement probes and connectors. In figure A.1 a one-port and a two-port network are shown with interconnecting lines.

![Diagram of one-port and two-port networks with interconnecting lines.](image)

Figure A.1: A one-port network and a two-port network with interconnecting lines. To obtain the parameters of the networks, the results must be de-embedded for the lines.

The effect of these lines is removed by measuring each line separately and de-embedding the data of the network for the lines. This approach has two major drawbacks. The first drawback is that the effect of discontinuities in the measurement of lines disturb the de-embedding. An example of a discontinuity is the transition from a coplanar probe to a coplanar line. The second drawback is that the measurement of a number of lines, especially if the lines are equal except for the length, is tedious and time consuming. As an alternative the extraction of transmission line parameters from measured scattering parameters is considered, leaving the length as a scaling parameter.
The scattering parameters of a uniform transmission line are given by:

\[ S_{11} = S_{22} = \frac{(Z_0^2 - 1) \sinh(\gamma l)}{2Z_0 \cosh(\gamma l) + (Z_0^2 + 1) \sinh(\gamma l)} \]  \hspace{1cm} (A.1)

\[ S_{12} = S_{21} = \frac{2Z_0}{2Z_0 \cosh(\gamma l) + (Z_0^2 + 1) \sinh(\gamma l)} \]  \hspace{1cm} (A.2)

where \( Z_0 \) is the normalised transmission line impedance with respect to the terminating impedance. If the complex impedance \( Z_0 \) and the complex propagation constant \( \gamma \) are known, the scattering parameters of a line are calculable for any given length \( l \). In the following the modelling of a coplanar transmission line is considered. A top view drawing of a coplanar transmission line is shown in figure A.2.

![Diagram of a coplanar transmission line and its equivalent circuit model.](image)

Figure A.2: A coplanar transmission line (left) and the model for the measurement setup (right). The capacitor \( C_{pg} \) models the capacitance from the probe and the line end to ground.

In this drawing the line width \( W \) and line to ground spacing \( S \) are indicated. The total length \( L_T \) and the actual length of the transmission line \( l \) are also indicated in this figure. Coplanar probes are put on the left end and right end of the line and moved approximately 40 \( \mu \)m over the line. The equivalent model for the measured situation is shown in the same figure. Two probes to ground capacitors \( C_{pg} \) model the capacitance from probe to ground and the capacitance from the open end of the line to ground. The transmission line models the actual coplanar line with length \( l \). Initially the effect of the capacitors is neglected. The extraction of the transmission line parameters reduces to a two-tier process:

1. Conversion of the measured two-port scattering parameters to chain parameters.
2. Calculation of the transmission line parameters from the chain parameters.

Both steps are discussed in the following.
Conversion of S-parameters to ABCD-parameters

The conversion of scattering parameters to chain parameters is straightforward:

\[
\begin{bmatrix}
A & B \\
C & D
\end{bmatrix} = \begin{bmatrix}
\frac{(1 + S_{11})(1 - S_{22}) + S_{12}S_{21}}{2S_{21}} & \frac{Z}{2S_{21}}(1 + S_{11})(1 + S_{22}) - S_{12}S_{21} \\
\frac{(1 - S_{11})(1 - S_{22}) - S_{12}S_{21}}{2ZS_{21}} & \frac{2S_{21}}{2S_{21}}(1 - S_{11})(1 + S_{22}) + S_{12}S_{21}
\end{bmatrix}
\]

where \(Z\) denotes the port impedance. In principle \(S_{11}\) should equal \(S_{22}\) and \(S_{21}\) should equal \(S_{12}\) for a reciprocal line. In practice however this is not the case, impeding the extraction of transmission line parameters, specially at lower frequencies, seriously. The first possible solution is to use only \(S_{11}\) and \(S_{21}\) or only \(S_{22}\) and \(S_{12}\) for the computation of the chain parameters. A second solution is to define an average transmission coefficient \(S_T = (S_{21} + S_{12})/2\) and an average reflection coefficient \(S_R = (S_{11} + S_{22})/2\). These average coefficient are used to compute the chain parameters. These solutions are not used in the following, although they give comparable or better results.

Extraction of transmission line parameters

Two methods are discussed to compute the transmission line parameters from the chain parameters. It is noted that both methods give equal results if \(S_{11} = S_{22}\) and \(S_{21} = S_{12}\).

- **Method I:** in the first method the impedance and the propagation constant are extracted in two steps from the ABCD-parameters. First the propagation constant is extracted and then the impedance is extracted:

\[
\gamma = \frac{A \pm \sqrt{A^2 - 1}}{l} \quad Z_0 = \frac{B}{\sinh(\gamma)}
\]

The sign in the extraction is chosen to satisfy \(\Re(\gamma) \geq 0\) and \(\Im(\gamma) \geq 0\). The length of the line is denoted by \(l\).

- **Method II:** in the second method the propagation constant is extracted as in the previous method. The impedance is extracted from the B- and C-parameter:

\[
\gamma = \frac{A \pm \sqrt{A^2 - 1}}{l} \quad Z_0 = \sqrt{\frac{B}{C}}
\]

An example of the extraction of coplanar parameters

To demonstrate the above procedures, coplanar transmission lines with differing lengths have been fabricated in an industrial thin-film process. The width \(W\) and spacing \(S\) are both 50 \(\mu m\) to match the dimensions of the Cascade GSG 100 \(\mu m\) pitch (WPH-205-100) probes. The length \(L_T\) of the respective lines is 100, 200, 300, 400, 500, 1000, 2000, 3000, 4000 and 5000 \(\mu m\). The transmission line parameters are measured in the range of 45 MHz - 10 GHz using a HP8510B vector network analyser. The system is calibrated with Cascade’s LRM calibration procedure and calibration standards. First, the scattering parameters are converted to chain parameters. Next, the transmission line parameters are extracted using both method I and II, discussed previously. Initially the effect of the capacitor \(C_{pg}\) is neglected. Although not
shown, the extracted line parameters are noisy for line lengths up to 1 mm. This behaviour is found for the imaginary part of the impedance, the attenuation constant and the real part of the impedance at low frequencies. In figure A.3 the extracted line impedance at 5 GHz is plotted for different line lengths. The total line length $L_T$ (cf. figure A.2) is used in the extraction procedure.

![Graph showing impedance as function of line length for two methods](image)

Figure A.3: Measured real part of the characteristic impedance as function of line length for two different extraction methods.

It is observed that both methods tend to the same impedance for longer lengths and for smaller lengths there are some differences between the methods. More importantly it is observed that the extracted impedance depends on the line length, where a length independent impedance is expected. The length dependency can be due to an incorrect model assumption for the measurement situation or limited measurement accuracy.

To refine the modelling the effect of the capacitor $C_{pg}$ is not neglected any more. The extraction procedure is repeated after de-embedding both ports for a capacitance of 10 fF. This procedure is repeated with a capacitance of 15 fF. The length used in the extraction is set to $l$ in figure A.2. The results for the lines of 1 to 5 mm are shown in figure A.4. For a capacitance of 10 fF the extracted real part of the impedance is almost independent of the line length. For the 15 fF capacitance, again a length dependence is introduced.

**Conclusions and recommendations**

The extraction of transmission line parameters from measured scattering parameters has been considered. It is shown that the extraction of the line impedance depends on the choice of chain parameters used. This dependency is due to $S_{11}$ not being equal to $S_{22}$ and $S_{21}$ not being equal to $S_{12}$.

Line lengths less than 1 mm should not be used for extraction of transmission line parameters. It is further shown that the extracted impedance depends on the line length if the transition from probe to line is not modelled.
Figure A.4: Measured real part of the characteristic impedance as function of line length. Results on the left are de-embedded for a capacitance of 10 fF and the results on the right are de-embedded for a 15 fF capacitance.
## Appendix B

### Mextram parameters

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Table B.1: Mextram parameters of one active area of the BLV 910 die. There are 8 active areas on the BLV 910 die.
Summary

In recent years wireless mobile communication has emerged as a mass communication medium. Wireless mobile communication is in essence a bidirectional link between a mobile telephone on the one hand and a base station on the other. In base stations, power amplifiers are found that amplify the transmitted signals to power levels of a few Watts and possibly up to over 100 Watts. Power transistors are used to construct power amplifiers. The power transistors are normally built using a package, matching capacitors, dies consisting of multi-call active devices and bondwires.

In the design of the dies, device simulation and analysis tools are used extensively. In the design of power transistors, however, trial and error methods are often applied due to a lack of electrical models for the bondwires, package and matching capacitors. Furthermore, power transistors dissipate substantial amounts of power and, as a consequence power transistors heat up significantly affecting the electrical behaviour due to the electro-thermal effect. Therefore there is a clear need for an electrical, a thermal model and an electro-thermal model for RF high power transistors.

In this work the segmentation approach is applied to modelling power transistors: first, models are derived and tested using measurement or rigorous simulation for the separate components. These models are connected together to form the full model for the power transistor. This approach is applied both to the electrical modelling and the thermal modelling. All models are implemented in the commercially available microwave simulator Microwave Design System (MDS) of Agilent Technologies. The models may also be used in the modelling of, for example, mutual inductances between bondwires in plastic packages or in the modelling of the thermal behaviour in integrated circuits.

By implementing the models in MDS, the full electrothermal simulation of power transistors under DC, RF small signal and RF large signal conditions is now possible.

As a demonstrator the modelling approach is applied to the Philips BLV 910 power transistor. This transistor is designed to deliver 10 Watts of RF power around 900 MHz. The results clearly demonstrate that the model accurately represents the DC behaviour and the small signal scattering parameters. Most important of all, the model also predicts very accurately the RF large signal parameters such as gain, efficiency and output power.
Samenvatting

In de afgelopen jaren is het gebruik van mobiele communicatie enorm gestegen. Deze mobiele communicatie komt tot stand door middel van een draadloze verbinding tussen de mobiele telefoon aan de ene kant en een basis station aan de andere kant. In de basis stations worden vermogensversterkers gebruikt om het uit te zenden signaal te versterken naar vermogensniveaus van een paar Watt en mogelijk meer dan 100 Watt.

In de vermogensversterkers worden vermogenstransistoren gebruikt. Deze transistoren zijn opgebouwd uit een behuizing, matching capaciteiten, actieve "die's" en bonddraden. De actieve "die's" vormen de "intrinsic transistor" waar de vermogensversterking plaats vindt. Bij het ontwerpen van de actieve die's wordt veelvuldig gebruik gemaakt van simulatie en analyse programmatuur. Bij het ontwerpen van de vermogenstransistoren wordt echter nog veel gebruik gemaakt van het 'trial and error' principe door een gebrek aan elektrische modellen voor de bonddraden, package en matching capaciteiten.

Vermogenstransistoren dissiperen een aanzienlijke hoeveelheid vermogen waardoor de vermogenstransistoren opwarmen en het elektrische gedrag verandert. Er is dus een grote behoefte aan een elektrisch, een thermisch model en een electro-thermisch model voor "Radio Frequency" (RF) vermogenstransistoren.

In dit proefschrift wordt de segmentatie aanpak gebruikt om vermogenstransistoren te modelleren: eerst worden modellen gemaakt van de afzonderlijke componenten en daarna worden deze modellen met elkaar verbonden om zodoende het totale model van een vermogenstransistor te verkrijgen. Deze aanpak wordt gebruikt voor zowel de elektrische modellering als ook voor de thermische modellering. Alle modellen zijn geïmplementeerd in het commercieel verkrijgbare microgolf analyse pakket Microwave Design System van Agilent Technologies. Door de modellen te implementeren in MDS is het mogelijk geworden om een volledige electrothermische analyse te maken van vermogenstransistoren onder DC, RF klein signaal en RF groot signaal condities. De modellen kunnen overigens ook gebruikt worden om de mutuele koppelingen tussen bonddraden in plastic behuizingen uit te rekenen of om het thermische gedrag van geïntegreerde circuits uit te rekenen.

Om de modelleringsaanpak te demonstreren is deze toegepast op een bestaande transistor: de BLV 910 van Philips Semiconductors. Deze transistor kan 10 Watt aan RF vermogen maken rond 900 Mhz. De resultaten laten duidelijk zien dat het geïmplementeerde model in staat is om nauwkeuring het DC gedrag en de klein signaal verstrooiings parameters te beschrijven. Als belangrijkste punt voorspelt het model ook de RF groot signaal parameters zoals versterking, efficiëntie en uitgangsvermogen.
Biography

Koen Mouthaan was born on June 22, 1967 in Voorburg, the Netherlands. He spent his wonder years in Geldrop from 1967 until 1979. From 1979 to 1987 he lived in Blaricum, the Netherlands, where he devoted a substantial amount of his time to pirate radio. He fulfilled military service from 1987 to 1988. In 1988 he started studying Electrical Engineering at Delft University of Technology. His masters thesis dealt with the RF modelling of integrated circuit interconnections on lossy silicon. He received his Masters degree in 1993. In that same year he started his PhD study in the Microwave Components Group of Delft University of Technology. This study forms the basis for this thesis. In the beginning of 1999 he joined the Physics and Electronics Laboratory of the Netherlands Organisation for Applied Scientific Research (TNO-FEL). His main task became business development with emphasis on microwave electronics. At the end of 2000 he joined the startup company Skygate B.V., Amsterdam, where he manages the design, development and procurement of microwave semiconductor products for Skygate.
Acknowledgements

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Photography
Photo in figure 1.3 (left): courtesy of Motorola, USA.
Photo in figure 1.5: courtesy of Philips Semiconductors, Nijmegen.
Photos in figures 1.3 (right) and figure 1.4: courtesy of Ted Johansson, Ericsson, Sweden.
Photos in figures 1.1, 1.8 and 2.1 by: Ili Kudus Photography, www.kudus.com
All other photos by: Koen Mouthaan.
Photo front cover: BLV 910 die after thermal runaway.