733 (12) 3455

30605/2

TR 3454

GALVANIC ETCHING OF SILICON

for fabrication of micromechanical structures

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for fabrication of micromechanical structures

PROEFSCHRIFT

ter verkrijging van de graad van doctor
aan de Technische Universiteit Delft,
op gezag van de Rector Magnificus prof.ir. K.F. Wakker,
in het openbaar te verdedigen ten overstaan van een commissie,
door het College voor Promoties aangewezen,

op maandag 10 januari 2000 te 13:30 uur

door

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University of Southampton

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Published and distributed by:

Delft University Press

P.O. Box 98

2600 MG Delft

The Netherlands

Telephone: +31 15 2783254

Telefax: +31 15 2781661

E-mail: DUP@DUP.TUDelft.NL

ISBN 90-407-2001-0

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Printed in The Netherlands

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Introduction

1

1.1 Silicon micromachining

Silicon microelectromechanical systems (MEMS) have become increasingly important in the last decades. Integration of the micromechanical structures with electronics (smart systems) has been successfully implemented to improve the performance and reduce the cost. The non-standard processing steps required for the formation of the micromechanical structures are performed after the standard IC-process for the electronics. In principle, this allows for high volume production of MEMS. Silicon is mainly used as the substrate material, since it has the most mature technology. Furthermore, it has excellent mechanical properties [Petersen, 1982]. The bulk-micromachined pressure sensor and accelerometer are perhaps two of the most successful and well-known examples of MEMS.

The term micromachining generally refers to fabrication of micromechanical structures on or in a substrate. When structures are formed on the substrate the process is called surface micromachining. Surface micromachining makes use of two types of layers; the sacrificial layer and the mechanical layer. A commonly used combination is an oxide

sacrificial layer which is deposited and patterned, followed by formation of a polysilicon mechanical layer. Once the mechanical layer has been patterned, the sacrificial layer is removed by a selective etch process. The mechanical structures can be made quite small and may consist of several layers. The most impressive example of a multilevel polysilicon surface micromachining process (with as many as five structural layers) was presented by Rodgers [Rodgers, 1999]. Based on this process, he made a highly complex microelectromechanical and optical system. Usually, the mechanical structures need to be planar, which implies that a good stress control of the layers is mandatory. Generally, a problem with surface micromachining is sticking of the freestanding structures to the substrate which may occur during processing or in use [Tas, 1996].

When structures are formed in the substrate, i.e. when it is sculptured to a final shape, the process is referred to as bulk micromachining. Two classes of silicon etching techniques are available, i.e. dry and wet etching. Usually, dry etching is carried out in a plasma reactor. Many different processes are available ranging from isotropic to anisotropic etches. Recently, deep reactive ion etchers have become available. Using these reactors, it is possible to etch through the entire wafer to yield structures which resemble surface micromachined structures but are typically much larger. It is possible to use reactive vapours and gases to etch silicon chemically without a plasma. As the plasma etch reactors are rather complex and expensive this offers an attractive alternative. These processes have the advantage of being highly selective to CMOS passivation layers. However, because of the chemical nature etching is isotropic which results in significant undercutting.

Wet etching is also widely used for bulk micromachining. Many different etchants are available both isotropic and anisotropic. The main advantage compared to plasma etching techniques is the cost efficiency. Much research has been devoted to the development of new etching systems with high etch rate, high selectivity and a high anisotropy. Recent examples of such systems are the alkaline tetramethyl ammonium hydroxide (TMAH) etchant (see Chapter 2) and the formation of high aspect ratio macropores in n-type Si in hydrofluoric acid (HF) solutions (see Chapter 3).

Usually, the dimensions of the microstructures must be highly uniform and reproducible. To achieve this, some sort of etch stop is required. Considerable attention has been paid to the development of reliable and accurate etch-stop techniques. Today, probably the most useful approach is the electrochemically controlled pn etch stop. However, there are still

some disadvantages with this method; a potential must be applied to the wafer using a power source and a wafer holder is usually required. Leakage, stress and handling are common problems with wafer holders. Generally, etching techniques which do not require external contacts are more easily implemented for batch fabrication and thus more cost efficient. In this thesis, we present alternative contactless etching techniques which do not involve an external power source. Etching is carried out in TMAH and HF solutions and used for the manufacturing of micromechanical membranes and cantilevers, trenches and porous layers. The techniques are described on the basis of silicon electrochemical etching which is treated in following chapters. A brief introduction to semiconductor etching mechanisms is given in the following subsection.

1.2 Semiconductor etching mechanisms

While this section gives a brief overview, a detailed treatment of semiconductor electrochemistry can be found in: [Bressers, 1995], [Kelly, 1998], [Kooij, 1997], [Morrison, 1980], [Notten, 1991]. The concept of a Fermi level in a solution which contains a redox couple is important for the understanding of semiconductor electrochemistry. The Fermi level is given by:

$$E_{F,redox} = -qV_{ox/red} \quad (1-1)$$

where $V_{ox/red}$ is the redox or Nernst potential of the redox couple:

with respect to the normal hydrogen electrode (NHE). Ox^{n+} represents the oxidizing agent, i.e. a species which can accept electrons. Red represents the reducing agent, i.e. a species which can donate electrons. An example of a redox system is the Fe^{3+}/Fe^{2+} couple. $V_{ox/red}$ is the equilibrium potential of an inert electrode (e.g. platinum) in a solution of the redox couple; the redox potential is measured with respect to a reference electrode, such as the saturated calomel electrode (SCE). At a potential more positive than $V_{ox/red}$ the reduced form of the redox couple (Red) is oxidized:

while at potentials more negative than $V_{\text{ox/red}}$, the oxidized form is reduced:

The standard redox potential of the $\text{Fe}^{3+}/\text{Fe}^{2+}$ system (the potential measured under standard conditions, i.e. at 298 K and 1 atm. and Ox^{n+} and Red concentrations of 1 mol/l) is 0.55 V with respect to SCE [Bard, 1985].

The donor and acceptor states of the redox system are described by two Gaussian distribution functions which intersect at the Fermi level. This is shown in Figure 1-1 where D_{ox} is the density of states of the oxidized form of the redox couple (the electron acceptor) and D_{red} is the density of states of the reduced form (the electron donor).

Fig. 1-1 *Energy diagram of a semiconductor and a solution containing a redox couple before (left) and after (right) contact.*

The energy band diagram of a semiconductor before contact with the solution is also shown in this Figure. When the semiconductor is brought into contact with the solution, equilibrium is established and the Fermi levels align. This is accomplished by a charge exchange and accompanied by bending of the energy bands; i.e. formation of a space charge layer in the semiconductor. When a voltage is applied, the system is no longer in equilibrium and a net current flows. With an inert semiconductor, this is

caused by the oxidation of a reduced species or the reduction of an oxidized species from solution. Depending on the system and the sign of the applied voltage, the following reactions may occur:

The key factor which determines whether a reaction will occur is the overlap between the filled or empty states of the redox couple and the conduction or valence band of the semiconductor; electrons transfer occurs isoenergetically. For the case shown in Figure 1-1, the oxidized species may be reduced by capturing an electron from the conduction band (equation 1-5) since the overlap between D_{ox} and the band is favourable. It cannot inject a hole (reaction 1-7) since the overlap between D_{ox} and the valence band is poor. There is a limited overlap between D_{red} and the conduction band, but no overlap with the valence band. Obviously, equilibrium involves electron exchange between the redox system and the conduction band (reactions 1-5 and 1-6). The rate of reaction 1-5 depends on:

- *the overlap between the filled states in the conduction band and empty states in the solution. Generally, this is independent of the applied voltage.*
- *the surface concentration of electrons, which is exponentially dependent on the band bending and thus the applied voltage.*

The rate of reaction 1-6 depends only on the overlap between D_{red} and the conduction band and is thus independent of the potential.

From this discussion, a rectifying current-potential characteristic is expected; for negative bias, a large cathodic current is measured as a result of reaction 1-5, while for positive bias a low anodic current is present (reaction 1-6).

In the example treated above, the semiconductor is considered to be inert. Under positive bias, solution species can be oxidized (reactions 1-6 and 1-8). However, many semiconductors, including Si, are not stable in aqueous solution. At positive potentials, the semiconductor itself may be oxidized and dissolve. The current-potential characteristics are similar to those for the oxidation of a solution species.

Generally, etching of a semiconductor is accomplished by removal of valence electrons from surface bonds to release the surface atom into solution. There are three different ways to achieve this; anodic, electroless or chemical. Anodic and chemical etching of silicon are generally carried out in indifferent electrolytes, i.e. aqueous alkaline or acidic solutions without redox couple, while electroless etching is performed in solutions with a strong oxidizing agent.

1.2.1 Anodic etching

Bonding electrons at the surface can be removed via the bulk semiconductor when it forms the anode of an electrochemical cell. Since the bonding electrons constitute the valence band, this process is carried by free holes in the valence band. For example, the localization of two holes in a Si-Si surface bond is equivalent to breaking the bond. The rate of anodic etching is determined by the surface hole concentration. Consequently, dissolution generally occurs with a p-type semiconductor in the dark and an n-type semiconductor only under illumination. In Figure 1-2 schematic current-potential curves of a p-type and an n-type semiconductor are shown for dissolution in an aqueous solution without added redox system. The energy schemes at different potentials are also shown.

First, the p-type semiconductor in the dark is considered. At negative potentials (point A) the band bending results in a depletion of holes at the surface. Therefore, the semiconductor is not etched in this potential range. At potentials positive with respect to A, the band bending decreases until a potential is reached at which there is no space charge present in the solid (B). This is called the flatband potential. At more positive potentials, a hole accumulation layer is created at the surface.

Fig. 1-2 Schematic current-potential curves of p-type and n-type semiconductors, with and without illumination. The energy band diagrams correspond to the potentials indicated in the current-potential curves.

The holes are used in the dissolution reaction. For example, in the case of silicon this can be schematically represented by the reaction:

This is measured as an anodic current. The current is proportional to the etch rate through Faraday's law [Bard, 1980]:

$$v[\text{mol} \cdot \text{s}^{-1} \cdot \text{cm}^{-2}] = \frac{i}{nFA} \quad (1-10)$$

where v is the reaction rate, i is the current, n is the number of electrons per atom dissolved, F is the Faraday constant (the charge of one mole of electrons), and A is the area. The reaction rate and the current (through equation 1-10) are determined by the surface hole concentration, and are therefore exponentially dependent on the applied bias.

For n-type semiconductors, a cathodic current is measured at potentials negative with respect to the open-circuit potential. This is due to the reduction of water leading to hydrogen evolution, which may be described by the following reaction:

in alkaline solutions, and

in acidic solutions. This current is not observed for p-type semiconductors in the dark. We measure a cathodic current only with illumination, which indicates that the reaction proceeds via the conduction band. Apparently, D_{ox} only has a good overlap with the conduction band and the reaction may only proceed through reaction 1-5. Note that at the n-type electrode, the cathodic current depends on the voltage since the surface concentration of electrons is dependent on this parameter.

With the n-type electrode in the dark, at point C and D there is almost no current since holes are not available for the dissolution reaction. When the semiconductor is illuminated, electron-hole pairs are generated. At point C, most of the holes are lost by the relatively fast recombination processes. At point D, the electric field is sufficiently strong to separate electrons and holes. The holes are driven to the semiconductor/solution interface. There, they participate in the dissolution reaction, while the electrons are measured as an anodic current in the external circuit. At this point, the current is limited by the light intensity. At sufficiently high intensity, the current-potential curve of n-type electrode resembles that of the p-type electrode.

Examples of anodic etching include dissolution of GaAs in a solution of sulfuric acid (H_2SO_4) [Notten, 1991] and of silicon in hydrofluoric acid solutions, which is discussed in Chapter 3.

1.2.2 Electroless etching

As mentioned previously, an oxidizing agent in the solution may be reduced either via the conduction band according to equation 1-5 or via the valence band, according to equation 1-7 depending on the redox potential $V_{\text{ox/red}}$ (Figure 1-1). In reaction 1-7 the oxidizing agent extracts electrons from the valence band; i.e. it injects free holes into the valence band. With relatively strong oxidizing agents, which have a positive standard potential $V_{\text{ox/red}}^0$, reaction 1-7 is favoured over reaction 1-5. Such an oxidizing agent is added to the solution in the case of electroless etching. As in the case of anodic etching, the holes are used for breaking surface bonds and, like chemical etching, electroless etching occurs at open-circuit potential. The rate of hole injection must be equal to the rate at which holes are used to oxidize the semiconductor. Therefore, the kinetics of reduction of the oxidizing agent are important in this case. In Figure 1-3 a schematic current-potential curve is shown of a p-type semiconductor in a solution containing a strong oxidizing agent Ox^+ . The partial oxidation current of the semiconductor resembles the curve in Figure 1-2. The partial reduction current is a result of the reduction of Ox^+ . The reduction starts at $V_{\text{ox/red}}$. At negative potentials the current becomes independent of the potential. In this range the reduction reaction is limited by the diffusion of Ox^+ to the semiconductor surface. The total measured current is obtained by adding the partial oxidation and reduction currents. At the rest potential (B), the semiconductor is dissolved at a rate which is dependent on the reaction rate of the reduction reaction. At negative potentials (A), the injected holes are drawn from the surface and etching stops. The injected holes are now measured as a cathodic current in the external circuit.

Note that electroless etching of both p-type and n-type semiconductors with an oxidizing agent with a positive $V_{\text{ox/red}}^0$ is possible in the dark. If the standard redox potential is not very positive, the reaction will proceed via reaction (1-5). In this case, the semiconductor can be dissolved under illumination.

An example of electroless etching is the dissolution of silicon in a solution of hydrofluoric acid and nitric acid (HNO_3). This is briefly considered in Chapter 3.

Fig. 1-3 *Current-potential curves and energy schemes of a semiconductor electrode in a solution containing a strong oxidizing agent. The partial oxidation and reduction currents are added to obtain the total measured current.*

1.2.3 Chemical etching

In chemical etching, electrons are exchanged locally between the surface bond and an etching agent in solution in a synchronous mechanism. Since free charge carriers are not involved, the etch rate for this form of etching is generally not affected if the potential of the semiconductor is changed. The rate is dependent on the composition and the temperature of the solution. An example of chemical etching is the dissolution of GaAs in bromine solutions, in which bond breaking can be represented as [Notten, 1991]:

Etching of silicon in alkaline solutions is another example. This is considered in the next Chapter.

1.3 Galvanic element formation

As an introduction to galvanic etching of silicon, a brief summary of galvanic element formation is given in this section [Bard, 1980], [Moore, 1983]. A galvanic cell generally consists of a conducting solution (electrolyte) and two externally connected electrodes; the anode and cathode at which electrochemical reactions (reactions involving electrons) occur. The main difference between an electrolytic cell, used to measure current-potential curves described in the previous section, and a galvanic element is that in the latter the reactions at the anode and cathode occur spontaneously when the electrodes are connected; chemical energy is converted into electrical energy.

The electromotive force or emf is the potential difference between the two electrodes at equilibrium. If the electrodes are short circuited, an oxidizing agent Ox_1^+ (of the redox couple with the highest redox potential ($V_{ox/red:1}$) in the solution is reduced at the cathode:

while at the anode a reducing agent Red_2 (of another redox couple with a lower redox potential ($V_{ox/red:2} < V_{ox/red:1}$) is oxidized:

Note that the anode has a negative potential, while in the case of an electrolytic cell it has a positive potential. A current flows from the cathode to the anode and the potential of the electrodes is shifted from the equilibrium Nernst potentials to a new value; the electrodes are polarized. The magnitude of this current is determined by the slowest

electrochemical reaction occurring at the two electrodes (reaction 1-13 or 1-14).

Galvanic element formation described in this thesis is related to galvanic corrosion as discussed by Fontana [Fontana, 1986]. When a metal is connected to a nobler metal, both immersed in the same solution, galvanic coupling may result in the enhanced corrosion of the less noble metal which forms the anode. An example is zinc in contact with platinum in an air-free acid solution. The galvanic coupling is schematically shown in Figure 1-4.

Fig. 1-4 Current-potential curves of zinc and platinum in air-free acid solution.

The zinc dissolution starts at $V_{Zn^{2+}/Zn}$. At potentials negative with respect to $V_{Zn^{2+}/Zn}$ a low cathodic current is measured at the zinc electrode; proton reduction on zinc is relatively slow. Proton reduction at the platinum electrode starts close to V_{H^+}/H_2 . Platinum acts as a catalyst for this reaction which results in a much larger reduction current than on zinc. When the two electrodes are in contact, the rest potential of the system assumes a value at which the anodic zinc dissolution and proton reduction currents are equal. The zinc corrosion rate is thus determined by the proton reduction rate at the platinum electrode. Other examples are given by Kelly [Kelly, 1975], [Kelly, 1978]. For various technological applications

(for example the production of thin film magnetic heads) the use of two or more stacks of different metal films is quite common. Galvanic interaction may result in enhanced dissolution of the least noble metal while the nobler metal is cathodically protected.

We observed similar effects when a platinum electrode was connected to a silicon electrode both immersed in a HF solution (see Chapter 5). In our case, all experiments were performed in solutions which were exposed to the air. The rate determining cathodic reaction is then oxygen reduction.

Anodic passivation may be used to prevent corrosion [Fontana, 1986]. Some metals (titanium and chromium) spontaneously passivate when their potential is shifted to values sufficiently positive with respect to the open-circuit potential; i.e. when they form the anode in a galvanic or electrolytic cell [Kelly, 1978]. We observed similar results when a sufficiently positive potential was applied to a silicon electrode either by an external power supply or through the formation of a galvanic element by connecting the Si to a gold sheet (see Chapter 4).

In the field of semiconductor micromachining little work has been reported on galvanic effects. In 1979 Hollan reported on possible galvanic effects between a noble metal and an etching GaAs surface [Hollan, 1979].

Notten reported on galvanic element formation between crystallographic planes with a different rest potential during etching of GaAs in an electroless system [Notten, 1987]. The etch rate of the plane with the most positive rest potential, i.e. the noblest plane, was decreased while that of less noble planes increased.

A recent report by Ivey describes galvanic element formation during cleaning of metallized III-V laser structures in 1% HF and concentrated H_3PO_4 solutions [Ivey, 1998]. The metal used was gold. Pinholes in the metal film led to galvanic dissolution of the underlying semiconductor layer. The problem was intensified by the large cathode/anode surface area ratio. This article was published at about the same time as Chapter 5 of this thesis and the results show a strong resemblance to the Si results. Both etching systems had an anodic dissolution mechanism. The main difference was the type of semiconductor used.

In contrast to the above mentioned reports on semiconductor galvanic etching, we go one step further by utilizing a galvanic effect, which is

normally avoided, for the fabrication of micromechanical systems (see Chapter 6).

1.4 Motivation and objectives

In 1996 French reported on a novel etch stop without applied bias in TMAH solutions [French, 1996]. This etch-stop technique combined all the advantages of existing methods. It was possible to make low-doped mechanical structures as with the conventional electrochemically controlled pn etch stop. It did not require external electrodes similar to the p+ etch stop. Moreover, an external power supply such as a strong light source as with the photovoltaic etch-stop technique was not needed. These properties made it a very promising alternative for batch fabrication of micromechanical structures. Initially, the mechanism was not clear. Therefore, the first goal of the project described in this thesis was to understand the operating principle and the limits of this technique. The next goal was to find out whether this technique could be applied to other etching systems such as hydrofluoric acid solutions. Compared to alkaline solutions, these are the second most important etchants for bulk micromachining. The final goal was to find out whether this technique could be used for the fabrication of micromechanical sensor systems such as pressure sensors and accelerometers.

1.5 Organization of this thesis

This thesis describes the operating principle of galvanic etching of silicon in TMAH and HF solutions, and its application to the formation of conventional micromechanical structures and sensors.

Chapter 2 describes bulk micromachining of silicon with alkaline etchants. The most important properties such as anisotropy, etch rate and surface morphology of commonly used alkaline etchants are reviewed. Finally, the main etching mechanisms and most important etch-stop techniques are discussed.

Chapter 3 describes bulk micromachining of silicon with hydrofluoric etchants. The basic dissolution mechanisms, i.e. anodic, electroless and light-assisted dissolution, are discussed, together with important features

such as porous silicon formation, electropolishing, isotropy, etch rate, porosity and doping concentration selectivity. The commonly used etch-stop techniques are reviewed and compared.

Chapter 4 treats galvanic etching in TMAH solutions. The principle of galvanic passivation in these solutions is explained. Next, galvanic element formation in the fabrication of crystalline silicon membranes and beams is described. The design rules for a successful implementation of the etch stop are given, together with some alternative solutions which allow for higher device package density on one wafer.

Chapter 5 discusses galvanic etching in HF solutions. The principle of galvanic element formation in these solutions together with its use to achieve an etch stop are explained. Finally, the design rules and limits of the etch stop are given.

Chapter 6 describes the application of the galvanic etch stop to the fabrication of a conventional pressure sensor in TMAH solutions. A front-side etch-stop process for the formation of a vibration sensor based on free-standing crystalline beams is presented. The fabrication of free-standing thick polysilicon structures with a galvanic etch stop in HF solutions is also discussed.

Finally, Chapter 7 presents the general conclusions of the research described in this thesis.

Bulk micromachining with alkaline solutions

2

In this chapter an overview is given of bulk micromachining of silicon with alkaline etchants for fabrication of integrated microelectromechanical systems. The basic electrochemical etching mechanisms of silicon are described. Finally, the most commonly used etch-stop techniques from the literature are reviewed and compared.

2.1 Chemical etching

Anisotropic wet etching of silicon is a commonly used bulk-micromachining technique for fabrication of micromechanical structures because of its relatively simple implementation and low costs. In most applications silicon is etched chemically without using an electrical power source. The reaction is given by [Allongue, 1993], [Bressers², 1995]:

The hydroxide ion does not appear explicitly in this reaction, but it is important since it catalyzes the reaction and ensures the solubility of the $\text{Si}(\text{OH})_4$ product. The etch rate depends on the temperature, etchant composition and the crystallographic orientation of the surface. Note that

since reaction (2-1) involves a chemical reaction, its rate is generally not affected when the potential of the semiconductor is changed by an external power source.

Anisotropy

All alkaline etchants etch silicon anisotropically, which means that the etch rate is dependent on the crystal orientation. The fastest etching plane is usually the (100)-plane, while the (111)-plane has the lowest etch rate. Dissolution is limited by the chemical reaction kinetics. For isotropic etchants dissolution is limited by diffusion of reacting species to the semiconductor. The anisotropy can be clearly observed from surface profiles. If a (100)-oriented Si wafer is patterned with an etch mask, the etch front is bounded by the (111)-planes. The final shape of the etched pit is a V-groove or an inverted pyramid. The sides are aligned to the (110)-planes independently of the initial shape of the etch mask. In Figure 2-1 this is shown.

Fig. 2-1 A SEM photo and schematic of the final shape of etched pits in (100)-silicon. Note that the initial shape of the etch mask is not a square. After some time in a TMAH solution at 80°C the etched shape is bounded by (111)-facets.

Because of the anisotropy, structures in (100)-oriented silicon are always limited in their smallest dimensions. The angle between the $\langle 100 \rangle$ and $\langle 111 \rangle$ direction is 54.74° . Therefore, an etched pit with depth A has a minimum width of $2A/\tan(54.74^\circ)$. This is shown in Figure 2-2.

Fig. 2-2 The minimum width of an etch mask required for an etched pit with depth A .

The low aspect ratio of the etched holes may be increased by using (110)-oriented silicon wafers. The limiting (111)-planes are perpendicular to the (110)-surface. Therefore, the angle between the sidewall of an etched pit and the surface is 90° [Kendall, 1979]. However, (110)-oriented wafers are not standard in today's IC processes and (100)-wafers are usually used for micromachining purposes.

There are many theories which try to explain the anisotropic etching of silicon (for example [Elwenspoek, 1993-1996], [Kendall, 1990], [Palik, 1985], [Seidel, 1990]) but the exact mechanism is still unclear. One theory explains the anisotropy in terms of the number of dangling bonds for different surface atoms. A (111) surface atom is bonded to three atoms in the crystal lattice and has only one dangling bond while a (100) surface atom is bonded to two atoms in the crystal and has two dangling bonds. Therefore, (100) surfaces are more reactive than (111) planes. This gives only a qualitative understanding of the anisotropic etching and cannot explain the anisotropy ratio of typically more than 100 [Bressers¹, 1995].

Convex structures

The anisotropic nature of the etching means that the formation of concave corners is quite straightforward. However, convex corners present complications. When free-standing structures such as the seismic mass of a bulk-micromachined accelerometer are made, the exposure of a convex corner is inevitable. At a convex corner many different crystal planes are

exposed to the etchant at the same time, resulting in considerable undercutting. For most micromachining applications, this is undesirable because it results in a badly defined shape (and mass). Different corner compensation masks have been realized to produce square corners (reported in for example: [Enoksson, 1997], [van Kampen, 1995], [Mayer, 1990]). The simplest structure consists of a beam oriented along the $\langle 100 \rangle$ -direction. The width of this beam should be twice the etched depth. The disadvantage is that the beam has to be rather long since it is undercut at the end at a considerable rate. The (411)-plane is the dominant plane causing the undercutting. More area-efficient structures have been designed, consisting of (110)- and (100)-oriented complex patterns.

Etch mask

The part of the wafer which is exposed to the solution is defined by an etch mask. The etchant should have a high selectivity (etch-rate ratio) towards the etch-mask material. Commonly used materials are silicon oxide and silicon nitride. Inert metals, i.e. gold, platinum, have also been used for this purpose [Petersen, 1982].

Commonly used etchants

The most commonly used etchants are solutions of ethylenediamine pyrocatechol (EDP) [Finne, 1967], hydrazine [Declercq, 1975], [Mehregany, 1988], KOH [Bean, 1978], [Kovacs, 1998], [Lee, 1969] and tetramethylammonium hydroxide (TMAH) [Merlos, 1993], [Tabata, 1992]. The first two are highly toxic and require special care during handling. They are less popular than the last two. The KOH-based etchant is non-toxic and has a relatively high etch rate and a high anisotropy ratio (anisotropy ratio is the (100)/(111) etch-rate ratio). However, it is not compatible with CMOS-processes due to mobile K^+ ion contamination. After etching, it is therefore impossible to perform thermal steps. In recent years, the TMAH etchant has received more interest since it is fully CMOS compatible. The tetramethylammonium ion is rather large and does not diffuse into the silicon lattice. An interesting feature is the possibility of passivating aluminum metallization by adding silicon or silicic acid [Sarro, 1998]. Another advantage over KOH solutions is the high selectivity towards silicon oxide. This means that relatively thin layers of silicon oxide can be used as an etch mask. TMAH solutions have a lower etch rate than KOH solutions (typically a factor of 2) and they also have a lower anisotropy ratio (typically a factor of 4). As a consequence, it is virtually impossible to produce well-defined convex corners with existing

corner compensation structures. An effective corner compensation structure is not possible because its dimensions tend to become too large for device applications. Furthermore, it is more expensive to dispose of organic solutions (such as TMAH) than non-organic solutions (such as KOH).

Etch rate of silicon and masking layers

In this thesis, TMAH solutions are mainly used. Hence, etch-rate data are only shown for this etchant. In Figure 2-3 the measured etch rate for different TMAH solutions at temperatures between 65°C and 95°C is shown [Sarro, 1998]. Note that a higher concentration results in a lower etch rate. A higher temperature results in a higher etch rate. The etch rate of a KOH solution with a typical concentration of 33% (50 g KOH for 100 ml water) at a typical etching temperature of 80°C is 120 $\mu\text{m/hr}$ [Kwa¹, 1995]. This is 4 times higher than the etch rate of a typical TMAH solution of 25% at the same temperature.

Fig. 2-3 The etch rate of (100)-oriented Si as a function of temperature and TMAH solution concentration (5% (a), 15% (b), 20% (c) and 25% (d)).

In Figure 2-4 the etch rate of different etch-mask layers (PECVD silicon oxide, PECVD silicon nitride, thermally grown silicon oxide and LPCVD silicon nitride) is shown [Sarro, 1998]. The trends are the same as for silicon etching; the lower the concentration, the higher the etch rate and a

higher temperature leads to a higher etch rate. Note that all layers have a very low etch rate and are therefore suitable as materials for etch masks. For comparison, thermally grown silicon oxide has an etch rate of 12 nm/hr in a 25% TMAH solution at 80°C and an etch rate of 1000 nm/hr in a 33% KOH solution at the same temperature [Kwa¹, 1995]. This demonstrates the high selectivity towards silicon oxide of TMAH solutions. The selectivity is 2500 for TMAH solutions and it is 120 for KOH solutions.

Fig. 2-4 The etch rate of different masking layers (PECVD oxide (a), PECVD silicon nitride (b), thermal oxide (c) and LPCVD silicon nitride (d)) as a function of temperature in a 5% and 25% TMAH solution. The solid curves are a guide to the eye.

Surface morphology

It is important for many sensor applications that the etching of the semiconductor results in a smooth surface [Kwa², 1995]. The surface morphology is dependent on the etching conditions. In Figure 2-5 two surfaces are shown, which were etched in different TMAH solutions. Solutions with a high concentration ($>20\%$) tend to result in a smoother finish than solutions with low concentration. Since high concentration also results in a lower etch rate, a trade-off between etch rate and surface roughness has to be made. For TMAH solutions the temperature proved to be unimportant for the surface morphology.

Fig. 2-5 SEM pictures of an etched surface in a 5% (a) and a 25% (b) TMAH solution at 80°C .

In Figure 2-5 it can be seen that the surface roughness consists of pyramidal hillocks. The exact mechanism of hillock formation is not clear. One theory is that hillocks are due to the formation of hydrogen gas. The bubbles adhere to the surface and thereby create local etch masks [Campbell, 1995]. Addition of oxygen to the solution was reported to reduce hillock formation because hydrogen reacted with oxygen to form water. Another theory attributes hillock formation to limited silicon deposition from silane (SiH_4) during the etching process. SiH_4 is only stable at low OH^- concentrations explaining the concentration dependence of the surface morphology [Bressers, 1996]. It was observed that etching under anodic polarization or with added oxidizing agents results in hillock suppression and a smooth surface. Since in this case the hydrogen

generation rate is unchanged, Bressers concluded that hillock formation cannot be due to hydrogen bubbles.

2.2 Electrochemical etching

The main etching mechanism for silicon in alkaline solutions is chemical. Etch-rate measurements with a Si anode in an electrochemical cell have shown that the additional anodic etch rate is small [Bressers², 1995]. The fact that the semiconductor passivates at sufficiently positive potentials is typical for electrochemical etching of Si in alkaline solutions. In this section this typical property is explained in more detail [Allongue, 1993], [Glembocki, 1985], [Palik, 1987]. In Figure 2-6 current-potential curves of p-type and n-type silicon electrodes in a 2 M potassium hydroxide (KOH) solution at room temperature are shown. For each electrode two scan directions are shown (indicated by the arrows).

Fig. 2-6 A current-potential curve of a p-type (a) and n-type (b) silicon electrode of 0.5 cm^2 in a 2M KOH solution at room temperature.

P-type silicon

Two typical potentials can be seen in Figure 2-6. The open-circuit potential (OCP) is the potential which a silicon electrode assumes when it is immersed in the KOH solution. The passivation potential (PP) is the

potential which corresponds to the peak current. The scan in Figure 2-6 starts at -2 V. At potentials negative with respect to the open-circuit potential the cathodic current is very low. In this range silicon is only dissolved chemically. The reaction is:

At the open-circuit potential the current is zero and the etching mechanism remains purely chemical. At potentials positive with respect to the open-circuit potential, an anodic current is measured which increases sharply until the passivation potential is reached. In this potential range, the silicon crystal is etched chemically and anodically. The overall etch rate in this range is only slightly higher than at open-circuit potential which proves that the chemical etching mechanism is dominant. The exact reaction mechanism in this potential range is unclear. The anodic dissolution reaction may proceed through the valence band according to the following reaction [Palik, 1983], [Michaud, 1998]:

This reaction seems rather unlikely since the anodic current starts 1 V negative with respect to the flat-band potential at which there is no bending of the silicon energy bands [Bressers², 1995]. The surface hole concentration at this potential would be too low for reaction (2-3) to proceed. It is more probable that the reaction proceeds through an electron injection mechanism as in the case of n-type silicon.

Up to the passivation potential the p-type silicon electrode has a current-potential curve which is typical for p-type semiconductors (see Chapter 1). At the passivation potential an anodic oxide layer is formed on the silicon, according to:

At potentials positive with respect to the passivation potential, the current drops to a low value. This is typical for silicon electrodes in alkaline etchants and deviates from current-potential curves in Chapter 1. In this range, chemical dissolution of the semiconductor stops because the etchant no longer has access to the Si-Si surface bonds. The current in the passive range is determined by the rate at which the oxide is chemically dissolved

by the solution. On the return scan to negative potentials, the current remains low since the anodic oxide is etched back rather slowly. To reactivate the surface and recommence chemical etching, the silicon electrode must be held at a negative potential for a sufficiently long time.

N-type silicon

In Figure 2-6 (b) a current-potential curve of an n-type silicon electrode in the dark is shown. The scan starts at negative potentials. Here, a large cathodic current is observed. This is due to the reduction of water. Since this current is not observed at p-type electrodes, the reaction must proceed through the conduction band:

The current-potential curve in the range positive with respect to the open-circuit potential resembles that of p-type Si. This is quite surprising and would not be expected from the theory described in Chapter 1.

As in the case of p-type silicon, in the potential range up to the passivation potential, the semiconductor is mainly etched chemically. The onset for the anodic current is negative with respect to that of p-type silicon. Since the concentration of holes in n-type silicon is very low the reaction cannot proceed via the valence band. The anodic current has been attributed to an electron injection from an activated intermediate of the chemical etching reaction [Bressers², 1995]. The intermediate injects an electron into the conduction band, thereby oxidizing the silicon surface. Similarly to p-type Si, at the passivation potential an anodic oxide layer grows on the silicon surface. The oxide layer for n-type electrodes is thinner than for p-type electrodes proving the importance of holes for this reaction. The passivation potential is at a more negative potential than that of p-type silicon. The current peak is somewhat broader and has a similar magnitude to that of p-type Si.

Electrochemical etching of Si is commonly used to induce an etch stop for fabrication of microstructures. This is considered in the next section.

2.3 Etch-stop techniques

As mentioned before, alkaline etchants are commonly used to make micromechanical structures such as pits (inverted pyramids), grooves, membranes and beams. Sometimes, the exact geometry of these structures is not critical or is simply defined by the anisotropy of the etching process (as with inverted pyramids and grooves). However, for many applications it is necessary to define the vertical dimensions with a high accuracy and uniformity. In this section, the most commonly used etch-stop techniques will be discussed. According to Collins, etch-stop techniques can be divided in two categories, i.e. intrinsic and extrinsic methods [Collins, 1997]. The intrinsic (also referred to as chemically limiting) techniques do not require an external power source. Extrinsic etch-stop techniques require some kind of external power source such as an electrical power supply or a light source. In this section, etch-stop techniques are categorized accordingly.

2.3.1 Intrinsic etch-stop techniques

(1) Timed etch stop

The simplest way to stop the etching is by taking the wafer out of the etching solution. The obvious problem associated with this method is the difficulty of accurately controlling the thickness. The etch rate in the solution should be known precisely and remain stable during a long time. However, the composition of the etchant changes in time since after each etch more Si is dissolved. For TMAH solutions, the resulting change in etch rate is quite large [Sarro, 1998]. Another drawback is that the initial thickness of the silicon wafers should be accurately measured before each etch. In order to have a batch process, only wafers of the same thickness can be etched in one batch. Furthermore, the etch rate might not be uniform throughout the whole wafer. This makes it impossible to make structures with a very small thickness.

(2) P+ etch stop

The etch rate of silicon is dopant independent over four orders of magnitude [Seidel, 1990]. However, silicon highly doped with boron etches very slowly. Generally, the doping concentration should be in excess of 10^{19} cm^{-3} , which is the concentration for the onset of degeneracy of the semiconductor, for a sufficiently low etch rate. With TMAH solutions the doping concentration needs to be even higher than 10^{20} cm^{-3}

which makes it less useful for these etchants [Steinsland, 1996]. Other acceptor ions such as gallium also reduce the etch rate [Senna, 1995], but boron is the most commonly used dopant since it has a high solubility in silicon. Even donor impurities such as phosphorus may be used to decrease the etch rate with a factor of 4 [Palik, 1982]. Because the reduction in etch rate is rather low it is not useful for micromachining applications. Hence, not much attention was given to the n+ etch stop.

Although many theories have been reported in the literature, the exact mechanism for the etch stop is still unclear and under debate. The most common theories are those of Palik and Seidel. Palik proposed that the high boron doping causes spontaneous formation of passivating oxide layers on the silicon [Palik, 1982]. However, they are not able to explain the reason for the oxide formation. Seidel suggested that the high hole concentration in the bulk of the p+-silicon is responsible for an interruption in the charge-exchange process at the silicon-solution interface [Seidel, 1990]. He claims that the chemical etching process is composed of two redox reactions which occur simultaneously. Silicon is oxidized through the injection of electrons in the conduction band. Reduction of hydrogen occurs by injection of the conduction band electrons back into the solution. Holes in the p+ material recombine with these electrons so that reduction of the hydrogen can no longer occur. The charge-exchange process is then interrupted and etching therefore stops. This model for chemical etching of silicon is implausible and cannot be understood with the theory presented in this thesis [Collins, 1997]. Furthermore, the etch-rate reduction with n-type silicon cannot be explained with this model.

The etch-rate reduction is observed with all alkaline etchants. The selectivity is greatest in EDP [Seidel, 1990]. This etch-stop technique allows the fabrication of real 3 dimensional structures and not just membranes [Weigold, 1998]. In Figure 2-7 an example of the etch stop is shown. In a first dry etch step, silicon is anisotropically etched. The etching is masked by a patterned metal film. Next, boron is diffused in the top layer. Then, the wafer is again dry etched, this time without a masking layer. Finally, the wafer is wet etched in a solution of EDP. In this solution, highly doped Si is not attacked while the undoped material is removed.

There are several disadvantages connected with this technique. It is rather difficult to obtain the required high boron concentration after a number of thermal process steps. Secondly, the high background doping makes it

impossible to fabricate electronic devices in these layers. Moreover, a high boron concentration introduces stress in the material which is usually undesirable when making fragile mechanical structures [Chu, 1993], [Ding, 1990], [Maseeh, 1990].

Fig. 2-7 The p^+ etch stop used for fabrication of free-standing resonator structures [Weigold, 1998].

(3) Etch stop with buried masking layers

Buried layers made of etch-mask materials can be used to obtain an etch stop. Materials which can be used are silicon oxide, silicon nitride and silicon carbide. There are several ways to fabricate these buried layers. One is to implant reactive ions, which react with the bulk silicon to form the buried etch-stop layer. For example, oxygen may be implanted to form silicon oxide, nitrogen to form silicon nitride [Peréz-Rodríguez, 1996] and carbon to form silicon carbide. Another approach is to grow an oxide layer on a silicon substrate. Next, a polysilicon layer is deposited and finally a thick polysilicon layer is grown in an epitaxial reactor [Gennissen, 1999]. It is also possible to use silicon-on-insulator (SOI) wafers for this purpose. Finally, epitaxial lateral overgrowth may be used to fabricate buried silicon oxide strips. The oxide strips should be spaced sufficiently close to allow stopping on the (111)-crystal planes [Bartek, 1995]. With these methods high doping levels are avoided. However, with the first method, the thickness of the structural layer is limited. With the second method, polysilicon is used which has less ideal mechanical and electrical properties than crystalline silicon. With the third method, the substrates used are rather expensive. And with the fourth method, the membranes are not uniform in thickness since V-grooves are formed between the oxide

strips. Finally, with this etch-stop technique only two-dimensional structures (membranes) can be made in a single etch step.

(4) Crystal damage etch stop

Silicon which has been implanted, but not properly annealed, fails to etch in anisotropic etchants [Collins, 1997], [Day, 1984]. The concentration of implanted ions may be much lower than in the p+ etch stop. The advantage of this technique is that Si or even electrons may be used for the implantation. After the etch stop, the wafers can be annealed which erases all traces of the etch stop. This etch stop can also be used in hydrofluoric acid based etchants [Lee, 1990].

Another crystal damage etch-stop technique is based on the preferential etching of silicon illuminated with a high-power Nd:YAG laser [Alavi, 1992]. The illuminated silicon crystal lattice is made amorphous and afterwards dissolved in an alkaline solution. Trenches and grooves are easily fabricated in this way, while free standing structures are impossible.

2.3.2 Extrinsic etch-stop techniques

The following techniques require external power from an electrical power supply or strong light source to stop the etching process. These techniques are all based on electrochemical passivation of silicon.

(1) Electrochemically controlled pn etch stop

This is one of the most commonly used methods to fabricate structures with a reproducible thickness, first proposed by Waggener [Waggener, 1970]. The structure normally used consists of a p-type silicon wafer with an n-type epi layer. The n-type layer is biased positive with respect to a platinum counter electrode in the solution. The electrical contact to the n-type epi-layer and metallization at the front of the wafer are protected from the etchant by a wafer holder. In Figure 2-8 the set-up is shown. The pn junction is reverse-biased. Because the alkaline solution is conducting and has a relatively low resistance, the p-type bulk floats at about the same potential as the solution. Most of the potential drop is across the depletion region of the pn junction. Since the p-type silicon is effectively isolated from the positive lead of the power supply it etches chemically. When the etch front reaches the pn junction it is destroyed locally. The remaining silicon layer is no longer isolated from the positive lead of the power supply.

Fig. 2-8 *The set-up for the pn etch-stop technique. A p-type wafer with an n-type epi-layer is mounted in a wafer holder. The n-type Si is biased positive with respect to a counter electrode. Etching of the p-type silicon stops at the pn junction.*

If the applied bias is sufficiently high and the silicon surface assumes a potential positive with respect to the passivation potential, an anodic current equal to the passivation current flows to the silicon/solution interface and an oxide layer grows on the surface. The remaining silicon is passivated and etching stops. A requirement for this etch-stop technique is that the pn junction is of good quality [Kloeck, 1989]. This means that the breakdown voltage should be high and the reverse-leakage current should be lower than the Si passivation current. If these requirements are not met, the p-type bulk will not start etching.

Some groups found that etching stops in the depletion layer, before the metallurgical junction [Huster, 1990], [Schmidt, 1994]. However, others found that the leakage current raises the potential of the remaining p-type layer and etching stops even before the depletion layer [Kloeck, 1989]. This has been attributed to a transistor action [Andrews, 1991]. The n-type silicon, p-type silicon and the etching solution form a npn-transistor. The thinning p-type region of the membrane acts as the floating base between a reverse-biased pn junction and a forward biased p-electrolyte junction. Any leakage current flowing through the p-base also influences the potential at the p-type bulk/electrolyte interface. This may then assume values positive with respect to the passivation potential and result in a premature etch stop. Other groups also describe the premature etch stopping in terms of a transistor [Lapadatu, 1998]. They claim that an npn-

transistor is formed by the n-type epi-layer, the p-type bulk and a shallow n⁺-degenerated layer which exists at the p-type/solution interface. Their etch-stop model agreed very well with the experimentally obtained results. Unfortunately, their model is only applicable to the four-electrode set-up (which is explained below).

Since the mechanism of the anodic reaction in p-type (and n-type) silicon is not exactly clear, it seems rather difficult to give any quantitative predictions about the thickness of the structures obtained. Therefore, only a qualitative explanation of the premature etch stop is given below. A bipolar effect may be expected, if we assume that the anodic current in p-type silicon is due to electron injection in the conduction band. As the etch front approaches the metallurgical junction at a distance equal to the diffusion length of minority carrier electrons, the reverse leakage current increases. When the reverse current is equal to the passivation current, etching stops. Since the passivation current density is relatively low, the exact location of the etch stop may be somewhat before the metallurgical junction. Depending on the quality of the junction and the doping concentrations, it can be inside the depletion layer or several microns before the depletion layer. For each configuration, this needs to be determined experimentally. The exact location of the etch stop is often not critical, as long as it remains reproducible and uniform.

With the set-up shown in Figure 2-8, the potentials of the electrodes are poorly defined and current dependent. Better potential control is obtained when a reference electrode is added to the configuration. The bias to the silicon electrode is then applied with respect to the reference electrode. To avoid the problem of premature etch stopping a four electrode set-up may be used [Kloeck, 1989]. The normally floating p-type substrate is biased at a well-defined potential. It was concluded that in this way etching stopped at the metallurgical junction irrespective of the depletion layer width (applied potentials) and leakage currents.

The two-electrode electrochemically controlled pn etch stop may also be used to fabricate freestanding structures [Muller, 1998], [Reay, 1994]. For example, a p-type wafer can be used as the substrate. A phosphorus diffusion defines the n-type structure to be underetched. Contact is only made to the n-type diffused layer at the front. With this technique, care has to be taken to protect the metallization during etching. A wafer holder which protects the front can obviously not be used. Usually, a protective PECVD oxide layer is deposited over the aluminum layer. An alternative

is to use gold or platinum for the metallization. This option will be considered in Chapter 6.

(2) Doping selective etching

This etch-stop technique is based on the difference in passivation potential between n-type and p-type silicon [Chen, 1995], [Linden, 1989]. The passivation potential of n-type silicon is slightly lower than that of p-type Si (see Figure 2-6). The same structure is used as with the conventional electrochemically controlled etch-stop technique. The electrical contact is made to the p-type bulk. The applied potential is carefully adjusted to a value in between the passivation potentials of n-type and p-type Si. Because the junction is forward biased n-type Si is at about the same potential as p-type Si. The quality of the junction and its reverse characteristics are not important for this technique. A disadvantage is that the applied potential should be carefully controlled. In reality, there is a small voltage drop over the forward-biased pn-junction which may change during the etching process. The applied potential should compensate for this voltage drop which proves to be difficult. If the difference between the two passivation potentials is low, as with TMAH solutions [Acero, 1995], this technique cannot be used.

(3) Electrochemically controlled np etch stop by pulsed anodization [Wang, 1992]

The electrochemically controlled etch stop is normally used with a p-type substrate and an n-type epi or diffused layer. With the present technique it is possible to use a p-type wafer with an n-type top-layer. As discussed in previous sections, when a silicon electrode is biased at a sufficiently high potential, an anodic oxide layer grows on the surface. With an equally high bias, the oxide layer formed on p-type silicon is thicker than that on n-type Si. Therefore, after a similar voltage pulse n-type silicon will commence etching sooner than p-type Si, since the oxide layer on n-type Si is etched back faster. The pulses are applied to the p-type epi-layer. The junction is forward biased, which results in a transmission of the voltage pulse to the n-type bulk. The frequency and duration of the pulses are carefully adjusted to make sure that p-type Si remains passivated while n-type Si etches. In this way, etching proceeds until the p-type layer is reached. The advantage of the technique is that it offers the possibility of stopping on p-type layers.

(4) Electrochemical metal-insulator-semiconductor etch-stop

With this technique a metal-insulator-semiconductor (MIS) structure is used to create an artificial pn-junction [Smith, 1993]. In Figure 2-9 the set-up is shown.

Fig. 2-9 The set-up for the MIS etch stop. The gate voltage V_G is used to create an n-type inversion layer, while the substrate voltage V_S is used to bias the inversion layer positive with respect to a counter electrode.

An oxide layer is grown on a p-type silicon wafer. Next, an aluminium metallization layer is evaporated on the oxide layer. At the back of the wafer a silicon oxide etch mask is patterned. At the edge of the p-type wafer, an n-type layer is created by diffusion. During etching the wafer is mounted in a wafer holder which exposes only the back to a KOH solution. The metal layer is biased with a voltage V_G with respect to the substrate. The substrate is held at a bias V_S with respect to a platinum counter electrode. In this way, the voltage V_G induces an n-type inversion layer by accumulation of electrons thereby creating an artificial pn-junction. Etching of the substrate proceeds until the depletion layer is reached. Then etching stops in a way similar to the electrochemically controlled pn etch stop. The electrical contact to the n-type diffused layer at the side is used to bias the inversion layer at a potential positive with respect to the passivation potential. It is not strictly necessary to use this n-type diffused layer. Contact may also be made directly to the p-type

substrate as with the doping selective etching technique. However, the bias should be carefully controlled to avoid passivation of the p-type substrate.

This technique has two main advantages over the conventional pn etch stop. First, the actual doping of the resulting membrane is also p-type making the process more flexible. Secondly, the thickness of the membrane can be easily controlled by the gate-substrate voltage V_G . A disadvantage of the technique is that when a direct contact to the p-type substrate is used (thus without the n-type diffusion at the edge of the wafer), a complete etch stop cannot be obtained. There is a sufficient etch-rate reduction of the MIS depletion layers to reproducibly control membrane thicknesses [Huster, 1993]. Another disadvantage is that it is impossible to make structures other than membranes with this method.

(5) Photovoltaic etch-stop technique [Peeters, 1994]

This etch-stop technique does not require external electrodes or wafer holders. An external power source in the form of a high intensity light source is needed. Etching stops on a p-type diffused or epi-layer. The set-up in its simplest form is illustrated in Figure 2-10.

Fig. 2-10 Device structure used for the photovoltaic etch-stop technique. The p-type layer is protected from the etchant by a nitride layer. The n-type substrate is contacted with a platinum film. When the etching stops the reactions indicated in the figure occur and a reverse current flows through the pn-junction.

An n-type silicon wafer with a p-type epi-layer is used. A platinum/titanium film is sputtered on the n-type back and patterned. The p-type epi-layer is protected from the solution by a silicon nitride layer. As etchant, a

KOH solution is used. The device is illuminated by a strong light source to ensure an etch stop at the epi layer. It was observed that the n-type silicon substrate and the platinum film interacted galvanically. In Chapter 4 we explain in more detail how a silicon-metal galvanic element may be formed.

During etching the wafer is illuminated with a strong light source which generates electron/hole pairs. In the bulk of the silicon these recombine while in the depletion layer these are separated by the electrical field. Holes driven into the p-type epi-layer cannot react as long as this layer is protected by the n-type bulk. Note that at the front the epi-layer is covered with a nitride layer. A photopotential develops and the photogenerated carriers are lost by recombination. Electron/hole pairs created in the n-type substrate will very likely also recombine; kinetics of surface reactions involving electrons and holes are slow compared to recombination kinetics. An anodic current flow, required for the passivation of silicon, is not present in the structure. The n-type substrate is therefore chemically etched. A galvanic effect due to oxygen reduction at the platinum might be expected. However, since the areas of n-Si and Pt exposed to the solution are comparable and the passivation current-density in KOH solutions is high, galvanic passivation of the n-type Si is unlikely. Once the p-type layer is exposed to the solution, photogenerated holes separated by the electric field of the depletion layer are free to react at the p-type semiconductor/solution interface. The silicon surface is oxidized. The photogenerated electrons can react at the n-type side walls or more likely at the platinum/solution interface, where hydrogen is generated. Now, there is an internal anodic photocurrent. If the photocurrent is sufficiently high, etching of the p-type epi-layer is prevented. There are two important requirements for the etch stop to work. First, there must be a high-power light source proving that an anodic photocurrent is essential. Second, there must be a sufficiently large platinum electrode. If this is not the case, the photocurrent will be limited by the reduction of water to hydrogen gas at the platinum/solution interface. The reduction of water at an n-type silicon interface is less efficient.

Besides p-type membranes freestanding structures such as beams [Strandman, 1998] and accelerometers [Lapadatu, 1996] are also possible with this method. This etch-stop technique has two main advantages. First, the fabricated structures are p-type which may be preferred in some applications. Second, the etch stop is contactless, making it easier to

implement in batch fabrication processes. However, the need for a strong light source still complicates the set-up.

(6) Galvanic etch stop

This etch stop is briefly discussed in this section. A detailed description is given in Chapter 4. Basically, the same structure is used as with the two-electrode pn etch stop (Figure 2-11).

Fig. 2-11 Device structure used for the galvanic etch stop. An n-type epi-layer on a p-type substrate is used. The n-type epilayer is contacted with a gold film. When the etching stops, the reactions indicated in the figure occur and a current flows through the epilayer.

The only non-standard step in the preparation of the structures is the deposition of a gold/chromium film. This film makes electrical contact only to the n-type silicon layer. An external power source or a wafer holder is not used with this technique [French, 1996]. This makes it rather an intrinsic etch stop. However, electrical power is used to stop the etching process, but the electrical power is generated within the structure itself. The gold/silicon couple forms a galvanic cell [Ashruf¹, 1998]. The difference in the rest potential of the two materials provides the driving electromotive force for the cell. The reduction of oxygen at the gold electrode generates the cell current. When the structure is immersed in the solution, the gold electrode and the p-type Si bulk are insulated by the reversed-biased pn junction. If the etch front reaches the pn-junction, the insulation is destroyed and the galvanic cell is formed. When a sufficiently large gold electrode is used, etching stops and an n-type membrane is

obtained. It is also possible to make three-dimensional structures such as beams with this technique [Ashruf¹, 1999]. The advantage of this technique is that external power sources and wafer holders are not required. This makes it easy to implement in batch fabrication. The disadvantage is that a relatively large gold electrode is required. This leaves little room on the chip for the actual device. However, there are ways to overcome this disadvantage, as will be discussed in Chapter 4.

2.3.3 Summary

In Table 1 the etch-stop techniques described in the previous section are compared. The following properties are listed:

- *Is there a need for a wafer holder?*
- *Is an external power source required? If so, should the contact be made to n-type or p-type Si?*
- *Is there mechanical stress in the etched structures due to high doping levels?*
- *Is the thickness of the structures controllable over a wide range?*
- *What is the doping type of the resulting mechanical structures?*

Table 2-1 Comparison of etch-stop techniques

Etch stop	Wafer holder?	External power source required?/ Contact to n-type or p-type?	Mechanical stress?	Thickness controllable?	Stop possible on p-type or n-type?
Timed	no	no	no	no	both
P+	no	no	yes	no	p
Buried masking layers	no	no	no	yes	both
Crystal damage	no	no	no	no	both
Electro-chemically controlled pn	yes	yes / n	no	yes	n
Doping selective	yes	yes / p	no	yes	n
Np by pulsed anodization	yes	yes / p	no	yes	p
Metal-insulator-semiconductor	yes	yes / both *	no	yes	p
Photovoltaic	no	yes / contactless	no	yes	p
Galvanic	no	no / contactless	no	yes	n

* Contact can be made to an n-type edge diffusion or directly to the p-type bulk.

From this Table it can be concluded that the galvanic etch stop is a promising alternative to existing techniques.

Bulk micromachining with hydrofluoric acid solutions

3

In this Chapter bulk micromachining in hydrofluoric acid (HF) solutions is discussed. We mainly concentrate on the use of HF solutions for the formation of micromechanical structures. Other important applications of silicon etching in HF solutions such as, for example, the fabrication of silicon-based light-emitting devices [Fauchet, 1995], [Hirschman, 1996], [Kaneko, 1993] are not considered. Etching is usually carried out in an electrochemical cell or in a solution containing a strong oxidizing agent. The charge exchange processes at the silicon/etching solution interface are briefly considered. Next, some practical aspects of the use of HF-based etchants are described. Finally, the most commonly used etch-stop techniques are reviewed and compared.

3.1 Electrochemical etching

Unlike in alkaline solutions, silicon is not etched chemically in hydrofluoric acid (HF) solutions. The main dissolution mechanism is anodic for which valence band holes are required. Hence, the reaction can be controlled by changing the surface hole concentration. Generally, this may be done in the following ways: with an electrochemical cell ((photo)anodic dissolution), by using an oxidizing agent (electroless or

“chemical” dissolution) or by high intensity illumination (open-circuit light-assisted dissolution).

3.1.1 Anodic dissolution

Silicon can be dissolved by making it the anode in an electrochemical cell. The silicon wafer with an ohmic contact at the back is mounted in a Teflon wafer holder. Usually, a two-electrode set-up is used with a platinum (Pt) counter electrode (shown in Figure 3-1).

Fig. 3-1 *A two-electrode electrochemical cell used for etching a silicon sample in an HF solution.*

For micromachining purposes, this set-up gives sufficient control over the etching process. The important process variables are the current density and the HF concentration. However, a better potential control is obtained with a three-electrode cell. Therefore, in the remainder of this chapter a three-electrode set-up with an Ag/AgCl reference electrode is considered. The standard redox potential of the Ag/AgCl reference electrode is 50 mV negative with respect to that of the calomel electrode.

In Figure 3-2 current-potential curves of silicon electrodes of 0.6 cm^2 (p-type in the dark and n-type in the dark and with weak illumination) are shown. Compared to alkaline solutions, there is a more pronounced difference with regard to the doping type of the Si. This difference may be explained with the theory presented in Chapter 1.

Fig. 3-2 Current-potential curves for silicon electrodes in a 1% HF solution. *p*-type Si was measured in the dark, while *n*-type Si was measured in the dark (a) and under low illumination (b).

p-type silicon

At potentials negative with respect to the open-circuit potential (0 V), a low cathodic current is observed. In this range the semiconductor is not dissolved. For the potential range more positive than 0 V, an anodic current is measured. At low over-potentials, this current is exponentially dependent on the applied bias. For the anodic dissolution reaction valence band holes are required. The reaction can be represented by:

Two valence band holes are required to oxidize each silicon atom, which goes into solution as a fluoride complex. One hydrogen molecule is produced for each silicon atom dissolved. The supply of holes to the silicon/solution interface is rate-limiting for the dissolution reaction. Silicon is only dissolved at certain reaction sites which are randomly distributed over the surface. This results in a microporous layer, with typical pore diameters and the interpore spacings between 1 and 5 nm. The layer consists of a highly interconnected and uniform pore network. When

the potential is scanned to more positive values, a current peak is observed. The corresponding potential is referred to as the peak potential. As in alkaline solutions, at the peak potential an oxide layer is grown on the silicon surface. The oxide layer is chemically dissolved in the HF solution. In this way, the silicon surface is etched uniformly; this process is called electropolishing [Smith, 1992]. In the potential range positive with respect to the peak potential, the hole concentration is rather high and the reaction is limited by the diffusion of hydrogen fluoride species to the silicon/solution interface.

n-type silicon

With n-type silicon a large cathodic current is found at potentials more negative than -0.7 V. This is due to the reduction of protons to hydrogen gas.

Since this current is not observed at p-type electrodes, the reaction must involve conduction band electrons. Because the anodic dissolution reaction requires valence band holes, n-type Si is not dissolved in the dark. As can be seen in Figure 3-2 (a), a low anodic current is measured in the dark. Note that the onset of the anodic current is negative with respect to that of p-type Si. With low illumination, a higher anodic current is measured due to generation of electron-hole pairs. The holes are consumed in the dissolution reaction 3-1, while the electrons are measured as an anodic photocurrent. The anodic current (and thus the etch rate) is proportional to the light intensity. If the light intensity is sufficiently high, the current-potential curve resembles that of p-type silicon. In this case, the reaction is no longer limited by the photogenerated holes. The pore diameters in n-type Si are considerably larger than in p-type Si and show a strong tendency to form straight channels.

Macroporous n-type silicon

Macroporous silicon consists of pores with a diameter larger than 50 nm. It is formed by illuminating from the back an n-type silicon sample at a potential close to the peak. Electron-hole pairs are only generated at the back of the sample as most of the light is absorbed in the first few microns. The holes diffuse or drift to the silicon/solution interface where they are consumed in the dissolution reaction. The reaction only proceeds at the pore tips because the strong electric field at the tip very effectively

captures the holes. By means of this technique, etched trenches and pores several hundreds of microns deep have been formed [Lehmann, 1993]. Figure 3-3 shows the setup.

Fig. 3-3 Set-up used for formation of macroporous silicon. The n-type silicon wafer is biased positively with respect to a platinum grid. The wafer is illuminated from the back. Initial pits are anisotropically etched in the wafer before the porous formation process to control the location of the pores.

Recently, it has been shown that these high-aspect ratio etched pores are also possible with low-doped p-type silicon without illumination [Ohji¹, 1999], [Wehrspohn, 1998]. A SEM picture of macroporous p-type silicon is shown in Figure 3-4.

Fig. 3-4 SEM photo of macroporous p-type silicon (from [Ohji¹, 1999]).

Pore formation vs. electropolishing

The critical current density at which the dissolution reaction becomes limited by the diffusion of HF species to the reacting surface is dependent on the HF concentration. At a higher HF concentration, the critical current density shifts to higher values. This is schematically displayed in Figure 3-5 [Zhang, 1989].

Fig. 3-5 *Plot of the logarithm of the current density versus the logarithm of the HF concentration. Above the critical current density silicon is uniformly etched, while below this value a porous layer is formed.*

Note that the critical current density is not a true function of the HF concentration. In the transition region between the electropolishing and porous ranges, the pores tend to have larger diameters. From this figure the conditions required for either pore formation or uniform etching are easily extracted. A low HF concentration and a high current density gives electropolishing, while a high HF concentration and a low current density gives pore formation. Both modes of etching are used to make micromechanical structures (see Chapter 6).

Etch mask

For HF solutions a highly resistant material such as LPCVD silicon nitride or a noble metal is required as an etch mask [Petersen, 1982]. The problem

with the latter is that, in highly concentrated solutions, underlying adhesion layers such as chromium or titanium may rapidly dissolve. This can be slowed down by depositing pinhole-free metal layers. Obviously, silicon oxide cannot be used as etch mask since it is chemically dissolved. A typical oxide etch rate in a 40% HF solution is $0.9 \mu\text{m}/\text{min}$ [Gennissen, 1999].

Isotropy

The pore formation process follows the lines of current flow. This results in undercutting at the edges of an etch mask as shown in Figure 3-6 [Bell, 1996]. Undercutting under electropolishing conditions is due to enhanced mass transport at the resist edge.

Fig. 3-6 *The etched surface follows the lines of current flow, resulting in undercutting of the etch mask.*

This property makes the use of HF solutions for micromachining applications in which precise lateral dimensioning is critical less favourable than alkaline solutions. However, etch-stop techniques may be used to limit the etching process to only one direction (see next sections). The large undercutting also allows for fabrication of relatively large micromechanical structures with a front-side etching process. Compared to alkaline solutions, in which etching is limited by the (111)-planes, the device package density may be increased.

Commonly used solutions

Commercially available solutions usually consist of mixtures of HF and water. Typical concentrations range from 1% to 40%. Recently, Gennissen proposed the use of higher concentrations ($\sim 73\%$) for release etching of

surface-micromachined structures with standard aluminium metallization. The etch rate of this metal is reduced by a factor of 30 compared to the etch rate in lower concentrations (40%), while the oxide etch rate is increased by a factor of 2 [Gennissen, 1999].

One of the reaction products of the silicon dissolution process is hydrogen gas (see reaction 3-1). When porous silicon is formed, the tips of the pores are active while the side walls are passive. Hydrogen gas which evolves at the tip may block the reacting surface from the HF solution, thereby inhibiting etching. A surfactant can be added to lower the surface tension of the solution. The hydrogen bubbles can then escape easily from the pores. Addition of these surfactants also changes the morphology of the resulting porous structure [O'Halloran, 1997]. Generally, in these solutions pore diameters and pore depths are more uniform. The etched surfaces also tend to be smoother. The most commonly used additives are ethanol and Triton X-100, which is a soap-based solution.

Other fluoride-based solutions are ammonium fluoride (NH_4F) and buffered HF (BHF), which is a mixture of HF, water and ammonium fluoride. These solutions are more selective with respect to resist than diluted HF solutions.

Etch (or porous silicon formation) rate

Etchants based on HF are usually used at room temperature. To characterize the etch rate there are two important figures.

- *The porous Si formation rate is defined as the thickness of the porous layer divided by the etch time. It is usually measured by dissolving the porous layer in a low concentration alkaline solution and making a scan of the surface profile. The step between a protected and unprotected part of the sample gives the thickness.*
- *The porosity is defined as the fraction of the etched volume taken up by voids. It is usually determined by a gravimetric technique. The weight of a sample is measured before (m_1) and after pore formation (m_2), and after dissolution of the entire porous layer (m_3). The porosity is calculated as $(m_1 - m_2)/(m_1 - m_3)$.*

The formation rate and the porosity are generally dependent on the HF concentration, the doping density of the silicon and the current density. As

an example, the dependence of these two parameters on the HF concentration and the current density are shown in Figure 3-7.

Fig. 3-7 The effect of HF concentration (a) and current density (b) on the porosity and formation rate of p-type silicon ($2-5 \Omega \text{ cm}$) [O'Halloran, 1999].

The formation rate is relatively independent of the HF concentration and linearly dependent on the current density; the number of moles of silicon dissolved is related to the current through Faraday's law (see Chapter 1). The porosity is relatively independent of the current density and inversely proportional to the HF concentration. The porosity and the surface morphology are important for applications where the porous silicon itself is used for its mechanical properties, such as for humidity sensing applications [O'Halloran, 1999]. In this thesis, porous silicon is used as a

sacrificial layer. Therefore, the only concern is that the porous layer is sufficiently thick so that the mechanical structures are undercut. The precise morphology or porosity is not critical.

Selectivity based on doping concentration

Generally, the current and thus the etch rate (see Chapter 1) are highly dependent on the silicon doping concentration. By varying the impurity concentration, selectivity can be obtained. In Figure 3-8 current-potential curves of silicon electrodes with different impurity concentrations are shown [Halimaoui, 1997]. The HF concentration is fixed at 30%.

Fig. 3-8 *Current-potential curves of silicon electrodes with different impurity concentrations.*

Formation of porous p-type Si starts at 0.05 V. Moderately doped n-type silicon in the dark cannot be made porous as discussed in section 3.1.1. Formation of highly doped p-type porous Si starts at negative potentials compared to moderately doped p-type Si as a result of the difference in surface hole concentration. Therefore, p+ Si is etched preferentially over p- Si. Highly doped n-type silicon ($>10^{18}\text{cm}^{-3}$) can be made porous in the dark by means of a breakdown mechanism [Lee, 1990]. If the applied bias is higher than the breakdown voltage of the semiconductor/solution junction a large current flows. Because of the very narrow space charge layer, valence band electrons tunnel through the bandgap to the conduction band, leaving behind holes at the surface of the semiconductor. These holes are used in the dissolution reaction at the silicon/solution interface while the electrons are measured as an anodic current. Note that the breakdown voltage decreases with increasing doping concentrations [Sze, 1981].

The relation between the etch rates at fixed potential is as follows: $n+ > p+ > p- \gg n-$ [Smith, 1992]. The difference in etch rate is commonly used for etch-stop techniques in HF solutions. These will be considered in following subsections.

3.1.2 Electroless dissolution

With this form of etching a strong oxidizing agent is added to the HF solution. The oxidizing agent is reduced and thereby injects holes into the valence band [Kooij, 1999]. This reaction can only occur if the oxidizing agent is sufficiently strong. In a following step the holes are consumed in the silicon dissolution reaction. Etching takes place under open-circuit conditions (i.e. an electrochemical cell is not used) and sometimes this form of etching is referred to as “chemical”. However, with electroless etching the etch rate is dependent on the potential of the electrode, which is not the case with chemical etching.

In general, the etch rate may be increased by increasing the hole injection current. This can be accomplished by increasing the oxidizing agent concentration. If the reduction reaction is mass-transport controlled agitation of the solution has a considerable effect on the hole injection current [Kovacs, 1998]. Usually, this results in an enhanced reaction rate.

As in the case of anodic dissolution, generally two types of surface morphology are possible with electroless etching. The silicon surface may be etched uniformly (referred to as isotropic etching) or a porous silicon layer is formed (referred to as stain etching [Fathauer, 1992], [Kidder, 1992], [Steckl, 1994]). An example of an isotropically etched surface profile is shown in Figure 3-9. The etch rate in these solutions is independent of the direction.

Fig. 3-9 Schematic of an isotropically etched silicon sample.

The determining factor for the resulting surface morphology is the hole injection current. If the dissolution reaction is limited by hole injection, a porous layer evolves. If the reaction is limited by diffusion of HF species to the surface, the silicon is electropolished. The morphology can be controlled by choosing either a relatively low oxidizing agent concentration for pore formation or a high concentration for uniform etching. Note that the pore formation process is isotropic as well since an electric field is not present in the Si bulk. This stems from the fact that oxidation and reduction reactions occur at the same sites. A disadvantage of stain etching is that the thickness of these layers is limited to a few microns [Schoisswohl, 1995]. When the layer reaches a thickness of about 500 nm the etch rate decreases drastically [Coffer, 1997], [Di Francia, 1995].

Commonly used solutions

One of the most commonly used isotropic etches is HNA; a mixture of HF, nitric acid (HNO_3), which is an oxidizing agent, and acetic acid (CH_3COOH). Acetic acid is added to stabilize the oxidizing agent concentration [Collins, 1997]. The reduction reaction of NO_3^- is autocatalytic, meaning that reaction products are required to keep the reaction going. This often results in an incubation time in which the concentration of the catalyzing species is built up. Only after this time does the reaction proceed at a considerable rate. This may limit the stability and reproducibility of etching. At room temperature a mixture of 250 ml HF, 500 ml HNO_3 and 800 ml CH_3COOH etches silicon at a typical rate of 4-20 $\mu\text{m}/\text{min}$. [Kovacs, 1998].

For stain etches a commonly used solution is a mixture of HF/ HNO_3 / H_2O with a ratio of 4:1:5. A typical porous formation rate is 60 nm/min [Coffer, 1997].

3.1.3 Open-circuit light-assisted dissolution

This technique is not commonly used for micromachining of silicon. It is briefly mentioned because it may be a promising alternative for existing etching techniques, e.g. for direct writing of patterns into a silicon wafer with a laser. It does not require an etch mask, nor implantations, diffusions, or external electrodes. In Figure 3-10 a schematic of the set-up is shown.

Fig. 3-10 Set-up used to form porous silicon layers by open-circuit illumination with a 1 mW He-Ne laser in 40% HF solution (left). Also shown is a profile scan of the etched hole in the n-type silicon sample (right).

A bare n-type silicon sample was immersed in a concentrated HF solution ($\sim 40\%$) and illuminated through a transparent plastic beaker with a 1 mW He-Ne laser (wavelength: 633 nm). The sample was kept under these conditions for 100 min. Afterwards, inspection with a microscope revealed a spot consisting of concentric rings with different colours, ranging from purple at the edges to green, blue and red/yellow in the centre. After a short dip in a 1% KOH solution at room temperature bubbles evolved at this spot and the colours disappeared, leaving behind an etched pit. The surface profile of this pit was scanned with a mechanical profilometer (Tencor α -step 500). The result is shown in Figure 3-10 (right). It is clear from this Figure that the etching is not uniform. Note the different scale of the X- and Y-axes. The non-uniformity is probably caused by the plastic beaker. The diameters of the spot size of the laser beam and the etched pit were 1 mm and about 3 mm, respectively. Refraction of the laser beam is caused by the set-up. The depth of the pit is about 2.5 μm , resulting in an estimated etch rate of about 25 nm/min.

There are few reports in literature on this type of porous silicon formation [Andersen, 1995], [Cheah, 1994], [Lim, 1992], [Noguchi, 1992]. In the first three reports similar laser powers and spot sizes (radius ~ 1 mm, resulting in an intensity of about 32 mW/cm^2) were used and similar etch rates were obtained (20-50 nm/min). In the last report, much higher

intensities were used (up to 2000 W/cm^2). It was found that the etch rate is dependent on the intensity. At high intensities etch rates of up to $1.3 \text{ }\mu\text{m/min}$ were obtained.

Etch mechanism

In these reports a detailed description of the etching mechanism is not given. It was proposed that the bending of the energy bands results in an electric field which drives the photogenerated holes to the silicon/HF solution interface, where they are consumed in the dissolution reaction. Due to the high intensity, the surface hole concentration is relatively high. The photogenerated electrons are driven into the bulk and to the unilluminated surface. At the unilluminated n-type Si/solution interface electrons are consumed in a reduction reaction. The most probable candidate is the reduction reaction of oxygen in solution.

3.2 Etch-stop techniques

In this section the most commonly known etch-stop techniques are reviewed. As in the previous Chapter, the methods are divided into two categories, intrinsic and extrinsic etch-stops. For electroless etching there is only one intrinsic etch stop technique. For electrochemical etching, etch-stop techniques are by definition all extrinsic since a power source is used.

3.2.1 Intrinsic etch-stop techniques

The HNA system etches heavily doped silicon preferentially with respect to lightly doped silicon [Lee, 1990]. For example, a HNA solution composed of 1 part 48 wt.% hydrofluoric acid, 3 parts 70 wt.% nitric acid and 8 parts acetic acid etches silicon with a resistivity of $10^{-2} \text{ }\Omega\text{-cm}$ at a rate of $0.7\sim 3 \text{ }\mu\text{m/min.}$, while silicon with a resistivity of $6.8 \times 10^{-2} \text{ }\Omega\text{-cm}$ does not have a measurable etch rate. This etch stop technique is often referred to as a lightly doped etch stop technique, not to be confused with the extrinsic lightly doped etch stop technique for the porous formation process. A disadvantage of this technique is that the HNA system has an irreproducible etch rate and selectivity. Moreover, this HNA composition etches defects preferentially. The low-doped layers should therefore be free from defects if a smooth finish is required after the etch stop. It proves to be quite difficult to grow low-doped defect-free epitaxial layers on

highly doped substrates. The defects in the substrate may easily propagate to the epitaxial layer during growth. Hence, only relatively thick membranes of more than $4\text{ }\mu\text{m}$ are possible.

3.2.2 Extrinsic etch-stop techniques

(1) *pn etch stop*

This technique is the most commonly used in porous silicon micromachining applications [Bell, 1996], [Bischoff, 1997], [Ducso, 1997], [Imai, 1984]. N-type mechanical structures are formed by diffusion of phosphorus in a p-type Si wafer. The p-type bulk is then anodized in the dark. The p-type silicon is made porous, while the n-type regions are left intact. In a second etching step the porous layer is removed in a low-concentration alkaline solution at room temperature. Alternatively, the p-type silicon is uniformly etched away [Eijkel, 1990]. This etch stop is schematically illustrated in Figure 3-11.

Fig. 3-11 *Illustration of the structure used for the pn etch stop. An n-type structure is undercut by p-type porous silicon, which is later removed in a second etching step.*

Note that etching should be done under absolutely dark conditions, as even moderate illumination generates enough holes to make the n-type structure porous. If the n-type layer is too thin, holes which are injected from the p-

type bulk may react at the n-type silicon/electrolyte interface before recombining. This also results in an n-type porous layer [Lee, 1990].

(2) Selective porous formation by electrical insulation

To overcome the limitations associated with the previous technique, the mechanical structures may be electrically insulated from the substrate. This can be done by using a polysilicon on oxide layer [Gennissen, 1999], [Kaltsas, 1998], [Steiner, 1993]. The structures are then made in the poly-Si layer while only the underlying p-type bulk is contacted and made porous. In this way the doping of the polysilicon layer may be either n- or p-type. This process resembles conventional surface micromachining. The difference is that a part of the bulk under the micromechanical structures is removed resulting in an increased air gap. Common problems associated with conventional surface micromachining such as sticking and air damping are thus avoided.

(3) Resistivity gradient limiting etch stop [Lee, 1990]

This technique is based on the difference in etch rate between very heavily doped n-type Si with a low resistivity ($<0.01 \Omega\text{-cm}$) and moderately doped n-type Si ($> 1 \Omega\text{-cm}$). The mechanical structures are formed using n-type doped Si in an n+ doped wafer. The applied bias has to be carefully adjusted between the breakdown voltages of n+ and n-type Si. The difference with the etch stop technique (1) is that the bulk material is n+ instead of p-type.

Thin structures of less than $1 \mu\text{m}$ are not possible with this technique. It is difficult to grow thin low-doped epitaxial layers on heavily doped substrates since the donor ions from the substrate diffuse easily into the top layer.

(4) Lightly doped etch stop [Bell, 1998]

With this technique an n-type silicon wafer is used as the substrate. The mechanical structures are formed using boron implantation and drive-in to yield low-doped p-type silicon islands. These islands are protected from the HF solution by a nitride layer. The bulk is biased positive during etching. Only n-type Si becomes porous because the pn junction blocks the current flow from n-type into p-type Si (see Figure 3-12). The built-in potential of the pn junction provides a barrier for the charge carriers. This results in undercutting of low-doped p-type crystalline structures.

Fig. 3-12 *The pn-junction blocks the flow of current resulting in undercutting of a lightly doped p-type silicon island.*

The nitride etch mask should cover the p-type area completely, since the reverse leakage current in the pn junction would lead to pore formation in the exposed p-type silicon as well. This method allows for fabrication of low-doped p-type structures and is complementary to the pn etch stop (1).

(5) *Damage limiting etch stop [Lee, 1990]*

This technique utilizes the difference in etch rate between implanted and unimplanted layers. It may also be used in alkaline solutions (see previous Chapter). When silicon is implanted with ions with an atomic mass equal to or greater than that of Si, the crystal lattice is damaged. This creates deep levels in the bandgap, which effectively trap holes and electrons. The free carrier concentration is reduced, which results in an increased resistivity of the damaged layers; the layer becomes semi-insulating. When this layer is exposed to a HF solution, the anodic current flow is blocked and etching stops. After the etch stop, the membrane may be annealed to regrow the crystal lattice. Figure 3-13 shows fabrication of membranes using this etch-stop process.

Fig. 3-13 *Etching stops at the ion implanted layer. After the etch stop the crystal damage in the membrane may be removed by annealing.*

With this technique very thin membranes (up to 30 nm) can be made. Because the trap levels are so effective in reducing the hole concentration, even n-type silicon substrates with implanted layers and a high illumination intensity may be used.

(6) Single-step etching using macroporous process for free-standing structures

This etch-stop technique is based on macroporous silicon formation developed by Lehman [Lehmann, 1993]. Free-standing mechanical structures are formed in one step by modulation of the light intensity [Ohji², 1999]. A similar set-up as shown in Figure 3-3 is used for this process. In the first stage macroporous trenches or vertical pores are etched with moderate-intensity illumination from the back. This is the anisotropic etch mode. In the second stage the light intensity is increased. As a result, the pore diameter increases and the etching becomes more isotropic (isotropic etch mode). In this mode, neighbouring vertical trenches are connected and free standing crystalline structures are obtained. The process is shown in Figure 3-14.

Fig. 3-14 *Process flow for fabrication of free-standing crystalline structures in a single etch step.*

The advantage of this technique is that only one mask and one etch step are required to fabricate relatively complex structures. The disadvantage is that a rather complicated set-up is needed for illumination at the back. Recently, this has been improved by using macropore formation in low-doped p-type Si.

(7) Contactless photovoltaic etch stop

The previous electrochemical etch-stop techniques have an important disadvantage. They require an etch holder or at least electrical contacts to the silicon wafer. The etch holder should be leak-free, which requires an O-ring construction which can withstand concentrated HF solutions. A batch process in which many wafers are etched at the same time is difficult to implement. For industrial applications, a contactless etch-stop technique would be advantageous. Such a technique is the photovoltaic etch stop [Yoshida, 1993]. The implementation is as follows. A p-type Si wafer is implanted or diffused with phosphorus to create n-type islands. When this wafer is immersed in an HF solution in the dark, the structure remains passive. Under illumination, charge carriers are generated in the semiconductor. In the bulk n- and p-type regions, the photogenerated minority carriers will recombine. In the depletion region of the pn-junction the photogenerated holes drift to the p-type silicon, where they participate in the anodic dissolution of the semiconductor. The photogenerated electrons drift to the n-type silicon side, where they participate in a reduction reaction of an oxidizing agent: oxygen or protons. In this way, the pn-junction functions as a photovoltaic cell which is short-circuited by the HF solution. The photocurrent flows from the positive n-side to the negative p-side, resulting in its anodic dissolution. The voltage between the two sides is approximately equal to the built-in potential of the pn junction. The structure is schematically depicted in Figure 3-15.

Fig. 3-15 *Contactless porous silicon formation with a pn junction. Photogenerated minority charge carriers are swept out of the depletion region and give rise to an anodic dissolution reaction at the p-type Si/electrolyte interface.*

It is obvious that the anodic current, and therefore also the etch rate, is dependent on the light intensity. However, if the light intensity is sufficiently high, the current and etch rate may become limited by the electrochemical reactions occurring at both sides of the pn junction.

Using this technique, free-standing n-type structures have been fabricated [Bischoff, 1997]. Instead of a p-type wafer an n-type wafer with a diffused p-well can be used as substrate to obtain a better defined airgap after etching.

(8) Galvanic etch stop

This is another technique which is contactless [Ashruf², 1999]. It is treated in detail in Chapter 5. Here, only a brief description is given. The structure used for this technique may be similar to that of the pn etch stop (1). Anodization is accomplished without an external power source. Instead, a platinum/chromium or gold/chromium layer is evaporated at the back where it makes electrical contact with p-type bulk silicon. The mechanical structures are formed using a phosphorous diffusion. When the wafer is immersed, oxygen in solution or another strong oxidizing agent is reduced at the metal surface. The holes generated at the metal/HF solution interface flow to the p-type Si/HF solution interface where p-type Si is anodically dissolved. N-type silicon is not attacked by HF in the dark, resulting in intact free-standing structures. Compared to the previous technique, a light source is not required, making it even more suitable for batch fabrication. Galvanic etching can also be used in combination with other etch-stop techniques, because the galvanic element only replaces the external power source.

3.2.3 Summary

In the following Table the etch-stop techniques are compared. The following issues are considered:

- *Is a wafer holder required?*
- *Is an external power source required (is the method extrinsic)?*
- *Is a light source required?*
- *Is a wide range of thicknesses possible?*
- *What is the doping type of the resulting structures?*

Table 3-1 *Comparison of etch-stop techniques*

Etch stop	Wafer holder or electrical contact?	External power source?/ Contact to n-type/p-type?	Illumination?	Thickness controllable?	Stop possible on p-type/n-type?
Intrinsic	no	no	no	no	both
pn	yes	yes / p	no	yes	n
Electrical insulation	yes	yes / p	no	yes	both
Resistivity gradient	yes	yes / n	no	no	n
Lightly-doped	yes	yes / n	yes	yes	p
Damage limiting	yes	yes / both	no	no	both
Single step macro porous	yes	yes / n	yes	yes	n
Photovoltaic	no	yes / contactless	yes	yes	n
Galvanic	no	no	no	yes	n

It can be concluded that the galvanic etch stop forms an attractive alternative to the conventional etch-stop techniques.

Galvanic etching in TMAH solutions

4

Fabrication of micromechanical structures with a reproducible thickness is usually accomplished by electrochemically controlled etching. This method requires an external contact to the n-type silicon to be passivated. For this purpose, usually a wafer holder is used which may introduce stress into the wafer and complicate batch fabrication. In this chapter, a new etch-stop technique based on a gold/silicon/TMAH galvanic cell is presented. The passivation potential and current are generated internally, which avoids the need for external contacts and makes the technique more suitable for batch fabrication. The theory of operation and experimental results on microstructure fabrication with this technique are presented in this chapter.

4.1 Introduction

Silicon micromechanical sensors are based on structures such as membranes and beams. There are a few techniques available for fabricating micromechanical membranes of a given thickness based on an etch stop in an anisotropic wet etchant (see Chapter 2). The simplest method is that of the timed etch stop, where a silicon sample is immersed in the etchant for a predetermined time. This is effective for applications where the thickness control of the membrane is not critical. A better

thickness control is achieved with the boron etch stop [Seidel, 1990]. However, this can only be used for single-clamped structures due to high stress. Furthermore, due to the high doping concentration electronics cannot be integrated in the structures. If membranes of a reproducible thickness are required the Electrochemically Controlled Etch Stop (ECES) can be used [Kloeck, 1989]. With this method excessive doping is not needed. An electrical contact to the wafer is usually achieved by a wafer holder [Sarro, 1986]. This has two main disadvantages. Firstly, the requirement to contact each wafer and each structure separately makes batch fabrication difficult. Secondly, the wafer holder itself can introduce mechanical stress into the silicon because of the difference in the thermal expansion coefficients. For the fabrication of fragile structures this can seriously reduce the yield of the process.

Recently, a new contactless etch-stop method has been reported by French et al. using a p-type bulk and an n-type diffused layer [French, 1996]. A gold/chromium film is evaporated onto the n-type epi layer, while an etch mask is patterned on the p-bulk side. When the system is immersed in a TMAH solution a galvanic element is formed. The gold surface acts as the cathode at which an oxidizing agent is reduced. The n-type silicon is oxidized and forms the anode. Due to galvanic element formation, the potential of the n-type epi-layer shifts to values positive with respect to its passivation potential. Etching of the p-type bulk proceeds until the pn-junction is reached, at which point etching stops resulting in an n-epi membrane. Compared to the photovoltaic etch-stop technique, a light source is not required making the method even more attractive for batch fabrication. In the following sections the etch-stop mechanism is explained and its application to the fabrication of microstructures such as membranes and beams is discussed.

4.2 Experimental

Four inch <100>-oriented silicon wafers (p- or n-type) with a doping concentration of approximately 10^{15} cm^{-3} ($2\text{-}5 \Omega \text{ cm}$) were used.

The electrochemical experiments were performed with a Bank POS73 Potentiostat. The cyclic voltammograms were measured at a scan rate of $10\text{-}20 \text{ mV/s}$ in the dark. The silicon working electrode consisted of a diced $1 \times 1 \text{ cm}$ sample with an ohmic contact at the back. The contact was made by high dose phosphorus or boron implantation with aluminium

metallisation. The electrode was mounted with its surface (area approximately 0.6 cm^2) facing upwards (schematically shown in Figure 4-1). This was necessary to prevent blocking of the Si surface by hydrogen gas which evolved during etching.

Fig. 4-1 *Set-up used for the current-potential measurements of silicon electrodes. The silicon samples were mounted in a special wafer holder.*

A platinum counter electrode with a relatively large surface area and a saturated calomel electrode (SCE) as reference were used.

With potential time measurements, a separate metal sheet was used as the cathode of the galvanic element. For the fabrication of micromechanical structures the gold cathode was formed by evaporation. Chromium was used as an adhesion layer. The thickness of the chromium layer was 40-60 nm, that of the gold layer was 400-600 nm. In some applications, the cathode area was patterned using a lift-off process.

For all experiments commercially available tetramethyl ammonium hydroxide (TMAH, 25% in water, Fluka Chemica) was used. The temperature was controlled using a double-walled glass vessel (see Figure 4-1). Before the etching experiments the wafers were dipped in a 1% HF (Merck) solution for 2 minutes to remove native oxide. The etched structures were analysed with a SEM.

4.3 Principle of galvanic element formation

4.3.1 Anodic passivation of silicon

The galvanic passivation mechanism was studied by measuring current-potential curves of silicon electrodes in a 25% TMAH solution. The mechanisms of dissolution and passivation are discussed in more detail in Chapter 2. The results for a p-type and n-type silicon electrode in a 25% TMAH solution at 70 °C are shown in Figure 4-2 and 4-3.

Fig. 4-2 A current-potential curve of a p-type silicon electrode of 0.5 cm^2 in a 25% TMAH solution at 70°C.

The stable open-circuit potential (OCP) of p-type Si is -1.6 V (SCE) and at this potential the semiconductor dissolves chemically at a rate which depends on the temperature and on the composition of the solution. At potentials more negative than OCP, a small cathodic current is observed. As the potential is made positive with respect to OCP, the current becomes anodic and increases markedly. Silicon is electrochemically oxidized and the products dissolve in the solution. The mechanism of this reaction is complex involving both electrochemical and chemical steps (see Chapter 2). At a critical current I_{pp} , corresponding to the passivation potential V_{pp} , an oxide layer is formed on the Si. The current drops markedly to a low value in the passive range. In this range the chemical etching of Si is also suppressed since the etchant no longer has access to the Si-Si surface

bonds. The current in the passive range is determined by the rate at which the oxide is dissolved chemically by the TMAH solution.

Fig. 4-3 A current-potential curve of an n-type silicon electrode of 0.5 cm^2 in a 25% TMAH solution at 70°C .

A significant cathodic current is observed at negative potentials with n-type Si in TMAH solutions. This results from the electrochemical reduction of water to hydrogen, requiring conduction band electrons. Apart from this process, which obviously does not occur at p-type Si, the form of the current-potential curves of the two types of electrode is similar. Note that the curves are similar to the results obtained in KOH solutions (Chapter 2). The current to achieve passivation of n-type Si (I_{pp}) is approximately the same as that required for p-type material. The open-circuit potential and the passivation potential are slightly negative with respect to p-type material, although this difference is less pronounced than with KOH solutions [Acero, 1995].

4.3.2 Galvanic passivation of silicon

Silicon, chemically etching at OCP in an electrochemical cell, can be passivated by applying a potential more positive than V_{pp} and by passing a current larger than I_{pp} through the cell. This means that some electrical power is required to accomplish anodic passivation. In principle, it should be possible to make use of a galvanic element to achieve the same effect without using an external source. In general, a galvanic cell consists of two

electrodes, i.e. the anode at which an oxidation reaction occurs (electrons are generated) and the cathode at which the reduction reaction takes place (electrons are consumed) [Bard, 1980]. When the electrodes are short-circuited, a stable rest potential is established, which can be measured with respect to a reference electrode. In the present case the Si electrode (anode) with ohmic contact is brought into electrical contact with an inert electrode (e.g. gold) at which an oxidizing agent Ox^{n+} can be reduced electrochemically (cathode):

The equation can also be written in terms of holes:

The standard redox potential for the redox system Ox^{n+}/Red must be positive with respect to the passivation potential of the Si. The principle of galvanic passivation can be understood with the help of the current-potential curves indicated in Figure 4-4. Curve (a) shows schematically the anodic partial current as a function of potential for p-type Si in the etching solution without oxidizing agent (see also Figure 4-2). Curves (b) and (c) are those expected for the cathodic reduction of the oxidizing agent at the inert gold electrode. Since in the galvanic cell the electrons required for this reaction are supplied from the valence band of Si, the reduction is better described by reaction (4-2). In Figure 4-4 it is assumed that the rate of this reaction is controlled by diffusion of the oxidizing agent to the electrode and the current is therefore independent of the applied potential in a wide potential range. For curve (c) the concentration of oxidizing agent is higher than for curve (b). The rest potential of the Au electrode in the solution containing Ox^{n+} is the redox potential $V_{Ox^{n+}/Red}$. When the two electrodes in the solution containing the oxidizing agent are short-circuited, holes injected by Ox^{n+} at the Au electrode (reaction 4-2) flow to the Si where they are available for electrochemical oxidation of the semiconductor. In the case of the lower concentration of oxidizing agent (curve (b)) the maximum current that can be expected, assuming no ohmic losses in the galvanic cell, is the mass transport limited current I_b . From Figure 4-4 it can be seen that this is lower than the current required to passivate the Si (I_{pp}). When the two electrodes are short-circuited in this case, the potential of the Si shifts from OCP to the rest potential V_b . Note that at V_b , the anodic (hole consumption) and cathodic (hole generation)

currents must be equal, since there is no external current source. In addition to chemical dissolution, Si is anodically dissolved due to galvanic element formation. In the case of a higher concentration of oxidizing agent, the maximum current I_c is larger than the passivation current. Short circuiting the electrodes leads to the formation of an anodic oxide layer on the Si. The Si potential is now in the passive range at V_c and the chemical etch rate of Si is negligibly low. The current required to maintain the passivated state at V_c is clearly very low.

Fig. 4-4 Schematic representation of galvanic cell formation in a TMAH solution containing oxygen from the air. Curve (a) shows the anodic current due to silicon oxidation. Curves (b) and (c) refer to the reduction of the oxidizing agent at the gold electrode. Curves (b) and (c) are the reduction currents with a low and high oxidizing agent concentration, respectively. If the two electrodes are connected the rest potential of the couple assumes a value in between the open-circuit potential of the silicon electrode (OCP) and the open-circuit potential of the gold electrode ($V(\text{Ox}^{n+}/\text{Red})$). At operation point V_b the cathodic current is not sufficient to achieve passivation. With a higher oxidizing agent concentration (curve (c)) V_c is reached. At this potential the silicon electrode is passivated.

To demonstrate that galvanic passivation works in practice two types of measurement were performed; (a) with separate Si and Au electrodes and (b) with a Si wafer the front of which was provided with an evaporated gold/chromium film. In both cases oxygen naturally present in the solution was used as oxidizing agent. The reduction reaction is:

The redox potential of the O_2/OH^- couple at pH 14 (0.17 V (SCE) [Bard, 1985] is more than one volt positive with respect to the Si passivation potential. In order to show that reaction (4-3) could provide sufficient current to passivate the Si, current-potential curves with gold electrodes were measured in the TMAH solution. A typical result is shown in curve (a) of Figure 4-5.

Fig. 4-5 *Current-potential curve of a gold electrode of approximately 4 cm² in a 25% TMAH solution at 70 °C, which was saturated with oxygen from the air (a). Next, oxygen was purged from the solution by argon bubbling and the scan was made again (b).*

The scan starts at positive potentials with respect to the open-circuit potential (-0.2 V). At this potential we find an anodic current. This is due

to oxidation of the gold surface. At higher potentials oxygen is generated according to:

For galvanic element formation, it is more interesting to consider the cathodic potential range. When the potential is scanned to values negative with respect to the open-circuit potential a cathodic current peak is observed (at -0.35 V). This is due to the reduction of the oxidized gold surface. At about -0.4 V the current becomes independent of the potential. This cathodic current is due to the reduction of oxygen which is naturally present from the air (reaction 4-3). This reduction reaction is limited by diffusion of oxygen to the gold surface. At about -1 V the current suddenly increases. This is due to reduction of water to hydrogen gas:

From curve (a), a mass transport limited current of about 300 μA is observed. That this plateau current is indeed due to oxygen reduction is clear from curve (b), which was measured after oxygen was purged from the solution by argon bubbling. A reduction in current of about 80% is clearly observed. Figure 4-5 shows that the cathodic current from the reduction reaction (300 μA) is not quite sufficient to provide the peak current of 400 μA (Figure 4-2). However, the oxygen concentration at the surface of the gold electrode immediately after immersion is the same as the concentration in the bulk solution. The initial rate of oxygen reduction is therefore considerably higher than the steady-state diffusion controlled rate. In hydrofluoric acid solutions the initial cell current was easier to measure (Chapter 5).

Measurement of the rest potential

In order to measure the change in rest potential of the system the following experiment was performed. The open-circuit potential of the silicon electrode in 25% TMAH solution at 70 °C (Figure 4-2) was monitored using a high impedance voltmeter. After some time, the silicon electrode was contacted to a gold electrode which was also immersed in the solution. The set-up is illustrated in Figure 4-6.

Fig. 4-6 *Set-up for open-circuit potential measurements. When the switch is closed, the rest potential shifts to positive values. This is recorded with a voltmeter.*

The measured potential-time curve is shown in Figure 4-7.

Fig. 4-7 *The time dependence of the rest potential of a silicon electrode in a 25% TMAH solution at 70°C. After 0.5 min. a gold electrode is connected to the Si and the rest potential of the system changes. After 1.5 min. the switch is opened again.*

The initial potential is -1.6 V. This is typical for a chemically etching silicon electrode. Chemical etching was obvious from the hydrogen evolution. After 0.5 minutes the switch was closed and the potential

rapidly changed to about -0.4 V (SCE), which is well into the passive range. It is useful to compare these potentials to those of Figures 4-2. The potential stabilized quickly and remained constant. Clearly, the Si had become oxidized and chemical etching stopped. After opening the switch at 1.5 min, a rapid decrease of the potential to -1 V (SCE) could be observed. The silicon does not immediately resume its initial OCP. This is due to the presence of the anodic oxide which was grown during passivation of the silicon. The time needed to re-establish the initial OCP is the etch-back time of the oxide [Bressers², 1995], [Palik, 1982].

4.3.3 Wafer-level galvanic element formation

As described in the previous sections, galvanic passivation is possible with separate electrodes. In this section we show that galvanic passivation is also possible on the wafer. The structure used for this purpose is illustrated in Figure 4-8.

Fig. 4-8 *Structure of a galvanic element made by evaporation of a gold/chromium film on a patterned silicon substrate.*

An n-type or p-type silicon substrate was patterned with a nitride layer. At the back, openings in the nitride layer exposed bare silicon to the etching solution. At the front, openings were etched in the nitride layer for the electrical contact. In these preliminary tests, n^+ or p^+ layers were not used for ohmic contact. A chromium layer of 40~60 nm and a gold layer of 400~600 nm were evaporated (with e-beam) on the silicon wafer. The chromium served as an adhesion layer. The wafers were dipped in 1~5% HF prior to etching. When the wafer was immersed in an 25% TMAH solution at 80 °C, etching did not start. Typically, there was a some gas formation at the silicon surface for a short time (< 1 s) after which the

electrode remained passive. As will be shown in the next Chapter, this is due to the dissolution of a porous silicon layer which was formed galvanically during stripping of the native silicon oxide layer in the HF solution. If the gold cathode was shielded from the etchant (with another wafer which was completely covered by silicon nitride), etching recommenced, proving that the gold film was responsible for the passivation.

In these tests, the surface area of the gold cathode was about 79 cm^2 (area of one side of a 4" wafer). The area of the exposed silicon was 9.3 cm^2 . This resulted in an area ratio of 8.5, which proved to be sufficient. In an attempt to find out the influence of the area of the gold contact opening on the effectiveness of the etch stop, wafers were prepared with contact areas of 36 cm^2 , 9.3 cm^2 , 1 mm^2 and $100 \mu\text{m}^2$. The last two contacts were made in the centre of the wafer. Only the wafer with the contact of $100 \mu\text{m}^2$ did not passivate. This proves that the contact area apparently is not critical in this configuration. These tests show, that galvanic element formation may lead to passivation for gold-to-silicon area ratios as small as 8. Hence, care must be taken when gold (or other noble metals) is used as an etch mask.

4.4 Galvanic etch stop

A pn-configuration can be used to fabricate n-type membranes in a way similar to the two electrode ECES. This technique is referred to as the galvanic etch stop. It has one major advantage compared to the conventional ECES, which is that a wafer holder and external contacts are not required. In principle, this allows for an easier implementation of batch fabrication, making the process cheaper. Elimination of the wafer holder should also result in a process with a higher yield. Breakage due to stress caused by the wafer holder or the pressure difference between the solution and the space inside the fixture is avoided.

4.4.1 Membrane fabrication

The basic structure used for these experiments is shown in Figure 4-9. An n-type epi-layer of $4 \mu\text{m}$ is grown on a p-type silicon wafer. Next, an LPCVD low stress silicon nitride layer is deposited. It is patterned at the front to form the electrical contact from gold/chromium to n-type silicon.

Fig. 4-9 *Basic structure used for the galvanic etch stop. A p-type substrate is provided with an n-type epi layer. Next, a silicon nitride layer is deposited. The front is patterned for electrical contact, while the back is patterned to expose bare silicon. Finally, a gold/chromium film is evaporated on the front.*

At the back, the patterned nitride serves as an etch mask. The total area of the windows in the nitride is 9.3 cm^2 . Finally, a gold/chromium (400-600 nm/ 40-60 nm) film is evaporated on the front. The area of the gold cathode is 79 cm^2 , resulting in a gold/exposed n-Si area ratio of about 16 (due to the anisotropy of the etching process the exposed n-Si area is not 9.3 cm^2 but 4.8 cm^2). The chromium serves as an adhesion layer. Note that this structure is similar to that used for the pn electrochemically controlled etch stop (see Chapter 2).

This structure is immersed in a 25% TMAH solution at 80°C . An anodic current equal to I_{pp} must be supplied from the gold to the p-Si/etchant interface to stop the etching process. However, the current which can flow in this direction is limited by the reversely biased pn-junction. In pn-junctions formed by a p-bulk and n-type epi-layer the reverse leakage-current is generally low. Therefore, the p-type Si bulk is effectively isolated from the gold cathode and etched chemically until the junction is reached. The low reverse leakage current results in a slightly enhanced etch rate. When the etch front reaches the pn-junction, the junction is destroyed locally. At this moment, the galvanic element is switched on. Electrons are injected into the n-Si conduction band, giving rise to an

anodic current and a passivating oxide layer is formed on the surface. The electrons are consumed at the gold electrode according to reaction (4-3).

In Figure 4-10 a resulting n-epi membrane obtained after etching for 18 hours in a 25% TMAH at 80°C is shown. Another two hours of overetching did not result in a measurable change in thickness.

Fig. 4-10 A cross-section of a resulting n-type epi membrane after the galvanic etch stop. Clearly seen is the epi membrane of 4.8 μm thick.

Current-time measurements were performed to verify the operation of the galvanic etch stop. For this purpose separate electrodes were used. In a wafer holder a pn-wafer was mounted which was identical to the wafers used for galvanic membrane fabrication (see Figure 4-9). For the gold cathode, a gold/chromium film was evaporated on a silicon wafer which was covered by a silicon nitride layer. The anode and cathode were externally contacted to a current meter. The galvanic current was monitored with a PC during the etching process. The result is shown in Figure 4-11. The initial current is 0.2 mA. This is the reverse leakage current in the pn-junction. After 950 minutes the current suddenly increases. At this time the etch front approaches the pn-junction. After a few minutes a peak of 2.4 mA is reached. At this point an anodic oxide layer grows on the surface and etching stops. Afterwards, the current drops to a low value of 1.5 mA. We expected a current which is lower than the reverse leakage current. Similar current-time transients have also been reported for electrochemical etch-stop experiments [Acero, 1995], [Andrews, 1991], [Götz, 1993]. It is unclear what causes this relatively high passive current.

Fig. 4-11 *Measurement of the galvanic current during the etching process.*

4.4.2 Uniformity of the thickness of the membranes

The uniformity of the thickness of the membranes was checked [Oemar, 1998]. The thickness was measured by inspecting the cross-section of a sample with a scanning electron microscope (SEM). The inaccuracy of this method was estimated to be $\sim 0.2 \mu\text{m}$. The number of membranes checked was > 20 .

The contact pattern on the front consisted of distributed squares and had a total area of 9.3 cm^2 . The same pattern was used for the etch mask at the back of the wafer. The etch-stop area of the n-type membranes was 4.8 cm^2 (see Figure 4-9). The experiments described in this section were all obtained from wafers which were only partly immersed in the etchant. About 25% of the wafer was left out of the solution. The reason for this is

outlined in the next section. The influence of the temperature, solution concentration and the contact pattern were investigated. The results are summarized in Table 4-1 and are discussed in following sections.

Table 4-1 *Thickness of membranes (μm) under various etching conditions*

Temperature vs solution concentration	5 %	12.5 %	25 %
70 °C	-	-	4 - 10 (4.9 ± 0.4) *
80 °C	0	4.6 ± 0.2	4.7 ± 0.2
87 °C	-	-	4.7 ± 0.2
90 °C	-	-	0

* These results were obtained in the dark.

The thickness distribution was within the accuracy of the measurement technique. In the Table the average value and the maximum deviations are indicated.

Influence of the etching temperature

The temperature was varied from 70 °C to 90 °C, while the concentration was kept fixed at 25%. A SEM photo of a wafer etched in a 25% TMAH solution at 70 °C is shown in Figure 4-12. The results for 70°C are somewhat surprising since the thickness of the membranes is not uniform. The etching was performed under normal laboratory illumination. Since illumination increases the reverse-bias current in pn-junctions, the passivation current may be reached sooner resulting in a preliminary etch stop. Similar effects with the conventional electrochemical etch stop were reported by Götz *et al* [Götz, 1993]. This led us to try the etching experiment in the dark. The etch set-up was placed in a black box and the experiment was repeated. The results are indicated in brackets. In this case, the thickness is more uniform. The average thickness appears to be slightly higher than at 80°C but with the present measurement technique, this cannot be confirmed.

The uniformity at 80°C and 87°C was not affected by the environment light. An etch stop was not obtained at 90°C. Qualitatively, this can be

explained by realizing that the passivation current density of a silicon electrode is highly dependent on the temperature (Figure 4-16). An upper limit for the allowable temperature is therefore expected. At 80°C the passivation current density is considerably higher than the reverse-bias photocurrent, so background light is not important. At 90°C, the peak current density is too high to permit galvanic passivation.

The following can be concluded:

- *The best uniformity is obtained by etching at temperatures around 80 °C.*
- *There is an upper limit to the temperature at which the galvanic etch stop is possible with a given configuration.*

Fig. 4-12 SEM photo of a membrane etched in a 25% TMAH solution at 70 °C.

Influence of the solution concentration

The concentration was varied while the temperature was fixed at 80 °C. Apart from the 25 % solution, which was presented in the previous section, concentrations of 5 % and 12.5 % were used.

The average thickness is similar to that from a 25% solution. At lower concentrations, the hillock density increased which is clearly seen in the Figure 4-13.

Fig. 4-13 SEM photo of a membrane etched in a 12.5% TMAH solution at 80 °C.

This is generally undesirable for micromachining applications. Note that the etch rate in a 12.5 % solution is about 1.5 times higher than in a 25% TMAH solution. There is a trade-off between etch rate and surface roughness. With a concentration of 5% the etching did not stop. This may be explained by considering that the passivation current density increases with decreasing concentration. Again, apparently there is not a sufficient oxygen reduction-current to supply this passivation current at the silicon/solution interface.

The following can be concluded:

- *The optimum concentration for a smooth surface is 25 %.*
- *There is a limit to the solution concentration, below which the galvanic etch stop does not work with a given configuration.*

Batch fabrication

A major advantage of this technique with respect to other techniques, which use a low dopant concentration (as discussed in Chapter 2), is the possibility for batch fabrication. Two identical wafers were etched at the same time. They were partly immersed in the etchant and spaced one centimeter apart. This resulted in an identical membrane thickness

distribution and average membrane thickness. The following can be concluded:

- *Batch fabrication with the galvanic etch stop is possible and easy to implement.*

Influence of the contact area

Experiments were repeated with a different contact area. Instead of a distributed contact area of in total 9.3 cm^2 a large square of 6 by 6 cm was used. This did not affect the average membrane thickness and uniformity.

4.4.3 Beam fabrication

The galvanic etch stop is not limited only to the fabrication of two dimensional structures, such as membranes. It may also be used to make free-standing structures in a single etch step. A simple beam was chosen to demonstrate this technique. A front-side etching process was used to release the structures. In Figure 4-14 the design of the structure is shown.

Fig. 4-14 *Schematic of the n-type crystalline silicon beam structure for a front-side etching process.*

An n-type epi-layer was grown on a p-type silicon substrate. The n-type crystalline beams were defined by a p-type boron diffusion. After boron diffusion, a silicon nitride layer was deposited and patterned. The etch windows and the gold to n-type silicon contacts were opened in one step. Finally, a gold/chromium film was evaporated and patterned using a lift-off process. From one wafer, 36 square dies of 1 by 1 cm were sawn. The experiments were performed with separate dies. The p-type diffusion layer was also made in the saw lanes, which were used to align the diamond saw. The edges of the chips were completely p-type and leakage currents

from cleaved pn-junctions were avoided. The area of the gold film, the initial n-type silicon and p-type exposed area on one die were 75 mm^2 , 2.3 mm^2 and 2.6 mm^2 , respectively. The total die area was 100 mm^2 . The gold to initial n-type silicon area ratio was 33. During undercutting of the n-type Si beams, the exposed Si area increases. This does not necessarily lead to a higher anodic current, since passivated n-type silicon has a low anodic current. The electrical characteristics of the pn-junction were first measured, to verify that the reverse current was sufficiently low. After a short 1% HF dip, the structures were etched in a 25% TMAH solution. If the structure was completely immersed, an etch stop was not obtained. By partly immersing the dies, the etch stop proved to be effective. The resulting n-type silicon beams are shown in Figure 4-15.

Fig. 4-15 SEM photos showing n-type silicon beams in a p-type substrate which is undercut (left). Also shown is a close-up of the tip of one beam (right).

This sample was etched for 2 hours at 80°C . The p-type silicon is not yet completely undercut. Note that the shape of the beams is typical for a diffusion profile.

4.5 Design rules for galvanic etch stop

Generally, the galvanic etch stop is successful when the following requirements are satisfied.

1. *The generated cell current should be equal to or larger than the silicon passivation current.*
2. *The potential of the silicon surface should be positive with respect to the passivation potential.*

The first requirement sets the design rules for the gold-to-silicon etch-stop area ratio. Once the etching conditions are decided, this area ratio has to be chosen such that requirement (1) is fulfilled. The passivation current is a function of temperature and concentration of the TMAH solution. The passivation current-density as a function of temperature is shown in Figure 4-16. In general, the passivation current is proportional to the chemical etch rate.

Fig. 4-16 *Measured passivation current density of a silicon electrode in a 25% TMAH solution as a function of temperature.*

In Chapter 2 it was concluded that a concentration of 25% gives the best surface quality. Therefore, this concentration was used for most experiments. The oxygen reduction current proved to be relatively independent of temperature. For higher temperatures a higher area ratio is required. From the previous section, it was concluded that a temperature of 80 °C is favourable for the uniformity. At this temperature, different area ratios were tested. The minimum area ratio was found to be about 40. This

was also expected from the current-potential measurements. A typical oxygen reduction current density was about $25 \mu\text{A}/\text{cm}^2$. From Figure 4-16 the typical silicon oxidation current density was about $1 \text{ mA}/\text{cm}^2$. The estimated area ratio is therefore 40. When the wafer was only partly immersed in the TMAH solution area ratios down to about 16 also proved effective. At the TMAH/air interface a meniscus is formed on the gold surface. Oxygen diffusion from the air through the meniscus is more efficient than diffusion of dissolved oxygen from the bulk of the solution. Hence, a higher reduction current-density is expected at the meniscus. Measurements with partially immersed electrodes of $1 \times 2 \text{ cm}$ resulted in an increase in the diffusion-limited reduction current by typically a factor of 5-7. In the literature, similar effects were described by Will [Will, 1963]. With evaporated electrodes with an area of 79 cm^2 (one side of a 4" wafer) the same reduction current was measured with partly immersed and completely immersed wafers. In this case, the meniscus effect was less pronounced but obviously still present.

The second requirement sets the design rules for the location of the electrical contacts relative to the etch-stop area. In general, the open-circuit potential of the gold electrode should be positive with respect to the silicon passivation potential. This limits the use of additives to sufficiently strong oxidizing agents. However, even if this constraint is satisfied, galvanic passivation is still not guaranteed. If there is an ohmic voltage drop between the electrical contact of the gold cathode to n-type silicon and the etch-stop area, the passivation potential of the etch-stop area shifts to positive values. The shifted value may become positive with respect to the open-circuit potential of the gold cathode. In Figure 4-17 this is illustrated: A typical passivation potential is -1 V (vs SCE), while the typical open-circuit potential of a gold electrode is -0.4 V (vs SCE) when oxygen is used. Therefore, with a shift of about 0.6 V galvanic passivation is no longer possible. With a passivation current of 0.5 mA (which is typical for an electrode of 0.5 cm^2 in a 25% TMAH solution at 80°C) this voltage drop occurs with a resistance of 1200Ω .

Current-potential measurements were done using silicon samples with an electrical contact placed 33 mm from the etching area. A schematic of the samples is shown in Figure 4-18.

Fig. 4-17 Schematic representation of galvanic element formation between a gold electrode and a silicon sample. A typical silicon current-potential curve is shown as curve (a). Its passivation potential is denoted as PP_1 . If there is a relatively large resistance between the electrical contact and the etching area, the characteristic is shifted by a value corresponding to the voltage drop over this resistance (curve (b)). The new passivation potential is PP_2 . The oxygen reduction curve is represented by (c). In this case it is impossible to passivate the silicon electrode galvanically.

Fig. 4-18 Schematic of the samples used to study the influence of the location of the electrical contacts relative to the etching area.

The passivation potential and current are compared to the values obtained with electrodes using ohmic contact at the back in Figure 4-19.

Fig. 4-19 Passivation current (a) and potential (b) as a function of temperature for silicon electrodes with contact at the back (α) and electrical contact placed 33 mm from the etching area (β).

The current for both electrodes increases with temperature (Figure 4-19 (a)). The bar-type electrodes had a larger current because of the exposed edges. The passivation potential of the bar-type electrodes is shifted to positive values (Figure 4-19 (b)). The shift becomes larger at higher temperatures since the passivation current increases. At a temperature of 80°C , the open-circuit potential of the gold electrode is only 0.1 V positive with respect to the passivation potential. With these electrodes, it was impossible to passivate the silicon surface galvanically.

P-type wafers with an n-type epi were fabricated with the electrical contacts at different locations. With a resistivity of 2-5 Ω cm and an epi-layer thickness of 4 μ m, an etch stop was only obtained when the contacts were located at a distance less than about 10 mm from the etching area. With the devices presented in Chapter 6, contacts were never placed more than 2 mm from the etch-stop area.

4.6 Alternatives to oxygen saturated TMAH solutions

4.6.1 Galvanic etching in other alkaline solutions

Obviously, galvanic passivation of silicon is not limited to TMAH solutions. This becomes clear by considering that the current-potential characteristics of silicon in all alkaline solutions are quite similar. As an example, in this subsection we consider galvanic element formation in KOH solutions since it is the most commonly used alkaline etchant. A typical passivation potential in a 33 % KOH solution at 80 °C is -0.8 V vs SCE, which is negative with respect to the rest potential of a gold electrode in oxygen-saturated solution. This means that galvanic passivation is in principle possible. The reason why this effect was never encountered is explained in Figure 4-20, which shows the passivation current density of (100) Si in a 33% KOH solution as a function of temperature. In the same Figure the passivation current density of the same electrode in a 25% TMAH solution is also shown [Ashruf², 1998]. Clearly, the passivation current density in KOH solutions is more than 4 times larger than in TMAH solutions. It is much easier to passivate silicon in TMAH solutions, which is consistent with the fact that TMAH solutions are more selective with respect to silicon oxide layers. For KOH solutions, the cathode to etch-stop area ratio should be 4 times larger than in TMAH solutions, which results in a ratio of >160. Therefore, when oxygen is used as oxidizing agent, galvanic passivation in KOH solutions is not practicable for device fabrication. When another strong oxidizing agent is added to the KOH solution this area ratio may be decreased. Experiments have demonstrated the possibility of galvanic passivation in these solutions.

Fig. 4-20 Passivation current density of a (100)-Si sample in a 33% KOH (a) and 25% TMAH (b) solution.

4.6.2 Galvanic etching using other oxidizing agents

For many applications the minimum area ratio between the cathode and etch-stop area of >40 is not feasible. Since the reduction current at the gold cathode is diffusion limited, it is very sensitive to agitation of the solution. The area ratio may be decreased if the solution is stirred. However, this is not an elegant solution of the problem since it is difficult to control the cell current in a reproducible way. Another solution would be to bubble oxygen along the cathode surface but this requires a more complicated set-up. Finally, the cell current density may be increased by increasing the oxidizing agent concentration. A strong oxidizing agent is then added to the TMAH solution. A suitable candidate for this purpose is ferricyanide ($\text{Fe}(\text{CN})_6^{3-}$). This is reduced as follows:

Reduction of this oxidizing agent starts at a potential sufficiently positive with respect to the passivation potential of Si; the standard redox potential of the $\text{Fe}(\text{CN})_6^{3-}/\text{Fe}(\text{CN})_6^{4-}$ couple is only 0.04 V negative with respect to the O_2/OH^- couple [Bard, 1985]. The problem associated with this method is that there is an upper limit to the concentration of ferricyanide that can be used. When the concentration is made too high, the silicon surface is oxidized and the electrode passivates [Bressers, 1995]. The electron

acceptor is sufficiently strong to extract electrons from the valence band; i.e. it injects holes. In a next step the holes are consumed in the dissolution of the silicon crystal. If the concentration and hole injection current exceed a limit, an oxide layer forms on the surface and the silicon crystal is shielded from the etchant. Similar effects were also found in solutions of $\text{NH}_3/\text{H}_2\text{O}_2$ [van den Meerakker, 1990]. In the case of a 10% KOH solution at 70°C the critical concentration of ferricyanide is 35 mM. In the case of a 25% TMAH solution at 80°C the critical concentration was 10 mM. Measurements showed that at concentrations <10 mM a reduction current density increase of at least a factor of 4 is possible. Therefore, cathode to etch-stop area ratios down to 10 should be feasible. However, these configurations have not yet been extensively studied.

4.7 Conclusions

To avoid the disadvantages of the ECES method, i.e. the need for a wafer holder and external contacts, a new etch-stop technique was developed for fabrication of crystalline silicon membranes and free-standing beams with a uniform thickness. The only non-standard processing step compared to the ECES technique is the evaporation of a gold/chromium layer which makes electrical contact to the silicon. With this technique an external power source is not required, as voltage and current are generated by a gold/silicon/TMAH galvanic cell. The galvanic etch stop is therefore believed to be an excellent alternative for batch fabrication of micromechanical structures. An etch stop is achieved if the galvanic cell supplies sufficient current which depends on the concentration of oxidizing agent in the solution. When oxygen is used as the oxidizing agent, the ratio between the areas of the gold cathode and silicon etch-stop region should be at least 40 to achieve an etch stop. This value holds when a 25% TMAH solution at 80°C is used. The electrical contacts should be placed at less than about 10 mm from the etch-stop area. This value depends on the resistance between the cathode contact and the etch-stop area. The area ratio may be decreased by adding strong oxidizing agents such as ferricyanide to the solution. In this case care should be taken not to exceed a critical concentration at which the silicon is passivated and etching is prevented.

Galvanic etching in HF solutions

5

Porous silicon is usually formed under anodic polarization in an electrochemical cell. In this chapter, a technique is described to form porous silicon without using an external power source. By connecting an inert metal electrode to a silicon sample, both immersed in a HF solution, a galvanic cell is formed. Reduction of oxygen at the inert electrode results in the etching of Si at the silicon/electrolyte interface. Porous silicon is formed at a rate which is dependent on the cell current. The formation rate may be enhanced by adding oxidizing agents to the solution. Galvanic formation of porous Si is a promising alternative for stain etching since it gives more uniform and reproducible results. Furthermore, it allows for fabrication of free-standing structures in a single etch step.

5.1 Introduction

Porous silicon can be used for a range of applications, including semiconductor-on-insulator technology [Smith, 1992], light-emitting devices [Hirschman, 1996] and sensors [Bischoff, 1997]. Porous silicon is usually formed electrochemically in aqueous or ethanolic HF solutions. The reactions occurring at the silicon anode were given in Chapter 3. For the anodic dissolution reaction valence band holes are required. Hence, the

p-type semiconductor can be made porous by etching in the dark, while for n-type Si illumination is necessary to generate valence band holes.

For certain applications it may be useful or necessary to form porous Si "chemically", i.e. without the need for an external current or voltage source. A process referred to as "stain etching" is based on the use of nitric acid as oxidizing agent in HF solutions [Fathauer, 1992]. Nitric acid is reduced at the silicon surface by injecting holes into the valence band which are used to etch the semiconductor [Kooij, 1999]. The reduction of nitric acid during porous Si formation is a complicated reaction, invoking a step which is catalyzed by nitrite, one of the reaction products. Induction periods and irreproducibility are common problems with this form of etching.

Zhang et al. [Zhang, 1993] reported the formation of a porous luminescent layer when n-type Si in contact with a noble metal was illuminated in a HF solution containing oxygen. In this chapter, we show that p-type Si can be made porous in a similar way without illumination. In addition, we show that etching is caused by the formation of a galvanic element, in which the Si forms the anode and the metal forms the cathode. The factors determining the etch rate and the uniformity of the etched layer are described. Finally, the new etching technique is used to form n-type crystalline micromechanical structures.

5.2 Experimental

For all experiments <100>-oriented n-type or p-type silicon with a resistivity of 2-5 Ω cm was used. These samples were etched in a dilute HF (Merck) solution. In some experiments a surfactant (Triton X-100) or ethanol was used to prevent the formation of large hydrogen bubbles. In most experiments oxygen in the solution served as the oxidizing agent for the galvanic cell. In some experiments, the concentration of oxidizing agents was increased by adding ammonium peroxodisulfate ($(\text{NH}_4)_2\text{S}_2\text{O}_8$) or hydrogen peroxide (H_2O_2) to the HF solution. The choice of oxidizing agent concentration was somewhat arbitrary. These oxidizing agents are not reduced at p-type Si and do not cause the semiconductor to be etched chemically. The current-potential curves of Si in these solutions were similar to curves measured in HF solutions without additives.

All experiments were performed at room temperature. In Figure 5-1 the set-up is schematically shown. The area of the silicon electrode was 0.6 cm^2 and the edges were protected from the solution by a HF-resistant O-ring.

Fig. 5-1 Set-up used for electrochemical measurements.

Electrochemical experiments were performed with silicon, gold and platinum electrodes in HF solutions. For this purpose, a POS703 Bank potentiostat was used. The scan rate was typically 1 mV/s . The potential is quoted with respect to a saturated calomel electrode (SCE) or an Ag/AgCl electrode. The difference of 50 mV between the two standard redox potentials is neglected.

In some experiments, a galvanic element was formed on the wafer to etch the silicon without external contacts. The metal cathode was evaporated on the wafer with an e-beam in this case. The inert metal cathode consisted of a Au/Cr or Pt/Cr film with a thickness of $400/40 \text{ nm}$.

5.3 Principle of galvanic element formation

5.3.1 Anodic dissolution of silicon

In Chapter 3, current-potential curves are shown for silicon in a 1% HF solution. Here, the reaction mechanisms at the different potentials are briefly repeated. At potentials negative with respect to the open circuit potential a low cathodic current is observed with p-type Si. In this potential range the semiconductor is not dissolved. At potentials positive with respect to the open circuit value an anodic current indicates the dissolution of Si. The supply of holes to the surface is rate limiting and porous Si is formed. When a critical potential (V_p) is reached, a peak is observed in the current-potential curve and dissolution becomes limited by mass transport of hydrogen fluoride species to the Si; this is the electropolishing range [Zhang, 1989].

At potentials negative with respect to the OCP a large cathodic current is observed for n-type Si. This is due to the reduction of protons to hydrogen gas by conduction band electrons. Formation of porous silicon requires valence band holes and is not possible on moderately doped n-type Si in the dark. Upon illumination electron-hole pairs are generated. The holes are used to oxidize the silicon, while the electrons are measured in the external circuit as an anodic photocurrent, which is proportional to the light intensity. If the light intensity is sufficiently high, the anodic current-potential curve has the same form as that measured with p-type silicon (the curve is shifted to negative potentials).

5.3.2 Galvanic etching of silicon

The formation of a galvanic element can be understood on the basis of Figure 5-2. Current potential curves are shown for a p-type silicon electrode and for an inert metal electrode in a HF solution containing an oxidizing agent such as oxygen. At potentials negative with respect to the redox potential (V_{Ox}^{n+}/Red) the oxidizing agent is reduced at the metal electrode. At more negative potentials the current becomes independent of the potential and assumes a value I_b ; the reduction reaction is limited by the diffusion of the oxidizing agent to the metal surface. On scanning further to negative potentials, a current increase due to reduction of protons to hydrogen is measured.

Fig. 5-2 Schematic representation of galvanic cell formation. Curve (a) shows the current-potential curve for p-type Si in a HF solution with oxidizing agent Ox^{n+} . The open-circuit potential is denoted as OCP. Curve (b) is the corresponding curve for a noble metal sheet in the same solution. The diffusion-limited reduction current is denoted as I_b . Curve (c) is the current resulting from a higher oxidizing agent concentration. $V_{Ox^{n+}/Red}$ is the redox potential. When the Si and metal electrodes are connected, the couple assumes a rest potential V_b . The anodic and cathodic currents are equal in this case.

The curve for the Si electrode is the same as that shown in Chapter 3. When the metal electrode is connected to the silicon electrode the rest potential of the system assumes a value V_b between the open-circuit potential of the silicon (OCP) and the redox potential of the metal ($V_{Ox^{n+}/Red}$). At this rest potential, the silicon dissolution current and the reduction current are equal. The electrons required for the reduction reaction are supplied from the valence band, i.e. holes are injected into the valence band and give rise to etching of the semiconductor. Depending on the value of the cathodic current and the HF concentration, Si is either made porous ($V < V_p$) or is electropolished ($V > V_p$). From Figure 5-2 it is clear that reduction of the oxidizing agent must start at a potential positive with respect to the onset of anodic dissolution, i.e. $V_{Ox^{n+}/Red}$ must be positive with respect to OCP. The silicon etch rate can be increased by increasing the reduction current. This may be accomplished by raising the concentration of oxidizing agent, increasing the surface area of the inert

electrode or by enhancing diffusion of the oxidizing agent to the inert surface; i.e. stirring the solution. However, with the latter it is difficult to control the current accurately.

Similarly, n-type silicon may be etched galvanically. In the case of moderately doped material, illumination is needed for the generation of holes.

In Figure 5-3 the current-potential curves of a gold electrode (of approximately 4 cm^2) and a platinum electrode (of approximately 8 cm^2) in a 1% HF solution with different oxidizing agents are shown. Since we are interested in the reduction of the oxidizing agents only the scans to potentials negative with respect to the open-circuit potential (about 0.6 V) are given.

Fig. 5-3 *Current-potential curves for the reduction of oxidizing agents at noble metal electrodes: oxygen (a) and peroxodisulfate (b) at gold, oxygen (c) and hydrogen peroxide (d) at platinum.*

At the platinum electrode the diffusion limited range for oxygen reduction (curve (c)) is reached sooner than at gold (curve (a)). In an attempt to increase the reduction current (and eventually the rate of porous Si formation) peroxodisulfate ($0.03 \text{ M } (\text{NH}_4)_2\text{S}_2\text{O}_8$) was added to the solution. This resulted in a higher current (curve (b)). Hydrogen peroxide ($0.1 \text{ M H}_2\text{O}_2$) was also added for this purpose. On platinum, this resulted

in a drastic current increase (curve (d)). On gold, the reduction current (not shown in the figure) was even lower than that of oxygen.

The OCP of a silicon electrode was monitored when the Si was connected to a gold or platinum electrode. Figure 5-4 shows the measured potential-time curves and the experimental set-up.

Fig. 5-4 Measurement of the open-circuit potential versus time of a p-type Si electrode when it was connected to; Au in O_2 containing solution (a), Pt in the same solution (b) and Pt in H_2O_2 containing HF solution (c). On the right the experimental set-up is shown.

The sudden increase in potential corresponds to the point at which the connection was established. The shift in OCP agrees well with what one expects from the partial oxidation and reduction currents. A gold/silicon couple in a solution containing only oxygen gave the smallest change in rest potential. As predicted, the shift is larger for a platinum electrode. The shift is largest in the case of platinum/hydrogen peroxide. While in all other cases a brown coloured layer appeared at the silicon surface indicating formation of porous silicon, with platinum and hydrogen peroxide, silicon was etched without colour change, i.e. the semiconductor was electropolished. At about 0.5 V the potential is in the electropolishing range (see Chapter 3). The current generated by the galvanic cell is then limited by the diffusion of fluoride species to the exposed silicon surface. For oxygen and peroxodisulfate containing solutions, after connection is made the concentration of oxidizing agent at the metal surface decreases in

time from the initial 'bulk' value to a steady-state 'diffusion' value. In these cases the current is clearly limited by the diffusion of oxidizing agent to the metal surface.

5.3.3 Etch rate measurements

The etch rate of Si in galvanic contact with Pt was measured in a 5% HF solution containing oxygen from the air; the Pt/Si area ratio was 12. Afterwards, the porous layer was dissolved in a 1% KOH solution at room temperature. Results are summarized in Table 5-1. The steady state short circuit current measured between the two electrodes is also shown. In the case of a 5% HF solution without additives, the uniformity of the porous layer thickness was poor. The uniformity was improved by adding the surfactant Triton X-100 to the solution. The best results were achieved with ethanol. With an increased area ratio of 19 and a current density of about 1 mA/cm² we obtained an etch rate of 65 nm/min which is similar to etch rates obtained with conventional electrochemical etching. Care should be taken when these values are compared with the literature because the resistivity of the silicon substrate has a large influence on the etch rate.

Table 5-1 *Etch rate and current density obtained with Si/Pt galvanic couple in different HF solutions (area ratio = 12)*

HF solution	Average current density (mA/cm ²)	Etch rate (nm/min)	Uniformity
40% HF:water (1:7)	0.22	not measurable	poor
40% HF:water (1:7) and 2 drops Triton X-100	0.32	23	good
40% HF:water:ethanol (1:3:4)	0.64	38	very good

A higher etch rate (and current density) could be obtained with H₂O₂ addition. For the formation of porous layers the HF concentration must be sufficiently high to ensure that the dissolution reaction is not limited by fluoride diffusion resulting in uniform etching.

5.3.4 Examples of galvanically etched porous layers

A p-type silicon sample with a gold-coated back was etched in 5% HF for 5 minutes. The resulting porous layer is shown in Figure 5-5.

Fig. 5-5 Galvanically formed porous layer, (left) top view and (right) cross-section.

This layer is rather thin but porous layers with a thickness of 7 μm have been obtained using galvanic etching. Porous layers obtained galvanically show a clear photoluminescence visible to the naked eye in the dark. Similar results were obtained with n-type Si which was illuminated from the front.

Galvanic etching may also be used for formation of macroporous silicon. In Figure 5-6 the experimental set-up (developed by Ohji [Ohji², 1999] and a SEM photo of a typical result are shown. The silicon sample was illuminated with a white light source from the back [Lehmann, 1993]. At the front of the sample a grid of inverted pyramids which were obtained by etching in a KOH solution was exposed to a 5% HF, 1% H₂O₂ solution. The inverted pyramids served as starting points for the macropore formation. A separate Pt electrode was contacted to the back of the sample. Two separate electrodes were used instead of an on-chip metal layer, as this allowed for monitoring of the galvanic current.

Fig. 5-6 *Macroporous n-type silicon formed by galvanic etching. A Si sample and a Pt electrode were short circuited while the back of the sample was illuminated. The resulting deep macropores are clearly visible on the SEM photo*

In this case the Pt/exposed Si area ratio was about 40. The etch time was 15 minutes and an etch rate of about 2 $\mu\text{m}/\text{min}$ was achieved. For practical applications an area ratio of 40 may be difficult to realize. The ratio can be decreased when the oxidizing agent concentration is increased. In a next step, the metal cathode can be made on the silicon wafer by evaporation.

5.4 Galvanic etch stop

A simple structure was designed to demonstrate a galvanic etch stop in HF solutions. A p-type substrate was provided with an n-type epi-layer. The n-type mechanical structures were defined by a boron diffusion in the regions which had to be removed. Most of the n-type Si was covered with a silicon nitride layer. At the back of the p-type substrate a p⁺ layer was implanted. Finally, a Pt/Cr film was evaporated on the back. The Pt/exposed p-type Si area ratio was 21. A schematic of the structure is shown in Figure 5-7. This structure was etched in a 1% HF, 1% H₂O₂ solution in the dark for 135 minutes. In Figure 5-8 SEM photos of the results are shown. The thickness of the epi layer was 4 μm . After etching the thickness of the n-type mechanical structures was measured to be about 2 μm .

Fig. 5-7 Schematic of the galvanic etch stop demonstrator structure.

Fig. 5-8 SEM pictures of n-type silicon microstructures. Picture (a) shows a free-standing n-type silicon beam with a nitride layer on top. The n-type structures in picture (b), (c) and (d) are not fully underetched. In photo (b) the nitride layer has been stripped off. In photo (c) there is a gold/chromium film on top of the nitride layer. In photo (d) a cross-section is shown. Part of the n-type top layer has been etched away. This was an n+ implantation.

Since the junction is forward biased, holes are injected in the n-type layer which may cause etching of this layer. Moreover, the etching experiments were not performed under absolutely dark conditions. The etched depth of the p-type silicon was 23 μm . The selectivity between n-type and p-type silicon is $2/23 = 0.09$. Some n-type structures were covered with a gold/chromium layer. This did not enhance dissolution of the n-type layer. Parts of the n-type layer were provided with an n+ implantation. These were exposed to the etching solution and from photo (d) it can be seen that this layer has been etched away, as was expected from the Chapter 3.

5.5 Design rules for galvanic etch stop

Galvanic etching of silicon is achieved if reduction of the oxidizing agent in the solution starts at a potential positive with respect to the onset of anodic silicon dissolution. Therefore, the ohmic voltage drop in the galvanic element should be sufficiently low ($< 0.6 \text{ V}$ in 1% HF solutions). This means that the electrical contacts of the cathode to the silicon substrate should be placed sufficiently close to the etching area. This does not really impose a constraint on the design since usually a front-side etching process is used and the cathode can be made at the back of the sample. Therefore, the distance between the cathode contacts and the etching area is determined by the thickness of the wafer.

The etch rate may be increased by increasing the oxidizing agent concentration. If electropolishing of the semiconductor is not required, a relatively high HF concentration should be chosen. In this work, the concentration of HF was limited to 5% because at higher concentrations problems were encountered with the adhesion of the noble metals. In general, chromium proved more resistant to HF solutions than titanium. In oxygen saturated 1~5% HF solutions and in ammonium peroxodisulfate (0.03 M) containing solutions, porous layers were obtained when a metal/Si area ratio of 9~12 was used. If 0.1 M hydrogen peroxide was added to 1~5% HF solutions the silicon surface was electropolished. Once the galvanic cell current density is measured, the appropriate concentration can be chosen with the help of Figure 3-5 of Chapter 3.

5.6 Conclusions

Formation of porous silicon without external contacts can be achieved by galvanic etching in HF solutions. Contact between the silicon sample and a noble metal is required. The etch rate may be controlled by the metal/Si area ratio and the concentration of oxidizing agent in solution. The main advantage of the galvanic porous formation technique is that a special sample holder to contact the Si is not required. This makes the technique suitable for batch fabrication. Compared to stain-etched layers galvanically formed porous layers have better uniformity and thick layers are easily obtained. The technique may also be used for contactless fabrication of free-standing crystalline structures. Care should be taken to etch in complete darkness. The design rules for this etching technique are straightforward and do not impose serious constraints.

In this Chapter, a conventional pressure sensor and an accelerometer structure, both fabricated with a galvanic etch stop in TMAH solutions, are presented. The sensitivity of the pressure sensor was 150 (mV)/(V bar) in the range up to 20 mbar. Next, a conventional vibration sensor made with a front-side etching technique in TMAH solutions is described. The sensor was sensitive to vibration frequencies ranging from 45 kHz to 282 kHz (with a quality factor of typically 300). The non-uniformity of the resonant frequencies on one wafer was better than 5%. Finally, free-standing thick polysilicon structures suspended 10 μm above the substrate have been formed with a contactless galvanic etching technique in a HF, H_2O_2 solution. The thickness of these structures remained constant throughout the etching process demonstrating the high selectivity.

6.1 Introduction

Electrochemical etching in alkaline or HF solutions is commonly used for fabrication of integrated silicon micromechanical sensors. The bulk-micromachined pressure sensor [for example: Clark, 1979] and accelerometer [for example: Roylance, 1979] are well-known examples. At present, these sensors are fabricated in high volume using an electrochemically controlled pn etch stop. An important cause of yield-

loss in the fabrication process is the wafer holder required during etching. This also complicates batch fabrication of these devices. In the following subsection, an alternative contactless fabrication method is presented.

The conventional electrochemical pn etch stop in alkaline solutions may also be used in a front-side etching process. This simplifies the fabrication as double-sided alignment is not required. However, some groups have reported on anomalies during the underetching of the mechanical structures [Linden, 1989], [Marco, 1993], [Özdemir, 1992]. Although the structures could be released, the p-type Si was not completely removed depending on the initial dimensions. The cause for this effect is still unclear. In the following subsections, a contactless front-side etching technique to fabricate a vibration sensor based on freestanding single-crystal silicon cantilevers will be presented. Similar anomalies were encountered with the undercutting of the mechanical structures in this work.

Recently, some groups have reported on surface-micromachined structures with a large air gap [Artmann, 1999], [Gennissen, 1999]. The advantage over conventional surface micromachining is the elimination of vertical sticking. At present, the most convenient way to form the air gap is by removal of the top part of the substrate with electrochemical etching in HF solutions. We demonstrate the formation of similar structures with a contactless galvanic etching technique.

6.2 Pressure sensor

6.2.1 Operating principle and design

A conventional silicon pressure sensor consists of a thin flexible membrane and a solid rim [Middelhoek, 1989]. The solid rim is used to attach the fragile sensing element to the package. A pressure difference between the two sides of the membrane results in a deflection. The deflection can be measured using a capacitive read-out technique. The advantage of this technique is the low temperature sensitivity. The disadvantage is the need for a counter electrode. Usually, this is a glass wafer with an etched recess on which a metal is sputtered. The glass wafer is anodically bonded to the silicon chip. The pressure can also be measured using the piezoresistive effect, the change in resistivity with applied stress.

Resistors are placed on the bending element at the location where the change in mechanical stress due to deformation is highest. Usually, this is at the clamp of the moving part; i.e. at the edge of a membrane or at the base of a cantilever. A change in stress is measured as a change in resistance. With this method, a counter electrode is not required and the read-out electronics are simple. However, the disadvantage is a rather high temperature sensitivity. This approach was chosen for the pressure and vibration sensor presented in this Chapter.

Piezoresistive read out

The relative change of the resistance of a resistor implanted or diffused in a deflecting silicon membrane is expressed as [Middelhoek, 1989]:

$$\frac{dR}{R} \approx \frac{d\rho}{\rho} = \pi_{||} \cdot \sigma_{||} + \pi_{\perp} \cdot \sigma_{\perp} \quad (6-1)$$

where R is the resistance, ρ is the resistivity, $\sigma_{||}$ and $\sigma_{\perp}$ is the stress parallel and perpendicular to the resistor as a result of the deflection of the membrane, $\pi_{||}$ and $\pi_{\perp}$ are the parallel and perpendicular piezoresistive coefficients. These coefficients are a function of the crystal orientation of the silicon wafer and of the orientation of the resistors. In this case, (100)-oriented p-type silicon is used. As a result, the magnitudes of $\pi_{||}$ and $\pi_{\perp}$ are practically equal but of opposite sign. Furthermore, the coefficients have a maximum in the $\langle 110 \rangle$ -directions, while the magnitude is zero in the $\langle 100 \rangle$ -directions. Therefore, the resistors are always aligned to the $\langle 110 \rangle$ -directions. Usually, the piezoresistors are placed on the silicon membrane as shown in Figure 6-1 [Kim, 1981].

Fig. 6-1 *Standard configuration of the piezoresistors on a silicon membrane.*

The resistors are located as close as possible to the edge of the membrane and centered. The resistances $R1$ and $R2$ are equal. Since $\pi_{||} \approx -\pi_{\perp}$ and $\sigma_{||}$

of R_1 is equal to $\sigma_{\perp}$ of R_2 , and vice versa, the following relationship holds:

$$\frac{dR_1}{R_1} \approx -\frac{dR_2}{R_2} \quad (6-2)$$

The relative changes in resistance are equal but of opposite sign. Note that the resistors should not be too long since R_1 and R_2 are then subject to different stress and equation 6-2 is no longer valid. The area of the resistor is usually kept to a minimum by using several loops. Generally, the resistors are connected in a Wheatstone bridge configuration. In this case, the bridge output is proportional to the bridge supply voltage and dR_1/R_1 .

Process flow

The process flow of the pressure sensors made with a galvanic etch stop did not differ significantly from that of a conventional pressure sensor made with the electrochemically controlled pn etch stop (see for example [Kim, 1983]). The main difference was the large gold cathode which made contact to the n-epi layer.

First, a p-type wafer was provided with an n-type epi-layer of 4 μm . Boron was diffused through the epi layer to isolate the devices and to avoid high leakage currents from the edge of the wafer during etching. Next, boron was implanted to form the p+ piezoresistors. The sheet resistance of this layer was 25 Ω/square . An LPCVD silicon nitride layer of 100 nm was deposited on the front and back. At the back an etch mask was patterned in the nitride, while at the front holes for the cathode to n-type silicon and metallization to piezoresistor contacts were opened. Finally, a gold/chromium film of 400/40 nm was evaporated on the wafer. A lift-off process was used to define the metallization and the cathode area. An advantage of the process is that the gold layer was used both for the cathode of the galvanic element and the metallization for the chip. After a short 1% HF dip for 30~60 seconds, the wafer was ready for etching. It was immersed in a 25% TMAH solution at 80°C for 18 hours. Hydrogen evolution from the silicon surface was used as the etch-stop indicator. In Figure 6-2 a schematic of the resulting structure is shown.

Fig. 6-2 Schematic of the pressure sensor. The metallization to contact the piezoresistors and the cathode of the galvanic cell are both made in gold/chromium.

Design

The cathode was formed outside the perimeter of the membrane. In this way, the gold/chromium layer did not influence the mechanical behaviour of the thin membrane. The cathode to n-epi contacts were never spaced more than 2 mm from the etch-stop area to avoid a high bulk resistance. The membrane size ranged from 1 by 1 mm to 4 by 4 mm with a seismic mass in the centre. On one wafer, the area ratio between the gold cathode and the n-type Si etch-stop area was about 48. In Chapter 4, it was concluded that this area ratio is sufficient to ensure an etch stop for a 25% TMAH solution at 80°C which contains only oxygen from the air. The active area (= the area of the sensing elements with the piezoresistors and metallization) on a die of 1 by 1 cm occupied only 36% of the die area. The package density was rather low (108 sensors with a chip size of 5 by 5 mm were fabricated per 4 inch wafer) and should be increased. This should be possible when oxidizing agents such as ferricyanide are added to the solution. In this case, the gold layer should be made pinhole free since alkaline ferricyanide solutions etch chromium adhesion layers.

6.2.2 Results

After the etch stop the wafers were sawn into chips of 5 by 5 mm, each consisting of one membrane. The pressure sensor chips were glued on a special header, kindly provided by John Dancaster of Lucas NovaSensor. In Figure 6-3, SEM photos of a mounted pressure sensor are shown. The spots on the membrane resulted from the sawing process. This is generally undesirable and can be avoided by spinning on resist before sawing. The resist is later removed in acetone or nitric acid.

Fig. 6-3 *Picture of the pressure sensor chip mounted on a header (left) and SEM photo of the chip (right). The light-grey area is gold (Au).*

A cross-section of a membrane is shown in Figure 6-4.

Fig. 6-4 *Cross-section of a membrane obtained with the galvanic etch stop. The thickness is 4.7 μm .*

The output was measured as a function of the pressure at room temperature. The pressure was regulated using a Druck DPI 520 pressure controller. The inaccuracy of the applied pressure was 0.05% Full Scale (35 mbar). The result is shown in Figure 6-5.

Fig. 6-5 Output of the pressure sensor as a function of the applied differential pressure. The linear range is about 20 mbar.

As can be seen, the sensor is not linear in the range from -500 to 1000 mbar. This was even more obvious for the negative differential pressure range (with higher pressure at the back of the membrane). Generally, the total stress in a membrane under pressure consists of two components; bending stress and membrane stretching stress [Suzuki, 1987], [Tufte, 1962]. If the sensor is operated in the linear range, the total stress is determined only by the bending stress as the membrane is not stretched (the deflection of the centre of the membrane must be small compared to the thickness). The values of the bending stress in the positive and negative ranges are of equal magnitude but of opposite sign and are given by [Clark, 1979]:

$$\sigma \sim \left(\frac{L}{h}\right)^2 \cdot P \quad (6-3)$$

where L is the side length of the membrane, h is its thickness and P is the pressure. The sensitivity increases with the square of the aspect ratio (L/h).

If the sensor is operated in the non-linear range, an additional membrane stretching stress is present which is always tensile, independent of the sign of the applied pressure. Therefore, the total stress in the positive range becomes larger than the total stress in the negative range. In this case, equation 6-3 is no longer valid. From Figure 6-5 it can be seen that at

about -150 mbar, the membrane stretching stress becomes more important than the bending stress; the sensor is operated far from the linear range. The linear operating pressure range may be estimated by [Djuric, 1990], [Suzuki, 1987],:

$$P < \frac{20 \cdot E \cdot h^4}{a^4 \cdot 12 \cdot (1 - \nu^2)} \tag{6-4}$$

where P is the pressure, E is the Young's modulus, h is the membrane thickness, a is $L/2$, ν is the Poisson ratio. In this range, the deflection is less than three tenths of the thickness. Using this equation, the linear deflection range for our membranes was estimated to be 20 mbar. Finite-element simulations (ANSYS) predicted that the deflection of our membranes at this pressure was about 1.7 μm . An additional cause for the non-linearity is the non-linear piezoresistance of the resistors [Yamada, 1982]. Therefore, many authors report on linear ranges which are lower than those estimated with equation 6-4, [Kim, 1983], [Suzuki, 1987]. This implies that the value of 20 mbar is probably too high. The sensitivity in the linear range was estimated as 150 (mV)/(V bar).

The resistance of one resistor was measured at various temperatures as well as the offset of the bridge output. The result is shown in Figure 6-6 . The resistance at room temperature was about 4.8 k Ω . The bridge voltage was 5 V.

Fig. 6-6 The offset of the output and the resistance of one resistor as a function of the temperature.

The temperature coefficient of resistance (TCR) is $6.1 \Omega/^{\circ}\text{C}$, which is $0.13\%/^{\circ}\text{C}$ at room temperature. The temperature coefficient of the offset (TCO) is $0.013 \text{ (mV)/(V }^{\circ}\text{C)}$ or estimated as $0.1 \text{ mbar}/^{\circ}\text{C}$. The measured parameters of the pressure sensor were compared to those from the literature (Table 6-1).

Table 6-1 *Pressure sensor specifications compared to those from the literature.*

Reference	Dimensions (mm x mm x μm)	Linear range (mbar)	Sensitivity (mV/V bar)	TCR at room temp. ($\%/^{\circ}\text{C}$)	TCO (mbar/ $^{\circ}\text{C}$)
Our sensor	1x1x4.7	20	150	0.13	0.1
[Kim, 1983]	1x1x23	1000	10	0.2	-3.2
[Kloeck, 1989]	0.5x0.5x10	400	15	-	1.1

The sensitivity of our sensor was higher than the values reported by Kim and Kloeck. From equation 6-3 an even higher value could be expected since the aspect ratio was more than 4 times larger. However, since we used a rather high doping concentration the piezoresistive coefficients $\pi_{||}$ and $\pi_{\perp}$ in equation 6-1 were not optimized [Tufte, 1962]. This also lowered the TCR of our resistors. Finally, the TCO of our sensor was lower than the values reported by Kim and Kloeck.

Accelerometer structures were also fabricated with the galvanic etching technique. A process flow for a micromachined accelerometer differs only slightly from that of a pressure sensor. Etching from the back results in a seismic mass suspended on a membrane. The shape of the seismic mass is defined by corner compensation structures. In Figure 6-7, SEM photos of a seismic mass are shown. The front of the sensor chip is shown in Figure 6-8. Note that the resistors are located at the edges of the membrane and the mass. In a next step, the membrane is perforated using a dry etching technique. Typically, this results in a mass suspended with four thin beams. This last step was not performed since part of the wafer surface was covered by gold which is usually not allowed in a standard clean room. However, the possibility of fabricating conventional piezoresistive bulk-micromachined accelerometers with the galvanic etch stop has clearly been demonstrated.

Fig. 6-7 *Seismic mass fabricated with different corner compensation structures. The corner compensation of the mass on the left was obviously more effective.*

Fig. 6-8 *Front of the accelerometer structure. The seismic mass shown in Figure 6-7 is suspended on a membrane.*

6.3 Vibration sensor

6.3.1 Operating principle and design

Generally, a vibration sensor consists of micromechanical elements with different resonant frequencies. The sensor is mounted on a vibrating body

under test. When the vibration frequency approaches the resonant frequency of one element, the element starts to resonate. The deflection can be detected capacitively or piezoresistively. In this work, we chose the latter detection method. The piezoresistors were placed at the clamp of the micromechanical elements, where the magnitude of the stress was highest. A reference sensor was placed on the rim of the chip. The resistors were arranged in a half Wheatstone bridge configuration.

The simplest micromechanical element is a cantilever. The first mode resonant frequency of a cantilever is given by [Middelhoek, 1989]:

$$f_0 \approx 0.16 \cdot \sqrt{\frac{E}{\rho}} \cdot \left(\frac{h}{L^2}\right) \quad (6-5)$$

where E is the Young's modulus ($1.7 \cdot 10^{11}$ Pa for (100)-Si in the $\langle 110 \rangle$ -direction), ρ is the density of the cantilever material (2330 kg/m^3 for silicon), h is the thickness of the cantilever and L is the length of the cantilever. With an array of cantilevers of different length, a range of frequencies can be detected [Benecke, 1985]. Other shapes may also be used for the vibration-sensitive elements. For example, a paddle may be formed at the end of the cantilever [Peeters, 1997]. This lowers the resonant frequency and increases the sensitivity of the microelements.

Process flow

The vibration sensor was made in a process similar to that of the pressure sensor. A schematic is shown in Figure 6-9. An advantage of this process over that of the pressure sensor is that double-sided alignment was not required. All masks are patterned at the front of the wafer. This reduces the misalignment from $10 \text{ }\mu\text{m}$ to less than $0.2 \text{ }\mu\text{m}$.

An n-type layer of $4 \text{ }\mu\text{m}$ was deposited on a p-type wafer. A deep boron diffusion perforated the n-type epi layer and defined the cantilevers. A p+ implantation was used to form the piezoresistors. An LPCVD silicon nitride layer of 100 nm was deposited. Next, holes were opened in the nitride for the cathode to n-type epi contacts and a shallow n+ layer was implanted to yield a low contact resistance. Finally, the etch holes and the contacts to the piezoresistors were opened in the nitride layer. The etch holes exposed only the diffused p-type layer. Next, the structure was dipped in a 1% HF solution for 30 sec. Finally, the structure was ready for etching in a 25% TMAH solution at 80°C .

Fig. 6-9 Schematic of the vibration sensor. N+ implantations were used to make low resistance cathode to n-epi layer contacts.

Design

Different types of cantilever arrays consisting of small beams (width 20 μm , length 200-600 μm , referred to as type S) or large beams (width 80 μm , length 1.1-1.7 mm, referred to as type L) were designed. On some beam tips a paddle of 300 by 300 μm was added to lower the resonant frequency. The design of the small beams and the resonant frequency measurements were performed by Robert Kazinczi. The resonant frequencies could be measured piezoresistively and optically [Kiesewetter, 1992], [Petersen, 1979], as the chips were designed to fit in an Atomic Force Microscope (AFM) head [Kazinczi, 1999].

The cathode to n-type Si contacts were never located more than 1 mm from the etch-stop area. On most sensors, these contacts were placed over the whole length of the cantilevers. In this case, the distance between the cathode and the etch-stop area was defined by the thickness of the cantilever.

On one wafer 36 dies each with 5 vibration sensors were made. The active area on one die occupied 26% of the die area. The package density was even lower than that of the pressure sensor (144 vibration sensors of type S with a chip size of 1.6 by 4.3 mm and 36 sensors of type L with a chip size of 2.3 by 4.6 mm per 4 inch wafer). The initial n-type silicon exposed to the solution was negligible. This means that the initial cathode to n-type Si area ratio was extremely high. As the etching proceeded this area ratio decreased since more n-Si became exposed. Once parts of the n-type Si were exposed, an anodic oxide grew on the surface after which it remained passive. A surface which has been passivated should, in principle, draw

only a low current. However, in Chapter 4 we observed a rather high passive current after the etch stop. This high current was also observed in this case.

6.3.2 Results

Figures 6-10 to 6-14 show the resulting cantilevers and paddles after etching. Figure 6-10 shows the two types of cantilever arrays.

Fig. 6-10 *Different types of cantilevers obtained after 14 hours of etching in a 25% TMAH solution at 80°C.*

Figure 6-11 shows the cantilevers of type S after 1 and 4 hours of etching. Note that the beams are not completely undercut after 4 hours. The gold cathode covered the entire cantilever on the left photo. In this case the cathode to n-type Si spacing was defined by the thickness of the beams.

Fig. 6-11 *S-type cantilevers obtained after 1 hour of etching (left photo), and after 4 hours of etching (right photo). The beams on the left were provided with a gold strip.*

Figure 6-12 shows a close-up of the cantilevers of type S after 4 hours of etching. Note the typical shape of the tip.

Fig. 6-12 *S-type cantilevers obtained after 4 hours of etching. Photo (a) shows one beam which is not yet fully underetched. Photos (b), (c) and (d) show a close-up of the tip. Note the typical shape of the diffusion pattern.*

Figure 6-13 shows cantilevers of type S obtained after 14 hours of etching. The beams are completely released. Figure 6-14 shows L-type cantilevers.

Resonant frequency measurement

The S-type chips were glued on a piezoelectric actuator (with around 0.1 μm displacement for 10 V driving voltage) which was excited over a range of frequencies. The output of one cantilever could be monitored using a conventional probe station and an oscilloscope. At resonance, a peak could be observed in the output signal. Six different sensors from different parts of the same wafer were measured; the mean resonance frequency and the relative maximum deviation from the mean are summarized in Table 6-2.

Fig. 6-13 *S-type cantilevers obtained after 14 hours of etching (a). Photo (b) shows a close-up of the base of a beam. The piezoresistor can be seen. Photo (c) shows the base of two neighboring beams. The top beam is not yet fully underetched. Photo (d) shows the tip of a beam. The thickness of the beam is not uniform.*

Fig. 6-14 *L-type cantilevers obtained after 14 hours of etching. The photo on the right shows a close-up of one beam; the piezoresistor is clearly visible. The spots are dust from sawing the wafer.*

Length	Calculated	Mean f	Rel.
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When the calculated and measured resonant frequencies are compared, it

slope of this line the effective beam thickness may be estimated to be about $8\text{ }\mu\text{m}$. However, the line does not go through the origin. This may be caused by the fact that the beam thickness is not uniform (see following discussion).

Fig. 6-15 The resonant frequency as a function of $(1/L)^2$.

The shape of the cantilevers was studied to understand the deviation from the expected results. From the SEM photos shown in previous Figures 6-10 to 6-14 it was rather difficult to determine the exact shape. Some samples were broken to reveal the under side of the cantilevers. The results of this study are given in Figures 6-16 and 6-17.

Figure 6-16 shows the shape of the S-type cantilevers. The silicon wafer was etched for 14 hours in a 25% TMAH solution at 80°C . Overetching for 2 hours did not result in a measurable change in shape. The shape of all beams was similar. The same thickness of p-type Si was left under the n-type structures and in all cases the tip of the beam was almost entirely undercut resulting in a thickness of about $5\text{ }\mu\text{m}$. The base had a typical thickness of $10\text{--}13\text{ }\mu\text{m}$, while the thickest part of the beam was $20\text{--}23\text{ }\mu\text{m}$.

Figure 6-17 shows the shape of L-type cantilevers. Only the two longest beams of $1700\text{ }\mu\text{m}$ and $1500\text{ }\mu\text{m}$ were not completely underetched after 14 hours. After 2 hours overetching, they were still not completely free. The rest of the beams (all smaller than $1400\text{ }\mu\text{m}$) were completely released. All free beams had a similar shape. The tip, consisting of a paddle of 300 by $300\text{ }\mu\text{m}$, was about $5\text{ }\mu\text{m}$ thick. The base of the beam was about $10\text{--}13$

μm , while the thickest part of the beam was $20\sim 23\ \mu\text{m}$. The clamping of the beams was underetched about $15\ \mu\text{m}$ in the horizontal direction. Note that the edge of the etch cavity has a typical shape. Different (111)-planes appeared near the surface. The conventional (111)-planes appeared at a depth of about $20\ \mu\text{m}$. Similar effects have been observed by Duch [Duch, 1998]. At present, the cause for this is unclear.

In the case of front-side etching of silicon nitride beams [Petersen, 1982] or highly boron-doped structures [Benecke, 1985] all underlying silicon was removed. Therefore, we conclude that incomplete undercutting in the case of an electrochemical etch stop (such as the galvanic etch stop) is not due to the anisotropy of the etchant [Linden, 1989]. Some groups have reported on incomplete removal of p-type Si with the electrochemical pn etch stop [Linden, 1989], [Marco, 1993], [Özdemir, 1992] and with the fabrication of membranes (Chapter 4) we encountered similar problems. Up to now, a detailed study to explain this effect has not been undertaken. A possible explanation is that compared to an electrochemical etch process from the back, the shape of the depletion layer is less uniform. Moreover, during the release etching of the beams, the area of the exposed non-passivated p-type Si under the n-type beams may become so small that the reverse leakage-current present in the pn-junction leads to a premature etch stop. This may explain why some parts of the beam are completely undercut (the tip) while other parts (near the base) are left with a thick p-type silicon layer.

Fig. 6-16 *S*-type cantilever array. Some *p*-type Si is left under all beams (a). Photo (b) shows a close-up of one beam. The tip has a thickness of about 5 μm. Photos (c) and (d) show the longest (600 μm) and shortest (200 μm) beam. The shapes are similar. Photo (e) shows the side view of a typical beam. Schematic (f) shows the typical shape of all beams. The tip of the beam is almost entirely defined by the *n*-type epi layer (about 5 μm) while the base has some *p*-type Si left (about 13 μm). The thickest part (about 20-23 μm) of the beam is located near the base.

Fig. 6-17 *L*-type cantilevers. Photo (a) shows a beam of 1200 μm . Note the shape of the base. Photo (b) shows a beam of 1700 μm . It is not completely underetched because the etch time was too short. Photo (c) shows the paddle of the beam displayed in (a). Photo (d) shows a close-up of this paddle. The thickness is about 5 μm . Photo (e) shows a side-view of a beam. Photo (f) shows the underetching at the edge of the etch cavity. The thickness is about 5 μm and the underetching in horizontal direction is 15 μm . Photos (e) and (f) show a typical shape of the underetching at the edges of the cavity.

6.4 Free-standing thick polysilicon structures

6.4.1 Process and results

In this subsection the potential of the galvanic etch stop in HF solutions is demonstrated. As discussed in Chapter 5, it may be difficult to obtain a high selectivity between the n-type epi layer and the underlying p-type substrate when long etching times are used with a galvanic etch stop. Due to the injection of holes from the p-type Si, some of the n-type epi layer may also be etched. A better electrical insulation may be achieved by using a polysilicon on oxide layer as described in [Artmann, 1999], [Gennissen, 1999]. The process flow is shown in Figure 6-18.

Fig. 6-18 Process flow for galvanic etch stop in HF, H_2O_2 solution using thick polysilicon on oxide.

A silicon oxide layer of 300 nm was grown on a p-type silicon substrate with ohmic back. An LPCVD polysilicon layer of 200 nm was deposited

followed by 10 μm deposition in an epitaxial reactor. Next, the layer is patterned using reactive ion etching. A Pt/Cr layer of 400/40 nm is evaporated on the back. Finally, the structure is ready for contactless etching in a HF, H_2O_2 solution. Compared to standard surface micromachining where only the oxide layer is etched away, this method results in a larger air gap under the mechanical structures which reduces vertical sticking.

The wafer was etched in a 1-5% HF, 1% H_2O_2 solution. The Pt- exposed p-type bulk area ratio on one wafer was approximately 5. The results are summarized in Table 6-3.

Table 6-3 *Etch rates obtained in different HF solutions.*

etching solution	etch rate (nm/min)
1% HF, 1% H_2O_2	90
5% HF, 1% H_2O_2	230

Figures 6-19 and 6-20 show SEM photos of free-standing structures obtained with this etching technique. These structures were designed by Paul Gennissen [Gennissen, 1999]. The samples were etched in a 5% HF, 1% H_2O_2 solution for 45 minutes. Etching was performed under normal laboratory illumination. The thickness of the epipoly mechanical layer did not decrease during etching.

In Figure 6-19 a stress measurement rotating structure is shown [Goossen, 1996]. A compressive or tensile stress results in a change in length of the clamped beams, which in turn results in a rotation of the freestanding beam. In this case a rotation could not be measured, indicating the low stress in the epipoly layer. Figure 6-20 clearly shows that the surface morphology after etching is not smooth. These layers were galvanically electropolished. Similar results were obtained with conventional electrochemical etching [Gennissen, 1999].

Fig. 6-19 *Epipoly stress measurement structure which is suspended 10 μm above the substrate. Photo (b) and (c) show a magnification of the centre and tip of the rotating structure, demonstrating the typically low mechanical stress in this layer.*

Fig. 6-20 *Epipoly structures suspended 10 μm above the substrate. The top photo shows a stress measurement structure. There are three cubic silicon structures under the free-standing bridge. These were released from other parts of the wafer. On the bottom photo an electrostatic actuator is shown.*

6.5 Discussion and conclusions

A conventional bulk-micromachined pressure sensor and an accelerometer structure have been fabricated with a galvanic etch stop in TMAH solutions. The process flow is similar to that of the conventional process; only one non-standard process step is involved. This is the evaporation of a noble metal layer, such as gold or platinum. The device package density of a wafer which is etched in a TMAH solution containing oxygen from

the air is still rather low. This may be improved by adding oxidizing agents to the solution.

Conventional piezoresistive vibration sensors have been made with a front-side etching process and a galvanic etch stop in TMAH solutions. The p-type Si under the n-type epi layer which defined the cantilevers was not completely etched away. The result was a rather poorly defined shape which made it difficult to predict the resonant frequency in the design phase. The non-uniformity of the resonant frequency of the structures was less than 5%. Another problem encountered with this technique was that relatively long ($>1400\text{ }\mu\text{m}$) and wide ($>80\text{ }\mu\text{m}$) structures required long etch times for complete release. This also results in considerable underetching of the clamping of the structures, which in turn lowers the resonant frequency and may introduce a mechanical coupling to neighboring resonating structures. These problems may be avoided by using an etching process from the back and galvanic etch stop to create a membrane. In a second step, the membrane may be perforated by dry etching to obtain highly uniform cantilevers [Peeters, 1997]. The disadvantage of this process is the need for double-sided alignment.

Free-standing thick polysilicon structures suspended $10\text{ }\mu\text{m}$ above the substrate have been fabricated with a galvanic etch stop in HF, H_2O_2 solutions. The only non-standard process step is the evaporation of platinum. This technique imposes virtually no constraints on the design of the micromechanical structures as the platinum film is deposited at the back of the wafer. A low area ratio of platinum to exposed p-type silicon requires the addition of more H_2O_2 and a higher concentration of HF to accomplish a higher etch rate. Once the design is fixed the appropriate concentrations are determined experimentally.

In general, all devices described in this Chapter may be fabricated in a batch process as wafer holders or external electrodes are not used. Since diffusion of oxidizing agent to the cathode is important the wafers should not be spaced too close together. For 4 inch wafers a spacing of a few centimeters should be sufficient.

Conclusions

7

In this thesis, galvanic etching of silicon in alkaline and hydrofluoric acid etching solutions for formation of micromechanical structures is described. The following can be concluded:

- *Silicon which is immersed in an alkaline solution containing oxygen can be passivated by connecting it to a noble metal.*

This etch-stop phenomenon has been described on the basis of galvanic element formation. It was more pronounced in TMAH solutions than in KOH solutions; i.e. a lower noble metal/silicon area ratio was required, as silicon is more easily passivated in the former etchant.

- *Selective etching of the p-type layer in a pn-wafer is accomplished by connecting only the n-type layer to a noble metal sheet. The metal film can be formed by gold/chromium evaporation.*

In this way, n-type crystalline silicon membranes of about 4.7 μm have been fabricated using an etching process from the back in 25% TMAH solutions. A highly uniform thickness was obtained. Similarly, n-type crystalline beams have been fabricated using a front-side etching process in the same solution. The thickness of each beam was highly non-uniform; the tip was almost entirely defined by the n-type layer while the p-type Si at the base was not completely etched away. A possible solution to obtain

a uniform thickness would be to align the beams along the $\langle 100 \rangle$ direction (rotated 45° with respect to the wafer flat). In this way, underetching of the beams proceeds faster and the etching process itself proceeds in a more uniform fashion. Note that in this case the clamp of the beams is also underetched. The shapes of similar beams on the same wafer showed a good uniformity: The maximum relative deviation from the average resonant frequency was less than 5%.

- *The galvanic etch stop can be used to fabricate micromechanical membrane-based devices such as a pressure sensor and an accelerometer structure.*

The package density of the devices is rather low and therefore the process is not directly usable for high volume production. Possible ways to improve this include the addition of an oxidizing agent such as ferricyanide to the TMAH solution or bubbling of oxygen through the etching solution.

The difficulty with the former solution is that the concentration of ferricyanide should be carefully controlled. This is difficult since the ferricyanide is also reduced at the silicon surface, as a result of which its concentration decreases during the process. An even more serious problem is the fact that alkaline ferricyanide solutions are corrosive to adhesive metal layers such as chromium and titanium; the cathode will not survive long etching times.

With the bubbling of oxygen, care should be taken that the oxygen bubbles come in physical contact with the metal cathode. Otherwise, the cathodic reduction current remains relatively low. In this case, the cell current would not be sufficient to accomplish an etch stop.

- *Galvanic etching may also be used with other etching systems such as HF.*
- *Porous layers can be formed on p-type silicon connected to a noble metal in HF solutions. On n-type silicon illumination is required to accomplish pore formation.*

The etch rate has been increased by using an oxidizing agent such as hydrogen peroxide. By adjusting the HF and oxidizing agent concentration, the etch rate and the mode of etching (electropolishing or pore formation), can be controlled.

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- *Micromechanical structures can be formed with a large air gap through removal of the top part of the p-type silicon bulk by connecting the bulk to a noble metal sheet.*

When the structures are made of n-type Si in direct contact with the p-type bulk, the selectivity for long etch times was about 0.1. Better results were obtained when the mechanical structures were formed in a thick polysilicon-on-oxide layer. There are no limiting design constraints since the metal layer may be deposited at the back.

The structures presented in this thesis may all be fabricated with conventional etch-stop techniques. However, one can take advantage of the unique properties of the galvanic etch stop and fabricate a range of new structures. In alkaline solutions, this technique allows for complete electrical isolation between the etch-stop area and the rest of the wafer. This may be used for fabrication of low-doped n-type silicon comb-drive structures in an alkaline etchant. A noble metal can be deposited on top of the comb-structures, to form the cathode of the galvanic element. Note that for this process, the cathode/etch stop area ratio is quite low, which will require addition of an oxidizing agent or oxygen bubbling. Another possibility is a dissolved wafer process in which many gold-coated n-type Si structures are released from a p-type substrate.

Finally, it can be concluded that the galvanic etch stop provides a useful and interesting additional tool to existing bulk-micromachining techniques. The technique may also be used with semiconductors other than silicon. The only requirement is that the onset of anodic dissolution is negative with respect to the onset of oxygen reduction on a noble metal.

Conclusions

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Summary

This thesis describes a novel etching technique for the fabrication of silicon micromechanical structures and sensors. These structures are formed in a single etch step without the use of high doping concentrations, external electrodes or wafer holders. The method is based on a galvanic effect and the operating principle is explained with existing models of semiconductor electrochemistry.

For the electrochemical etching of Si in alkaline solutions with an external power source, a sufficiently high positive potential and sufficiently high anodic current result in the growth of a passivating anodic oxide layer. In HF solutions, a positive potential and anodic current result in the formation of a porous layer or in the uniform etching of the top layer. These effects are commonly used to induce an etch stop; the etching stops automatically at a pn junction resulting in a micromechanical structure with a uniform thickness. Galvanic etching shows strong resemblance to electrochemical etching. In the case of galvanic etching, the current and voltage are generated within the structure itself, eliminating the need for external power source and contacts. Because the external power source is no longer required, the galvanic etch stop is easier to implement in batch processes compared to the previously mentioned etch-stop techniques.

This novel technique is demonstrated by the fabrication of different micromechanical structures, such as membranes and free-standing cantilevers. With galvanic etching, a noble-metal cathode is required with a large area. This cathode contacts either the n-type silicon that needs to be passivated in the case of TMAH solutions, or the p-type silicon that needs to be etched in the case of HF solutions. The disadvantage of such a large cathode area is that less space remains for the actual mechanical structures. This results in a low package-density of structures on the chip. These limitations are more severe for TMAH than for HF solutions, since with HF solutions, the cathode may be placed at the back of the wafer. Moreover, with these solutions a low galvanic cell current is not critical. With TMAH solutions, the density of structures may be increased by adding strong oxidizing agents.

The novel technique has also been used for the fabrication of a sensitive piezoresistive pressure sensor, a vibration sensor and an epipoly stress-

measuring structure. The membrane thickness of these pressure sensors has the same uniformity as that obtained with the conventional techniques. The vibration sensor is based on an array of free-standing microcantilevers of different length, which are released from the front. Because the etching stops before the pn junction, the shape of each beam is not uniform. However, the shape is constant over the whole wafer and reproducible. The fabrication of free-standing epitaxial structures in HF solutions results in a well-defined uniform thickness.

Galvanic etching is a useful and interesting tool for silicon micromachining. Future research may include other applications of this technique and its extension to other semiconductors.

Samenvatting

Dit proefschrift beschrijft een nieuwe etsmethode voor de fabricage van silicium micromechanische structuren en sensoren. De structuren worden gevormd in één etsstap, zonder gebruik te maken van een hoge dotering, externe elektroden en speciale etshouders. De methode is gebaseerd op een galvanisch effect en het werkingsmechanisme wordt verklaard met behulp van de bestaande theorie van de halfgeleider-elektrochemie.

Bij het elektrochemisch etsen van Si in alkalische oplossingen met een externe bron resulteert een voldoende hoge positieve potentiaal en een voldoende hoge anodische stroom in de groei van een passiverende anodische oxidelaag. In HF oplossingen resulteert een positieve potentiaal en anodische stroom in de vorming van een poreuze laag of in het uniform weg etsen van de toplaag. Deze effecten worden doorgaans gebruikt om een etsstop te induceren; het etsen stopt automatisch op een pn junctie, waardoor er een micromechanische structuur verkregen wordt met een uniforme dikte. Galvanisch etsen vertoont sterke gelijkenis met elektrochemisch etsen. De spanning en stroom worden echter in de structuur zelf gegenereerd, waardoor externe bron en contacten overbodig worden. Vanwege het ontbreken van de externe bron, is de galvanische etsstop gemakkelijker te implementeren voor batch-processen vergeleken met de eerder genoemde etsstop technieken.

De nieuwe techniek wordt gedemonstreerd aan de hand van de fabricage van verschillende micromechanische structuren, zoals membranen en vrijstaande balkjes. Bij het galvanisch etsen is voor de kathode een edelmetaal nodig met een groot oppervlak. Deze kathode contacteert of alleen het n-type silicium dat gepassiveerd moet worden in geval van TMAH oplossingen, of het p-type silicium dat weggeëtsd moet worden in geval van HF oplossingen. Het nadeel van een groot kathode-oppervlak is dat er minder ruimte overblijft voor de mechanische structuren. Dit resulteert in een nogal lage dichtheid van structuren op de chip. In het geval van TMAH oplossingen zijn de beperkingen belangrijker dan in het geval van HF oplossingen. De reden hiervoor is dat bij HF oplossingen de kathode aan de achterkant van de plak kan worden geplaatst. Verder is het bij deze oplossingen niet kritisch als de galvanische cel een kleine stroom

levert. In TMAH oplossingen kan de dichtheid van de structuren nog worden opgevoerd door sterke oxidatoren toe te voegen.

De nieuwe etstechniek is ook gebruikt voor de fabricage van een gevoelige piëzoresistieve druksensor, een trillingssensor en een structuur voor het meten van mechanische spanning in dunne lagen. De membraandikte van deze druksensoren heeft dezelfde uniformiteit als die verkregen met de conventionele technieken. De trillingssensor is gebaseerd op vrijstaande microbalkjes van verschillende lengte, die vrijgeëet worden vanaf de voorzijde. Doordat het etsen voortijdig stopt, is de vorm van elk balkje grillig. Het blijkt dat die vorm wel constant over de hele plak en goed reproduceerbaar is. De fabricage van vrijstaande epipoly structuren in HF oplossingen resulteert in een goed gedefinieerde uniforme dikte.

Galvanisch etsen vormt een nuttig en interessant alternatief voor het bewerken van silicium plakken. Toekomstig onderzoek kan zich richten op andere toepassingen van de techniek en op het gebruik van andere halfgeleiders.

Acknowledgments

I would like to thank the following people for making it possible and enjoyable to perform the research described in this thesis:

Prof. Paddy French, for his support and for giving me the freedom to define my own project. Lina Sarro, for her advice on the project and the processes. Prof. John Kelly, for his interest and large input in the project. Prof. Middelhoek and Prof. Huijsing, the chairmen of the group.

Robert Kazinczi, Kari Hjelt, Peter Szczaurski and Lucien Breems, for making live at work less serious. Evert Oemar, for his help with the project (section 4.4.2. was based on his graduation work). Sandra Bellekom, Wilko Kindt, Paul Gennissen and Zhixiong Xiao, my roommates who made sure there were no quiet days at work. In our room there were often helpful discussions on all possible subjects. Orla O'Halloran, Frederik Cremer, Ulrike Dauderstädt, Hiroshi Ohji, Davies de Lima Monterio, Serhat Sakarya, Hans Goosen, Dafina Tanase, Piet Trimp, Ger de Graaf, Maureen Meekel, Jeroen Bastemeier, Evelyn Sharabi, Ingeborg Egmond, Sabine de Boer, Willem van der Sluijs, and all the other members of the Electronic Instrumentation Lab. and DIMES for the helpful and friendly working atmosphere. A special thanks to Wim van der Vlist and Jan Groeneweg for processing and advice, and Adrie Looijen for the metal deposition.

Peter Bressers, Stefan Kooij, Xinghua Xia and the other members of the Debye Institute for helping me with the electrochemical measurements.

Dr. Stephen Prosser and Prof. Popovic for arranging the stay at Lucas, Birmingham and EPFL, Lausanne, respectively. Andre Bossche for his help with the project in general and STW for the financial support of the project (no. DEL55.3780). Mirjam Nieman, for correcting the English of Chapter 3.

And finally I would like to thank Kim, my father & mother, Ramses, Jesse & Svati for their support.

Acknowledgments

List of publications

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About the Author

Colin Ashruf was born in Delft, The Netherlands, on February 15, 1973 and lived in Paramaribo, Suriname, up to 1983. He started his study in electrical engineering at the Delft University of Technology in 1991 and received his masters degree in 1995. Afterwards, he spent four months at the Advanced Engineering Centre of Lucas in Birmingham, UK where he worked in the sensor group. Since 1996 he has been at the Laboratory for Electronic Instrumentation at the Delft University of Technology, working towards a Ph.D. degree in the field of wet etching for sensor fabrication. During his first year he spent four months at the Swiss Federal Institute of Technology (EPFL) in Lausanne, Switzerland, where he worked on a piezo-tunneling strain sensor.