High Quality SiO₂ Deposited at 80°C by Inductively Coupled Plasma Enhanced CVD for Flexible Display Application

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In this article, we investigated the high quality SiO₂ deposited at 80°C by inductively coupled plasma enhanced chemical vapor deposition (CVD). The interface trap density of $1.48 \times 10^{10} \text{ cm}^{-2} \text{ eV}^{-1}$ and breakdown voltage of 5.6 MV/cm were realized successfully despite the low deposition temperature. Thin film transistors (TFTs) have been fabricated under 100°C by excimer laser annealing. The electron mobility can reach $225 \text{ cm}^2/\text{V s}$. The interface density of SiO₂ is comparable with that of thermal oxide. The high quality gate oxide is very suitable for fabricating high performance TFTs for large-area flexible displays on plastics.

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High performance single-grain Si thin film transistors (TFTs) with a field effect mobility of $600 \text{ cm}^2/\text{V s}$ are realized with location-controlled Si grains and with a maximum process temperature of 350°C.¹ Their properties are comparable with those using silicon on insulator wafers. For high performance TFTs, a high quality gate oxide with an interface quality as good as that of a thermal oxide is required to meet the high quality Si. However, the difficulty lies in obtaining those SiO₂ at ultralow temperature, i.e., a temperature below 100°C, for application in a flexible display on a plastic integrated with system circuits.

There are many methods to deposit an oxide at around 400°C such as by tetraethoxysilane (TEOS),² electron cyclotron resonance plasma-enhanced chemical vapor deposition (ECR-PECVD),³ reactive plasma deposition,⁴ etc. ECR can realize SiO₂ with a D_{it} of $2 \times 10^{10} \text{ eV}^{-1}$. However, those processes cannot realize good interface property at a deposition temperature. At an ultralow temperature, the SiO₂ layer tends to become less dense and more porous, hence, low quality interface with Si because of less chemical reaction at the growing surface. Inductively coupled plasma chemical vapor deposition (ICP-CVD) has many advantages, such as independent control of ion energy and current, high electron concentration, and wide pressure range. These can allow less ion damage to the Si surface and a high density of reactive radicals. Thus, it can deposit high quality SiO₂ with good interface property. However, the deposition temperature reported so far is 250°C, which is still too high for the plastic electronics.

In this research, we investigated SiO₂ deposited by ICP-CVD at 80°C. The interface trap density of $1.48 \times 10^{10} \text{ cm}^{-2} \text{ eV}^{-1}$ and breakdown voltage of 5.6 MV/cm were realized successfully despite the low deposition temperature. High quality SiO₂ was used for fabricating TFTs under 100°C. The field mobility for the electron was able to reach $225 \text{ cm}^2/\text{V s}$.

Experimental

We used a Sentec ICP-CVD deposition system, which consists of a plasma generator, a planer-type inductor, and a ceramic chamber. Radio-frequency (rf) power with a frequency of 13.65 MHz was applied to the inductor. ICP was generated in a ceramic chamber that is encircled by an inductive coil. RF power was applied to the coil with a frequency of 13.56 MHz. Plasma was excited by an electric field generated by a transformer from the rf current in a conductor. The changing magnetic field of the conductor induces an electric field in which the plasma electrons are accelerated. Oxygen was fed through an up gas shower and subjected to the plasma, while the SiH₄ (diluted in 95% He gas) was fed through a gas ring just above the heat chuck and reacted with oxygen radicals to form SiO₂. The standard process condition is as follows: 9.2 sccm O₂ flow, 150

sccm SiH₄/He flow, 2 Pa pressure, and 500 W rf power. The oxygen plasma treatment was for 5 s, which was introduced just before the deposition to oxidize the surface and ensure a high oxygen/silane ratio at the interface during growth. It also stabilized the plasma before the deposition. The deposition time was 60 s. The deposition rate was 1.5 nm/s in the standard conditions. The total range of uniformity across a 4 in. wafer was 6.4%. So for an average thickness of 100 nm SiO₂ deposited by ICP on a 4 in. wafer, the thickness variation is $\pm 3.2 \text{ nm}$. Different depositions of SiO₂ were also performed with the pressure range of 2–8 Pa and SiH₄/He flow of 80–240 sccm.

Metal-oxide-semiconductor capacitors were processed on p-type (100) silicon wafers with a resistivity of 5–10 $\Omega \text{ cm}$. After the wafer dip etching in 0.55% HF solution for 4 min to remove the native oxide, SiO₂ was deposited under various conditions. We have also deposited TEOS by PECVD at 350°C for comparison. Then aluminum was sputtered on the oxide surface and patterned onto an area of 0.1225 cm^2 by photolithography and reactive ion etching. The back side of the wafer was also covered with Al to form an ohmic contact. All the processes were kept under 100°C.

The SiO₂ film was used as a gate insulator for the TFTs. The TFTs used in this experiment were fabricated with the μ -Czochralski process⁵ under 100°C. A 250 nm amorphous Si was sputtered at 100°C. Then the amorphous Si was crystallized by an excimer laser with an energy density of $900 \text{ mJ}/\text{cm}^2$. The grain size was 4 μm after laser crystallization.⁶ After patterning the Si island, 100 nm SiO₂ oxide was deposited by ICP-CVD and a 675 nm Al gate was sputtered. After patterning the gate, the source and drain were doped with $10^{16} \text{ ions}/\text{cm}^2$ by phosphorus implantation at 30 keV for the n-channel. The dopants were activated by an excimer laser at $300 \text{ mJ}/\text{cm}^2$. The channel width and length were 1 μm .

Results and Discussion

Capacitance–voltage (*C-V*) measurement was used to investigate the interface characteristic using an LCR meter (Agilent 4282A). Interface density D_{it} was calculated from low (100 Hz) and high frequency (1 MHz) *C-V* measurements. Figure 1 shows the *C-V* characteristic of SiO₂ deposited at the standard conditions. The good matching of the low and high frequency *C-V* in the accumulation and transition regions indicates a high quality interface with Si. The interface trap density as a function of the applied gate voltage [$D_{it}(V_{AG})$] within the bandgap is extracted from the high and low frequency *C-V* characteristics.⁷ The D_{it} was calculated to be $1.48 \times 10^{10} \text{ cm}^{-2} \text{ eV}^{-1}$ and the threshold voltage (V_{th}) was 0 V. The D_{it} of TEOS was measured and calculated to be $8 \times 10^{10} \text{ cm}^{-2} \text{ eV}^{-1}$ in the same way, which is much higher than the ICP oxide deposited at a low temperature. Figure 2 shows D_{it} as a function of deposition pressure. By increasing the pressure from 4 to 8 Pa, the D_{it} increases from 1.48×10^{10} to $7.27 \times 10^{10} \text{ cm}^{-2} \text{ eV}^{-1}$. When the pressure is lowered to 2 Pa, the D_{it} increases to $1.24 \times 10^{11} \text{ cm}^{-2} \text{ eV}^{-1}$. The

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Figure 1. (Color online) High and low C - V characteristics of SiO_2 deposited under the standard conditions.

pressure causes the plasma region to expand or contract during the deposition. The lower deposition pressure increases the ion energy, which causes damage to the Si surface. However, the higher deposition pressure decreases the ion energy, which is inefficient for the decomposition of SiH_4 . The best pressure condition is 4 Pa. Figure 3 shows D_{it} as a function of the gas flow of SiH_4/He . The oxygen flow is fixed to be 9.2 sccm. The D_{it} increases when the SiH_4/He flow is either increased or decreased. The best gas flow rate is $\text{O}_2:\text{SiH}_4/\text{He} = 9.2:150$.

The current-voltage (I - V) characteristic of SiO_2 was measured by an Agilent 4156C. Figure 4 shows the current density (J) as a function of the applied electrical field for the SiO_2 deposited with the standard deposition conditions. Resistivity, defined by a resistance at an electrical field (E) of 1 MV/cm, is $4.7 \times 10^{14} \Omega \text{ cm}$. Breakdown field (E_B), defined by an E value when J is at $1 \times 10^{-6} \text{ A/cm}^2$, is 5.6 MV/cm.

Figure 5 shows the transfer characteristic (I_D - V_G) of TFTs. The field effect mobility μ_{Fec} evaluated in the linear region at low V_D was estimated to be $225 \text{ cm}^2/\text{V s}$.

Conclusions

We investigated high quality SiO_2 deposition at 80°C by ICP-CVD. D_{it} was measured by high and low frequency C - V . We optimized the deposition condition and got a D_{it} lower than $1.48 \times 10^{10} \text{ cm}^{-2} \text{ eV}^{-1}$, which is comparable to that of a thermal oxide.

Figure 2. Interface density of SiO_2 (D_{it}) as a function of pressure.

Figure 3. Interface density of SiO_2 (D_{it}) as a function of SiH_4/He gas flow.

Breakdown field strength and resistivity were 5.6 MV/cm and $4.7 \times 10^{14} \Omega \text{ cm}$, respectively. The high quality SiO_2 was used for

Figure 4. Current density (J) as a function of applied electric field (E) of the SiO_2 film deposited under the standard conditions.

Figure 5. (Color online) Transfer characteristic (I_D - V_G) of TFTs fabricated under 100°C .

fabricating TFTs. The process temperature was under 100°C. The field mobility for the electron can reach 225 cm²/V s.

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