Enabling Low-Distortion Varactors for Adaptive Transmitters

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Abstract—A varactor diode configuration is presented for the implementation of low-distortion tunable matching networks, phase shifters, and filters. The configuration is based on varactors with an “exponential” $C(V)$ relation in antiseriess configuration with specific control voltage harmonic loading conditions. The resulting network combines a high capacitance tuning range with relatively low control voltages and excellent linearity. The linearity is independent of the applied control voltage and does not degrade at low tone spacing, which is ideal for the realization of adaptive transmitters and modulators. A specific $N_d x^{-2}$ varactor doping profile is required for exact third-order intermodulation (IM3) cancellation. The remaining distortion is dominated by the much smaller fifth-order nonlinearities. The required impedance levels of the harmonic terminations are studied in terms of the maximum modulation bandwidth for which the proposed configuration remains linear. The doping profile optimization for quality factor, tuning range, and breakdown voltage is discussed. For experimental verification, the proposed varactor configuration has been implemented using a silicon-on-glass technology. The measurements demonstrate IM3 cancellation and indicate a superior linearity for modulated signals up to 10-MHz bandwidth.

Index Terms—Adaptive systems, band switching, impedance matching, low distortion, tunable filters, tuners, varactors.

I. INTRODUCTION

NEXT-GENERATION wireless systems, such as multi-mode transceivers and “cognitive radios,” require circuit techniques that facilitate RF adaptivity. Some examples of adaptive circuits include tunable filters [1], [2] and tunable matching networks for low-noise and power amplifiers [3], [4]. An ideal tuning element for these applications will exhibit extremely low loss, low dc power consumption, high linearity, ruggedness to high voltage and high current, wide tuning range, high reliability, very low cost, low area usage, and will be continuously tunable with a high tuning speed.

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p-i-n diodes or GaAs pseudomorphic HEMTs (pHEMTs) are widely used today for these challenging applications. However, these solutions are considered to be too expensive, or consume too much dc power, to be an acceptable long-term solution for cost and performance sensitive applications.

This limitation has triggered an intensive search for alternatives that do not suffer from the drawbacks of traditional approaches. One example is the microelectromechanical systems (MEMS) capacitor [5]–[7], which, in its most popular implementation, is able to switch between two fixed capacitance values. MEMS capacitors provide a very high quality factor and extraordinarily high linearity, but they require nonstandard processing and packaging techniques, high control voltages, and their reliability and switching speed are still poor compared to semiconductor-based solutions. Other proposed tuning techniques, based on voltage-variable dielectrics [8], exhibit similar drawbacks of manufacturability and performance.

In view of this urgent need, more simple tunable elements like varactor diodes would seem to be a logical choice for implementing RF adaptivity. However, their inherently nonlinear behavior does not comply with modern communication standards, characterized by high peak-to-average power ratios, and their related quality factors are usually too low at the microwave frequencies of interest for most demanding applications.

In order to overcome these drawbacks, varactor diode-based circuit topologies—along with a high performance silicon-on-glass varactor diode process technology—have been presented [9], [10]. These proposed varactor configurations can act as variable capacitors with ideally zero or extremely low distortion [9]–[15]. A brief description of these two previous low-distortion varactor configurations is given as follows.

- The distortion-free varactor stack [11]–[15] is based on an antiseriess connection of two identical uniformly doped varactors (capacitance power law coefficient $n = 0.5$), which use an infinitely high impedance as center-tap connection. Under these conditions, all distortion components at the RF terminals are perfectly canceled, yielding a distortion-free operation.
- The high tuning range varactor stack [9] is a combined antiseriess/antiparallel topology of four hyperabrupt varactor diodes [16] (capacitance power law coefficient $n > 0.5$), which uses two infinitely high center-tap impedances. At the RF terminals, the resulting even and third-order distortion products are cancelled through a proper selection of the varactor area ratio.

Fig. 1. Schematic for the Volterra analysis of the antiseriess varactor diode circuit.

Although very good results have been achieved with the configurations above, their practical implementations still have linearity constraints for complex modulated signals or other signals with narrow tone spacing. This is caused by the severe requirements for the center-tap impedance, which should approximate infinity when the tone-spacing approaches zero. Due to the requirement of these very high center-tap impedances, rapid modulation of the capacitance value of the distortion-free varactor stack and high tuning range varactor stack becomes problematic. Parasitic leakage currents of the diodes can also cause voltage drops over this center-tap impedance, yielding an undesired shift of the intended capacitance value.

The novel high-linearity narrow tone-spacing varactor stack presented in this study aims to overcome these limitations. This new configuration exhibits improved linearity for narrowband signals, little sensitivity to leakage currents, higher capacitance control range, and lower control voltages. These improvements will make it perfectly suitable for the implementation of linear tunable filters, matching networks, and/or modulators.

This paper is organized as follows. The theory of operation for the narrow tone-spacing varactor stack is given in Section II. The requirements on doping profile and its optimization for tuning range, breakdown voltage, and quality factor are discussed in Section III. The influence of IM5 distortion on the linearity is considered in Section IV. A comparison of this new configuration with the distortion-free varactor stack is done in Section V. The practical implementation issues related to process deviation are discussed in Section VI. In Section VII, a silicon-on-glass implementation of the proposed varactor is given, together with measurements to support the theory, followed by a conclusion in Section VIII.

II. THEORY OF OPERATION

The novel high-linearity narrow tone-spacing varactor-stack configuration is based on a Volterra analysis of the circuit shown in Fig. 1. As a measure of the varactor linearity, we consider the third-order intermodulation (IM3) current flowing through the varactor diodes at frequency $(2f_1 - f_2)$.

The low-frequency impedance of the center tap is set to zero ($Z_c(f_2 - f_1) = 0$), while this center-tap impedance is set to infinity at the higher harmonics. Using general Volterra series techniques [17], the resulting IM3 at a narrow tone spacing

$[(f_2 - f_1)/f_1 \approx 0]$ for this specific varactor configuration can be achieved, namely,

$$\text{IM3} \Big|_{Z_c(s=0)=0} = \left| \frac{(3c_0c_2 - 2c_1^2)\hat{A}^2}{2c_0^2(s_{\text{RF}}c_0Z_s(-s_{\text{RF}}) - 2)(s_{\text{RF}}c_0Z_s(s_{\text{RF}}) + 2)^2} \right| \quad (1)$$

where

$$c_0 = C(V_R) \quad (2)$$

$$c_1 = \frac{1}{2} \frac{dC(V_R)}{dV_R} \quad (3)$$

$$c_2 = \frac{1}{6} \frac{d^2C(V_R)}{d^2V_R} \quad (4)$$

are the capacitance Taylor coefficients of each varactor diode with V_R being the reverse applied voltage with a positive value, $Z_s(s)$ is the source impedance, s_{RF} is the complex RF center frequency ($j\omega_{\text{RF}}$) of the two-tone signal, and $\hat{A}$ represents the voltage amplitude of the source signal.

By setting (1) to zero, we can enforce IM3 cancellation, and we find an exponential $C(V_R)$ relation for the varactors, i.e.,

$$C(V_R) = a_1 \exp(-a_2 V_R). \quad (5)$$

In this relation, a_1 and a_2 indicate the integration constants, which add some flexibility to the solution. Note that any choice of a_1 and a_2 with positive values will satisfy (1), yielding perfect cancellation of the IM3 distortion component. For this low distortion to be achieved in practice, there must be a *low-impedance* path (relative to the ac impedance of the varactor capacitance itself) between the center node c and two RF terminals (a and b) of the varactor stack at low frequency ($f_2 - f_1$). At the same time, there must be a *high-impedance* path for the high-frequency components (fundamental and higher harmonics) of the impedance between the center node c and two RF terminals (a and b) of the varactor stack. When these conditions are met, a very high linearity tunable capacitance is achieved between the RF terminals of the varactor stack.

Note that the condition for IM3 cancellation (numerator of (1) equal to zero) only demands a functional relation between the Taylor coefficients, which is fully satisfied by using varactors with an exponential $C(V_R)$ relation. Consequently, the achieved IM3 cancellation neither depends on the value of the reverse bias voltage, nor the surrounding circuitry [note, for example, that Z_s does not appear in the numerator of (1)]. Therefore, this low-distortion tunable capacitive element can be applied in any circuit topology (including series configuration), provided that the designer takes the proper measures to guarantee the low-impedance paths for the baseband components between the center node c and the RF terminals (a and b), while loading of the center node for higher frequencies should be avoided. The resulting component will also exhibit excellent in-band linearity for the typical wireless complex modulated signals. Linearity restrictions with respect to the bandwidth of these signals (e.g., $B \gg 10$ MHz) only arise when the baseband short circuit between the center node and RF terminals fails to provide

Fig. 2. Required varactor doping profile of the narrow tone-spacing varactor stack, to achieve the exponential $C(V_R)$ relation. The black dashed line shows the restriction on the doping level of the “spacer” layer due to the sheet resistance (see Appendix A). The solid line represents the ideal doping profile (see Appendix B).

a sufficiently low impedance, a phenomenon we will discuss in Section V.

III. DOPING PROFILE AND PERFORMANCE COMPROMISE

A. Doping Profile

Based on a Volterra-series analysis and the solution of (1), the desired capacitance–voltage relation for ideal IM3 cancellation was determined in (5). The next step is to determine the required doping profile. For this purpose, we assume a one-sided junction (e.g., a Schottky diode) and solve for the doping profile using [16]

$$N(x) = \frac{C(V_R)^3}{e\epsilon_s} \left(\frac{dC(V_R)}{dV_R} \right)^{-1} \quad (6)$$

where

$$x = \frac{\epsilon_s}{C(V_R)}. \quad (7)$$

Making use of these relations, it can be shown that the required doping profile for an exponential capacitance voltage relation is

$$N(x) = N_d x^{-2} \quad (8)$$

in which N_d is a doping concentration constant to be defined and x is the distance from the metallurgical junction. It should be noted that this result is singular for $x = 0$, and measures to avoid this singularity must be taken. In order to explain how the doping profile should be defined, we consider Fig. 2.

In this figure, the ideal doping profile is indicated by the solid line. Since we cannot provide an infinitely high or extremely low doping concentration, this limits the validity of the $N_d x^{-2}$

relationship between x_{low} and x_{high} . Therefore, we define the useful capacitance tuning range (T_{tune}) since the capacitance is inversely proportional to the distance x , i.e.,

$$T_{\text{tune}} = \frac{C_{\text{max}}}{C_{\text{min}}} = \frac{x_{\text{high}}}{x_{\text{low}}}. \quad (9)$$

To maintain the “exponential” $C(V_R)$ relation, a spacer layer (Region 1 in Fig. 2) is required in order to satisfy the $N_d x^{-2}$ doping versus depth relation with respect to the metallurgical junction position (e.g., a doubling in distance to the metallurgical junction should result in one-fourth the doping concentration). To avoid reduced breakdown voltage, quality factor, and capacitance tuning range (T_{tune}), the normally depleted spacer layer should not significantly increase the electric field. To achieve this, the doping concentration of this spacer layer must be kept low with respect to $N(x_{\text{low}})$. This is analyzed in Appendix A, resulting in a lower bound on the effective sheet resistance of this spacer layer.

Here we assume for reasons of simplicity that the low doped spacer layer consumes the total built-in voltage of the junction, while the applied voltage is used to deplete the $N_d x^{-2}$ region. As a result, the exponential $C(V_R)$ relation of the fabricated diode (see Appendix B) is given by

$$C(V_R) = \frac{A\epsilon_s}{x_{\text{low}}} \exp \left(-\frac{\epsilon_s}{eN(x_{\text{low}})x_{\text{low}}^2} V_R \right) \quad (10)$$

where A is the area of the capacitor and the constant ($A\epsilon_s/x_{\text{low}}$) represents the zero-bias capacitance value.

Although, in principle, we can always choose an appropriate doping concentration of the spacer layer to make (10) valid, some practical implementations might use an even lower doping of the spacer layer. In this situation, the depletion distance (x'_{low}) at zero applied voltage can be larger than x_{low} , as shown in Fig. 2, and consequently, the $C(V_R)$ relation has to be modified to (Appendix B)

$$C(V_R) = \frac{A\epsilon_s}{x'_{\text{low}}} \exp \left(-\frac{\epsilon_s}{eN(x_{\text{low}})x_{\text{low}}^2} V_R \right). \quad (11)$$

The formulation above indicates that the zero-bias capacitor value is now $A\epsilon_s/x'_{\text{low}}$, which will reduce the capacitance tuning range by a factor of $x'_{\text{low}}/x_{\text{low}}$ for the same maximum depletion depth (x_{high}). Note that although the tuning range is reduced, the exponential $C(V_R)$ relation remains, and the IM3 distortion cancellation condition is still valid. In addition, due to the same doping profile in the $N_d x^{-2}$ region, the exponent coefficient a_2 in (5) is unchanged. Later in this paper, we investigate the doping profile constraints for practical varactor implementations, which exhibit deviations from the ideal profile.

B. Varactor Diode Performance Tradeoffs

Based on the above equations, we can optimize the tuning range and quality factor of the varactor for a maximum reverse applied voltage ($V_{R-\text{max}}$). The maximum operation voltage ($V_{R-\text{max}}$), series resistance R , and quality factor at zero applied

voltage ($Q|_{V_R=0}$) of the varactor are given by

$$V_{R\_max} = \frac{eN(x_{low})x_{low}^2}{\varepsilon_s} \left(\ln \frac{x_{high}}{x_{low}} \right) \quad (12)$$

$$R|_{V_R=0} = \int_{x_{low}}^{x_{high}} \rho(x) \frac{dx}{A} = \frac{1}{Ae\mu_n N(x_{low})x_{low}^2} \left(\frac{x_{high}^3}{3} - \frac{x_{low}^3}{3} \right) \quad (13)$$

$$Q|_{V_R=0} = \frac{\left| \frac{1}{j\omega C} \right|}{R|_{V_R=0}} = \frac{3e\mu_n N(x_{low})}{\omega \varepsilon_s \left[\left(\frac{x_{high}}{x_{low}} \right)^3 - 1 \right]} \quad (14)$$

where μ_n is the electron mobility.

Since the increase of the electric field due to the lightly doped spacer layer can be neglected, we can use the electric field at the boundary of the lightly doped region (Region 1 in Fig. 2) and the $N_d x^{-2}$ region (Region 2 in Fig. 2) to estimate the peak electric field when the capacitor is just fully depleted ($V_R = V_{R\_max}$), which is given by

$$E_{full\_depletion} = \frac{eN(x_{low})x_{low}^2}{\varepsilon_s} \left(\frac{1}{x_{low}} - \frac{1}{x_{high}} \right) \leq E_{breakdown} \approx 6 \times 10^5 \text{ V/cm}. \quad (15)$$

Based on (9) and (12)–(15), the quality factor at zero bias can be rewritten as

$$Q|_{V_R=0} = \frac{3\mu_n \ln(T_{tune})}{\omega V_{R\_max}(T_{tune}^3 - 1)} \left(\frac{T_{tune} E_{full\_depletion}}{T_{tune} - 1} \right)^2. \quad (16)$$

Since the quality factor at zero bias is proportional to the square of $E_{full\_depletion}$ for a given tuning range and maximum reverse applied voltage, the quality factor can be optimized by dimensioning the varactor such that $E_{full\_depletion} = E_{breakdown}$, which is, for silicon, approximately $6 \times 10^5 \text{ V/cm}$ [16]. Consequently, the maximum reverse applied voltage to deplete the varactor should be chosen close to the breakdown voltage of the varactor. Using this approach, the maximum achievable quality factors at zero bias (Q_{opt}) for different V_{R_max} and tuning ranges C_{max}/C_{min} are listed in Table I for a silicon implementation.

As indicated by (16), for a given fixed tuning range (T_{tune}), the optimized quality factor (Q_{opt}) is inversely proportional to the maximum operation voltage (V_{R_max}). The quality factor can be further improved through the use of wide bandgap materials like GaAs and GaN since these materials allow higher electric fields at the device junction and typically provide higher mobilities, enabling even higher quality factor values.

TABLE I
OPTIMIZED CALCULATED QUALITY FACTOR AT 2 GHz FOR GIVEN
TUNING RANGE (T_{tune}) AND V_{R_max} ($\mu_n = 1000 \text{ cm}^2/\text{V} \cdot \text{s}$)

Tuning Range (T_{tune})	$V_{R\_max}=5 \text{ V}$	$V_{R\_max}=10 \text{ V}$	$V_{R\_max}=20 \text{ V}$	$V_{R\_max}=40 \text{ V}$
3	$Q_{opt}=1634$	$Q_{opt}=817$	$Q_{opt}=408$	$Q_{opt}=205$
	$a_2=0.22 \text{ V}^{-1}$	$a_2=0.11 \text{ V}^{-1}$	$a_2=0.055 \text{ V}^{-1}$	$a_2=0.028 \text{ V}^{-1}$
6	$Q_{opt}=206$	$Q_{opt}=103$	$Q_{opt}=52$	$Q_{opt}=26$
	$a_2=0.36 \text{ V}^{-1}$	$a_2=0.18 \text{ V}^{-1}$	$a_2=0.09 \text{ V}^{-1}$	$a_2=0.045 \text{ V}^{-1}$
9	$Q_{opt}=66$	$Q_{opt}=33$	$Q_{opt}=16$	$Q_{opt}=8$
	$a_2=0.44 \text{ V}^{-1}$	$a_2=0.22 \text{ V}^{-1}$	$a_2=0.11 \text{ V}^{-1}$	$a_2=0.055 \text{ V}^{-1}$
12	$Q_{opt}=30$	$Q_{opt}=15$	$Q_{opt}=7$	$Q_{opt}=4$
	$a_2=0.50 \text{ V}^{-1}$	$a_2=0.25 \text{ V}^{-1}$	$a_2=0.12 \text{ V}^{-1}$	$a_2=0.062 \text{ V}^{-1}$
15	$Q_{opt}=16$	$Q_{opt}=8$	$Q_{opt}=4$	$Q_{opt}=2$
	$a_2=0.54 \text{ V}^{-1}$	$a_2=0.27 \text{ V}^{-1}$	$a_2=0.14 \text{ V}^{-1}$	$a_2=0.070 \text{ V}^{-1}$

IV. INFLUENCE OF FIFTH-ORDER INTERMODULATION (IM5) DISTORTION ON LINEARITY

A. Fifth-Order Volterra Series Analysis

Although the exponential $C(V_R)$ relation is very effective in cancelling the IM3, and all even distortion products are canceled by the symmetric antiseriess varactor configuration, IM5 is still present. In the following analysis of the fifth-order distortion, we use the same termination conditions at the center tap as for the IM3 cancellation, i.e., $Z_c(f_2 - f_1) = 0$, while $Z_c(f)$ is infinity for all other frequency components. Next, we substitute the $C(V_R)$ relation from (5) into the IM5 formulation. To simplify the analysis, we assume $\Delta f \rightarrow 0$ and $Z_s(S) \rightarrow 0$, yielding the IM5 products that appear at the IM3 frequencies $2f_1 - f_2$ and $2f_2 - f_1$, namely,

$$\text{IM5} \approx \frac{5}{48 \times 2^4} a_2^4 \hat{A}^4 \quad (17)$$

where $a_2 = -\varepsilon_s / (eN(x_{low})x_{low}^2)$ is the exponential coefficient of $C(V_R)$ relation (5) and $\hat{A}$ is the amplitude of the two-tone test signal at the fundamental frequencies. In order to be consistent with our further discussions, we replace $\hat{A}$ by V_{RF_peak} , which represents the peak amplitude of the two-tone input voltage signal. Hence, (17) becomes

$$\text{IM5} \approx \frac{5}{48 \times 2^4} a_2^4 \left(\frac{V_{RF\_peak}}{2} \right)^4. \quad (18)$$

Based on (18), the fifth-order input intercept point (IIP5) can be expressed as

$$\text{IIP5} \approx 4 \cdot \left(\frac{48}{5} \right)^{1/4} \frac{1}{a_2} = \frac{7.04}{a_2}. \quad (19)$$

Note that the IIP5 is independent of the applied control voltage at the center pin and only depends on the grading coefficient a_2 , which can be chosen freely to adjust the tuning range. Practical values of a_2 are in the range of 0.028 to 0.54 V^{-1} (see Table I), yielding IIP5 values of 12 – 256 V . Since the IM5 drops at the rate of 80 dB per decade, outstanding linearity can be achieved for even modest IIP5 values.

Fig. 3. Definition of effective tuning range. Note that by plotting $\ln(C)$ versus V_R , our desired exponential $C(V_R)$ relation appears as a straight line. This property will be used later to evaluate practical implementation of the varactor devices.

B. Compromise Between Linearity, Quality Factor, V_{R_max} , and Effective Tuning Range

The discussion in Section III did not account for the signal swing when calculating tuning range limits. In practical situations, the RF voltage swing will reduce the effective tuning range. For these reasons, it is useful to repeat the capacitance tuning range analysis for large-signal operation by including breakdown, forward biasing, and linearity constraints.

In order to maintain acceptable linearity, both varactor diodes in the stack must remain reverse biased during large-signal operation, and consequently, the useful range of capacitance variation will be reduced by the magnitude of the applied RF signal (Fig. 3). For this reason, the tuning range of Section III is replaced by the effective tuning range, which is a function of V_{R_max} and V_{RF_peak} . Since the magnitude of the RF input signal is V_{RF_peak} and the RF impedance between node c and d in Fig. 1 is high, the RF voltage across each individual diode is roughly half of V_{RF_peak} . Hence, the dc-bias voltage at the center tap must be higher than $V_{RF\_peak}/2$ to avoid forward biasing and it must be lower than $V_{R\_max} - V_{RF\_peak}/2$ to avoid breakdown.

As illustrated in Fig. 3, when the diode is biased at $V_{RF\_peak}/2$, the corresponding capacitor value is C_{max} , when the diode is biased at $V_{R\_max} - V_{RF\_peak}/2$, the corresponding capacitor value is C_{min} . Therefore, the effective tuning range (T_{tune_eff}) can be written as

$$\begin{aligned} T_{tune\_eff} &= \exp[a_2(V_{R\_max} - V_{RF\_peak})] \\ &= T_{tune} \exp(-a_2 V_{RF\_peak}) \end{aligned} \quad (20)$$

where T_{tune} is the original tuning range defined in (9). From (20), the $C(V_R)$ exponential a_2 can be expressed as a function of V_{R_max} , V_{RF_peak} , and T_{tune_eff} as follows:

$$a_2 = \frac{\ln(T_{tune\_eff})}{V_{R\_max} - V_{RF\_peak}}. \quad (21)$$

Fig. 4. Tradeoff of breakdown voltage, linearity, quality factor (solid lines), and effective tuning range (GaAs material with $\mu_n = 6000 \text{ cm}^2/\text{V} \cdot \text{s}$) for an RF signal with: (a) 2-V and (b) 15-V amplitude. Note that V_{R_max} must be larger than V_{RF_peak} to avoid clipping and forward bias.

Substituting the formulation above into (20), the IM5 can be written as

$$\text{IM5} = 4 \cdot 20 \log \left(\frac{\ln(T_{tune\_eff})}{7.04(V_{R\_max} - V_{RF\_peak})} V_{RF\_peak} \right) \text{ dBc}. \quad (22)$$

Based on (14)–(16) and (20), the optimized quality factor at zero bias (Q_{opt}) of the varactor can be rewritten as a function of V_{R_max} , V_{RF_peak} , and T_{tune_eff} . Therefore, we can plot the effective tuning range, quality factor, and V_{R_max} for different V_{RF_peak} values, as shown in Fig. 4. In order to give an indication of the achievable performance, the calculation of Fig. 4 is based on the mobility of GaAs ($\mu_n = 6000 \text{ cm}^2/\text{V} \cdot \text{s}$). For the silicon implementation, since the critical field at breakdown ($E_{breakdown}$) is within 10% of that of GaAs [16], one can approximate the quality factor by simply dividing the quality factor of GaAs by a factor of 5–6.

Fig. 4 shows the tradeoff between the quality factor and peak RF voltage. For example, if V_{RF_peak} is small (e.g., 2 V), we can achieve a quality factor of 400 for a device with a breakdown voltage of 12 V, an IM5 limited linearity of -110 dBc, and effective capacitance tuning range of 4:1 [see Fig. 4(a)].

In the case of a larger RF signal amplitude (e.g., 15 V), high tuning range, linearity, and high breakdown voltage can still be achieved at the cost of higher control voltages and a lower quality factor [see Fig. 4(b)].

V. PERFORMANCE COMPARISON WITH UNIFORMLY DOPED VARACTOR DIODES

A. Linearity Comparison

We claimed earlier that our varactor stack is distortion “free” (through IM3 cancellation) at narrow tone spacing; however, in practice, the IM5 distortion is the limiting factor. The task now is to compare the linearity of our novel varactor stack with traditional uniformly doped diodes. For this purpose, we use the distortion-free varactor-stack topology [12], which is also designed for high linearity performance.

Before comparing the linearity, the tuning range and maximum operation voltage should be normalized. Here, for comparison, we use a varactor stack with an effective zero-bias capacitance (a_1) of 5 pF, a breakdown voltage (V_{R_max}) of 8 V, and a tuning range (T_{tune}) of 3. Consequently, the corresponding exponential coefficient (a_2) for our narrow tone-spacing varactor stack should be equal to 0.137 V^{-1} [see (5) and (10)].

According to [11]–[15], for ideal operation of the distortion-free varactor stack, the power law exponent must be equal to 0.5 (corresponding to a uniformly doped diode) and the center-tap resistance should be as large as possible. One way, proposed in [12], to implement the high impedance at the center tap is the use of a small antiparallel diode pair, which benefits from the high zero-bias impedance of the diodes. However, the dc leakage of the varactor stack will result in some current flow through the antiparallel diodes, placing an upper limit on the effective center-tap impedance. As result, the linearity improvement resulting from the use of the antiparallel diode pair will be bounded in practice. To avoid these complications and to illustrate the different linearity behavior as a function of tone spacing, in this comparison we will use a resistor implementation of the center-tap impedance.

In contrast to the distortion-free varactor stack, the narrow tone-spacing varactor stack proposed here requires zero center-tap impedance for the baseband frequencies and infinitely high impedance for all the higher harmonic frequencies. Note that this center-tap impedance requirement is relative to the impedance offered by the varactor capacitance itself at these frequencies. In practical implementations, this can be a single resistor or an inductor since the capacitive reactance of the varactor stack itself exhibits relatively high impedance at low tone spacing. Note that, for the distortion-free varactor stack of [11]–[15], the finite resistive center-tap impedance cannot fulfill the IM3 cancellation condition at low tone spacing. Fig. 5 shows the simulated two-tone linearity comparison between the distortion-free varactor stack and the proposed narrow tone-spacing varactor stack, as measured by the dBc ratio of the fundamental and distortion current (at $2f_1 - f_2$) as a function of the tone spacing of the RF input signal (Δf).

Fig. 5. Simulated capacitive current distortion component at $2f_1 - f_2$ versus the tone spacing of the input RF voltage signal ($V_R = 4 \text{ V}$, $V_{RF\_peak} = 8 \text{ V}$, $f_{RF\_center} = 2 \text{ GHz}$, $C_{zero \text{ bias}} = 5 \text{ pF}$) for the distortion-free varactor stack and the proposed narrow tone-spacing varactor-stack circuits.

From Fig. 5, we observe that the traditional distortion-free varactor stack with 100-k Ω center-tap resistance is more linear than the proposed narrow tone-spacing varactor stack for large tone spacing, but less linear for narrow tone spacing. Note that the tone-spacing range of the resistive center tapped proposed narrow tone-spacing varactor stack can be extended with a smaller resistance value, but this would reduce the quality factor. Detailed analysis indicates that the product of the 6-dB corner frequency (Δf_{corner}), which is defined as the tone-spacing frequency ($f_1 - f_2$) from which the linearity of the narrow tone-spacing varactor stack expressed in dBc degrades by 6 dB, and the quality factor (only considering the influence of the resistive center-tap impedance) is a constant value for silicon of

$$\Delta f_{corner} \cdot Q = \frac{5a_2^2 V_{R\_max}^2 f_{RF}}{\sqrt{36864 - 25a_2^4 V_{R\_max}^4}}. \quad (23)$$

In this comparison example, this product equals to $6.3 \times 10^7 \text{ Hz}$. If a 1-k Ω center-tap resistor is applied, a 6-dB corner frequency (Δf_{corner}) of 500 kHz and a quality factor of 126 can be achieved. It is important to note that, for very low values of the center-tap resistor, the quality factor of the varactor stack will be reduced. For this reason, an inductive center-tapped narrow tone-spacing varactor stack can provide better performance since it facilitates a linear operation for larger tone spacing (above 10 MHz) without lowering the quality factor. However, for varactor stacks with a low capacitance value, a large inductor value is required to achieve the sufficiently high impedance at the fundamental RF frequency. A more advanced center-tap impedance network can increase the linear bandwidth of the proposed narrow tone-spacing varactor stack to much larger values, as long as it provides a low impedance for the baseband and a high impedance for all higher harmonics.

Fig. 6. Illustration of linear modulation using capacitive mixing and the narrow tone-spacing varactor stack and distortion-free varactor stack.

B. Comparison When Operated as a Linear Modulator

When considering varactors in an antiseriies diode configuration as a three-terminal capacitive mixing device, where the applied RF signal is modulated by the baseband center-tap voltage, the effective capacitance between the RF terminals *a* and *b* is modulated by the baseband voltage of node *c* (Fig. 6). In order to create a useful linear mixing function, the following two basic conditions should be fulfilled.

- The capacitive current flowing through the effective capacitance of the varactor stack should be linearly related to the applied RF voltage. In most practical (telecommunication) applications, this requires a zero value for the third-order distortion with respect to the applied RF signal. Consequently, no IM3 distortion products should arise in the resulting current.
- The effective capacitance must be modulated such that the transfer function is linear. As a consequence, the input should be pre-distorted for the nonlinear $C(V_c)$ relation of the total capacitance with respect to the center tap voltage, as well as for how a capacitance change relates to the transfer function of the total circuit.

When utilizing the earlier distortion-free varactor-stack configuration [12] for capacitance modulation, we faced the following conflict: the high-impedance requirement for the center-tap connection requires the baseband center-tap voltage to “float” ($Z_c(s) = \infty$). Imposing a controlling voltage to modulate the effective capacitance value will violate this high-impedance condition and directly yield intermodulation distortion of the applied signal at the RF terminals. This phenomenon can also be observed from the following simulation experiment.

Consider the simple setup of Fig. 6 where a two-tone RF voltage source is connected to a capacitance modulated varactor stack. The center node of the varactor stack is modulated by an independent voltage source (V_{mod}). Depending on the $C(V_R)$ relation, we pre-distort this modulating voltage such that a linear variation of the capacitance is achieved. In Agilent’s Advanced Design System (ADS), we have implemented this pre-distortion function using a symbolic defined device (SDD). Note that, in this simple example, the pre-distorting function is basically the inverse $C-V_R$ relation of the varactor technology used. Consequently, when using the distortion-free varactor stack (uniform

doping), the required pre-distortion function can be written as

$$V_c = \frac{K^2}{V_{mod}^2} - \phi \quad (24)$$

with K being the capacitance constant, ϕ being the build-in voltage [9], [12], and V_{mod} being the modulation voltage (see Fig. 6); while in the case of the proposed narrow tone-spacing varactor stack, the pre-distortion function is

$$V_c = \frac{\ln(V_{mod})}{a_2}. \quad (25)$$

As result of this pre-distortion, we obtain a linear variation of capacitance with the modulating baseband signal. Due to this linear variation, the resulting mixing current flowing through the varactor stack should be perfectly linear, provided that the varactor stack itself does not generate any intermodulation distortion due to the applied RF voltage. In our modulation experiments, we apply the pre-distorted voltage to the center-tap node through a high-value inductor, which behaves as short circuit for the baseband frequencies and as an open circuit for fundamental and higher harmonics.

The resulting simulated spectrum of the capacitive current flowing through the distortion-free varactor stack is given in Fig. 7(a). IM3 distortion is observed around the carrier and modulation sideband frequencies. One can argue that this result is expected since the baseband loading condition for the center tap was violated. Increasing this baseband impedance to the desired level will lower the IM3 distortion for two-tone signals with relatively large tone spacing; however, at the same time, it will effectively eliminate the intended capacitance modulation. In theory, one can circumvent this problem by performing the capacitance modulation by charge injection using a very high-impedance charge pump. However, this will create many implementation difficulties and drift problems.

In contrast to the distortion-free varactor stack, the proposed narrow tone-spacing varactor stack requires a baseband short circuit to guarantee its low-distortion operation. Consequently, we have to provide a low-impedance path at baseband frequencies between the center tap and RF terminals and high impedances for the fundamental and higher harmonics. The resulting simulated spectrum of the capacitive current is given in Fig. 7(b). The simulated distortion of the capacitive current is significantly improved compared to the results for the distortion-free varactor stack. It should be noted that the minimum intermodulation levels achieved in this experiment now depend on how well one can meet the center-tap impedance conditions.

VI. INFLUENCE OF PROCESS VARIATION ON LINEARITY

A. Process Tolerance

Besides the required harmonic termination, the main issue for the linearity of the proposed narrow tone-spacing varactor stack is the exponential $C(V_R)$ relation, which requires a $N_d x^{-2}$ doping profile, as shown in Fig. 2. However, the actual doping profile will deviate somewhat from the desired profile due to process variations.

In Section II, we found that as long as the $C(V_R)$ relation can be described by (5), the IM3 distortion will be cancelled.

Fig. 7. (a) Simulated spectrum of the capacitive current of the distortion-free varactor stack and (b) proposed narrow tone-spacing varactor stack when performing a 3-MHz capacitance modulation on a 0.5-MHz spacing two-tone signal using Fig. 6. Note that the distortion of the modulated signal is -50 dBc in the distortion-free varactor-stack case and -100 dBc in the proposed narrow tone-spacing varactor-stack case (for both cases, $c_{ab} = 5$ pF).

Referring to the derivation of the $C(V_R)$ relation in Appendix B, the following two deviations of the profile will cause a violation of the exponential $C(V_R)$ relation.

- The doping concentration is not proportional to $1/x^2$.
- The thickness of the spacer layer is not equal to x_{low} , resulting in an offset of the origin of the $N_d x^{-2}$ region.

Note that a doubling of the distance with the junction should result in one-fourth the doping concentration. If the origin of the $N_d x^{-2}$ region changes, this condition is violated.

For the first case, we can assign an arbitrary power (m) for the exponent of the doping concentration, and consequently, the $C(V_R)$ relation (see Appendix C) can be written in an explicit form as follows:

$$C(V_R) = A \frac{\epsilon_s}{x_0(V_R)} = \frac{A \epsilon_s}{\left[\frac{\epsilon_s (m+2) V_R x_{low}^m}{eN(x_{low})} + x_{low}^{m+2} \right]^{1/(m+2)}}. \quad (26)$$

For the second case, we can assume the origin of the distance (x) is offset by a factor of Δx , and consequently, the $C(V_R)$ relation (see Appendix D) can only be written in an implicit form as follows:

$$V_R = \frac{eN(x_{low})x_{low}^2}{\epsilon_s} \cdot \left[\ln \left(\frac{\frac{A \epsilon_s}{C} - \Delta x}{x_{low}} \right) + \frac{\Delta x}{x_{low}} - \frac{\Delta x}{\frac{A \epsilon_s}{C} - \Delta x} \right]. \quad (27)$$

B. Influence on Linearity Due to Process Deviation of the Power Law Exponent (m)

Using (26), we can analyze the influence of a deviation of the power coefficient from the ideal $m = -2$ case using the ADS harmonic-balance simulator [18]. Fig. 8 show the simulated nonlinear capacitive current at $2f_1 - f_2$, which is composed of IM3 and IM5 contributions, relative to the fundamental as a function of the RF signal amplitude (V_{RF_peak}) with Fig. 8(a) for low-voltage ($V_{R\_max} = 5$ V) and Fig. 8(b) for high-voltage ($V_{R\_max} = 20$ V) applications. Note that the simulator does not separate the IM3 and IM5 contributions, but they can be distinguished by their slopes.

In Fig. 8, the slope of the line for $m = -2$ is -80 dB/decade, as predicted by (18). One may find the IIP5 by extrapolating the line with $m = -2$ to 0 dBc in Fig. 8, which yields IIP5 values of 21 and 74 V, respectively, which is consistent with (19). The slope of the lines with $m = -1.8$ and $m = -1.9$ is roughly -40 dB/decade when V_{RF_peak} is small, which indicates that the third-order distortion component is the dominant factor for nonlinearity at this drive level; with the increase of V_{RF_peak} , the slope becomes larger, and finally, the slope is similar to that of the line with $m = -2$.

Note that the lines with $m = -2.1$, -2.15 , and -2.2 are clearly different from the others. The reason for this is that when V_{RF_peak} is small, third-order distortion constrains the linearity, when V_{RF_peak} increases, the fifth-order term becomes important and cancellation effects occur at a certain power level since the fifth-order distortion term has an opposite sign to the third-order term. Consequently, when V_{RF_peak} continues to increase, the fifth-order terms dominate and the nonlinearity has a similar slope as the line for the $m = -2$ case. The third- and fifth-order distortion cancellation phenomenon does not occur with $m = -1.9$ and -1.8 because the third- and the fifth-order distortion terms have the same sign for these two cases.

To define the fabrication window of the varactor, one may specify a linearity requirement as -60 dBc (sufficient for most applications) and check the acceptable range of m and V_{RF_peak} from Fig. 8. The maximum V_{RF_peak} , which still results in a distortion component smaller than -60 dBc, becomes larger and larger when m approaches -2.15 due to the third- and fifth-order distortion cancellation, which occurs when $m < -2$. On the other hand, the existence of the third-order distortion term with the same sign as the fifth-order distortion term will degrade the linearity for $m > -2$. Note that, since the distortion component exceeds the -60-dBc limit for $m < -2.15$ (Fig. 8),

 (a) $V_{R\_max} = 5$ V, $T_{tune} = 6$, $V_R = 2.5$ V and $IIP5_{ideal} = 21$ V

 (b) $V_{R\_max} = 20$ V, $T_{tune} = 6$, $V_R = 10$ V and $IIP5_{ideal} = 74$ V

Fig. 8. Simulated current distortion component at $2f_1 - f_2$ in dBc versus the magnitude of the input RF signal when m is not equal to -2 using the simulation setup of Fig. 1. Note that since this is a voltage driven situation, the results are insensitive to the actual varactor capacitance ($f_{RF\_center} = 2$ GHz).

the acceptable range of V_{RF_peak} values for this linearity constraint will drop drastically for smaller m values.

Consequently, when using a varactor with m in the range of -1.85 and -2.15 , a very high linearity can be achieved. The most remarkable conclusion is found for values of m close to -2.15 . For this value of m , two-tone signals will not generate any significant distortion (i.e., distortion is less than -60 dBc) as long as their peak amplitude does not exceed the maximum control voltage (device breakdown) or drive one of the diodes into forward conduction.

C. Effect of Spacer Layer Thickness (x_{low}) Variation on Linearity

Using (27), we can analyze the influence of variations in the spacer layer thickness on linearity using the ADS harmonic-balance simulator. The simulated nonlinear capacitive current at $2f_1 - f_2$ for the low-voltage ($V_{R\_max} = 5$ V) and high-voltage ($V_{R\_max} = 20$ V) applications are shown in Fig. 9(a) and (b),

 (a) $V_{R\_max} = 5$ V, $T_{tune} = 6$, $V_R = 2.5$ V and $IIP5_{ideal} = 21$ V

 (b) $V_{R\_max} = 20$ V, $T_{tune} = 6$, $V_R = 10$ V and $IIP5_{ideal} = 74$ V

Fig. 9. Simulated current distortion component at $2f_1 - f_2$ versus magnitude of the input RF signal when the spacer layer thickness is not equal to x_{low} . Note that since this is a voltage driven situation, the results are insensitive to the actual varactor capacitance ($f_{RF\_center} = 2$ GHz).

respectively. It demonstrates that when the spacer layer thickness is larger than x_{low} ($\Delta x > 0$), the third- and fifth-order distortion cancel for higher input voltages; when the spacer layer thickness is smaller than x_{low} ($\Delta x < 0$), no cancellation occurs and the third-order distortion dominates the nonlinearity.

We may again specify a linearity requirement of -60 dBc and check the acceptable range of Δx and V_{RF_peak} . We find that when the spacer layer thickness deviation is in the range of $\pm 20\%$, we meet the linearity requirement. When $\Delta x > 0$, the acceptable range of V_{RF_peak} is increased, and for values of $\Delta x < 0$, it is decreased.

In conclusion, the proposed varactor concept, in terms of linearity, has a very reasonable fabrication window to allow a reliable production of this new device type.

VII. EXPERIMENTAL RESULTS

The narrow tone-spacing varactor stack is implemented in a dedicated silicon-on-glass technology developed at the Delft

TABLE II
MAIN PARAMETERS OF THE PROCESSED VARACTOR STACK EXTRACTED FROM
THE MEASUREMENT RESULTS, COMPARED WITH THE DESIGNED VALUES

Parameter	x'_{low} (nm)	x_{high} (nm)	a_2 (V ⁻¹)	$V_{R,max}$ (V)	$V_{breakdown}$ (V)	T_{tune} @ $V_{R,max}$
Designed	50	250	0.358	5	5	5
Measured	50	175	0.358	3.5	>5	3.5

Fig. 10. Measured $C-V_R$ dependency (the dashed line indicates the ideal exponential relationship).

University of Technology, Delft, The Netherlands [19], [20]. This wafer-transfer technology eliminates substrate losses and facilitates patterning of both the frontside and backside of the wafer. Using this feature, the intrinsic varactor can be directly contacted by thick metal interconnects on both sides. This eliminates the finger structures used in conventional varactor implementations to lower the influence of the buried layer series resistance. The remaining losses of the metal interconnects can be significantly reduced through the use of plated copper, facilitating very high quality factors [9]. For our experiments, a trial run was defined to achieve the exponential $C(V_R)$ relation based on the proposed varactor profile of Fig. 2. In this particular test, we aimed for low-voltage varactor devices to serve applications that do not allow the use of high control voltages.

A. Measurement of the $C-V_R$ Dependence and Doping Profile

The varactor parameters (intended and realized) are listed in Table II. The intended varactor parameters are based on MEDICI simulations [21], which indicated a zero-bias depletion depth (x'_{low}) of 50 nm and a tuning range (T_{tune}) of 5. The measured $C(V_R)$ behavior and related electron concentration are given in Figs. 10 and 11, respectively. Although not perfect, the measured $C(V_R)$ behavior is very close to the intended one over the voltage range of 0.5–3.5 V. The deviation at very low voltages is due to out diffusion of electrons from the highly doped $N_d x^{-2}$ region into the lightly doped spacer layer. This yields a minor deviation for small reverse bias voltages (Fig. 10). In future implementations, this deviation can be compensated by slightly increasing the doping concentration close to x_{low} . The measured electron concentration, which is a

Fig. 11. Extracted electron distribution from $C(V_R)$ measurement compared with the ideal doping profile.

Fig. 12. Microphotograph of the 33-pF varactor stack used in the $C(V_R)$ and linearity measurements with 10-nH center-tap inductor.

good indication of the realized doping profile, starts to deviate from the relation at 175 nm due to an imperfect transition to the backside contact of the varactor. This deviation (Fig. 11) limits the quality factor of the realized varactors. The extracted parameters from the $C(V_R)$ measurements are given in Table II.

B. Linearity Measurements

To verify the linearity theory, the proposed narrow tone-spacing varactor-stack devices need to be combined with the proper harmonic terminations. For this purpose, we have used a shunt device of 33 pF in a two-port configuration with a 10-nH inductive center tap connection. A microphotograph of the layout is given in Fig. 12.

Linearity testing of the structure of Fig. 12 was performed using a two-tone signal ($f_{center} = 2.14$ GHz) with varying tone spacing. For the calibrated power measurements, we have used the system of [22]. Fig. 13 plots the measured and simulated distortion component at $2f_1 - f_2$ as a function of output power for different values of tone spacing. The measurement results confirm that successful third-order distortion cancellation occurs for low-tone spacing (see the results for 10 kHz, 100 kHz, and 1 MHz) resulting in a slope of 4 : 1 versus output power for the

Fig. 13. Measured and simulated distortion components at $2f_1 - f_2$ versus output power (capacitance of varactor stack = 33 pF, center tap inductance = 10 nH (simulated self-resonance frequency > 8 GHz), $f_{\text{center}} = 2.14$ GHz and $V_R = 2$ V).

distortion component at $2f_1 - f_2$ (in dBc). The slope of 4 : 1 indicates that the remaining source of nonlinearity is the much smaller fifth-order distortion component (IM5). For large tone spacing (> 10 MHz), the third-order distortion cancellation condition is violated by the increased center-tap impedance of the inductor for the baseband frequency ($f_2 - f_1$). Consequently, a slope of 2 : 1 versus output power for the now IM3-dominated distortion at $2f_1 - f_2$ (in dBc) is observed, as expected.

When comparing our measured linearity with the harmonic-balance simulation results based on ideal varactor devices with a perfect exponential $C(V_R)$ relation, we find—in spite of the already overwhelming linearity improvement—that there is a 10-dB discrepancy. To investigate if this deviation can be related to imperfections of the realized $C(V_R)$ behavior, a nonlinear varactor model based on a 15th-order polynomial fit of the measured $C(V_R)$ data was developed within ADS. As Fig. 13 shows, the modeled $C(V_R)$ behavior of the fabricated diodes explains the measured increase in distortion. Consequently, even better linearity is feasible by further optimization of the N_{dx}^{-2} profile. Finally, Fig. 14 plots the measured and simulated distortion component at $2f_1 - f_2$ and $2f_2 - f_1$ as function of tone spacing at a power level of 12 dBm. The narrow tone-spacing varactor stack clearly offers a superior performance over the single diode (with comparable effective capacitance) and the results match the theory quite well.

VIII. CONCLUSION

A new ultra-low distortion narrow tone-spacing varactor topology has been introduced that acts as an enabler for the realization of future adaptive transmitters, receivers, and linear capacitive modulators. The proposed structure exhibits a high capacitance tuning range, low-control voltages, and excellent linearity for in-band modulated signals in contrast to other known solutions. The proposed solution is based on two identical varactors with an exponential $C(V_R)$ relation in an antiseriess configuration. For this topology, IM3 cancellation can be achieved provided that the proper harmonic terminations are applied to its terminals. When the IM3 products are successfully

Fig. 14. Measured and simulated distortion components at $2f_1 - f_2$ and $2f_2 - f_1$ as function of tone spacing (capacitance of varactor stack = 33 pF, center tap inductance = 10 nH, $V_R = 2$ V, and $f_{\text{center}} = 2.14$ GHz).

cancelled, the remaining distortion is extremely low and dominated by IM5 products, which very rapidly decrease in backoff due to their fifth-order dependency. The related IIP5 voltage proves to be independent of the applied control voltage, which guarantees high linearity even at very low control voltages.

The implementation tradeoffs to achieve a good compromise between quality factor, (effective) tuning range, breakdown voltage, linearity, and RF signal handing have been given. The feasibility of practical implementations has been demonstrated by evaluating the influence of process spread on the linearity. This study indicates a very workable processing window for the realization of the required doping profile. For the experimental verification, the proposed varactor configuration has been implemented using our in-house DIMES silicon-on-glass technology. The measurements provided experimental evidence for the predicted IM3 cancellation and indicate a superior linearity for modulated signals up to 10-MHz bandwidth.

With the information provided, the proposed narrow tone-spacing varactor stack can be easily optimized for various applications, making it an attractive candidate for the implementation of tunable filters, capacitive switches, adaptive matching networks, phase shifters, antenna mismatch correction, or capacitive modulators. The unique feature of this novel varactor topology, compared to the distortion-free varactor stack and MEMS varactors, is its high modulation frequency for operation and high linearity for signals with low tone spacing, making it suitable for the next generation of adaptive handsets featuring multiband/multimode operation.

APPENDIX A

CALCULATION OF ELECTRIC FIELD DUE TO THE DOPING OF THE SPACER LAYER

Here we derive the restrictions on the doping level of the spacer layer in order not to seriously degrade the tuning range, breakdown voltage, and quality factor.

Assume that the spacer layer (Fig. 2) is arbitrarily doped and the doping concentration is defined as $N_{\text{fill}}(x)$ ($0 < x < x_{\text{low}}$).

Fig. 15. Typical electric field distribution of the graded varactor, the solid line represents the situation that the spacer layer (up to x_{low}) is not doped. The dashed line represents the situation when doping in the spacer layer is present (increasing the electric field).

The additional electric field, due to the spacer layer, as shown in Fig. 15 can be expressed as

$$\Delta E = \frac{e}{\epsilon_s} \int_0^{x_{low}} N_{fill}(x) dx. \quad (A.1)$$

The sheet resistance of the spacer layer can be written as

$$R_{sheet\_spacer\_layer} = \frac{1}{e\mu_n \int_0^{x_{low}} N_{fill}(x) dx} = \frac{1}{\mu_n \epsilon_s \Delta E}. \quad (A.2)$$

Consequently, if we assume that the increase in electric field must be limited to $\Delta E = E_{breakdown}/10 = 6 \times 10^4$ V/cm, we can derive that—for silicon—the sheet resistance of the spacer layer equals 12 k $\Omega/\square$. As a result, practical implementations of the quality factor optimized varactor diode will exhibit a sheet resistance for the spacer layer higher than this value.

APPENDIX B DERIVATION OF THE DOPING PROFILE FOR THE EXPONENTIAL $C(V_R)$ RELATION

In order to develop the analytical relationship between the doping profile, as shown in Fig. 2, and the $C(V_R)$ relation, we assume the following.

- 1) The n-type region has an abrupt boundary between the low doped spacer region and $N_d x^{-2}$ region.
- 2) The donor doping concentration is the same as the electron concentration in the n-type region.
- 3) Due to the high doping level at the start of the $N_d x^{-2}$ region, the low-doped spacer region consumes the total built-in voltage, while the applied voltage completely depletes the $N_d x^{-2}$ region.

The doping concentration of the varactor is defined as follows:

$$N(x) = \begin{cases} N_1(x) = N_{fill}, & 0 < x < x_{low} \\ N_2(x) = N(x_{low}) \left(\frac{x}{x_{low}} \right)^{-2}, & x_{low} \leq x \leq x_{high}. \end{cases} \quad (B.1)$$

The electric field is determined from Poisson's equation, which, for a 1-D analysis, is

$$\frac{d^2 \phi(x)}{dx^2} = \frac{-\rho(x)}{\epsilon_s} = -\frac{dE(x)}{dx} \quad (B.2)$$

where $\phi(x)$ is the electric potential, $E(x)$ is the electric field, $\rho(x)$ is the volume charge density, and ϵ_s is the permittivity of the semiconductor. The electric field (Fig. 15) in the n-region is found by integrating (B.2) as follows:

$$E_2(x) = -\frac{eN(x_{low})x_{low}^2}{\epsilon_s} \left(\frac{1}{x} - \frac{1}{x_0} \right), \quad x_{low} \leq x \leq x_0 \quad (B.3)$$

$$E_1(x) = \frac{eN_{fill}}{\epsilon_s} (x - x_{low}) - \frac{eN(x_{low})x_{low}^2}{\epsilon_s} \left(\frac{1}{x_{low}} - \frac{1}{x_0} \right), \quad 0 \leq x \leq x_{low}. \quad (B.4)$$

Due to the Schottky contact, the potential at $x = 0$ can be defined as zero. Based on (B.3) and (B.4), the potential at x_0 can be determined as follows:

$$\phi(x_0) = \frac{eN_{fill}}{2\epsilon_s} x_{low}^2 + \frac{eN(x_{low})x_{low}^2}{\epsilon_s} \ln \frac{x_0}{x_{low}} = V_{bi} + V_R. \quad (B.5)$$

The first item in (B.5) is the built-in voltage, and we then have

$$C(V_R) = \frac{A\epsilon_s}{x_0} = \frac{A\epsilon_s}{x_{low}} \exp \left(-\frac{\epsilon_s}{eN(x_{low})x_{low}^2} V_R \right) \quad (B.6)$$

where the constant $(A\epsilon_s/x_{low})$ is the capacitance of the original depletion region.

The derivation of the $C(V_R)$ relation above assumes that the low-doped spacer region consumes the total built-in voltage, while the applied voltage completely depletes the $N_d x^{-2}$ region. However, even if the beginning of the $N_d x^{-2}$ region is highly doped (normally from 2×10^{17} cm $^{-3}$ to 2×10^{18} cm $^{-3}$), it still consumes part of the built-in voltage. Now, we consider the more general situation, where the depletion width at zero applied voltage is x'_{low} , which is larger than x_{low} .

In this situation, (B.5) is still valid since there is no change in the doping profile. The difference is that the built-in voltage no longer equals the first term of (B.5). Instead, it should be written as

$$\phi(x'_{low}) = \frac{eN_{fill}}{2\epsilon_s} x_{low}^2 + \frac{eN(x_{low})x_{low}^2}{\epsilon_s} \ln \frac{x'_{low}}{x_{low}} = V_{bi}. \quad (B.7)$$

As previously done, we substitute (B.7) into (B.5), and we then have

$$\frac{eN(x_{low})x_{low}^2}{\epsilon_s} (\ln x_0 - \ln x'_{low}) = V_R. \quad (B.8)$$

Similarly, the C - V_R relation can be written as

$$C(V_R) = \frac{A\varepsilon_s}{x'_{\text{low}}} \exp\left(-\frac{\varepsilon_s}{eN(x_{\text{low}})x_{\text{low}}^2} V_R\right) \quad (\text{B.9})$$

where the constant $(A\varepsilon_s/x'_{\text{low}})$ is the zero-bias capacitance value.

APPENDIX C

DERIVATION OF $C(V_R)$ RELATION IN THE CASE OF VARIATION FROM THE IDEAL POWER LAW EXPONENT

Here, we keep the three assumptions mentioned above in Appendix B, but, due to process variations, the doping concentration of the varactor is modified as

$$N(x) = \begin{cases} N_1(x) = N_{\text{fill}}, & 0 < x < x_{\text{low}} \\ N_2(x) = N(x_{\text{low}}) \left(\frac{x}{x_{\text{low}}}\right)^m, & x_{\text{low}} \leq x \leq x_{\text{high}} \end{cases} \quad (\text{C.1})$$

Note that only the exponent of the doping profile is changed from its ideal value.

Making use of the Poisson equation, the electric field in the n-type region can then be written as

$$E_2(x) = \frac{eN(x_{\text{low}})x_{\text{low}}^{-m}}{\varepsilon_s(m+1)} (x^{m+1} - x_0^{m+1}), \quad x_{\text{low}} \leq x \leq x_0 \quad (\text{C.2})$$

$$E_1(x) = \frac{eN_{\text{fill}}}{\varepsilon_s} (x - x_{\text{low}}) + \frac{eN(x_{\text{low}})x_{\text{low}}^{-m}}{\varepsilon_s(m+1)} (x_{\text{low}}^{m+1} - x_0^{m+1}), \quad 0 \leq x \leq x_{\text{low}}. \quad (\text{C.3})$$

Still defining the potential at $x = 0$ as zero, based on (C.2) and (C.3), the potential at x_0 is given by

$$\begin{aligned} \phi(x_0) &= \frac{eN_{\text{fill}}}{2\varepsilon_s} x_{\text{low}}^2 + \frac{eN(x_{\text{low}})x_{\text{low}}^{-m}}{\varepsilon_s(m+2)} (x_0^{m+2} - x_{\text{low}}^{m+2}) \\ &= V_{\text{bi}} + V_R. \end{aligned} \quad (\text{C.4})$$

As was done earlier, the first item in (C.4) cancels with the built-in voltage V_{bi} . Consequently, the $C(V_R)$ relation can be written as

$$C(V_R) = A \frac{\varepsilon_s}{x_0(V_R)} = \frac{A\varepsilon_s}{\left[\frac{\varepsilon_s(m+2)V_R x_{\text{low}}^m}{eN(x_{\text{low}})} + x_{\text{low}}^{m+2}\right]^{1/(m+2)}}. \quad (\text{C.5})$$

Note that the result above is only valid when m is not equal to -2 .

APPENDIX D

DERIVATION OF $C(V_R)$ RELATION FOR VARIATION OF DOPING DENSITY AT THE ORIGIN

Here, we maintain the three assumptions mentioned in Appendix B, but the doping concentration of the varactor is modified as

$$N(x) = \begin{cases} N_1(x) = N_{\text{fill}}, & 0 < x < x_{\text{low}} + \Delta x \\ N_2(x) = N(x_{\text{low}}) \left(\frac{x - \Delta x}{x_{\text{low}}}\right)^{-2}, & x_{\text{low}} + \Delta x \leq x \leq x_{\text{high}} + \Delta x. \end{cases} \quad (\text{D.1})$$

Making use of the Poisson equation, the electric field in the n-type region can be written as

$$E_2(x) = -\frac{eN(x_{\text{low}})x_{\text{low}}^2}{\varepsilon_s} \left(\frac{1}{x - \Delta x} - \frac{1}{x_0 - \Delta x}\right), \quad x_{\text{low}} + \Delta x \leq x \leq x_0 \quad (\text{D.2})$$

$$\begin{aligned} E_1(x) &= \frac{eN_{\text{fill}}}{\varepsilon_s} (x - x_{\text{low}} - \Delta x) \\ &\quad - \frac{eN(x_{\text{low}})x_{\text{low}}^2}{\varepsilon_s} \left(\frac{1}{x_{\text{low}}} - \frac{1}{x_0 - \Delta x}\right), \quad 0 \leq x \leq x_{\text{low}} + \Delta x. \end{aligned} \quad (\text{D.3})$$

Defining the potential at $x = 0$ as zero and canceling the built-in voltage, based on (D.2) and (D.3), the $x_0(V_R)$ relation can be written as

$$V_R = \frac{eN(x_{\text{low}})x_{\text{low}}^2}{\varepsilon_s} \left(\ln \frac{x_0 - \Delta x}{x_{\text{low}}} + \frac{\Delta x}{x_{\text{low}}} - \frac{\Delta x}{x_0 - \Delta x}\right). \quad (\text{D.4})$$

Consequently, the $C(V_R)$ relation is given by

$$V_R = \frac{eN(x_{\text{low}})x_{\text{low}}^2}{\varepsilon_s} \left[\ln \left(\frac{\frac{A\varepsilon_s}{C} - \Delta x}{x_{\text{low}}}\right) + \frac{\Delta x}{x_{\text{low}}} - \frac{\Delta x}{\frac{A\varepsilon_s}{C} - \Delta x}\right]. \quad (\text{D.5})$$

Note that the $C(V_R)$ relation can only be written in an implicit form.

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