Master Thesis

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Design of a Distributed Clock Generator for Multiple Power Domain System-on-Chip Integrated Circuits

Msc. student: Jinbo Wan
Mentor at NXP Semiconductors: Maurice Meijer, Arnoud van der Wel
Supervisor at TUDelft: Prof. John Long
Abstract

Modern system-on-chip IC designs show great requirement on minimizing power consumptions. One of the low power techniques is using dynamic voltage frequency scaling for each power domain. Yet the clock generator unit is the bottleneck to apply this technique. In this thesis, we focus on the local clock generator unit solution and design three new local clock generators which share the power supply with digital blocks. The best candidate provides good jitter performance (10ps) under large power supply noise, low power consumption (900µW) and small area (90 × 60µm²). The influence of power supply noise on jitter of each circuit components, like voltage control oscillator, frequency divider, phase frequency detector, charge pump, loop filter and clock buffers are studied in thoroughly.
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1. Introduction

CMOS technology scaling has been driven by Moore’s Law for more than forty years. Nowadays, the minimum feature size in integrated circuit (IC) designs is as small as 45 nm. ICs realised in such advanced CMOS technology can integrate a billion of transistors on the same silicon die. As CMOS technology advances, the integration density is increased, which enables more cost-effective solutions and smaller form-factor devices. Moreover, ICs fabricated in newer CMOS technologies can operate at higher operating frequencies, thereby opening avenues for higher performance electronic products. Despite these benefits, the power consumption has become a major concern because the dense devices produce a significant amount of heat imposing constraints on circuit performance and IC packaging. The case for portable devices is obvious, e.g. the goal is to maximize battery time. Designing ICs for low power will be a key practical and competitive advantage in the coming decade [1.1][1.2].

1.1. Clock Generation in Modern System Chips

Modern system-on-chip (SoC) IC designs are getting equipped with multiple power domains to meet the chip power-performance demands [1.3][1.4]. A power domain is a region in the IC that is powered from its own dedicated power supply voltage ($V_{DD}$), and operates at its own dedicated frequency ($f$). A power domain may contain multiple intellectual property (IP) cores of which each shared the same power-performance demands. Figure 1.1 shows an example of a multiple power-domain SoC design in which power domains are defined based on the functionality of the IP cores.

![Figure 1.1](image.png)  
**Figure 1.1** Example of a multiple power-domain SoC
In this respect, power domains are optimized to have power characteristics that are unique from the rest of the design. On one hand, this may concern dedicated hardware (HW) blocks that should operate at a fixed $V_{DD}$ and $f$. On the other hand, the may concern processor cores that require dynamic voltage and frequency scaling (DVFS). Power domains may contain advanced power management features, e.g. clock gating, power-down support with or without state-retention, DVFS, and defined operating modes [1.5][1.6].

Traditionally, ICs make use of a custom-designed on-chip clock generator unit (CGU) which produces the operating frequencies required in the whole chip design [1.7][1.8]. Typically, this component contains various phase-locked-loops (PLL) for frequency generation, and they are referenced to a low-frequency crystal oscillator on the printed-circuit-board (PCB). Also, it contains the frequency dividers and control logic for supporting a wide range of operating frequencies and clock gating functionality. We will refer to such CGU as central clock generator unit (C-CGU) in the remainder of this report. With the increasing amount of power domains in the IC, also the need for more independent operating frequencies increases. The CGU requirements for power domains that need DVFS support will be more stringent, because the required frequency changes at run-time. When only a few power domains are present in the IC, a C-CGU can meet the requirements with moderate complexity. However, with the number of power domains increasing, the operating frequencies required and the associated control overhead will totally overwhelm the C-CGU, which constrains IC power-performance optimization. Another issue with a C-CGU is the clock distribution which will become problematic in large high-performance ICs [1.9]. This will degrade the quality of the clock signals as provided to the local flip-flop registers in the design. Consequently, larger design margins for clock uncertainty are needed that eventually degrade the maximum performance of the IC.

An alternative, yet revolutionary clocking approach is the use of local clock generator units (L-CGU) [1.10]. Each power domain contains its own L-CGU which generates the required frequencies for the respective power domain. It can solve the problems associated to the C-CGU, and offers a modular and flexible clocking approach. However, the challenge of an L-CGU is to generate a good quality clock while located in the close proximity to the digital circuitry that acts as noise source. Furthermore, the penalty for a
clean analog $V_{DD}$ for each L-CGU becomes too high during chip integration. Finally, the traditional globally synchronous inter power domain communication scheme needs to be revisited.

1.2. Project Description
This work concerns an investigation of clock generators suitable for use in a local clocking scheme for digital logic CMOS circuits. Such L-CGU should have low-jitter characteristics for providing a good quality clock to the power domain. It should be programmable to support various operating frequencies with glitch-free frequency transitioning to enable DVFS support. Also, it should support clock gating functionality for standby operation. The L-CGU should operate from a ‘noisy’ digital power supply voltage to simplify integration complexity. Finally, the L-CGU should have a minimum overhead in terms of area occupation and power consumption. The following research questions should be addressed:

- What kinds of oscillator are suitable for L-CGU application?
- How the power supply noise influence the jitter of the L-CGU?
- What is the lowest possible jitter that can be achieved by an L-CGU?
- What the clock buffer network influence to the final jitter performance when the L-CGU output need to be distributed?

Potential candidate L-CGUs should be compared on their characteristics (e.g. jitter, power consumption, area, etc.). The outcome of this work should be an implementation of the most promising clock generator in 65nm LP-CMOS. Furthermore, the clock buffer jitter contribution should also be investigated, which will serve as a starting point for optimizing the clock distribution network.

1.3. Report Outline
Chapter 2 will review the clock generation approach and compare C-CGU and L-CGU. The requirements for the L-CGU design will be presented at the end of Chapter 2. Chapter 3 will focus on jitter analysis. The relationship between jitter and phase noise will be discussed. Power supply noise influence to jitter will be studied. And at last the jitter produced by the clock buffer in the clock distribution networks will be discussed. Chapter 4 will present the L-CGU system structure and the brief analysis for each part in the L-CGU. Chapter 5 will show both schematics and layout of the L-CGU. The
Chapter 1   Introduction

simulation results and test bench will be introduced in Chapter 6. And finally, Chapter 7 concluded the thesis work and prospect the future works.

Reference


2. **SoC Clock Generation Approach**

Power efficient design technologies have become key drivers in modern integrated circuits targeting portable to high-performance application ranges. The implementation of circuits and systems in new deep submicron technologies requires new ideas to make the system performance successfully feasible. In this chapter we will first elaborate on the clocking needs in high-performance digital logic CMOS circuits. Next, we will review the central and local clocking approaches for power domain SoCs, and discuss inter domain communication schemes. Finally, we formulate the requirements for the L-CGU design.

2.1. **Clocking Requirements for Digital Logic Blocks**

The ongoing CMOS technology scaling enables higher frequency operation. The shorter clock periods require also a reduction of timing margins for maximizing the useful cycle time. Consequently, clock design becomes increasingly challenging for meeting clock, skew and jitter targets.

Traditionally, circuit designers use 10% clock uncertainty margin of the total clock budget when implementing their circuits. Figure 2.1 puts in perspective the influence of clock uncertainty on circuit area and performance. The values have been obtained from logic synthesis for maximum speed with Cadence Ambit for a RISC processor design in 65nm LP-CMOS. In this example, the use of a clock uncertainty of 300ps results in an area penalty of 20% with respect to the case of no clock uncertainty. Alternatively, the minimum clock period can be decreased by 8%, leading to an improved circuit performance. Although the use of a ‘no clock uncertainty’ margin is not realistic, the design over-dimensioning for larger clock uncertainties has become evident. A high-quality clock generation and clock distribution is of prime importance in high-performance IC designs.
The power consumption in modern ICs has become a primary concern. The use of power domain approaches is a means to further reduce power consumption by selecting optimum V_DD’s and frequencies at design-time or during circuit operation. An example of a power management (PM) technique for reducing active-mode power consumption is dynamic voltage and frequency scaling (DVFS) [2.1]. DVFS can be utilized only in those cases where the circuit does not require peak performance. Significant power savings can be achieved. Figure 2.2 illustrates the dependency between frequency and power consumption when operating at the optimum V_DD (ref. DVFS).

**Figure 2.1** Circuit area versus performance for different clock uncertainty settings for a RISC processor design in 65nm LP-CMOS

**Figure 2.2** Frequency versus Power Consumption for Different Supply Voltage Settings for a 65nm LP-CMOS ring-oscillator circuit
DVFS requires a clock generator that supports multiple clock frequencies. Without frequency scaling support, this PM technique cannot be utilized. Moreover, the transitioning between frequency points needs to be free of spurious glitches since the circuit is operational at that time. It also needs to be fast, because this offers the most power benefits. Furthermore, a sequence is needed between frequency and $V_{DD}$ control in order to guarantee circuit operation. For example, the frequency needs to be reduced before the $V_{DD}$ is reduced, and the $V_{DD}$ must be increased before the frequency is increased. The required frequency control needs intelligent clock management. Especially, in multiple power-domain ICs the clock management can become a bottleneck, depending on the amount of power domains that require DVFS support.

Finally, modern ICs also require standby-mode power management. Clock generators need to be equipped with clock gating support to avoid the needless switching of circuit nodes while the clock generator is still running. There should also be clock enable support to fully stop the clock generator, which reduces its power consumption to a minimum.

### 2.2. Review of the Central Clocking Approach

The traditional clock generation scheme in digital SoCs is the centralized or global clocking approach. A C-CGU generates the clocks for each part in the design. Figure 2.3 illustrates this concept when used in a multiple power-domain SoC design. The C-CGU as well as the global and local clock distribution networks are indicated.

![Figure 2.3 Example of a Central Clocking Approach in an SoC](image)
The main benefit of a central clock is that the C-CGU can be supplied from its own clean analog power supply and ground connections. Although this requires extra package pins, it is very effective to suppress the influences of noise as generated by the digital circuitry. Consequently, this will improve the quality of the clock.

The drawbacks of a C-CGU are as follows. Since there is only one clock generator in the SoC, it needs to support all the required operating frequencies for the HW blocks. This makes the C-CGU complicated. Moreover, the clock management may be dramatically complex for a larger number of power domains. Each power domain needs to interact with the C-CGU to request a certain frequency of operation, or clock gating for standby mode. This will result in a communication bottleneck in case many power domains communicate with the C-CGU. Furthermore, for each SoC their may be different clocking needs and C-CGU customization is required, or alternatively, a generic C-CGU is taken which is not used to its full potential.

An example of a C-CGU is shown in Figure 2.4. Modern C-CGUs can easily contain tens of phase-locked-loops (PLL) and several reference inputs. The C-CGU shown in Figure 2.4 is a programmable CGU. The number of external clock inputs, PLLs (and type), frequency dividers (and type), and clock outputs are selectable at compile time. Test control block (TCB) determines the C-CGU working mode. Design for debug (DfD) and delay fault test (DFT) blocks are used to monitor the PLLs status and test. Power (PWR) block control the CGU power consumption by setting some PLLs into sleep mode when they are not needed.
The clock distribution for a central clocking scheme is becoming extremely challenging for high-performance ICs. On one hand this is caused by the further CMOS technology scaling. The die area may not scale with the same amount as the transistor area, thus, the coverage area for clock distribution may increase. On the other hand, higher performance operation reduces the cycle time. The clock uncertainty margin needs to be scaled accordingly to have the maximum benefit from performance increase due to technology scaling. In a central clocking scheme, the clock needs to distribute globally (to the different HW blocks) and locally (within each HW block). It is essential that all registers, or leaf cells of the clock distribution, receive the clock in-phase (or at a defined phase-shift) with the master clock to avoid communication problems. These matters make a central clocking scheme not easily scalable. The clock distribution itself is also a source of clock uncertainty. Since the clock buffers are typically powered from the digital ‘noisy’ supply to lower implementation complexity, they are sensitive to the power supply noise that exists on the supply due to the switching digital circuitry. As a result, the quality of the clock signal at the output of the clock generator is degraded to a large extent when it arrives at the receiving flip-flop clock input. For clock skew management, a place-and-route tool inserts many clock buffers in clock distribution network, however, the clock jitter increases for the amount of clock buffers in the path are increasing. Thus, the clock quality is very much dependent on the clock tree optimization.

2.3. Review of the Local Clocking Approach
A local clocking approach can alleviate the drawbacks associated to a central clocking approach. Now, each power domain is equipped with its own L-CGU, and it needs to provide the clock frequencies to all HW blocks that share the same power domain. Typically, a power domain contains a single HW block, and the L-CGU only needs to provide a single clock. Figure 2.5 illustrates the local clocking concept when used in a multiple power-domain SoC design. Observe from this Figure, the modularity of a local clocking approach. The global clock distribution network as found in the central clocking approach is not required in case of local clocking.
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![Diagram of local clocking approach in a SoC](image)

**Figure 2.5**  Example of a Local Clocking Approach in a SoC

Since the L-CGU generates the clock for one power domain at a time, also the communication overhead for a domain that uses PM like DVFS is rather low. The local clocking approach fits seamlessly in the context of local power-performance managed domains. Moreover, the local clocking offers a scalable solution for multiple power domain SoCs. When the number of power domains is increasing, the complexity of the local clocking approach will not increase. Each clock domain is smaller in size as compared to the central clocking approach, thereby it is simpler for skew and jitter control. Therefore, this approach seems to be more suitable for next generation chips as compared to the central clocking approach.

There are also challenges to overcome when local clocking is utilized. The global communication, i.e. inter power domain communication may be an issue. The traditional globally synchronous communication may give too much performance penalty and may require larger data buffering because the clocks in the local domains may be out-of-phase. In the next section we will elaborate more on this communication. Furthermore, from an integration perspective it is not desired to use a clean analog supply for each L-CGU. The layout effort becomes too complicated, and the layout overhead becomes too much in case of many power domains. Alternatively, the L-CGU may be powered from the digital ‘noisy’ supply but this will sacrifice the quality of the clock. This requires L-CGUs that are insensitive to the noise as produced by the digital circuitry. In this work we focus the development of such L-CGU.
2.4. Inter Power Domain Communication Schemes for L-CGU

As briefly mentioned before, the global communication when utilizing a local clocking scheme may become a problem. Within a power domain, the working frequency is the same, and communication is done synchronously and referenced to the L-CGU. Between power domains, the communication is more complicated because the frequencies in different power domains may not be the same, or at least not be at the same phase. There exists different communication approaches as alternative to the traditional globally synchronous communication approach [2.2][2.3][2.4]. Two examples are: source synchronous or Globally Asynchronous Locally Synchronous (GALS). Figure 2.6 shows an example of the previous methods.

![Diagram](image)

**Figure 2.6** Example communication schemes for inter power domain communications

The operation of the communication schemes is as follows. Globally synchronous
communication (see Figure 2.6a) uses a global clock reference to communicate between a sending power domain and receiving power domain over a Connection Link (CL). It requires a clock in the chip that is properly balanced. This communication scheme is simple but faces insertion delay, high power and clock skew problem. Source Synchronous is more complicated (see Figure 2.6b), there is a buffer needed in which data is stored by using a source clock, and data is read by using a destination clock. The buffer is indicated in Figure 2.6b as Asynchronous Connection Link (ACL). The clock-data skew is critical in this approach. Source Synchronous communication is suitable for use in combination with a local clocking approach since both source and destination clocks are used for the communication. The imbalance of these clocks has an effect on the buffer size. GALS communication is realized by handshake (or asynchronous) control. As in case of Source Synchronous, there is a buffer in which data is stored and data is read from. Synchronous communication is used within the power domains. Also, GALS communication is suitable for use in combination with a local clocking approach.

At this point it should be clear that there exist global communication schemes suitable for inter power domain communications when power domains are equipped with an L-CGU. The global communication is beyond the scope of this work. Our focus is on is on the clock generation and clock distribution, particularly the design of an L-CGU.

2.5. L-CGU Requirements and Design Specifications

In this section we will summarize the requirements and design specifications related to the L-CGU design.

The main requirement is an L-CGU topology that is insensitive to external noises (i.e. power supply noise, substrate noise, …) such that the L-CGU is able to generate a high quality clock. The L-CGU output frequency should be accurate and stable, i.e. the clock jitter should be as low as possible. The output frequency should be independent of process parameter variations and temperature conditions. The L-CGU should be powered from the digital ‘noisy’ supply to simplify the IC top-level integration.

Other requirements are: 1) the L-CGU should be fully integratable in bulk CMOS technology, 2) a small circuit area, 3) a low active and static power consumption, 4) the L-CGU should support multiple frequency points, frequency scaling, clock gating for L-
CGU output gating and clock enabling for full L-CGU stop, 5) seamless and glitch-free frequency transitioning, 6) a digital L-CGU interface for frequency programming, and 7) an output signal that indicates if the L-CGU output is stable.

The L-CGU design should be implemented in a 65nm LP-CMOS technology. The previous summarized requirements have been translated into design specifications of the L-CGU, which are shown in Table 2.1. These design specifications have been used as the basis for the L-CGU design which will be shown in the following chapters.

<table>
<thead>
<tr>
<th>Items</th>
<th>Requirements</th>
</tr>
</thead>
<tbody>
<tr>
<td>CMOS technology</td>
<td>65nm LP-CMOS</td>
</tr>
<tr>
<td>Supported Operating Frequencies</td>
<td>550MHz, 500MHz, 450MHz, 400MHz, 350MHz, 300MHz, 250MHz, 200MHz, 150MHz, 100MHz, 50MHz</td>
</tr>
<tr>
<td>Jitter specification</td>
<td>Max RMS period jitter&lt;30ps at 550MHz output frequency</td>
</tr>
<tr>
<td>Frequency Switching</td>
<td>• Switch time as small as possible</td>
</tr>
<tr>
<td></td>
<td>• Glitch-free frequency transitioning</td>
</tr>
<tr>
<td></td>
<td>• Clock gating and clock enabling support</td>
</tr>
<tr>
<td>Area Occupation</td>
<td>At least &lt;0.1mm², as small as possible</td>
</tr>
<tr>
<td>Active Power Consumption</td>
<td>Lower than 1mW</td>
</tr>
<tr>
<td>L-CGU Supply Voltage</td>
<td>• Nominal digital V_{DD} of 1.2V</td>
</tr>
<tr>
<td>L-CGU Outputs</td>
<td>Clock frequency signal, clock valid signal</td>
</tr>
</tbody>
</table>

2.6. Summary

In this chapter, the clock requirements for the digital logic blocks in modern SoC design are first reviewed. The two approach for clock generation: the L-CGU and the C-CGU are investigated. Depends on these reviews, the requirements for the L-CGU are presented. Also the inter power domain communication schemes for the L-CGU are briefly examined. Next chapter, we will analyze the requirements for the L-CGU. The most critical one—jitter performance, will be focused.
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Reference


3. Jitter Performance Models

The most critical requirement of the L-CGU is the quality of the output clock signal, which is quantified by the timing jitter. Although jitter is widely used, the symbols and definitions of jitter are still not unique. In this chapter, we will first provide the reader with an overview and definition of jitter as used in this work, and its relation to phase noise. Next, we present the jitter due to power supply noise, and the associated power supply noise model used for emulating a noisy digital environment. Finally, we analyze the jitter performance of a single CMOS inverter as well as a CMOS inverter chain.

3.1. Jitter Definitions

Jitter is measure for the clock uncertainty in time domain. In this section we will use the jitter definitions from Ken Kundert [3.1].

For any clock signal, there exists a time sequence \( \{ \tau_i \} \) that refers to the clock transitions as illustrated in Figure 3.1 for the rising clock transitions. For a noise-free clock signal, \( \tau_i \) is separated by exactly one clock period of \( T \) seconds (\( \tau_i = iT \)). When the clock signal is noisy, \( \tau_i \) can be described as \( \tau_i = iT + \delta t_i \) which now becomes of a statistical nature. Three jitter metrics exist for the statistical characterization of this time sequence. A graphical representation of these jitter metrics is shown in Figure 3.2.

![Figure 3.1 Time sequence \( \{ \tau_i \} \)]

The simplest one is the edge-to-edge jitter, \( J_{ee} \), which is defined as the delay variation between a triggering and a response event. Since a noise-free clock input signal is as-
sumed, the edge-to-edge RMS jitter $J_{ee}$ can be described as

$$J_{ee}^2(i) = \text{var}(\tau_i - iT) = \text{var}(\delta \tau_i) = \text{var}(\tau_i)$$ (3.1)

$J_{ee}$ is an input referred jitter metric which is only defined for driven systems. Examples of driven systems are: a phase-frequency detector (PFD), a frequency divider (FDIV) and clock buffer. For such systems, a transition at the output is a direct result of a transition at the input. The reason why $J_{ee}$ is only defined for driven systems is because the reference point is fixed and free of noise. Consequently, it can not be used for autonomous systems such as a voltage-controlled oscillator (VCO).

The second jitter metric is K-Cycle jitter, $J_k$. $J_k$ measures the uncertainty of the clock signal over $k$ clock cycles. It is defined as the standard deviation of $\tau_{i+k} - \tau_i$.

$$J_k^2(i) = \text{var}(\tau_{i+k} - \tau_i)$$ (3.2)

The reference point ($\tau_i$) refers to a point on a previous $k$-cycle transition, and therefore it is not free of noise which increases the jitter. K-Cycle jitter is suitable as a metric in both driven and autonomous systems. A special case is found for $k=1$; $J_1$ is the standard deviation of the length of a single clock period. This case is often referred as period jitter or cycle jitter, which is denoted as $J$ (where $J=J_1$). In Cadence SpectreRF™, K-Cycle jitter is expressed as $J_c$.

The third jitter metric is cycle-to-cycle jitter, $J_{cc}$. Consider $T_i = \tau_{i+1} - \tau_i$ to be the period of cycle $i$. Now, $J_{cc}$ can be described as

$$J_{cc}^2(i) = \text{var}(T_{i+1} - T_i)$$ (3.3)

$J_{cc}$ is a jitter metric for identifying large adjacent clock cycle displacements. It is similar to edge-to-edge jitter because it does not contain information about the correlation in the jitter between distant clock transitions. However, the difference is due to the fact that it is a measure of short-term jitter, because it is relatively insensitive to long-term jitter. That is to say it can get rid of flicker noise influence. Also, $J_{cc}$ is suitable as a metric in both driven and autonomous systems.
If the clock signal noise is either stationary or $T$-cyclostationary [3.1], then the time sequence $\{\tau_i\}$ is stationary. This means that the jitter metrics do not vary with $i$. Consequently, $J_{ee}(i)$, $J_k(i)$, and $J_{cc}(i)$ can be written as $J_{ee}$, $J_k$, and $J_c$.

We will use period jitter, $J$, for characterizing the performance of the L-CGU components. The values of $J$, which will be shown in the remained chapters, are the root-mean-square (rms) value, not the peak value.

### 3.2. Phase noise

Jitter is a simple measure of the clock quality. Yet it cannot give much insight into the design. Based on the jitter measurement, we don’t know important information such as which parts of the circuit dominate the jitter performance and need to be improved, or which circuit part doesn’t matter and can be relaxed in its design requirements. Correspondingly, phase noise can give much insight to help the design and is more familiar to oscillator designers. What’s more, the relationship between jitter and phase noise is determined and very clear.

There exists several different spectral density functions commonly used to characterize phase noise [3.2][3.3]. In this section we referred to the definition in Gardner’s book [3.4] and only elaborate on those functions that are relevant for this work. For this purpose, we make use of a generic oscillator whose output voltage $v_o(t)$ has a sinusoidal waveform at a nominal frequency $f_0$ Hertz.

$$v_o(t) = A\cos[2\pi f_0 t + \phi(t)]$$  \hspace{1cm} (3.4)
where \( A \) is the voltage amplitude, and \( \phi(t) \) contains all phase and frequency deviations from the nominal frequency \( f_0 \) and phase \( 2\pi f_0 \). The presence of amplitude noise is not separately accounted for because oscillators contain an amplitude-control mechanism largely suppress this noise. Hence, we treat all the noise as phase noise.

### 3.2.1. \( S_{v_o}(f) \): Passband spectrum of the oscillator signal \( v_o(t) \)

\( S_{v_o}(f) \) is the Fourier transform of the autocorrelation function of the random process \( v_o(t) \). It is one-side spectral description, and requires a stationary autocorrelation function. Figure 3.3 shows an example of \( S_{v_o}(f) \) for three different cases of phase noise. When phase noise is absent, the spectrum contains a single frequency at \( f_0 \) and can be expressed as \( \frac{A^2}{2} \delta(f - f_0) \). When phase noise occurs, the spectrum is spread. Irrespective of the amount of phase noise present in the signal, the integral of \( S_{v_o}(f) \) over all frequencies equals \( \frac{A^2}{2} \). In other words, the variance of \( v_o(t) \) equals \( \frac{A^2}{2} \).

\[
\text{var}[v_o(t)] = \int_0^\infty S_{v_o}(f) df = \frac{A^2}{2} \tag{3.5}
\]

![Figure 3.3: Theoretical spectrum \( S_{v_o}(f) \) of oscillator output \( v_o(t) \)[3.4]](image)

#### 3.2.2. \( L(\Delta f) \): Single Side Band (SSB) Phase Noise

SSB phase noise \( L(\Delta f) \) is the normalized version of \( S_{v_o}(f) \), which is defined as

\[
L(\Delta f) = \frac{S_{v_o}(f_0 + \Delta f)}{A^2/2} \tag{3.6}
\]

\( L(\Delta f) \) is the noise power, relative to the total power in the signal, in a bandwidth of
1Hz in a single sideband at a frequency offset \( \Delta f \) from the carrier frequency \( f_0 \). The value of \( L(\Delta f) \) is commonly expressed as \( 10 \log[L(\Delta f)] \) dBc/Hz. dBc means “dB relative to carrier,” where the term “carrier” actually means total power in the signal. In fact, in SpectreRF\textsuperscript{TM}, \( L(\Delta f) \) is calculated by the noise power divide fundamental frequency power, not the total power. This is a good approximation for a sinewave oscillator output, but is not correct for other waveforms such as square wave.

### 3.2.3. \( S_\phi(f) \): Baseband spectrum of the phase noise \( \phi(t) \)

Both \( S_\phi(f) \) and \( L(\Delta f) \) are spectra of the physical RF signal \( v_o(t) \). Their peaks are at the carrier frequency \( f_0 \), and their sidebands are located at either side of the peaks. Contrarily, \( S_\phi(f) \) is defined as a low-pass, single-side spectrum of phase noise modulation \( \phi(t) \). This baseband phase noise expression is more convenient for use in our calculations. J.A.Barnes et.al. [3.5] showed that the continuous phase noise spectra can be well approximated as

\[
S_\phi(f) = \frac{c_4}{f^4} + \frac{c_2}{f^2} + \frac{c_1}{f} + c_0,
\]

where \( c_i \) is a constant.

The \( \frac{c_4}{f^4} \) term is the result of random walking noises which modulate the frequency. It is only relevant to consider for high-precision frequency standards, i.e., atomic frequency standards, at frequency well below 1Hz. This term can be neglected in case of PLLs.

The \( \frac{c_2}{f^2} \) term is due to flicker noises which modulate the frequency, also called flicker FM phase noise. For a high frequency reference PLLs, this component comes from the VCO, and can be greatly suppressed by the loop. Moreover, when calculating the period jitter from phase noise, the contribution of this phase noise component is very small [3.6]. Therefore, we do not account for this noise, unless the corner between \( \frac{c_3}{f^3} \) term and \( \frac{c_2}{f^2} \) term, flicker corner, is beyond the PLL loop bandwidth.
The $\frac{C_2}{f^2}$ term comes from white noise that modulates the frequency, also called white FM phase noise. This phase noise is the most relevant one in oscillators and PLLs. Most of the phase noise as referred to in this work, relates to this phase noise component.

The $\frac{C_1}{f}$ term is caused by flicker noise phase modulation, often called flicker PM phase noise. Typically, it is only present in a narrow frequency range, and sometimes even overlapping with white FM phase noise. Therefore, we do not consider this phase noise component in this work.

Finally, $c_o$ is the noise floor due to white noise phase modulation. For PLLs, this noise comes from driven components which do not influence the oscillation frequency, e.g., the frequency divider and other digital logic and buffer circuits. These circuits add uncorrelated phase noise to the noise floor. In fact, most of the jitter contributed by clock buffers is from this part. It is considered an important component in this work.

Figure 3.4 shows a graphical representation of expression (3.7). In a log-log plot, this expression provides a piece-wise linear representation of the phase noise spectrum and frequency dependency. Each line segment has different slopes as illustrated in Figure 3.4.
In summary, we will consider only the $\frac{c_2}{f^2}$ and $c_0$ phase noise parts which are the result of white noise sources. Consequently, we simplify expression (3.6) to

$$S_\phi(f) = \frac{c_2}{f^2} + c_0 \quad (3.8)$$

### 3.3. Phase noise and jitter relationship

Phase noise is a continuous stochastic process indicating random accelerations and decelerations in phase $\phi$ as an oscillator orbits at a nominally constant frequency $f_0$ in steady state [3.6]. Jitter arises from sampling the orbit at certain points (transition points). The two are fundamentally different and the relationship is not obvious. In this section we will derive simplified relationships between jitter and phase noise.

A noisy clock output signal $v_n(t)$ can be expressed as a noise-free signal $v(t)$, plus a noise $n(t)$. An alternative representation is to add a jitter term $j(t)$ to time $t$. Yet an-
other representation is use phase noise \( \phi(t) \) instead of the jitter term, since \( j(t) \) can be translated to phase by multiply \( 2\pi f_0 \). This gives

\[
\nu_n(t) = \nu(t) + n(t) \\
= \nu[t + j(t)] \\
= \nu[t + \phi(t) / 2\pi f_0]
\]

For time points when \( \nu_n(t) \) is positive-going and crossing the threshold value, normally zero for sinewave and \( V_{dd}/2 \) for a digital clock, we obtain a sequence of time points \( \{\tau_i\} \)

\[
\{\tau_i\} = \{t_i + j(t_i)\} = \{t_i + \phi(t_i) / 2\pi f_0\} .
\]

While combining (3.2) and (3.10), we obtain the following expression for period jitter

\[
J^2 = \text{var} \left[ \frac{\Delta \phi(t_i)}{2\pi f_0} \right] = \frac{\text{var}[\Delta \phi(t_i)]}{4\pi^2 f_0^2}
\]

where \( f_0 \) is the oscillation frequency, and \( \Delta \phi(t_i) = \phi(t_{i+1}) - \phi(t_i) \).

The variance of \( \Delta \phi(t_i) \) can be calculated by using the Wiener-Khinchine theorem [3.7]. The deducing procedure is shown in Appendix 3A. Finally we get the exact relationship between jitter and phase noise, shown in expression (3.12).

\[
J^2 = \frac{\text{var}[\Delta \phi(t_i)]}{4\pi^2 f_0^2} = \frac{1}{4\pi^2 f_0^2} \int_0^{f_0/2} S_{\Delta \phi_{fold}}(f) df
\]

In the expression (3.12), \( S_{\Delta \phi_{fold}}(f) \) is the folded version of \( S_{\Delta \phi}(f) \) by sample effect and defined only over the frequency range \([0, f_0/2]\).

In practice, the phase noise of an oscillator is very small for frequencies beyond \( f_0/2 \). As a result, the spectrum folding of \( S_{\Delta \phi}(f) \) due to sampling can be neglected. Therefore, the relationship between period jitter and phase noise can be approximated with a simpler expression. By combining (3.12) and other expressions in Appendix 3A, we
obtain the commonly used general form of the jitter and phase noise relationship.

\[
J^2 = \frac{1}{4\pi^2} \int_0^\infty S_{\Delta \phi}(f) df = \sum_0^\infty S_{\phi}(f) \frac{\sin^2(\pi f/f_0)}{(\pi f_0)^2} df
\] (3.13)

To further simplify (3.13), we will now determine jitter and phase noise relationship for the special case when phase noise arises from white noise sources only. Next, we will consider phase noise \( S_{\phi}(f) \) that consists of two components, namely \( \frac{c_2}{f^2} \) and \( c_0 \) as shown in (3.8).

### 3.3.1. White PM phase noise only (noise floor): \( S_{\phi}(f) = c_0 \)

For this phase noise component, the integration result of (3.13) is infinite when the upper integration limit is infinite, which means that the jitter is infinitely large. The error comes from the upper limit of the integration. In fact, the noise floor is influenced by the spectrum folding. The spectrum folding due to sampling effect makes the integration upper limit finite, as in case of (3.12). Lee et.al. showed that the upper integration limit can be approximated by \( f_0/2 \) in case of white PM phase noise [3.8]. As a result, (3.13) can be re-written to

\[
J^2 = \frac{c_0}{(2\pi)^3 f_0} = \frac{1}{4\pi^2 f_0} S_{\phi}(f) \] (3.14)

### 3.3.2. White FM phase noise only (-20dB/dec): \( S_{\phi}(f) = \frac{c_2}{f^2} \)

The integration of (3.13) is finite in case of white FM phase noise. Lee et.al. showed the use of an upper integration limit of \( \infty \) for this noise component. Therefore, we obtain

\[
J^2 = \int_0^\infty \frac{c_2}{f^2} \cdot \frac{\sin^2(\pi f/f_0)}{(\pi f_0)^2} df = \frac{c_2}{\pi^3 f_0^3} \int_0^\infty \frac{\sin^2 x}{x^2} dx = \frac{c_2}{\pi^3 f_0^3} \cdot \frac{\pi}{2} = \frac{c_2}{2 f_0^3} = S_{\phi}(f) \cdot \frac{f^2}{2 f_0^3}
\] (3.15)

Finally, we have obtained simple jitter and phase noise relationships in the presence of white noise only. The relationship found for the case of white PM phase noise (noise floor) only is suitable for driven systems in which an output event occurs as a direct result of, and some time after, an input event. The jitter appears as a modulation of the
phase of the output. So the jitter produced by such systems is also called synchronous jitter, phase modulated or PM jitter. The relationship found for the case of white FM phase noise (-20dB/dec part) only is suitable for autonomous systems such as oscillators. The jitter appears as a modulation of the frequency of the output, which is why it is sometimes referred to as accumulating jitter, frequency modulated or FM jitter.

3.4. Power supply noise (PSN) determined jitter

The amount of jitter in a clock generator is strongly dependent on the quality of the power supply voltage. Since the L-CGU needs to operate from a digital ‘noisy’ supply voltage, a power supply noise (PSN) model is needed for analyzing the jitter performance. Our analysis is constrained to the PSN influence on the VCO performance, because most of the jitter comes from the VCO in well-designed PLLs.

Within the IC power domains, the PSN is caused by the switching logic gates inside the digital blocks. The exact PSN spectrum is different from power domain to power domain, and from chip to chip. Therefore, we have developed a general PSN model for our purpose. Every digital circuit design has a requirement for maximum acceptable power supply voltage variation as a consequence to meet performance specifications. A commonly used maximum power supply voltage variation is ±10% of the nominal $V_{dd}$.

We use the same value in this work. Since our L-CGU needs to be implemented in 65nm LP-CMOS, its nominal $V_{dd}$ equals 1.2V and a maximum $V_{dd}$ variation of 120mV will be tolerated.

3.4.1. Time-domain PSN analysis

We assume a transient PSN that is described by a Gaussian distribution with a zero-mean value and a 3σ value equal to 10% of $V_{dd}$.

$$V_{dd} = V_{dd_{nom}} + \nu_n, \quad \nu_n: \text{Gaussian distribution} \quad \begin{cases} \mu_{\nu_n} : 0 \\ \sigma_{\nu_n} : 0.1\times V_{dd_{nom}} / 3 = 0.04V \end{cases}$$ (3.16)

The oscillation frequency is sensitive to $V_{dd}$ described by a frequency-voltage sensitivity $K_{Vdd}$. The oscillation frequency under PSN conditions becomes
\[ f = f_0 + K_{V_{dd}}V_n \quad f: \text{Gaussian distribution} \]
\[ \begin{cases} \mu_f: & f_0 \\ \sigma_f: & K_{V_{dd}}\sigma_v \end{cases} \] (3.17)

The oscillation period equals \(1/f\), and may be no longer Gaussian distributed. However, when the PSN is much smaller than the nominal \(V_{dd}\), the following linear approximation can be made:

\[ T = \frac{1}{f} = T_0 + \Delta T \approx T_0 + \left. \frac{dT}{df} \right|_{f=f_0} \Delta f \quad T: \text{Gaussian distribution} \]
\[ \begin{cases} \mu_T: & \frac{1}{f_0} \\ \sigma_T: & \frac{K_{V_{dd}}\sigma_v}{f_0^2} \end{cases} \] (3.18)

In case \(\mu_f >> \sigma_f\), that is to say \(\mu_f \geq 10\sigma_f\), the oscillation period \(T = \frac{1}{f}\) can assumed to be a Gaussian distribution. For this case, the period jitter can be determined by

\[ J = \sigma_T = \frac{K_{V_{dd}}\sigma_v}{f_0^2} \] (3.19)

This expression will give us an upper bound of the period jitter, as we will see later. For other conditions, the oscillation period can not be treated as a Gaussian distribution, and the previous expression for period jitter is not valid.

### 3.4.2 Frequency-domain PSN analysis

In the previous analysis we have obtained jitter due to normally distributed PSN in time domain, which has no relationship to the frequency spectrum. In this section we will develop a PSN model accounting for this relationship.

The phase noise induced by PSN can be expressed in (3.20) [3.6].

\[ S_p(f) = \frac{K_{V_{dd}}^2}{f^2} V_n^2(f) \] (3.20)

By combining (3.13) and (3.20), we obtain the general relationship for period jitter for any PSN spectrum:
Chapter 3  Jitter Performance Models

\[
S_p(f) = \frac{K_{\text{Vdd}}^2}{f^2} S_{v_i}(f) \]

\[
J^2 = \int_0^\infty S_p(f) \frac{\sin^2 \left( \frac{\pi f}{f_0} \right)}{\left( \frac{\pi f}{f_0} \right)^2} df
\]

Typically, the PSN spectrum is of a band limited nature [3.9]. We assume such PSN spectrum with a noise bandwidth of \( f_{NB} \) and a magnitude of \( N_{\text{color}} \). The maximum noise power has been calculated assuming the normally distributed PSN as shown in (3.16). Figure 3.6 shows a graphical representation of the PSN spectrum for three different noise bandwidths.

\[
S_{v_i}(f)
\]

\[\sigma_{v_i}^2 = N_{\text{color} i} f_{NB i} \]

**Figure 3.5**  Example colored noise spectra of PSN with same noise variance

Based on the colored noise spectrum, the period jitter can be expressed as

\[
J = \frac{\sigma_{v_i} K_{\text{Vdd}}}{f_0^2} F \left( \frac{f_{NB}}{f_0} \right)
\]

and

\[
F \left( \frac{f_{NB}}{f_0} \right) = \left( \frac{f_0}{\pi f_{NB}} \right)^{1/2} \int_0^{f_{NB}} \frac{\sin^2 x}{x^2} dx
\]

Expression (3.23) can not be expressed in a closed-form. From numerical analysis we
have found that the solution of this expression is always smaller than 1 (see Figure 3.7).

![Figure 3.6 Numerical solution of expression (3.23)](image)

Therefore, the following relation for period jitter holds

\[ J = \frac{\sigma_v K_{Vdd}}{f_0^2} F \left( \frac{f_{NB}}{f_0} \right) \leq \frac{\sigma_v K_{Vdd}}{f_0^2} \]  

(3.24)

The maximum jitter is reached when the PSN spectrum equals to \( \sigma_v^2 \delta(f) \). In practice, the PSN spectrum can not be a delta function, and (3.19) gives an overestimated result. The results of (3.23) for \( f_{NB}=f_0 \) shows that the period jitter is 0.6719 times the value as obtained from (3.19). The actual value of \( f_{NB} \) is dependent on the chip design and package parasitics, but may be smaller than \( f_0 \). In modern IC designs, \( f_{NB} \) is in the range of hundreds of MHz.

It is more convenient to use a white noise PSN spectrum instead of a colored one. We compared both spectra with equal noise spectrum amplitude for the case of white noise and \( f_0 \) bandwidth colored noise (which means \( N_{white}=N_{color} \)). For white noise, the period jitter can be calculated by

\[ J = \frac{K_{Vdd}}{\sqrt{2} f_0^{3/2}} \sqrt{N_{white}} = \frac{K_{Vdd} \sigma_v}{\sqrt{2} f_0^2} = 0.707 \frac{K_{Vdd} \sigma_v}{f_0} \]  

(3.25)
For $f_0$ bandwidth colored noise, the period jitter can be gotten from figure 3.6 and expressed in (3.26)

$$J = \frac{K_{\text{yld}} \sigma_n}{f_0^2} \cdot 0.6719$$

(3.26)

The resulted jitter of (3.25) and (3.26) is much closed. It means that we can use the white PSN spectrum with the amplitude equal to $f_0$ bandwidth colored noise. The resulted jitter is $\sqrt{2}$ times smaller than the over estimated one from (3.19), which is considered as a reasonable approximation.

3.5. Jitter analysis in CMOS circuits

Before discussing in detail the L-CGU, we will first conclude this chapter by elaborating the jitter characteristics of several CMOS circuits. The analysis of such circuits is valuable, since they are used as the cornerstones of the clock distribution network in digital circuits. In this section we analyze the jitter characteristics of a single inverter and an inverter chain.

3.5.1. A single CMOS inverter

The most simple CMOS circuit is the inverter. There are two kinds of noise sources in an inverter that contribute to jitter. The first noise source is intrinsic noise due to e.g., channel noise in MOS devices. The second noise source is extrinsic noise such as PSN. While the former noise source can not be suppressed, it is the case for the latter noise source. Typically, extrinsic noise is the dominant in digital CMOS circuits.

3.5.1.1 Intrinsic noise injected jitter

The intrinsic noise sources that contribute to phase noise and jitter have been analyzed by Abidi et.al. [3.9]. We follow his approach, but applied several changes in the expressions.

![Figure 3.7 Inverter with positive input step signal [3.9]](image)
Consider the case of a rising input step voltage of the inverter as shown in Figure 3.8. The PMOS is shut off, and the NMOS is discharging $C$ from $V_{dd}$ to 0. For this case, the propagation delay is referred to as $t_{dN}$. The inverter switching threshold is assumed to be located at $V_{dd}/2$. Furthermore, we assume that even if the NMOS enters triode during $t_{dN}$, its drain current $I_{D\text{Nsat}}$ will not change appreciably. Therefore, the output voltage crosses the switching threshold with a slope equal to

$$\frac{dv_{\text{out}}}{dt} = I_{D\text{Nsat}} / C$$ \hspace{1cm} (3.27)

For calculating jitter, the output voltage noise $n(t)$ at the switching threshold should be calculated first. This voltage noise can then be used to calculate jitter by using the signal slope characteristics, as illustrated in Figure 3.9. For simplicity, we assume that the jitter of the rising or falling transitions is equal.

Recall (3.9) for expressing a noisy clock output signal $v_n(t)$. Using a Taylor series expansion to approximate (3.9), the period jitter $J$ can be calculated

$$v_n(t) \approx v(t) + \frac{dv(t)}{dt} j(t) \quad \text{with} \quad n(t) = \frac{dv(t)}{dt} j(t)$$ \hspace{1cm} (3.28)

$$J^2 = \text{var}[j(t_{i+1}) - j(t_i)] = 2 \text{var}[j(t_i)]$$ \hspace{1cm} (3.29)

We assume stationary or cyclostationary noise, which is uncorrelated between time $t_{i+1}$ and $t_i$. By combining (3.28) and (3.29) we can calculate the jitter based on the output
voltage slope at the transition time. The resulting expression becomes

\[ J^2 = 2 \text{var}[j(t_i)] = 2 \text{var}[n(t_i)] \cdot \left( \frac{1}{d\text{v}(t_i)/dt} \right)^2 \]  \hspace{1cm} (3.30)

Next we determine the expression of \( \text{var}[n(t_i)] \). The details of this derivation can be found in [3.9]. Its result, together with (3.27) and (3.29) give the following expression of period jitter

\[ J^2 = 2 \text{var}[n(t_{dn})] \cdot \left( \frac{1}{d\text{v}(t_{dn})/dt} \right)^2 = \frac{S_i}{I_{DNsat}^2} t_{dn} \]  \hspace{1cm} (3.31)

where \( I_{DNsat} \) is the current that charges capacitor \( C \) over a time window \( t_{dn} \). The spectral density of current noise \( i_n \) is

\[ S_i = 4kT\gamma_N g_{DS0} = 4kT\gamma_N g_m = 4kT\gamma_N \frac{\alpha \cdot I_{DNsat}}{V_{DD} - V_{DN}} \]  \hspace{1cm} (3.32)

where \( \alpha \) is the velocity saturation index from Sakurai’s alpha power model [3.10]. The \( \alpha \) is 2 for long channel devices, and about 1.3 for short channel devices.

Finally, we obtain a compact expression for jitter caused by current noise integrating on the capacitor \( C \) by combining (3.31) and (3.32)

\[ J^2 = \frac{S_i}{I_{DNsat}^2} t_{dn} = \frac{4akT\gamma_N t_{dn}}{I_{DNsat} (V_{DD} - V_{DN})} \]  \hspace{1cm} (3.33)

Jitter is also influenced by initial noise on capacitor \( C \), prior to the switching event, due to the channel resistance of the PMOS pull-up device. The mean square noise and the associated jitter of this initial noise are

\[ \text{var}[n_{ini}] = kT/C \]

\[ J^2 = 2 \frac{\text{var}[n_{ini}]}{(I_{DNsat}/C)^2} = 2 \frac{kTC}{I_{DNsat}^2} \]  \hspace{1cm} (3.34)

The expression of the total jitter due to these uncorrelated noise sources becomes

\[ J^2 = \frac{4akT\gamma_N t_{dn}}{I_{DNsat} (V_{DD} - V_{DN})} + 2 \frac{kTC}{I_{DNsat}^2} \]  \hspace{1cm} (3.35)
Since the total jitter does not influence the driving signal, the phase noise can be obtained from the relation between period jitter and white PM phase noise, as shown in (3.14).

### 3.5.1.2 Extrinsic noise injected jitter

Consider a CMOS inverter driven by ideal clock source under PSN conditions. Like before, the jitter can be calculated from the output voltage noise and the output voltage slope at the switching threshold of the inverter. The output voltage slope can be obtained from (3.27) while replacing $I_{D_{\text{Noat}}}$ with $I_D$ to have a generic expression.

Consider the case of rising output voltage of the inverter under PSN as shown in Figure 3.10. We assume that noise is injected only at the $V_{dd}$ side, i.e. the ground is free of noise. The NMOS is shut off, and the PMOS is charging $C$ from 0 to $V_{dd}$. The noise current that charges capacitor $C$ can be calculated from the common gate configuration.

$$i_n = g_m v_{ddn}$$

(3.36)

where $v_{ddn}$ is the voltage noise at power supply $V_{dd}$.

Now we follow the same approach as before in case of the intrinsic noise injected jitter. The output voltage noise $n(t_{dp})$ at the switching threshold can be calculated as follows.

$$n(t_{dp}) = \frac{1}{C} \int_0^{t_c} i_n dt = \frac{g_m}{C} \int_0^{t_c} v_{ddn} dt$$

(3.37)

$$\text{var}[n(t_{dp})] = \frac{g_m^2}{C^2} S_{vddn} \frac{t_{dp}}{2}$$

(3.38)

$S_{vddn}$ is the power noise spectrum and we assume white noise. In such cases, the period
jitter due to PSN for a rising output transition is

\[
J^2 = 2 \text{var}[n(t_{dp})] \left( \frac{1}{dV_{out}/dt} \right)^2
\]

\[
= 2 \frac{g_m^2}{C^2} S_{vddn} \frac{I_{dp}}{2} \frac{C^2}{I_{DP}^2} = \frac{g_m^2}{I_{DP}^2} S_{vddn} I_{DP}
\]

\[
= \frac{\alpha^2}{(V_{dd} - V_t)^2} S_{vddn} I_{DP}
\]

(3.39)

where \( \alpha \) is Sakurai’s velocity saturation index.

Jitter is also influenced by initial noise on capacitor \( C \), prior to the falling output switching event, due to the channel resistance of the PMOS pull-up device.

\[
\text{var}[n(t_{dn})] = S_{vddn} \cdot \frac{1}{4R_p C}
\]

\[
J^2 = 2 \text{var}[n(t_{dn})] \left( \frac{1}{\text{slop}} \right)^2 = \frac{S_{vddn} C}{2R_p I_{DN}^2}
\]

(3.40)

where \( R_p \) is the PMOS channel resistance in triode region. As compared to the jitter associated to the rising output edge, this jitter is normally much smaller.

When the case of PSN at the \( V_{ss} \) connection, \( S_{vssn} \), is considered, a similar observation is made as in case of PSN at the \( V_{dd} \) connection (\( S_{vddn} \)). The only difference is that the results for the falling and rising output edge are reversed. As a result, the expressions of total jitter are as follows.

For the rising output edge of the inverter:

\[
J^2 = \frac{\alpha^2}{(V_{dd} - V_t)^2} S_{vddn} I_{DP} + \frac{S_{vssn} C}{2R_N I_{DN}^2}
\]

(3.41)

For falling output edge of the inverter:

\[
J^2 = \frac{\alpha^2}{(V_{dd} - V_t)^2} S_{vssn} I_{DN} + \frac{S_{vddn} C}{2R_p I_{DN}^2}
\]

(3.42)

When operating at ‘noisy’ digital power supplies, the jitter due to extrinsic noise domi-
nates the jitter caused by intrinsic noise sources.

### 3.5.2. A CMOS Inverter Chain

The analysis for a single CMOS inverter can be easily extended to a chain of inverters. In this section we will present the results for an inverter chain that consists of $M$ stages. We assume that the MOS devices of each stage have equal $t_d$, $V_i$ and $I_D$.

#### 3.5.2.1 Intrinsic noise injected jitter

The intrinsic noise sources of different inverters are uncorrelated. Therefore, the total jitter is the mean square sum of the jitter of a single inverter.

Suppose there are $M$ stages in the chain. The total period jitter of the inverter chain can be described as

$$J^2 = \sum_{i=1}^{M} \left[ \frac{2\alpha k T t_{bi}}{I_{Di}(V_{DD} - V_a)} (Y_{Ni} + Y_{Pi}) + 2 \frac{k T C_i}{I_{Di}} \right]$$

(3.43)

#### 3.5.2.2 Extrinsic noise injected jitter

When considering PSN, the analysis of jitter for the inverter chain is more complicated than in case of a single inverter. Since all inverter stages share the same power supply, the PSN may not be correlated because each inverter switches at a different point in time. We assumed PSN to be white and uncorrelated for each stage when the output transition occurs.

Also, the jitter performance of the first stage and the other stages is different. The first stage is driven by an ideal clock signal which is free of noise. Therefore, we compose the total jitter of the inverter chain by the jitter of first stage and the jitter of other stages.

For an inverter chain that includes $M$ stages where $M$ is a even number. Considering PSN at the $V_{dd}$ side only, the total period jitter can be expressed as below.

For a rising input transition

$$J^2 = \frac{S_{vdda_{ddn}}}{2R_{p_{-1}}} \frac{C_i}{I_{DN_{-1}}} + \sum_{i=1}^{M/2} \frac{\alpha^2}{(V_{dd} - V_{ip})^2} S_{vdda_{dp_{-2i}}} + \sum_{i=1}^{M/2-1} \left( \frac{\alpha^2}{(V_{dd} - V_{ip})^2} S_{vdda_{dn_{-2i+1}}} + \frac{S_{vdda_{ddn}}}{2R_{p_{-2i+1}}} \frac{C_{2i+1}}{I_{DN_{-2i+1}}} \right)$$

(3.44)
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For a falling input transition:

\[
J^2 = \frac{\alpha^2}{(V_{dd} - V_{dp})^2} S_{vddl_dP_1} + \sum_{i=1}^{M/2-1} \frac{\alpha^2}{(V_{dd} - V_{dp})^2} S_{vddl_dP_{2i+1}} + \sum_{i=1}^{M/2} \left( \frac{\alpha^2}{(V_{dd} - V_{ni})^2} S_{vddl_dN_{2i}} + \frac{S_{vdd}}{2R_{p_{2i}} I_{DN_{2i}}} \right)
\]

(3.45)

Expressions (3.44) and (3.45) can be simplified under certain assumptions. Typically, the initial noise due to the MOS channel resistance is smaller than the PSN injected noise. If all stages in the inverter chain including the first stage, have the same jitter performance, (3.44) and (3.45) can be simplified to

\[
J^2 \approx \frac{\alpha^2}{(V_{dd} - V_{i})^2} S_{vddl_d_{total}}
\]

(3.46)

where \( t_{d_{total}} \) is the total delay of the inverter chain.

SpectreRF\textsuperscript{TM} circuit simulations have been performed to validate the correctness of (3.46). A six stage inverter chain has been used as test-circuit in 65nm CMOS. For each stage, the PMOS and NMOS transistors use W/L of 0.83\( \mu \)m/0.06\( \mu \)m, and 0.58\( \mu \)m/0.06\( \mu \)m, respectively. Each stage is loaded by a capacitor. The input of the chain is driven by a pulse-shaped input voltage with signal slopes of 100ps. All stages can have by different power supply noise sources or the same power supply noise sources. The nominal V\(_{dd}\) is 1.2V. The test-circuit and test-bench has been illustrated in Figure 3.11.

![Figure 3.10 Test-bench for the jitter of an inverter chain](image)

For obtaining valid results, the simulation conditions for SpectreRF\textsuperscript{TM} should be properly set. The number of harmonics in PSS, and the maximum sideband in PNOISE
should be set large enough to cover all noise folding. If the number of harmonics is set correctly, the increase of this number will lead to a different jitter simulation result.

(a) Period jitter versus load capacitance

(b) inverter chain propagation delay versus load capacitance

Figure 3.11 Simulation results of the inverter chain
We set the number of harmonics to cover a frequency band of about 50GHz, e.g., 1000 harmonics for 50MHz input, and 100 harmonics for a 500MHz input.

Simulation results for different load capacitor values while using a 50MHz input signal in Figure 3.12. A white-noise PSN spectrum amplitude of 1.227E-12 $V^2/Hz$ has been used. The pink line in Figure 3.12a is the calculation using (3.46). The lower red line is the simulated jitter when all stages use one common power noise source. The upper blue line is the simulated jitter when each stage has its own independent power noise source, each having the same noise value. Observe the trend lines of (3.46) and the case of a common PSN noise source are the same, while (3.46) somewhat overestimates the jitter. Although the case of independent PSN sources shows a slightly different trend, (3.46) is still able to approximate jitter with sufficient accuracy. Furthermore, we have observed that the period jitter is not influenced by the change of input frequency.

The previous analysis showed similar results in case of PSN at the $V_{ss}$ connection. Therefore, the simplified expression for this case becomes

$$J^2 \approx \frac{\alpha^2}{(V_{dd} - V_{t})^2} S_{vsn} t_{d \_total}$$

(3.47)

Finally, the period jitter of inverter chain due to PSN in both $V_{dd}$ and $V_{ss}$ connection is

$$J^2 \approx \frac{\alpha^2}{(V_{dd} - V_{t})^2} (S_{vsn} + S_{vddn}) t_{d \_total}$$

(3.48)

It shows that when power ground noise dominate, the jitter of clock buffer chain is mainly determined by the noise level in power ground connections ($S_{vsn} + S_{vddn}$), the total delay of the clock buffer chain ($t_{d \_total}$), the supply voltage level ($V_{dd}$), threshold ($V_{t}$) and technology ($\alpha$). Normally, clock buffers are powered by digital supply and use the same technology as digital circuits. So the only thing we can control is the total delay of the clock buffer chain ($t_{d \_total}$). No matter what the number and size of clock buffers are, if the total delay of the clock buffers is reduced, then the jitter of them will be reduced too.
3.6. Summary
The most critical requirement of the L-CGU is jitter. Thus Chapter 3 is all focus on jitter analysis. Since phase noise brings much more insight in oscillator designs than jitter, we first discuss the jitter and phase noise relationship as well as the definitions for jitter and phase noise in the beginning of Chapter 3. After that, the power supply noise together its influence to jitter are studied. Finally the jitter contributed by the clock buffer (inverter chain) under power supply noise is examined and a useful estimation formula is presented.

Appendix 3A
In this appendix we will derive the expression for jitter and phase noise relationship. The derivation is used as background for section 3.3.

The variance of $\Delta \phi(t_i)$ can be calculated by using the Wiener-Khinchine theorem. The approach is to first determine the spectral density of $\Delta \phi(t_i)$, and then integrating over the entire frequency range. Since $\phi(t)$ is a continuously evolving variable, $\Delta \phi(t)$ is found by the first-difference operation for a time period equal to the clock period $T_0 = 1/f_0$. Thus the spectral density $S_{\Delta \phi}(f)$ is given by

$$S_{\Delta \phi}(f) = S_{\phi}(f) \left| 1 - e^{-2\pi f / f_0} \right|^2 = 4S_{\phi}(f) \sin^2 \left( \pi f / f_0 \right)$$  \hspace{1cm} (3A.1)

So far we have obtained the spectral density of $\Delta \phi(t)$. How about the spectral density of $\Delta \phi(t_i)$? The $\Delta \phi(t_i)$ is the sampled version of $\Delta \phi(t)$ at a sampling frequency $f_0$. According to the Nyquist sampling theory, the spectral density of $\Delta \phi(t_i)$ is the folded version of $S_{\Delta \phi}(f)$ and defined only over the frequency range $[3.0, f_0/2]$. Figure 3A.1 shows an illustration of the noise folding in which $S_{\Delta \phi\_fold}(f)$ the spectral density of sampled sequence $\Delta \phi(t_i)$.
Mathematically, the spectrum folding operation can be expressed as

$$\hat{S}_{\Delta \phi \_\text{fold}}(f) = \sum_{k=-\infty}^{\infty} \hat{S}_{\Delta \phi}(f - kf_0)$$  \hfill (3A.2)

To properly account for spectrum folding, we have used the double-sided representation $\hat{S}_{\Delta \phi \_\text{fold}}(f)$ and $\hat{S}_{\Delta \phi}(f)$ for $S_{\Delta \phi \_\text{fold}}(f)$ and $S_{\Delta \phi}(f)$, respectively. Being a real sequence, the spectrum $\hat{S}_{\Delta \phi \_\text{fold}}(f)$ is also conjugate symmetric about 0. For the single-sided transform, $S_{\Delta \phi \_\text{fold}}(f)$, the frequency range of interest becomes 0 to $f_0/2$. Everything outside this range is either a repeat, or a repeat of a mirror image. Contributions to this range from large values of $k$ in (3A.2) are negligible because the finite bandwidth of $S_{\phi}(f)$.

Now we can obtain the relationship between period jitter and phase noise using the Wiener-Khinchine theorem. Expression (3A.3) shows the exact form of that relationship:
\begin{equation}
J^2 = \frac{\text{var}\[\Delta \phi(t_i)\]}{4\pi^2 f_0^2} = \frac{1}{4\pi^2 f_0^2} \int_0^{f_0} S_{\Delta \phi_{fold}}(f)df
\end{equation}

(3A.3)

Reference


4. Design Space Exploration of L-CGU Components

Since the L-CGU needs to be supplied from a digital ‘noise’ supply, it is extremely difficult to generate an accurate clock signal when operating in such a harsh environment. We qualify the L-CGU by analyzing its clock jitter performance as it is perceived as an important parameter by digital IC designers. In this chapter, we perform a design space exploration for the L-CGU to determine suitable circuit solutions to meet design specifications. First, we will define the L-CGU basic structure. Next, we will discuss the different L-CGU components required, and analyze their jitter performance. Finally, we propose an L-CGU solution.

4.1. L-CGU Basic Architecture

The L-CGU design specifications have been summarized in Table 2.1, as shown in Chapter 2. Eleven different output frequencies are required ranging from 550MHz down to 50MHz with frequency steps of 50MHz. The support of these many frequencies can be done through frequency multiplication or frequency division.

Frequency multiplication is based on the use of an integer-N phase locked loop (PLL). The reference clock should be an integer $N$ times lower frequency than the required PLL output frequency. Examples of the reference clock are 50MHz, 25MHz, 10MHz. Since the input or reference clock is lower or equal to the PLL output frequency, this solution is referred to as frequency multiplication. An integer-N PLL can achieve low jitter and phase noise, while offering good frequency stability. Its locking time is determined by its bandwidth and normally in the microsecond range. Another solution is frequency division, which requires an oscillator that runs at a common multiple of the required frequency. All of the required frequencies are obtained by division from the common multiple frequency. Yet the common multiple frequency for 50MHz to 550MHz is too high (16.632THz). One may also use fractional dividers which require a lower multiple frequency. For example, if using 550MHz as the common multiple frequency, the division factors will be 11, 11/2, 11/3..., 11/10. However, the implementation of the fractional divider is complicated, while it suffers from large jitter and phase noise. In this project we will use both frequency multiplication and frequency division for the L-CGU. The final L-CGU design will be composed by an integer-N PLL to-
together with a programmable frequency divider at the PLL output, which will be introduced in Chapter 5.

The heart of the L-CGU is an integer-N PLL, whose generic structure is shown in Figure 4.1. Let’s consider the how to meet the requirements in Table 2.1. For a low-area solution, the voltage-controlled oscillator (VCO) and loop filter (LF) should be implemented to be as small as possible since these building blocks will occupy most of the area. The most power-hungry part of the PLL is the VCO. However, also the frequency divider (FDIV) could be power hungry if its input frequency is so high that can not be realized by CMOS digital logic. For the other parts, the power consumption is low because of their low operating frequencies, and since most of them are fully realized by using CMOS digital logic. The PLL structure inherently guarantees no glitch at the output when switching between frequency points.

In case frequency transitioning time is critical, a solution could be the use of two PLLs in the L-CGU. A frequency transitioning is done by simply switching between the clock outputs of the PLLs which requires additional digital control logic. This concept was demonstrated for a digital ring-oscillator based CGU by Meijer et.al. [4.1]. If the switching time is not critical, only one PLL is sufficient.

The most critical L-CGU design requirement is the jitter performance. Since the power supply and ground are shared with digital blocks, PSN will worsen jitter performance to easily exceed the 30ps specification. In the following section, the individual L-CGU building blocks will be analyzed in detail, with a main focus on jitter performance.
4.2. Selection of a Suitable Oscillator Type

Oscillators are the heart of the PLL, thus they are the critical elements in every PLL design. For a good PLL design, the phase noise and jitter performance will be dominated by the oscillator. We examine the jitter and phase noise performance of different oscillator types. The purpose is to select a good oscillator for the L-CGU design.

There exist many kinds of oscillators. Each oscillator type has its own benefits and drawbacks. In our analysis we will focus on the phase noise (or jitter) performance aspect only, while considering two categories of oscillators: RC oscillators and LC oscillators. The RC oscillators can be divided into three types: inverter-based ring oscillator, differential ring oscillator and relaxation oscillator. The LC oscillators commonly have four types: Colpitts LC oscillator, current-biased LC oscillator, voltage-biased LC oscillator, and complementary LC oscillator.

Figure 4.2 Different oscillator types
oscillator and complementary LC oscillator. Figure 4.2 shows a schematic overview of the full or part of these seven oscillators. The oscillators are compared on different quality metrics as summarized in Table 4.1. In common, the oscillator performance is compared by using a normalized figure of merit (FOM) that includes performance, phase noise and power consumption. The FOM is expressed as [4.2]

\[
FOM = \left( \frac{f_0}{f} \right)^2 \frac{1}{L(f)P}
\]

(4.1)

Where \( P \) is the power consumption in mW, \( L(f) \) is the phase noise at an offset \( f \) from a center frequency \( f_0 \).

In this section we will compare the oscillators one by one to find a suitable oscillator for the L-CGU design.

### 4.2.1. Inverter-Based Ring Oscillator

A thorough analysis of the inverter-based ring oscillator has been performed by Abidi et.al. [4.3]. We will use their results without detailed derivations of the relevant expressions.

The oscillation frequency \( f_0 \) of inverter-based ring oscillator depends on the number of stages in the ring, and the stage delay. This can be expressed as

\[
f_0 = \frac{I}{NV_{dd}C}
\]

(4.2)

\( I \) and \( C \) are the saturation current and load capacitance, both for a single stage, \( V_{dd} \) is the supply voltage, and \( N \) is the number of stages. The maximum frequency is achieved when the ring oscillator contains three stages only. Since only one stage is switching at a given point in time, this type of ring oscillator is consuming only little power consumption independent of the number of stages.

The period jitter can be calculated by

\[
J^2 = \frac{2kT}{f_0} \left( \frac{\gamma_N + \gamma_P}{V_{dd} - V_t} + \frac{1}{V_{dd}} \right)
\]

(4.3)
where $V_t$ is the device threshold voltage, and $\gamma_N$ and $\gamma_P$ are the channel noise parameters of NMOS and PMOS transistors, respectively. The phase noise can be calculated by

$$S_\phi(f) = \frac{4kT}{I} \left( \frac{1}{V_{dd} - V_t} (\gamma_N + \gamma_P) + \frac{1}{V_{dd}} \right) \left( \frac{f_0}{f} \right)^2$$ (4.4)

In practice, the oscillator designers often use SSB phase noise $L(f)$. When using the narrow band FM approximation, $L(f) = \frac{S_\phi(f)}{2}$ [4.4], the SSB phase noise is

$$L(f) = \frac{2kT}{I} \left( \frac{1}{V_{dd} - V_t} (\gamma_N + \gamma_P) + \frac{1}{V_{dd}} \right) \left( \frac{f_0}{f} \right)^2$$ (4.5)

For long-channel devices, $\gamma_N$ and $\gamma_P$ can achieve its minimum value of $2/3$. In 65nm CMOS technology, the $V_t$ is about $\frac{V_{dd}}{3}$. So the minimum jitter and SSB phase noise are

$$J_{\min}^2 = \frac{6kT}{I f_0 V_{dd}} \quad \text{and} \quad L_{\min}(f) = \frac{6kT}{I V_{dd}} \left( \frac{f_0}{f} \right)^2$$ (4.6)

Consequently, the best achievable FOM is

$$FOM_{\text{best}} = \frac{0.167}{kT}$$ (4.7)

### 4.2.2. Differential Ring-Oscillator

A thorough analysis of the differential ring-oscillator has also been performed by Abidi et.al. [4.3]. We will use their results without detailed derivations of the relevant expressions.

The oscillation frequency of differential ring-oscillator is

$$f_0 = \frac{1}{2 \ln 2 \cdot NRC} = \frac{I_{\text{tail}}}{2 \ln 2 \cdot NCV_{op}}$$ (4.8)

where $N$ is the number of stages, $R$ is the load resistor per stage, $C$ is the loading capacitor per stage, $I_{\text{tail}}$ is the tail current per stage, and $V_{op}$ is the output voltage amplitude.
The period jitter can be calculated by
\[ J^2 = \frac{2kT}{f_0 T_{\text{tail}}^2 \ln 2} \left( \gamma_t \frac{g_{mt}}{2} + \gamma_d \frac{3g_{md}}{4} + \frac{1}{R} \right) \] (4.9)

where \( \gamma_t \) and \( \gamma_d \) are the channel noise parameters of tail transistor and differential-pair transistors, \( g_{mt} \) and \( g_{md} \) are the associated transconductances.

The SSB phase noise is
\[ L(f) = \frac{2kT}{I_{\text{tail}}^2 \ln 2} \left( \gamma_t \frac{1}{V_{\text{eff}t}} + \gamma_d \frac{3}{4V_{\text{eff}d}} + \frac{1}{V_{op}} \right) \left( \frac{f_0}{f} \right)^2 \] (4.10)

For long-channel devices, \( \gamma_t \) and \( \gamma_d \) can achieve its minimum value of 2/3. \( V_{op} \) should be made as large as possible to achieve better phase noise. When \( V_{op} \) is maximized,
\[ \frac{V_{op}}{2} + V_{\text{eff}d} + V_{\text{eff}t} = V_{dd} \] (4.11)

Using the Lagrange multiplier method, we can obtain the minimum value of the middle part of (4.10). The minimum value is achieved when \( V_{op}=0.634V_{dd}, V_{\text{eff}d}=0.317V_{dd} \) and \( V_{\text{eff}t}=0.366V_{dd} \). As a result, the minimum jitter and SSB phase noise are
\[ J_{\text{min}}^2 = \frac{14.4kT}{f_0 T_{\text{tail}} V_{dd}} \quad \text{and} \quad L_{\text{min}}(f) = \frac{14.4kT}{I_{\text{tail}} V_{dd}} \left( \frac{f_0}{f} \right)^2 \] (4.12)

The power consumption of differential ring-oscillator is much larger than an inverter-based ring oscillator. This is because each stage consumes a static current, thus its total power is the sum of the power of each stage.

The highest achievable FOM is
\[ FOM_{\text{best}} = \frac{0.07}{NkT} \]  

(4.13)

### 4.2.3. Relaxation Oscillator

The relaxation oscillator has been analyzed by Reza Navid et.al. [4.5]. We will use their results without detailed derivations of the relevant expressions. The minimum SSB phase noise with considering only resistor noise is

\[ L_{\text{min}}(f) \approx \frac{3.1kT}{P} \left( \frac{f_0}{f} \right)^2 \]  

(4.14)

As a result, the best achievable FOM is

\[ FOM_{\text{best}} = \frac{0.33}{kT} \]  

(4.15)

Reza Navid et.al. mentioned that the SSB phase noise as expressed in (4.14) is usually more than 20dB higher than the actual measured one [4.5]. So the (4.14) and (4.15) are not of much practical value.

The oscillation frequency of relaxation oscillator is

\[ f_0 = \frac{1}{RC \ln \left( \frac{V_{dd} - V_1}{V_{dd} - V_2} \right)} \]  

(4.16)

where \( V_1 \) and \( V_2 \) are the two trigger threshold voltage in the relaxation oscillator.

### 4.2.4. Colpitts LC Oscillator

Typically, Colpitts LC oscillators are used in combination with an external inductor, because it only needs one connection for the external inductor. A detailed analysis of the Colpitts LC oscillator has been performed by Emad Hegazi et.al. [4.6]. From [4.6] is clear that the phase noise is not better than that of differential LC oscillators. Moreover, it is difficult to guarantee that the oscillation is starting up. Consequently, the Colpitts LC oscillator has been rarely used in IC designs, and will not be considered further.
4.2.5. Differential LC Oscillators
Differential LC oscillators have been analyzed by Emad Hegazi et.al. [4.6]. We will use their results without detailed derivations of the relevant expressions.

All LC oscillators have the same expression for operation frequency.

\[ f_0 = \frac{1}{\sqrt{LC}} \]  \hspace{1cm} (4.17)

The SSB phase noise can be written like

\[ L(f) = \frac{4kTR}{V_{out}^2} F \left( \frac{f_0}{2Qf} \right)^2 \]  \hspace{1cm} (4.18)

where \( R \) is the LC tank resistor, \( Q \) is the quality factor of LC tank, \( F \) is the oscillator noise figure, and \( V_{out} \) is the voltage amplitude of the output signal.

For a current-biased LC oscillator, \( F \) can be expressed as

\[ F = 1 + \gamma_d + \frac{1}{4} \gamma_i g_{mR} \]  \hspace{1cm} (4.19)

where 1 is contributed by the LC tank resistor \( R \), \( \gamma_d \) is due to the differential-pair transistor channel noise, and the dominant term \( \frac{1}{4} \gamma_i g_{mR} \) is due to the tail current source transistor.

For a voltage-biased LC oscillator, \( F \) can be expressed as

\[ F = 1 + \gamma_d \]  \hspace{1cm} (4.20)

For a complementary LC oscillator, \( F \) can be expressed as

\[ F = 1 + \gamma_{dN} + \gamma_{dp} + \frac{1}{4} \gamma_i g_{mR} \]  \hspace{1cm} (4.21)

where \( \gamma_{dN} \) and \( \gamma_{dp} \) are the differential-pair channel noise parameters for NMOS and PMOS devices.
Next we will compare the best FOM for these three types of differential LC oscillators. For the current-biased type, the best FOM is obtained when the $\frac{1}{4} \gamma_c g_m R$ term in (4.19) is eliminated by noise filtering, and $\gamma_d$ is set to a minimum value of 2/3. Therefore, the best achievable FOM becomes

$$FOM_{best} = \frac{2}{\pi} \frac{\alpha Q^2}{kT(1 + \gamma_d)} = \frac{0.38\alpha Q^2}{kT} \quad \text{and} \quad \alpha = \frac{V_{out}}{V_{dd}} \leq 2 \quad (4.22)$$

For the voltage-biased type, the best FOM is obtained when $\gamma_d$ achieves its minimum value of 2/3. The $Q$ value is only half of the unloaded LC tank $Q$ value because of the heavy load of the differential pair. Therefore, the best achievable FOM becomes

$$FOM_{best} = \frac{2}{\pi} \frac{\alpha Q^2}{4kT(1 + \gamma_d)} = \frac{0.19Q^2}{kT} \quad \text{and} \quad \alpha = \frac{V_{out}}{V_{dd}} = 2 \quad (4.23)$$

For the complementary type, the best FOM is obtained when the $\frac{1}{4} \gamma_c g_m R$ term in (4.21) is eliminated by noise filtering, and $\gamma_{dn}, \gamma_{dp}$ are set to the minimum value of 2/3. Moreover, the complementary differential LC oscillator can save nearly half of the power that is consumed by the current biased type. The best achievable FOM is

$$FOM_{best} = \frac{4}{\pi} \frac{\alpha Q^2}{kT(1 + \gamma_{dn} + \gamma_{dp})} = \frac{0.55\alpha Q^2}{kT} \quad \text{and} \quad \alpha = \frac{V_{out}}{V_{dd}} \leq 1 \quad (4.24)$$

### 4.2.6. Oscillator Type Selection

An overview of the quality metrics for the previous oscillators has been given in Table 4.1. We will now trade-off the different oscillator types to select suitable oscillators for the L-CGU design.

First, a suitable oscillator should be easy to design and guarantee oscillation start-up. Since the relaxation oscillator and Colpitts LC oscillator do not satisfy this requirement, they have been ruled out.

Second, a suitable oscillator should have a low sensitivity to power supply variation.
because of the low jitter requirement. The differential structures are capable to convert the power supply noise to common-mode, and suppress it. Therefore, this type of oscillator is better suitable than a single-ended type. This rules out both the inverter-based ring-oscillator and the voltage-biased differential LC oscillator. The latter one is not a real differential oscillator due to the absence of the tail current source.

The remaining oscillators are the differential ring-oscillator, the current-biased differential LC oscillator, and complementary differential LC oscillator. All of these oscillators could be the candidates. However, the complementary differential LC oscillator can perform the same as the current-biased LC differential oscillator while consuming only half current. Hence only two oscillators are valuable in the L-CGU applications: the differential ring oscillator and complementary differential LC oscillator.

Normally, the complementary differential LC oscillator can achieve the best phase noise and jitter performance, while the differential ring oscillator consume much smaller current and area. In the project, the most important requirement for the L-CGU is the jitter. So based on the consideration of low jitter, we use both of these two oscillators to design the L-CGU. Finally, through comparing the measurement results, the best oscillator type for the L-CGU can be obtained.

### 4.3. Analysis of the PLL Building Blocks

In this section we will discuss the different PLL building blocks of which the L-CGU is composed. Like before, we mainly focus on the jitter and phase noise performance. For each building block, we will present analytical formulae to give insight in its performance.

#### 4.3.1. Voltage-Control Oscillator Considerations

Table 4.1 gives an overview of fixed frequency point oscillators. Since the PLL makes use of a VCO, a frequency tuning function needs to be added to enable the oscillator to generate the multiple required clock frequencies. The presence of a frequency tuning function worsens the jitter and phase noise performance of the oscillator, because noise will be coupled to the VCO’s tuning port that modulates the frequency.

The phase noise added by tuning port noise can be calculated as
where $S_n(f)$ is the voltage noise spectra at VCO tuning port and $K_{VCO}$ is the frequency tuning slope. From (4.25), we observe that there exist two approaches for reducing phase noise. The first approach is to suppress the noise injected at VCO tuning port.
<table>
<thead>
<tr>
<th>Oscillator Type</th>
<th>Performance</th>
<th>Figure of Merit</th>
<th>Power Supply Rejection</th>
<th>Tuning Range</th>
<th>Frequency (Stability)</th>
<th>Frequency Band</th>
<th>Integrate Ability</th>
<th>Cost (Area)</th>
</tr>
</thead>
<tbody>
<tr>
<td>RC Oscillator</td>
<td>Inverter Based</td>
<td>$FOM = \left( \frac{f_0}{A_f} \right)^2 \frac{1}{kT} \cdot P$</td>
<td>$\frac{\partial f_0}{\partial V_{DD}} = I_0 \cdot \frac{1}{NC \cdot V_{DD}^2}$</td>
<td>Inherently better than inverter based ring oscillator</td>
<td>$f_0 = \frac{I_0}{NV_{DD}C}$</td>
<td>Up to $\frac{1}{6\tau_d}$</td>
<td>Smallest</td>
<td></td>
</tr>
<tr>
<td></td>
<td>Differential</td>
<td>$0.083 \cdot \frac{1}{N \cdot kT}$ (N stages)</td>
<td>(Depends on single end or differential)</td>
<td>$f_0 = \frac{1}{2\ln 2 \cdot NRC}$</td>
<td>$I_0 = \frac{2\ln 2 \cdot NCV_{out}}{\tau_d}$</td>
<td>($\tau_d = \frac{CV_{out}}{2I_0}$)</td>
<td>(Delay per inverter)</td>
<td>Middle</td>
</tr>
<tr>
<td></td>
<td>Relaxation</td>
<td>$0.33 \cdot \frac{1}{kT}$ (Only ideal RC noise, NOT include comparator noise)</td>
<td></td>
<td></td>
<td>$f_0 = \frac{1}{RC \ln \left( \frac{V_{DD} - V_2}{V_{DD} - V_1} \right)}$</td>
<td>Maximum frequency much lower than ring and LC oscillator</td>
<td>Do NOT need process options in CMOS065</td>
<td></td>
</tr>
<tr>
<td>LC Oscillator</td>
<td>Colpitts</td>
<td>Not better than differential pair LC oscillator</td>
<td>Worse than differential pair LC oscillator</td>
<td></td>
<td></td>
<td></td>
<td>Largest (200-200-300-300µm²)</td>
<td></td>
</tr>
<tr>
<td></td>
<td>Current Biased</td>
<td>$0.38\alpha Q^2 \cdot \frac{1}{kT}$</td>
<td>$\alpha \leq 2$</td>
<td>$Q$ times better than differential ring oscillator</td>
<td>$f_0 = \frac{1}{\sqrt{LC}}$</td>
<td>Up to $f_{max}$</td>
<td>(Seldom use in sub-GHz)</td>
<td></td>
</tr>
<tr>
<td></td>
<td>Voltage Biased</td>
<td>$0.19Q^2 \cdot \frac{1}{kT}$</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>Complementary</td>
<td>$0.55\alpha Q^2 \cdot \frac{1}{kT}$</td>
<td>$\alpha \leq 1$</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
This may require significant design effort and complexity, especially in the presence of PSN. Another way to reduce the phase noise is lowering $K_{\text{VCXO}}$. This approach is more robust because it does not require the suppression of noise, but it needs more consideration on how to cover the whole frequency range. For the L-CGU we use the latter approach which will be shown in more detail in Section 5.2.2 of the next chapter.

### 4.3.2. Frequency Divider

The frequency divider (FDIV) reduces a high input frequency to a lower one. The division ratio can be an even number, an integer or even a fractional number. Ideally, the FDIV does not add noise to its output signal. Moreover, it is capable of even reducing the phase noise that is present in its input signal. Next, we will discuss the FDIV jitter and phase noise characteristics. For this purpose, we make use of the phase model of FDIV is shown in Figure 4.3.

![Frequency divider phase model](image)

**Figure 4.3** Frequency divider phase model

\[ f_{\text{out}} = \frac{f_{\text{in}}}{N}, \quad \phi_{\text{out}} = \frac{\phi_{\text{in}}}{N}, \quad S_{\phi_{\text{out}}}(f) = \frac{S_{\phi_{\text{in}}}(f)}{N^2} \]

The FDIV output jitter can be obtained from both the white PM phase noise and white FM phase noise (see section 3.3). For the white PM phase noise (noise floor), the FDIV output jitter is

\[ J_{\text{out, PM}}^2 = S_{\phi_{\text{out}}}(f) \cdot \frac{1}{4\pi^2 f_{\text{out}}} = \frac{S_{\phi_{\text{in}}}(f)}{N^2} \cdot \frac{1}{4\pi^2 f_{\text{in}}/N} = \frac{1}{N} \cdot \frac{S_{\phi_{\text{in}}}(f)}{N^2} \cdot \frac{1}{4\pi^2 f_{\text{in}}/N} = \frac{J_{\text{in, PM}}^2}{N} \]

For the white FM phase noise (-20dBc per decade part), the FDIV output jitter is

\[ J_{\text{out, FM}}^2 = S_{\phi_{\text{out}}}(f) \cdot \frac{f_{\text{in}}^2}{2 f_{\text{out}}^3} = \frac{S_{\phi_{\text{in}}}(f)}{N^2} \cdot \frac{f_{\text{in}}^2}{2 f_{\text{in}}^3/N^3} = N \cdot \frac{S_{\phi_{\text{in}}}(f)}{N^2} \cdot \frac{f_{\text{in}}^2}{2 f_{\text{in}}^3} = N \cdot J_{\text{in, FM}}^2 \]

The total FDIV output jitter is found by taking the mean square sum of these two parts. The strict analysis of the FDIV phase noise and jitter is complicated because of different
possible FDIV implementations. Commonly, the approach is to first calculate the output noise voltage at the switching threshold and divide it by the voltage slope at that point.

\[
S_\phi(f) = \left[2\pi f_{out} \frac{1}{dv_{out}/dt}\right]^2 S_{n_{\text{fold}}}(f) \tag{4.29}
\]

\[
J^2 = 2 \text{var}[n(iT)] \left[\frac{1}{dv_{out}/dt}\right]^2 \tag{4.30}
\]

\[
\text{var}[n(iT)] = S_{n_{\text{fold}}}(f) \frac{f_{out}}{2} \tag{4.31}
\]

Expression (4.31) has been confirmed with Wiener-Khinchine theorem [4.7].

In practice, the FDIV will contribute to jitter and phase noise as a result of intrinsic and extrinsic noise sources. Since the FDIV is a driven system, its phase noise can not influence the output frequency of the PLL. The FDIV noise will only convert to the white PM phase noise, e.g., it increases the phase noise floor. Fortunately, the FDIV phase noise can be reduced using re-synchronization. The output signal of the FDIV is re-synchronized with the FDIV input signal, which reduces any phase noise degradation due to the FDIV. An example of re-synchronization is shown in Figure 4.4.
Figure 4.4 Re-synchronization for a Frequency Divider

For an asynchronous FDIV, the noise of each stage is accumulated and the FDIV output signal will contain this accumulated noise. A resynchronized FDIV can remove the accumulated noises by using resynchronized D flip-flop. As a result, the FDIV output noise will only contain the noise of the D flip-flop, and significant noise reduction is achieved. One should make the FDIV delay without resynchronization smaller than half of the input period (T/2). Otherwise, the circuit may become unstable after adding a resynchronized D flip-flop.

In this work we will focus on programmable integer number FDIV. The design details will be provided in the next chapter.

4.3.3. Phase Frequency Detector and Charge Pump

The phase frequency detector (PFD) compares the phase difference of a reference and feedback signal. It produces pulse output signals (up and down), whose pulse widths are proportional to the phase difference. The PFD does not continuously monitor the phase difference, but only compares the phase at the rising (or falling) edge of the inputs. In this respect, the circuit operation may cause pulse width and timing mismatch issues at its output. The charge pump (CP) converts the PFD output signals to a current output. This output will be immediately passed to a low pass filter that is designed to suppress signals at frequencies of 1/T and above. In most cases the pulsed nature of this signal can be ignored in favor of its average value, $\langle i_{cp} \rangle$. The transfer function of the combined PFD-CP is

$$\langle i_{cp} \rangle = \frac{K_{det}}{2\pi} (\phi_{ref} - \phi_{fd}) = \frac{I_{cp}}{2\pi} (\phi_{ref} - \phi_{fd}) = \frac{I_{cp}}{2\pi} \phi_{error}$$  \hspace{1cm} (4.32)

The logic model and phase model of PFD-CP is shown in Figure 4.5.

Next, we analyze the noise contribution of the PFD-CP. The intrinsic and extrinsic noises of PFD add jitter to its outputs, which in their turn add disturbance to the pulse width and timing of up down signal. This disturbance will affect the CP output $i_{cp}$ accordingly, which then converts to voltage noise through low pass filter and finally adds
to the control port of VCO. Now suppose the transfer function of the low pass filter is \( Z_{LF}(f) \). Then the phase noise due to PFD-CP output current \( i_{cp} \) is

\[
S_{\phi}(f) = \frac{K_{eCO}^2}{f^2} S_{i_{cp}}(f) |Z_{LF}(f)|^2
\]  

\( (4.33) \)

**Figure 4.5** The logic model and phase model of PFD-CP

The PFD-CP jitter and phase noise is caused by two effects. The first effect is because of random noise and PSN, which produces a continuous phase noise in the PLL. Fortunately, this contribution can be neglected because the charge pump is closed most of the time when the PLL is locked. The second effect is because of the spurious signals in the PLL output produced by the CP output current. This is the main jitter contribution to the jitter on which we will focus our analysis. The spurs show themselves at reference frequency \( f_{ref} \) and its harmonics, which are called reference spur. An illustration is shown in Figure 4.6.

There are two sources which produce reference spur. The first source is the noise produced by other components of PLL that modulate the phase error. The modulated phase error will modulate the PFD-CP current and generate reference spur. Figure 4.7 illustrates the \( i_{cp} \) pulse sequences generated by noise in PLL. The detail analysis is made in the book of Keliu Shu et.al [4.8].

The second source that produces the reference spur is the mismatch inside the PFD-CP.
The following analysis will assume no phase error input to PFD-CP for acquiring insight in the reference source contribution to the phase noise. Figure 4.8 illustrates the PFD-CP output current in one reference period $T_{ref}$ due to non-idealities of the charge pump.

Since the PFD-CP output current $i_{out}$ is a periodic signal with period of $T_{ref}$, it can be decomposed into a discrete Fourier series.
Thus the reference spur in the VCO phase noise is

\[
S_\phi(f_{\text{ref}}) = \frac{K_{\text{VCO}}^2}{f_{\text{ref}}^2} |\omega_1|^2 |Z_{L_F}(f_{\text{ref}})|^2
\]  

(4.35)

Figure 4.8 Charge-pump output current in locked state due to mismatch [4.8]

If we can get the \(c_1\), the reference spur can be calculated. The detail expression deducing is made in the book of Keliu Shu et.al [4.8]. Here we only show the results.

In Figure 4.8a, the pulse width of current \(I_{cp}\) is for compensating the leakage current \(I_{\text{leak}}\). The coefficient corresponding to the reference spur is

\[
|c_1| \approx I_{\text{leak}}
\]  

(4.36)

In Figure 4.8b, there is current mismatch between up and down current sources. The coefficient for the reference spur due to current mismatch is

\[
|c_1| \approx \pi \Delta I_{cp} \left( \frac{t_{\text{on}}}{T_{\text{ref}}} \right)^2
\]  

(4.37)

Figure 4.8c shows the PFD-CP output current due to the timing mismatch. It concerns
timing mismatch between the falling edges of up and down, which causes both a positive and negative current pulse $I_{cp}$ with a pulse width equal to the timing mismatch. The coefficient for the reference spur due to the timing mismatch is

$$|c_1| = 2\pi I_{cp} \frac{T}{T_{ref}} \frac{T_{on}}{T_{ref}}$$  \hspace{1cm} (4.38)

Besides the three kinds of mismatches as discussed above, the mismatches of clock feed-through and charge sharing of up and dn switches also contribute to the reference spur. Sometimes, dummy switches are used to reduce clock feed-through and charge sharing.

Note that in a PLL with on-chip loop filter and VCO, the reference spur can be partially contributed by the periodic PSN due to the periodic operation of the PFD, charge-pump and loop divider.

4.3.4. Loop Filter

In a PFD-CP PLL, the loop filter (LF) is a kind of trans-impedance. An example of the common structure is shown in Figure 4.9. The resistance and capacitance values are calculated based on the required PLL loop bandwidth and phase margin.

![Loop filter in a PFD-CP PLL](image)

*Figure 4.9  Loop filter in a PFD-CP PLL*

Normally, the capacitance values are very large which leads to a large LF layout area. The noise from ground and substrate can be coupled to the LF output very easily. See one simulation result example in figure 4.10. Since the LF output is directly connected to VCO tuning port, such noise coupling would degrade the jitter and phase noise performance. In this work, substrate shielding is not an option because the ground is shared
with digital blocks. The only viable way to reduce this noise coupling effect is to reduce
the VCO tuning slope $K_{VCO}$.

**Figure 4.10** Simulation result for the LF output at the condition of no noise,
with $Vdd$ noise and with $gnd$ noise.

### 4.4. Summary

In this chapter, we present our L-CGU solution. The L-CGU is based on an integer-N
PLL. The most important part in the L-CGU is the oscillator. In order to find the suit-
able oscillator type for the L-CGU application, seven different kinds of oscillators are
compared in phase noise, power consumption, area, power supply sensitivity, and inte-
gration capability. The two suitable oscillator types are chosen as the core for the L-
CGU. In the following sections, the jitters under power supply noise of clock buffer,
frequency divider (FDIV), phase frequency detector and charge pump (PFD-CP), loop
filter (LF) are analyzed. Next chapter we will show the detail design of the L-CGU,
which include both schematics and layouts.
Chapter 4  Design Space Exploration of L-CGU Components

Reference


5. L-CGU Design

So far we have discussed the requirements for the L-CGU. A detailed analysis has been performed on the most critical requirement, namely the jitter performance when operating from a digital ‘noisy’ supply. In this chapter we will present the L-CGU schematic designs and layouts implemented in a 65nm low-power CMOS technology. The simulation results that are shown in this chapter are based on Spectre™ circuit simulations using extracted layouts. The supply voltage for all circuits is 1.2V and can tolerate ±10% variations (1.08V~1.32V).

5.1. L-CGU System Architecture

The L-CGU is based on an integer-N PLL which produces all the required clock frequencies and control functions such as, e.g. frequency transitioning, clock gating and clock enabling. Control logic is used to provide an easy way for monitor and control the PLL working conditions. Since the working condition of the L-CGU is determined by the application, the control logic may be different from power domains to power domains. Normally the control logic will be designed by the system engineer who what to use the L-CGU. So in this thesis, only the integer-N PLL of the L-CGU is introduced. The control logics used in the thesis test chip are just some scan chain registers. Figure 5.1 shows a general block diagram of the L-CGU.

![General block diagram of the L-CGU](image)

Figure 5.1 General block diagram of the L-CGU

Figure 5.2 shows a block diagram of the integer-N PLL. The basic components are the
voltage-controlled oscillator (VCO), phase-frequency detector (PFD), charge pump (CP),
loop filter (LF), frequency dividers (FDIV), and a lock detector.

![Integer-N PLL structure](image)

**Figure 5.2** Integer-N PLL structure

The PLL output frequency, $f_{out}$, is $N/M$ times the reference frequency $f_{ref}$.

$$f_{out} = \frac{f_{VCO}}{M} = \frac{N \cdot f_{ref}}{M} \quad (5.1)$$

In this work, we use a 26MHz reference frequency that is commonly available in mobile systems, and generated by a crystal oscillator. Since $f_{out}$ is a multiplication of $f_{ref}$, the clock output frequencies are slightly shifted from the requirements shown in Table 2.1. The PLL output frequencies for given frequency divider settings are shown in Table 5.1.

<table>
<thead>
<tr>
<th>Frequency [MHz]</th>
<th>48.75</th>
<th>97.5</th>
<th>156</th>
<th>195</th>
<th>247</th>
<th>312</th>
<th>338</th>
<th>390</th>
<th>442</th>
<th>494</th>
<th>546</th>
</tr>
</thead>
<tbody>
<tr>
<td>N</td>
<td>15</td>
<td>15</td>
<td>12</td>
<td>15</td>
<td>19</td>
<td>12</td>
<td>13</td>
<td>15</td>
<td>17</td>
<td>19</td>
<td>21</td>
</tr>
<tr>
<td>M</td>
<td>8</td>
<td>4</td>
<td>2</td>
<td>2</td>
<td>2</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
</tr>
</tbody>
</table>

As compared to conventional integer-N PLLs, our integer-N PLL differs on two parts. The first one is the VCO design which is the most critical part in the PLL; it should generate a robust oscillation frequency insensitive to supply noise. We consider two types of VCO designs: 1) a differential ring-oscillator VCO, and 2) a differential LC VCO. In the course of this work we have designed two differential ring-oscillator VCOs and one differential LC VCO. The second part is the Lock Detector.
which is used to monitor the PLL status during frequency transitioning. It produces two output signals: no phase error (NPE) and Lock, which will be explained in section 5.7.

The PLL is a 3rd-order type II charge pump PLL. To make the PLL loop stable, its loop bandwidth $f_c$ is set to be tenth of the reference frequency: 2.6MHz.

$$f_c = \frac{I_{cp}K_{VCO}}{2\pi N} R_1 \frac{C_1}{C_1 + C_2} = \frac{f_{ref}}{10} = 2.6MHz \tag{5.2}$$

In (5.2), $I_{cp}$ is the charge pump current. $K_{VCO}$ is the VCO tuning sensitivity in (Hz/Volt). $R_1$, $C_1$ and $C_2$ are the components value in the loop filter (LF). The normalized third pole is set to be 9 to get fast lock [5.1].

$$b = \frac{\tau_2}{\tau_3} = 9 \tag{5.3}$$

where $\tau_2$ is the time constant of the “stabilizing” zero, and $\tau_3$ is the time constant of the pole which is used to attenuate the reference frequency and its harmonics. They will be discussed in Section 5.6.

In order to get the maximum phase margin, the normalized loop bandwidth is set to be 3.

$$K' = 2\pi f_c \tau_2 = \sqrt{b} = 3 \tag{5.4}$$

This gives a phase margin of $53^\circ$ [5.2].

### 5.2. Voltage Control Oscillator

The VCO determines most of the PLL performance, such as jitters, clock frequencies, power consumption, and the area occupation. We have developed three different VCO’s for trading-off L-CGU characteristics and comparison purposes. The design has been started with a differential ring-oscillator VCO, and a differential LC VCO. Later, we have improved the differential ring-oscillator VCO, and have developed a third VCO. Each VCO has been used to design and implement a PLL in 65nm CMOS. Next, we will discuss the different VCO designs in detail.
5.2.1. **Differential ring-oscillator VCO**

Figure 5.3 shows a simplified block diagram of the differential ring-oscillator VCO. Its oscillation frequency ranges from 624MHz up to 1092MHz. The Ring-VCO output frequency is divided by 2 to guarantee 50% duty cycle at the VCO output. Finally, the VCO output frequency ranges from 312MHz up to 546MHz.

![Figure 5.3 Structure of the differential ring-oscillator VCO](image)

5.2.1.1 **Schematics design for differential ring-oscillator VCO**

The implemented differential ring-oscillator VCO is based on the famous design of John G. Maneatis [5.3]. The delay cells in the ring-oscillator use symmetric loads as tuning resistors. The two tuning voltages, which tune the symmetric load PMOS and tail current source, are generated from replica bias. The sine-wave shaped output amplitude of the delay cell is impacted by the tuning voltage, and is not suitable as ring-VCO output. Therefore, a high gain buffer for generating a full voltage swing square wave. We refer to [5.3] for the detailed design considerations. Figure 5.4 shows the top-level circuit schematic of the differential ring-oscillator VCO. It consists of three delay stages, a replica bias circuit and an output buffer. The circuit schematics of the replica bias, differential delay cell, and output buffer are shown in Figure 5.5, Figure 5.6, and Figure 5.7, respectively.
Figure 5.4  Top level schematic of the differential ring VCO

Figure 5.5  Replica bias for tuning the VCO

Figure 5.6  Differential delay cell with symmetric load
Figure 5.7  VCO output buffer

One difference from [5.3] is that we add fixed capacitors to each differential delay cell. By using fixed capacitors, the influence of parasitic capacitances is reduced, which in its turn reduces the sensitivity to the power supply noise. To maximize the capacitance value of these capacitances, the number of the delay stages is set to a minimum of 3 stages.

The tail current for each delay cell is setting by the replica bias and in sequence controlled by the tuning voltage. So there is only one current which required to be biased outside. It is the bias current for the differential amplifier within the replica bias, which named “Ibias”. The normal current for “Ibias” is 45 μ A. Yet it needn’t to be very accurate. Current from 20 μ A to 70 μ A are all acceptable.

The power consumption of the differential ring-oscillator VCO is variable with output frequency. When operates at its highest required frequency 1.092GHz and fabricates at nominal process corner, the total current for the VCO is around 800 μ A.

5.2.1.2 Layout for differential ring-oscillator VCO
The layout design has a large impact on the final circuit performance. A badly designed layout increases the circuit parasitics, lowers the maximum operating frequency, worsens the noise coupling and makes the circuit mismatch unbalanced. Therefore, it is of prime
importance that the layout is carefully designed for achieving a good performing circuit. All differential transistor pairs make use of a common-centroid layout organization to ensure proper matching of transistor pairs [5.4].

The layout of the differential ring-oscillator VCO is shown in Figure 5.8. The layout consists of three parts. The bottom part is the replica bias, which processes the tuning signal from the LF output. The top part is the VCO output buffer that converts the differential output of the ring-oscillator to a full-swing square wave signal. The middle part consists of three differential delay cells that constitute the ring-oscillator. Their layout is stacked to make a symmetrical ring-oscillator layout. So any coupling noise will mostly convert to common mode noise. However, such layout configuration will make the wire connections among the delay cells unequal in length. Moreover, the output buffer is connected with the upper delay cell. This makes the delay cells to be not equally loaded, and the phase is not divided in exactly 120 degrees. Since we do not care about the phase at the VCO output, this layout configuration is acceptable.

The whole VCO layout is made to be as symmetrical as possible. Each transistor group is surrounded with a guard ring. The whole VCO is surrounded with power ground rings together with a big guard ring. The power and ground connections are made large in width (about 1µm) to reduce the resistance in the power ground networks. The area for the differential ring-oscillator VCO is 18 µm × 48 µm.

5.2.1.2 Simulations for differential ring-oscillator VCO

The VCO tuning range is found to be very large, e.g. from several tens of MHz to about 1.2GHz. Figure 5.9 shows the simulation results of the oscillation frequency versus tuning voltage. A tuning voltage has been applied from 0V up to 0.9V. The different lines indicate the results from five process corners: fnfp (purple), fnsp (blue), nominal (red), snfp (yellow), and snsp (light blue). The lines saturate for tuning voltages lower than 0.2V because the “vbp” output of replica bias (see Figure 5.5) can not follow the change of tuning voltage anymore.
Figure 5.8  Layout of the first differential ring-oscillator VCO

Power ring, ground ring and guard ring. They are stacked
Figure 5.9 Simulation results of oscillation frequency versus tuning voltage of the differential ring-oscillator VCO for various process corners

Figure 5.10 shows the simulated phase noise without any power supply noise. Figure 5.11 shows the simulated phase noise while applying white power supply noise according to our model shown in Section 3.4 using noise spectrum amplitude of about $1.23 \times 10^{-12} V^2/Hz$. A comparison of Figure 5.10 and Figure 5.11 shows that the phase noise becomes more than 30dB worse when power supply noise is present. While including the divide-by-2 frequency divider, we calculated the RMS jitter of the VCO at 546MHz. We observed a jitter of 3ps in case of no power supply noise, while the jitter with power supply noise is 108ps! Such large jitter cannot be tolerated for the L-CGU design.
Figure 5.10  Phase noise of the differential ring-oscillator VCO at 1092MHz, no power supply noise. RMS period jitter (at 546MHz): 3ps

Figure 5.11  Phase noise of the differential ring-oscillator VCO at 1092MHz, with power supply noise added. RMS period jitter (at 546MHz): 108ps
5.2.2. Reduce the jitter of the VCO under large power supply noise

In order to find the root cause of the large jitter in case of power supply noise, we analyzed the differential ring-oscillator VCO in more detail. The phase noise induced by power supply noise can be expressed as follows,

\[ L(f) = \frac{K_{vdd}^2}{2f^2} S_{vdd}(f) \tag{5.5} \]

\( S_{vdd}(f) \) is the power supply noise spectrum. \( K_{vdd} \) is the sensitivity of the VCO output frequency to the power supply variation. \( S_{vdd}(f) \) can not be lowered easily in this project, because not only the power supply of the L-CGU is shared with digital IP blocks, but also the L-CGU itself is totally embedded in the digital circuits. So the only way to reduce the phase noise is to reduce the frequency sensitivity \( K_{vdd} \). In fact, there are at least three ways to reduce the VCO sensitivity to power supply noise.

The first way is through balancing the load resistors. The power supply noise directly couples to the delay cell output through the load resistors (see Figure 5.12). Since this noise is common mode, it can greatly rejected by the next delay stage when the circuit is fully symmetric. However, mismatch may occur in the symmetric load PMOS pair, which makes their equivalent resistance not equal at all times. This makes common mode rejection ratio (CMRR) poor, and \( K_{vdd} \) is influenced.

![Figure 5.12 Power supply noise coupling to the output through load resistors](image-url)
Chapter 5  L-CGU Design

The second way is to reduce the power supply controlled parasitics. The VCO oscillation frequency is determined by the RC time constant of the delay cell. By making the RC time constant insensitive to power supply, the $K_{Vdd}$ can be reduced. When fixed load resistors and fixed capacitors are used, the parasitic capacitance change seen at the delay cell differential output changes because of a change in DC bias point (see Figure 5.13). Such change in DC bias point can reduced if the fixed resistance and fixed capacitance values dominate the parasitic ones. Moreover, a large tail current source impedance can also help to reduce $K_{Vdd}$. Unfortunately, there is not much voltage headroom for a stack of three transistors in case of the delay cell shown in Figure 5.6. Consequently, the tail current source operates close to the triode region, and its output impedance is not large. Also, symmetric load PMOS pairs add parasitic capacitances.

![Figure 5.13 Parasitics seen at the differential output of the delay cell](image)

The third way to reduce the VCO sensitivity to power supply noise is by accurate voltage control. In a differential ring VCO, the frequency tuning is realized through voltage control components, such as voltage control resistors or varactors. The value of such components is determined by the voltage apply at the tuning port and the voltage at the reference port. Normally the reference port is biased at a fixed DC value. Yet when power supply varies, the reference port no longer fixed any more. It is equal to applying a tuning voltage at the voltage control component. And as a result, the frequency will change with respect to the varying of the power supply. For example, in Figure 5.14, suppose the frequency is controlled by varactors. Then $vout^+$ and $vout^-$ are reference
ports. When Vdd changes, the DC bias voltages at vout+ and vout- are changed accordingly. It’s equal to tuning the varactors, although the voltages applied at tuning ports are not varied. Based on the above discussion, an immediate observation can be made: the larger the VCO tuning sensitivity $K_{VCO}$, the larger the power supply sensitivity $K_{Vdd}$.

Wide tuning VCOs often have poor phase noise performance when the power supply is noisy. In the designed a differential ring VCO, the tuning range is wide and $K_{VCO}$ is very large (about 3.3GHz/V). Moreover, the replica bias will induce some power supply noise to the tuning port. So the phase noise is very bad when we add power supply noise.

![Figure 5.14](image)

**Figure 5.14** Reference ports of the tuning components influenced by power supply noise

### 5.2.3. Improved differential ring-oscillator VCO

Based on the previous observations, we have designed an improved differential ring-oscillator VCO. Figure 5.15 shows a schematic diagram of its delay cell. We use a special capacitor tuning instead of resistor tuning; a number of small tuning varactors are connected in parallel with a switchable large fixed capacitor tank. This lowers the influence of parasitic capacitances at the differential output nodes. Moreover, we use fixed polysilicon resistor loads. This provides better load resistor balancing and high CMRR for power supply noise. Also, it increases the voltage head room for the tail current source, which can now operate strong inversion to increase its output impedance.
Figure 5.15  Sketched circuit for the improved differential ring VCO delay cell

5.2.3.1 Schematics design for the improved differential ring-oscillator VCO

Figure 5.16 shows the top-level schematic of the improved differential ring-oscillator VCO. The two footer NMOS transistors are for bias and shutdown purpose. The circuit schematic of the differential delay cell is shown in Figure 5.17. The VCO output buffer is the same as shown in Figure 5.7.

Figure 5.16  Top level schematics for improved differential ring VCO

Unlike the previous differential ring-oscillator VCO, the tail current for each delay cell is constant and does not change with the VCO operating frequency. The outside applied
bias current (through “Ibias”) is 30 μ A. Under this bias setting, the tail current for each delay cell is 100 μ A. The bias current range for “Ibias” is from 20 μ A to 40 μ A.

The total current consumption of the improved differential ring-oscillator VCO is around 550 μ A.

![Schematic circuit for the delay cell of the improved VCO](image)

**Figure 5.17** Schematic circuit for the delay cell of the improved VCO

5.2.3.2 Layout for the improved differential ring-oscillator VCO

Figure 5.18 shows the layout of the improved differential ring-oscillator VCO. The layout structure is similar to Figure 5.8 except the replica bias which is not needed. The VCO output buffer is the same as used before. Some decoupling capacitors are used to fill in the space at both sides of the buffer. The delay cells of the improved differential ring-oscillator VCO are larger as compared to the previous ones. This is because the fixed metal capacitors in the tuning tank are larger (45fF compare to 10fF). Between these metal capacitors, some space should be kept to reduce the direct coupling, otherwise the VCO oscillation frequency will reduce and the switches in the tuning tank will
loose their effect. Moreover, power and ground rings are used to surround each delay cell. They can reduce the direct coupling between delay cells through the edges of the big metal capacitors. The whole layout of the improved differential ring VCO is designed to be fully symmetrical, and the area is $55 \mu m \times 42 \mu m$.

**Figure 5.18** Layout of the improved differential ring-oscillator VCO

### 5.2.3.3 Simulations for the improved differential ring-oscillator VCO

The simulated frequency tuning range and phase noise are shown in Figure 5.19 and Figure 5.20, respectively.

Again, we calculated the RMS period jitter after the divide-by-2 frequency divider using the same method as before, e.g. the jitter at 546MHz VCO output. We observed a jitter of 2.1ps in case of no power supply noise, while the jitter with both power and ground
Figure 5.19  Simulated frequency tuning range at nominal process corner

Figure 5.20  Simulated phase noise at 1.092GHz under no power supply noise, only power noise and only ground noise situations
noise is 7.4ps. We conclude that the improved differential ring-oscillator VCO is much better than old one.

The drawbacks of the improved differential ring VCO is the larger area cost and the need of initial calibration. From the simulation result show in Table 6.1 of Chapter 6, we see that the frequency range of the improved differential ring-oscillator VCO is limited, and does not cover the basic requirement, i.e. 624MHz up to 1092MHz for all process corners. One solution to this problem is to redesign this VCO and add another switch capacitor pair to the tuning tank to enlarge the frequency range. However, adding such capacitor pair will increase the circuit area significantly because of the large required capacitance value. Moreover, the maximum VCO frequency will be reduced due to the large parasitic capacitive loading. Another solution is to increase the tuning varactor value to cover more frequency range. Unfortunately, this will increase $K_{VCO}$, which in its turn, will degrade the VCO jitter performance. We do not use follow this solution, but rather we use a calibration approach to solve this problem. The calibration approach of the improved differential ring VCO based PLL is shown in Appendix 5B.

5.2.4. **LC VCO part**

The second type of L-CGU is based on an LC VCO. We developed an LC VCO based PLL for test and comparison purposes against the differential ring-oscillator based PLLs. Figure 5.21 shows a simplified block diagram of the LC VCO. A high-frequency frequency divider (FDIV X) has been designed allowing the VCO to operate at an oscillation frequency in between 3.9GHz and 4.42GHz with a small tuning range (of about 12%). Table 5.2 shows the relation of the frequency divider number, $X$, and the VCO output frequency.

![Figure 5.21 LC VCO part structure](image)
The design of the frequency divider (FDIV X) will be discussed in section 5.3.

Table 5.2  Frequency plan for LC VCO and the divider number of FDIV X

<table>
<thead>
<tr>
<th>Output frequency [MHz]</th>
<th>312</th>
<th>338</th>
<th>390</th>
<th>442</th>
<th>494</th>
<th>546</th>
</tr>
</thead>
<tbody>
<tr>
<td>LC-VCO frequency [MHz]</td>
<td>4368</td>
<td>4056</td>
<td>3900</td>
<td>4420</td>
<td>3952</td>
<td>4368</td>
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<tr>
<td>X</td>
<td>14</td>
<td>12</td>
<td>10</td>
<td>10</td>
<td>8</td>
<td>8</td>
</tr>
</tbody>
</table>

5.2.4.1 Schematics design for the LC VCO

Figure 5.22 shows the toplevel schematic of the LC VCO. The circuit details of the LC VCO and the output buffer are shown in Figure 5.23 and Figure 5.24, respectively. The LC VCO is implemented as a complementary LC oscillator. The varactor is implemented as NMOS in Nwell for biasing the device in the depletion region or accumulation region only. The varactor can achieve a very wide tuning range, because its reference port is biased at about $V_{DD}/2$. Moreover, the oscillator voltage swing is limited in between 0 and $V_{DD}$ which enables a reliable operation in a 65nm low-power CMOS technology. We make use of two control signals (switch0 and switch1 in Figure 5.22, and Figure 5.23) for frequency calibration purposes. The reason for such calibration is because the inductor model provided in the technology library may not be very accurate. In the final implementation, the use of these calibration signals and the associated capacitor tanks may be discarded.

![Figure 5.22  Top level schematic of the LC VCO](image)
Figure 5.23  Circuit schematic of the LC VCO

Figure 5.24  Circuit schematic of the VCO output buffer
The buffer shown in Figure 5.24 has two functions. First, it isolates the VCO and the FDIV X which followed the VCO. Second, it converts the dc bias of the VCO output (0V) to the required level by the FDIV X (0.8V). For the isolation function, two small capacitors (10fF) are used at the input of the buffer. They will largely reduce the influence from the output buffer to the VCO, and achieve very good isolation. At the same time, the small capacitors serials in the signal route will reduce the amplitude of the VCO output signals, which will increase the noise floor. Yet the increase of the noise floor will not be found because it is overwhelmed by the large power supply noise. For the bias level converting, the buffer used the similar circuits, the same components values, and same bias current with the FDIV X, together with negative DC feedback.

There are two outside bias pins for the LC VCO. One for oscillator core (“Itail”) and the other for the buffer (“Ibuffer”). Normally, the bias current for “Itail” is 40μA, and “Ibuffer” is 50μA. Under these bias currents, the tail current of the complementary LC oscillator is 350μA, and the tail current for each differential stage in the buffer is 150μA. The bias range for “Itail” is from 30μA to 80μA, and the bias range for “Ibuffer” is from 45μA to 80μA. The total current consumption of the LC VCO (include the buffer) is around 750μA.

5.2.4.2 Layout for the LC VCO

Figure 5.25 shows the layout of the LC VCO. This is the biggest VCO due to the need of a spiral inductor. We used a “0” shaped inductor which was supported in the technology library. The spiral inductor use three top layer (metal 6, metal 7 and AP) with inner diameter 60μm, line width 10μm, spacing 2.51μm and 5 loops. The inductance is about 3.079nH with serial resistance about 1.64Ω. The differential floating shield inductor we used in the layout may pick up some noise, which is difficult to simulate. Measurement results should provide insight on this.

The LC VCO is surrounded by power and ground rings together with a big guard ring. These rings are stacked and at least “5*W” (50μm) far from the inductor. Otherwise the
magnetic coupling from the inductor to the rings will reduce the Q value of the resonate tank. The power and ground rings are interrupted at the top centre to avoid the induced loop current. The wire connections between the inductor to the oscillator circuit are made by stacked metal layers, which can achieve both low resistance and low capacitance. The whole layout is designed to be fully symmetrical. The area is about $360 \mu m \times 325 \mu m$.

![Figure 5.25 Layout of the LC VCO](image)

**5.2.4.3 Simulations for the LC VCO**

Figure 5.26 illustrates the frequency range of the LC VCO at all possible calibrating situations. Figure 5.27 and Figure 5.28 show the phase noise at the LC-VCO output at 4.368GHz for the case without and with power supply noise, respectively. We have determined the RMS period jitter at VCO output at 546MHz. The jitter without power supply noise is found to be about 0.2ps, while the jitter with power supply noise is found to be about 10ps.
Figure 5.26 Frequency range at all calibration situations

Figure 5.27 LC VCO phase noise at 4.368GHz, no power supply noise
In this section, we have described three different VCO designs as developed in this work. The first differential ring-oscillator VCO is easy to use and is smallest in area, but suffers from the worst jitter performance under power supply noise conditions as compared to the other VCO’s. The improved differential ring-oscillator VCO offers a very good jitter performance, even under power supply noise conditions. However, it requires initial calibration for process condition compensation and it consumes more silicon area. The LC VCO has the largest silicon footprint, and it consumes the most power consumption. However, it is easy to use and offers a good jitter performance.

5.3. Frequency Divider (FDIV)
In this section we will show the design of the three frequency dividers (FDIV M, FDIV N, and FDIV X). The differential ring-oscillator VCO based PLL does not make use of the FDIV X frequency divider.

5.3.1. Schematic designs of FDIV
The simplest frequency divider is FDIV M for which the circuit schematic is shown in...
Figure 5.29. It divides the input clock frequency by a factor of 1, 2, 4, or 8 based on the selection signal (see Table 5.3). The FDIV M output is re-clocked by the clock frequency of two times the input one to get rid of the frequency divider jitter (the re-clocking is not shown in Figure 5.29). Using the FDIV M input to re-clock its output will not work, because the delay through the 4:1 MUX is simply too small when the FDIV M is set to be divide-by-1. In this case, the re-clocking D flip-flop can not produce a stable output signal when its data and clock input change at the same time.

![Circuit schematic of the frequency divider FDIV M](image)

**Figure 5.29** Circuit schematic of the frequency divider FDIV M

<table>
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<tr>
<th>p1</th>
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</tr>
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</tr>
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</tr>
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<td>1</td>
<td>1</td>
<td>÷8</td>
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</table>

The FDIV N is realized by using a special programmable frequency divider structure, as proposed by C. Vaucher [5.2] (shown in Figure 5.30). It is composed of a basic divide-by-2/3 cell as shown in Figure 5.31. This kind of frequency divider can achieve very wide divide range as well as a short propagation delay. Its division number can be set from ÷8 to ÷31, thereby it fully covers the required divide range: ÷12, ÷13, ÷15, ÷
17, \( \div 19 \), and \( \div 21 \). Table 5.4 shows the detailed settings of FDIV N. The FDIV N design has intrinsic support for re-clocking its output by its input. Consequently, one can get rid of most of the noise generated by the frequency divider circuits.

![Figure 5.30](image)

**Figure 5.30** Circuit schematic of the frequency divider FDIV N

![Figure 5.31](image)

**Figure 5.31** Divide-by-2/3 cell logic
Table 5.4  Divide number settings for FDIV N

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<th></th>
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<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>÷24</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>÷25</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>÷26</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>÷27</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>÷28</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>÷29</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>÷30</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>÷31</td>
</tr>
</tbody>
</table>

The FDIV X used by the LC VCO is based on the same concept as the FDIV N, but its circuit implementation is different. Since the FDIV X input frequency could be higher than 5GHz, it requires special high-speed circuits because conventional standard cell circuits are speed-limited. The FDIV X makes use of Source Coupled Logic (SCL) cir-
cuits, which offer such high frequency operation at the expense of power consumption.

Figure 5.32 illustrates the toplevel schematic of FDIV X. The first divide-by-2/3 cell consumes full power (total tail current for the first divide-by-2/3 cell is 600 μA) and working at full speed (higher to 5GHz), while the second divide-by-2/3 cell consumes only half power because its input frequency is only half of the first cell and can work at lower speed.

![Figure 5.32](image1.png)

**Figure 5.32** Circuit schematic of the frequency divider FDIV X

Since the SCL logic output is a differential signal, a buffer is used for converting the differential output to a single-ended full-swing square wave. A circuit schematic of this buffer is shown in Figure 5.33.

![Figure 5.33](image2.png)

**Figure 5.33** The FDIV X buffer to convert a differential to single-ended output
One of the SCL D-latches with AND function is shown in Figure 5.34. A key point in the design is to keep the loop gain of the cross-coupled pair large enough to ensure a stable operation of the latch.

![Figure 5.34](source_coupled_logic_d-latch_combined_and_function.png)

**Figure 5.34** Source Coupled Logic D-latch combined with an AND function

The divide number settings of FDIV X are shown in Table 5.5. They include a divide-by-2 D flip-flop for guaranteeing a 50% duty-cycle operation. This D flip-flop is located at the FDIV X output and not shown in Figure 5.32.

<table>
<thead>
<tr>
<th>p1</th>
<th>p0</th>
<th>Divider number</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>÷8</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>÷10</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>÷12</td>
</tr>
</tbody>
</table>

**Table 5.5** Divide number settings for FDIV X (including ÷2 stage, which is not shown in Figure 5.32)
5.3.2. Layouts of FDIV

The FDIV M and FDIV N are composed of logic gates from the digital standard-cell library. Their layout is straightforward, and does not require a symmetrical layout. This is because is simply implements a given logic function which is operating at a relatively low frequency. The layout of the FDIV M and FDIV N are shown in Figure 5.35 and Figure 5.36 separately.

Figure 5.35  Layout of FDIV M

Figure 5.36  Layout of FDIV N
The FDIV X is used in the LC PLL only; its layout is shown in Figure 5.37. Like the previous frequency dividers, the layout of FDIV X does not need to be symmetrical. However, the main concern is to make the connections as short as possible for achieving the required high-frequency operation. We designed the FDIV X to operate up to 6GHz independent of the process corner.

![Figure 5.37 Layout of the high-frequency divider FDIV X](image)

The two connections in the differential pair in the FDIV X should be matched to ensure the phase of the differential signals to remain the same. Another point of attention is the folding of the MOS transistors in the SCL D-latches. The eight SCL D-latches are placed symmetrically with respect to the vertical axis, i.e. towards right or towards left. For proper matching, the MOS transistors should be insensitive to such placement. We have solved this problem by folding the MOS transistors such they become centro-symmetric.
As previously, power rings, ground rings, and guard rings are used in the layout.

### 5.4. Phase Frequency Detector (PFD)

#### 5.4.1. Schematic of PFD

Figure 5.38 shows the PFD that has been used in this work. The comparison is done at the falling edges of the input signals. The circuit has been designed to be symmetric in nature for ensuring a low timing mismatch. The PFD output consists of four signals: “up”, “upn”, “down”, and “down”. The “upn” signal is the inverse of “up”, and “downn” is the inverse of “down”. The time mismatch between the inverted and non-inverted signals is minimized by using XOR pairs, which can generate opposite polarity signals with nearly the same delay.

![Figure 5.38 PFD circuit schematic](image-url)

The minimum pulse width of the outputs is found to be about 1ns. Although this pulse width is fairly large and can produce large spurs, it is sufficient for meeting our requirement. The spurs requirement will be discussed in Section 5.5. A large pulse width (about 1ns) makes the measurement simple, and it enables a simpler charge pump design. Moreover, the dead zone disappears.
5.4.2. Layout of PFD
The PFD is composed of logic gates from the digital standard-cell library. Its layout is straightforward, but it is made symmetrical to minimize potential timing mismatch within the circuit. The circuit is surrounded by power rings, ground rings, and guard rings. The layout of the PFD is shown in Figure 5.39.

![Figure 5.39 PFD layout](image)

5.5. Charge Pump (CP)
Most of the spurs in a PLL are generated by the charge pump. The largest spur is located at the reference frequency (reference spur), and it has the biggest influence on the PLL jitter performance. Therefore, the most important requirement for the CP design is the reference spur level. Since the total RMS jitter target for the PLL is 30ps, the reference spur should contribute less than one-tenth of 30ps, that’s to say 3ps. Based on the phase-noise jitter relationship, the reference spur level should be lower than -32.25dBc.
From the reference spur analysis of Chapter 4, we can get the following conclusion:

If current leakage dominates the reference spur, then \( I_{\text{leak}} < 20nA \)

If current mismatch dominates the reference spur, then \( \Delta I_{cp} < 70\mu A \)

If timing mismatch dominates the reference spur, then \( \tau < 4\,\text{ns} \)

We noticed that the above requirements for the CP are quite loose. As a consequence, even the simplest CP can be used.

### 5.5.1. Schematic design of the CP

The CP circuit schematic is shown Figure 5.40.

![PFD circuit schematic](image)

**Figure 5.40** PFD circuit schematic

The CP current is determined by the PLL loop parameters. This gives [5.2]:

\[
I_{cp} = \frac{N2\pi f_c}{R_1 K_{VCO}} \frac{b}{b-1}
\]  

(5.6)

where \( R_1 \) is the resistor value in the loop filter, \( N \) is the frequency divide number (FDIV N). The CP current settings for each implemented PLL are shown in Table 5.6.

### 5.5.2. Layout of the CP

Figure 5.41 shows the CP layout. The design is symmetrical (except the input and output connections), and all MOS transistor pairs are placed in a common-centroid layout or-
ganization. These efforts reduce the mismatch between the up and down current sources.

![Figure 5.41 Layout of the CP](image)

**Figure 5.41** Layout of the CP

5.6. **Loop Filter (LF)**

Figure 5.42 shows the loop filter used in this work. Normally, the LF will occupy a lot of area in the PLL because of the large capacitors. For the improved differential ring PLL and the LC PLL, the mental-insulator-mental (MIM) capacitor are used with good accuracy. For the first differential ring PLL, the MOS capacitors are used, which achieve the highest capacitance-per-area ratio. Since their capacitance voltage-dependent, we have verified that this variation does not cause loop instabilities. The phase margin is determined by $b$, which is determined by the ratio of the capacitors in the LF. See (5.6). So the capacitance values can be calculated from PLL loop parameters as shown in expression (5.7) [5.2].
\[ b = \frac{\tau_2}{\tau_3} = 1 + \frac{C_1}{C_2} \]  
\[ C_1 = \frac{\tau_2}{R_1} \quad \text{and} \quad C_2 = \frac{C_1}{b - 1} \]  

Figure 5.42 Loop filter circuit schematic

A potential problem in the LF is the coupled noise. Due to the LF size and the large capacitance values, the noise from ground and substrate could easily be injected to the LF output, which is directly connected to the VCO tuning port. In our design, we did not use a shield for reducing the noise coupling. Therefore, the only way to reduce this noise influence is by making \( K_{VCO} \) of the VCO as small as possible. Since the improved differential ring-oscillator VCO has the smallest \( K_{VCO} \), it achieves the best suppression for such noise coupling. Finally, the LF components values for the three developed PLLs are shown in Table 5.6.

| Settings for CP and LF for the three implemented PLLs |
|-----------------------------------------------|-------------------|-------------------|---------|
| **R** \(_1\) | **C** \(_1\) | **C** \(_2\) | **I**\(_{cp}\) |
| Differential ring PLL | 50K | 3.6pF | 450fF | 3uA |
| Improved differential ring PLL | 10K | 1pF | 125fF | 15uA |
| LC PLL | 50K | 3.6pF | 450fF | 12uA |

The layout of the LFs are not shown here separately, there will be shown in the whole PLL layout at Section 5.8.
5.7. **Lock Detector (LD)**

The lock detector indicates if the PLL is locked, or not. It shares the inputs with the PFD, which are the reference frequency signal and the feedback signal from the FDIV N output. When the time mismatch between the falling edges of both signals is smaller than 1ns, the no phase error (NPE) output will be set to logic “1”. If NPE remains at logic “1” for seven consecutive reference clock periods (it is chosen arbitrarily and also can be judged from the NPE signal by outside logic), the PLL is considered to be locked and the lock output is set to logic “1”. The NPE and lock outputs will be released when the time mismatch exceeds 1ns. The 1ns threshold in time mismatch is equal to a 10-degree in phase mismatch for 26MHz reference. Figure 5.43 shows the lock detector circuit schematic, and Figure 5.44 shows its layout.

![Lock detector circuit schematic](image1)

**Figure 5.43** Lock detector circuit schematic

![Lock detector circuit layout](image2)

**Figure 5.44** Lock detector circuit layout

5.8. **The implemented PLLs**

Three PLLs have been developed which use the same components except the VCO. The pin descriptions of the PLLs are shown in Appendix 5A.
5.8.1. Schematics of the PLLs

Figure 5.45 shows the top-level schematic of the two differential ring-oscillator based PLLs. They have the same schematic structure while the VCO part is different. The complementary LC based PLL is shown in Figure 5.46. It includes one more part—FDIV X compare to the other two ring PLLs. All three PLLs use the same clock gating function, 50% duty cycle guarantee function and clock re-synchronization function. They are shown in Figure 5.47. The A block is a frequency divide-by-2 function, which is used to divide the VCO output frequency to guarantee 50% duty cycle. The B block in Figure 5.47 is the clock gating function. The C block is clock re-synchronization, which is used to get rid of the jitter produced by block A, FDIV M and block B.

![Figure 5.45](image1.png)  
**Figure 5.45**  Top level schematic for the two differential ring PLLs

![Figure 5.46](image2.png)  
**Figure 5.46**  Top level schematic for the LC PLL
The first differential ring-oscillator based PLL and the LC based PLL are both very easy to use. Their output frequency can be adapted by changing the divider numbers of the FDIV N and FDIV M. After such change, the “lock” output indicates when the PLL is in lock.

The improved differential ring-oscillator based PLL requires an initial calibration procedure. This is because the switching tank configuration is not the same for each die sample due to the impact of process variations. As a result, a process calibration is needed before the chip is used. After this calibration, the improved differential ring PLL can be used in the same way as the other two PLLs. The initial calibration process is shown in more detail in Appendix 5B.

5.8.2. Layouts of the PLLs
This section shows the complete PLL layouts for the three different implementations. Figure 5.48 shows the layout of the differential ring-oscillator based PLL. Figure 5.49 shows the layout of the improved differential ring-oscillator based PLL. Finally, Figure 5.50 shows the layout of the LC PLL. The individual PLL building blocks are indicated in each respective layout.
Each PLL is surrounded by decoupling capacitors, power and ground rings, and guard rings. The total decoupling capacitance added to each PLL is made equal to avoid differences in jitter performance due to differences in decoupling capacitance.

As explained in Section 5.6, the loop filter capacitances of the differential ring-oscillator based PLL are different as compared to the other PLLs. The MOS capacitors used in the LF have been separated into many smaller ones. The reason for such separation is to satisfy the charge release time. If this time is violated, the usable frequency range of the MOS capacitor will be limited. In the other two PLLs, the LF capacitors are implemented as MIM capacitors, which are large area but reliable in capacitance value.

The area occupation of the first differential ring PLL is 60×60 μm². The improved differential ring PLL occupies 90×60 μm². The LC PLL is the largest one (due to the required inductor): 385×325 μm². The LC PLL is about 34 times larger than the first differential ring PLL, and 23 times larger as compared to the improved differential ring PLL.

5.9. Summary

In this chapter, we have shown the design details of the three developed PLLs which are the main parts of the L-CGUs and will be measured. The designs of each part of the PLLs are given. Among them, a improved differential ring-oscillator VCO is created, which has better jitter and phase noise performance than other kinds of ring VCOs under power supply noise. Other interesting parts such as high frequency programmable FD, PFD and CP are shown in this chapter. Finally the whole designs of the three PLLs are presented. Next chapter, the simulation results for these three PLLs will be shown and the test chip structure will be introduced.
Figure 5.48  The first differential ring PLL layout (60 × 60 µm²)

Figure 5.49  The improved differential ring PLL layout (90 × 60 µ m²)
Appendix 5A    Pins for all three PLLs

In this appendix we will show the input output pins for the three designed PLLs.

5A.1    Pins for differential ring PLL (20 pins + 2 vdd, gnd)

Figure 5A.1 is the symbol for the differential ring PLL used in the Cadence schematic design. All input and output pins which have been shown in the Figure 5A.1 are de-
scribed in Table 5A.1.

**Figure 5A.1** Symbol for the differential ring PLL

**Table 5A.1** Pins description for the differential ring PLL

<table>
<thead>
<tr>
<th>Pins</th>
<th>Type</th>
<th>Num.</th>
<th>Function</th>
<th>Character</th>
</tr>
</thead>
<tbody>
<tr>
<td>n0 ~ n4</td>
<td>Digital Input</td>
<td>5</td>
<td>Set the divide ratio of FD_N</td>
<td></td>
</tr>
<tr>
<td>m0 ~ m1</td>
<td>Digital Input</td>
<td>2</td>
<td>Set the divide ratio of FD_M</td>
<td></td>
</tr>
<tr>
<td>clken</td>
<td>Digital Input</td>
<td>1</td>
<td>Enable the PLL output</td>
<td></td>
</tr>
<tr>
<td>shutdown</td>
<td>Digital Input</td>
<td>1</td>
<td>Shut down the VCO</td>
<td></td>
</tr>
<tr>
<td>ref</td>
<td>Clock Input</td>
<td>1</td>
<td>Reference clock input</td>
<td>26MHz crystal clock</td>
</tr>
<tr>
<td>out</td>
<td>Clock Output</td>
<td>1</td>
<td>PLL frequency output</td>
<td>Up to 546MHz. Max. load 289fF</td>
</tr>
<tr>
<td>fd</td>
<td>Clock Output</td>
<td>1</td>
<td>FD_N output (for test)</td>
<td>About 26MHz. Max. load 289fF</td>
</tr>
<tr>
<td>Pin</td>
<td>Description</td>
<td>Pin Count</td>
<td>Function Details</td>
<td></td>
</tr>
<tr>
<td>-------------</td>
<td>------------------------------------</td>
<td>-----------</td>
<td>-----------------------------------------------------------------------------------</td>
<td></td>
</tr>
<tr>
<td>osc</td>
<td>Clock Output</td>
<td>1</td>
<td>VCO output (for test)</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Up to 1.092GHz. Max. load 289fF</td>
<td></td>
</tr>
<tr>
<td>up, downn</td>
<td>Pulse output</td>
<td>2</td>
<td>PFD output (for test)</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Minimum pulse width 1ns. Max. load 289fF</td>
<td></td>
</tr>
<tr>
<td>no_phase_error</td>
<td>Digital output</td>
<td>1</td>
<td>Indicate no phase error</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Active if phase error between ref and fd is 0 or 180 degree.</td>
<td></td>
</tr>
<tr>
<td>lock</td>
<td>Digital output</td>
<td>1</td>
<td>Lock detected</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Active if no phase error for continues 7 reference clock cycles.</td>
<td></td>
</tr>
<tr>
<td>Icp</td>
<td>Analog input</td>
<td>1</td>
<td>Bias current for Charge Pump</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Normally 3uA</td>
<td></td>
</tr>
<tr>
<td>Ibias</td>
<td>Analog input</td>
<td>1</td>
<td>Bias current for VCO replica bias circuit</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Normally 44uA (do not need to be very accurate)</td>
<td></td>
</tr>
<tr>
<td>vbn</td>
<td>Analog output</td>
<td>1</td>
<td>VCO tail NMOS gate voltage (for test)</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Low frequency (Can be deleted)</td>
<td></td>
</tr>
<tr>
<td>vdd, gnd</td>
<td>Power supply and ground</td>
<td>2</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>1.2V</td>
<td></td>
</tr>
</tbody>
</table>

5A.2 Pins for improved differential ring PLL (22 pins + 2 vdd, gnd)

Figure 5A.2 is the symbol for the improved differential ring PLL used in the Cadence schematic design. All input and output pins which have been shown in the Figure 5A.2 are described in Table 5A.2.
Figure 5A.2  Symbol for the improved differential ring PLL

Table 5A.2  Pins description for the improved differential ring PLL

<table>
<thead>
<tr>
<th>Pins</th>
<th>Type</th>
<th>Num.</th>
<th>Function</th>
<th>Character</th>
</tr>
</thead>
<tbody>
<tr>
<td>n0 ~ n4</td>
<td>Digital Input</td>
<td>5</td>
<td>Set the divide ratio of FD_N</td>
<td></td>
</tr>
<tr>
<td>m0 ~ m1</td>
<td>Digital Input</td>
<td>2</td>
<td>Set the divide ratio of FD_M</td>
<td></td>
</tr>
<tr>
<td>clken</td>
<td>Digital Input</td>
<td>1</td>
<td>Enable the PLL output</td>
<td></td>
</tr>
<tr>
<td>shutdown</td>
<td>Digital Input</td>
<td>1</td>
<td>Shut down the VCO</td>
<td></td>
</tr>
<tr>
<td>ref</td>
<td>Clock Input</td>
<td>1</td>
<td>Reference clock input</td>
<td>26MHz crystal clock</td>
</tr>
<tr>
<td>out</td>
<td>Clock Output</td>
<td>1</td>
<td>PLL frequency output</td>
<td>Up to 546MHz. Max. load 289fF</td>
</tr>
<tr>
<td>fd</td>
<td>Clock Output</td>
<td>1</td>
<td>FD_N output (for test)</td>
<td>About 26MHz. Max. load 289fF</td>
</tr>
<tr>
<td>osc</td>
<td>Clock Output</td>
<td>1</td>
<td>VCO output (for test)</td>
<td>Up to 1.092GHz.</td>
</tr>
</tbody>
</table>
### Max. load 289fF

<table>
<thead>
<tr>
<th>Description</th>
<th>Type</th>
<th>Value</th>
<th>Notes</th>
</tr>
</thead>
<tbody>
<tr>
<td>up, downn</td>
<td>Pulse output</td>
<td>2</td>
<td>PFD output (for test)</td>
</tr>
<tr>
<td>no_phase_error</td>
<td>Digital output</td>
<td>1</td>
<td>Indicate no phase error</td>
</tr>
<tr>
<td>lock</td>
<td>Digital output</td>
<td>1</td>
<td>Lock detected</td>
</tr>
<tr>
<td>Icp</td>
<td>Analog input</td>
<td>1</td>
<td>Bias current for Charge Pump</td>
</tr>
<tr>
<td>Ibias</td>
<td>Analog input</td>
<td>1</td>
<td>Bias current for VCO replica bias circuit</td>
</tr>
<tr>
<td>s0 ~ s2</td>
<td>Digital input</td>
<td>3</td>
<td>Setting the VCO tuning tank capacitors</td>
</tr>
<tr>
<td>vdd, gnd</td>
<td>Power supply</td>
<td>2</td>
<td>1.2V</td>
</tr>
</tbody>
</table>

### 5A.3 Pins for LC PLL (24 pins + 2 vdd, gnd)

Figure 5A.3 is the symbol for the LC PLL used in the Cadence schematic design. All input and output pins which have been shown in the Figure 5A.3 are described in Table 5A.3.
Figure 5A.3 Symbol for the LC PLL

Table 5A.3 Pins description for the LC PLL

<table>
<thead>
<tr>
<th>Pins</th>
<th>Type</th>
<th>Num.</th>
<th>Function</th>
<th>Character</th>
</tr>
</thead>
<tbody>
<tr>
<td>n0 ~ n4</td>
<td>Digital Input</td>
<td>5</td>
<td>Set the divide ratio of FD_N</td>
<td></td>
</tr>
<tr>
<td>m0 ~ m1</td>
<td>Digital Input</td>
<td>2</td>
<td>Set the divide ratio of FD_M</td>
<td></td>
</tr>
<tr>
<td>x0 ~ x1</td>
<td>Digital Input</td>
<td>2</td>
<td>Set the divide ratio of FD_X</td>
<td></td>
</tr>
<tr>
<td>s0 ~ s1</td>
<td>Digital Input</td>
<td>2</td>
<td>Set the VCO frequency band. (for test)</td>
<td></td>
</tr>
<tr>
<td>clken</td>
<td>Digital Input</td>
<td>1</td>
<td>Enable the PLL output</td>
<td></td>
</tr>
<tr>
<td>shutdown</td>
<td>Digital Input</td>
<td>1</td>
<td>Shut down the VCO</td>
<td></td>
</tr>
<tr>
<td>ref</td>
<td>Clock Input</td>
<td>1</td>
<td>Reference clock input</td>
<td>26MHz crystal clock</td>
</tr>
<tr>
<td>out</td>
<td>Clock Output</td>
<td>1</td>
<td>PLL frequency output</td>
<td>Up to 546MHz.</td>
</tr>
<tr>
<td>Component</td>
<td>Type</td>
<td>Description</td>
<td>Max. load 289fF</td>
<td></td>
</tr>
<tr>
<td>-----------</td>
<td>------</td>
<td>-------------</td>
<td>-----------------</td>
<td></td>
</tr>
<tr>
<td>fd</td>
<td>Clock Output</td>
<td>FD_N output (for test)</td>
<td>About 26MHz. Max. load 289fF</td>
<td></td>
</tr>
<tr>
<td>osc</td>
<td>Clock Output</td>
<td>VCO output (for test)</td>
<td>Up to 1.092GHz. Max. load 289fF</td>
<td></td>
</tr>
<tr>
<td>Up, downn</td>
<td>Pulse output</td>
<td>PFD output (for test)</td>
<td>Minimum pulse width 1ns. Max. load 289fF</td>
<td></td>
</tr>
<tr>
<td>No_phase_error</td>
<td>Digital output</td>
<td>Indicate no phase error</td>
<td>Active if phase error between ref and fd is 0 or 180 degree.</td>
<td></td>
</tr>
<tr>
<td>lock</td>
<td>Digital output</td>
<td>Lock detected</td>
<td>Active if no phase error for continues 7 reference clock cycles.</td>
<td></td>
</tr>
<tr>
<td>Icp</td>
<td>Analog input</td>
<td>Bias current for Charge Pump</td>
<td>Normally 3uA</td>
<td></td>
</tr>
<tr>
<td>Itail</td>
<td>Analog input</td>
<td>Bias current for LC VCO</td>
<td>Normally 40uA</td>
<td></td>
</tr>
<tr>
<td>Ibuffer</td>
<td>Analog input</td>
<td>Bias current for VCO Buffer and FD_X SCL logic</td>
<td>Normally 44uA</td>
<td></td>
</tr>
<tr>
<td>vdd, gnd</td>
<td>Power supply and ground</td>
<td></td>
<td>1.2V</td>
<td></td>
</tr>
</tbody>
</table>
Appendix 5B  Calibration Procedure for the Improved Differential Ring PLL

In this appendix, the calibration for the improved differential ring PLL will be introduced. First, the requirement for the calibration is discussed and then the calibration procedure is presented.

From the VCO frequency post-layout simulation result in Table 6.1, we found the frequency range of the improved differential ring VCO is not very wide and cannot cover the basic requirement: 624MHz to 1092MHz over all process corners. One way to solve this problem is to redesign the VCO and add another switched capacitor pair to enlarge the frequency range. But the added capacitor pair will be very large in both value and area, and it also will reduce the maximum frequency of the VCO through the coupling bypass the switching. Another way is to increase the tuning varactor value to cover a wider frequency range. Yet this will increase the $K_{vco}$, and then increase the frequency sensitivity to power supply.

We use calibration to solve the problem. The basic frequency range requirement is to cover 624MHz, 676MHz, 780MHz, 884MHz, 988MHz, and 1092MHz, which will produce 312MHz to 546MHz output clock through frequency divide-by-2. Yet if we increase the lowest frequency two times, we will get $624*2=1248MHz$ and output through a frequency divide-by-4 to get 312MHz. The divide-by-4 function can be realized by FDIV M through changing the settings. Now we get the new frequency range requirement: 676MHz~1248MHz (676MHz is the second lower frequency point in previous requirement). For the same reason, we can get another frequency range requirement: 780MHz~1352MHz. All the process corners are included in these frequency ranges. The things we need to do is to determine which frequency band is used when a chip is fabricated. This work can be done by an initial calibration procedure.

When the PLL is power up, the control logic will search for the configuration bits, such as “s2s1s0”, N and M, for each required frequencies, and write down these successful configuration information to a config-table. This is called initial calibration and after that,
no calibration would be required in normal situation except temperature or supply voltage changes (how large are these changes still haven’t been measured) make the current configuration not valid any more. At this situation, the calibration needs to be performed again to update the config-table.

The calibration procedure is described following. First select a required output frequency to configuration and set the “s2s1s0”, numbers for N and M. Then waiting for a mount of time (waiting time) to see if the PLL is lock or not. Since the PLL will lock in 1µs when the configuration is correct, the waiting time can be set to any time larger than 1µs. For stable reason, we use 10µs. If the PLL can’t lock with waiting time, we need to know whether the VCO frequency needs to be lower or higher. This information can be get using the logic shown in Figure 5B.1, and the working principle is present as a wave form in Figure 5B.2. In Figure 5B.1 and 5B.2, the “downn”, “up”, “ref”, and “fd” signal has been described in Appendix 5A. The point a to e is marked in Figure 5B.1.

![Logics to detect whether the VCO frequency need to be lower or higher](image-url)

**Figure 5B.1** Logics to detect whether the VCO frequency need to be lower or higher
After know that the PLL can’t lock because VCO frequency need to be lower or higher, we can change the “s2s1s0” setting and try again. The flow chart for one frequency calibration procedure is shown is Figure 5B.3.

When doing the calibration for frequency 624MHz and 676MHz, it may happen that the “s2s1s0” has been set to 111 but still can’t lock. At these situations, multiply the number of N and M by 2 (N=2*N, M=2*M) and set the “s2s1s0” to 000. Then doing calibration again, and they will find there positions. Now the required frequency range of the improved differential ring VCO has been shifted from 624MHz~1092MHz to 676MHz~1248MHz or to 780MHz~1352MHz.

Figure 5B.2 Wave explanation for Figure 5B.1
Chapter 5   L-CGU Design

Figure 5B.3 One frequency calibration procedure flow chart

Reference
6. L-CGU Simulation and Testing

The proposed L-CGU solution is based on an integer-N PLL. Three suitable PLL designs have been discussed in detail in the previous chapter. In this chapter we will present the simulation results as obtained from simulations on extracted layouts. For each PLL, we will quantify the output frequencies, the jitter performance, locking time and power consumption. Finally, we will show the test-chip which has implemented in a 65nm low-power CMOS process.

6.1. Extracted Layout Simulation Results

This section will show the results obtained from circuit simulations on extracted layouts for each PLL. Firstly, the PLLs function simulation will be shown, which make sure that the PLLs are working under all process corners. Then the most important performances – jitter and phase noise simulation results will be shown. Upon these results, the results table will be concluded. The circuit simulations have been performed using the SpectreRF™ circuit simulator. The layout extraction has been performed using Cadence Assura™.

6.1.1. PLLs Function Simulation

PLLs function simulations are performed to make sure that the PLLs will work under all process corners. These simulations include the VCOs frequency range test, the PLLs loop bandwidth and phase margin test, and finally transient simulation to check the whole PLL.

In the VCOs frequency range test, the VCOs frequency ranges under all process corners are test to make sure the required frequency range is covered. The simulation test bench for the differential ring VCO and the improved differential ring VCO is shown in Figure 6.1 (a). The test bench for the LC VCO is shown in Figure 6.1 (b). The supply voltage used for all simulations is 1.2V. Bias currents use the normal value mentioned in Section 5.2. “Shutdown” signals are not active to make the VCOs oscillate. For the two ring VCO, “vtune” is swept from 0V ~ 1.2V, and the frequency test point is shown in Figure
6.1 (a). For the LC VCO, tank control signals “s1 s0” are swept from “0 0” to “1 1”. Under each “s1 s0” configuration, the “vtune” is swept from 0V ~ 1.2V, and the frequency test point is shown in Figure 6.1 (b). Harmonic balance simulation (PSS in SpectreRF™) is engaged.

(a) Simulation test bench for the differential ring VCO and the improved differential ring VCO

(b) Simulation test benches for the LC VCO

Figure 6.1 Simulation test benches for the VCO frequency range test
The frequency range test results are concluded in Table 6.1. It can be observed that both the differential ring-oscillator VCO, as well as the LC VCO cover the required frequency range for all process corners. The improved differential ring VCO can cover the required frequency range for all process corners through calibration (see Appendix 5B).

Table 6.1 Frequency range for each VCO under different process corners

<table>
<thead>
<tr>
<th>VCO Type</th>
<th>Required frequency range [6 MHz]</th>
<th>Simulated frequency range of the VCO [6 MHz]</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td>nominal</td>
</tr>
<tr>
<td>Differential ring VCO</td>
<td>624-1092</td>
<td>204.9-</td>
</tr>
<tr>
<td></td>
<td></td>
<td>1495</td>
</tr>
<tr>
<td>Improved differential</td>
<td>624-1092</td>
<td>631-</td>
</tr>
<tr>
<td>ring VCO</td>
<td>676-1248*</td>
<td>1271</td>
</tr>
<tr>
<td></td>
<td>780-1352*</td>
<td></td>
</tr>
<tr>
<td>LC VCO</td>
<td>3900~4420</td>
<td>3758-</td>
</tr>
<tr>
<td></td>
<td></td>
<td>5069</td>
</tr>
</tbody>
</table>

* Refered to Appendix 5B, the frequency range for the improved differential ring VCO can be switched between these three ranges.

Another important thing is to make sure that the PLL can lock stably. In fact, we are not worry about the unlock problem. The lock can be sure when the PLL loop bandwidth is smaller than the tenth of the reference frequency, and the phase margin is 53 degree which we selected. From Section 5.6, we know the phase margin is determined by $b$, which is determined by the ratio of the capacitors in the LF. So the phase margin is kept under all process corners. The only thing we need to do is keep the loop bandwidth smaller than tenth of the reference frequency. The loop bandwidth is expressed in (5.2). The $K_{VCO}$ will change will different process corner, but fortunately the $I_{sp}$ is controlled by ourselves in the test. So we can sure that the PLL can lock in all process corners.

After we sure the VCOs is no problem and the PLL is stable in theory, the whole PLLs need to be checked in transient simulation. The transient simulation for the whole PLLs
can guarantee the success of the design. In fact some stupid mistakes often occur when the whole PLLs are connected, such as misconnect the reference and feedback signal at PFD input to make the loop positive feedback and never lock. These kinds of mistakes can only be find when using transient simulation to test the whole PLLs. The test benches are shown in Figure 6.2. The supply voltage is 1.2V. Bias currents for the VCOs are the same with the VCOs frequency range test in Figure 6.1 and the values are the normal values mentioned in Section 5.2. The charge pump currents are the same as shown in Table 5.6. Reference clock frequencies are all 26MHz.

(a) Test bench for the differential ring PLL simulation
(b) Test bench for the improved differential ring PLL simulation
There are 11 working modes (corresponding to 11 output frequencies) for each PLL under each process corner. We can not show all of them in the thesis, otherwise it will become unacceptable long. Here only the simulation results for the PLLs working at highest frequency mode (output 546MHz) in nominal process corner are shown in Figure 6.3, Figure 6.4, and Figure 6.5.

In Figure 6.3 ~ 6.5, “vtune” is the LF output and VCO tuning voltage. Form “vtune”, the PLL locking procedure is very clear. “No phase error” monitors the PLL status, and if the “no phase error” keeps high for seven continues reference clock cycles, the “lock” will be active and means the PLL is locked stably now. For all three PLLs, the “lock” is active within 1µs. “Up” and “down” signals are the outputs of PFD. From the zoomed pictures,
the pulse widths when PLL is locked are about 1 ns. For the other signals, please refer to Appendix 5A.

(a) Transient simulation of the first differential ring PLL in transistor level at 546 MHz output
(b) Transient simulation of the first differential ring PLL in transistor level at 546MHz output (continued)
(c) Transient simulation of the first differential ring PLL in transistor level at 546MHz output (zoom in “output” and “osc” to see them clearly)

**Figure 6.3** Transient simulation of the first differential ring PLL in transistor level
Chapter 6  L-CGU Simulation and Testing

(a) Transient simulation of the improved differential ring PLL in transistor level at 546MHz output

(b) Transient simulation of the improved differential ring PLL in transistor level at 546MHz output (continued)
(c) Transient simulation of the improved differential ring PLL in transistor level at 546MHz output (zoom in “output” and “osc” to see them clearly)

Figure 6.4 Transient simulation of the improved differential ring PLL in transistor level at 546MHz output
Chapter 6  L-CGU Simulation and Testing

(a) Transient simulation of the LC PLL in transistor level at 546MHz output

(b) Transient simulation of the LC PLL in transistor level at 546MHz output

(continued)
Transient simulation of the LC PLL in transistor level at 546MHz output

Figure 6.5 Transient simulation of the LC PLL in transistor level at 546MHz output

The PLLs current consumptions are also shown in Figure 6.3~6.5. For the improved differential ring PLL, the total current for the PLL at 546MHz is about 735 μA. It is smaller compare to 1mA of the differential ring PLL and 1.7mA of the LC PLL.

6.1.2. PLL Phase Noise and Jitter Simulation

The phase noise and jitter of a PLL can not be easily obtained from SpectreRF™ circuit simulations. A more convenient approach is to extract phase noise for each PLL building block, and combine those results to obtain the overall PLL phase noise using a numerical
solver like MatLab [6.1]. We have followed this approach.

Figure 6.6, Figure 6.7 and Figure 6.8 show the phase noises of the three developed PLLs. The blue-line marked “PLL” is the overall phase noise at the PLL output. The green-line marked “VCO” is the phase noise for the whole VCO in the PLL. The red-line marked “ref” is the phase noise of the reference crystal oscillator. The light-blue-line is the reference crystal oscillator phase noise as transferred to the PLL output. The pink-line is the phase noise of the whole VCO as transferred to the PLL output. The yellow-line is the phase noise added by the FDIV N. The black-line is the voltage noise at the LF output, which is the noise contribution mainly due to the noise coupled from the ground through big capacitors in the LF. The PLL phase noise in figure 6.6~6.8 has a unit of “dB” not “dBc”. That is because the phase noise we used here is the baseband spectrum $S_{\phi}(f)$ not the SSB phase noise $L(\Delta f)$.

Figure 6.6 Phase noise $S_{\phi}(f)$ of the first differential ring PLL at 546MHz output
The RMS period jitter of the three developed PLLs is summarized in Table 6.2. These values have been determined by using the jitter and phase noise relationship as shown in expression (3.13). The Matlab program to calculate these results is shown in Appendix 6A.
### Table 6.2  Jitter contributions of each PLL at 546MHz output

<table>
<thead>
<tr>
<th>Jitter contributions (rms period jitter)</th>
<th>VCO part</th>
<th>Loop Filter</th>
<th>other parts (Ref, FDIV N, PFD and CP)</th>
<th>Total PLL jitter</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>20 / dB dec</td>
<td>-20dB / dec</td>
<td>noise floor</td>
<td>total</td>
</tr>
<tr>
<td>Differential ring PLL</td>
<td>95ps</td>
<td>6.8ps</td>
<td>95.3ps</td>
<td>80.7ps</td>
</tr>
<tr>
<td>Improved differential ring PLL</td>
<td>5ps</td>
<td>6.8ps</td>
<td>8.5ps</td>
<td>5.4ps</td>
</tr>
<tr>
<td>LC PLL</td>
<td>8.6ps</td>
<td>6.8ps</td>
<td>11ps</td>
<td>10.7ps</td>
</tr>
</tbody>
</table>

Table 6.2 indicates that the phase noise of the PLL components, except the VCO and LF, has only a small contribution to the period jitter (see column “other parts”). This relates to the phase noise part within the PLL loop bandwidth (0-2.6MHz). This reason for this is because their jitter is suppressed by the LF.

The PLL’s white FM phase noise (-20dB/dec) beyond the loop bandwidth contributes most to the jitter when $K_{VCO}$ is large. This includes the VCO white FM phase noise and the LF noise contribution. The jitter will reduce when $K_{VCO}$ is reduced.

Although the noise floor part induced jitter is not so large (6.8ps), it is considered as an important contribution due to its dependency on the PSN spectrum characteristics. The PSN spectrum amplitude directly impacts the noise floor, for example a noise floor increase of about 10dB will results in a 30ps jitter contribution instead of 6.8ps. In that case, the noise floor contribution will dominate the total jitter in the improved differential ring-oscillator PLL and the LC PLL.
6.1.3. PLL Simulation Conclusion
The simulation results for the three PLLs are concluded in Table 6.3. So far it seems that the improved differential ring-oscillator PLL offers the most advantages for use in an L-CGU application.

<table>
<thead>
<tr>
<th>Table 6.3 PLL simulation results</th>
</tr>
</thead>
<tbody>
<tr>
<td>Items</td>
</tr>
<tr>
<td>Operating Frequencies</td>
</tr>
<tr>
<td>Jitter at 546MHz</td>
</tr>
<tr>
<td>Lock time</td>
</tr>
<tr>
<td>Area Occupation</td>
</tr>
<tr>
<td>Active Power Consumption (at 546MHz)</td>
</tr>
<tr>
<td>L-CGU Supply Voltage</td>
</tr>
<tr>
<td>Clock gating, clock enable, and no glitch during switching</td>
</tr>
<tr>
<td>others</td>
</tr>
</tbody>
</table>

6.2. PLL Test-Chip Design and Measurement Set-up
To validate previous observations for the developed PLLs based on simulation results from extracted circuit layouts, two PLL test-chips have been designed in TSMC’s 65nm low-power CMOS technology. This IC technology makes use of 7 metal layers, and the nominal digital power supply voltage is 1.2V. All three PLLs have been taped-out. The reason for this is to perform a silicon characterization of the PLL performance than rather
relying on the simulation results. At this moment in time, it is not clear if the power supply noise spectrum used to model the disturbance of the digital block is representative. Through silicon measurements this model, as well as the noise influence on the PLL performance will be validated.

The first test-chip contains a digital logic block for noise generation, the differential ring-oscillator PLL, and the LC PLL. The chip has been taped out in May 2008. At that moment in time, the improved differential ring-oscillator was not developed yet. Recently, a second test-chip has been prepared that contains this PLL. The tape-out of this test-chip is planned in September 2008. In the next subsection we will provide more details about the content of the first test-chip.

### 6.2.1. PLL Test-Chip Overview

A PLL test-chip has been designed that is composed of, amongst others a digital logic block, the differential ring-oscillator PLL and the LC PLL. Figure 6.9 shows the layout of this test-chip design. The test-chip design occupies a silicon area of $2 \text{mm} \times 1.5 \text{mm}$, and has 80 bondpads.

The purpose of the digital logic block is to offer a programmable circuit solution for generating power supply noise. The digital logic block implements a circular shiftregister of 8K flip-flops, while using delay lines in between two consecutive flip-flops. On average, the logic depth of the delay lines is about 20 logic gates. The shiftregister can be loaded with a data vector for programming the average circuit activity. Its working mode can be set to generate no circuit activity (clock gated or power down), clock activity only, or clock activity plus data activity of 0-100%. The circuit activity can be programmed to be homogeneous, or spatially distributed in particular regions of the shiftregister. In addition, the digital block is equipped with a linear feedback shift register (LSFR) to generate random circuit activity which can be inserted at various locations in the shift register. Finally, the operating frequency of the digital block is programmable, and it is provided through an I/O pad. It should be clear that such circuit enables a flexible and programmable solution to generate power supply noise with different magnitudes and frequency spectrum.
The digital logic block uses four power and ground connections, which are located at the same position at a different corner of the digital logic block. Such configuration ensures that a symmetrical noise propagation throughout the logic block. At the top-right corner, power and ground observation pads have been placed for measuring the power supply noise spectrum up to a few gigahertz. The digital block is surrounded by power switches for power gating purposes. Finally, the block is surrounded by power and ground rings.

![Image of PLL test-chip layout](image)

**Figure 6.9** Layout of the first implemented PLL test-chip in 65nm CMOS

The differential ring-oscillator PLL is located in the bottom-right corner of the chip. The LC PLL is located in the bottom-left corner of the chip. Both PLLs are connected to the power supply of the digital logic block at the same location, but at a different side of the digital logic block. The PLLs are equipped with a scan-chain based control register for setting the proper control signals to the PLLs.
Since PLL output frequencies are up to a value of 550MHz, special output buffers are needed for enabling reliable jitter and phase noise measurements. In this test-chip, five of those high-frequency outputs make use of the special RF test buffer. The circuit and layout details of the RF test-buffer will be disclosed in Section 6.2.2.

Finally, the PLL test-chip also contains contributions from other projects, which will not be described in this thesis.

### 6.2.2. RF Test Buffer

A special output buffer has been designed for providing a reliable off-chip output connection of high-frequency signals. Each PLL has two high-frequency square wave signals which require such output buffering (see Appendix 5A). The first output signal is “osc”, which is the test signal of the VCO output. When the PLL is locked, its frequency range is in between 624MHz and 1092MHz. The second output signal is “output”, which is the PLL output. When the PLL is locked, its frequency range is in between 48.75MHz and 546MHz. Based on these requirements, the designed RF test buffer allows an input frequency up to 2 GHz and produces at least a -9dBm output. The output impedance of the RF test buffer is 50Ω, which is easy to match the test cables. For a reliable phase noise and jitter measurement, the signal power at the input port of the measurement equipment should not be lower than -16dBm. It is important to mention that a DC blocking capacitor (such as 1000pF) is required in between the RF test buffer output and the measurement equipment. This capacitor is used for blocking the DC bias voltage of the RF test buffer, and it should be located close to the chip output pin on the application printed-circuit board.

Figure 6.10 shows the circuit schematic of the proposed RF test buffer. One RF test buffer consumes about 10mA of current. This large current made us to choose a differential structure, because it can reduce the current injected into the substrate. The required differential inputs are produced by the same design in the PFD. In order to ensure that the PLL output phase noise and jitter is not polluted by the RF test buffer, the buffer has been supplied from a dedicated but clean analog power supply and ground. Figure 6.11 shows the layout of the RF test buffer. It occupies 0.005 mm² of silicon area.
6.3. Summary
The simulation results for the three PLLs which were designed in Chapter 5 are shown and discussed. Based on the results, the improved differential ring PLL has found to be...
the lowest jitter, smallest power consumption and acceptable in area. It is the best candidate for the L-CGU applications. The test structure and some supplements such as test RF buffer are also introduced in this chapter.

Appendix 6A  Matlab Program for the PLL Phase Noise and Jitter Calculations

The phase noise and jitter calculation programs for three PLLs are the same except for the PLL loop parameters and phase noise simulation values. So here only the program for the differential ring PLL is shown below.

clear;
K_vco = 3e9*2*pi/2; % Be careful of the unit
f_osc = 26e6;
f_vco = 1092e6/2;

% f_exp = [6.3:0.01:9];
f = 10.^f_exp;
s = i*2*pi*f;
N = f_vco/f_osc;

% K =2*pi*f_vco/10; % K = K_det*K_vco*K1/N; % Be careful of the unit
b = 9; % b = 1 + C/C3; % b = 9 is wanted
tal_2 = sqrt(b)/K;%*2*pi); % tal_2 = R2*C;
K_normal = K*tal_2;%*2*pi;  % K_normal = 3 is wanted
pole_3 = b/tal_2;
zero_1 = 1/tal_2;

damp_app = sqrt(K_normal/4); % Aprroximate damping factor. When the third pole is far away, the third order pll is aproximate second order pll within loop band width.
wn_app = K/(2*damp_app); % Aprroximate natural freq

% Charge pump filter
R1 = 51.6e3
C1 = tal_2/R1
C2 = C1/(b-1)

% PFD
ip = K*2*pi*N*b/(K_vco*R1*(b-1))
K_det = ip/(2*pi);

% Z_f = (b-1)*(s*tal_2+1)./(b*s*C1.*(s*tal_2/b+1));
G_f = K_det*K_vco*Z_f/s;
H_f = G_f*N./(N+G_f);
\[ E_f = \frac{N}{N+G_f}; \]

```matlab
figure(1);
semilogx(f,20*log10(abs(H_f)));
grid on;
title('PLL System Transfer Function H(f)');
xlabel('frequency');
ylabel('dB');

figure(2);
semilogx(f,20*log10(abs(E_f)));
grid on;
title('PLL Error Transfer Function E(f)');
xlabel('frequency');
ylabel('dB');
```

\[
\text{t} = \left[ 6.0 \times 3^{0.1/f_{\text{osc}}} : 3^{10/f_{\text{osc}}} \right];
\]
\[
delta_w = 100e3^2 \pi;
\]
\[
\text{phase\_error\_t} = \frac{\delta w/\omega_n}{1 - \delta^2} \exp(-\delta \omega_n t);
\]

```matlab
figure(3);
plot(t, phase_error_t);
grid on;
title('Transient Phase Error');
xlabel('second');
ylabel('rad');
```

% Phase noise of VCO (without power supply noise) after divide-by-2 at 546MHz
\[
S0_{\text{VCO}} = -120; \quad \% \text{Noise floor in dB} \ !!
S2_{\text{VCO}} = -51.16 \cdot 3; \quad \% \text{White FM part in dB} \ !!
S3_{\text{VCO}} = -56.69 \cdot 3; \quad \% \text{Flicker FM part in dB} \ !!
\]
\[
f2_{\text{VCO}} = 1e6; \quad \% \text{The offset frequency point to get } S2_{\text{VCO}}
f3_{\text{VCO}} = 1e5; \quad \% \text{The offset frequency point to get } S3_{\text{VCO}}
\]
\[
Sf_{\text{VCO}} = 10^4((S3_{\text{VCO}}+30\log10(f3_{\text{VCO}})/10)).f.^3 +
10^4((S2_{\text{VCO}}+20\log10(f2_{\text{VCO}})/10)).f.^2 + 10^4(S0_{\text{VCO}}/10));
\]

% Phase noise of ref OSC
\[
S0_{\text{OSC}} = -150; \quad \% \text{Noise floor in dB} \ !!
S2_{\text{OSC}} = -140 \cdot 3; \quad \% \text{White FM part in dB} \ !!
S3_{\text{OSC}} = -80 \cdot 3; \quad \% \text{Flicker FM part in dB} \ !!
\]
\[
f2_{\text{OSC}} = 1e3; \quad \% \text{The offset frequency point to get } S2_{\text{OSC}}
f3_{\text{OSC}} = 1e3; \quad \% \text{The offset frequency point to get } S3_{\text{OSC}}
\]
\[
Sf_{\text{OSC}} = 10^4((S3_{\text{OSC}}+30\log10(f3_{\text{OSC}})/10)).f.^3 +
10^4((S2_{\text{OSC}}+20\log10(f2_{\text{OSC}})/10)).f.^2 + 10^4(S0_{\text{OSC}}/10));
\]

% Phase noise of frequency divider
\[
S0_{\text{FD}} = -110.1; \quad \% \text{White noise in dB}
S1_{\text{FD}} = -107; \quad \% \text{Flicker noise in dB}
\]
\[
f1_{\text{FD}} = 1e3; \quad \% \text{The offset frequency point to get } S1_{\text{FD}}
\]
\[
Sf_{\text{FD}} = 10^4((S1_{\text{FD}}+10\log10(f1_{\text{FD}})/10)).f + 10^4(S0_{\text{FD}}/10);
\]
% voltage noise of PFD, CP and filter at the filter output
V0_filter = -119.1;        % White noise in dB
V1_filter = -107;        % Flicker noise in dB
f1_filter = 1e3;        % The offset frequency point to get V1_filter

V_filter = 10^((V1_filter+10*log10(f1_filter))/10)./f + 10^((V0_filter/10);

% PLL Phase noise
Sf_pll = (Sf_OSC + Sf_FD + V_filter.(abs(Z_f*K_det).^2)).*abs(H_f).^2 + Sf_VCO.*abs(E_f).^2;

Sf_pll_dB = 10*log10(Sf_pll);

figure(4);
semilogx(f, Sf_pll_dB, '.', f, 10*log10(Sf_VCO), '--', f, 10*log10(Sf_OSC), '*', f, 10*log10(Sf_FD), f, 10*log10(V_filter), '+');
grid on;
ylim([-160 -50]);
title(PLL Phase Noise);
xlabel('offset frequency');
ylabel('dB');
legend('PLL', 'VCO phase noise', 'ref', 'ref * H(f)', 'VCO * E(f)', 'FDIV N phase noise', 'voltage noise of the LF output');

%%Jitter

Z_fun = @(freq) (b-1)/(i*2*pi*freq*tal_2+1)./(b*i*2*pi*freq*C1.*(i*2*pi*freq*tal_2/b+1));
G_fun = @(freq) K_det*K_vco*Z_fun(freq)./(i*2*pi*freq);
H_fun = @(freq) G_fun(freq).*N./(N+G_fun(freq));
E_fun = @(freq) N./(N+G_fun(freq));

Sf_VCO_fun = @(freq) (10^((S3_VCO+30*log10(f3_VCO))/10)./freq.^3 + 10^((S2_VCO+20*log10(f2_VCO))/10)./freq.^2 + 10^(S0_VCO/10));
Sf_OSC_fun = @(freq) (10^((S3_OSC+30*log10(f3_OSC))/10)./freq.^3 + 10^((S2_OSC+20*log10(f2_OSC))/10)./freq.^2 + 10^(S0_OSC/10));
Sf_FD_fun = @(freq) 10^((S1_FD+10*log10(f1_FD))/10)./freq + 10^(S0_FD/10);
V_filter_fun = @(freq) 10^((V1_filter+10*log10(f1_filter))/10)./freq + 10^(V0_filter/10);

int_fun_VCO_white_FM_part = @(freq) 10^((S2_VCO+20*log10(f2_VCO))/10)./freq.^2.*(sin(pi*freq/f_vco)).^2/(pi*f_vco)^2;
int_fun_VCO_noise_floor_part = @(freq) 10^(S0_VCO/10).^2.*(sin(pi*freq/f_vco)).^2/(pi*f_vco)^2;
int_fun_VCO_part_total = @(freq) Sf_VCO_fun(freq).^2.*(sin(pi*freq/f_vco)).^2/(pi*f_vco)^2;
int_fun_LF_part = @(freq) (V_filter_fun(freq)./(abs(Z_filter*freq*K_det).^2)).^2.*(sin(pi*freq/f_vco)).^2/(pi*f_vco)^2;
\begin{align*}
\text{int\_fun\_other\_pll\_part} &= @(freq) \quad (Sf\_OSC\_fun(freq) + Sf\_FD\_fun(freq)) \cdot \text{abs}(H\_fun(freq)) \cdot \sin^2(\pi \frac{freq}{f\_vco}) \cdot \frac{1}{(\pi \frac{f\_vco}{2})^2}; \\
\text{int\_fun\_total\_jitter\_PLL} &= @(freq) \quad \text{int\_fun\_VCO\_part\_total}(freq) + \text{int\_fun\_LF\_part}(freq) + \text{int\_fun\_other\_pll\_part}(freq);
\end{align*}

\begin{align*}
Jc\_VCO\_white\_FM\_part &= \sqrt{\text{quad}(\text{int\_fun\_VCO\_white\_FM\_part}, 1\times10^3, \frac{f\_vco}{2})} \\
Jc\_fun\_VCO\_noise\_floor\_part &= \sqrt{\text{quad}(\text{int\_fun\_VCO\_noise\_floor\_part}, 1\times10^3, \frac{f\_vco}{2})} \\
Jc\_VCO\_part\_total &= \sqrt{\text{quad}(\text{int\_fun\_VCO\_part\_total}, 1\times10^3, \frac{f\_vco}{2})} \\
Jc\_LF\_part &= \sqrt{\text{quad}(\text{int\_fun\_LF\_part}, 1\times10^3, \frac{f\_vco}{2})} \\
Jc\_other\_pll\_part &= \sqrt{\text{quad}(\text{int\_fun\_other\_pll\_part}, 1\times10^3, \frac{f\_vco}{2})} \\
Jc\_total &= \sqrt{\text{quad}(\text{int\_fun\_total\_jitter\_PLL}, 1\times10^3, \frac{f\_vco}{2})}
\end{align*}

**Reference**

7. Conclusions

In this work we have investigated suitable local clock generator units (L-CGU) for use in multiple-power domain system chips. Local clocking is attractive for advanced power management applications for replacing the traditional central clocking. The most important requirement of the L-CGU is that it should generate a robust high-quality, low-jitter clock (period jitter <30ps), while operating from the digital ‘noisy’ power supply. The L-CGU output frequency should be from 550MHz down to 50MHz with steps of 50MHz.

Phase noise and jitter under noisy power supply conditions has been analyzed. A power supply noise model has been developed that enabled us to explore trade-offs involved between different oscillators approaches.

A number of oscillator types have been compared on various defined quality metrics. Two suitable candidates for use in an L-CGU have been identified. The first solution is a differential ring-oscillator based VCO, and the second one is a complementary differential LC oscillator. Both oscillator types have been implemented in a PLL in 65nm LP-CMOS.

A L-CGU has been implemented by an integer-N PLL. Three different versions have been developed. The first version is based on a differential ring-oscillator VCO, the second version based on an improved differential ring-oscillator VCO, and the third one is based on the differential LC oscillator. Post-layout extracted simulations showed that the improved differential ring-oscillator PLL achieves the best jitter performance, lowest power consumption, and small area occupation. However, it requires an initial calibration before use. It is considered as the preferred solution for implementation of an L-CGU. Table 7.1 summarizes the key design characteristics of the different implementations.
### Table 7.1: L-CGU Design Characteristics in 65nm LP-CMOS

<table>
<thead>
<tr>
<th></th>
<th>RMS period jitter</th>
<th>Active current</th>
<th>Circuit Area</th>
<th>Specialties</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Differential ring PLL</strong></td>
<td>125ps</td>
<td>1mA</td>
<td>$60 \times 60\mu m^2$</td>
<td>no</td>
</tr>
<tr>
<td><strong>Improved differential ring PLL</strong></td>
<td>10ps</td>
<td>735\mu A</td>
<td>$90 \times 60\mu m^2$</td>
<td>initial calibration</td>
</tr>
<tr>
<td><strong>LC PLL</strong></td>
<td>15.4ps</td>
<td>1.7mA</td>
<td>$300 \times 400\mu m^2$</td>
<td>no</td>
</tr>
</tbody>
</table>

Furthermore, we have analyzed the jitter performance of clock net buffers under power supply noise conditions. In general, we found that the jitter in digital circuits can be dominated by the jitter contributed by the clock buffers in the clock distribution network. In that case, the efforts to develop a high-quality low-jitter L-CGU would have no meaning.
Future Work

Although we have developed a suitable L-CGU solution, more work is needed to find answers to some questions that could not be addressed in the timeframe of this investigation.

First, the power supply noise model that has been developed in this work needs to be validated and calibrated through silicon measurements. This is possible when the implemented test-chip design will return from fabrication and assembly.

Second, silicon measurements of the developed L-CGUs are required to confirm our observations in this investigation. Noise correlations should be studied as well as the means how to reduce the noise floor of the buffers.

Third, an investigation should be started on the jitter performance of the clock distribution network. The clock distribution could be responsible for most of the jitter experienced in digital circuits. The optimization for achieving a low-jitter and low clock skew clock delivery is recognized as a very challenging task.