Time-Gain-Compensation Amplifier for Ultrasonic Echo Signal Processing

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Preface

This thesis is a final report of a Master of Science project, which lasted from April 2009 to February 2010. This work has been done in Electronics Instrumentation Laboratory, Department of Microelectronics, Faculty of EEMCS, Delft University of Technology.

In this thesis a time gain compensation amplifier (TGC) for ultrasonic echo signal processing has been designed and fabricated. The problem of low power TGC used in echocardiography is analyzed and a solution is provided. The simulation result shows that this TGC consumes much less power than all the other prior designs. The post-layout simulation has been performed to make sure our chip could work.

This thesis is intended to be useful reference for people who are interested in ultrasonic echo signal process and low power amplifier design.
Acknowledgements

This thesis could never be finished in such a limited time without the help from many people.

I would like to thank my supervisor Prof. Dr. Gerard Meijer. He gave me the chance to do this project. He gave me a lot of suggestions in our discussion.

I would express my deepest appreciation to my daily supervisor Msc. Zili Yu. She has been helping me throughout the whole project. From the beginning of the project, she gave me inspiring discussion almost every working day. I have learned a lot from her. The most valuable thing is the patience and confidence. She not only teaches me scientific knowledge but also set a good example for me in being a scientist and researcher.

I also want to thank Michiel Pertijs, Jia Qi, Wu Jiafeng. Maybe I still could not find a right way to my destination without your help.

Further, I want to say thank you to all the people from the team of ultrasonic echocardiography. I have learned a lot from the PID meeting every month. I hope you could finish the good product in the near future.
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Chapter 1

Introduction

1.1 3D echocardiography

The cardiography is widely used to monitor activity and health of the human heart. Echocardiogram utilizes ultrasound waves to form a picture of the heart providing information about the heart’s size, structure, and movement and how the valves work.[8]

Ultrasound images of the heart are generally made either from the chest (trans-thoracic echo, TTE) or from the esophagus (trans-esophageal echo, TEE) using a special transducer and an ultrasound machine.

- Trans-thoracic echo (TTE)

In this case, the echocardiography transducer (or probe) is placed on the chest wall (or thorax) of the subject. Images are taken through the chest wall. This is a non-invasive, highly accurate and quick assessment of the overall health of the heart. A cardiologist can quickly assess a patient’s heart valves and degree of heart muscle contraction. The images are displayed on a monitor, and are recorded either by videotape (analog) or by digital techniques. TTE in adults is of limited use for the structures at the back of the heart, such as the left atrial appendage. Trans-esophageal echocardiography may be more accurate than TTE because it allows closer visualization of common sites for vegetations and other abnormalities.[20]

- Trans-esophageal echo (TEE)

This is an alternative way to perform an echocardiogram. A specialized probe containing an ultrasound transducer at its tip is passed into the patient’s esophagus.
A classical trans-esophageal ultrasound probe consists of a gastroscope with a small multi-element phased array ultrasound transducer. It can produce a real-time two-dimensional cross sectional image through the heart. The image plane is manipulated by the physician to visualize the moving structures within the heart and a three dimensional impression of the structures is composed mentally. The TEE approach produces better quality images than the TTE imaging, but the gastrosopic procedure is discomforting for the patient.

There is a clear need for creating three-dimensional images of the heart directly using the TEE approach. This can be done by stepwise acquisition of adjacent or rotating planes, gated to the heart rate. However, this is a slow, error-prone and very discomforting procedure. Faster mechanized acquisitions are possible, but a better approach is using a matrix array, a phased array consisting of multiple elements such that the ultrasound beam can be steered in two orthogonal directions, covering a pyramidal volume rather than a single plane.

In our project, we use a 2D matrix ultrasonic transducer with more than 2000 elements. The integrated circuit for the transducer and the matrix transducer will be put into the tip of a trans-esophageal probe for 3D electrocardiography (Figure 1.1).

### 1.2 Ultrasonic Echo Signal Processing

Actually, there are several architectures of an ultrasonic system. We use the architecture shown in Figure 1.2. It consists of a transmission signal path and a receiving...
signal path. In the transmission signal path, a high voltage pulser will stimulate the transducer to produce ultrasonic signal. When the ultrasound wave is travelling in the tissue, it experiences attenuation due to scattering, absorption and other propagation effects. It’s quite challenging to receive the echo signals and make a clear image out of them. The receiving path consists of a matrix transducer and electronics. The transducer will convert the ultrasonic signal into electrical signal. The echo from the deep tissue is attenuated more than the echo from the near field tissue, and also the return time is longer. So we can not make use of these electrical signals directly. We need a low noise amplifier to improve the signal-to-noise ratio. A time-gain-compensation (TGC) amplifier should be used to provide the echo signals with increased gain along the time, in order to maintain the image uniformity. Then the analog beam forming is used in our design to sum up the signals from the different transducers. The block diagram of the receiving path is shown in Figure 1.3. After the beamforming, the electrical signal will be transmitted to the main frame machine (Lecoeur) by the cables. Then the main frame machine will process the signals and display a 3D image on the screen.

1.3 Time Gain Compensation Amplifier (TGC)

When ultrasound wave is transmitting in the tissue, it will experience power loss. The reasons for power loss fall in two categories:

1. Attenuation of biological media.

Sound wave will attenuate when passing through media. The attenuation rate
is media and frequency dependent. For example, a 6MHz signal travelling across blood, the attenuation coefficient is about 1.3dB/cm. If the longest signal path is about 10cm, so the maximum attenuation is about 26dB.

(2) Spreading

Spreading is the other important reason for power loss.

The TGC amplifier is used to compensate the unequal attenuation and spreading of the received signals. Because the power loss will increase with the penetration depth and the penetration depth is proportional to the penetration time. The gain of the TGC amplifier will also change with the time to compensate the loss. Ideally, if the gain of the TGC amplifier has an exponential relationship with the time, the compensation will be perfect.

1.4 Organization of the Thesis

The thesis consists of six chapters. Following the introduction, Chapter 2 presents the system principles. In this chapter, we will introduce the property of the ultrasonic echo signal processing system. In Chapter 3, the function of the time gain compensation amplifier in the system will be emphasized and the target specification of the TGC will be listed. In Chapter 4, we will introduce some prior implementations of the TGC and compare the different topologies. The topology based on our design requirements will be presented. Chapter 5 describes the circuit implementation and the associated simulation results. This work will be concluded in chapter 6.
Chapter 2

System principles

2.1 Ultrasound Imaging System

The basic ultrasound imaging system consists of a transducer that converts electrical pulses from the transmitter to acoustic pluses and reconvert the received echoes into electrical signals. Then, these signals will be processed and displayed as a time record on an oscilloscope (Figure 2.1).

Ultrasound imaging is now in very widespread clinical use. Echocardiography is one of the most popular ultrasound imaging products. Over the last 4 decades, echocardiography has evolved from single-beam imaging to sophisticated 3-D techniques that enable the study of cardiac structure. This development is illustrated in Figure 2.2[10]. The most important technologies of ultrasound imaging include transducer, beam forming, tissue harmonic imaging, contrast agent and three-dimensional imaging [19].

The block diagram of our ultrasonic system has been shown in Figure 2.1. Each part in the block diagram will be analyzed in detail.

Figure 2.1: The block diagram of basic ultrasound imaging system
2.2 2D-matrix Transducer

Transducer is an important element in the ultrasonic system. It works as a bridge between the electrical signal and ultrasonic signal. The piezoelectric transducer converts electrical signals into mechanical vibrations and produce ultrasonic wave (transmitting mode). The ultrasonic wave will make the piezoelectric element vibrate and it will convert the mechanical signals into electrical signals (receiving mode). There are four types of transducer: linear array transducer, phased array transducer, two-dimensional array transducer and annular array transducer [3]. The 2D-matrix transducer is the most versatile transducer since one doesn’t have to move the transducer to scan a volume if a phased array approach is used. However, the complexity increases by $N^2$. Here we will compare the two-dimensional transducer(Figure 2.3(B)) to the one-dimensional transducer(Figure 2.3(A)). Replacing the single row of elements found in conventional linear(1D) transducers, the elements in a matrix array transducer are arranged in a two-dimensional grid. As with the linear array, the direction in which the matrix array transmits and receives ultrasound energy is controlled by timing individual transducer elements during transmission and reception of the ultrasound. With a linear array, only the direction within a slice, the so-called azimuth, can be controlled, whereas a matrix array offers steering in both the beam’s azimuth an elevation, permitting interrogation of an entire pyramid-shaped volume [7].

In our ultrasound imaging system, the transmitting transducer is separated from
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Table 2.1: The specification of the transmit array

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<tr>
<td>Bandwidth</td>
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</tr>
<tr>
<td>Material</td>
<td>CTS 3203 HD</td>
</tr>
<tr>
<td>Number of elements and pitch</td>
<td>48 x 48 elements of 200 x 200$\mu$m$^2$ or 40 x 40 elements of 250 x 250$\mu$m$^2$</td>
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</table>

Table 2.2: The specification of the receiving array

the receiving transducer. We could avoid the problem of high voltage electronics on the chip for receiving part. The two arrays are mounted adjacent to each other, in the length direction of the gastroscope tip. One array will be dedicated to transmission and the other will be dedicated to reception of ultrasound. A cross section of the current design is shown in Figure 2.4.

The transmit array and electronics can be separately optimized for the transmission of fundamental frequency ultrasound pulses of high power. The specification is shown in Table 2.1.

The receiving array and electronics can be separately optimized for the reception of ultrasound signals of low power. The specification is shown in Table 2.2.

2.3 Tissue Harmonic Image

Harmonic imaging technique is used in our system. A sound wave with a central frequency of 3MHz is sent into the medium by the transmit matrix, and the receiving frequency is 6MHz. As soon as the 3MHz signal entered the tissue, the signal starts to experience a distortion due to the fact that the propagation velocity is pressure dependent. As an example, we can think about a pure sine wave pulse which is transmitted into the tissue. The sound pressure at the wave crest is higher with respect to the rest pressure, therefore the sound speed is higher than the small-signal sound speed and the pressure at the trough is lower, which leads to a lower sound speed. In this way, a pure sine wave is distorted and tends ideally, with the increasing
Figure 2.3: (A) Linear 1-Dimension transducer (B) 2-Dimension matrix transducer (in courtesy of G.D.Stetten[7])

Figure 2.4: Cross section through the tip with the two arrays, shielding, cables, receive electronics and interconnect (in courtesy of Oldelft Ultrasound B.V.)
of depth, to be a saw tooth wave, which contains higher harmonics. These harmonic components arise also because the transmitted pulse is distorted in its propagation through inherently nonlinear tissue. Although harmonics higher than the second one are also produced a result of the nonlinear propagation of the transmitted pulse, they are relatively weak.

There are two rates co-exist: the distortion rate and the attenuation rate. In the beginning, the distortion rate dominates. After certain moment, the attenuation rate will dominate. From then on, the strength of the second harmonic signal will decline. For the near field, we are not able to use harmonic imaging, because the second harmonic signal needs time to build up. At first, the second harmonic signal is too weak to be detected. We estimated that, at about 3cm to 4cm depth, then the harmonic signal reached its peak and is suitable for receiving. The benefit of using second harmonic imaging, in our application, is to get much lower side-lobes and clutter effects.

### 2.4 Readout Circuit

There should be an analog readout circuit to process the electrical signal from the receiving transducer. The block diagram for the readout circuit is shown in Figure 2.5. It consists of three parts: LNA (low noise amplifier), TGC (time gain compensation amplifier) and micro-beamformer (analog delay&sum circuit).

#### 2.4.1 LNA (low noise amplifier)

Good noise performance relies on an ultra low noise amplifier at the beginning of the signal processing chain, which minimizes the noise contribution of the following
circuitry. To consider the total noise value for the system, the overall noise performance is discussed in a noise chain. If several devices are cascaded, the total noise factor can be found as

\[ F = 1 + \frac{F_2-1}{G_1} + \frac{F_3-1}{G_1G_2} + \cdots + \frac{F_n-1}{G_1G_2\cdots G_{n-1}} \]

Where \( F_n \) is the noise factor of the \( n \)-th device and \( G_n \) is the power gain of the \( n \)-th device [18].

From the equation above, we can see that, the noise performance of the first stage dominates. Since the noise of the input stage is also amplified by the second stage, the first stage becomes the important to optimize for the noise.

2.4.2 TGC (time gain compensation amplifier)

A time gain compensation (TGC) amplifier is an important module in ultrasonic scanners because it provides the echo signals with increased gain along with time to maintain the image uniformity. In most cases the signal strength decreases exponentially with the penetration depth, so the corresponding amplification slope is represented by an exponential function.

When the ultrasound wave is traveling in the tissue, it experiences attenuation and spreading. For different biological media, the attenuation coefficient is different (Figure 2.6). From the figure, we could also find that the attenuation coefficient is a non-linear function of frequency. Actually, most of the tissue that the ultrasound wave will meet in echo-cardiography system is blood. For the 6MHz ultrasound signal, the attenuation coefficient in blood is about 1.3dB/cm according to the Figure 2.6.

Spreading is another important effect when we consider the power loss of the signal.

A time gain compensation amplifier is needed to compensate the power loss. Ideally, if the gain of the TGC could change with the time exponentially which is shown in Figure 2.7, the power loss could be compensated perfectly. It’s difficult to design such TGC amplifier for circuit implementation. Actually, it is not necessary to build such an ideal amplifier. We could just set the gain for several steps. The reason will be given in Chapter 3.
Figure 2.6: Summary of published experimental results for the attenuation-versus-frequency characteristics of various biological media and water (in courtesy of R.S.C.Cobbold [14]).
2.4.3 Beamformer (Delay&Sum Circuit)

As shown in Figure 2.4, there are more than 2000 elements of transducers in the receiving path. Only a limited amount of cables can be guided through the gastrointestinal pipe, the number of receiving channels should be reduced by a factor of 10. Therefore, the signals from the individual elements should be combined in some “smart” way to get as much information as possible. This combining of the signals is called micro-beamforming. The micro-beamformed signals are transmitted over the coaxial cables to the main frame machine. This machine performs the actual beamforming by delaying and summing the signals received from the groups of elements so that they interfere constructively in the required focal point.

The array is divided into groups of 9(3×3) elements. To increase the sensitivity, each group of elements is pre-steered to ‘look’ into a certain direction. This steering of groups is done by delaying the elements within the group relative to each other. The delay has to be realized in the chip by a cascade of delay circuits. The system design for a group of elements is shown in Figure 2.8.

2.5 Conclusion

In this chapter, we have given an overview about the whole system of our 3D ultrasonic echocardiography. Each component of the system is briefly introduced. The function of the time gain compensation amplifier is to compensate the power loss of ultrasound due to the signal propagation. It is the foundation of this thesis.
Figure 2.8: The system design for one group of elements (in courtesy of Z.Yu)
Chapter 3

Specification of Time Gain Compensation Amplifier

In this chapter, we will explain the relationship between TGC and other parts of the ultrasonic imaging system. Then the specifications of the TGC will be listed.

3.1 The Relationship between TGC and Other Circuit Blocks

The relationships between TGC and the other blocks are shown in Figure 3.1.

3.1.1 The relationship between TGC and 2D-Matrix Transducer

The transmitter of the 2D-matrix transducer will produce the 3MHz ultrasonic wave. We will make use of the second harmonic of the ultrasound wave. The receiving transducer will receive the 6MHz ultrasonic wave and produce mechanical vibrations. Then transducer will convert mechanical vibrations into 6MHz electrical signal. The central frequency of the transducer is 6MHz and the bandwidth is 50% of the central frequency. So it will process the signal from 4.5MHz to 7.5MHz. Then, the signal bandwidth of the whole readout circuit is also from 4.5MHz to 7.5MHz. It means the input signal frequency of the TGC is from 4.5MHz to 7.5MHz.

Because the frequency range of the input signal is from 4.5MHz to 7.5MHz. The signal will be distorted when it pass through the TGC due to group delay.
CHAPTER 3. SPECIFICATION OF TIME GAIN COMPENSATION AMPLIFIER

Given a linear system block with frequency domain transfer function $H(jw)$, writing

$$H(jw) = A(jw)e^{j\varphi(jw)} \quad (3.1)$$

Then the group delay $\tau$ is defined as

$$\tau(w) = -\frac{\partial \varphi(w)}{\partial(w)} \quad (3.2)$$

That is the negative rate of phase change with frequency. The quantity $\tau$ has the dimension of time. It is a useful measure of phase distortion. The linear portion of the phase response is converted to a constant value (representing the average signal-transit time) and the deviation from linear phase is transformed into deviation from constant group delay. The variation in group delay cause signal distortion, just as deviation from linear phase cause distortion.

A single stage amplifier’s open-loop transfer function is

$$H(s) = \frac{1}{1 + \tau s} \quad (3.3)$$

Assume the amplifier has a unit DC gain. A cascade of $n$ such amplifiers will
therefore have an overall transfer function of

\[ H(s) = \left( \frac{1}{1 + \tau s} \right)^n \] (3.4)

\( \frac{1}{2\pi} \) is the bandwidth of each amplifier stage.

We use 'Matlab' to calculate the group delay of the amplifier from single stage to three stages in cascade. The m-file could be found on [11]. Then we could read the group delay of different bandwidth for single-stage amplifier (Table 3.1), two-stage amplifier (Table 3.2) and three-stage amplifier (Table 3.3).

<table>
<thead>
<tr>
<th>Bandwidth</th>
<th>gd(4.5MHz)</th>
<th>gd(6MHz)</th>
<th>gd(7.5MHz)</th>
<th>( \tau(max) - \tau(min) )</th>
</tr>
</thead>
<tbody>
<tr>
<td>10MHz</td>
<td>13.23ns</td>
<td>11.71ns</td>
<td>10.18ns</td>
<td>3.05ns</td>
</tr>
<tr>
<td>20MHz</td>
<td>7.577ns</td>
<td>7.306ns</td>
<td>6.978ns</td>
<td>0.6ns</td>
</tr>
<tr>
<td>30MHz</td>
<td>5.189ns</td>
<td>5.103ns</td>
<td>4.995ns</td>
<td>0.24ns</td>
</tr>
<tr>
<td>40MHz</td>
<td>3.929ns</td>
<td>3.891ns</td>
<td>3.844ns</td>
<td>0.09ns</td>
</tr>
</tbody>
</table>

Table 3.1: Group delay for single stage amplifier

<table>
<thead>
<tr>
<th>Bandwidth</th>
<th>gd(4.5MHz)</th>
<th>gd(6MHz)</th>
<th>gd(7.5MHz)</th>
<th>( \tau(max) - \tau(min) )</th>
</tr>
</thead>
<tbody>
<tr>
<td>10MHz</td>
<td>26.5ns</td>
<td>23.64ns</td>
<td>20.38ns</td>
<td>6.12ns</td>
</tr>
<tr>
<td>20MHz</td>
<td>15.15ns</td>
<td>14.61ns</td>
<td>13.96ns</td>
<td>1.2ns</td>
</tr>
<tr>
<td>30MHz</td>
<td>10.38ns</td>
<td>10.12ns</td>
<td>9.987ns</td>
<td>0.4ns</td>
</tr>
<tr>
<td>40MHz</td>
<td>7.859ns</td>
<td>7.785ns</td>
<td>7.687ns</td>
<td>0.2ns</td>
</tr>
</tbody>
</table>

Table 3.2: Group delay for two stages amplifier

<table>
<thead>
<tr>
<th>Bandwidth</th>
<th>gd(4.5MHz)</th>
<th>gd(6MHz)</th>
<th>gd(7.5MHz)</th>
<th>( \tau(max) - \tau(min) )</th>
</tr>
</thead>
<tbody>
<tr>
<td>10MHz</td>
<td>39.75ns</td>
<td>35.2ns</td>
<td>30.58ns</td>
<td>9.17ns</td>
</tr>
<tr>
<td>20MHz</td>
<td>22.73ns</td>
<td>21.92ns</td>
<td>20.93ns</td>
<td>1.8ns</td>
</tr>
<tr>
<td>30MHz</td>
<td>15.57ns</td>
<td>15.31ns</td>
<td>14.98ns</td>
<td>0.6ns</td>
</tr>
<tr>
<td>40MHz</td>
<td>11.79ns</td>
<td>11.68ns</td>
<td>11.53ns</td>
<td>0.3ns</td>
</tr>
</tbody>
</table>

Table 3.3: Group delay for three stages amplifier

We could draw some conclusions from the three tables above:

1. The group delay of the 2\textsuperscript{nd} order and 3\textsuperscript{rd} order amplifier are 2 times and 3 times larger that of the 1\textsuperscript{st} order amplifier.

2. The difference of the group delay for the signal from 4.5MHz to 7.5MHz will become small if we increase the bandwidth.
3. The signal period for the 7.5MHz is about 133ns. We hope that the difference of the group delay between the 4.5MHz signal and 7.5MHz signal will be less than 10%. From the tables above, we could say group delay is not a problem as long as we could make the bandwidth larger than 10MHz.

We used the open loop transfer function of an amplifier $H(s) = \frac{A}{1 + \tau s}$ ($A$ is the DC gain) to calculate the group delay. What about the closed loop amplifier? The transfer function of the closed loop amplifier is

$$H'(s) = \frac{H(s)}{1 + H(s)\beta}$$ (3.5)

The bandwidth is $(1 + A\beta) \cdot \frac{1}{2\pi\tau}$, which should be much larger than the open loop bandwidth. Then the value of group delay will be much smaller.

### 3.1.2 The relationship between TGC and Low Noise Amplifier

The low noise amplifier is in front of the TGC amplifier. It receives the signals from the transducer. The voltage that the receiving transducer produce is from $10\mu V_{p-p}$ to $100mV_{p-p}$. The gain of the low noise amplifier is set by 20dB. So the input signal voltage of the TGC is form $70\mu V_{rms}$ to $0.7V_{rms}$. The output impedance of the LNA should be as small as possible to reduce the impact of the input referred noise current of TGC.

### 3.1.3 The relationship between TGC and Beamformer

The TGC amplifier is connected to the delay&sum circuit used for beamfoming. The output signal of TGC should not exceed the input signal dynamic range of the delay line circuit. The input signal dynamic range of the delay line circuit is from $0.7mV_{rms}$ to $0.7V_{rms}$, which is about 60dB.

### 3.1.4 The relationship between TGC and Harmonic Imaging

The second harmonic imaging technique is utilized. The objective of the TGC amplifier is to compensate the attenuation and spreading of the second harmonic wave. Our colleagues have done a lot of work to investigate the second harmonic wave. In figure 3.2, the input signal the TGC will deal with is from $70\mu V_{rms}$ to $700mV_{rms}$. After the gain compensation, we hope that all the output signal of the TGC will
CHAPTER 3. SPECIFICATION OF TIME GAIN COMPENSATION AMPLIFIER

<table>
<thead>
<tr>
<th>Input signal Range</th>
<th>70\mu V_{rms} \sim 0.7 V_{rms}</th>
</tr>
</thead>
<tbody>
<tr>
<td>Frequency of input signal</td>
<td>4.5MHz~7.5MHz</td>
</tr>
<tr>
<td>Gain Step</td>
<td>0dB/13dB/26dB/39dB tunable</td>
</tr>
<tr>
<td>Gain error</td>
<td>&lt;1dB</td>
</tr>
<tr>
<td>Input Referred Noise</td>
<td>&lt; 70\mu V_{rms} (Noise bandwidth is from 4.5MHz to 7.5MHz)</td>
</tr>
<tr>
<td>Power Consumption</td>
<td>&lt; 100\mu W</td>
</tr>
<tr>
<td>Power Supply</td>
<td>3.3V</td>
</tr>
<tr>
<td>IC Process</td>
<td>0.35\mu m CMOS Process</td>
</tr>
</tbody>
</table>

Table 3.4: Specification of TGC

locate at the range from 0.7mV_{rms} to 700mV_{rms}. That is the signal range that the delay line circuit could deal with.

We could set the gain of 39dB for the signal from 70\mu V_{rms} to 3.2mV_{rms}. For the signal from 3.2mV_{rms} to 32mV_{rms}, we could set the gain of 26dB. We set the gain of 13dB for the signal from 32mV_{rms} to 150mV_{rms}. At last, for the signal larger than 150mV_{rms}, we set the gain of 0dB. The gain setting of the TGC is shown in Figure 3.3. There is one thing to mention the time that the gain being set from one value to another is not fixed. Users can control the timing based on the signal strength in different occasions.

3.2 Specifications of TGC

According to the analysis above, the specifications of the TGC is shown in Table 3.4.

3.2.1 Gain Error

The gain error consists of two parts:

(1) Systematic error due to the roll-off of the amplifier (The gain at 4.5MHz differs from the gain at 7.5MHz). The roll-off gain difference between 4.5 and 7.5 is of less importance. As long as it is below say 3-6 dB and the same for all channels.

(2) Random error due to process variations (e.g. the gain will deviate from the typical simulation value, but should be in a certain statistical range). It is more critical. The element signals will be coherently added and averaged by the delay & sum circuit. The signal levels should not differ too much. The random error below 1dB is fine.
CHAPTER 3. SPECIFICATION OF TIME GAIN COMPENSATION AMPLIFIER

Figure 3.2: The signal compensation schematic (in courtesy of Charles Lancee)
Figure 3.3: The gain setting of TGC
Chapter 4

General Design Methodology

In this chapter, some general implementations for TGC will be presented at first. After that, we need to consider the implementation of our TGC according to the specification and try to make a reasonable choice.

4.1 Discrete Implementation

The majority of commercially available ultrasonic systems occupy large spaces in clinic rooms. Their power consumption can exceed hundred Watts and mainly used near the bedside of patient. Even for the portable system, most of the ultrasound receivers used in medical diagnostics are built with several discrete compounds mounted on the printed circuit board and combined with software drivers.

There are two most famous analog front-end circuit for ultrasound. One is the AD9271 from Analog Devices[1]. The other is AFE5805 designed by Texas Instruments[16].

4.2 Integrated Implementation

There are two ways people have tried to design the TGC amplifier for integrated implementation. One is the voltage amplifier. The other one is the current feedback amplifier (CFA).
CHAPTER 4. GENERAL DESIGN METHODOLOGY

4.2.1 Voltage amplifier

Voltage amplifier is the schematic that we are familiar with. So designers try to design the TGC by this simple idea.

The block diagram of one prior art of TGC amplifier [12] is shown in Figure 4.1. The time gain compensation amplifier consists of three parts: 1. the digital control circuit 2. the analog gain stages 3. a multiplexer used to choose the output voltage.

The whole TGC could provide the gain range form 0dB to 80dB and each stage is set the gain of 20dB. Four cascaded stages are used in the TGC and the differential output is selected by using analog multiplexer. Each stage is composed of a Gm stage and a trans-impedance. To reduce the capacitive load, analog buffers are used to separate the various stages (Figure 4.2).

4.2.2 Current feedback amplifier (CFA)

Current feedback amplifier is widely used in the application of the variable gain amplifier.

As is well known that the voltage feedback amplifier(VFA) is characterized by fixed Gain-Bandwidth-product(GBW)(Figure 4.3). This means the bandwidth is inversely proportional to the gain. If we want to use a VFA to implement the variable gain, the bandwidth will change for different gain setting.
In contrast, structures based on current feedback amplifier (CFA) have a fixed BW independent of gain. Gain bandwidth is proportional to the gain (Figure 4.4). In another words, CFA BW is independent to adjusted gain, whereas the UGB of VFA is a constant value. From this point of view, variable gain systems with CFA perform better than VFA.

The operation of the CFA is best understood by considering the idealized model shown in Figure 4.5. A unity gain buffer is connected between the two input terminals such that $v_{in-}$ is forced to track $v_{in+}$. The inverting/non-inverting input terminals are actually the output/input of the unity gain buffer, which ideally has zero output impedance and infinite input impedance. As a result, the inverting input impedance is zero whereas the non-inverting input impedance is infinite. The output is a linear,
current-controlled voltage source with zero output impedance. The transfer function can be written as:

\[ v_0 = z(s) \cdot i_{inv} \] (4.1)

where \( z(s) \) is the trans-impedance parameter (in Ohms) and \( i_{inv} \) is the current flowing out of the inverting input terminal.

The basic non-inverting feedback configuration of a CFA is shown in Figure 4.6. Analysis of this circuit reveals a unique relationship between the feedback resistor and the closed loop bandwidth. The output voltage is sensed and converted into current, which is fed back to the inverting input. Feedback acts to minimize the inverting input current. The unity gain buffer forces the voltage at the inverting terminal to \( v_{in+} \). Combining the feedback current \( i_f \) and source current \( i_{src} \) at the inverting input terminal gives
\[ i_{\text{inv}} = i_{\text{src}} - i_f = \frac{v_{\text{in}} - v_0}{R_1} - \frac{v_0 - v_{\text{in}}}{R_f} \] (4.2)

The overall closed loop voltage gain is then,

\[ A_{\text{CL}} = \frac{v_0}{v_i} = \frac{1 + \frac{R_f}{R_1}}{1 + \frac{R_f}{z(s)}} \] (4.3)

As expected, the familiar closed loop voltage gain \( 1 + R_f/R_1 \) is obtained as \( z(s) \) approaches infinity. Assuming dominant pole compensation, the trans-impedance can be approximated by,

\[ z(s) = \frac{z_0}{1 + j\left(\frac{w}{w_0}\right)} \] (4.4)

where \( w_0 \) is the -3dB frequency and \( z_0 \) is the DC resistance. Substituting Eq(3.4) into Eq(3.3) gives,

\[ A_{V_{\text{CL}}} = \frac{(1 + \frac{R_f}{R_1})(\frac{z_0}{z_0 + R_f})}{1 + jw(\frac{R_f}{(z_0 + R_f)w_0})} = \frac{1 + \frac{R_f}{R_1}}{1 + j\left(\frac{w}{w_a}\right)} \] (4.5)

Where the approximation for \( A_{V_{\text{CL}}} \) is valid for \( z_0 \geq R_f \). The closed loop amplifier -3dB frequency \( (w_a) \) is given by,

\[ w_a = \frac{(z_0 + R_f)w_0}{R_f} = \frac{z_0w_0}{R_f} \] (4.6)

Thus, for a first order circuit only the feedback resistor determines the closed loop bandwidth. The closed loop gain can be set using resistor \( R_1 \). The relationship between the gain and frequency characteristics is already shown in Figure 4.4.
A modern single stage CFA is shown in Figure 4.7. The input unity gain buffer consists of transistors Q1-Q4. Q3 and Q4 are configured as a complementary pair, push-pull-stage with low output impedance. The bias for this stage is generated by passing a constant current through Q1,2 such that Q3,4 are just on the edge of the active operating region. Q5 and Q6 sense the collector currents $i_c3$ and $i_c4$, which are mirrored to the high impedance node(Z) by Q7 and Q8 respectively. Thus, the effective current flowing into the node Z ($i_c7-i_c8$) is replica of $i_{inv}$. The output stage consisting of Q9-Q12 buffers the voltage at node Z to the output, thereby providing a low output impedance.

The basic model of the presented differential CFA is shown in Figure 4.8.

Table 4.1 compares the proposed design with the prior VGA.

### 4.3 Circuit Topology Consideration

In the last section, the specification of the time gain compensation amplifier is already shown. The low power consumption is the item that we need to pay attention to.
Figure 4.8: Differential CFA model

<table>
<thead>
<tr>
<th>Process</th>
<th>[21]</th>
<th>[17]</th>
<th>[9]</th>
<th>[2]</th>
<th>[12]</th>
<th>[5]</th>
</tr>
</thead>
<tbody>
<tr>
<td>Area (mm²)</td>
<td>N/A</td>
<td>N/A</td>
<td>0.03</td>
<td>0.8</td>
<td>N/A</td>
<td>0.052</td>
</tr>
<tr>
<td>CMFB</td>
<td>N/A</td>
<td>N/A</td>
<td>Yes</td>
<td>N/A</td>
<td>Yes</td>
<td>No</td>
</tr>
<tr>
<td>$V_{dd}$ (V)</td>
<td>5</td>
<td>3</td>
<td>3</td>
<td>5</td>
<td>3.3</td>
<td>3</td>
</tr>
<tr>
<td>Power (mW)</td>
<td>10.5</td>
<td>11.7</td>
<td>0.72</td>
<td>7.5</td>
<td>11</td>
<td>1.96</td>
</tr>
<tr>
<td>Gain (dB)</td>
<td>0-40</td>
<td>0-6</td>
<td>0-12</td>
<td>0-6</td>
<td>0-80</td>
<td>0-46</td>
</tr>
<tr>
<td>Bandwidth (MHz)</td>
<td>12</td>
<td>70</td>
<td>35</td>
<td>110</td>
<td>100</td>
<td>4.5</td>
</tr>
<tr>
<td>GBW (MHz)</td>
<td>1200</td>
<td>140</td>
<td>140</td>
<td>220</td>
<td>&gt;15</td>
<td>900</td>
</tr>
</tbody>
</table>

Table 4.1: Performance comparisons of different VGA
According to the Table 4.1, all the schematics of VGA used by prior work consume much more power than our target. In the latest design of VGA [5], it also use the 0.35µm CMOS Process. However, the power dissipation is 2.18mW with the power supply of 3.0V.

4.3.1 Overall feedback

4.3.1.1 Topology 1 - One stage feedback amplifier

The topology is shown in Figure 4.9. The gain steps are set by changing the ratio between $R_f$ and $R_g$. The load capacitor is 0.25pF. Because we will process the signal from 4.5MHz to 7.5MHz, the bandwidth should be larger than 10MHz to reduce the roll off effect. According to the equation $UGB = \frac{g_m}{2\pi C_L}$, the unity gain bandwidth (UGB) of the amplifier will be about 900MHz.

The trans-conductance will be 1.4mS. We assume that $g_m/I_d = 10$ (in our 0.35µm process), the bias current $I_d$ will be 141µA. For the differential pair, the bias current will be 282µA. Then the power consumption is 930µW. This exceeds our power budget.

4.3.1.2 Topology 2 - Two stages cascaded feedback amplifier

In this schematic, two stages cascaded feedback amplifier are used to design the TGC. The topology is shown in Figure 4.10. We still change the ratio between $R_f$ and $R_g$ to set the gain. The load capacitor is 0.25pF. In order to get a 39dB gain, we could set 20dB for the first stage and 19dB for the second stage. The bandwidth of each stage is still 10MHz with roll of error. The unity gain bandwidth (UGB) of the second stage is about 90MHz. According to the equation $UGB = \frac{g_m}{2\pi C_L}$, the transconductance
will be 141μS. Assume that $g_m/I_d = 10$, the bias current $I_d$ will be 14.1μA. For the differential pair, the bias current will be 28μA. The power consumption will be about 100μW. Assume that the first stage also consumes 100μW. It consumes about 200μW which exceeds the power budget.

Besides, the output impedance of the two stages is big due to the low power consumption. The resistors $R_f$ and $R_g$ must be set high value to prevent loading effect.

4.3.2 Local feedback

The topology of open loop amplifier shown in Figure 4.11 could provide high bandwidth with the low power budget. However, the gain $A_v = g_mR_L$ will vary a lot due to the temperature, process and etc.

The topology of the local feedback shown in Figure 4.12. The trans-conductance amplifier is utilized to make a linear relationship between the input voltage and output current. And a linear relationship between the input current and output voltage
could be derived if the current flow through a trans-impedance or resistor. Then we could get an accurate gain without overall feedback. It is proved that the bandwidth of local feedback is larger than overall feedback under the same power budget.

The transfer function of an overall feedback amplifier is

\[ A_v = \frac{v_0}{v_i} = \frac{A(s)}{1 + \beta A(s)} \quad (4.7) \]

where \( A(s) \) is the open loop transfer function of the opAmp. \( A(s) = \frac{A_0}{1 + j\omega_0} \). Then we could get

\[ A_v = \frac{A_0}{(1 + \beta A_0)(1 + j\omega_0)\beta} \]

So the bandwidth of the overall feedback amplifier is \( \omega_0(1 + A_0)\beta/2\pi \).

The transfer function of the trans-conductance amplifier is

\[ z_g(s) = \frac{A(s)}{1 + A(s)} \cdot \frac{1}{R_1} = \frac{A_0}{(1 + A_0)(1 + j\omega_0)\beta} \cdot \frac{1}{R_1} \]

So the bandwidth of the trans-conductance amplifier is \( \omega_0(1 + A_0)/2\pi \).

The transfer function of the trans-impedance amplifier is

\[ z_g(s) = \frac{A(s)}{1 + A(s)} \cdot R_2 = \frac{A_0}{(1 + A_0)(1 + j\omega_0)\beta} \cdot R_2 \]

So the bandwidth of the trans-conductance amplifier is \( \omega_0(1 + A_0)/2\pi \).

It seems that we could extend the bandwidth a lot if we adopt the local feedback topology. Because in our design, the overall feedback amplifier the value of \( \beta \) is about \( \frac{1}{90} \).
4.4 Conclusion

In this chapter, some prior arts of TGC are presented. All the present work consumes much more power than our target. The overall feedback amplifier is proved difficult to meet our target specification. The local feedback amplifier seems a reasonable choice.
Chapter 5

Circuit Implementation

5.1 The comparison of several trans-conductance amplifiers

Local feedback has been proved as a good topology to realize the function of TGC. The topology consists of two conversion: a voltage-to-current conversion and a current to voltage conversion. A trans-conductance amplifier needed to realize the linear relationship between the voltage and the current is of importance. There are several types of linearization technique for trans-conductor: 1. attenuation 2. non-linear term cancellation 3. Caprio’s pair 4. source degeneration

5.1.1 Attenuation

The ideal output current of a differential input trans-conductance amplifier is

\[ i_0(v_1, v_2) = (v_1 - v_2) \cdot g_m \]  \hspace{1cm} (5.1)

where \( v_1 \) and \( v_2 \) are the positive and negative input signals of the trans-conductance amplifier. In reality, the trans-conductance is implemented by the MOS transistors which are nonlinear devices. Therefore, there exists non-linearity. In general, we can assume that

\[ i_0(v_1, v_2) = \sum a_i v_i^i + \sum b_i v_i^j + \sum \sum c_{ij} v_i^i v_j^j + I_{os} \]

This equation indicates that in order to have a linear trans-conductance, one option is that the input voltage should be made small, such that yields:
Thus a basic linearization idea consists of attenuating the input signals by a factor $k$. This attenuation yields a linearization approximation that can be expressed as

$$i_0(v_1, v_2) \approx k(v_1 - v_2) \cdot g_m$$

The topology is shown in Figure 5.1. But this technique is not suitable for our design for several reasons:

1. In this technique, a block is needed to implement the attenuation effect. Obviously, this block will consume power.

2. The trans-impedance must provide more gain because the input signal has been attenuated.

### 5.1.2 Non-linear term cancellation

This trans-conductor use an optimal algebraic sum of the nonlinear terms to yield ideally only a linear term. This can be done in practice by interconnecting several trans-conductors, which ideally will cancel the nonlinearity yielding only a linear relation between the input voltage and output current. Actually, a simple current mirror (Figure 5.2) is a voltage-to-current converter. The output current of the current mirror is

$$I_0 = \frac{V_{ref} - \phi}{R} \frac{W_2}{W_1} + \frac{V_0}{r_0}$$

(5.2)

$r_0$ is the output impedance of transistor $M_2$. It is clear that the output current of the circuit is subject to change with the bias voltage $\phi$.

It is proposed that the simple circuit may be modified to produce the desired result $I_0 = \frac{V_{ref}}{R}$, by the addition of circuitry (Figure 5.3) to accomplish:
1. The cancellation of the output current dependence on $\phi$.
2. A significant increase in the value of $r_0$ in the second term.

Neglecting the output impedance term, the output current may be expressed as

$$I_0 = \left[ \frac{V_{ref} - \phi_1}{W_1} \right] \frac{W_2}{W_1} - \left[ \frac{1}{2} \frac{V_{ref} - \phi_3}{R/2} \right] \cdot \frac{W_2}{W_1} \cdot \frac{W_4}{W_3} \quad (5.3)$$

For the case where $\phi_1 = \phi_3$ and $\frac{W_4}{W_3} = 1$, the equation becomes $I_0 = \frac{V_{ref}}{R} \left( \frac{W_2}{W_1} \right)$ which is the desired result for a current reference amplifier.

But it is not suitable for the voltage-to-current conversion in the AC domain. When the value of $V_{ref}$ changes, the value of $\phi_1$ and $\phi_3$ will change too.

### 5.1.3 Caprio’s quad

Here we change this structure from bipolar to mosfet shown in Figure 5.4. The loop consists of M1, M2, M3, M4 and R satisfying the equation:

$$V_{in} - V_{gs3} - V_{gs2} - R I_x + V_{gs1} + V_{gs4} = 0$$

If $V_{gs1} + V_{gs4} = V_{gs2} + V_{gs3}$

$$I_x = \frac{V_{in}}{R}$$

$$I_{02} - I_{01} = 2I_x$$
Figure 5.3: Current mirror with $\phi$ cancellation

Actually, the circuit changes the degeneration resistor by introducing a negative resistor(Figure 5.5). We will calculate the negative resistor:

$$I_x = g_{m2}(V_2 - V_4)$$

$$I_x = -g_{m1}(V_1 - V_3)$$

$$I_x = \frac{V_4 - V_3}{R}$$

$$\frac{V_1 - V_2}{I_x} = -\frac{g_m R + 2}{g_m}$$

The value of negative resistor is $-\frac{g_m R + 2}{g_m}$. However, this structure is easy to oscillate if significant parasitic capacitance is present at the sources of M1 and M2.

5.1.4 Linearization techniques by source degeneration

Perhaps the source degeneration technique is the most natural high-frequency linearization scheme [15].

The schematic of source degeneration is shown in Figure 5.6. The output current is related to the input voltage by the following equation [13]:

...
Figure 5.4: The schematic of Caprio’s pair

Figure 5.5: The negative resistor in Caprio’s pair
The trans-conductance of the amplifier is

\[ G_m = \frac{g_m}{1 + g_m R} \]  

(5.6)

If \( v_{id} \ll 2(1 + g_m R)V_{d(sat)} \)

\[ G_m = \frac{g_m}{1 + g_m R} \]  

(5.7)

In general, the source degeneration improves the linearity of the small signal trans-conductance at the price of reducing it by the degeneration factor \( 1 + g_m R \). The linearity could be improved by increasing the value of \( R \) or the transconductance \( g_m \).

But we will try to prove that increasing the value of the degeneration resistor is not a good choice in our design by the following assumption and calculation:

Let’s assume that 20\( \mu \)A is spent on the trans-conductor due to the total power budget is 30\( \mu \)A. The bias current of each pair is 10\( \mu \)A. Then the value of the trans-conductance \( g_m \) is about 100\( \mu \)S (In the 0.35\( \mu \)m process, \( \frac{g_m}{I_d} \) is about 10). If \( g_m R = 10 \gg 1 \), the value of \( R \) will be 100\( k\Omega \). The degeneration resistor will be 200\( k\Omega \). It will produce a lot of noise. Besides, if we want to get a 39dB gain of the
whole system, then resistance of the trans-impedance will be 9MΩ. It will consume a lot of chip area. So it’s better to find a way to increase the trans-conductance.

In our design, source degeneration has been chosen as the topology to realize voltage-to-current conversion.

5.2 Circuit Implementation

We know that the trans-conductance of the source degeneration is

$$G_m = \frac{g_m}{1 + g_m R} = \frac{1}{\frac{1}{g_m} + R}$$

In order to get a linear trans-conductance, we need make the value of the degeneration resistor much larger than $1/g_m$.

Actually we could explain this question from another point of view. Two input transistors could be treated as source follower with output impedance of $1/g_m$ shown in Figure 5.7. The input voltage could not be exactly copied from the gate to the source due to the large value of $1/g_m$. So what we need now is just a source follower with very low output impedance.

5.2.1 Cascoded flipped voltage follower (CASFVF)

The cascoded flipped voltage follower (Figure 5.8) could provide very low output impedance.
5.2.1.1 Low frequency output impedance

The three transistors consist of an unity gain close loop. We could calculate the output impedance by breaking the loop at point X (Figure 5.9). Considering the loading effect, the resistors $R_{L1}$ and $R_{L2}$ are introduced.

\[ R_{L1} = r_{s1} \parallel g_{m1} r_{01} r_{02} \]  
(5.8)

\[ R_{L2} = \frac{r_{s2} + r_{03}}{1 + (g_{m3} + g_{mb3}) r_{03}} \approx \frac{r_{s2} + r_{03}}{g_{m3} r_{03}} \]  
(5.9)

$r_{s1}$ and $r_{s2}$ are the equivalent impedance of the current source $I_{s1}$ and $I_{s2}$.

The open loop output impedance (seen from point Y) is the output impedance of M2 ($r_{02}$) in parallel with impedance seen from the source of the common gate transistor M1 ($r_{cg1}$).

\[ r_{cg1} = \frac{r_{s1} \| R_{L2} + r_{01}}{1 + (g_{m1} + g_{m01}) r_{01}} \approx \frac{r_{s1} \| R_{L2} + r_{01}}{g_{m1} r_{01}} \]  
(5.10)

\[ R_{o,open} = r_{cg1} \| r_{02} \approx \frac{r_{s1} \| R_{L2} + r_{01}}{g_{m1} r_{01}} \| r_{02} \]  
(5.11)

The open loop gain is

\[ A_{v,0} = \frac{v_{0,0}}{v_{i,0}} = \frac{g_{m3} r_{03} \cdot r_{s2}}{r_{03} + r_{s2}} \cdot g_{m2} \cdot \left[ g_{m1} r_{01} r_{02} \| r_{s1} \| R_{L2} \right] \]  
(5.12)

\[ R_{o,close} = \frac{R_{o,open}}{1 + \beta \cdot A_{v,0}} \]  
(5.13)

Because it is a unity gain close loop amplifier, so the feedback factor $\beta = 1$

- Assume current sources $I_{s1}$ and $I_{s2}$ are ideal current sources, so that $r_{s1} \to \infty$, $r_{s2} \to \infty$. Then $r_{cg1} \to \infty$.

\[ R_{o,open} = r_{cg1} \| r_{02} \approx r_{02} \]  
(5.14)

The open loop gain shown in the Figure 5.9 is

\[ A_{v,0} = \frac{v_{0,0}}{v_{i,0}} \approx g_{m3} r_{03} g_{m2} r_{02} g_{m1} r_{01} \]  
(5.15)

The close loop output impedance is
If current sources $I_{s1}$ and $I_{s2}$ are single transistor current sources:

In order to simplify the equation above, we assume $r_{01} = r_{02} = r_{03} = r_{s1} = r_{s2} = r_0$.

$g_m = g_{m1} = g_{m2} = g_{m3} = g_m$ and $r_0 \gg 1/g_m$:

$$R_{0,close} = \frac{1}{g_m r_{01} g_{m3} r_{03} g_{m2}}$$

(5.16)

- If current sources $I_{s1}$ and $I_{s2}$ are single transistor current sources:

$$R_{0,close} = \frac{R_{0,open}}{1+A_{v,0}/\beta} = \frac{r_{02}}{1+g_m r_{03} r_{02} g_{m1} r_{01}}$$

$$R_{0,close} = \frac{1}{g_m r_{01} g_{m3} r_{03} g_{m2}}$$

(5.17)

$$R_{0,open} = r_{cg1} \parallel r_{02} = \frac{1}{g_m}$$

(5.18)

$$A_{v,0} = \frac{v_{o,0}}{v_{i,0}} = g_m r_0$$

(5.19)

Then close loop output impedance is
CHAPTER 5. CIRCUIT IMPLEMENTATION

Figure 5.9: The-open-loop-of-CASFVF

\[ R_{0,\text{close}} = \frac{1}{g_m g_m r_0} \]  \hspace{1cm} (5.20)

• If we use cascoded current source for \( I_{s1} \) and \( I_{s2} \), \( r_{s1} = r_{s2} = g_m r_0^2 \)

\[ R_{0,\text{open}} = r_{cg1} || r_{02} = \frac{2}{g_m} \]  \hspace{1cm} (5.21)

\[ A_{v,0} = \frac{v_{0,0}}{v_{i,0}} = g_m r_0 g_m r_0 \]  \hspace{1cm} (5.22)

\[ R_{0,\text{close}} = \frac{1}{g_m (g_m r_0)^2} \]  \hspace{1cm} (5.23)

5.2.1.2 High frequency stability

The CASFVF is an unity gain feedback amplifier. We analyze the stability of the amplifier by breaking the loop. In Figure 5.9, there are four nodes that will produce poles: M, N, X, Y.

Node X:

The resistance seen from node X to ground (\( R_X \)) is \( R_{L1} \) in parallel with input impedance of the common gate transistor M3.
\[ R_X = R_{L1} \left| \frac{r_{s2} + r_{03}}{1 + (g_{m3} + g_{mb3})r_{03}} \right| (5.24) \]

The capacitance seen from node X to ground \((C_X)\) consists \(C_{sg3}\), the parasitic capacitance \(C_{cs1}\) of current source \(I_{s1}\) and \(C_{dg1}\).

Node M:
the resistance seen from node M to ground \((R_M)\) is:

\[ R_M = r_{03} \left| r_{s2} \right| (5.25) \]

The capacitance seen from node M to ground \((C_M)\) consists of the capacitance \(C_{gs2}\), the parasitic capacitance \(C_{cs2}\) of current source \(I_{s2}\) and \(C_{dg3}\).

Node Y:
The resistance seen from node Y to ground \((R_Y)\) is \(r_{02}\) in parallel with the input impedance of the common gate transistor M1.

\[ R_Y = r_{02} \left| R_{L2} + r_{01} \right| \frac{r_{s2}}{1 + (g_{m1} + g_{mb1})r_{01}} (5.26) \]

The capacitance seen from node Y to ground \((C_Y)\) consists of the capacitance \(C_{sg1}\), \(C_{ds2}\) and \(C_{dg2}\).

Node N:
The resistance seen from node N to ground \((R_N)\) is \(R_{L2}\) in parallel with \(r_{s1}\) and the output impedance of the cascoded transistors M1&M2.

\[ R_N = R_{L2} \left| r_{s2} \right| g_{m1}r_{01}r_{02} (5.27) \]

The capacitance seen from node N to ground \((C_N)\) consists \(C_{sg3}\), the parasitic capacitance \(C_{cs1}\) of current source \(I_{s1}\) and \(C_{dg1}\).

Assuming all the transistors have the same size, then \(C_X = C_M = C_Y = C_N\).

In order the simplify the equation above, we assume \(r_{01} = r_{02} = r_{03} = r_{s1} = r_{s2} = r_0\), \(g_{m1} = g_{m2} = g_{m3} = g_m \gg g_{mb}\) and \(r_0 \gg 1/g_m\):

\[ R_X \approx \frac{2}{g_m} \quad (5.28) \]

\[ R_M \approx \frac{r_0}{2} \quad (5.29) \]
\[ R_Y \approx \frac{1}{g_m} \]  \hspace{1cm} (5.30)

\[ R_N = \frac{2}{g_m} \]  \hspace{1cm} (5.31)

\( R_M \) is much larger than \( R_X \), \( R_Y \) and \( R_N \). So the node M is dominant pole of the CASFVF.

If we use cascoded current source for \( I_{s1} \) and \( I_{s2} \), \( r_{s1} = r_{s2} = g_m r_0^2 \):

\[ R_X \approx r_0 \]  \hspace{1cm} (5.32)

\[ R_M \approx r_0 \]  \hspace{1cm} (5.33)

\[ R_Y \approx \frac{2}{g_m} \]  \hspace{1cm} (5.34)

\[ R_N \approx r_0 \]  \hspace{1cm} (5.35)

\( R_X \), \( R_Y \) and \( R_M \) are almost on the same order. The node M, X, Y are dominant poles of the CASFVF. We need to do frequency compensation.

A compensation capacitor is added at node M which is shown in Figure 5.10. The gain bandwidth is \( g_{m2}/2\pi C_C \).

Actually, there is a zero from the node M to node Y. The value of the zero is:

\[ S_{zero} = \frac{g_{m2}}{C_{gd2}} \]  \hspace{1cm} (5.36)

### 5.2.2 Trans-conductor by cascoded flipped voltage follower structure

A voltage follower with relatively low output impedance has been built. So we could get a linear relationship between the input voltage and output by the source degeneration schematic with a small degeneration resistor. The block diagram of our schematic is shown in Figure 5.11.

We will analyze the schematic step by step. The schematic of source degeneration
Figure 5.10: The compensation of CASFVF

Figure 5.11: Block diagram of trans-conductor by CASFVF
by the cascoded flipped voltage follower is shown in Figure 5.12. Two differential signals is applied to the gate of the input pair $M_{1A}$ and $M_{1B}$. The input voltage will be copied to the source of the input pair. The relation of the is

$$V_0^+ - V_0^- = \frac{V_i^+ - V_i^-}{R_{out1} + R_{out2} + R_s} R_s$$  \hspace{1cm} (5.37)$$

$R_{out1}$ and $R_{out2}$ are the output impedances of two CASFVF. If $R_s \gg R_{out1} = R_{out2}$, the input voltage will be exactly copied to the source of the differential pair.

$$V_0^+ - V_0^- = V_i^+ - V_i^-$$  \hspace{1cm} (5.38)$$

There is a current $i_0$ flowing through the degeneration resistor $R_s$.

$$i_0 = \frac{V_0^+ - V_0^-}{R_s} = \frac{V_i^+ - V_i^-}{R_s}$$  \hspace{1cm} (5.39)$$

Then the current flowing through $M_{2A}$ will be reduced by $i_0$, while the current flow through $M_{2B}$ will increase by $i_0$.

A linear voltage to current converter has been presented. However, there is a problem with this schematic that the output current cannot be read from the transistors $M_{2A}$ and $M_{2B}$ directly. There is a current mirror needed to read the output current. To copy the current exactly, a cascoded current mirror is preferred to prevent the channel length modulation effect (Figure 5.13).

Because $M2$ is part of the CASFVF, it can not be diode connected like cascoded current mirror. However the drain voltages of $M2$ and $M5$ are still the same. Now we could get the relationship between the output current and input voltage:

$$i_{01} - i_{02} = 2 \times \frac{V_i^+ - V_i^-}{R_s}$$  \hspace{1cm} (5.40)$$

This is a linear relationship between the input voltage and the output current.

### 5.2.3 Trans-impedance

After building the block of voltage to current converter, there should be a trans-impedance to convert the accurate current into voltage. However, according to the transfer function of the trans-impedance, we need to create a high gain amplifier to make sure the transfer function is $R_f$. It must consume large power. In stead of trans-impedance, a resistor at the output of the trans-conductor is used. It could
Figure 5.12: The schematic of the source degeneration by CASFVF

Figure 5.13: The trans-conductor with current mirror by CASFVF
still provide an accurate current to voltage.

5.2.4 Main circuit

Now we could combine the trans-conductor and the trans-impedance to get an opAmp with accurate gain (Figure 5.14).

The transfer function of the opAmp is

$$V_{\text{out}} - V_{\text{in}} = 2 \frac{R_L}{R_s} (V^+_i - V^-_i)$$  \hspace{1cm} (5.41)

Because the amplifier is local feedback and overall open-loop, high bandwidth performance can be derived under the same power budget as we have analyzed. The mismatch of the input pair will cause offset problem. However, DC offset is not critical in our design.

From the equation of (5.41), we could change the gain by resetting the value of resistor $R_s$. The main circuit of the time gain compensation amplifier is shown in 5.15.

The matching of the transistors $M_5A$, $M_5B$, $M_2A$, $M_2B$ is also very critical. The mismatching between $M_2$ and $M_5$ will make the gain inaccurate. The mismatching between $M_5A$ and $M_5B$ will cause DC offset at the output.

5.2.5 Kelvin switch

If the schematic in Figure 5.15 is implemented, the on-resistance of the switch is in series with the degeneration resistor. The on-resistance varies a lot when the process changes. That will affect the accuracy of the gain. The kelvin switch could solve this problem, which is shown in Figure 5.17.

This idea originates from the kelvin resistance measurement (Figure 5.16). We want to measure the voltage across the resistor $R$. Ideally, the resistance of the voltmeter is infinite. There is no current flow through the voltmeter, sw1 and sw2. The voltmeter will measure the value of the resistor precisely. The on-resistance of sw1 and sw2 doesn’t affect the measurement result.

In Figure 5.17, the current flowing through $M_{1A}$ and sw1 is $i_{s1A} - i_{s2A}$. The current flowing through $M_{1B}$ and sw2 is $i_{s1B} - i_{s2B}$. These values are fixed due to the ideal current sources according to the kirchoff’s current law. The gate source voltages of $M_{1A}$ and $M_{1B}$ will not change. The signals from the gate will be exactly
Figure 5.14: The schematic of the main circuit opAmp

Figure 5.15: The schematic of the variable gain amplifier
copied to the source. The signals will be copied from the one end to the other end of sw1 and sw2 exactly. Then an accurate current $\frac{V^+-V^-}{R}$ is produced. According to the kirchoff’s current law, the current flowing through sw3 consists of the current from sw1 and the current from degeneration resistor. The signal current only flow through $M2_A$, $M4_A$, sw3, $R$, sw4, $M4_B$, $M2_B$. There is no AC current flowing through sw1 and sw2.

5.2.6 Gain setting

The gain stages of 0dB/13dB/26dB/39dB are required. However, these numbers are not integer. The gain of the opAmp is decided by:

$$A_v = \frac{2R_L}{R_s} \quad (5.42)$$

In order to get an accurate gain, the matching between the resistor $R_L$ and $R_s$ is critical. The value of $R_L$ should be integral multiple of $R_s$. We change the gain stage to 1/4/20/100 corresponding to 0dB/12dB/26dB/40dB. All these gain are the value for low frequency. The signal frequency from 4.5MHz to 7.5MHz, there will be some roll of the gain. As long as the signal at 6MHz is above 38dB, then it’s fine.

5.2.7 Output stage

We use the source follower working as output stages to decrease the output impedance. The final circuit is shown in Figure 5.18

5.3 Simulation Result

The simulation results of the TGC will be presented in this section.
Figure 5.17: The schematic using kelvin switch

Figure 5.18: The final circuit
5.3.1 AC Simulation Result

5.3.1.1 39dB gain

Firstly, the Monte-Carlo AC simulation result for the 39dB gain is shown in Figure 5.19. At central frequency 6MHz, the gain is from 38.44dB to 39.11dB. The difference is about 0.7dB which is smaller than 1dB.

5.3.1.2 26dB gain

The Monte-Carlo AC simulation result for the 26dB gain is shown in Figure 5.20. At central frequency 6MHz, the gain is from 24.96dB to 25.66dB. The difference is about 0.7dB.

5.3.1.3 13dB gain

The Monte Carlo AC simulation result for the 13dB gain is shown in Figure 5.21. At central frequency 6MHz, the gain is from 11dB to 11.7dB. The difference is about 0.7dB.
Figure 5.20: The Mento-Carlo Simulation Result of 26dB

Figure 5.21: The Mento-Carlo simulation result of 13dB
5.3.1.4 0dB gain

The Mento-Carlo AC simulation result for the 13dB gain is shown in Figure 5.22. At central frequency 6MHz, the gain is from -3.86dB to -3.2dB. The difference is about 0.7dB which is still much smaller than 1dB.

5.3.2 Transient Simulation

The transient simulation result for the 6MHz signal will be presented.

5.3.2.1 39dB gain

The input signal is $4.52mV_{p-p}$ sine wave, the output signal is shown in Figure 5.23.

5.3.2.2 26dB gain

The input signal is $14.1mV_{p-p}$ sine wave, the output signal is shown in Figure 5.24.

5.3.2.3 13dB gain

The input signal is $141mV_{p-p}$ sine wave, The output signal is shown in Figure 5.25.
Figure 5.23: The output signal for 39dB transient simulation

Figure 5.24: The output signal for 26dB transient simulation
5.3.2.4 0dB gain

The input signal is $452mV_{p-p}$ sine wave. The output signal is shown in Figure 5.26.

5.3.3 The transit time of different gain setting

The transit time for different gain setting is shown in Figure 5.27. From 0dB to 13dB, the transit time is about 240nS. From 13dB to 26dB, the transit time is about 346nS. From 26dB to 39dB, the transit time is 500nS.

5.3.4 Noise simulation

The noise simulation is performed under the 39dB gain, because it’s the maximum gain stage and receiving the weakest signal. The delay line circuit following the TGC and ADC in the mainframe machine will do the bandwidth limit, so we only need to integral the noise spectrum from 3MHz to 9MHz (Figure 5.28).

The input referred noise is $45\mu V_{rms}$.

The input signal is $v_{0,mim} = 70\mu V_{rms}$.
Figure 5.26: The output signal for 0dB transient simulation

Figure 5.27: The transit time for different gain settings
So the signal to noise ratio for the worst case is 4dB.

### 5.3.5 Power consumption

The power consumption is about 130µW.

### 5.4 Layout and Post-layout Simulation

The layout of the TGC is shown in Figure 5.29.

In order to improve the chance that our chip could work, the post layout simulation has been performed.

#### 5.4.1 Post-layout AC simulation result

##### 5.4.1.1 39dB gain

The AC simulation result for the 39dB gain is shown in Figure 5.30. At central frequency 6MHz, the gain is 37.9dB. The gain at 4.5MHz is about 38.5dB and the signal at 7.5MHz is about 37.3dB. The difference is about 1.2dB.
Figure 5.29: The layout of the time gain compensation amplifier

Figure 5.30: AC post layout simulation result for 39dB
5.4.1.2 26dB gain

The AC simulation result for the 26dB gain is shown in Figure 5.31. At central frequency 6MHz, the gain is 24.8dB. The gain at 4.5MHz is about 25.1dB and the signal at 7.5MHz is about 24.5dB. The difference is about 0.3dB.

5.4.1.3 13dB gain

The AC simulation result for the 13dB gain is shown in Figure 5.32. At central frequency 6MHz, the gain is 11.2dB. The gain at 4.5MHz is about 11.3dB and the signal at 7.5MHz is about 11dB. The difference is about 0.3dB.

5.4.1.4 0dB gain

We give the ac simulation result for the 0dB gain(Figure 5.33). At central frequency 6MHz, the gain is -1dB. The gain at 4.5MHz is about -0.8dB and the signal at 7.5MHz is about -1.3dB. The difference is about 0.5dB.
Figure 5.32: AC post layout simulation result for 13dB

Figure 5.33: AC post layout simulation result for 0dB
5.4.2 Post-layout transient simulation result

5.4.2.1 39dB gain

The input signal is $4.52mV_{p-p}$ sinewave, the output signal is shown in Figure 5.34.

5.4.2.2 26dB gain

The input signal is $14.1mV_{p-p}$ sinewave, the output signal is shown in Figure 5.35.

5.4.2.3 13dB gain

The input signal is $141mV_{p-p}$ sinewave, the output signal is shown in Figure 5.36.

5.4.2.4 0dB gain

The input signal is $452mV_{p-p}$ sinewave, the output signal is shown in Figure 5.37.
Figure 5.35: The output signal for 26dB post layout transient simulation

Figure 5.36: The output signal for 13dB post layout transient simulation
Figure 5.37: The output signal for 0dB post layout transient simulation
Chapter 6

Conclusion

It seems we don’t have very much experience to design the amplifier working at several MHz. The relationship between the bandwidth and power is the key point of our design specification. In this thesis, a low power time gain compensation amplifier is presented and corresponding simulation results are performed. This chip has been taped out on December 7th, 2009. We will test the chip in March of 2010. Comparing to the previous work, this design consumes much less power and the circuit schematic is very simple. The local feedback system is implemented, so the bandwidth is larger than the overall feedback system under the same power. However, we must pay attention to the stability of the CASFVF because it is the feedback loop. And the output impedance of the CASFVF at high frequency will become much larger than the value at low frequency.

Future work should include:

- Measuring the chip in March 2010.
- Try to connect the TGC with LNA and Beamfoming Circuit.
- Redraw the layout, because it wastes a lot of area now.
- Investigate the current feedback amplifier. Maybe we could meet the specification if we use this topology properly.
Bibliography


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Appendix A

Test Circuit

Our chip will be package in Delft Institute for Microelectronics and Submicron Technology. The die size $1 mm^2(1.123 mm \times 0.864 mm)$ will be mounted in a DIL 16 package (Figure A.1). The pin configurations are shown in Figure A.2 and Table A.1.

Measurement Block Diagram

The measurement block diagram is shown in Figure A.3. A function generator is used to generate sine wave signal from 4.5MHz to 7.5MHz. Control signals are used for $V_{s1}$, $V_{s2}$, $V_{s3}$ and $V_{s4}$ to set the different gains. The voltage for control signal is 3.3V. In order to prevent the signal distortion of control signals due to long cable, schmitt triggers are used on PCB. A regulator is used to produce accurate power supply 3.3V. The output signal will be show on oscilloscope.

We will process the input signal from $70 \mu V_{rms}$ to $0.7 V_{rms}$. The function generator used is HP33120A. It could produce the signal from $35 mV_{rms}$ to $7 V_{rms}$. So we need a signal attenuator to produce the signals below $35 mV_{rms}$. The attenuator consists of a resistor ladder and a unity gain buffer (Figure A.4). We scale the signal voltage by changing the value of resistor $R_s$. In order to avoid scaling the DC voltage, the ground of the function generator is connected to an external DC voltage source. THS4504 produced by Texas Instruments is chosen to work as the unity gain buffer. It is a single-ended to differential Conversion Amplifier.
Figure A.1: Package of the chip
Figure A.2: Pins configuration

<table>
<thead>
<tr>
<th>Pin Number</th>
<th>Pin Name</th>
<th>Pin Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>SUB</td>
<td>the ground of the pad ring</td>
</tr>
<tr>
<td>3</td>
<td>$V_{s1}$</td>
<td>the switch for the 0dB gain</td>
</tr>
<tr>
<td>4</td>
<td>$V_{s3}$</td>
<td>the switch for the 13dB gain</td>
</tr>
<tr>
<td>5</td>
<td>EXTres</td>
<td>It is connected to the external resistor which is used in the pad driving buffer.</td>
</tr>
<tr>
<td>6</td>
<td>Vbuf</td>
<td>the supply voltage for pad driving buffer</td>
</tr>
<tr>
<td>8</td>
<td>buffer_plus</td>
<td>the port of the output signal</td>
</tr>
<tr>
<td>9</td>
<td>buffer_minus</td>
<td>the port of the other output signal</td>
</tr>
<tr>
<td>10</td>
<td>Vdd</td>
<td>the supply voltage used for the TGC</td>
</tr>
<tr>
<td>11</td>
<td>$V_{s2}$</td>
<td>the switch for the 26dB gain</td>
</tr>
<tr>
<td>12</td>
<td>$V_{in2}$</td>
<td>the port of the input signal</td>
</tr>
<tr>
<td>13</td>
<td>$V_{in1}$</td>
<td>the port of the other input signal</td>
</tr>
<tr>
<td>14</td>
<td>$V_{s1}$</td>
<td>the switch for 39dB gain</td>
</tr>
</tbody>
</table>

Table A.1: Pin configuration
**Measurement Setting**

- 39dB gain

The input signal amplitudes are set of 70\(\mu V_{rms}\), 0.5\(mV_{rms}\), 1\(mV_{rms}\) and 3\(mV_{rms}\). The signal frequencies are set of 4.5MHz, 6MHz, 7.5MHz.

- 26dB gain

The input signal amplitudes are set of 3.5\(mV_{rms}\), 15\(mV_{rms}\) and 30\(mV_{rms}\). The signal frequencies are set of 4.5MHz, 6MHz, 7.5MHz.

- 13dB gain

The input signal amplitudes are set of 50\(mV_{rms}\), 100\(mV_{rms}\) and 150\(mV_{rms}\). The signal frequencies are set of 4.5MHz, 6MHz, 7.5MHz.

- 0dB gain

The input signal amplitudes are set of 200\(mV_{rms}\), 400\(mV_{rms}\) and 700\(mV_{rms}\). The signal frequencies are set of 4.5MHz, 6MHz, 7.5MHz.

- A network analyzer will be used to test the AC frequency response of different gain stages.

- The transit time for different gain stages will also be tested.
Figure A.4: The voltage attenuator