Detection, Characterization and Extinction of Electric Arcs in DC Systems

Load side Arc Detection in LVDC Grids and Bus Transfer in HVDC Systems

Aditya Shekhar
Detection, Characterization and Extinction of Electric Arcs in DC Systems
Load side Arc Detection in LVDC Grids and Bus Transfer in HVDC Systems

MASTER OF SCIENCE THESIS

For the degree of Master of Science in Electrical Power Engineering at Delft University of Technology

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by

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Advancements in power electronics has sparked the adaptability of dc systems in varied application fields. The phenomenon of electric arcing in such dc systems, arising due to the absence of zero crossing of current during normal operation, has impeded the widespread proliferation of dc-based technologies in the market. Considering the advantages presented by adopting dc over the ac systems in terms of efficiency and compatibility with renewable energy, it is of great interest to remove any such impediments involved in developing a mature, viable and sophisticated dc system.

In context of low voltage dc microgrids, a novel arc detection method has been proposed and validated through simulations as well as real time experiments. It is shown that the detection scheme is able to rapidly and selectively identify series arcing by solely monitoring the load side voltage. The boundaries associated with threshold trigger voltage selection and detection time are defined based on varied circuit configurations. The algorithm is designed to be tolerant to the grid side voltage fluctuations in order to avoid spurious triggering.

In context of arc characterization in high voltage dc systems, the bus transfer facilitated by GIS disconnector is studied. Analytical expression for recovery and re-strike voltage is derived to enable their estimation from the measurable space variables of the experimental set-up. The simulation model emulating the experimental set-up and the parameter estimation methodology is developed and validated. By varying the configurable parameters like initial capacitor voltage, switching frequency and source inductances, the possible recovery voltages across the disconnector is simulated. Based on this, a series of experiments aimed at studying the arcing characteristics during bus transfer process are designed and conducted. Finally, analysis tools are created to estimate the parameters describing the arc behaviour, such as burn time, starting arc current, corrected arc voltage, input arc energy, recovery and re-strike voltage.
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Aditya Shekhar
ॐ गुरु ब्रह्म गुरु विष्णु गुरु देवो महेश्वर
गुरु साक्षात्परब्रह्म तस्मै श्री गुरवे नमः

Guru Brahma, Guru Vishnu, Guru Devo Maheshwara
Guru Saakshaat, Param Brahma,
Tasmai Shree Guruvey Namaha
Advancements in power electronics has sparked the adaptability of dc systems in varied application fields [1, 2]. The phenomenon of electric arcing in such dc systems, arising due to the absence of zero crossing of current during normal operation, has impeded the widespread proliferation of dc-based technologies in the market. Considering the advantages presented by adopting dc over the ac systems in terms of efficiency and compatibility with green renewable energy, it is of great interest to remove any such impediments involved in developing a mature, viable and sophisticated dc system.

This thesis is divided into two parts, both aimed at mitigating the arcing problem in dc systems. The first part looks into the low voltage dc (LVDC) systems and offers a load side arc detection method which is rapid and selective in identifying and extinguishing arcs by solely monitoring the load side voltage. In this context, the following research objectives are fulfilled:

- The proposed arc detection scheme is described and validated, both through theoretical simulations and real time experimental studies.
- The selectivity and localized action of the developed detection algorithm to extinguish arcs without disturbing the other parallel loads in the system is depicted.
- The algorithm is designed in such a way that it is insensitive to the low frequency grid side voltage fluctuations in order to avoid spurious triggering.
- The boundary of operation based on varied circuit configurations and selected set point of threshold detection voltage is precisely defined. In this context, the quantified impact on detection time is described, both analytically and experimentally.
Second part of this thesis deals with the arcing behaviour in the high voltage dc (HVDC) system. Tools have been developed to analyse the characteristics of arcs when a GIS disconnector carries out a high dc current, high voltage bus transfer between two parallel buses, a fundamental system application in multi-terminal HVDC substation. The success of this technology has noted advantages, which are discussed in detail in the introductory chapter of this part. The following research objectives are accomplished:

- The experimental set-up used to study the arc characteristics is described and a simulation model emulating the set-up is developed.

- A methodology is developed to estimate all the unknown parameters (inductances) of the system through specifically designed experiments.

- Analytical expression for recovery and re-strike voltage is derived. These parameters are very important in describing the operating limits of the GIS disconnector and are not precisely measurable. The analytical expression provides a way to estimate them through the measurable space variables of the experimental set-up.

- Impact of changing the circuit parameters like initial capacitor voltage, switching frequency and source inductance (all configurable in the actual experimental set-up) on possible recovery voltages is simulated. Based on the results, bus transfer experiments are designed and conducted.

- Due to non-zero GIS disconnector inductance, the exact arc voltage is not measurable. A method to compute the same with measured data is presented.

- Graphical user interface is developed to estimate the parameters like burn time, input arc energy and power, starting arc current, exact arc voltage, recovery voltage and re-strike voltage, on which arc characteristics during bus transfer may depend upon.

- Analysis results for typical bus transfer experiments are presented.
Part I

Load-side Series Arc Detection in Low Voltage DC Microgrids
Decentralized dc nano- and microgrids provide interesting opportunities to address the challenges faced by the modern energy distribution systems [1]. Apart from inherently more efficient operation and saving on materials as compared to ac distribution grids, they can offer higher flexibility and availability. In countries facing rapid urban expansion, the idea of designing self sustainable smart cities as satellite towns of main cities is increasingly interesting [3,4]. Furthermore, in developing countries where grid infrastructure is not as extensive, standalone dc nano grids in remote rural areas can prove to be a lifeline. This will not only provide access to energy to millions of people, but also increase the reach of renewable energy such as PV technology, which is inherently dc in nature. Sudden replacement of ac infrastructure is challenging, however dc ready devices, working on both ac and dc, could simplify transition [5]. Standardization has first to be brought forward.

In dc microgrids, arcs do not extinguish as easily as ac ones due to the absence of current zero crossing. This demands a rapid protective response in detecting and eliminating any arcs that may arise, particularly in case of unintended energized unplugging of loads. Various methods are discussed in literature [6–8]. Current technology uses mechanically designed contacts to reduce the risk of arcing and to shield the users from the arc location. Such devices are prone to wear and tear and may fail after several usage cycles. Arc reduction using internal diode in the plug is explored in [7]. Arcs can also be prevented by plugs with early disconnection pins wherein the load can monitor these pins and switch off before the main contacts open. Another solution is an arc free dc plug [8] that uses a solid state switch in the plug itself to eliminate any arcs.

While these solutions require special plug designs and additional components, the algorithm proposed in this thesis detects the electrode dependent drop in the load side voltage to identify series arcing in the network. A simplified equivalent circuit is depicted in Figure 2-1 and a typical measurement for load side voltage profile during series arcing for constant resistance load without any parallel input capacitance is illustrated.

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Electric arcs are formed when two electrodes of an energized electric circuit with non-zero current are drawn apart. Just before the electrodes separate, the high contact resistance vaporizes the metal and in combination with electrons ejected from thermionic emission that ionize the air between the electrodes, creates a conductive plasma channel to bridge the gap. The arc can sustain itself if the input energy is greater than the energy removed through heat transfer.

In the absence of zero crossing of current in dc circuits, extinguishing the arc is more difficult. Sustained series arc faults, if left unattended, can cause fires and serious property damage [9]. The 2011 National Electric Code [10], has defined guidelines for photovoltaic (PV) systems with operating voltage of 80 V or higher and necessitates arc fault current interrupters (AFCI) to detect arcs greater than 300 W and interrupt them within 2 s.

With the proliferation of dc systems in the PV market, research by Sandia, SMA, Tigo Energy, Eaton, etc have developed an AFCI functionality in their products based on the detection of high frequency ac noise associated with the arcing behaviour [11–13]. In these applications, the low frequency component of the current and voltage signals cannot be used in the detection of series arcs because the IV characteristics of the PV module side change unpredictably with weather conditions and due to the presence of maximum power point tracking algorithms at the converter side [14].

The recognized disadvantage of such a centralized arc fault detection is that the entire system down the line is shut down [6], therefore selective isolation of fault location from the rest of the grid becomes important. Detecting the load voltage drop at arc initiation offers a possibility of rapid localized protective response. Using the here proposed method, the protection scheme can allow selectivity for series arc detection and prevent tripping of a larger part of the grid. With proper coordination with grid side converter, which detects high frequency noise signature, differentiation between series and parallel arcs can also be achieved.

In this thesis, the focus is on validating the developed arc detection scheme both through
simulations and real time experiments. The initial findings were published in [16] and the concerned paper is attached as Appendix A. Subsequent chapters strengthen the developed idea, define clear operating boundaries and offer working solutions to contingencies the detection algorithm might face in the actual grid connected system.

In Chapter 3, the proposed arc detection method is explained in detail and theoretically validated via simulations. Selectivity of the detection scheme is depicted in a parallel load system, wherein, the algorithm is able to identify and extinguish the arc by disconnecting the concerned load without disturbing the other connected parallel load.

Further, a contingency associated with vulnerability to grid voltage fluctuations is identified. In order to avoid spurious triggering [16] bandpass filter is designed to be insensitive to such fluctuations that are of low frequency [15]. Finally, the impact of grid inductance, resistance and load capacitance value on the detection scheme is studied and operating boundaries in terms of set threshold detection voltages and arc detection time are defined.

Chapter 4 presents the experimental validation of the proposed detection scheme both with off-line study as well as online study in real time. Impact of threshold voltage set point on detection time and signal pitch is depicted for 100 V and 400 V supplies.
Chapter 3

Theoretical Study on Arc Detection

The proposed arc detection algorithm has been validated through MATLAB simulations. The arc model used, simulations for arc detection with constant resistance and constant power load and subsequent experimental study resulting in a publication [16] is attached as Appendix A for reference.

The arc detection algorithm is described in detail in Section 3-1. Simulation results for arc detection and selective disconnection in network with parallel loads is described in 3-2. Section 3-3 develops on the discrete band pass filter used in the arc detection algorithm and describes the impact of a range of grid inductance and load capacitances on the detection voltage.

3-1 Proposed Arc Detection Method

The drop in the load voltage associated with series arc initiation is specifically dependent on the electrode material [17] and can be detected by the load side power electronic converter, which can then respond accordingly to detach the load from the grid by reducing the load current to zero and thereby extinguishing the arc rapidly. The flow diagram depicting the proposed algorithm is shown in Figure 3-1.

The load voltage $V_{load}$ measured in the equivalent circuit of Figure 2-1 is passed through the low pass filters (LPF), with Laplace transfer functions (3-1) and (3-2).

$$V_{slp}(s) = \frac{1}{1 + \tau_{s} s} V_{load}(s) \quad (3-1)$$

$$V_{f lp}(s) = \frac{1}{1 + \tau_{f} s} V_{load}(s) \quad (3-2)$$
The output voltages $V_{slp}$ and $V_{flp}$ of the slow and fast LPF are compared as per (3-3) to create a band-pass filter with time constant for slow LPF $\tau_{slp}$ and fast LPF $\tau_{flp}$ chosen such that the detection scheme is resistant to low frequency (below 150 Hz) fluctuations in the grid side voltage and high frequency noise (>10 kHz) due to switching operation. A complete analysis involving the choice of filter time constants is provided in Section 3-3.

$$\Delta V = V_{slp} - V_{flp} > V_{detect} \quad (3-3)$$

As soon as the difference $\Delta V$ is greater than the trigger voltage $V_{detect}$, the arc is detected and the device power electronics can initiate the switch off action. One possible way is to linearly reduce the load current to zero. The choice of the slope with which the algorithm decreases the load current depends on the circuit constraints and the time within which the arc needs to be extinguished.

The choice of the threshold trigger voltage influences the speed of the arc detection and also has to account for the attenuation due to the bandpass filter of the detection algorithm. Hence, it is lower than the actual electrode dependent voltage drop associated with the copper electrode. However, a very small value may result in spurious triggering and must be avoided. Boundary of sensitivity of detection scheme and associated detection time with the choice of trigger voltage level is described in Section 3-3-3.

The discrete time realization for the use in micro-controllers is given by (3-4) wherein, the smoothing factor $\alpha$ is computed using (3-5) based on the sample time $\Delta T$ and the required time constant $\tau_{lpf}$ for low pass filter from (3-1) and (3-2). Theory on digital signal processing is presented in [20].

$$V_{lpf,k} = (1 - \alpha)V_{lpf,k-1} + \alpha V_{load,k} \quad (3-4)$$

$$\alpha = \frac{\Delta T}{\tau_{lpf} + \Delta T} \quad (3-5)$$

Figure 3-1: Arc detection algorithm based on drop in load voltage due to minimum electrode gap voltage of series arcs.
3-2 Arc Detection and Selectivity with Parallel Loads

Figure 3-2. shows the equivalent circuit for two constant power loads of 470W connected in parallel via cables of resistances \( R_{cab1} \) and \( R_{cab2} \) of 0.01Ω each and inductances \( L_{cab1} \) and \( L_{cab2} \) of 3μH each to a grid of 100V constant voltage and inductance \( L_{dc} \) and resistance \( R_{dc} \) of 100μH and 0.25Ω respectively.

![Equivalent Circuit Diagram](image)

**Figure 3-2:** Equivalent circuit for two parallel constant power loads.

The corresponding state space equations are given by:

\[
\frac{dI_{dc}}{dt} = \frac{1}{L_{dc}} (V_{dc} - V_{com} - R_{dc}I_{dc}) \quad (3-6)
\]

\[
\frac{dI_{cab1}}{dt} = \frac{P_1}{L_{cab1}} (V_{com} - V_{L1} - I_{cab1}(R_{cab1} + R_{arc1})) \quad (3-7)
\]

\[
\frac{dI_{cab2}}{dt} = \frac{P_2}{L_{cab2}} (V_{com} - V_{L2} - I_{cab2}(R_{cab2} + R_{arc2})) \quad (3-8)
\]

\[
\frac{dV_{L1}}{dt} = \frac{1}{C_{L1}} (I_{cab1} - I_{L1}) \quad (3-9)
\]

\[
\frac{dV_{L2}}{dt} = \frac{1}{C_{L2}} (I_{cab2} - I_{L2}) \quad (3-10)
\]

From (3-6)-(3-8), the voltage at the common coupling point \( V_{com} \) is given by (3-11). The time constants \( \tau_{dc} = \frac{L_{dc}}{R_{dc}}, \tau_{cab1} = \frac{L_{cab1}}{(R_{cab1} + P_1R_{arc1})} \) and \( \tau_{cab2} = \frac{L_{cab2}}{(R_{cab2} + P_2R_{arc2})} \).

\[
V_{com} = \left( \frac{P_1V_{L1}}{L_{cab1}} + \frac{P_2V_{L2}}{L_{cab2}} + \frac{V_{dc}}{L_{dc}} \right) - \left( \frac{I_{dc}}{\tau_{dc}} - \frac{P_1I_{cab1}}{\tau_{cab1}} - \frac{P_2I_{cab2}}{\tau_{cab2}} \right) \left( \frac{1}{\tau_{dc} + \frac{P_1}{R_{cab1}} + \frac{P_2}{R_{cab2}}} \right) \quad (3-11)
\]
Herein, arcing during plug out can be simulated for either loads by input of arc length and current dependent resistance \([18,19]\) \(R_{\text{arc}1}\) and \(R_{\text{arc}2}\) respectively based on the model presented in Appendix A.

The arc modelling parameter \(P_1\) and \(P_2\) for load cable 1 and 2 respectively is ‘1’ when the corresponding cable contact to common coupling point is arcing and/or the load is attached to the circuit. It is set to ‘0’ when arc is extinguished, computed when \(R_{\text{arc}} > 100 \, \text{k} \Omega\) and arc current < \(1 \times 10^{-6}\) A. This is necessary because computed arc resistance is inversely proportional to the arc current and goes to infinity at current zero. Further, after load disconnection, the corresponding network equations change, which is also incorporated through this modelling parameter.

The application of arc detection algorithm for the scenario in which the first load is plugged out is shown in Figure 3-3. The slow LPF time constant is set at 0.001 s and that of fast is 0.0001 s. The threshold detection voltage is at 10 V. It can be observed that voltage drop is detected at Load 1 within 1 ms and the current is ramped to zero within 8 ms at the rate of -0.7 A/ms. The Load 2 continues running as no significant voltage fluctuation occurs across its input capacitor \(C_2\). Hence, a localized arc detection and clearing action is achieved and selectivity is given.
3-3 Discrete Band Pass Filter Design

In order to be selective in detecting the measured voltage drop at the input load side capacitor, it is necessary to design an appropriate band pass filter with the following criteria in mind:

- Insensitivity to low frequency fluctuations (below 150 Hz) in the grid side voltage [15, 16].
- Insensitivity to high frequency ripple (above 10 kHz) primarily due to load side switching.
- Impact of the grid inductance and load side capacitance magnitude on the behaviour of the detection algorithm.
- Threshold voltage value determines the detection time. High value may render the algorithm insensitive to arcing while low values can result in spurious triggering.

In this section, all the above design considerations are looked into and appropriate values of slow and fast low pass filter time constants, threshold voltages and behaviour of algorithm for the selected design parameters in varying network configurations is studied.

3-3-1 Time Domain Simulations for Different Time Constants

Figure 3-4 shows the simulated time domain behaviour of detection voltage at the output of the discrete band pass filter with varying slow and fast low pass time constants for the network model presented in Figure 3-2.

![Figure 3-4: Simulated ∆V at filter output with different slow and fast low pass time constants.](image)

The following can be observed:
• With very low slow LPF time constant of 0.4 s, the filter output does not reach steady state before arcing is initiated. This can make the algorithm insensitive to arcing occurring just when the loads are connected.

• With decreasing slow LPF time constant,
  – Attenuation in the detection voltage increases
  – Detection time increases

For the sensitivity of the detection scheme, the slow LPF time constant must be higher. However, in order to obtain resistance to low frequency grid side voltage fluctuations, it is necessary to decrease it.

• With decreasing fast LPF time constant,
  – Attenuation of high frequency components decreases.
  – Detection time decreases.

The constraint on this time constant is the need to eliminate high frequency noise due to switching at load side and also the slow LPF behaviour of the Resistor Inductor Capacitor (RLC)-network dependent on the grid side inductance and the load side capacitance as described in Section 3-3-3.

3-3-2 Effect of Cascading

The band pass filter action obtain till this point was from the difference of two first order low pass filters. By cascading two low pass filters, a sharper attenuation can be obtained after the cut-off frequency, as shown in the bode plot for a 3 Hz LPF in Figure 3-5.

![Bode Magnitude Plot for LPF with τ = 0.05 s](image)

**Figure 3-5:** Bode plot for low pass filter - effect of cascading.
The bode plot for the discrete band pass filter obtained by different cascading combinations of slow LPF and high LPF is shown in Figure (3-6) for bandpass of 3Hz-150Hz. Cascading the slow LPF decreases the attenuation of low frequency components, which is not desirable while cascading the fast LPF increases the attenuation of high frequency component, which is desirable. While the bandpass for 3Hz-150Hz offers a stronger detection signal, it is not resistant to low frequency fluctuations in the grid voltage, that may lead to spurious triggering.

The bode plot for the discrete band pass filter obtained by different cascading combinations of slow LPF and high LPF is shown in Figure (3-7) for bandpass of 150Hz-1.5kHz.

**Figure 3-6:** Bode plot for discrete band pass filter between frequencies of 3 Hz and 150 Hz.

**Figure 3-7:** Bode plot for discrete band pass filter between frequencies of 150 Hz and 1.5 kHz.

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If only the fast LPF is cascaded, we get a sharper attenuation for higher frequencies and good attenuation below 150 Hz, which is desirable. The pass band itself is slightly attenuated and hence, threshold voltage value must be set accordingly to get a faster arc detection.

### 3-3-3 Impact of Grid Side Inductance and Load Side Capacitor

A series resistance-inductance-capacitance (R-L-C) circuit acts as a low pass filter for the load side voltage across the capacitor. The grid inductance and load side capacitance values have impact on both attenuation of the load side voltage magnitude and the time it takes to reach the detection threshold when a 'step' in the input occurs, which has implications on the detection time and possible set values of threshold voltage value of the algorithm. Furthermore, the high frequency components of the arcing step are bypassed, which must be known to determine the effective value of fast LPF time constant.

### Frequency Domain Study

It is necessary to determine the attenuation in the load voltage magnitude for the frequency spectrum in order to find adequate time constants for the discrete band pass filter used in the arc detection algorithm. The cut-off voltage and magnitude response depend on the natural frequency \( f_0 = \frac{1}{2\pi \sqrt{LC}} \) and the damping factor \( \alpha = \frac{R}{2L} \) which are shown in Figure 3-8 and Figure 3-9.

![Figure 3-8: Natural frequency for different grid inductance and load side input capacitance values.](image)

- Capacitance= 10 µF
- Capacitance= 22 µF
- Capacitance= 47 µF
- Capacitance= 100 µF
- Capacitance= 215 µF
- Capacitance= 464 µF
- Capacitance= 1000 µF
The magnitude response of the load side voltage ($V_c$) to input voltage ($V_i$) is given by (3-12). Herein, the frequency of input is $\omega = 2\pi f$, natural frequency is $\omega_0 = 2\pi f_0$ and the quality factor $Q$ is given by $\frac{\omega_0}{2\alpha}$.

$$\frac{|V_c|}{|V_i|} = \frac{1}{\sqrt{\left(1 - \left(\frac{\omega}{\omega_0}\right)^2\right)^2 + \left(\frac{\omega}{Q\omega_0}\right)^2}} \quad (3-12)$$

The magnitude response of the load side voltage ($V_c$) with varying inductances and capacitances is shown in Figure 3-10.
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Figure 3-11: Time domain response of load side voltage to minus 13.3 V step in input for different grid inductance and input capacitance values.

**Grid Inductance=47 µH, Resistance=0.125 Ω**

**Grid Inductance=100 µH, Resistance=0.25 Ω**

**Grid Inductance=216 µH, Resistance=0.5 Ω**

**Grid Inductance=465 µH, Resistance=1 Ω**

**Grid Inductance=1000 µH, Resistance=2 Ω**
**Figure 3-12:** Discrete Filter Output for minus 13.3 V step in input for different grid inductance and input capacitance values.
The x-axis is in normalized frequency \( \frac{\omega}{\omega_0} \) such that the behaviour at a certain frequency for a particular ’L’ and ’C’ value can be determined by finding the natural frequency from Figure 3-8. The magnitude response is also dependant on the Q factor which takes into account damping and can be mapped to the circuit parameters R, L and C values using Figure 3-8 and Figure 3-9.

It can be observed that above the natural frequency, the magnitude gets attenuated and the step response to an event such as arcing will contain the frequency spectrum which is below this value. It is also worth noting that with lower Q factor corresponding to higher damping resistance, attenuation is also observed for frequencies below the cut off point.

**Time Domain Response**

Time domain response is important to determine the time it takes to detect the drop in load-side voltage. This has implications on how fast an arc can be cleared and the threshold value of the detection voltage to be set. Figure 3-11 shows the load side voltage response to a minus 13.3 V step in the input voltage (corresponding to initial electrode dependent arc voltage [17] for different grid inductances and input capacitance values. In the simulations, resistance values are taken proportional to the length of a 12 gauge wire, for the corresponding inductance value [22,23]. Figure 3-12 shows the corresponding discrete bandpass filter output with slow LPF time constant at 1 ms and fast LPF time constant at 0.1 ms. The following can be observed:

- With increasing inductance and resistance for the same capacitance, the quality factor \( Q = \frac{1}{R\sqrt{LC}} \) decreases due to the dominant increase in resistance to which it is inversely proportional against a direct square proportionality to inductance.
  - The peak voltage swing and the maximum voltage at the filter output decreases, indicating that successful detection can be achieved by setting the threshold voltage to a lower limit for higher inductances.
  - Detection time increases for the same threshold voltage level.

- With increasing capacitance for the same resistance and inductance, 
  - Peak voltage swing and the maximum voltage at the filter output decreases, indicating that successful detection can be achieved by setting the threshold voltage to a lower limit for higher capacitances.
  - Detection time increases for the same threshold voltage.

Hence, with changes in R, L and C, the detectable threshold increases with increasing quality factor. As the product of inductance and capacitance increases, the natural frequency decreases, which implies a greater detection time for the same threshold voltage level. Hence, faster arc detection can be achieved for the same threshold voltage if the product LC is smaller.

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While the above theory offers an intuitive understanding about variation in the threshold voltage and detection time based on the circuit parameters, in order to quantify the precise boundaries, a more rigorous approach is needed. Furthermore, in above simulations the variation in resistance is ‘pinned’ to be directly proportional to the variation in the grid inductance. A more generic selection scheme, allowing all three circuit parameters (R, L and C) to vary independently, is necessary. Figure 3-13 shows the maximum voltage at the 150 Hz - 1.5 kHz discrete bandpass filter output for varying quality factor and natural frequencies for a voltage step of minus 13.3 V corresponding to the electrode dependent voltage drop at arc initiation [17]. Herein, the quality factor and natural frequency can be mapped back to the circuit parameters R, L and C using Figure 3-8 and Figure 3-9.

It can be observed that, with increase in quality factor \( Q = \frac{1}{R \sqrt{L/C}} \), the maximum voltage computed at the output of discrete bandpass filter increases when the natural frequency is close to the frequency bandwidth of the filter. This is because a quality factor greater than 1 amplifies the frequency components of the step in the voltage around the natural frequency as depicted in Figure 3-10. Hence, when the natural frequency falls within the bandpass frequencies, this amplification passes through to the output. However, at other places of the frequency spectrum, the amplification in signal due to high quality factor occurs only for frequency components that lie outside the specified bandwidth, which are attenuated.

Without this amplification of the step input for frequency components about the natural frequency corresponding to the designed bandwidth of the filter, the maximum voltage is stable at a value between 7.5 to 8 V, independent of both natural frequency and the quality factor of the circuit. In other words, this voltage corresponds to the signal available for

---

3-3 Discrete Band Pass Filter Design

Figure 3-13: Maximum voltage at discrete filter output with varying circuit quality factor and natural frequency.
detection regardless of the circuit parameters R, L and C.

Figure 3-14 shows the detection time for minus 13.3V step in input for different threshold voltages with filter bandwidth of 150 Hz-1.5 kHz. The black regions show the simulation points where no arc can be detected for the corresponding set threshold value. Herein, the quality factor was varied from 0.25 to 10 in steps of 0.25 and frequency was varied from 100 Hz to 10 kHz in steps of 100 Hz.

Note how the shape of the detection boundary resembles the bode plot for the discrete bandpass filter used shown in Figure 3-7 about the frequency spectrum for higher set threshold detection voltage. Following can be observed:

- The detection time decreases with increasing natural frequency until it saturates to a low value towards the outer limit of the filter band.

- At very low natural frequency, there is no detection for any quality factor or set threshold voltage because the circuit attenuates the higher frequencies where the filter is sensitive.

- For very low quality factor (much less than 1), there is no detection when the natural frequency is within the range of filter bandwidth due to the high damping effect depicted in Figure 3-10. For very high frequencies, this damping effect is pushed outside the frequency spectrum to which the bandpass filter is sensitive, while the step signal components in the frequency spectrum for detection is not affected.

- With higher set detection threshold voltage, the detection boundary confines around the natural frequencies corresponding to the filter bandpass. Threshold voltages of 8 V, 9 V and 10 V are detected in this region due to the amplifying effect of a quality factor greater than unity. In other words, the boundaries for these thresholds are a result of interaction of filter attenuation and the amplification/damping of the specific frequency components of the step input about the natural frequency based on the quality factor.

- Threshold voltage of 7 V is detectable for a wide range of frequency spectrum and quality factors. This is because the signal components of 13.3 V step within the frequency spectrum of the bandpass filter add up to a value greater than 7 V. In other words, amplifying effect of quality factor greater than unity is not needed to reach the threshold and also there is some margin to accommodate damping when the quality factor is below unity. For natural frequencies higher than the spectrum of the filter, the quality factor anyway plays no role in damping or amplifying the signal components.

Hence, threshold voltage of 7 V is the most favourable to ensure arc detection for varying grid inductances and load side capacitances. Making the detection sensitive when the natural frequency is below 150 Hz is not possible, because we want to avoid spurious triggering due to grid side voltage fluctuations at this frequency.

Insensitivity to arc detection when quality factor is very low and the natural frequency lies with the frequency spectrum of filter can be avoided by setting the threshold voltage lower than 7 V. However, this decision must be taken after careful consideration to avoid spurious triggering due to noise in the system.
Figure 3-14: Detection time for minus 13.3 V step in input with varying circuit quality factor and natural frequency.
4-1 Off-line Validation of Proposed Arc Detection Method

In order to validate the proposed arc algorithm, arcs were created on the experimental setup and the measurement data for the load side capacitor voltage was run through the developed algorithm. The first results of this study pertaining to off-line arc detection for a stable supply are described in the publication attached in Appendix A. In this section, off-line study for arcing experiments with noisy supply is carried out. The obfuscation of detection signal due to noise frequencies and associated amplitude is studied and possible solutions by notching out these frequencies are explored.

4-1-1 Experimental Setup

Figure 4-1 shows the equivalent circuit for the experimental setup used.

![Figure 4-1: Equivalent circuit for the experimental setup used.](image)
Herein, the inductance $L_{\text{cable}}$ of 100 $\mu$H is introduced in the circuit and the load capacitor $C_{\text{load}}$ used is of 30 $\mu$F. A constant resistance load is attached and a series arc is generated which introduces a variable resistance $R_{\text{arc}}$ in the circuit. The experimental setup was prepared as shown in Figure 4-2.

![Figure 4-2: Experimental setup for series electric arcing study.](image)

The arc current is measured at (a) and it goes via $L_{\text{cable}}$ (b) through the arc generator (c). The capacitor (d) is connected to the constant resistance load (e). Arc current, source voltage and load side voltage are measured by the oscilloscope (f). A series of experiments were performed in the company ‘Direct Current BV, The Netherlands’. A typical computation on measured load capacitor voltage data during arcing scenario with a noisy supply is shown in Figure 4-3.

Herein, the filter has a band-pass of 3-150 Hz is able to attenuate the 300 Hz noise in the supply and give a clear detection of arcing. However, this filter does not have immunity to the low frequency fluctuations in the grid voltage, as depicted in bode plot of Figure 3-6.

Also noteworthy is that when only fast LPF is cascaded or when both slow and fast LPF...
are cascaded, the ripple is lower owing to a sharper attenuation at the high frequency side. While we get greater attenuation in the signal of interest when cascading only fast LPF as compared to cascading both fast and slow LPF, the fact that cascading only fast LPF has greater immunity to low frequencies makes it a preferred choice.

In dc micro-grids, grid side voltage fluctuations must be limited below 100 Hz from stability and protection point of view [1,15]. The 300 Hz noise in this particular supply obfuscates the detection signal when designed bandpass of 150 Hz - 1.5 kHz is used as shown in Figure 4-4 and hence a notch filter must be added to stamp out the noise frequency component in order to get good detection and avoid spurious triggering. Further, the filter time constants are so set that complete possible frequency spectrum from 100 Hz - 10 kHz is passed. The computed voltage output of this discrete band pass filter cascaded with the 300 Hz notch filter for...
measured data during arcing is able to distinguish the arcing instant as shown in the figure.

![Designed Filter with Bandwidth 150 Hz to 1.5 kHz without 300 Hz Notch](image1)

![Designed Filter with Bandwidth 100 Hz to 10 kHz with 300 Hz Notch](image2)

**Figure 4-4:** Off-line computed discrete band pass filter (100Hz-10kHz) output with 300 Hz notch filter for measurement data of a typical arcing scenario with noisy supply.

Hence, the offline study in this section depicts the vulnerability of the detection algorithm to a supply with noise in the frequency spectrum of interest and a way to circumvent this issue by cascading the bandpass filter with notch filters for those noise frequencies.

### 4-2 Real Time Arc Detection Experiments

As final thread towards validating the proposed arc detection scheme, experiments were designed to create arcs and run the algorithm for obtaining real time detection. The experi-
mental setup for real time arc detection is shown in Figure 4-5.

![Experimental setup for real time arc detection experiments.](image)

**Figure 4-5:** Experimental setup for real time arc detection experiments.

A switch controls the arc generating relay (a) that supplies voltage to a constant resistance load paralleled with a 30 µF capacitor (b). The load voltage is fed via a 1000 V/3.3 V voltage divider (c) to the Pin ‘ADCINA0’ of the analog to digital converter of the micro-controller LAUNCHXL-F28027 C2000 Piccolo LaunchPad Experimenter Kit [24](d). The algorithm used is a discrete band pass filter to let through frequencies between 150 Hz-1500 Hz as a difference of a slow low pass filter and a cascaded fast low pass filter of respective time constants. The programming was done in MATLAB and burned to the controller using code composer software. When output of this filter is greater than the set threshold value, a trigger signal is provided to the output pin ‘GPIO3’ which triggers the oscilloscope. This trigger can be used to shut down the load.

A series of experiments with real time arc detection with varying threshold detection voltages were performed on 100 V and 400 V supplies; results are plotted in Figure 4-6 and Figure 4-7 respectively. As observed, the detection trigger from output pin ‘GPIO3’ from C2000 goes high soon after the arc is initiated in the experimental setup.

It must be noted that different power supplies were used to create 100 V and 400 V in the two sets of experiments. The transient behaviour of these supplies is different as can be observed from the load voltage waveforms during arcing. Hence, correlation in results should be drawn only for the sets conducted for the same supply voltage level.

For the set of experiments conducted with the same power supply, as the threshold voltage detection value is increased from 6 V to 9 V, the trigger time after arc initiation increases. The pitch of the trigger signal decreases with increasing threshold value, indicating the time for which the signal remains above the threshold value. The figures highlight the detection time and the signal pitch for all experiments depicted.
Figure 4-6: Real time arc detection for a 100 V supply with 5 A load current.
Figure 4-7: Real time arc detection for a 400 V supply with 2.5 A load current.
In this part of the thesis, a novel way has been proposed for detecting arcing from the load side during plug out. It is first theoretically proved through simulations that the detection algorithm is capable of extinguishing the arc by detecting the initial electrode dependent voltage drop at the load side capacitor. The simulations display selectivity in disconnecting only the load at which arcing is occurring and other parallel loads keep running.

Next, the discrete band pass filter is designed to have a pass frequency bandwidth for rapid arc detection at set threshold but are insensitive to the grid voltage fluctuations of below 150 Hz to avoid spurious triggering. Further, the impact of grid inductance, resistance and the load side capacitance on detection voltage at the designed filter is studied. The threshold voltage is selected to ensure that these parameters have minimal to no impact on the correct triggering in the detection scheme. Towards this purpose, the dependence of the threshold voltage and the detection time on the circuit parameters is exhaustively described.

Finally, a series of experiments are conducted to validate the proposed detection algorithm. First, arcs are generated in a developed experimental setup and the measured data is run through different detection algorithm settings off-line. Then, a micro-controller is programmed to take the load side capacitor voltage as input and send a trigger upon arc detection in real time. The set point of threshold voltage is varied to see the real time sensitivity and detection time of the arc detection algorithm for 100 V and 400 V supplies.

In future, the following studies can move this detection scheme towards becoming a market ready mature technology:

- Real time experimental study should be conducted to depict the selectivity and localized action in more complicated parallel load systems. The circuit schematic in Figure 5-1 is proposed for experimental study of the response of the detection algorithm in real time for arc generation in location (1), (2) and (3).
Conclusion and Future Work

- A robust insensitivity of the designed bandpass filter to grid side voltage fluctuations should be depicted experimentally.

- A more sophisticated bandpass filter can be implemented and time constants can accordingly be tuned. Figure 5-2 shows the bode plots for the filter used in this thesis (bandpass 1, blue, $\tau_{slpf} = 1\, ms$, $\tau_{flpf} = 0.1\, ms$), filter with difference of slow and fast LPF cascaded with itself (bandpass 2, red, $\tau_{slpf} = 1\, ms$, $\tau_{flpf} = 0.1\, ms$) and filter with both slow and fast LPF cascaded and then the difference of this entire unit cascaded with itself (bandpass 3, green, $\tau_{slpf} = 0.5\, ms$, $\tau_{flpf} = 0.1\, ms$).

Such permutations and combinations should be studied in terms of price and computational time for choice of the best possible option.

- Notch filters can be designed for expected noise frequencies in the grid at 100 Hz, 120 Hz, 300 Hz and 360 Hz in order to avoid spurious triggering.

- Proper coordination with central grid side arc detection from frequency signature of arcs should be defined to offer secondary protection and enable differentiation between series and parallel arc.

Figure 5-1: Circuit schematic for future arc detection experiments.

Figure 5-2: Sophisticated bandpass filter design.
Part II

Bus Transfer Switching with HVDC
GIS Disconnector
High voltage dc technology is a cost effective, high efficiency solution to issues related to reactive power over ac transmission of energy. With no limitations on line length [25], point to point HVDC energy transmission is finding applications in long distance, transcontinental large scale solar and offshore wind projects [26,27]. Researchers recognize that the evolution of an interconnected multi-terminal HVDC network, ensuring that outage of power in one section does not interrupt power to any terminal of the system, is possible only with the sophistication of circuit breakers, disconnectors and grid infrastructure capable of directing and controlling the dc power flow as per requirements [2,28].

A specific application area is facilitating bus transfers in multiple parallel bus bars in a highly interconnected substation [29]. Utilizing disconnector switches Disconnector Switch (DS) for this purpose instead of circuit breaker can reduce the size and cost of the gas insulated switchgear Gas insulated Switchgear (GIS). This is possible because during bus transfer operation, the voltage that falls across the switch after disconnection is much smaller as opposed to the full rated voltage that usually needs to be isolated.

A typical current flow depiction before, during and after the bus transfer in two parallel buses is shown in Figure 6-1. The commutation of current from bus one (green) to bus two (red) is facilitated by first making DS2 and then breaking DS1. In the process, the voltage that appears across DS1 after breaking is the voltage drop across the parallel path (red) due to the resistance and inductance.

In a substation with many such parallel buses interconnected with each other, variation in lengths of each parallel path can introduce different resistance and inductance combinations which has implications on the ability of disconnector to successfully implement the bus transfer. It hence becomes essential to know the operating conditions in terms of length of each
bus in the parallel path, recovery voltage, burn time and current magnitude for which we safely expect the DS to work.

![Diagram](image_url)

**Figure 6-1:** Bus transfer process using disconnector switches at a typical substation with parallel buses feeding two feeders via bus-couplers.

Figure 6-2 shows the equivalent circuit diagram representing the network in Figure 6-1.

![Diagram](image_url)

**Figure 6-2:** Equivalent Circuit Diagram for Bus Transfer Process.

Current $I_2$ from bus two with inductance $L_2$ and resistance $R_2$ is commuted to bus one with inductance $L_1$ and resistance $R_1$ when the disconnector switch opens. When the switch is closed, the total current $I_{tot}$ is shared between the two buses and the voltage across the switch, $V_{DS}$ is negligible. After successful opening, it will be equal to the bus voltage $V_{bus}$ that depends on the length dependent resistance and inductance of bus one.

Before the current $I_2$ reaches zero, arcing between the contacts of the DS occurs. The time of first zero crossing is dependent on the loop formed by the two buses and has implications on input arc energy and first arc burn time. Upon arc extinction, the recovery voltage that appears across the GIS DS electrodes is crucial in ascertaining whether re-strike will occur or
not [28–30]. Due to lack of research in this area for dc systems, the focus of this thesis is in developing experimental direction to collect and analyse data for the capability limits under which the HVDC GIS disconnector operates and can facilitate successful bus transfer. The standards for ac disconnectors for rated voltage levels upto 1200 kV presented in IEC 62271-102 are taken as starting points for development of their counterparts in dc context [28].

The flow diagram depicting the research methodology used in this part of the thesis is shown in Figure 6-3.

![Flow diagram](image)

**Figure 6-3:** Research process used in this study.

Chapter 7 describes the experimental setup used in the study. A simulation model is prepared using the state space equations describing the physics of the system and the control strategy used.

Chapter 8 presents the parameter estimation methodology used for finding the unknown inductances and resistance of the complete system. Of particular importance is the inductance of the GIS disconnector switch across which a voltage drop occurs, which must be analytically removed to obtain the arc voltage. Other parameters are essential for computation of recovery and re-ignition voltages during bus transfer. Graphical user interface developed for this purpose is also described.

In Chapter 9, the parameter estimation methodology and the simulation model developed is validated by comparing the simulations with measured data from experimental setup under similar conditions. Sources of errors are identified and justified.

Recovery voltage and re-ignition voltages which are crucial in determining the operable limits of GIS DS during bus transfer are defined and their analytical expression is derived in Chapter 10. Due to noise and re-ignition, these are not directly measurable. The analytical expression provide a way to estimate these from the system space variables that do not change suddenly. Using the simulation model and possible configurable circuit parameter values, behaviour of the experimental setup is studied.

Finally, Chapter 11 describes the tools developed for analysing the measurement series and presents the results of typical experiments conducted.
Chapter 7

Experimental Setup

In this chapter the experimental setup used is described. Subsequently, a simulation model is prepared based on the state space equations along with the control strategy.

7-1 Hardware Description

7-1-1 DC Source Room

Figure 7-1 shows the source room from which the dc power is supplied.

![Figure 7-1: DC power supply system for the experimental setup.](image)
There are three high voltage buck converters of current rating 1 kA connected in parallel to supply 0-3 kA controlled current to the experimental bay. Each converter has individually controlled operating phase and output current. Peak current control strategy is used to control the IGBT switches with an operating frequency variable upto 10 kHz. A detailed theory underlining the development of this supply system is given in [32].

The output inductance (A), (B) and (C) of each converter can be varied by changing taps from 0-9 upto an inductance of 1.5 mH to achieve a current gradient upto 150 A/µs. Further, an external inductance (G) can be added to extend the inductance value to 5.5 mH. The three input capacitors (D), (E) and (F) of nameplate capacitance of 2 mF each, also connected in parallel with each other, can be charged upto a voltage level of 3 kV. Discharge resistance (H) discharges the input capacitor as soon as the safety circuit kicks in.

7-1-2 Experimental Bay

A controlled current is supplied to the experimental setup via a main copper bus and series external resistance. Figure 7-2 depicts the experimental setup used in the study.

The system consists of two parallel buses along with GIS DS on bus number two to emulate the system shown in Figure 6-1. The inductance associated with length of the bus is varied using taps from 0-15 on the two inductor coils shown in the figure. The inductance and resistance values are adjusted corresponding to typical GIS substation bus lengths [31] between 10 m to 600 m. Double wires can be used to reduce the resistance of the inductor coils, if required.

7-1-3 HVDC GIS Disconnector

A 5.62 bar SF₆ GIS disconnector [33] of type ELK-3 for upto 420 kV is installed in series with bus two inductor coil to facilitate high dc current bus transfer. This product is provided by ABB to ETH, Zurich for experimental purposes. Due to confidentiality agreements, sharing the specifications of this product is beyond the scope of this document. The switchgear is indicated in the top-view of the experimental bay in Figure 7-2.

7-1-4 Event Sequence and Trigger Timing

The experiment is controlled from the control room through serial communication. The contact separation of the GIS DS is initiated by the motor controller which is activated by the operator. Finite time before the motor is about to open, an automatic trigger is sent to the IGBT controller which then begins supply of a controlled current after a pre-set delay and triggers the oscilloscopes to log the measurements.

Since the input capacitors can supply sustained energy only for about 20-60 ms before discharging, in order to ‘catch’ the arcing event it is essential to set the pre-set IGBT switching delay to take into account the time it takes for the DS contacts to actually begin separating (and therefore arc initiation) after the motor tells that it is about to separate.

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Figure 7-2: Experimental setup for bus transfer measurements.
7-2 Simulation Model for Setup

7-2-1 Equivalent Circuit

The circuit diagram based on the experimental setup [31, 32] to study dc arcing for bus transfer with GIS disconnector is shown in Figure 7-3.

![Circuit Diagram](image)

**Figure 7-3**: Circuit diagram based on the experimental setup

The circuit parameters for the experimental setup are listed in Table 7-1.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Switching Frequency</td>
<td>0-10.0 kHz</td>
</tr>
<tr>
<td>Buck Input Capacitance ($C_{nn}$)</td>
<td>2.0 mF</td>
</tr>
<tr>
<td>Buck Output Inductance ($L_{nn}$)</td>
<td>0.1-1.5 mH</td>
</tr>
<tr>
<td>Number of Buck Converters in Parallel</td>
<td>3</td>
</tr>
<tr>
<td>Main Bus Inductance (measured) ($L_m$)</td>
<td>12 $\mu$H</td>
</tr>
<tr>
<td>Main Bus Resistance (measured) ($R_m$)</td>
<td>466.3 m$\Omega$</td>
</tr>
<tr>
<td>Bus 1 Inductance ($L_1$)</td>
<td>10-160 $\mu$H</td>
</tr>
<tr>
<td>Bus 1 Resistance ($R_1$)</td>
<td>Measured for each tap separately</td>
</tr>
<tr>
<td>Bus 2 Inductance ($L_2$)</td>
<td>10-160 $\mu$H</td>
</tr>
<tr>
<td>Bus 2 Resistance ($R_2$)</td>
<td>Measured for each tap separately</td>
</tr>
<tr>
<td>Capacitor Voltage ($V_C(0)$)</td>
<td>0-3.0 kV</td>
</tr>
<tr>
<td>Initial Source Current ($I_{tot}(0)$)</td>
<td>0.0 A</td>
</tr>
<tr>
<td>Initial Bus 1 Current ($I_1(0)$)</td>
<td>0.0 A</td>
</tr>
<tr>
<td>Initial Bus 2 Current ($I_2(0)$)</td>
<td>0.0 A</td>
</tr>
</tbody>
</table>

Table 7-1: Parameter Values for dc Equivalent Circuit
7-2.2 State Space Equations

The switching pulse parameter $P_n$ for nth buck converter is defined such that,

$$P_n = \begin{cases} 1 & \text{if switch is closed} \\ 0 & \text{if switch is open} \end{cases} \quad (7-1)$$

$$P_n = \begin{cases} 1 & \text{if switch is closed} \\ 0 & \text{if switch is open} \end{cases} \quad (7-2)$$

The state space equations used to develop the simulation model are (7-3)-(7-7)

\[
\begin{align*}
\frac{dV_C}{dt} &= \frac{-1}{\sum_{n=1}^{3} C_{nn}} \left( \sum_{n=1}^{3} P_n I_{bn} \right) \quad (7-3) \\
\frac{dI_{in}}{dt} &= \begin{cases} 0, & \text{if } I_{bn} = 0 \text{ & } P_n = 0 \\ \frac{V_C - V_{out} - R_{nn} I_{bn}}{L_{nn}}, & \text{otherwise} \end{cases} \quad (7-4) \\
\frac{dI_{tot}}{dt} &= \frac{V_{out} - V_{bus} - R_{m} I_{tot}}{L_{m}} \quad (7-5) \\
\frac{dI_1}{dt} &= \frac{V_{bus} - R_1 I_1}{L_1} \quad (7-6) \\
\frac{dI_2}{dt} &= \frac{V_{bus} - R_2 I_2 - V_{DS}}{L_2} \quad (7-7)
\end{align*}
\]

Where,

- $V_C$ is the input capacitor voltage
- $I_{in}$ is the current through output inductance $L_{nn}$ of nth buck converter
- $V_{out}$ is the output voltage at the parallel connection of buck converter

All other terms are indicated in Figure 7-3 and defined earlier. Herein, the space variables are $V_C$, $I_{in}$, $I_{tot}$, $I_1$ and $I_2$. The intermediate terms $V_{out}$ and $V_{bus}$ must be represented in terms of the space variables. The circuit time constants are defined as $\tau_{nn} = \frac{L_{nn}}{R_{nn}}$, $\tau_m = \frac{L_m}{R_m}$, $\tau_1 = \frac{L_1}{R_1}$ and $\tau_2 = \frac{L_2}{R_2}$. In order to represent the derived expressions concisely, we define $\frac{1}{L_{tot}} = \frac{1}{L_{in}} + \frac{1}{L_{out}}$ (corresponding change in $L_{in}$ and $L_{out}$ based on the non-zero current flow through component inductances is incorporated in the model). From Kirchoff’s law, it follows that,

$$\frac{dI_{tot}}{dt} = \sum_{n=1}^{3} \frac{dI_{bn}}{dt} \quad (7-8)$$

Substituting (7-4) in (7-8) for $I_{bn} > 0$,

$$\frac{dI_{tot}}{dt} = V_C \sum_{n=1}^{3} \left( \frac{P_n}{L_{nn}} \right) - \frac{V_{out}}{L_{in}} - \sum_{n=1}^{3} \left( \frac{I_{bn}}{\tau_{nn}} \right) \quad (7-9)$$

Substituting (7-5) in (7-9) and rearranging,

$$V_{out} = \left( \frac{\sum_{n=1}^{3} P_n}{L_{nn}} \right) V_C - \sum_{n=1}^{3} \left( \frac{I_{bn}}{\tau_{nn}} \right) + \frac{I_{tot}}{\tau_m} + \frac{V_{bus}}{L_m} \quad (7-10)$$

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Similarly,

$$\frac{dI_{\text{tot}}}{dt} = \frac{dI_1}{dt} + \frac{dI_2}{dt}$$  \hspace{1cm} (7-11)$$

Substituting 7-5, (7-6) and (7-7) in (7-11) and rearranging,

$$\frac{V_{\text{out}}}{L_m} = V_{\text{bus}} \left( \frac{1}{L_m} + \frac{1}{L_{\text{out}}} \right) + \frac{I_{\text{tot}}}{\tau_m} - \frac{I_1}{\tau_1} - \frac{I_2}{\tau_2} - \frac{V_{\text{DS}}}{L_2}$$  \hspace{1cm} (7-12)$$

Substituting $V_{\text{out}}$ from (7-10) in (7-12),

$$\left( \sum_{n=1}^{3} P_n \frac{L_n}{L_{\text{in}}} \right) \frac{V_C - \sum_{n=1}^{3} \left( \frac{I_{n}}{\tau_n} \right) + \frac{I_{\text{tot}}}{\tau_m} + \frac{V_{\text{bus}}}{L_m} }{L_m \left( \frac{1}{L_{\text{in}}} + \frac{1}{L_m} \right)} = V_{\text{bus}} \left( \frac{1}{L_m} + \frac{1}{L_{\text{out}}} \right) + \frac{I_{\text{tot}}}{\tau_m} - \frac{I_1}{\tau_1} - \frac{I_2}{\tau_2} - \frac{V_{\text{DS}}}{L_2}$$  \hspace{1cm} (7-13)$$

Solving for $V_{\text{bus}}$,

$$V_{\text{bus}} = \left( \sum_{n=1}^{3} P_n \frac{L_n}{L_{\text{in}}} \right) \frac{V_C - \sum_{n=1}^{3} \left( \frac{I_{n}}{\tau_n} \right) + \frac{I_{\text{tot}}}{\tau_m} + \sum_{n=1}^{3} \left( \frac{I_{n}}{\tau_m} \right) }{1/L_m - L_m \left( \frac{1}{L_{\text{in}}} + \frac{1}{L_m} \right) \left( \frac{1}{L_{\text{in}}} + \frac{1}{L_m} \right)}$$  \hspace{1cm} (7-14)$$

Hence, $V_{\text{out}}$ and $V_{\text{bus}}$ can be computed in terms of space variables using expressions (7-10) and (7-14) respectively. The variable $V_{\text{ds}}$ provides the measured drop across the disconnector switch and it is given by (7-15),

$$V_{\text{ds}} = L_{\text{ds}} \frac{dI_2}{dt} + R_{\text{ds}} I_2 + U_{\text{arc}}$$  \hspace{1cm} (7-15)$$

Here, $U_{\text{arc}}$ models the arc as a voltage source with polarity depending on the bus two current $I_2$. The voltage probes in the experimental setup are such that there is a non-zero inductance $L_{\text{ds}}$ and resistance $R_{\text{ds}}$ between them, which must be estimated and their effects subtracted from $V_{\text{ds}}$ for precise analysis of electrical characteristics of the arc.

Since the dc source is designed as an arbitrary current source, a control strategy for the three module currents $I_{b1}$, $I_{b2}$ and $I_{b3}$ is implemented in hardware in the IGBT controller unit. The control strategy relies on measuring the momentary values of these currents and determines the points in time when IGBTs $S_1$, $S_2$ and $S_3$ are switched on or off individually.

### 7-2-3 Current Control Strategy

Predictive current control [34] offers an elegant way of controlling the IGBT switching to operate the buck converter as a current source. The governing equations for computing the duty cycle are derived in Appendix C. The ability of this control strategy to 'look into' the future as against the responsive strategies is an added advantage. However, the precise value of output inductance is required for accurate duty cycle computation. Since our experimental setup uses variable inductances through tap changes, the peak control strategy is used due to its simplicity, as described below.
Peak Current Control

To protect sensitive equipment from overcurrents and to guarantee fast response times of the IGBT controller, the control strategy currently implemented is a peak current control scheme. Analog comparators continuously relate the measured current and the set current for each of the three modules. Switching on of a switch $S_i$ occurs if at a set point in time the measured current is below the set current. This time point is determined by the switching period $\tau$ and phase shift $\phi_i$ which are constant over the course of an experiment run. The signal to switch off switch $S_i$ is sent at any time when the measured current is above the set current. The algorithm for peak current control strategy is shown in Figure 7-4. Only measurement of the source buck converter current ($I_{bn}$) is required to ensure that the peak current never exceeds the required value.

![Figure 7-4: Algorithm for peak current control strategy.](image)

A typical simulation result with peak current control strategy is shown in Figure 7-5. Each converter output inductance is set at 1.5 mH and operating frequency is 2 kHz and the phase shift is $0$, $T_s/3$ and $2T_s/3$ respectively. All other parameter values are set according to typical setup values and the bus one and bus two inductances are set at $80 \mu$H and $15 \mu$H respectively.

Since it is not known whether the GIS DS will be able to successfully facilitate the bus transfer and the arc will extinguish with the existing circuit configuration, the setup allows the user to preset the time for which the converters will supply current as an additional protection scheme to prevent damage to the disconnector electrodes. In this simulation, the operating time is set as 20 ms after which all three buck converters switch off.

Input capacitor voltage, operating frequency, phase shift, output inductance of all three buck converters, output current and the coil inductances of bus one and bus two are configurable so as to provide specific conditions in which we want to study the bus transfer process. After developing the parameter estimation strategy and validating the simulation model in the subsequent chapters, this will be used to decide the circuit configuration in which the experiments will be conducted to study the arcing behaviour of the disconnector under known conditions.
Figure 7-5: Simulation results with peak current control strategy.
Estimation of Circuit Parameters

The above developed system model behaviour evolves in time based on the inductances and resistances shown in Figure 7-3. In order to design setup configurations for conducting bus transfer experiments under specific conditions, precise circuit parameters governing the system behaviour must be known. It is also desired to analytically estimate the recovery and re-strike voltage (derived in Chapter 10) from the measured space variables. These, as it shall be discussed, are not measurable due to noise and arc re-strike. Further, the voltage drop against the unknown GIS DS inductance is to be analytically removed from the measured voltage across the disconnector in order to obtain the actual arc voltage.

Hence, a series of specially designed experiments have been conducted and each unknown circuit parameter has been estimated with accuracy. With taps in the coils and frequency dependence of inductances, these experiments must be redone every time there is a change in the hardware configuration or change in operating conditions. In order to make accurate estimations, the following circuit conditions are observed during analysis:

- Single source buck converter is used to minimize changes occurring in the circuit configuration during measurement. By minimizing the number of current paths and the number of controller interventions, the circuit is made simpler.

- Since the input voltage is changing (capacitor discharge), only the periods during which the current is falling are analysed. During the falling edge of the current, the buck input IGBT switch is off and the capacitor voltage is not in play, thereby eliminating the impact of this parameter during analysis.

- Low source inductance \( L_{on} \) is used to enable faster \( \frac{dI}{dt} \) through the bus inductance. This ensures a higher voltage drop across the circuit inductances which makes the analysis more accurate.
- Lower switching frequency for longer falling edges, to facilitate better curve fitting as we have more data points to work with.

For some estimations, other circuit configurations are observed, which shall be described in subsequent sections. The selected time intervals (red) for parameter estimation are shown in Figure 8-1.

![Figure 8-1](image)

**Figure 8-1**: Selected operating periods for estimation of inductances.

### 8-1 Circuit Resistances

Due to the small value of resistances, the voltage drop across them was negligible as compared to the drop across the inductances. Due to this reason, the resistances cannot be analytically estimated accurately from the measured data. Hence, all resistances were measured separately using a micro-ohmmeter. The exact values of these resistances are used as inputs for inductance estimation.

### 8-2 Inductances Estimation with Disconnector Open

In order to estimate the bus one inductance $L_1$, main bus inductance $L_m$ and source inductance $L_{nn}$, the experiment is run keeping bus two open. Figure 8-2 shows the equivalent circuit during switch off duration with GIS disconnector open. The circuit is a series R-L network with exponentially decaying current. The equivalent inductance and resistance of...
the circuit during the falling current period is given by (8-1) and (8-2) respectively.

\[ L_{\text{eq}} = L_{\text{nn}} + L_{\text{m}} + L_1 \]  
\[ R_{\text{eq}} = R_{\text{nn}} + R_{\text{m}} + R_1 \]  

**Estimation of Bus One Inductance**

\( L_1 \) is estimated from current \( I_1 \) and \( V_{\text{bus}} \). A curve fitting function is developed, which is called for the current and voltage for each selected period to determine the time dependent equations of the form shown in (8-3)-(8-5),

\[ I_1 = a_i e^{-t/\tau_i} \]  
\[ \frac{dI_1}{dt} = -a_i \frac{e^{-t/\tau_i}}{\tau_i} \]  
\[ V_{\text{bus}} = a_v e^{t/\tau_v} \]

Herein, the coefficients \( a_i \) and \( a_v \) depend on the initial current and voltage of the selected period respectively. Starting values provided to the curve fitting algorithm help the solution to converge faster and more accurately. The current is much smoother than the bus voltage due to presence of large circuit inductances. \( a_i \) is approximated as the mean of first 5 current array values. Due to high frequency oscillations in voltage due to parasitic capacitances, \( a_v \) is approximated as the mean of first 51 voltage array values. The algorithm is set to allow \( \pm 10\% \) variation in these approximate values while fitting.

The time constant \( \tau_i = \frac{L_{\text{eq}}}{R_{\text{eq}}} \) where the equivalent resistance and inductance of the circuit is given by (8-1) and (8-2) respectively. While the equivalent resistance is known with certainty, the equivalent inductance is not. An approximate starting value of inductance is input to the estimation algorithm from a look-up table mapping their theoretical values computed from the tap settings [31]. The fitting algorithm itself is allowed to vary \( \tau_i \) from 0 to minus infinity.
Estimation of Circuit Parameters

(it is negative as the current is falling). The relationship between \( I_1 \) and \( V_{bus} \) is such that the theoretical time constants must be the same. Hence, the output \( \tau_i \) of the current fitting algorithm is used as the starting value approximation of \( \tau_v \) for the voltage fitting algorithm. Since the voltage signal is noisier and certainty in the estimated \( \tau_i \) is more, the voltage fitting algorithm is allowed to vary \( \tau_v \) in the range of \( \pm 10\% \) of its approximated starting value.

Figure 8-3 and Figure 8-4 show typical fitting results (red) for current \( (I_{eq}) \) and voltage \( (V_{eq}) \) waveforms in the selected periods respectively. As observed, the fitting result closely follows the measurement data.

![Figure 8-3: Fitting for bus one current during selected periods with GIS open.](image)

![Figure 8-4: Fitting for bus voltage during selected periods with GIS open.](image)
With equations of current and voltage known, and the time differential of current given by (8-4), the array values of these parameters are found for the selected time period and fed into the inductance fitting algorithm which works based on the relationship described by (8-6). Each selected period provides an over-defined system with n data points for a linear equation for unknown inductance. As discussed, since the drop across the resistance cannot be accurately determined from the fitting algorithm, it is measured beforehand and provided as a known constant.

\[
\begin{bmatrix}
\frac{dI_1}{dt}(1) & I_1(1) \\
\frac{dI_1}{dt}(2) & I_1(2) \\
\vdots & \vdots \\
\frac{dI_1}{dt}(n) & I_1(n)
\end{bmatrix}
\begin{bmatrix}
L_1 \\
R_1
\end{bmatrix} =
\begin{bmatrix}
V_{bus}(1) \\
V_{bus}(2) \\
\vdots \\
V_{bus}(n)
\end{bmatrix}
\]

(8-6)

Figure 8-5 shows the actual measured bus voltage (red) and the estimated voltage (black) with inductance given by the fitting algorithm for each time interval. As observed, the voltage drop across the inductance (green) is by far the more dominant one as compared to that across the resistance (blue). The theoretical bus voltage estimation using the estimated inductance value and the measured resistance closely follows the measured voltage in each selected period.

**Figure 8-5:** Actual and fitted bus voltage during selected periods with GIS open.

**Estimation of Main Bus Inductance** \( L_m \)

The inductance \( L_m \) is introduced in the setup due to the geometry and the length of the main bus that connects the dc source room to the experimental bay. In order to compute the
recovery voltage, this value must be known. $L_m$ is estimated from current $I_{tot}$ and voltage $V_{out} - V_{bus}$ during the falling edge in open circuit measurement.

Plot a) of Figure 8-6 shows the computed voltage drop across the main bus (black) as compared to the measured $V_{out} - V_{bus}$ (red) in the original circuit configuration with a source inductance of 0.5 mH. It can be observed that the voltage drop across the main bus resistance $R_m$ (blue) is significant and by far dominates the drop across $L_m$ (green). This rendered the estimation algorithm inaccurate and an analysis of a series of experiments did not offer consistent results for $L_m$ in this circuit configuration.

$R_m$ consists of 2 components: the resistance of the main bus itself and an external resistance of 466 mΩ to incorporate a voltage drop across the parallel buses. It is across this external resistance that the high voltage drop is occurring. The estimation of $L_m$ is needed to be done only once, owing to the fact that unlike $L_{nn}$ and $L_1$, tap changes in source side and parallel bus side does not impact $L_m$. For this reason, the location of measuring point of $V_{out}$ is temporarily changed such that it bypasses this external resistance, such that the measured difference $V_{out} - V_{bus}$ is only due to voltage drop across $L_m$ and a negligible actual main bus resistance. Plot b) shows the fitting attempt in this scenario with 0.5 mH source inductance. While, it can be observed that the voltage drop across the resistance (blue) and inductance (green) are now comparable, they cancel each other and the actual voltage to be fitted for inductance computation is nearly zero (red).

A lower source inductance of 0.2 mH is used to ensure faster current changes and hence, high voltage drop across the main bus inductance as shown in plot c) of Figure 8-6. Now, the measurements are conducive to accurately estimate $L_m$ and successive measurements consistently gave an inductance value of 12 µH. The waveforms are exponentially decaying as described by (8-3)-(8-5). The starting values and variation bounds for coefficients $a_i$, $a_v$,
τ_i and τ_v set in the fitting algorithm are determined by the same methodology described in previous section.

**Estimation of Source Inductance L_{nn}**

L_{nn} is estimated from current I_{tot} and voltage minus V_{out} during the falling edge in open circuit measurement. The waveforms are exponentially decaying as described by (8-3)-(8-5). The starting values and variation bounds for a_i, a_v, τ_i and τ_v set in the fitting algorithm are determined by the same methodology described in previous section.

### 8-3 Inductances Estimation with Disconnector Closed

In order to estimate the bus two inductance L_2 and the disconnector inductance L_{ds}, the experiment is run keeping disconnector switch in closed position. Since the inductances to be estimated are extremely low, particularly the inductance of the disconnector switch, the source inductance of the input buck converter is set at low value to enable faster current changes in the circuit and hence ensuring a higher voltage drop across these inductances. The inductances are estimated using the switch off period of the measured current and voltage. The equivalent circuit in this configuration is shown in Figure 8-7.

![Figure 8-7: Equivalent circuit during switch off duration with GIS disconnector closed.](image)

The differential equations governing the system behaviour in this configuration is given by (8-7)-(8-9). Here, L_{tot} = L_{11} + L_m and R_{tot} = R_{11} + R_m

\[
L_{tot} \frac{dI_{tot}}{dt} + R_{tot} I_{tot} = -V_{bus}
\]  
\[
L_1 \frac{dI_1}{dt} + R_1 I_1 = V_{bus}
\]  
\[
L_2 \frac{dI_2}{dt} + R_2 I_2 = V_{bus}
\]  

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The simplifying of the above set of equations to its state space representation is shown in (8-10).

\[
\begin{bmatrix}
\frac{dI_1}{dt} \\
\frac{dI_2}{dt}
\end{bmatrix} =
\begin{bmatrix}
\left( \frac{1}{L_1} \left( \sum \frac{1}{L_{\text{inv}}} \right) - \frac{1}{\tau_1} \right) & \left( \frac{1}{L_1} \left( \sum \frac{1}{L_{\text{inv}}} \right) \right) \\
\left( \frac{1}{L_2} \left( \sum \frac{1}{L_{\text{inv}}} \right) \right) & \left( \frac{1}{L_2} \left( \sum \frac{1}{L_{\text{inv}}} \right) - \frac{1}{\tau_2} \right)
\end{bmatrix}
\begin{bmatrix}
I_1 \\
I_2
\end{bmatrix}
\]  

where, time constants are \( \tau_1 = \frac{L_1}{R_1} \), \( \tau_2 = \frac{L_2}{R_2} \) and \( \tau = \frac{L_{\text{nn}} + L_m}{R_{\text{nn}} + R_m} \). The inductance \( L_{\text{inv}} \) is defined as \( L_{\text{inv}} = \frac{1}{\frac{1}{L_{\text{nn}}} + \frac{1}{L_m} + \frac{1}{L_1} + \frac{1}{L_2}} \).

As per the theory presented in [35], given a linear system of order ‘n’ described by the equation \( \dot{x} = Ax \) such as given in (8-10), the homogeneous response of any state variable of the system can be determined from an arbitrary set of initial conditions and a linear combination of components \( e^{\lambda_it} \), where, \( \lambda_i \) are the eigenvalues of matrix A. The time domain evolution of bus currents with GIS disconnector in closed position from their initial values \( I_1(0) \) and \( I_2(0) \) during the switch off period is given by (8-11).

\[
\begin{bmatrix}
I_1(t) \\
I_2(t)
\end{bmatrix} = v \begin{bmatrix}
e^{\lambda_1 t} & 0 \\
0 & e^{\lambda_2 t}
\end{bmatrix} v^{-1} \begin{bmatrix}
I_1(0) \\
I_2(0)
\end{bmatrix}
\]  

Here, v is matrix of set of eigenvectors of A presented in (8-10). The approximate values of elements of matrix A can be determined from the exact values of measured resistances described in Section 8-1, estimated values of bus one inductance \( L_1 \), main bus inductance \( L_m \) and source inductance \( L_{\text{nn}} \) described in Section 8-2 and approximate theoretical value of bus two inductances from lookup table developed based on the theory presented in [31]. Finally, from (8-11), the starting values for coefficients and time constants of (8-12)-(8-14) are determined.

**Estimation of Bus Two Inductance**

During the switch off period of input buck converter with GIS disconnector in closed position, the response of bus two current and the voltage across it is of the nature given by,

\[
I_1 = a_{i1} e^{t/\tau_{i1}} + a_{i2} e^{t/\tau_{i2}} \]  
\[
\frac{dI_1}{dt} = -a_{i1} \frac{e^{t/\tau_{i1}}}{\tau_{i1}} + -a_{i2} \frac{e^{t/\tau_{i2}}}{\tau_{i2}} \]  
\[
V_{\text{bus}} = a_{v1} e^{t/\tau_{v1}} + a_{v2} e^{t/\tau_{v2}} \]

All coefficients and time constants of the exponential terms \( a_{i1}, a_{i2}, \tau_{i1} \) and \( \tau_{i2} \) described in (8-12)-(8-14) can be derived from (8-11) and their starting values used in the fitting algorithms.
are determined. Depending on the tap settings of \( L_1 \) and \( L_2 \), one of the exponential terms is dominant, particularly in the time period equal to the time constant associated with this exponential. In the estimation result presented here, the second term is more dominant and 20% variation is allowed in it during current fitting.

The output coefficients of the current fitting function are used to compute the starting values for the voltage fitting algorithm. The slope of first exponential can be estimated more accurately from bus voltage fitting and the tolerance should be fixed in all four starting values to get accurate voltage fitting. Finally, the current fitting function is called again. The starting values for first exponential is computed from the output from voltage fitting function call and the starting values for the second exponential is provided from output of the first current fitting function call. A typical fitting result for bus two current for the selected periods is shown in Figure 8-8. As observed, the waveform of measured bus two current (blue) closely follows the fitting result \( I_{eq} \) (red).

A typical fitting result for the bus voltage \( V_{eq} \) (red) against the measured values (blue) for selected periods with GIS disconnector in closed position is shown in Figure 8-9.

The differential equation that determines the behaviour of bus voltage based on the bus two current is similar to the one described by (8-6) for the inductance and resistance of bus two. With time dependant equations for \( V_{bus} \), \( I_2 \) and the time differential of current available for the selected periods from the previously described fitting functions, the over defined linear system is solved simultaneously for bus two inductance with known measured value of bus resistance. Figure 8-10 shows that the measured (red) and the fitted bus voltage (black) with estimated bus two inductance closely follow each other for the selected periods.

Note that the inductance estimated in this way is the entire inductance in the path of bus two between the measurement points for \( V_{bus} \), including that of the GIS disconnector inductance \( L_{ds} \).

Figure 8-8: Fitting for bus two current during selected periods.

Figure 8-9: Fitting for bus voltage during selected periods.

Figure 8-10: Fitting for bus two inductance during selected periods.

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Estimation of GIS Disconnector Inductance

The inductance associated with the GIS disconnector due to its structure and length exists in path of the voltage measurement \( V_{ds} \) and while small in value, significant voltage drop can occur due to it during rapid current change, particularly during switch on time of the buck converter. In order to estimate the arc voltage across the separating electrodes of the GIS, it is crucial to know this inductance and subtract the drop associated with it from the measured disconnector voltage during bus transfer analysis. Figure 8-11 shows the fitting for voltage across the GIS disconnector during closed position.

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The fitting algorithms used are similar to the one described in previous subsection. Note that
the voltage that appears across the disconnector is minute during the falling edge of current
even when a low source inductance of 0.2 mH is used. The inductance of the GIS section
is found to be 1.5 \( \mu \)H over a series of similarly designed experimental conditions. Typical
estimation results based on the methodology described here are presented in Appendix E.

## 8-4 Graphical User Interface for Parameter Estimation

Figure 8-12 depicts the graphical user interface (GUI) developed in MATLAB for analysing
the results of open circuit and short circuit experiments and determining the circuit param-
eters from back end algorithms based on the theory explained in previous sections.

On initiation, the GUI prompts the user to load the measurement data. The panels indicated in Figure 8-12 allow the user to do the following:

1. **Plot area:** Displays waveforms of two measured parameters and the user selected
periods for data analysis.

2. **Display selection:** Allows the user to chose the two parameters to be displayed in the
plot area. Options available are \( I_1 \), \( I_2 \), \( I_{\text{tot}} \), \( V_{\text{bus}} \), \( V_{\text{out}} \) and \( V_{\text{ds}} \). The ‘Display’ button
updates the plot area waveforms according to the selected data.

3. **Data selection:** This panel allows the user to select periods in the displayed waveforms
to be used for the parameter estimation.
4. **Inductance computation**: This panel allows the user to define the set of experimental conditions within which the loaded measurement was made and choose the inductance to be computed.
• The precise measured values of all relevant circuit resistances must be entered by the user in mΩ. As described in the previous section, the voltage drop across the resistances is negligible and separately measuring it increases the accuracy of inductance estimation.

• Drop down menu for selecting the tap settings of various inductances in the experimental setup provides appropriate starting values to the fitting algorithm. The look up table containing the theoretically estimated inductances for corresponding tap selections [31] is prepared. The input lower and upper limit of inductances to the fitting algorithm is 10% of the lowest tap setting and 110% of the highest tap setting in the look up table respectively.

• User must select the inductance that is to be estimated from the drop down menu. Upon selection, the back-end of the GUI ‘loads’ the appropriate voltage and current data as described in the previous section required to compute the selected inductance. Proper legend names and dynamically named variables for saving the final results are also triggered.

• Measurement test type should be selected as open circuit (OC) or short circuit (SC). This triggers the corresponding current and voltage fitting algorithms as per the theory described. This selection also computes the various start values required by the fitting algorithms. The string ‘OC’ or ‘SC’ is also used for part of the naming structure of the final result file.

• On clicking the ‘Compute’ button, the chosen inductance is estimated for each selected period of the appropriately loaded current and voltage waveform. The fitting algorithm first fits the current and voltage waveforms, then based on the output coefficients, finds the time differential of current. Then, the inductance fitting algorithm is called to estimate the inductance value. Figures with waveforms depicting the actual and fitted data, for each period as sub-plot, are plotted and the MATLAB figure is automatically saved in the ‘results’ folder created in the folder from which the user had loaded the data. Variables that are dynamically named based on the user selected inductance, are used to save the final estimated parameters like coefficients from current fitting algorithm, voltage fitting algorithm, sum of square of errors and the estimated inductance.

• ‘Save Computation’ button saves all results in the ‘results’ folder in a .mat file of name structure as (measurement type)_(loaded measurement file name)_(results).
Chapter 9

Validation of Simulation Model and Parameter Estimation Methodology

The simulation model developed to emulate the experimental setup in open and short circuit condition of GIS electrodes is important to design experimental series for bus transfer process and predict the possible voltages and current that can appear in the GIS during bus transfer. Tap settings of the two buses and source inductance, the initial capacitor voltage and switching frequency can influence these parameters and hence the arcing behaviour during bus transfer.

Similarly, parameter estimation is important to determine the various inductances and resistances that govern the system behaviour during the simulation. Further, to determine the arc voltage and analytical estimation of re-strike and recovery voltage from the measurement data, it is crucial to know the various parameters of the system.

The physics of the experimental setup, control strategy used and the methodology to estimate the parameters is described in detail in previous sections. However, it is also important to determine the accuracy of simulation model and the parameter estimation in emulating the actual experimental setup. In order to do this, a comparative analysis is done for the measured data under specific conditions and simulation data with estimated parameters and simulation model under similarly defined conditions.

9-1 Safety Factor Correction

Figure 9-1 shows the current waveforms when the buck converter controllers of both the actual setup and the simulation model are programmed to control the peak current to 700 A with single buck converter in operation and GIS in open condition.

It can be observed that in this scenario the actual measured current peak is lower than its set value. This is because the converter controller is programmed to take a safety factor into
account which is estimated by obtaining and averaging the peaks of the measurement and dividing by the set current value as shown in Figure 9-1. The safety factor varies slightly during a series of experiments due to uncertainty in current measurement and controller behaviour during the experiment. Similarly the safety factor of all three converter controllers are obtained.

9-2 Validation For GIS in Open Condition

The comparative analysis of simulation data and the measurement data with GIS in open condition for single buck converter is shown in Figure 9-2.

As observed, the total current, capacitor voltage, bus voltage and the output voltage of the buck converter of the simulation model closely follow the corresponding measured parameters for the experimental setup configured with the same conditions. The relative error is computed using (9-1).

\[
E_{rel} = \left( \frac{|M - S|}{|M|} \right) \cdot 100
\]  

(9-1)

where, M is the measured data and S is the simulated data. Figure 9-3 shows the percentage
error in simulation results as compared to the measurement data for total current, bus voltage,
capacitor voltage and the voltage at the output side of the buck converter.

The relative error in the bus current remains less than 10% and increases towards the end
of falling edge due to small actual values. In this scenario, the error in capacitor voltage
remains less than 2%. The error in bus voltage is high during the instant of switching due
to transient overshoot due to parasitic capacitance of the inductance coils used to replicate
the buses. Relative error when high frequency oscillations have damped out is about 10%.
In case of output voltage of the source buck converter, the error associated with transient

Figure 9-2: Comparison of simulation results with measured data with GIS open.

Figure 9-3: Percentage error in simulation results as compared to measured data with GIS open.
overshoot is lower and the relative error in other time instants is also low as compared to the bus voltage.

9-3 Validation For GIS in Closed Condition

Similar experimental series was conducted with GIS in closed position for different tap settings of the inductance coils. The measured values of circuit voltages and currents were then compared with the simulated values under similar parameter settings as presented in Appendix E. The comparisons show a similar trend as described in previous section and hence both the simulation model as well as the parameter estimation methodology for all circuit inductances is validated.

9-4 Sources of Error

The deviations in simulation results from the measured data are due to several independent factors like:

- Parasitic capacitances of the inductance coils result in high frequency oscillations in the bus voltage at the switching instant.

- Uncertainty in the converter controller and the current measurement leads to some fluctuations in the current peaks in consequent switching instants. The simulation model has a crisp and precise control which can deviate from the setup that operates with practical uncertainties.

- Errors associated with estimation of various circuit parameters, temperature and frequency dependant variations in resistances and inductances can influence the comparative results.

- Measurement and rounding off errors also play a role.
Chapter 10

Recovery and Re-strike Voltage

10-1 Definition and Analytical Expression

Recovery voltage is the voltage that appears across the electrodes of the GIS disconnector at the instant of arc extinction.

Restrike Voltage is the voltage across the disconnector just before the instant of arc reignalion.

During arcing, recovery voltage appearing across the disconnector electrodes at current zero of bus two is important to study the arcing behaviour and reignition. The value of bus voltage in this circuit configuration depends on several parameters like capacitor voltage $V_c$, source inductance $L_{in}$, switching frequency of source IGBT and the bus one inductance $L_1$. This is not accurately measurable in case reignition does occur and further, the parasitic capacitances can introduce transient voltages at switching instant. Hence, the analytic expression described by (10-1) is used to estimate the recovery and re-strike voltages. This is derived for the equivalent circuit shown in (7-3) with disconnector switch open. Note that the transient voltages appearing at arc extinction due to parasitic capacitances are also important and measurable for analysis.

\[
V_{\text{bus}} = \frac{(I_{\text{tot}} \frac{1}{\tau_m} - \frac{1}{L_1})}{\tau_m} \left( L_m \left( \frac{1}{L_m} + \frac{1}{L_1} \right) \right) - \left( \sum_{n=1}^{3} \frac{P_n}{L_m} \right) V_c - \frac{I_{\text{tot}} \frac{1}{\tau_m} + \sum_{n=1}^{3} \left( \frac{1}{L_{\text{nn}}} \right)}{\frac{1}{L_m} - L_m \left( \frac{1}{L_m} + \frac{1}{L_1} \right) \left( \frac{1}{L_m} + \frac{1}{L_1} \right)}
\]  

(10-1)

In order to determine the possible values of recovery voltage that can appear across the parallel buses at the instant the arc extinguishes, the model described above is modified to simulate the circuit configuration with bus two disconnected. This scenario is simulated for different parameter values.

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10-2 Effect of Source Voltage and Inductance

Figure 10-1 shows the voltage that appears across the bus with the disconnector open during one switching period for different capacitor voltages $V_c$ and source inductance $L_{nn}$.

With decrease in source buck converter inductance, the following can be observed:

- Peak bus voltage increases during both switch on and switch off time due to higher $\frac{di}{dt}$ in the bus one inductance.
- Switch on time decreases as the current is able to reach its set value faster.
- As the circuit time constant during the fall period of current decreases, the bus voltage falls to zero faster.

The source capacitor voltage is charged upto 1500 V, 2000 V and 2500 V. With increase in source voltage level, the bus voltage with disconnector open varies in the following way:

- Peak voltage increases during switch on duration but remains the same during switch off duration.
- Switch on duration decreases as the current is able to reach its set value faster.
10-3  Effect of Switching Frequency

Figure 10-2 shows the voltage that appears across the bus with the disconnector open during one switching period for different switching frequencies and source inductance $L_{nn}$.

![Figure 10-2: Bus Voltage for different switching frequencies and source inductances with capacitor voltage 1.5 kV, bus one inductance 80 $\mu$H and switching frequency of a) 1 kHz b) 2 kHz c) 3 kHz](image)

With increase in switching frequency the switch on time remains more or less similar but switch off time decreases. As a result, the recovery voltage does not fall to low values towards the end of switch off period.

10-4  Approximation in Recovery Voltage

(10-1) offers a way to analytically estimate the recovery voltage from the measured space variables like main bus current, bus current and the capacitor voltage. The buck converter current on the other hand, is not measured. In case only one converter is operating, the buck converter current $I_{b1}$ is equal to the main bus current $I_{tot}$. However, when more than one buck converter is operating, particularly to increase the main bus current to a value greater than the rated current capacity of individual converters, an approximation is needed. The time constant $\tau_{nn} \gg \tau_{m}$, considering that the source buck converter inductance is greater than the main bus inductance by an order of $10^3$. In such a scenario, the term $\sum_{n=1}^{3} \left( \frac{I_{bn}}{\tau_{nn}} \right)$ can be neglected during estimation.

In most cases when two buck converters are used, one of them is of a high source inductance of 5.5 mH to introduce higher current of lower ripple. Figure 10-3 shows the simulation result...
for voltage across the bus one for system with two source buck converters with 0.2 mH and 5.5 mH inductance, 80 µH bus one inductance, 2 kHz switching frequency and 1500 V initial capacitor voltage with GIS opened with peak current controlled at 500 A. Corresponding approximated bus voltage and the relative percentage error is also shown. Herein, the buck current is the corresponding current outputs from the source buck converters.

By neglecting the buck converter current, the maximum estimation error remains below 4%. This error increases with increasing buck converter current. In the experiments, the peak buck converter currents are known from the controller set values and the safety factor. By introducing the average buck converter current equal to half of the peak current corresponding to the boundary conduction mode operation of the buck converter in the term \( \sum_{n=1}^{3} \left( \frac{I_{bn}}{\tau_{nn}} \right) \), the relative error is significantly reduced to below 2%. The associated reduced error in approximation is also shown in Figure 10-3.

It is important to understand the impact of increasing source inductance on the approximation error. Further, the absolute error in volts that is introduced during approximation must be of acceptable value. Figure 10-4 shows the absolute error for different source inductances of one buck converter with other buck converter at 5.5 mH, 80 µH bus one inductance, 2 kHz switching frequency and 1500 V initial capacitor voltage with GIS opened with peak current controlled at 500 A.

With increasing source inductance, the ripple in the buck current decreases and the average value is higher than that during boundary conduction mode. The average absolute error in estimated recovery voltage is highest for the high source inductance of 1.5 mH at 0.88 V. It should be noted that with known frequency of operation and inductance, a more precise average buck current value can be assumed based on an expected duty cycle value (which is not measurable).

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10-5 Switching Pulse State Computation

The switching pulse state $P_n$ of the buck converter (1 for closed, 0 for opened) is also required for the computation of the recovery voltage from the analytical expression in (10-1). This can be obtained from the time derivative of the main bus current $I_{tot}$. Figure 10-5 shows the switching pulse state of a single buck converter computed based on the time derivative of the main current.

In this case positive time derivative of current corresponds to $P_n = 1$ while negative corresponds to $P_n = 0$. Since the negative level is close to zero, $P_n$ is taken as 0 if the derivative level is lower than average of the two levels and 1 if it is greater.
In case two buck converters are used, the main bus current time derivative will have four operating levels corresponding to the different switch state combinations, while for three buck converters, there will be eight operating levels. In a more complicated setup for future measurements, it is appropriate to obtain the measured information on the individual switching pulses of each buck converters.

10-6 Validation of Analytical Expression

Computation of both recovery and re-strike voltage is after the arc in bus two has extinguished and hence the validation process for GIS in open condition described in Section 9-2 also holds true for the analytical expression described in (10-1).
Chapter 11

Analysis of Bus Transfer Measurements

11-1 Graphical User Interface for Data Analysis

The graphical user interface developed on MATLAB to analyse the bus transfer measurement series is shown in Figure 11-1.

*Figure 11-1: Graphical user interface for bus transfer analysis.*
In the default view, after the user loads the measurement data from MATLAB prompt at GUI initiation, sub-plot 1 shows the measured currents, sub-plot 2 the optical sensor output (described in Appendix D), sub-plot 3 the measured bus voltage and sub-plot 4 shows the voltage measured across the GIS disconnector. Y-axis ticks are whitened out for bus voltage and disconnector voltage in Figure 11-1 due to confidentiality obligations with ABB.

‘Display’ button in the center allows the user to update the plots after choosing from measured data of bus voltage, disconnector voltage, optical sensor output, capacitor voltage, buck output voltage, total main bus current and the currents of the two parallel buses.

The arcing period can be recognized from the disconnector voltage waveform. At arc initiation, a jump in voltage associated with the electrode drop can be observed. At arc extinction, it becomes equal to the bus voltage. In many situations, arc voltage is similar to the recovery voltage, due to which arcing periods cannot be easily differentiated. To circumvent this problem, an optical sensor was designed and installed to provide a visual identification of arcing. The complete design of optical sensor is described in Appendix D.

‘Arc Start’ button registers the index points corresponding to the user specified cursor position at all arc initiations. ‘Arc Stop’ button registers the index points corresponding to the user specified cursor position at all arc extinctions. These buttons must be pressed in sequence [Arc Start]-[Arc Stop] from the instant of first arc initiation to the instant of last arc extinction. From the number of specified arc periods, back-end program determines the number of re-ignitions. Typical waveforms\(^1\) during bus transfer are shown in Figure 11-2.

\[\text{Figure 11-2: Typical waveforms when GIS disconnector is implementing bus transfer.}\]

In the extreme right side of the GUI, the user must enter the circuit parameters estimated using the methodology presented in Chapter 8 corresponding to the conditions in which

\(^1\) Voltages from which the arcing characteristics can be determined are expressed in per unit. For base values, contact the author of this document.

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the bus transfer experiment was conducted. The back-end program of the GUI uses these parameters for analysis.

The function of GUI buttons ‘Period Start’ and ‘Period Stop’ is described in Section 11-2. ‘Redo Last’ erases the last start-stop user input sequence while ‘Reset All’ erases all changes made by the user.

Button panel of the left bottom of the GUI provides analysis for various parameters that can influence the arcing characteristics during the bus transfer process such as:

- The burn time of the arc during each strike.
- Starting arc current.
- Arc voltage during bus transfer.
- Recovery voltage at successful extinction and re-strike voltage.
- Input power (both average and instantaneous) and energy during each strike.

‘Save Computation’ buttons saves the mat file with all data analysis in the appropriate results folder.

11-2 Actual Arc Voltage Determination

The voltage measured across the GIS disconnector has a non-zero inductance and resistance between the probes as described in Section 8-3. The drop occurring across it can be significant, particularly during the switch-on duration of the input buck converter. In order to obtain the arc voltage across the separating electrodes, this drop must be removed from the measured voltage as described by (11-1). The time differential of the measured arc current is shown in Figure 11-2.

\[ U_{\text{arc,fast}} = V_{ds} - L_{ds} \frac{dI_{\text{arc}}}{dt} - R_{ds} I_{\text{arc}} \]  

(11-1)

Due to parasitic capacitance associated with the inductance coil used to model the bus connected to the GIS, high frequency fluctuations are observed in \( U_{\text{arc,fast}} \) during switching instant. In order to obtain the correct arc voltage \( U_{\text{arc,lp}} \), a digital low pass filter is used, described by (11-2)-(11-4).

\[ U_{\text{arc,lp,1}} = \text{mean}(U_{\text{arc,fast}}(0.5\,ms)) \]  

(11-2)

\[ \alpha = \frac{\Delta T}{\tau_{\text{lpf}} + \Delta T} \]  

(11-3)

\[ U_{\text{arc,lp,k+1}} = (1 - \alpha)U_{\text{arc,lp,k}} + \alpha U_{\text{arc,fast,k+1}} \]  

(11-4)

Where, \( k \) is from 1 to \( n \), \( \Delta T \) is the sample rate of data points and time constant \( \tau_{\text{lpf}} \) corresponds to the high frequency oscillations associated with parasitic capacitance of the bus.
after switching action. The initial point $U_{\text{arc,lp,1}}$ is obtained by averaging the first 0.5 ms of stable $U_{\text{arc,fast}}$. The period specifying this stable regions can be specified using buttons ‘Period Start’ and ‘Period Stop’ of the GUI. The corrected arc voltage waveform is shown in Figure 11-3.

\begin{figure}[h]
\centering
\includegraphics[width=\textwidth]{image113.png}
\caption{Corrected arc voltage waveform.}
\end{figure}

### 11-3 Arc Power and Energy Computation

Input arc energy is also an important parameter analysis that can influence arcing behaviour. Typical arc power input is shown in Figure 11-4.

\begin{figure}[h]
\centering
\includegraphics[width=\textwidth]{image114.png}
\caption{Power input to the arc when bus transfer is under way.}
\end{figure}
Arc energy $E_{\text{arc}}$ is determined from (11-5).

$$E_{\text{arc}} = \int_{t_{\text{arc, start}}}^{t_{\text{arc, stop}}} I_{\text{arc}} U_{\text{arc}} dt$$  \hspace{1cm} (11-5)

### 11-4 Experimental Series on HVDC Bus Transfer

Based on the theory developed in the previous chapters, several bus transfer experiments were performed under varying conditions and analysed. Analysis results of two typical experiments are presented in Table 11-1.

**Table 11-1: Typical analysis results for HVDC bus transfer experiments**

<table>
<thead>
<tr>
<th>#</th>
<th>1</th>
<th>2</th>
</tr>
</thead>
<tbody>
<tr>
<td>Bus one inductance (µH)</td>
<td>80</td>
<td>80</td>
</tr>
<tr>
<td>Bus two inductance (µH)</td>
<td>15</td>
<td>15</td>
</tr>
<tr>
<td>Source inductance (mH)</td>
<td>0.2</td>
<td>0.2</td>
</tr>
<tr>
<td>Initial capacitor voltage (V)</td>
<td>1700</td>
<td>1700</td>
</tr>
<tr>
<td>Buck current set point (A)</td>
<td>800</td>
<td>600</td>
</tr>
<tr>
<td>Number of re-strikes</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>Burn time (ms)</td>
<td>1.1</td>
<td>0.83, 0.15</td>
</tr>
<tr>
<td>Re-ignition delay (ms)</td>
<td>-</td>
<td>0.06</td>
</tr>
<tr>
<td>Starting arc current (A)</td>
<td>428</td>
<td>333, 202</td>
</tr>
<tr>
<td>Average arc voltage (p.u)</td>
<td>0.21</td>
<td>0.21, 0.3</td>
</tr>
<tr>
<td>Average arc power (p.u)</td>
<td>4.6</td>
<td>4.2, 3.1</td>
</tr>
<tr>
<td>Average arc energy (J)</td>
<td>5.3</td>
<td>3.4, 0.5</td>
</tr>
<tr>
<td>Arc voltage before extinction (p.u)</td>
<td>0.38</td>
<td>0.34, 0.48</td>
</tr>
<tr>
<td>Recovery voltage (p.u)</td>
<td>-0.51</td>
<td>-0.37, -0.49</td>
</tr>
<tr>
<td>Re-strike voltage (p.u)</td>
<td>-</td>
<td>3.72</td>
</tr>
</tbody>
</table>
In this part of the thesis, the bus transfer process for two buses in parallel facilitated by the HVDC GIS disconnector was studied. The experimental setup for the same was described and a simulation model was developed based on its physics and control strategy. Different circuit inductances were estimated by designing specific experiment series and a graphical user interface was developed to aid in computing the required parameters. Both the simulation model and the parameter estimation methodology were validated by comparing the simulation results and the measurement data under similar configurations.

The analytical expression for recovery and re-strike voltage was defined to study the arcing characteristics of the GIS disconnector and associated approximation methods were described and justified for computing the voltages from existing measured parameters of the experimental setup.

The simulation model was used to simulate and study the effect of changing the setup configurations like the source buck inductance, switching frequency and initial capacitor voltage. Based on the results a series of experiments were designed and conducted for specific circuit configurations in which bus transfer characteristics were most interesting to study.

Analysis tools were developed to aid in studying the GIS characteristics during bus transfer. The actual arc voltage was computed by removing the drop against the GIS disconnector inductance. A graphical user interface was developed and described that can compute the parameters like arc burn time, starting arc current, actual arc voltage, power, energy, number of re-strikes, re-strike time, recovery and re-strike voltage and the arc voltage just before extinction. Finally, analysis results of typical bus transfer experiments were presented.

The graphical user interfaces for parameter estimation and bus transfer analysis that were developed in this study offer a package to analyse measured data and compute various parameters important for characterization of arcs and hence the bus transfer process. A validated simulation model and configurable circuit parameters allows the design of experiments under varied predictable conditions under which the bus transfer process is interesting to study.
Appendix A

Publication 1

Paper Title - Series Arc Extinction in DC Microgrids using Load Side Voltage Drop Detection

Authors - Laurens Mackay; Aditya Shekhar; Bart Roodenburg; Laura Ramírez-Elizondo; Pavol Bauer

Conference - International Conference on Direct Current Microgrids (ICDCM), 2015
Abstract—Due to the absence of current zero crossing, dc arcs do not extinguish as easily as ac ones. It is essential to detect and eliminate series arc faults in dc microgrids in order to ensure safety, particularly while unplugging loads. Several detection and extinction methods using various means are known in literature. In this paper a novel arc detection method is proposed. It detects the load side input voltage drop due to the initial electrode specific minimum arc voltage. Only the local input voltage has to be measured and selectivity is given. The arc can be extinguished by shutting down the load’s power electronics converter. The proposed method is elaborated through simulation of arc behaviour for constant resistor and constant power loads with input capacitors. First experimental results correspond with the theoretical analysis.

Index Terms—Arcing, arc detection, arc extinction, dc arc, dc microgrid, series arc

I. INTRODUCTION

Decentralized dc nano- and microgrids provide interesting opportunities to address the challenges faced by the modern energy distribution systems [1]. Apart from inherently more efficient operation and saving on materials as compared to ac distribution grids, they can offer higher flexibility and availability. In countries facing rapid urban expansion, the idea of designing self sustainable smart cities as satellite towns of main cities is increasingly interesting [2], [3]. Furthermore, in developing countries where grid infrastructure is not as extensive, standalone dc nano grids in remote rural areas can prove to be a lifeline. This will not only provide access to energy to millions of people, but also increase the reach of renewable energy such as PV technology, which is inherently dc in nature. Sudden replacement of ac infrastructure is challenging, however dc ready devices, working on both ac and dc, could simplify transition [4]. Standardization has first to be brought forward. This paper is aiming to contribute to the discussion.

In dc microgrids, arcs do not extinguish as easily as ac ones due to the absence of current zero crossing. This demands a rapid protective response in detecting and eliminating any arcs that may arise, particularly in case of unintended energized unplugging of loads. Various methods are discussed in literature [5]–[7]. Current technology uses mechanically designed contacts to reduce the risk of arcing and to shield the users from the arc location. Such devices are prone to wear and tear and fail after several usage cycles. Arc reduction using internal diode in the plug is explored in [6]. Arcs can also be prevented by plugs with early disconnection pins wherein the load can monitor these pins and switch off before the main contacts open. Another solution is an arc free dc plug [7] that uses a solid state switch in the plug itself to eliminate any arcs. While these solutions require special plug designs and additional components, the algorithm proposed in this paper by detecting the load voltage drop at arc initiation shown in Fig. 1 can mitigate the arcing problem without additional components.

Electric arcs are formed when two electrodes of an energized electric circuit with finite current are drawn apart. Just before the electrodes separate, the high contact resistance vaporizes the metal and in combination with electrons ejected from thermionic emission that ionize the air between the electrodes, creates an conductive plasma channel to bridge the gap. The arc can sustain itself if the input energy is greater than the energy removed through heat transfer.

In the absence of zero crossing of current in dc circuits, extinguishing the arc is difficult. Sustained series arc faults, if left unattended, can cause fires and serious property damage [8]. The 2011 National Electric Code [9], has defined guidelines for photovoltaic (PV) systems with operating voltage of 80 V or higher and necessitates arc fault current interrupters (AFCI) to detect arcs greater than 300 W and interrupt them within 2 s.

With the proliferation of dc systems in the PV market,
Fig. 2. Arc detection algorithm based on drop in load voltage due to minimum electrode gap voltage of series arcs.

research by Sandia, SMA, Tigo Energy, Eaton, etc have developed an AFCI functionality in their products based on the detection of high frequency ac noise associated with the arcing behaviour [10]–[12]. In these applications, the low frequency component of the current and voltage signals cannot be used in the detection of series arcs because the IV characteristics of the PV module side change unpredictably with weather conditions and due to the presence of maximum power point tracking algorithms at the converter side [13].

In low voltage dc distribution networks it is advantageous to limit inrush currents and rate of change of loads and therefore uncontrolled voltage dips can be avoided if standards are made accordingly [1], [14]. The recognized disadvantage of centralized arc fault detection is that the entire system down the line is shut down [5], and selective isolation of fault location from the rest of the grid is important. Detecting the load voltage drop at arc initiation as proposed in this paper offers a possibility of rapid localized protective response. Using the here proposed method in combination with the high frequency arc signature detection can enable series and parallel arc detection and proper coordination with grid side source converter protection scheme can allow selectivity for series arcs and prevent tripping of a larger part of the grid.

Section II describes the proposed arc detection method and its implementation in devices. Section III discusses the arc model used and the simulation results for the detection algorithm during arcing for constant resistance, constant power and parallel constant power loads. In Section IV, experimental results for arcing with constant resistance load is shown and compared with the simulation model. Detection time taken by the algorithm to reach the trigger level for load voltage drop is shown. The findings are discussed in Section V and conclusions for future work are drawn.

II. PROPOSED ARC DETECTION METHOD

The drop in the load voltage associated with series arc initiation is specifically dependent on the electrode material [15] and can be detected by the load side power electronic converter, which can then respond accordingly to detach the load from the grid by reducing the load current to zero and thereby extinguishing the arc rapidly. The flow diagram depicting the proposed algorithm is shown in Fig. 2.

Fig. 3. Circuit diagram for series arc simulation.

The load voltage \( V_{\text{load}} \) is passed through the low pass filter (LPF), with Laplace transfer functions:

\[
V_{\text{slp}}(s) = \left( \frac{1}{1 + \tau_{s} s} \right) V_{\text{load}}(s) \tag{1}
\]

\[
V_{\text{flp}}(s) = \left( \frac{1}{1 + \tau_{f} s} \right) V_{\text{load}}(s) \tag{2}
\]

The time constant of the slow LPF \( \tau_{s} \) is taken here as 0.4 s, typically chosen to determine the grid voltage before the arc initiation but fast enough to reach steady state otherwise. A faster LPF with time constant \( \tau_{f} \) of 1 ms is taken to eliminate the high frequency noise in the load voltage. The output voltages \( V_{\text{slp}} \) and \( V_{\text{flp}} \) of the slow and fast LPF are compared:

\[
\Delta V = V_{\text{slp}} - V_{\text{flp}} > V_{\text{detect}} \tag{3}
\]

As soon as the difference \( \Delta V \) is greater than the trigger voltage \( V_{\text{detect}} \), the arc is detected and the device power electronics can initiate the switch off action. One possible way is to linearly reduce the load current to zero. The choice of the slope with which the algorithm decreases the load current depends on the circuit constrains and the time within which the arc needs to be extinguished.

The choice of the trigger voltage influences the speed of the arc detection and also has to account for the reduction in \( V_{\text{slp}} \). Hence, it is chosen lower than the actual electrode dependent voltage drop associated with the copper electrode. However, a very small value may result in spurious triggering and must be avoided.

The discrete time realization for the use in micro-controllers is given by (4) wherein, the smoothing factor \( \alpha \) is computed using (5) based on the sample time \( \Delta T \) and the required time constant \( \tau_{\text{lpf}} \) for low pass filter from (1) and (2).

\[
V_{\text{lpf},k} = (1 - \alpha) V_{\text{lpf},k-1} + \alpha V_{\text{load},k} \tag{4}
\]

\[
\alpha = \frac{\Delta T}{\tau_{\text{lpf}} + \Delta T} \tag{5}
\]

III. SIMULATION OF ARC DETECTION ALGORITHM

In this section, the proposed arc detection algorithm is validated through a MATLAB simulation.

A. Circuit Model

The circuit diagram used to simulate the series arc behaviour and to validate the arc detection algorithm is shown in Fig. 3. The state space equations are derived as
Empirical understanding of the arcing behaviour associated with the gap length, contact separation speed, circuit excitation voltage and arc current is necessary for modelling the arc. The initial electrode dependent voltage drop [15] for copper electrodes in open air in low voltage networks with arc current $I_{arc} < 100$ A for different electrode gap lengths is presented in Table I.

The arc model introduces a variable resistance into the circuit at arc initiation at time $t = 0$ s, before which the circuit is in steady state with $I_{arc} = I_{load}$. In order to model the arc resistance, the actual arc current is passed through a LPF with a time constant chosen $\tau_{arc} = 0.1$ ms. The temperature dependent arc resistance is not dependent on high frequency fluctuations in the current as the thermal time constant is greater than the electrical time constant. The electrode separation rate is at a constant speed of 30 mm/s. The arc resistance is linearly interpolated between the known data points of gap distance as per Table I.

### C. Constant Resistance

The circuit is simulated with a source voltage of 100 V, and typical circuit parameters for a 50 m cable with resistance $R_{cable}$ of 0.25 $\Omega$, cable inductance $L_{cable}$ of 100 $\mu$H and input load capacitor of 30 $\mu$F.
The arc current and load voltage simulated for 21.28 $\Omega$ constant resistance is shown in Fig. 4. The load voltage decreases as the arc voltage increases with increasing gap length. Subsequently, the arc current decreases due to a drop in load voltage until the arc extinguishes in about 0.21 s. A drop in the arc current can be observed at arc initiation which recovers within 0.2 ms. A similar initial arc current oscillation is observed with experimental results in Fig. 12.

The arc detection algorithm as described in (1)-(3) is used to detect the trigger voltage $V_{\text{detect}}$ of 10 V drop in the load voltage, which is chosen as 75% of the electrode dependent arc voltage for copper electrode. This enables fast arc detection, while being high enough to avoid spurious triggering. Upon detection, the load current is reduced to zero at the rate of -0.7 A/ms. As observed, the arc is extinguished in 7 ms.

D. Constant Power

Similarly, the circuit is simulated for a constant power load of 470 W (corresponding to the initial load current of 4.7 A as in the case of constant resistance load) as shown in Fig. 6. The load current is computed using a LPF output of measured load voltage ($\frac{1}{1+\tau_s}$) with $\tau_s = 0.01$ s to account for the finite response time of the power electronic converter.

With drop in the load voltage, the load current increases in order to maintain a constant power drawn at the load side.

Due to this, the time for which the arc is able to sustain is longer as compared to that of constant resistance load with the same initial circuit current and power drawn. The arc current and load voltage corresponding to the simulation with the arc detection algorithm is shown in Fig. 7. The rate of decrease in load current upon arc detection is again taken as -0.7 A/ms. As observed, the arc is extinguished in 9 ms.

E. Arc Detection and Selectivity with Parallel Loads

Fig. 8. shows the equivalent circuit for two constant power loads of 470 W connected in parallel via cables of resistances $R_{c1}$ and $R_{c2}$ of 0.01 $\Omega$ each to a grid of 100 V constant voltage and inductance $L_{dc}$ and resistance $R_{dc}$ of 100 $\mu$H and 0.25 $\Omega$ respectively.

Arcing during plug out can be simulated for either loads by
Fig. 9. Simulated circuit response for two parallel constant power loads with arc detection algorithm. The selectivity of the method is shown.

Fig. 10. Experimental setup for series electric arc.

Fig. 11. Measurement for constant resistance load without input capacitor.

The experimental data for arc current and load voltage for constant resistance load without parallel input capacitance is shown in Fig. 11. At $t = 0$ s relay is signalled to open and bouncing of contacts is observed. The main arc initiates at 1 ms. It can be observed that load voltage drops for about 8 ms as the relay contact opens and a stable arc is attained at constant gap distance of 1 mm. The simulation results for arc model under similar conditions are also depicted and they closely follow the experimental results.

The experiment setup is rerun for constant resistance load with parallel input capacitance $C_{load}$ of 30 $\mu$F and a cable with measured inductance $L_{cable}$ of 100 $\mu$H. The sample time $\Delta T$ of the experimental data shown in Fig. 12 is 0.8 $\mu$s. This data is fed into the discrete time realization of the arc detection algorithm as described in (4)-(5).

The discrete LPF output voltages $V_{slp}$ and $V_{flp}$ and the corresponding voltage difference are shown in Fig. 12. The arc is detected within 2 ms, after which the load side converter can initiate appropriate action by reducing the load current and thereby extinguishing the arc.

V. DISCUSSION AND CONCLUSION

The proposed series arc detection algorithm that makes it possible to eliminate arcs without additional components was simulated using MATLAB using a theoretical arc model. The input of arc length and current dependent resistance $R_{arc1}$ and $R_{arc2}$ respectively. The application of arc detection algorithm for the scenario in which the second load is plugged out is shown in Fig. 9.

It can be observed that voltage drop is detected at Load 2 and the current is ramped to zero at the rate of -0.7 A/ms. The Load 1 continues running as no significant voltage fluctuation occurs across its input capacitor $C_1$. Hence, a localized arc detection and clearing action is achieved and selectivity is given.

IV. EXPERIMENTAL RESULTS

The experimental setup was prepared as shown in Fig. 10. The electric arc is created by triggering the relay with a 12 V dc supply which opens its contact at a velocity of 125 mm/s and introduces a constant gap after reaching 1 mm. The dc supply voltage is 100 V and the circuit current is set to 4.7 A at steady state with constant resistance load of 21.28 $\Omega$ before arc initiation.

The experimental data for arc current and load voltage for constant resistance load without parallel input capacitance is shown in Fig. 11. At $t = 0$ s relay is signalled to open and bouncing of contacts is observed. The main arc initiates at 1 ms. It can be observed that load voltage drops for about 8 ms as the relay contact opens and a stable arc is attained at constant gap distance of 1 mm. The simulation results for arc model under similar conditions are also depicted and they closely follow the experimental results.

The experiment setup is rerun for constant resistance load with parallel input capacitance $C_{load}$ of 30 $\mu$F and a cable with measured inductance $L_{cable}$ of 100 $\mu$H. The sample time $\Delta T$ of the experimental data shown in Fig. 12 is 0.8 $\mu$s. This data is fed into the discrete time realization of the arc detection algorithm as described in (4)-(5).

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V. DISCUSSION AND CONCLUSION

The proposed series arc detection algorithm that makes it possible to eliminate arcs without additional components was simulated using MATLAB using a theoretical arc model. The
load voltage drop associated with arc initiation was detected and arc could be eliminated in 7 ms for constant resistance load and 9 ms for constant power load. From experimental data, it was shown that the arc can be detected in 2 ms.

Future work entails analysis on series arc fault behaviour with different load configurations such as constant power loads with input capacitor, as well as special input stages like inrush current limiter, a diode limiting grid short-circuit currents or power line communication with filtering inductors and testing the accuracy of proposed detection scheme in these scenarios. Furthermore, the arc protection coordination with AFCI devices at source side has to be studied. The voltage levels up to which the algorithm is sensitive needs to be determined, as at higher voltages, the arc dependent voltage drop will become insignificant.

References


Appendix B

Bus Transfer with AC Arcing

Based on the paper [31], a simulation model was prepared to analyse the theoretical behaviour of the system under similar conditions. The simulation results are depicted along with the measurement plots presented in the publication.

B-1 Equivalent Circuit of Experimental Setup

The circuit diagram based on the experimental set-up described in [31] to study ac arcing for bus transfer with Gas Insulated Switch (GIS) disconnector is shown in Figure B-1.

\[\begin{align*}
V_C & \quad C_S \\
L_S & \quad R_S & \quad I_{st} & \quad I_2 \\
L_1 & \quad I_1 & \quad L_2 \\
R_1 & \quad R_2 & \quad V_{DS} \\
V_{bus} & \end{align*}\]

**Figure B-1:** Circuit diagram based on the experimental set-up

Herein, \(L_1\) and \(R_1\) correspond to the inductance and resistance of bus 1, while \(L_2\) and \(R_2\) correspond to the inductance and resistance of bus 2. The SF6 gas insulated switch (GIS) disconnector introduces an arc in bus 2, across which the voltage \(V_{DS}\) is measured.

\(L_S-C_S-R_S\) acts as a high energy storage damped series resonant current source. Use of inout capacitor is a safety mechanism to ensure that circuit discharges in 10-20 ms in case the arc
Table B-1: Parameter Values for AC Equivalent Circuit

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Source Capacitance ($C_S$)</td>
<td>923 µF</td>
</tr>
<tr>
<td>Source Inductance ($L_S$)</td>
<td>9.2 mH</td>
</tr>
<tr>
<td>Natural Resonant Frequency ($f_s$)</td>
<td>54.6 Hz</td>
</tr>
<tr>
<td>Source Resistance ($R_S$)</td>
<td>285 mΩ</td>
</tr>
<tr>
<td>Bus 1 Inductance ($L_1$)</td>
<td>22 µH</td>
</tr>
<tr>
<td>Bus 1 Resistance ($R_1$)</td>
<td>1 mΩ</td>
</tr>
<tr>
<td>Bus 2 Inductance ($L_2$)</td>
<td>3 µH</td>
</tr>
<tr>
<td>Bus 2 Resistance ($R_2$)</td>
<td>0.55 mΩ</td>
</tr>
<tr>
<td>Arc Voltage at First Arc Ignition ($V_{DS}$)</td>
<td>15 V</td>
</tr>
<tr>
<td>Initial Capacitor Voltage ($V_C(0)$)</td>
<td>5000 V</td>
</tr>
<tr>
<td>Initial Source Current ($I_{tot}(0)$)</td>
<td>0 A</td>
</tr>
<tr>
<td>Initial Bus 1 Current ($I_1(0)$)</td>
<td>0 A</td>
</tr>
<tr>
<td>Initial Bus 2 Current ($I_2(0)$)</td>
<td>0 A</td>
</tr>
</tbody>
</table>

does not extinguish by itself, thereby preventing damage to the disconnector. The parameters used in simulation of the developed circuit model are mentioned in Table B-1.

**B-2 State Space Equations for Simulation Model**

The initial conditions of the state variable associated with the energy storage elements of the circuit ($V_C(0)$, $I_{tot}(0)$, $I_1(0)$ and $I_2(0)$) are mention in Table B-1. The state space equations corresponding to the circuit diagram in Figure B-1, used to develop the simulation model for the experimental set-up are presented in (B-1)-(B-4),

\[
\frac{dV_C}{dt} = \frac{1}{C_S} (-I_{tot}) \\
\frac{dI_{tot}}{dt} = \frac{V_C}{L_S} - \frac{V_{bus}}{L_S} - \frac{R_S I_{tot}}{L_S} \\
\frac{dI_1}{dt} = \frac{V_{bus}}{L_1} - \frac{R_1 I_1}{L_1} \\
\frac{dI_2}{dt} = \frac{V_{bus}}{L_2} - \frac{R_2 I_2}{L_2} - \frac{V_{DS}}{L_2}
\]

The bus voltage $V_{bus}$ is one of the measured parameters in the experimental set-up and can be expressed in terms of the space variables as per (B-5),

\[
V_{bus} = \left(\frac{1}{L_S} + \frac{1}{L_1} + \frac{1}{L_2}\right) \left(\frac{V_C}{L_S} + \frac{V_{DS}}{L_2} - I_1 \left(\frac{R_S}{L_S} - \frac{R_1}{L_1}\right) - I_2 \left(\frac{R_S}{L_S} - \frac{R_2}{L_2}\right)\right)
\]

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B-3 Simulation Results

The simulation results of the MATLAB model based on the afore mentioned state space equations is shown in Figure B-3.

Figure B-2: Simulation results for bus transfer with ac arc.

As observed, in this configuration, the bus transfer is successful with arc getting extinguished after the first current zero of the bus 2.

Figure B-3: Measurement results for bus transfer with ac arc (adapted from [31]).
Appendix C

Predictive Current Control

The duty cycle of the input switch is computed to control the each input buck converter current $I_{bn}$ individually. Each buck converter can be phase shifted to increase the effective frequency. It is computed by adapting the predictive current control strategy [34]. The governing conditions from which the predicted value of the duty cycle at $k+1$th step is derived from are shown in (C-1)-(C-3),

\begin{align*}
\left(\frac{dI_{bn}}{dt}\right)_{req} &= I_{ref} - I_{bn,k} \quad D_{k+1} \quad V_{out,k+1} \quad V_{C,k} \\
D_{k+1} &= \frac{V_{out,k+1}}{D_{k+1}T_S} \quad (C-1) \\
\left(\frac{dI_{bn}}{dt}\right)_{k+1} &= \frac{V_{C,k} - V_{out,k+1}}{L_{nn}} \\
\left(\frac{dI_{bn}}{dt}\right)_{k+1} &= \frac{V_{C,k} - V_{out,k+1}}{L_{nn}} \quad (C-2) \\
\end{align*}

wherein by equating the required input current derivative $\left(\frac{dI_{bn}}{dt}\right)_{req}$ by the actual current derivative at $k+1$th step $\left(\frac{dI_{bn}}{dt}\right)_{k+1}$, a quadratic expression for $D_{k+1}$ is obtained as in (C-5),

\begin{align*}
I_{ref} - I_{bn,k} &= \frac{V_{C,k}(1 - D_{k+1})}{L_{nn}} \quad (C-4) \\
D_{k+1}^2 - D_{k+1} + \frac{L_{nn}(I_{ref} - I_{bn,k})}{V_{C,k}T_S} &= 0 \quad (C-5) \\
\end{align*}

The roots of the equation are given by (C-6),

\begin{align*}
D_{k+1} &= 1 \pm \sqrt{1 - \left(\frac{4L_{nn}(I_{ref} - I_{bn,k})}{V_{C,k}T_S}\right)} \\
D_{k+1} &= 1 \pm \sqrt{1 - \left(\frac{4L_{nn}(I_{ref} - I_{bn,k})}{V_{C,k}T_S}\right)} \quad (C-6)
\end{align*}
We know that as the error between the reference current and the actual current at \( k \)th step increases, the predicted value of duty cycle must decrease. Hence, the duty cycle at \( (k+1) \)th step is given by (C-7),

\[
D_{k+1} = 1 - \sqrt{1 - \left( \frac{4L_{nn}(I_{ref} - I_{nn,k})}{V_{C,k}T_S} \right)^2}
\]  

(C-7)

It is important to note that for large deviation in the actual current value from its reference value, the term within the square root may become negative. In this situation, the duty cycle is set to 1.

\[\text{Figure C-1: Simulation results with predictive current control strategy.}\]

The simulation results with predictive current control strategy is shown in Figure C-1. Each buck converter is individually controlled to provide one third of the total current, and each has a phase shift of one-third of the switching time period resulting in an effective frequency of three times, thus reducing th ripple in the total current.

The limitation of this control strategy is that the value of the inductance, \( L_{nn} \) is variable and unknown, and must be pre-determined for accurately predicting the duty cycle. Hence, the peak current control strategy is used for the IGBT controller in the experimental set-up.
In each measurement interval, the arcing interval is of a small fraction. From the measured current and voltage waveforms of the system, it was difficult to distinguish when the bus transfer was occurring. This was particularly the case when the arc voltage was nearly equal to the recovery voltage. [36]

In order to provide a ‘visual’ identification of arcing, an optical sensor was designed which could highlight the bus transfer interval based on the highly luminous signature of arcing. Figure D-1. shows the bottom and top view of the optical sensor designed for visual identification of arcing during the bus transfer process.

For this purpose, the optical sensor OPT101 from Texas instruments [37] was used. By varying the value of external resistance, the gain and the bandwidth for cut-off frequency
can be varied. With lower gain, cut-off frequency increases, but the sensor becomes less sensitive to lower signal strength. Since the bandwidth is more relevant, and the sensor works adequately with lower gains as well [36], an external resistance of 50 kΩ and external capacitance of 56 pF is used to give a gain of $0.05 \times 10^6$ V/A and a bandwidth of 58 kHz.

Typical waveforms during bus transfer with multiple re-strikes is shown in Figure D-2. It can be appreciated how the visual input from optical sensor can help the user to quickly identify interesting intervals for analysis, which otherwise would be difficult to discern.

![Waveforms during bus transfer process depicting usefulness of optical sensor as visual aid.](image)

**Figure D-2:** Waveforms during bus transfer process depicting usefulness of optical sensor as visual aid.
Appendix E

Supporting Plots from Measured Data Analysis

E-1 Parameter Estimation Results

Figure E-1 shows the estimation results for the actual disconnector inductance \( L_{ds} \) for each selected period of three experiments conducted under conditions conducive to accurate analysis.

![Figure E-1: Estimation Results for Disconnector Inductance.](image)

Figure E-2 shows the estimated inductance values for bus one inductance \( L_1 \), bus two inductance \( L_2 \), main bus inductance \( L_m \), inductance of a prototype GIS disconnector \( L_{ds} \) and...
source inductance $L_{11}$ from a series of experiments conducted.

Figure E-2: Parameter Estimation Results for System Inductances.

E-2 Validation Results for GIS Disconnector in Closed Position

Figure E-3 shows the measured and simulated waveforms for various system parameters under similar circuit configuration. As observed, the waveforms are comparable and closely follow each other. The associated percentage error between the experimental and simulated results is shown in Figure E-4.
Figure E-3: Comparison of simulation results with measured data for GIS closed.
Figure E-4: Percentage error in simulation results and measured data.


[16] Laurens Mackay; Aditya Shekhar; Bart Roodenburg; Laura Ramirez-Elizondo; Pavol Bauer, “Series Arc Extinction in DC Microgrids using Load Side Voltage Drop Detection,” International Conference on Direct Current Microgrids(ICDCM), 2015.


### List of Acronyms

<table>
<thead>
<tr>
<th>Acronym</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>ac</td>
<td>Alternating Current</td>
</tr>
<tr>
<td>AFCI</td>
<td>Arc Fault Current Interrupters</td>
</tr>
<tr>
<td>dc</td>
<td>Direct Current</td>
</tr>
<tr>
<td>DS</td>
<td>Disconnector Switch</td>
</tr>
<tr>
<td>GIS</td>
<td>Gas insulated Switchgear</td>
</tr>
<tr>
<td>HVDC</td>
<td>High Voltage Direct Current</td>
</tr>
<tr>
<td>IGBT</td>
<td>Insulated Gate Bipolar Transistor</td>
</tr>
<tr>
<td>LPF</td>
<td>Low Pass Filter</td>
</tr>
<tr>
<td>LVDC</td>
<td>Low Voltage Direct Current</td>
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<tr>
<td>OC</td>
<td>Open Circuit</td>
</tr>
<tr>
<td>PV</td>
<td>Photovoltaic</td>
</tr>
<tr>
<td>RLC</td>
<td>Resistor Inductor Capacitor</td>
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<tr>
<td>SC</td>
<td>Short Circuit</td>
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