Laser Annealing of Self-Aligned As⁺ Implants in Contact Windows for Ultrashallow Junction Formation

C. Biasotto*, V. Gonda, L. K. Nanver, J. van der Cingel and V. Jovanović.

ECTM-DIMES, Delft University of Technology, P.O. BOX 5053, 2600 GB Delft,
The Netherlands;

Tel: +31 (0)15 2788837 *E-mail: c.biasotto@tudelft.nl

Abstract

In the past it has been shown that ultrashallow junctions with minimum lateral dimensions can be made by implanting self-aligned to the contact window and using one-shot excimer laser annealing (ELA) to activate the dopants. Besides the recrystallization of the implanted Si, the final structuring at the contact window perimeter is very important for the ideality of the diode. In this paper this process has been investigated for 5 keV As⁺ implanted in windows etched in a thermal/LPCVD oxide layer stack. The window perimeter processing is very critical but tilted implants can be used to increase the junction overlap with the window and good diode characteristics are obtained. The junction depths have been analyzed by secondary ion mass spectrometry (SIMS) and transmission electron microscopy (TEM). A junction of only 15 nm deep with a sheet resistance of 311 Ω /square was obtained for an implantation tilt angle of 45° and laser energy density of 1000 mJ/cm², whereas the junction depth of 20 nm and sheet resistance of 220 Ω /square was obtained for the tilt of 7°.

Introduction

With the scaling down of metal-oxide-semiconductor device technology, highly activated and ultrashallow yet highly conductive junctions for source and drain regions are required to suppress the short-channel effects [1]. Excimer laser annealing (ELA) technique has been successfully demonstrated to be an attractive alternative to rapid thermal anneal procedures, offering benefits such as precise control of the junction depth, good abruptness of dopant profile and higher dopant activation [2-8]. The minimum junction depth is determined by the profile of the ion implantation and the real junction depth is determined by the melt depth induced by ELA. Therefore, lowering the implantation energy is one of the ways to further reduce junction depth.

To minimize the lateral junction dimensions, self-aligned schemes are often implemented. In this paper we investigate integration of laser annealing in a process where the junction dopant implant is self-aligned to the diode contact window. The final overlap of the junction region with the contact window perimeter is critical for achieving good diode characteristics. Particularly for arsenic implants, which at energies below 5keV are inherently very shallow, maintaining sufficient overlap during the contact window processing can become problematic. This overlap has been studied as a function of oxide-layer-stack composition, implant tilt angle and ELA energy density of a single-shot anneal procedure. The I-V characterization of fabricated n⁺p diodes is used to evaluate the perfection of the junction at the perimeter.

Experimental procedures

An Exitech M8000V double laser system with a Lambda Physik LPX 210 XeCl excimer laser (308 nm, 25 ns full width at half maximum (FWHM) and single pulse) was used in this work. The energy densities are set through attenuators after which the laser beams are combined. A homogenizer is used to produce a flat top intensity profile over the $1.75 \times 2.5 \text{ mm}^2$ spot. Energy densities from 700 mJ/cm^2 to 1000 mJ/cm^2 were used.

To investigate junction depth, secondary ion mass spectroscopy (SIMS) and transmission electron microscopy (TEM) were utilized, four-point probe measurements was applied to extract sheet resistance. The fabricated diodes were electrically characterized by I-V measurements using a HP4156B parameter analyser.

The n^+p diodes with $40 \mu\text{m} \times 40 \mu\text{m}$ area were fabricated on (100) 2-5 $\Omega\cdot\text{cm}$ p-type Si wafers. The basic process flow for the fabrication of laser annealed diodes is shown in Figure 1.

Figure 1. Process flow for fabrication of n^+p laser annealed diodes.

Silicon dioxide layer of 30 nm is grown by thermal oxidation on the silicon surface and covered with 300 nm LPCVD oxide at 700°C , followed by a 100 nm thick Al(1%Si) reflective layer sputtered at 50°C . The Al layer is used as a reflective mask for laser light. Possible Al ablation at the window edges is not of importance for the resulting diode properties. The contact window is opened by dry etching landing on the silicon surface and the native oxide is removed using a BHF (1:7) solution for 15 seconds, which only removes 50 nm of the Al. Buffered-HF dip-etch is performed immediately before the low energy implantation. The n^+ region to be laser annealed is formed by a 5 keV, $2-3 \times 10^{15} \text{ cm}^{-2}$ As⁺ implantation with either a 7° or 30° tilt from eight directions. The implanted regions are then annealed by the laser at a 900 mJ/cm^2 energy density while the wafer-chuck temperature was kept at room temperature. A 4 min HF (0.55%) dip-etch is performed to remove the native oxide before metallization, which is done by depositing and patterning 600 nm Al(1%Si). Alloying in forming gas at 400°C is the final process step. The backside of the wafer was also metallized for contact to the p-substrate. To take full advantage of the laser-annealed ultrashallow junctions transient-enhanced diffusion

(TED) needs to be avoided after dopant activation by the laser and therefore all thermal processing steps above 400°C were avoided after laser annealing.

Results and Discussions

Ultrashallow junction can be achieved by using low implantation energies. The increasing of the laser energy density results in the increase of surface temperature [9] and for energies above 1000 mJ/cm² the surface degradation is present and can be correlated to the increasing of the surface roughness [10,11]. With a thin a-Si implanted layer above c-Si, the melting of a-Si occurs earlier than c-Si because the a-Si melting temperature is approximately 300°C lower than c-Si. When the sample is exposed to the laser light the a-Si layer starts melting and the melting depth is propagated until it reaches the c-Si interface. Once the c-Si surface is reached, the c-Si interface (which has higher melting temperature than a-Si) becomes the seed layer for recrystallization and an epitaxial layer is formed. If the c-Si melting temperature is reached the melting depth can be extended deeper.

A secondary ion mass spectrometry (SIMS) spectrum of the samples implanted with a dose of 10¹⁵ ions/cm² for different tilt angles (7°, 30° and 45°) and laser annealed at 1000 mJ/cm² is shown in Figure 2. Cross-sectional TEM image of the laser annealed junction with As⁺ ions implanted at 45° tilt is shown in Figure 3.

Figure 2. SIMS profile of As⁺ implanted with 5 keV to a dose of 10¹⁵ at/cm² with tilt angles of 7, 30 and 45 degrees and laser annealed at 1000 mJ/cm².

Figure 3. Cross-sectional TEM image of the edge of the laser annealed junction, 1000 mJ/cm² anneal and a 45° implantation tilt.

As can be seen from SIMS analysis, by implanting ions at higher tilt angles the junction depth is reduced. This is in accordance with the fact that the implantation depth will be smaller but also a loss of implanted dose coming from more ions reflecting from the silicon surface is revealed. Ultrashallow junctions with depths of 20, 18 and 15 nm are observed for 7°, 30° and 45° implantation angles, respectively. The TEM analysis suggests that some point defects remain at the edge of the junction since this region is darker than the surrounding Si. This could be a source of higher leakage along the diode perimeter [12]. The sheet resistances of all samples with laser energy varying from 750 mJ/cm² to 1000 mJ/cm² in 50 mJ/cm² steps are shown in Figure 4(a). The averaged sheet resistances are shown in Figure 4(b).

(a)

(b)

Figure 4. (a) Sheet resistances of all samples with laser energy varying from 750 mJ/cm² to 1000 mJ/cm² in 50 mJ/cm² steps. The lowest spread can be observed over the wafer annealed at 1000 mJ/cm². (b) Averaged sheet resistances.

As evidenced by the decrease in sheet resistance, higher levels of dopant activation and/or deeper junctions are obtained at higher annealing energies. Moreover, the lowest spread can be observed over the wafer laser annealed at 1000 mJ/cm² and the spread increases as the laser energy density is reduced. The minimum sheet resistance values of 220, 275 and 311 Ω/square are achieved at 1000 mJ/cm² for ions implanted at 45°, 30° and 7° tilt angles, respectively. The larger sheet resistances at higher tilt angles are expected from the lower junction depth and a loss of implantation dose evident in SIMS analysis. Table I summarizes the obtained SIMS and sheet resistance results and shows the trade-off between the junction depth and sheet resistance offered by implantation angle.

Table I. Summary of the low energy arsenic implants. Average sheet resistance (R_s) is given.

Laser energy density (mJ/cm ²)	Nominal dose (at./cm ²)	SIMS dose (at./cm ²)	Implantation (tilt angle)	Junction depth (nm)	Implantation dose (at./cm ²)	Sheet resistance avg. (Ω/square)
1000	1 E15	1.05 E15	7°	20	1.05 E15	220
1000	1 E15	7.98 E15	30°	18	7.98 E15	275
1000	1 E15	7.43 E15	45°	15	7.43 E15	311

Following the International Technology Roadmap for Semiconductors (ITRS) [1], junction depth of 7.7 nm for drain extension X_j and 16.9 nm for contact X_j , sheet resistance values of less than 1060 Ω/square (for drain extension) will be required for technologies below 32 nm node. Our results can fulfil the ITRS requirements for the next technology nodes. The summary of these requirements are shown in Table II.

Table II. ITRS 2008 (update) requirements for junction depth and sheet resistance [1].

Year of Production	2007	2008	2009	2010	2011	2012	2013	2014	2015
MPU Physical Gate Length (nm)	32	29	27	24	22	20	18	17	15
Contact X_j (nm) for bulk MPU/ASIC	35.2	32	29	26.7	24.7	22	19.8	18.6	16.9
Drain extension X_j (nm) for bulk MPU/ASIC	11	11	11	11	11	10	9	8.5	7.7
Maximum drain extension sheet resistance for bulk MPU/ASIC (NMOS) (Ω/sq)	650	670	660	680	750	810	900	960	1060

The state of the silicon surface before low-energy implantation is critical for the quality of the ultrashallow laser-annealed junctions. An excessive dry etching step landing on the silicon surface during the contact window opening can damage the silicon surface increasing the roughness. Additionally, for high-quality diodes, native oxide needs to be removed also before implantation since its roughness increases nonuniformities of the implanted profiles, which in turn disturbs the perfection of the epitaxial regrowth during the laser recrystallization process and this leads to increased leakage [7]. Therefore, the optimum contact-window etching includes a highly selective etching step in some HF-solution for landing on silicon or a dry etching step with reduced power, i.e. “soft landing” on silicon, in combination with the pre-implant dip in HF or buffered-HF solution to remove native oxide and create a hydrogen passivation of the Si surface. However, wet etching steps also remove isolation oxide in the lateral direction and cause enlargement of contact windows, potentially increasing the leakage current at the perimeter of the diodes if the junction is exposed or moved too close to the contact window perimeter.

Near-ideal diode characteristics have in the past been achieved with a 300 nm thermal oxide isolation layer [7], which is recessed about 25 nm in the 4 min HF (0.55%) HF dip-etch step. To operate in a lower thermal budget of the isolation layer, LPCVD oxide deposited at 700 °C was tested as a replacement of the thermal oxide. However, this type of oxide is recessed 75 nm in the dip-etch step, which proved to be too much for a reliable isolation of the junction perimeter. As a compromise, the 30 nm thermal oxide plus 300 nm LPCVD oxide was investigated. The contact window is opened by dry etching with the soft landing on silicon surface (Figure 5(a)) and a short dip etch in buffered-HF (1:7) solution is performed for 15 seconds to remove the native oxide immediately before ion implantation. The short dip etch in BHF (1:7) solution removes isolation oxide in the lateral direction with different etch rates for thermal SiO_2 and LPCVD oxide and a first enlargement of the contact window is observed (Figure 5(b)). The implanted region is laser annealed followed by the 4 min HF (0.55%) dip-etch and a second enlargement can be observed (Figure 5(c)). Figure 6 shows the final diode structure and the TEM image of the contact window (right corner). A smaller enlargement of the contact window at the Si interface is observed due to the lower etch rate of thermal SiO_2 compared to LPCVD oxide and contact dimensions are preserved.

Figure 5. Zoom-in of the right corner contact window during the process fabrication. (a) contact window after dry etching ("soft landing" on Si) (b) BHF (1:7) dip etch, As⁺ implantation and excimer laser annealing. First enlargement of the contact window in the lateral direction (c) HF (0.55%) dip etch and metallization. Second enlargement of the contact window in the lateral direction.

Figure 6. TEM image of the right corner contact window.

In Figure 7 the I-V characteristics of the self-aligned laser annealed junctions are presented and low leakage current is observed, confirming there is no excessive perimeter leakage coming from the enlargement of contact windows. A high reverse leakage is observed for 7° tilt As⁺ implantation which can be related to a more critical alignment of the contact edges (corners) to the contact window increasing the leakage current. This situation is improved when the implantation tilt is changed from 7° to 30° as can be seen in I-V characteristics of n⁺p diodes in Figure 7. A minimum leakage current of 7.5×10^{-13} A is observed for a 30° tilt and 900 mJ/cm² laser energy density.

Figure 7. I-V characteristic of n⁺p self-aligned diodes.

Conclusions

It has been demonstrated that a laser-annealing only process can be used to create good quality n⁺p ultrashallow junctions that are implanted self-aligned to the contact window. When pure oxide windows are employed, the necessary wet dip-etching in HF requires that the etch rate of the oxide directly on Si is low enough to prevent exposure of the laser annealed junction at the window perimeter. A high implantation tilt angle can also be used with advantage to increase the overlap of the implant with the window perimeter and achieve much better diode characteristics than if a standard 7° tilt is used. Moreover, the junction depth can be significantly decreased when using high tilt angles: when going from 7° to 45° junction depth goes from 20 nm to only 15 nm while the sheet resistance goes from 220 Ω/square to 311 Ω/square. A minimum leakage current of 7.5×10^{-13} A (at 1V reverse bias) was observed for a 30° tilt and 900 mJ/cm² laser energy density. These properties make the ELA technique an interesting candidate for the fabrication of future MOSFET devices.

Acknowledgements

The authors would like to thank staff of the DIMES IC-processing group for their support. This work has been supported by the EU FP6 project D-DotFet.

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