A Front-end ASIC with High-Voltage Transmit Switching and Receive Digitization for Forward-Looking Intra-Vascular Ultrasound

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Master of Science Thesis

A FRONT-END ASIC WITH HIGH-VOLTAGE TRANSMIT SWITCHING AND RECEIVE DIGITIZATION FOR FORWARD-LOOKING INTRA-VASCULAR ULTRASOUND

by

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ABSTRACT

This thesis discusses the basic architecture, circuit implementation and measurements of a 4-cable front-end ASIC with high-voltage (HV) transmitting and receive digitization for Intravascular ultrasound imaging. It is the first ASIC that digitizes the received signals locally, allowing them to be transmitted in a robust digital form to an external imaging system.

The ASIC mainly contains three parts: the receive signal chain, the clock and data recovery circuits and the HV transmit switch circuits. The receive signal chain employs an energy-efficient inverter-based OTA in the analog front end (AFE) and a 60MS/s charge-sharing SAR ADC. The clock and data recovery circuits decode clock and data from the command line. The HV transmit switches are used to transfer the HV pulse generated in the imaging system to the selected transducer elements.

Several techniques are proposed to reduce the required number of cables. A multi-functional mixed-voltage command line is employed to combine the clock, the command data and the supply for the HV switch control circuits through pulse width modulation and amplitude modulation. The ADC output codes are transmitted through only 1 cable by means of load modulation.

A prototype has been implemented in a TSMC 0.18 μm HV CMOS process. The measurement results show that the prototype is able to transmit HV pulses and receive echo signal with only 4 cables. Besides, a B-mode image has been generated to show the imaging ability of the ASIC.

Keywords: Intravascular ultrasound, high-voltage switching, receive digitization, 4-cable.

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1

INTRODUCTION

1.1. BACKGROUND

1.1.1. INTRAVASCULAR ULTRASOUND

Intravascular ultrasound imaging is an important tool to monitor blood vessels, which is useful to diagnose coronary artery disease (CAD). In 2013, CAD was the most common cause of death globally [1]. CAD is mainly caused by atherosclerosis of the arteries which results from the narrowed and blocked coronary arteries due to the fatty deposits.

Figure 1.1: Comparison between normal artery and narrow artery [2]

Figure 1.1 shows the differences between a normal artery and a narrow artery. The lipid deposit of plaque will reduce blood flow rate, which would probably result in heart problems. The area of lipid deposit must be decreased to enable the arteries to carry more oxygen and nutrient-rich blood to the heart muscle. Therefore, the key thing is to localize the lipid deposit in the blood vessels. There are many ways to diagnose coronary artery disease, including baseline electrocardiography (ECG) [3], echocardiography [4], coronary angiography [5], magnetic resonance imaging (MRI) [6] and intravascular ultrasound (IVUS) imaging [7]. Among them, intravascular ultrasound (IVUS) and angiography are used to visualize the inside or lumen of the blood vessels. IVUS can not only show the lumen of the coronary arteries accurately but also the atheroma (membrane or cholesterol loaded white blood cells) hidden within the wall [7]. Therefore, it can help doctors to have a better understanding of the atherosclerosis process in living people in order to select proper treatment.

IVUS utilizes a catheter at the tip of which a miniature ultrasonic transducer is mounted. The transducer is used for pulse-echo measurement. It can be excited to transmit a pulse

and generates ultrasonic waves. When the ultrasonic waves reach the target tissues, an echo signal will be reflected back to the transducers. Piezo-electric transducers (PZT) or capacitive micro-machined ultrasonic transducers (CMUT) are used. The PZT converts electrical pulses to mechanical vibration which creates ultrasound waves in transmit mode. In receive mode, the mechanical vibrations are converted into electrical signals [8]. A CMUT is composed by a thin membrane which is sitting on top of a vacuum cavity and supported by sidewalls. The CMUT needs to be biased at a DC voltage. When there is an AC voltage applied, the CMUT will generate ultrasonic waves [9]. In receive phase when the CMUT receives the echoes, the echoes result in the membrane vibrations which will be converted into electrical current.

The other side of the catheter is connected to a computer-based imaging system. An example of a commercial IVUS imaging system is shown in Figure 1.2.

Figure 1.2: An example of the IVUS imaging system and the IVUS catheter [10].

The ultrasonic probe will be put into the vessels and capture the “information” on the vessel walls around the probe. This information, usually represented by analog signals in the voltage domain, will be transferred through the cable in the catheter to the imaging system.

1.1.2. ULTRASOUND TRANSMIT-RECEIVE CYCLE

In a typical ultrasound system, the pulse-echo measurement is time-interleaved into two phases, the transmit (TX) phase and the receive phase (RX), as shown in Figure 1.3. In the transmit phase, the TX transducer is driven by a high voltage pulser in order to generate transmit waves and the receive circuitry in the receive signal chain should be inactive. In the receive phase after some delay, the RX transducer is stimulated by the received echo signal the receive signal chain should be active to amplify the received signals.

Figure 1.3: Timing diagram of a typical transmit and receive cycle

In the IVUS imaging system, this type of pulse-echo operation is also applied.

1.2. PRIOR ART

In [11] and [12], a forward-looking IVUS imaging based on single transducer rotation system is proposed. However, the systems in [11] and [12] are costly and complex because they need mechanical rotation system. The nonlinearity of the rotation system can create some image artifacts. In order to eliminate the use of a complex rotation system, transducer-array based IVUS imaging systems are proposed in [13][14]. Figure 1.4 shows the block diagram of the IVUS imaging system proposed in [15].

Figure 1.4: A block diagram of the IVUS imaging system presented in [15].

Four 8-1 input multiplexers are employed to interface with 32 receive elements. Each channel is connected to an amplifier. The 24 transmit elements are directly connected

to cables. Some additional cables are necessary for the power supply and digital control signals. However, for catheter-based IVUS imaging system, the number of interconnection cables is constrained because of the limited catheter diameter (~ 2 mm).

Figure 1.5: A block diagram of the IVUS imaging system presented in [16].

In order to further reduce the required number of cables, an on-chip high voltage (HV) pulser is proposed in [16] to reduce the number of cables used for the transmit elements. The block diagram is shown in Figure 1.5. The HV pulser eliminates the need of cables for each transmit element by generating HV pulses on the chip. It requires only 1 cable (HV Supply). 4 cables are used for the signal outputs and additional cables are also necessary in digital control signals and power supply. Finally, this IVUS imaging system only requires 13 cables. In [17], the number of required cables is reduced to 9 by further multiplexing the receive channels which reduces the number of analog outputs from 4 to 1. However, 9 cables are still a lot for the IVUS application.

1.3. OBJECTIVES

The IVUS imaging systems proposed in [15][16][17] are all using analog output. In order to transfer the analog signal through the coaxial cable, a cable driver or buffer is required to match the cable impedance characteristics for certain bandwidth requirements, which means that the cable driver could be the most power-hungry block. Another drawback is that the analog signal is sensitive to interference (e.g., coupling from the digital signals). A direct solution is to locally digitize the received analog signal and then transmit digital code through the coaxial cable. In order to keep the total cable counts same, all the signals (there are 11 signal outputs for a 10b ADC, 10 for the parallel data and 1 for the data ready signal) from the ADC must be transmitted through only 1 coaxial cable. The number of cables for digital control signals can also be reduced by

combining multiple functions into one cable, which can be done via various modulation schemes (e.g., amplitude shift keying [18][19], phase shift keying[20]).

The latest publication on IVUS has achieved a 9-cable implementation [17]. The goal of this work is to reduce this to only 4 (one cable for the signal output, one cable for the digital control signals, one cable for the HV pulse generator and one cable for the power supply).

Table 1.1 lists the target specification of the prototype front-end ASIC.

Table 1.1: Design Targets of Prototype

	[16]	[21]	This work
Process	0.35 μ m HV CMOS	0.35 μ m HV CMOS	0.18 μ m HV CMOS
Supply voltage	3.3V	3.3V	1.8V
#Transmit	56	64	16
#Receive	48	64	64
Receive output	analog	analog	digital
Receive bandwidth	40MHz	n/a	>10MHz
Max.transmit amplitude	25V	12.5V	30V
Power consumption	20mW	n/a	<20mW
#Cables	13	13	4

1.4. THESIS ORGANIZATION

This thesis presents a 4-cable front end ASIC with in-probe digitization for intravascular ultrasonic imaging, including basic architecture, prototype implementation and experimental results. Apart from this introductory chapter, the rest of this thesis is divided into six chapters.

Chapter 2 contains the architecture of the receive signal chain, including analog front end (Low noise pre-amplifier, time-gain compensation stage, ADC driver and a 10b 60MS/s SAR ADC). A data transmission scheme is proposed to transfer the ADC data through only 1 cable.

Chapter 3 illustrates the working principle and circuit implementation of the high voltage switches.

Chapter 4 discusses the clock and data recovery circuits which aim to reduce the required cables for shift register from 3 to 1 by embedding the data into the clock signal, Besides, the control signals for the high voltage control circuit are also embedded.

Chapter 5 briefly introduces the prototype implementation of the ASIC's sub-blocks and the chip layout.

Chapter 6 describes the electrical measurements and the acoustical measurements.

Finally, chapter 7 summaries the contributions of this thesis.

2

RECEIVE SIGNAL CHAIN

THIS chapter discusses analog front end (AFE), ADC and load modulation. It includes three main parts. The first part is the discussion on the different stages in the AFE and the architecture of the OTA used in the AFE. The second part describes the ADC architecture and its different build blocks. Finally, the load modulation that is used to transmit the ADC's output code is discussed.

2.1. TRANSDUCER CHARACTERISTICS

Figure 2.1: Simulated Impedance Characteristics of Transducer

Figure 2.2: Impedance characteristics: extracted model (solid line) versus simulated model (dashed line)

Figure 2.1 shows the simulated impedance characteristics. In order to acquire the parameters of the lumped-element impedance model, we use ZView [22] for data fitting and model extraction (Figure 2.2).

The extracted model is shown in Figure 2.3, which includes a serial RCL branch and a shunting capacitor. The extracted values for the model parameters and the fitting errors are also shown in Figure 2.3. Some important specifications of the analog front end are determined from the impedance characteristics, for instance, input referred noise, bandwidth, input impedance.

Figure 2.3: Transducer Lumped-element impedance model and values of parameters

Table 2.1 summarizes the transducer signal characteristics. There are some difference between the value of extracted R_s (23.6kΩ) and the simulated element impedance (38kΩ) at 14MHz. This is because of the fact that the resonant frequency calculated from the extracted model ($f = 1/(2\pi\sqrt{LC})$) is around 12MHz which is smaller than the resonant frequency in simulation (14MHz).

Table 2.1: Summary of transducer signal characteristics

Specification	Target
Operational frequency	14MHz
Element Impedance at 14MHz	38kΩ
-3dB Bandwidth	40%
Dynamic Range	50dB

2.2. SIGNAL CHAIN ARCHITECTURE

Figure 2.4 shows the block diagram of the signal chain which contains AFE, ADC and load modulation module.

The transducer resonant frequency is around 14MHz and the impedance around that

Figure 2.4: The block diagram of signal chain

frequency is approximately $38\text{ k}\Omega$. In order to readout $>90\%$ signal from the transducer, the input impedance of the analog front end around 14 MHz should be 10 times less than $38\text{ k}\Omega$ when reading out signal current or be 10 times larger than $38\text{ k}\Omega$ when reading out signal voltage. The 14 MHz central frequency and 40% bandwidth translate to a 5.6 MHz bandwidth (from 11.2 MHz to 16.8 MHz). Obviously, the bandwidth of the AFE needs to cover this bandwidth. Therefore, the target analog front end bandwidth is $>5\text{ MHz}$. The target dynamic range of the signal chain is 50 dB . In order to leave some margin, a 10bit ADC whose dynamic range is 60 dB in the ideal case is suitable for this design. Besides, a variable gain amplifier can also be designed to obtain more dynamic range [23]. Because the transducer signal is a wide band signal with a central frequency of 14 MHz , the sampling rate of the ADC is chosen to be 60 MHz , which is larger than 4 times of receive signal central frequency to enable accurate pulse timing. Another important parameter to decide is the gain of the analog front end, which should be determined by the system input referred noise requirements and the maximum input signal level. The total input referred noise is comprised of two parts: amplifiers noise and ADC noise, which can be expressed as.

$$V_{n,SignalChain}^2 = V_{n,amp}^2 + \frac{V_{n,ADC}^2}{A^2} \quad (2.1)$$

Where $V_{n,SignalChain}$ is the total input referred noise, $V_{n,amp}$ is the input referred noise of the AFE, $V_{n,ADC}$ is the ADC noise and A is the gain of the AFE. The input referred noise of signal chain $V_{n,SignalChain}$ should be smaller than the noise of transducers $V_{n,Transducer}$.

In addition, the gain A should be high enough to attenuate the noise of ADC in order to make the system thermal-noise-dominant. The noise of the transducer $V_{n,Transducer}$ is mainly produced by the resistor in lumped-element impedance model, which is $23\text{ k}\Omega$ (corresponds to $0.85\text{ pA}/\sqrt{\text{Hz}}$). Apart from the noise, the gain will also affect the amplifier output swing and ADC input range $V_{in,ADC}$.

$$V_{inTransducer} = \frac{V_{in,ADC}}{A} \quad (2.2)$$

Larger output swing means larger input signal the circuits can handle which means larger dynamic range. However, the output swing of the amplifier is limited by the supply voltage, amplifier architecture, and linearity requirements. Based on the transducer

noise and dynamic range requirement (50dB), the estimated maximum peak-to-peak input signal is about $1.7\mu A$. Assuming the full scale of ADC input signal is $1V$ which is a reasonable value for an amplifier under $1.8V$ supply, the estimated required gain of the signal chain is $115dB\Omega$.

The quantization noise of the ADC (a 10 bit ADC with a full scale of $1V$) is about $\sqrt{\frac{1}{12}} V_{LSB}$ which is approximately $280\mu V_{rms}$. If considering some related thermal noise, the estimated noise of the ADC is $500\mu V_{rms}$. Therefore, eq. 2.1 will be translated to eq. 2.3, leading to the required amplifier noise of $1.76nA_{rms}$.

$$V_{n,SignalChain}^2 = V_{n,amp}^2 + \frac{500\mu V_{rms}^2}{115dB\Omega^2} < V_{n,Transducer} = 1.9nA_{rms} \quad (2.3)$$

A summary of signal chain performance design target is shown in Table 2.2

Table 2.2: Performance Specification of Signal Chain

Specification	Target
Supply Voltage	1.8
Dynamic Range	>50dB
Bandwidth	>5MHz
ADC Sampling Frequency	60MHz
ADC Resolution	10Bit
IRN of AFE	$1.76nA_{rms}$
Gain of Signal Chain	$115dB\Omega$

IRN: Input Referred Noise

Based on above analysis, the key parameters (input referred noise, signal chain gain, ADC sampling rate, resolution and bandwidth) of a signal acquisition system are determined. Another important parameter, the power consumption, should be minimized.

2.3. ANALOG FRONT END

As discussed in Section 2.2, the requirements of gain, bandwidth and noise have been determined. The transducer impedance characteristic is also known. Figure 2.5 shows the architecture of analog front end. It contains a low noise amplifier (LNA), a flipped voltage follower (FVF) and a variable gain amplifier (VGA).

2.3.1. LOW NOISE AMPLIFIER

The low noise amplifier is the first stage of the signal chain and it should provide enough gain to attenuate noise from later stages and generate low enough noise to be able to see the transducer signal noise floor. As mentioned in section 2.1, the transducer has an

Figure 2.5: Architecture of Analog Front End

impedance of $38k\Omega$ at the resonant frequency which is a relatively large value. Therefore, a trans-impedance amplifier, which usually has a small input impedance, is more suitable compared to a voltage amplifier. Figure 2.6 shows the block diagram of a TIA.

Figure 2.6: Block diagram of the trans-impedance amplifier

The feedback capacitor C_F is used to limit the bandwidth and load capacitor C_L is the input capacitance of the next stage and the intrinsic parasitic of the OTA. The signal current that flows into the TIA can be expressed as:

$$I_{in} = I_{source} \frac{Z_{source}}{Z_{source} + Z_{in}} \quad (2.4)$$

If $Z_{source} > 10Z_{in}$, approximately 90% of signal current will flow into the TIA. Therefore, the requirement for the Z_{in} is:

$$Z_{in} = \frac{R_F}{A_o(1 + j\omega R_F C_F)} < 3.8k\Omega \quad (2.5)$$

Where A_o is the open-loop gain of the OTA.

The available architectures for the OTA include telescopic, folded cascode and inverter based OTA. For low power design, the inverter based OTA is preferred because it has two times current efficiency compared to the other two architectures although the output swing is smaller [24]. In this design, the inverter-based OTA is applied. Figure 2.7 shows the single-ended and differential architecture. Both architectures have been employed

Figure 2.7: Differential and single-ended inverter-based OTA

in integrators for sigma-delta modulators [25][26][24] and preamplifiers for bio-medical applications [27][28]. There are two main differences between the single-ended version and the differential version. The first is that the biasing of the differential one is determined by the tail current sources Mp and Mn, and the biasing of the single-ended one is set by the DC biasing of the input signal, the size of M5 and M6 and the supply, which makes this architecture hard to achieve the PVT-insensitive biasing. The split capacitor technique has been employed to bias M5 and M6 separately [29], but the required capacitor will increase the circuit area. Another difference is that the differential OTA has a better PSR (Power supply rejection) compared to the single-ended one, not only because of the fully differential operation but also because of the tail current source Mp and Mn. Considering that the TIA is a noise-sensitive stage [30], the differential OTA with the higher PSR is preferred although a larger current needs to be burned to achieve the same transconductance.

The bandwidth and transimpedance of the TIA in Figure 2.6 can be expressed by eq. 2.6 and eq. 2.7

$$BW_{TIA} \approx \frac{1}{2\pi R_F C_F} \quad (2.6)$$

$$Gain_{TIA} \approx \frac{R_F}{1 + j\omega R_F C_F} \quad (2.7)$$

Figure 2.8 shows the main noise sources of the TIA which include OTA noise $V_{n,OTA}^2$ and noise of feedback resistor V_{n,R_F}^2 .

Figure 2.8: Noise source in a resistive feedback TIA

The equivalent input referred current noise can be calculated by:

$$i_{in}^2 = V_{n,OTA}^2 (\omega C_p)^2 + V_{n,OTA}^2 / \left(\frac{R_F}{1 + j\omega R_F C_F} + \frac{1}{j\omega C_L} \right)^2 + \frac{4kT(1 + j\omega R_F C_F)^2}{R_F} \quad (2.8)$$

The noise generated by feedback resistor is attenuated by the TIA close-loop gain and the parasitic capacitance increases the noise contribution of the OTA noise. Therefore, based on eq. 2.8, increasing feedback resistor and reducing parasitic will help to reduce the input referred noise but will decrease the close loop bandwidth (see eq. 2.6).

2.3.2. TIME GAIN COMPENSATION

Time gain compensation is used to compensate for propagation attenuation [31]. The basic principle of an ideal case is shown in Figure 2.9. With the wave propagation, the received echo signal will decrease with time because of propagation attenuation. In order to compensate for this, a stage whose gain is increasing with time is employed, which generates a uniform signal amplitude versus time. This stage is the so-called time gain compensation (TGC) stage. TGC can help to increase the overall dynamic range of the receive circuitry. For instance, if the dynamic range of the transducer receive signal is 60dB,

10dB of which is due to propagation attenuation, the receive signal chain only needs a 50dB dynamic range amplifier and a time gain compensation stage with the 10dB gain step.

Figure 2.9: Basic principle of ideal time gain compensation

Figure 2.10: Time gain compensation with 3 discrete gain steps

However, designing a TGC stage whose gain increase continuously complying with the propagation attenuation needs a complicated design. Therefore, three discrete gain step are applied in this design as shown in Figure 2.10

Figure 2.11 shows the block diagram of the TGC stage. In this design, a 12dB gain step TGC stage is designed. The time gain compensation stage is implemented with an inverter-based OTA and a capacitive feedback network, in which the gain is set by the ratio of capacitors. The three gain steps 6dB, 12dB and 18dB are controlled by two switches which correspond to two bits in the shift register. The architecture of the OTA is the same as the one used in the TIA.

The input capacitance of the TGC stage will be 800fF (if a 100fF C_u is applied) which will be the load capacitance of the proceeding stage: the TIA. In order to reduce the TIA loading, a buffer stage is employed between the TIA and the later stage. There are two types of source follower which are shown in Figure 2.12.

Compared to conventional source follower, the flipped voltage follower has better cur-

Figure 2.11: Block diagram of time gain compensation stage

Figure 2.12: Basic source follower and flipped voltage follower

rent sink and source capabilities [32]. The output impedance of the FVF is approximately $r_{o,FVF} = 1/(g_{m1}g_{m2}r_{o1})$ which is smaller than that of a PMOS source follower.

2.4. ADC

2.4.1. OPERATION OF AN SAR ADC

The operation of an SAR ADC is based on a binary search algorithm. The principle of the binary search algorithm is shown in Figure 2.13.

The basic operation is to halve the search range each time and then compare V_{in} with

Figure 2.13: Successive approximation based on binary search algorithm

Figure 2.14: Block diagram of a N-bit SAR ADC

V_{dac} to determine the next step. This procedure is repeated until all steps are finished. Due to the limited steps, there must be some differences between V_{dac} and V_{in} after the SAR operation finishes, which is the so-called quantization error.

The main building blocks of an SAR ADC are shown in Figure 2.14. It contains a track and hold block, a DAC, a comparator, digital controllers. The track and hold circuit first samples the input signal V_{in} , and then holds it during the SAR operation. The dynamic comparator will amplify the difference between the inverting and the non-inverting inputs, which correspond to the input signal and the signal of the DAC output, respectively. Based on the comparison result, the digital controller will generate a code 1 or 0 and the control signals for the DAC. This procedure will be repeated until all the SAR cycles finish. The timing diagram is also shown in Figure 2.14. There are two clocks, F_s and F_{comp} . F_s

is used to control the sampling switch in the T/H circuit and F_{comp} controls the dynamic comparator and digital control circuitry. F_{comp} is approximately N time of F_s , where N is the resolution of the ADC.

2

2.4.2. OVERVIEW OF CHARGE SHARING SAR ADC

A number of SAR ADCs have been proposed in recent years, the resolution of which varies from 8b to 10b [33][34][35][36]. Besides, the SAR ADC has also been applied in pipeline ADCs leading to the so-called pipelined SAR ADC [37][38][39], and in high speed time-interleaved ADCs [40][41]. The low power and low voltage features lead to the popularity of the SAR ADC, and it also allows asynchronous operation which eliminates the need of external high-frequency clock source and thus reduces the system complexity.

Figure 2.15: charge redistribution SAR and charge sharing SAR [42]

Conventional SAR ADCs require power-hungry reference buffers to ensure adequate DAC settling speed and accuracy. For example, the time available for the DAC settling is only 2ns for a 10bit 50MHz SAR ADC. Besides, a large CDAC is also required which means large area and large loading capacitance to the proceeding state, e.g., a 10bit CDAC needs $1024C_u$.

In [43], a charge sharing SAR ADC (CSSAR) is proposed. Figure 2.15 shows the comparison between the charge redistribution SAR ADC and the charge sharing SAR ADC. For the CSSAR ADC, the input signal is first sampled on two sampling capacitor C_s in the sampling phase and in the meanwhile, the DAC is precharged to a reference voltage. In the holding phase or the SAR operation phase, the C_s is connected with the CDAC. According to the comparison results, the signal charge which is stored on C_s will be added or subtracted with a binary weighted charge. This procedure is repeated until all the pre-charged capacitors are connected to the C_s . Therefore, the quantization unit for the CSSAR is the charge rather than the voltage. The biggest advantage of the CSSAR ADC is

that it does not require power hungry reference buffers during the SAR operation phase. The reference voltage has been pre-charged into the CDAC in the sampling phase. Although a buffer is also required to pre-charge the CDAC, the time available to charge the CDAC is longer compared to the time of each SAR operation which releases the bandwidth requirement.

2.4.3. CHARGE SHARING CDAC

The CDAC of the charging sharing SAR is shown in Figure 2.16 [43]. The CDAC contains a 7b binary CDAC and a 3b unary CDAC to form a 10b CDAC. The charging of the binary DAC is controlled by the pre-charge signal. The unary DAC generates three LSBs by four control signals: *share1*, *share2* and *share3*. The timing diagram of these control signals is also shown in Figure 2.16.

Figure 2.16: CDAC of charge sharing SAR ADC [43]

When *Pre-charge* is valid, the binary CDAC is charged by V_{ref} and the unary CDAC is reset. The total charge stored on CDAC is

$$Q_{total} = 64CV_{ref} \quad (2.9)$$

The *Pre-charge* phase is also the sampling phase of ADC. After the *Pre-charge* phase, the SAR operation starts. When the MSBs are being decided, the charges that are used for the last 3 LSBs will be generated. The *Share1* is valid first. It connects C_3 and C_2 which starts the first charge sharing. The charged stored on C_3 during the *Pre-charge* phase will be halved:

$$Q_{C_3} = Q_{C_2} = \frac{1}{2}CV_{ref} \quad (2.10)$$

Then, *Share1* becomes low to disconnect C_3 and C_2 . After some delay, *Share2* turns to high to connect C_2 and C_1 which triggers another charging sharing. The charge on C_2

and C_1 are:

$$Q_{C_2} = Q_{C_1} = \frac{1}{4} C V_{ref} \quad (2.11)$$

Similarly, the third charge sharing operation triggered by *Share3* redistributes the charge on C_1 and C_0 to:

$$Q_{C_1} = Q_{C_0} = \frac{1}{8} C V_{ref} \quad (2.12)$$

If we quantize the charges on each capacitor with the minimum charge which is shared on C_1 and C_0 and note it Q_u :

$$Q_u = \frac{1}{8} C V_{ref} \quad (2.13)$$

The charge stored on each capacitor is $Q_u, Q_u, 2Q_u, 4Q_u \dots 256Q_u$, which is exactly a 10b binary weighted *Charge DAC*.

However, the parasitic of the capacitors and the switches will affect the accuracy of the 3LSBs charge. Figure 2.17 shows the charge sharing model including the parasitics.

Figure 2.17: Charge sharing model including the parasitics

After the pre-charging phase, the charge stored on the capacitor is:

$$Q_1 = V_{ref}(C + C_{p1}) \quad (2.14)$$

During the charge sharing phase, the charge Q_1 is shared through R_{on} . Because of the parasitic capacitance C_{p1} and C_{p2} , the charge stored on the two capacitance will be:

$$Q_1 = \frac{C + C_{p1}}{1 + \frac{C + C_{p2}}{C + C_{p1}}} V_{ref} \quad (2.15)$$

$$Q_2 = \frac{C + C_{p2}}{1 + \frac{C + C_{p1}}{C + C_{p2}}} V_{ref}$$

In the ideal case, Q_1 and Q_2 should both equal to $\frac{1}{2}CV_{ref}$. In order to reduce the effect of the parasitics, the value of the capacitor should be increased while the size of the switches should be decreased which, in turn, will degrade the DAC settling speed.

The required number of unit capacitors for the CDAC is only 67 compared to 1024 in the conventional CDAC. Therefore, the area of the CDAC is reduced dramatically. Assuming the reference voltage is V_{ref} and the unity capacitor is C_u , the total charge stored on the CDAC is:

$$Q_{CDAC} = 64C_u V_{ref} \quad (2.16)$$

The full-scale input charge which could be quantized by the charge in the CDAC is $-2Q_{CDAC}$ to $2Q_{CDAC}$. The full-scale input charge can also be expressed as $V_{in,FS}C_s$. Therefore, the relationship between C_s , C_u , $V_{in,FS}$ and V_{ref} is:

$$4Q_{CDAC} = 256C_u V_{ref} = V_{in,FS}C_s \quad (2.17)$$

If C_u is chosen as 30fF and C_s is 2pF, according to eq. 2.17, we get:

$$V_{in,FS} = 4V_{ref} \quad (2.18)$$

Figure 2.18 illustrates the CDAC unit [43]. CN_x and CP_x are the control signals from digital SAR logic which is used to decide to add or subtract charge to or from the CDAC. After the finishing of the CDAC settling, the V_{comp} and V_{comp} will be updated and next decision will also be updated when the rising edge of the comparator clock comes.

Figure 2.18: Control details of a CDAC unit [43]

2.4.4. CAPACITOR MISMATCH

The bottleneck of the achievable resolution of the SAR ADC is determined by capacitor mismatch. Capacitor mismatch can be modeled as.

$$\frac{\sigma_{\Delta C}}{C} = \frac{A_C}{\sqrt{C}} \quad (2.19)$$

Figure 2.19: Maximum achievable resolution versus standard deviation of unit capacitor $\sigma(C)/C$ [44]

where the $A_C = 2.27\% \sqrt{fF}$ in TSMC $0.18\mu\text{m}$ Technology [45]. This model shows that the accuracy is proportional to the area.

According to the plot shown in Figure 2.19, in order to reach the 10b resolution, the required standard deviation of $\sigma(C)/C$ should be 0.7% to 0.8% which can be translated to a capacitor value of 10.5fF.

2.4.5. ADC DRIVER

An ADC driver needs to drive the ADC sampling capacitors. In order to ensure enough settling, a powerful driver amplifier is required. The settling accuracy and speed of the sampling signal is related to four parameters: output impedance of the ADC driver, sampling time, on-resistance of the sampling switches and the value of the sampling capacitor.

Figure 2.20 shows the ADC driver with a feedback factor of β and a G_m cell and an ideal sampling switch.

The close-loop bandwidth of the ADC driver is shown as follows:

$$BW = \frac{\beta G_m}{C_s} \quad (2.20)$$

Figure 2.20: Block diagram of an ADC driver, sampling switch and sampling capacitor

In order to achieve desired settling accuracy, the sampling period T_s should be larger than M times of the settling time constant:

$$T_s > M\tau = M \frac{C_s}{\beta G_m} \quad (2.21)$$

Where N varies from 7 to 10 for settling accuracies ranging from 0.1% to 0.005%. For a 10b ADC, the required settling accuracy is 0.1%.

Figure 2.21: Block diagram of ADC driver with a gain of 2

From eq. 2.21, a larger closed-loop gain means a larger settling time constant. Therefore, the ADC driver should not be designed to have too much gain, but some gain in this stage helps to reduce the noise contribution of the ADC noise. In this thesis, a gain of 2 is chosen for the ADC driver. The block diagram of the ADC driver is shown in Figure 2.21.

Figure 2.22 shows the basic fully differential sampling network. V_{inp} and V_{inn} are the ADC driver outputs. Based on the ADC driver settling analysis in eq. 2.21, the required G_m of the ADC driver is inversely proportional to the sampling period. A longer sampling period means a smaller required G_m and thus lower power consumption. However, longer sampling period also means shorter hold period which requires a faster and power-hungry SAR logic and comparator. Therefore, there is a trade-off in power consumption between the power consumption of the ADC driver and the power consumption of the digital logics (SAR logic + Comparator).

Time-interleaved sampling can be employed to obtain more sampling time and eliminate this trade-off [46] by time-interleaved the sampling period and the period for the SAR operation. Figure 2.23 shows the two paths of a time-interleaved sampling network. It requires two times of sampling switches and capacitors and a pair of the non-overlapping sampling clock.

Figure 2.23: Two-path Time-interleaved sampling network

Apart from the length of the sampling period, the values of on-resistance of MS and MH are also critical. A smaller on-resistance results in a smaller time constant. In order to reduce switch on-resistance, a bootstrapped sampling switch is applied [35], which can enlarge the over-drive voltage and also keep it constant which makes the switch on-resistance independent on the signal swing. The basic idea is shown in Figure 2.24.

Figure 2.24: Basic principle of bootstrapped switch

In phase 1, the NMOS switch is turned off and bootstrap capacitor C_{bs} is pre-charged to V_p . In phase 2, C_{bs} is connected to the source and the gate of NMOS switch. The voltage of the gate is bootstrapped to $V_{in} + V_p$ and the over-drive voltage will be kept constant and independent of the signal swing.

In the charge sharing SAR ADC, the DAC settling speed is determined by the switch on-resistance and the value of capacitors. The on-resistance of a NMOS switch can be expressed by.

$$R_{on} = \frac{L}{W\beta(V_{GS} - VT)} \propto \frac{1}{V_{DD} - V_{in}} \quad (2.22)$$

R_{on} is inverse-proportional to source or drain voltage V_{in} . Increasing the switch size can help to reduce R_{on} , but it will introduce more parasitic into the CDAC. Reducing common mode voltage (reducing the V_{GS} in eq. 2.22) of the signal also helps reduce the on-resistance. In [34], a dynamic common mode variation scheme is employed to reduce the common mode voltage during the DAC settling. The principle is shown in Figure 2.25.

In the sampling phase, for instance, when F_{s1} is high and F_{s2} is low, the bottom plate of C_{SH1} , C_{SL1} are connected to 1.8V and C_{SH2} , C_{SL2} are connected to ground. The total sampling charge is:

$$Q_p = (V_{inp} - 1.8)C_{SH1} + V_{inp}C_{SH2} \quad (2.23)$$

$$Q_n = (V_{inn} - 1.8)C_{SL1} + V_{inn}C_{SL2}$$

In the holding phase, the total charge can be expressed by:

$$Q_p = V_{outp}C_{SH1} + V_{outp}C_{SH2} \quad (2.24)$$

$$Q_n = V_{outn}C_{SL1} + V_{outn}C_{SL2}$$

$$\begin{aligned} V_{outp} &= V_{inp} - \frac{1.8C_{SH1}}{C_{SH1} + C_{SH2}} \\ V_{outn} &= V_{inn} - \frac{1.8C_{SL1}}{C_{SL1} + C_{SL2}} \end{aligned} \quad (2.25)$$
$$\begin{aligned}\Delta V_{cmp} &= V_{inp} - V_{outp} = \frac{1.8C_{SH1}}{C_{SH1} + C_{SH2}} \\ \Delta V_{cmn} &= V_{inn} - V_{outn} = \frac{1.8C_{SL1}}{C_{SL1} + C_{SL2}}\end{aligned}\quad (2.26)$$

Based on the above analysis, the common mode voltage will be reduced by $1.8 \frac{C_{SH1}}{C_{SH1} + C_{SH2}}$. For instance, if the total sampling capacitor is $2pF$, $(C_{SH1} + C_{SH2}) = 2pF$, and $C_{SH1} = 0.5pF$, the common mode voltage will be reduced by $0.45V$.

The value of the sampling capacitor C_s needs to be determined first. In eq. 2.17, multiple

trade-off problems can be seen. The choice of C_u also affects the choice of C_s , V_{ref} and the output swing of the proceeding stage $V_{in,FS}$. Because the power consumption should be minimized in this design and the value of C_s affects the power consumption of the proceeding stage, C_s should be minimized. Besides, the input full-scale signal $V_{in,FS}$ should be maximized in order to obtain the maximum dynamic range.

The $V_{in,FS}$ is also the output swing of the ADC driver, which is limited by the applied architecture of the OTA. For the cascode inverter-based OTA, assuming the V_{ds} of the two tail current source is 300mV and the V_{ds} of the input transistor and the cascode transistor is 100mV, the differential output swing is approximately 800mV. Based on the previous capacitor mismatch analysis, the minimum requirement of the unit capacitor is 10.5fF. However, in the standard library cell of this technology, the minimum mom cap is 25fF. Besides, as discussed in Section 2.4.3, the large unit cap helps reduce the effects of switch parasitic although it degrades the settling speed. As a trade-off between these factors, a unit capacitor of 32fF is chosen. Finally, according to eq. 2.17, a reference voltage of 0.2V and the sampling capacitor of 2pF is chosen. In order to leave some margins for the dynamic range, a reference voltage of 0.3V, which corresponds to an input full-scale signal of 1.2V, is chosen. Table 2.3 summarizes the parameters of the ADC.

Table 2.3: Summary of Design Parameters of the SAR ADC

Item	Value
Unit cap	32fF
Reference Voltage (V_{ref})	0.3V
Sampling cap	2pF ($C_{S1} = 1.5\text{pF}$, $C_{S1} = 0.5\text{pF}$)
Optimized Input Full Scale	800mV
Maximum Input Full Scale	1.2V

2.4.7. COMPARATOR NOISE, OFFSET AND SPEED

Figure 2.26 shows the digram of CSSAR ADC with comparator offset.

In order to avoid decision errors, the offset voltage V_{os} and the input referred noise of the comparator should be less than 1LSB in the conventional charge redistribution SAR ADC. However, the quantization unit of the CSSAR is charge. Therefore, in order to evaluate the requirements for the comparator offset, the charge LSB should be convert into voltage domain. For the CDAC shown in Figure 2.16, the charge LSB is:

$$Q_{LSB} = \frac{256C_u V_{ref}}{2^{10}} = \frac{C_u V_{ref}}{4} \quad (2.27)$$

Due to the charge sharing, the charge LSB is shared by the sampling capacitor and the CDAC. Therefore, the LSB in voltage domain is.

Figure 2.26: The diagram of a charge sharing SAR ADC with comparator offset

$$V_{LSB} = \frac{Q_{LSB}}{C_S + C_{DAC}} = \frac{C_u V_{ref}}{4(C_S + C_{DAC})} \quad (2.28)$$

The 32fF C_u , 0.3V V_{ref} and 2pF C_{DAC} result in a LSB voltage of 0.6mV. Both comparator offset and input referred noise should be less than 600 μ V.

Apart from the noise and offset, the comparator should be fast enough to insure that the 10-step SAR operation can finish several ns before the next sampling period starts. Figure 2.27 shows the comparator speed analysis.

Figure 2.27: Comparator Speed Analysis

The total time available is 16.6ns. 1ns is used for the pre-charging of the CDAC and another 1ns is used for the DataRdy signal. The remaining 14.6ns is used for the SAR operation which leads to 1.46ns for each SAR operation step. Within 1.46ns, the comparator needs to finish the decision, the SAR logic and the DAC settling also need to be finished.

the requirement for the comparator speed, the SAR logic speed and the DAC settling speed is:

$$t_{comp} + t_{logic} + t_{dac} < 1.46ns \quad (2.29)$$

A trade-off problem is seen from eq. 2.29. The three terms in eq. 2.29 affect the power consumption of the comparator, the power consumption of the SAR logic and the switch and capacitor size in the CDAC. Although it is hard to quantitatively optimize the overall performance, a rough requirement of the comparator speed can be obtained by equating the three terms, which leads to:

$$t_{comp} < 1.46ns/3 \approx 480ps \quad (2.30)$$

2.5. ADC DATA TRANSMISSION

In order to transmit the 11b ADC code (10b ADC Data and 1 Data Ready signal) through one cable, the data needs to be serialized and encoded. Figure 2.28 shows an example of a basic synchronous data transmission system.

Figure 2.28: An example of data transmission system

A high-speed clock signal is required to serialize and encode data. For example, a 60MHz 10b ADC output code needs at least 600MHz to serialize them which means an additional block: DLL or PLL, needs to be designed to derive this high-frequency clock from the sampling clock, or the high-frequency clock needs to be sent to the ASIC from the system. Besides, a coding system is also preferred to encode the clock into the data stream, for example, the manchester coding [47]. A power-hungry driver is used to drive the large load capacitance of the cable.

Rather than transmitting the data synchronously, a simpler and more power-efficient asynchronous scheme is proposed. As discussed in Section 2.4, the SAR logic generates the ADC output codes according to the comparator's decision. Therefore, instead of designing a system as shown in Figure 2.28, the comparator outputs can be transmitted through the load modulation scheme. Figure 2.29 shows the principle.

The differential comparator outputs represent the ADC output codes and they drive two

Figure 2.29: The principle of ADC Data transmission based on load modulation and its timing diagram

NMOS switches ML1 and ML2 through a buffer and an inverter to generate three different loads seen from 1.8V supply in the Test PCB. The three different loads correspond to three states : '1', '0', and 'DataReady' and they will generate three voltage levels in V_{out} which will be captured through the oscilloscope and processed by the MATLAB.

3

HIGH VOLTAGE TRANSMIT SWITCH

3.1. TRANSMIT CIRCUIT: THE PRIOR ART

In order to obtain sufficient acoustic pressure, a pulse voltage of tens of volts is typically used in ultrasound imaging which means that high voltage transistors are required. The TSMC 0.18 μm BCD technology used in this work provides 1.8V, 5V, 6V, 7V, 12V, 45V and 70V transistors. Although the HV transistor has relatively large breakdown voltage compared to the LV one, the area of the HV transistor is much larger. Figure 3.1 shows the layout of a minimum size 45V NMOS transistor ($W = 10\mu\text{m}$, $L = 600\text{nm}$). Therefore, the area needs to be taken into consideration when designing the HV transmit circuits.

Figure 3.1: The layout of a 45V HV NMOS Transistor

The basic idea of a high voltage pulse generator is to level-shift up a low-voltage pulse. Figure 3.2 shows two commonly-used types of the HV pulser. In Figure 3.2 (a), only one HV NMOS is needed which is area-efficient [16]. But this type of pulser is power hungry, because except the power burned in charging and discharging the transducers capacitance C_{PZT} , extra static current is flowing from HV VDD to ground when the HV NMOS transistor is turned on. Therefore, the resistive pull-up pulser is simple and compact, but not power-efficient. In Figure 3.2 (b), a fully-dynamic design is proposed in which an HV level-shifter is used to close the PMOS transistor when HV NMOS transistor is turned off [48]. Although no static current is consumed during the switching, at least 6 HV transistors (2 or 4 in the HV level-shifter) are used. Although this design is more power-efficient, it is not preferred in an area-constraint system. In Figure 3.2 (c), a HV switch circuit is

proposed [49]. Two bootstrap capacitors are connected between the gate and source of switch M1 and M2 and the capacitors are charged and discharged through two low voltage transistor M3 and M4. The power consumption includes the charging and discharging of the bootstrap capacitors and transducer parasitic capacitor C_{PZT} , which is similar to the HV pulser based on fully-dynamic topology. But this architecture needs fewer HV transistors and allows arbitrary transmit waveforms.

Figure 3.2: (a) HV Pulser based on resistive pull-up [16] (b) HV Pulser based on fully-dynamic topology [48] (c) HV switch [49]

3.2. DEVICE FEATURES

For the design of the HV pulse generator, there are two important parameters of HV transistor to be determined: the breakdown voltage which limits the maximum pulse voltage and the transistor on-resistance which constrains the output pulse settling speed.

In the TSMC 0.18 μm HV BCD technology, the devices (LV and HV MOS transistors and diodes) have specific tolerance requirements which should be taken into consideration to avoid the device breakdown. For example, a 45V transistor has a $|V_{gs}|$ tolerance of 5.5V and $|V_{ds}|$ tolerance of 45V. Table 3.1 summarizes the voltage tolerance of 1.8V, 5V, 29V and 45V transistors.

Table 3.1: Device Features of 1.8V/5V/29V/45V transistor

Device	$ V_{gs} $	$ V_{ds} $	$ V_{bs} $	$ V_d - V_{sub} $	$ V_{db} $	$ V_{gb} $	$ V_b - V_{sub} $
1.8V MOS	0 - 1.8	0 - 1.8	0 - 1.8	-	-	-	-
5V MOS	0 - 5	0 - 5	0 - 5	-	-	-	-
29V MOS	0 - 5.5	0 - 29	0 - 5	0 - 29	0 - 29	0 - 5.5	0 - 29
45V MOS	0 - 5.5	0 - 45	0 - 5	0 - 45	0 - 45	0 - 5.5	0 - 45

The transducer needs to be excited at the resonant frequency which means that the pulse width of the HV pulse should equal:

$$t_{pulse} = 1/2f_{res} \quad (3.1)$$

Because piezoelectric transducers with a resonant frequency of 14MHz are used, the

Figure 3.3: On resistance of a HV transistor versus V_{gs}

pulse width should be approximately 36ns. Assuming the rising edge of the input pulse is 3ns and the transducer parasitic is 0.3pF, to ensure >90% settling, the required transistor on-resistance is around $1.4k\Omega$

Figure 3.3 shows a plot of the transistor on-resistance versus the V_{gs} . From Figure 3.3, when V_{gs} is 3.6V, the on-resistance of the transistor is around $1.4k\Omega$. However, this is simulated at a drain-source voltage V_{ds} of 30V. When a voltage pulse is charging a capacitor through a switch, the switch on-resistance is not constant but increases with the settling, because the V_{ds} is decreasing with the settling. Therefore, in order to compensate this effect, 5V is chosen as the gate voltage of the HV MOS transistor.

3.3. PROPOSED HV TRANSMIT CIRCUITS

Based on previous analysis, the HV switch circuits are power-efficient and are able to transmit arbitrary waveforms. But extra HV transistors are required to open the switches (2 in Figure 3.2 (c)). In principle, only two HV transistors are required: one for the HV switch and another one for open the HV switch. The bootstrap capacitors are still necessary because the switch should be turned on during the HV pulse.

Figure 3.4 shows the proposed HV switch and the required control signal. MH1 and C_{bs2} are used to open MH2. C_{bs1} and low voltage control signal generator are used to open MH1. The switch control signal $V_{charge1}$, $V_{charge2}$ and V_{bs1_bot} are all in 5V low voltage domain.

The two bootstrap capacitors C_{bs1} and C_{bs2} are used to open the switches MH1 and MH2 respectively. The operation timing diagram is also shown in Figure 3.4. In the first cycle when $V_{charge1}$ and $V_{charge2}$ are both high and V_{bs1_bot} is low, the bootstrap capacitor C_{bs1} is charged to 5V. The diode D1 is used to prevent the capacitor discharge when $V_{charge1}$ turns to low. When $V_{charge2}$ is low and V_{bs1_top} is high, MH1 is turned on which

Figure 3.4: Schematic of High voltage switch and timing diagram of required control signal

pulls down V_{bs2_top} and turns off MH2. In the next transmit cycle when V_{bs1_bot} is high, V_{bs1_top} will be bootstrapped to 10V because there are already $5C_{bs1}$ charge stored on C_{bs1} . MH1 will be turned on and V_{bs2_top} will be charged to $V_{charge2}$ and turn on MH2. The diode D2 protects the gate of MH2. When high voltage pulse comes, V_{bs2_top} is bootstrapped and keeps MH2 on. When $V_{charge2}$ is low, C_{bs2} is discharged which turns off the switch.

Figure 3.5: Schematic of High voltage switch with the parasitic capacitance of MH1

However, because of the parasitic of the drain of MH1, the bootstrapped voltage will be smaller than expected. Figure 3.5 shows the effect of parasitic. Due to the parasitic, C_{bs2} and C_p will form a capacitor divider. When the HV pulse comes, the charged stored on C_{bs2} will be shared with C_p . Therefore, V_{gs} will decrease to less than 5V.

$$V_{gs} = 5 \frac{C_{bs2}}{C_{bs2} + C_p} \quad (3.2)$$

The solutions are to increase C_{bs2} or decrease the size of MH1. The proposed HV-switch-based HV pulse generator only requires 2 HV MOS transistors and its power consumption is limited by the charging and discharging of the transducer capacitance which is $f_{PRF}CV^2$.

4

CLOCK AND DATA RECOVERY

THIS chapter discusses techniques that help to reduce the numbers of cables. Clock and data are combined on one cable by means of pulse width modulation (PWM). Amplitude modulation is also applied to provide a 5V supply, which is used to open the HV switches.

4.1. MULTI-FUNCTIONAL COMMAND LINE

As discussed in Chapter 1 and Section 1.1.2, a shift register is a necessary part because the ASIC needs to be configured by the imaging system. Besides, the imaging system also needs to determine the length of the transmit phase and the receive phase. A basic block diagram of a conventional buffered shift register is shown in Figure 4.1. A shift

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Figure 4.1: Block diagram of a basic shift register and its timing diagram

register needs 2 signals, the clock and the data. The input data bits are shifted in one by one in every clock cycle. In order to prevent the control signals D1 ... DM, from toggling which new data is shifted in, a buffered shift register, which uses a load signal to latch all the bits, is necessary.

Conventionally, 3 cables are needed for the shift register. In order to reduce 3 cables to 1 cable, pulse width modulation (PWM) is applied to embedded the data into the clock signal first. The basic principle is to modulate 1 and 0 into different pulse widths or duty cycles (e.g., 25% duty cycle represents "0" and 75% represents "1"), which is shown in Figure 4.2. The clock edge is still accurate which can be used as the shifting clock and as

Figure 4.2: Basic principle of pulse width modulation

a clock for the ADC which is 60MHz in this thesis.

The clock and data have been combined with pulse width modulation, however, a load signal is also necessary. Similarly, the state for the load signal can be modulated into another duty cycle, for instance, 10% or 90%. However, the increased states to be modulated will increase the complexity of the demodulation circuit and, more importantly, there will be transmission line-dependent duty cycle fluctuation when the 60MHz PWM signal is transferred through the coaxial cable. If two states are modulated, the margin for the duty cycle fluctuation is around 50% compared to 33% when three states are modulated. Although the difference between 50% and 33% is not huge, the fewer states to be modulated is still preferred in terms of communication stability and simplicity of demodulation.

Figure 4.3: Block diagram of PWM signal demodulator and its timing diagram

Figure 4.3 shows the demodulation scheme of a two-state PWM signal. Because only two states need to be determined, the circuits for the demodulation are quite simple, which consist of a delay cell and two D flip-flops.

The D flip-flop with asynchronous clear works as an edge detector: it generates a new clock "CLK_Sample" whose frequency is same as "CLK_In" where the duty cycle is controlled by the delay cell "Td". In order to obtain the maximum duty cycle headroom, the optimum delay should be half clock cycle. The delay can be generated by a delay-locked-loop (DLL) which can generate a delay that is much less sensitive to the PVT (Process, voltage and temperature) variations [50] compared to the delay generated by standard inverter chain. However, if the duty cycle headroom can cover the change caused by the PVT variations, an inverter chain is preferred compared to the DLL. Figure 4.4 shows the simulated delay variations of a delay cell from TSMC 0.18 um digital library. The delay only changes 30ps over 100 degrees, 30ps over $\pm 0.2V$ supply voltage variations and 40ps over process variations, which are negligible compared our target clock period (16.6ns).

As discussed in Chapter 1, an ultrasound system has its transmit phase and receive phase. In transmit phase, the receive circuitry is inactive which means the shift register can be

Figure 4.4: Delay versus PVT variations

loaded in the transmit phase. Therefore, a "TX" signal can be generated to be used as an indicator of the start of the transmit phase and also as the "Load" signal for the shift register. Besides, as discussed in Chapter 3, the transmit circuits need 5V to open the HV switch. Therefore, the amplitude modulation can be employed to embed 5V into 1.8V PWM signal. By demodulating the 5V signal, the supply for the HV switches, the "TX" signal and the "Load" signal can be obtained. In the ASIC side, the demodulator can threshold the input signal to be able to distinguish between the signal in the 1.8V domain and in the 5V domain. Figure 4.5 shows the timing diagram of the proposed multi-functional command signal. The rising edge of 5V can be used as the load signal for the shift register and an indicator of the start of transmit phase. The 5V can be used to open the HV switch.

A threshold detection circuit should be able to extract information which is related to 5V. Because there are three amplitudes in the multi-functional command signal (0V, 1.8V and 5V), therefore, 1.8V can be used as the threshold voltage to distinguish between the 1.8V PWM signal and 5V signal. Besides, a voltage limiter is necessary in the input of the PWM demodulator in order to clip the 5V. A simple voltage limiter is shown in Figure 4.6.

Figure 4.5: Timing diagram of the Proposed Multi-functional Command Signal

A 5V transistor's gate is biased at constant 1.8V and its drain and source are connected to V_{in} and V_{out} respectively. The relationship between V_{in} and V_{out} follows eq. 4.1.

Figure 4.6: A simple voltage limiter

$$V_{out} = \begin{cases} V_{in} & \text{if } V_{in} < 1.8 - V_{th} \\ 1.8 - V_{th} & \text{if } V_{in} \geq 1.8 - V_{th} \end{cases} \quad (4.1)$$

From eq. 4.1, the maximum value of V_{out} will be $1.8 - V_{th}$ which should be recovered to standard 1.8V digital signal. Therefore, a continuous time comparator is needed.

Figure 4.7: Block diagram of clock and data recovery unit

Figure 4.7 shows the architecture of clock and data recovery unit which extracts clock, data and shift register load signal from a multi-functional mix-voltage command signal.

5

PROTOTYPE IMPLEMENTATION

THIS chapter describes the implementation details of different blocks in the ASIC, including the OTA in the analog front end, the analog input multiplexer, the high voltage switches, the comparator and SAR logic in the ADC, the bootstrapped switch, the continuous comparator in the clock and data recovery circuit. Some auxiliary circuits, for instance, reference buffer and constant-GM biasing, are also discussed.

5.1. SYSTEM GLOBAL MAP

In the previous chapters, the receive signal chain and the clock and data recovery have been discussed. For the HV switches, a switch control signal generator and HV switch controllers are required. The final architecture is shown in Figure 5.1.

Figure 5.1: Final Architecture of IVUS ASIC

This ASIC only requires 4 external connections and is able to interface with 64 receive elements and 16 transmit elements.

5.2. INPUT MULTIPLEXER AND DECODER

In the receive phase, only one channel will be connected to the receive circuitry and the other 63 channel should be connected to ground in order to reduce the crosstalk. Figure 5.2 shows the schematic of the 64-to-1 input multiplexer. Each channel contains two NMOS switches and an inverter. When one channel is selected, M1 of this channel is turned on and M2 is turned off. In the other channels, M1 is off to disconnect the transducer from the receive circuitry and M2 is on to ground the transducer.

A 6-to-64 decoder is employed to generate 64 channel enable signals. The 6-to-64 decoder is comprised of 9 3-to-8 decoders. The schematic of the 3-to-8 decoder is shown in Figure 5.3. The *EN* signal is used to gate the decoded output. When *EN* is 0, all the

Figure 5.2: Schematic of the input multiplexer

outputs is set to 0.

Figure 5.3: Schematic of the 3-to-8 Decoder

Figure 5.4: Schematic of the 6-to-64 Decoder

The schematic of the 6-to-64 decoder is shown in Figure 5.4. The 3 LSBs of the input codes D0, D1 and D2 are the inputs of the 8 3-to-8 decodes and the 3 MSBs of the input codes D3, D4 and D5 are the inputs of a separate decoder whose outputs are connected to the *EN* ports of the 8 3-to-8 decoders. The *MUX_EN* is used to disable or enable the

6-to-64 decoder. When MUX_EN signal is 0, all the 64 outputs are set to 0.

5.3. OTAs USED IN AFE

Based on the discussion on the input multiplexer, the transducer is biased at the ground before it is connected to the receive circuitry. In order to avoid an additional voltage step on the transducer when it is connected to the TIA virtual ground, which would create a pseudo-transmit action, the TIA shown in Figure 5.5 applies an AC coupling capacitor to bias the TIA input to ground. The switch controlled by TX are used to configure the TIA in a unity-gain configuration which will help to keep the biasing point stable in the transmit phase. The input impedance of TIA can be expressed as:

$$Z_{in} = Z_{C_{ac}} + Z_{in,OTA} \quad (5.1)$$

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Which should be $>10\times$ smaller than the source impedance of transducer as discussed in Section 2.3. The bandwidth is roughly calculated from the combination of R_F and C_F which is around 18MHz. The same OTA is employed in the TGC.

Figure 5.5: OTA architecture used in the TIA and TGC

Figure 5.6 shows the schematic of the ADC driver and the OTA used in it. The TX signal is valid in the transmitting phase when the ADC driver is configured in unity gain. The ADC driver applies a fully-differential OTA whose CMFB is passively built by an RC network. Besides, in order to obtain enough gain, cascode inverter-based OTA is employed. The biasing voltage V_{bp} comes from a constant-gm biasing circuit

Table 5.1 lists the supply current of the OTAs used in the AFE.

Figure 5.6: Schematic of ADC Diver and the fully differential OTA

Table 5.1: The supply current of different stages in the AFE

Stage	Supply Current
Low Noise Amplifier	217.7 μ A
Flipped Voltage Follower	105.5 μ A
Time gain Compensation	217.7 μ A
ADC Driver	404.8 μ A
Total Supple Current in the AFE	945.7 μ A

5.4. CONTINUOUS TIME COMPARATOR IN CDR

A continuous time comparator is applied in the clock and data recovery block which is used to recover the amplitude limited signal to a 1.8V standard digital signal. The comparator consists of an amplifier and a buffer as shown in Figure 5.7. The biasing

Figure 5.7: Schematic of continuous time comparator

voltage V_b comes from a constant-gm biasing circuit. The input of the comparator is

a digital signal with an amplitude of 1.1V. If using a standard inverter to regenerate a 1.8V digital signal, the rising edge and falling edge will not be symmetric. Therefore, a pre-amplifier, whose output is biased at mid supply (0.9V) is employed. The continuous time comparator consumes 192 μ A current.

5.5. BIASING CIRCUIT

A constant-gm biasing circuit [51] is used to generate biasing current for the amplifiers in the AFE, the continuous time comparator and the dynamic comparator in the ADC. The schematic is shown in Figure 5.8. The two PMOS transistors with the equal W/L

Figure 5.8: Schematic of constant-gm biasing circuit and its start-up circuit

make the current equal in two branches. The voltage across R_b equals to the difference between V_{gs} of M2 and M1. We can get:

$$I_2 = I_1 = \frac{V_{gs1} - V_{gs2}}{R_b} \quad (5.2)$$

Neglecting the body effect, the current can also be expressed by:

$$I_1 = \frac{1}{2} \frac{kW}{L} \mu C_{ox} V_{OD1}^2 = I_2 = \frac{1}{2} \frac{W}{L} \mu C_{ox} V_{OD2}^2 \quad (5.3)$$

$$\Delta V_{OD} = \Delta V_{gs}$$

Besides, the g_m is:

$$g_m = \frac{2I_D}{V_{OD}} \quad (5.4)$$

Therefore, g_m equals:

$$g_m = \frac{2}{R_b} \left(1 - \frac{1}{\sqrt{k}}\right) \quad (5.5)$$

Based on eq.5.5, the g_m will be constant and only related to resistor R_b and the ratio between the size of M2 and M1. In order to avoid a lock-up state [52] in which all transistors are off, a start-up circuit is usually required. In Figure 5.8, when the chip is powered on, M3 is turned and pulls up the gate of M5. M5 injects a small current into the constant-gm biasing circuit to start-up circuit which will pull up the gate of M4 to disable the start-up circuit. The power consumption is negligible because of the long channel device M3. $20\mu\text{A}$ current is consumed in the constant-gm block.

5.6. DYNAMIC COMPARATOR IN ADC

Figure 5.9 shows the employed dynamic comparator [35]. When designing a comparator, three parameters need to be considered: speed, noise and offset. The offset of a comparator can be expressed as [53].

$$V_{os} = \Delta V_{TH1,2} + \frac{(V_{GS} - V_{TH})_{1,2}}{2} \left(\frac{\Delta S_{1,2}}{S_{1,2}} + \frac{\Delta R}{R} \right) \quad (5.6)$$

where $\Delta V_{TH1,2}$ is the threshold voltage mismatch of the differential pair transistor M1 and M2, $\Delta S_{1,2}$ is the area mismatch of M1 and M2 and ΔR is the loading mismatch of the differential pair [53]. The first term in eq. 5.6 is the static offset which is independent to input signal. The second term is affected by the input signal $((V_{GS} - V_{TH})_{1,2})$ which is the so-called dynamic offset. However, the $(V_{GS} - V_{TH})_{1,2}$ will be kept constant because of the fact that the comparator shown in Figure 5.9 uses Mb to generate bias current which can hardly be affected by input signal.

The achievable speed of a comparator is limited by the unity gain bandwidth [45]:

$$\omega = \frac{g_{m,in}}{C_{load}} \quad (5.7)$$

The biasing current is determined by Mb and Vb in Figure 5.9. For the PMOS input pair, the large common mode voltage leads to large $g_{m,in}$, and thus higher speed. In Section 2.4.7, the requirement for the comparator noise, offset and speed has been derived. The noise requirement is $600\mu\text{V}$. The designed comparator has a simulated noise of $150\mu\text{V}$ which is 4 times smaller than the requirement. The offset of this comparator is mainly comprised of the static offset, which can be decreased by increase the size of the input differential pair. However, the increased size of input pair will increase the load capacitance and thus reducing the comparator speed (see eq. 5.7). Comparator offset calibration technique can be employed which is done by adding CDAC at node X+ and X- [54]. But it also increases the load capacitance. Considering that the offset only results in the nonlinearity and the speed is a more important parameter, the simulated offset of this comparator is approximately 3mV which is larger than the requirement. The biasing current is around $547\mu\text{A}$.

Figure 5.9: Schematic of Dynamic comparator [35]

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5.7. REFERENCE BUFFER

The CDAC needs to be pre-charged to a reference voltage. Therefore, a low output impedance reference buffer is required. Figure 5.10 shows the schematic.

Figure 5.10: Schematic of ADC Reference Buffer

In order to reduce the power consumption of the closed-loop stage, the reference buffer applies the replica driving technique [55]. As shown in Figure 5.10, a resistive divider generates an input voltage V_{in} . An OTA and a source follower form an op amp which is configured as a unity gain stage and forces $V_{o2} = V_{in}$. Another source follower comprised of M2 and R/m, which is a scaled replica stage, drives the load capacitor of the CDAC in an open-loop manner. The replica stage isolates op amp output V_{o2} from large load capacitance which means an energy-efficiency close loop stage can be designed. The sizes of transistor and resistor in the two source followers are designed to have a ratio of m so that $V_{o2} = V_{ref}$, and thus $V_{ref} = V_{in}$. Only $38.5\mu\text{A}$ is consumed in the amplifier and $60\mu\text{A}$ in the source follower comprised of M1 and R. $600\mu\text{A}$ is consumed in the replica stage, which results in an output impedance R_o of 80Ω .

In Section 2.4.7, the time available for the CDAC pre-charging is approximately 1.1ns. In order to achieve 10bit settling accuracy (see Section 2.4), the time constant comprised of R_o and C_{dac} should be less than 0.14ns. For a CDAC of 2pF, the required R_o is 78 Ω , which is close to the simulated output impedance of 80 Ω .

5.8. BOOTSTRAP SWITCH

In the discussion of sampling network in Chapter 2, the sampling switch should be bootstrapped in order to reduce its on-resistance and increase its linearity [56]. The schematic is shown in Figure 5.11. The M_s is the switch to be bootstrapped. CLK and CLKb is a pair

Figure 5.11: Schematic of Bootstrap circuit

of non-overlapping clock signal. When CLKb is high, M4 and M7 is turned on and Cb is pre-charged to Vdd. When CLK is high, the top plate of Cb is connected to the gate of M5, M6 and Ms. Because M6 is open, when the input signal comes, the bottom plate of Cb is connected to M6 and the top plate of Cb is bootstrapped to $V_{dd} + V_{in}$. Therefore, the V_{gs} of sampling switch will equal to VDD, which is independent to input signal.

Figure 5.12 shows the schematic of the non-overlapping generator and its timing diagram. The CLKs and CLKsb are used for the sampling clock of the ADC.

5.9. HV SWITCH CONTROL GENERATOR

As discussed in Chapter 3, a set of control signals is required to be able to switch on and off the HV switches. In order to generate control signals shown in Figure 3.4, Figure 5.13 illustrates HV switch control circuits and the timing diagram. As discussed in Chapter 4, the input command signal is a mix of a 1.8V digital signal and a 5V supply. In Figure

Figure 5.12: Schematic of non-overlapping generator

Figure 5.13: Schematic of HV switch, LV switch control and the timing diagram

5.13. M4 works as a threshold detector. When V_{cmd} is 1.8V or less, M4 and M1 are turned off. The current source pulls the gate of M2 and M3 down, pulling up the gate the M5 and thus pulling down V_{5V} . Therefore, when the command line is transmitting the 1.8V PWM signal, the HV switch control circuits and HV switches are both disabled. When the 5V comes up, M1 and M4 are turned on. By properly sizing M1 and the current source to make the pull-up current large than the pull-down current, the gate of M2 and M3 will be pulled up to 5V and thus turn off M5. Therefore, when the command line is transmitting the 5V signal, V_{5V} will be active and the HV switch control circuits and HV switches start to work.

When EN is high, the gates of M10 and M15 are pulled down and in the meanwhile, the bootstrap capacitor C_{bs1} is charging to 5V by V_{5V} . The node V_s is pulled to 5V, so

is the source of M14. M14 and M13 will work as an inverter whose output is connected to V_{bs1_bot} . R1 and C1 form a low pass network which generates a delayed version of V_{5V} : V_{5V_delay} . As shown in the timing diagram of Figure 5.13, after V_{5V_delay} passes the inverter, the inverter output, V_{bs1_bot} , will be a 5V pulse which bootstraps V_{bs1_top} to 10V. In the meanwhile, V_s is pulled up to 5V because M10 is open, which opens the switch MH1, charges C_{bs2} to 5V and open the switch MH2. The HV pulse comes up in the transmit phase when the HV switch is on. When EN is low, M11 and M12 will pull down V_s and V_{bs1_bot} and thus turn off MH2. Therefore, the switch control circuits are able to turn on and turn off HV switch by setting the 1.8V low voltage digital signal EN .

5.10. DESIGN FOR TESTABILITY

In order to characterize the functionality and performance of the receive signal chain, an analog test input is designed at the input of the AFE. An analog test output which can monitor the TGC output is also employed. Except for the high-speed serial ADC outputs, the parallel outputs are also designed as test outputs in a parallel and lower speed way. Figure 5.14 shows the diagram of the test input and outputs.

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Figure 5.14: Schematic of Test circuits

Because the LNA in the AFE is a trans-impedance amplifier which requires a current input, an on-chip resistor is employed to convert an external voltage into the current:

$$I_{in} = \frac{V_{in}}{R_{in}} \quad (5.8)$$

A $TESTIN_EN$ signal is used to enable or disable the test input. Besides, the analog multiplexer should be disabled when the circuit is in the test mode. Therefore, MUX_EN is used to disable the analog multiplexer. The AFE output is connected to the cable driver. The output of the cable driver is shared with the output of the load modulation module. To avoid conflicting of the two outputs, the load modulation is controlled by

The cable driver is used to drive coaxial cables with large capacitance (27pF/m to 110pF/m [57]). A power-efficient class AB CMOS buffer is applied [58] which is shown in Figure 5.15.

The two switches which are controlled by EN signal are used to bypass the cable driver. The output of the cable driver is shared with the high-speed serial output. When the high-speed serial output is enabled and cable driver is bypassed, a kick back path from the output node V_o to the input node V_{in} would affect the signal at the ADC driver input and generate high-speed spikes. Therefore, a transmission gate is designed at the input of the cable driver which cuts off the kick back path when high-speed serial output is enabled.

5.11. CHIP LAYOUT

Figure 5.16 shows the layout diagram of the prototype with the critical sub-blocks labeled, including the AFE, the ADC, the HV switches, the CDR and the input multiplexer.

Table 5.2: Contents of the shift register bits

Bits	Function
1-6	6 input bits of the 6-to-64 decoder
7-22	16 control bits for the HV switches
23-24	Two control bits for the gain control of the TGC stage
25	AnalogMUXEn: To enable or disable the analog multiplexer
26	AnalogTestEN: To enable or disable the analog test input
27	ADCTestEn: To enable or disable the ADC test input
28	DigitalOut: To enable or disable the load modulation output
29	AnalogOut : To enable or disable the analog output
30	ADCEN: To enable or disable the ADC sampling clock

Figure 5.16: Layout diagram of the prototype

Two round-shape seal rings have been made to protect the active circuits when the chip is laser-cut to a donut-shape pattern. The inner seal ring creates a hole with 0.45mm diameter for the guidewire and the outer seal ring determines the outer boundary of the core chip.

Figure 5.17 shows the chip layout with only the pad layer. In the donut-shape core chip area, there are 16 pads for transmit transducers, 64 pads for receive transducers and the

Figure 5.17: Layout diagram with only the pad layer of the prototype

Figure 5.18: The vertical cross-section of the shielding strategy

remaining 5 pads are for the 4-cable connections (one of the 5 pads is connected to the shield of the coaxial cables). The pads that are in the periphery are used for testing. As shown in Figure 5.16, the circuits are sitting below the pads for receive transducers and transmit transducers. In order to avoid coupling effects between the transducers and circuits (e.g., the HV pulse in the HV switches coupling into the receive transducers through parasitic capacitance and high-speed low-voltage pulses in the CDR and ADC coupling into the receive transducers), a shield plane is used. Figure 5.18 shows the vertical cross-section of the shielding strategy. Metal 5 is connected to ground and works as a shield between metal 6 and metal1-4 to reduce the coupling effects.

6

MEASUREMENTS

IN this chapter, measurement results of the IVUS ASIC are presented. The fabricated chip is briefly introduced first. Then the measurement setup is described in detail. Next, the results of electrical measurements and acoustic measurements are discussed.

6.1. FABRICATED CHIP

The IVUS ASIC is implemented in the TSMC HV 0.18 μm BCD technology. Figure 6.1 shows the die microphotograph. This chip is comprised of a donut-shaped core chip and peripherals test pads. On the core chip, there are 5 pads for 4-cable connections: VDD Pad, HV pulse pad, command pad, RX data pad and ground pad (the ground pad will be connected to the shield of the coaxial cables). The remaining pads are for the transducers (16 for the TX and 64 for the RX). The chip area is 4 mm² (2 mm x 2 mm) and the core chip has a outer diameter of 1.5 mm and inner diameter of 0.45 mm.

Figure 6.1: IVUS Diemicrophotograph (the "Regular" pattern)

Figure 6.2: IVUS Diemicrophotograph (the "Sun-flower" pattern)

Figure 6.2 shows the die microphotograph with the transmit and receive bondpads distributing as a "sun-flower" pattern. This arrangement of the transmit and receive bondpads is intended to achieve a better image quality. However, it is difficult to obtain the "sun-flower" pattern through laser dicing. The arrangement of the remaining pads are the same as the die shown in Figure 6.1.

6.2. MEASUREMENT SETUP

Figure 6.3 shows the measurement setup. The ADC parallel test outputs are connected to the test PCB and then captured by the FPGA. An Altera Cyclone-IV E-series FPGA (EP4CE115F29C7) is employed. The VerilogHDL-based PWM generator generates the command signal, and then the pulse generator in the test PCB will combine the PWM signal with the 5V supply. The pulse generator in the PCB is shown in Figure 6.4.

Figure 6.3: The measurement setup

An SPDT (single pole, double throw) analog switch is used to switch between 5V DC supply and 1.8V PWM signal. The switch control signal is also generated by the FPGA. A 200MHz 2:1 SPDT switch (ADG719 [59]) is employed which has 12ns t_{on} and 6ns t_{off} and approximately 4Ω on-resistance. The HV pulse is provided by an external HV pulser (AVIR-4DB [60]) which has 20KHz PRF, maximum 200V amplitude, 2ns rising time and 2.5ns falling time. The 1.8V supply for the chip power and load modulation are provided by two 1.8V regulators.

After the FPGA captures the ADC parallel output codes, the data will be transmitted to the PC through a UART interface. The high-speed serial output is captured by the oscilloscope and then transmitted to the PC through the USB interface. All the received data are processed by the MATLAB. The analog test input is generated by an arbitrary waveform generator (AWG).

Figure 6.4: Diagram of the pulse generator in the Test PCB

Figure 6.5: Layout of the MATLAB-GUI-based IVUS Demo

In MATLAB, a control interface has been designed to automate the measurements. Figure 6.5 shows this MATLAB GUI. The control command can be selected in the user interface and then the command word is packaged and transferred to the FPGA through the UART. The FPGA will decode the received data and obtain the command word, then, the PWM generator generates PWM signal according to the command word. Besides, the

FPGA captures the parallel ADC outputs and then transmits to the PC, then the MATLAB GUI receives, processes and displays the data. Figure 6.6 shows the control flow between FPGA and PC.

Figure 6.6: The control flow between FPGA and PC

6.3. TEST PCB

The test PCB is divided into two parts, the daughter board on which the IVUS ASIC is mounted and the mother board where the electronics are located. The daughter board is mounted on the mother board through headers in the test mode, while in the 4-cable mode, the daughter board is connected with the mother board only with the four cables. Figure 6.7 shows the layout of the mother board and the components.

Figure 6.7: The layout of the MotherBoard of the Test PCB and its components

Figure 6.8: The layout of the Daughter Board

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The mothers board provides the supply voltage to the fabricated chip and the 1.8V supply voltage for the load modulation. Moreover, the command signal and the ADC parallel outputs are connected to the FPGA through a 40-pin connector. Figure 6.8 shows the layout of the daughter board. It contains the four connectors for 4 coaxial cables, two connectors for transducer test, one header for controlling the parallel digital output and the fabricated chip.

6.4. ELECTRICAL MEASUREMENT RESULTS

The electrical measurement results contain the transfer function of the receive signal chain, the ADC output spectrum obtained through the parallel outputs and the high-speed serial output and the HV switch output waveform.

6.4.1. THE MEASURED COMMAND SIGNAL

Figure 6.9 shows the measured multi-functional mix-voltage command signal generated on the mother board. It clearly shows the 60MHz PWM signal and 5V DC signal. Figure 6.10 shows that the command signal also defines the length of the transmit phase and the receive phase and the PRF which is programmable through FPGA. The PRF rate of Figure 6.10 is approximately 20kHz.

Figure 6.9: The measured command signal which shows the details of PMW signal and 5V DC signal

Figure 6.10: The measured command signal which shows the PRF rate

6.4.2. DATA RECOVERY FROM HIGH SPEED SERIAL OUTPUT

Figure 6.11 shows the high speed serial output. Compared to the ideal waveform shown in Figure 2.29, the measured waveform is limited by the bandwidth of the probe and the oscilloscope.

The way of recovering data is to apply two threshold voltages in the MATLAB to deter-

Figure 6.11: The measured high speed serial output

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Figure 6.12: The comparison between the FFT spectrum of the two types of output

mine the data bits and a "timing threshold" to determine the "DataRdy" signal. To verify the functionality of the high-speed serial output decoding scheme, a sinuous signal is applied at the analog test input and the FFT spectrum of the parallel ADC output and the decoded high-speed serial output are compared (Figure 6.12).

The results show that the FFT spectrum obtained from the two types of output is similar and the calculated SNR is also the same (33dB).

6.4.3. TRANSFER FUNCTION OF THE RECEIVE SIGNAL CHAIN

Figure 6.13 shows the transfer function of the receive signal chain measured through the ADC parallel output. It shows the three TGC gain steps of 6dB, 12dB and 18dB. The ideal total programmable gain is 12dB. But due to the limited gain accuracy, the achieved total gain step is approximately 11.3dB. The -3dB bandwidth is approximately 16MHz which is smaller than the simulated bandwidth of 23MHz. The reduced bandwidth is probably caused by the reduced supply current (the supply current is reduced by 250 μ A compared to the simulation).

Figure 6.13: The transfer function of the receive signal chain

6.4.4. ADC OUTPUT SPECTRUM

Figure 6.14 shows the ADC parallel output spectrum when the high-speed output is enabled. The SNR (calculated in 5MHz bandwidth) obtained when high-speed output is disabled is around 46dB and it decreases to 40dB when high-speed output is enabled. Combined with the 11.3dB programmable gain step, the achieved dynamic range will be approximately 51.3dB in the 4-cable mode and 57.3dB in the test mode which meets the 50dB dynamic range design target.

The SNR degradation is mainly caused by the fact that the high-speed output results in a large current flowing into the ground, which vibrates the ground for analog circuitry. A direct solution is to reduce the signal swing of the high-speed serial output. Figure 6.15 shows parallel output spectrum after reducing the high-speed serial output swing.

By reducing the high-speed output swing, the SNR degradation decreases from 6dB to 2dB. Except for the SNR improvement, the lower swing also means lower power con-

Figure 6.14: The ADC output spectrum

Figure 6.15: The ADC output spectrum

sumption. However, the lower swing (Figure 6.16) on the high-speed output makes the thresholding-based decoding scheme shown in Figure 6.11 unreliable. A better decoding scheme is required.

Figure 6.16: The high speed serial output with lower swing

6.4.5. HV SWITCH OUTPUT

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Figure 6.17: Measurement output waveform at a transmit pad

Figure 6.17 shows the measured output waveform at a transmit pad. The input pulse width is around 50ns which are suitable for the transducer with a central frequency of 10MHz and the input pulse amplitude is 30V. The measurement result shows that the switch output only settles to 28V which is because of the fact that the time constant is increased by the extra parasitic capacitance ($\sim 5\text{pF}$) introduced by the PCB trace.

6.5. ACOUSTICAL MEASUREMENT

6.5.1. ACOUSTICAL MEASUREMENT SETUP

Figure 6.18: Layout of the transducer prototype

In order to test the functionality of the ASIC when processing real ultrasound signals, the IVUS ASIC is connected to a transducer prototype built on an interconnect test chip via wire bonding.

Figure 6.18 shows the layout of the test chip. The PZT transducers are directly integrated on the pads shown in Figure 6.18. In the right side, the pads for the wire bonding will be connected to the transmit pads and receive pads of the IVUS ASIC through bonding wires. Figure 6.19 illustrates the connection of the IVUS ASIC to a transducer prototype via wire bonding. Both of them are sitting on top of the mother board.

Figure 6.19: The connection of the IVUS ASIC to a transducer prototype via chip to chip bonding

Figure 6.20 shows the microphotograph of the setup. In the IVUS ASIC, only 16 receive pads and 9 transmit pads are connected to the transducer prototype, leading to a transmit and receive array as shown in Figure 6.21. The middle 3x3 array is used for transmit. The 2 3x3 array in the right side and left side are used for receive and test. The two test transducers are used to characterize the transducer frequency response.

Figure 6.20: The micro-photograph of the setup

Figure 6.21: The transmit and receive array for the acoustical measurement

Figure 6.22: The 4 cable measurement setup

The acoustical measurement is done in 4-cable mode, which means there are only 4 cable connections between the mother board and the daughter board. A water bag is

sitting on top of the transducer. The setup is shown in Figure 6.22

6.5.2. IMPEDANCE MEASUREMENT OF TRANSCUDER

Figure 6.23 shows the measured impedance characteristics of one transducer of the transducer array. It shows that the resonant frequency is around 10MHz and the parasitic capacitance is about 5pF after calibrating the capacitance introduced by the PCB trace. However, the simulation results show the 14MHz resonant frequency and 0.3pF parasitic capacitance. The increased parasitic capacitance will affect the noise performance of the AFE and also cause some signal attenuations.

Figure 6.23: The measured impedance characteristics of a transducer in the transducer array

6.5.3. TRANSMIT PRESSURE MEASUREMENT

To verify the functionality of the transmit circuits, transmit pressure is measured by placing a hydrophone at 2.5mm in front of the transducer array and exciting different transducer elements. The results are shown in Figure 6.24.

The hydrophone receives the pulse generated by the transducers which are amplified and then captured by the oscilloscope. The results shown in Figure 6.24 shows that the amplitudes of the transmit pressure do not increase linearly with the number of excited elements. The reason is that when the hydrophone is placing close to the transducer array, the ultrasound waves generated by different transducer elements would not be

Figure 6.24: Transmit pressure measured using a hydrophone

superposed in phase because of the phase shift. Therefore, the transmit pressure is increasing when the number of excited transducers is increasing, which means that the HV transmit circuits are able to turn on one switch or multiple switches simultaneously.

6

6.5.4. RECEIVE MEASUREMENT

To verify the functionality of the receive circuitry, a receive signal measurement is done by putting a 5MHz transmit transducer on top of the transducer array and receiving the signal from different receive elements. Figure 6.25 shows the digitized echoes received through the ASIC.

Figure 6.25: Receive measurement: pulses from a transmitted captured using the ASIC

Element A and element B are two receive transducers in the transducer array shown in Figure 6.21. The relative time delay is also shown in Figure 6.25. Therefore, the ASIC is

able to receive and digitize echo signal through selected channel.

6.5.5. IMAGING

Based on the transmit pressure measurement and the receive measurement, the ASIC is able to pulse selected transducer elements and receive from selected receive channel. In order to show the imaging ability of the ASIC, a three-needle phantom is placed in front of the array. The setup is shown in Figure 6.26.

Figure 6.26: 3-Needle experimental setup for Imaging

Figure 6.27: The final B-mode image

By successively pulsing 9 transmit transducers and receiving digitized data from 16 receive transducers, a B-mode image is generated which is shown in Figure 6.27. The position of the 3 needles is clearly shown.

6.6. MEASUREMENT CONCLUSION

The measurement details and results of the IVUS prototype shows the imaging ability in the 4-cable mode. The concept of "4-cable front-end ASIC with high-voltage transmit switching and receive digitization for IVUS imaging" is tested and verified.

7

CONCLUSIONS

7.1. THESIS CONTRIBUTION

This thesis describes the design of a front-end ASIC with high-voltage transmit switching and receive digitization, which is intended to be put into the tip of a catheter for IVUS imaging. The ASIC requires only 4 coaxial cables to interface with a total of 80 piezoelectric transducer elements (Figure 7.1). It is the first ASIC that digitizes the received signals locally, allowing them to be transmitted in a robust digital form to an external imaging system.

Figure 7.1: The artist's impression of the IVUS catheter

To do so, several techniques are proposed.

- **A multi-functional mixed-voltage command line**

The command line provides the sampling clock for the ADC, command data for the chip configuration and supply for the HV switch control circuits. Pulse width modulation (PWM) is applied to embed the data into clock signal. Amplitude modulation is employed to combine a 5V supply with the 1.8V PWM signal.

- **HV switches and LV switch control circuits**

HV pulse generating in the imaging system are connected to selected transmit elements by HV switches. These HV switches are controlled by LV switch control circuits whose supply is provided by the 5V signal in the command line.

- **ADC data transmission implemented by the load modulation**

Instead of transmitting ADC parallel outputs, the comparator outputs are transmitted asynchronously by means of load modulation, which eliminates the need for a high-speed clock source.

Besides, in the receive circuitry, an inverter-based OTA, which has a better current efficiency compared to conventional architectures and a charge sharing SAR ADC, which eliminates the need for high-speed power-hungry reference buffers, are applied.

Table 7.1 summarizes the performance of the IVUS ASIC and compares it to the prior art. This work presents a receive digitization solution to offer a more robust data transmission compared to the analog output. Besides, it only requires 4 cables, which is more

than 3 times less than the prior art.

Table 7.1: Summary of the performance of the IVUS ASIC and comparison between the prior art

	[16]	[21]	This work
Transducer type	CMUT	CMUT	PZT
Process	0.35 μ m HV CMOS	0.35 μ m HV CMOS	0.18 μ m HV CMOS
Supply voltage	3.3V	3.3V	1.8V(V_{dd}) + 5V(V_{cmd})
#Transmit	56	64	16
#Receive	48	64	64
Center frequency	10MHz	12MHz	10MHz
Receive output	analog	analog	digital
Receive bandwidth	40MHz	n/a	16MHz
Transmit circuit	pulser	pulser	switch
Max.transmit amplitude	25V	12.5V	30V
Power consumption	20mW	n/a	24mW
#Cables	13	13	4

7.2. FUTURE WORK

Beyond the prototype chip, the front-end ASIC can be further improved. A summary of several potential improvements is provided below.

- In the acoustical measurement, the transducer elements on the test chip is connected to the bondpads on the IVUS AISC through wire-to-wire bonding. The parasitics introduced by the bonding wires and the potential crosstalk among the bonding wires can be reduced by directly integrating the transducer on top of the ASIC.
- The voltage swing of the high-speed serial output affects the signal-to-noise ratio (SNR) of the receive signal chain in the prototype. Reducing the signal swing and applying a better decoding scheme will help to improve the SNR.
- The comparator offset is larger than the requirements in the prototype. The calibration can be applied to reduce the offset and thus increasing the linearity.
- The power rejection ratio (PSR) of the AFE can be increased by applying a local regulator shared by the LNA, the FVF and the TGC. The OTA in the AFE can be switched into a single-ended design.

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