Quo Vadis Microelectronics?

Intre rede

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intreerde

uitgesproken bij de aanvaarding van het ambt van hoogleraar, werksam op het vakgebied “Integrated Sensing Devices”, in de faculteit der Informatietechnologie en Systemen van de Technische Universiteit Delft, op Vrijdag 19 mei 2000 door

prof. dr. dipl.-ing. Joachim N. Burghartz

“We are confronted with portentous problems which cannot be solved just by providing for our material existence, however abundantly. On the contrary, progress in this direction is fraught with hazards and perils not less menacing than those born from want and suffering. If we were to release the energy of the atoms or discover some other way of developing cheap and unlimited power at any point of the globe this accomplishment, instead of being a blessing, might bring disaster to mankind... The greatest good will come from the technical improvements tending to unification and harmony, and my wireless transmitter is preeminently such. By its means the human voice and likeness will be reproduced everywhere and factories driven thousands of miles from waterfalls furnishing the power; aerial machines will be propelled around the earth without a stop and the sun’s energy controlled to create lakes and rivers for motive purposes and transformation of arid deserts into fertile land...”

Nikola Tesla, 1919
(Electrical Experimenter Magazine)
Mijnheer de Rector Magnificus en overige leden van het College van Bestuur,
geachte leden van deze universitaire gemeenschap,
beste familieleden, vrienden, collega’s en andere gasten,
zeer gewaardeerde toehoorders:

Graag wil ik het College van Bestuur van de TU Delft danken voor het in mij gestelde vertrouwen. Tevens wil ik alle leden van de faculteit Informatietechnologie en Systemen, de onderzoeksschool DIMES, en in het bijzonder de afdeling microelectronica en de basiseenheden ECTM en Electronica, bedanken voor het uitstekende werkklmaat en de ondersteuning, die ik heb hervaren in de loop van mijn eerste jaar in Delft. Dit soort van ondersteuning is heel belangrijk voor mij, omdat ik gevraagd ben, een nieuwe onderzoeksrichting in communicatietechnologie op silicium-basis bij de onderzoeksschool DIMES in te richten. Verder was ik gevraagd, tijdelijk de basiseenheid Electronica voor te zitten totdat een nieuwe hoogleraar voor de vakgroep gevonden zal zijn. Ook hier stel ik een grote bereidheid voor cooperatie vast, waarvoor ik graag iedereen wil bedanken.

Maar uiteindelijk zijn het mijn vrouw Susanne en mijn dochters Pia, Julia, en Tamara, die ik moet danken voor de bereidheid, na 11 jaar in Amerika opnieuw te beginnen met een vreemde taal, in een andere cultuur, en in andere levensomstandigheden.

Zo is het leren van het Nederlands ook een van mijn projecten, die ik samen met mijn vrouw Susanne in privé lessen wekelijks met veel interesse volg.

Maar voor het hoofddeel van mijn intreerende vandaag heb ik toch voor het Engels gekozen, ook om mijn collega’s en vrienden in de Verenigde Staten, in Asië, en in Europa met mijn rede te kunnen bereiken:

Ik vraag u hiervoor uw begrip.

Ladies and Gentlemen,

The title of an inaugural speech is expected to convey a positive message, pointing into a bright future and a new and long-lasting research activity. With the title “Quo Vadis Microelectronics?” or “What is the Future of Microelectronics?”, this is not very obvious. Many of us may sense a negative undertone in that question and may read through the lines “Let’s quietly bury microelectronics!” or may ask, “What is next?” I am sure that young graduates in electrical engineering wonder if they should decide for a career in a field that is with us for about forty years and is moving against its physical limits, in spite of the incredibly high demands for engineers by the microelectronics industry today. Adding a note of sarcasm, one may say that they feel as if they would board the cruise liner Titanic in the last part of its journey, the iceberg already in sight. It is for them, as well as for myself starting a research program in microelectronics, that I am posting the question:

“Quo Vadis Microelectronics?”

But, to find answers, we have to ask in more detail. We will have to clearly understand the factors that drive this major industry today and those that have been driving it historically. This will give us an impression of the momentum that is behind this industry. Next, we will have to put the achievements and the capabilities of silicon technology into perspective to fully understand its value and the manufacturing volume of the microelectronics industry. But, we cannot neglect to investigate the physical limits of integrating electronic devices and the wires interconnecting them. Those physical limits are expected to hamper the proper functioning of the integrated devices and the metal interconnects. The result will be that the benefits of miniaturization will more and more become diminished.

Of course, limitations in the device fabrication process, in contrast to the device physics, have been faced several times in the past, and, as a result, the end of microelectronics had already been announced a couple of times.
Those limitations could be overcome due to significant improvements of the processing equipment, which, in contrast, can hardly be expected for truly physical limits of the active devices and interconnects, which we will be facing soon.

Let us now take a closer look at the factors that have initiated this major industry and those that are driving it today. This means that we have to step back in time and take a look at the important historical steps of microelectronics development. The evolution of microelectronics is clearly based on logic technology.

![Diagram of Evolution of Computer Technology](image)

*Figure 1* Evolution of computer technology.

It relates to the need of high switching speed and a large and fast random access memory under the constraints of low power consumption and an acceptable physical size of a computer. Major advancements of silicon-based computers go only back to 1975 (Fig. 1). From that time on the computing speed and the memory size could be improved at a constant rate, as shown in the chart. It is interesting to extrapolate this steady trend back to the first computing machine, Karl Zuse’s Z1 (Fig. 1, top-left). The Z1 was created in 1938. It was a fully mechanical computer, used switching metal sheets, and had already 1.4-kb of memory [1]. In that aspect, the machine was far ahead of its time, but its clock frequency of 1 Hz was significantly lacking behind the extrapolated trend. A few years later, the University of Pennsylvania presented the ENIAC, a computing machine based on 18,000 vacuum tube switches and with a clock frequency of 100 kHz (Fig. 1, top-center). ENIAC, however, had a weight of 30 tons and consumed a power of 150 kW [2]. This made an extension of the technology not very intriguing, as one can imagine. The shortcomings in the early computers clearly indicated the need for a semiconductor-based machine. The result of this development are computers based on silicon technology, in which today up to a billion transistors are combined on a chip of 1-2 cm², approaching a clock frequency of 1 GHz with a power far below 10 W (Fig. 1, top-right).

This evolution would not have been possible without the invention of the transistor in 1947. The discovery of the transistor was based on Ferdinand Braun's observation of the rectification effect in 1874, Lee de Forest's vacuum-tube triode in 1906, and Lilienfeld's patent of the field-effect concept in 1926. Ironically, the field-effect device was described 20 years prior to the bipolar transistor, and 34 years before a functioning field-effect transistor was presented by Khand and Attala. Nevertheless was the field-effect already present in the first bipolar transistor in form of a parasitic surface channel. The first transistor by Bardeen and Brattain (Fig. 2) is shown in Fig. 3.

*Figure 2* Brattain, Shockley, and Bardeen (left to right) [4].  
*Figure 3* First transistor, 1947 [4].
It was shaped as a wedge in order to suppress the surface currents and to highlight the bipolar transistor action in the bulk of the semiconductor [3]. It is also interesting to note, that the first demonstration of the transistor operation and the theory of the bipolar transistor were achieved within one week. William Shockley, who was the manager of Bardeen and Brattain, saw himself in danger, not to be part of the pioneering team. He therefore challenged himself to develop the complete bipolar transistor theory over the weekend following the transistor demonstration by Bardeen and Brattain. This was a really astonishing effort [3].

It took one more important step after the discovery by Bardeen, Brattain, and Shockley until the foundation of microelectronics was completed. In 1958, Jack Kilby of Texas Instruments demonstrated the successful integration of one transistor and a few passive components on a single piece of silicon (Fig.4).

Soon thereafter, in 1961, the Fairchild Corporation, founded by Bob Noyce, Gordon Moore, and others (Fig.5), defined the planar silicon fabrication technology, in which all process steps and the contacts to the devices were applied from the front side of the silicon wafer.

The remaining problem was in power management, as the density of transistors on the chip was increased. Using bipolar technology, it was not possible to restrict power consumption to the switching action. In fact, the standby power in bipolar circuits was very large. The breakthrough came with the introduction of the complementary metal-oxide-silicon field-effect technology, called CMOS, from 1963 to 1966.

In those years, microelectronics was still in its initiation phase. The growth phase began about in 1974, as the plot of the number of technical publications versus time in Fig.6 indicates. Growth in microelectronics was for many years driven by the need for random access memory, abbreviated as RAM. Memories have a regular structure, and therefore their density is directly limited by the size of the transistors and the number of transistors required for a memory cell. The initial memories were static RAMs.

They required 6 transistors per cell, which made the cell size larger than that of the magnetic memories. The solution to the problem was the dynamic RAM, also called DRAM, patented in 1968 by Bob Dennard of IBM. Dennard’s invention was a result of a competitive situation at IBM.
With respect to the activity in thin-film magnetic memories, Dennard describes the way to his discovery [7]:

"I went home that evening discouraged because their approach looked very simple compared to the complex six-transistor memory cell which my team was using for each bit of data. That evening I started exploring the possibility of storing data in a simpler way as a charge level on a capacitor. Within a few hours I had gotten the basic ideas for the creation of DRAM ironed out in my mind."

His memory cell was as simple as it could be; it only contained two elements, a switch transistor and a capacitor. In many of today's technologies a trench with lateral dimensions of far less than a micrometer but more than five micrometer in depth is used to form the capacitor, as illustrated in the schematic in Fig.8. The DRAM has been driving microelectronics until today, has always been the first technology announced in a given generation, followed by the logic technologies and others. DRAM alone is a 25 billion dollar business, with 2.5 billion units sold in 1999.

To date, 1-Gb DRAM and microprocessors operating at a 600-MHz clock can be realized by using 0.18-μm minimum dimensions. The reason for the constant growth is a simple, but effective recipe to miniaturize CMOS transistors. This is the scaling theory presented by researchers of IBM in 1974. It says, that the device density can be increased quadratic and the circuit speed can be improved linearly, while keeping the power density constant. This forms the foundation of a strategy by the Semiconductor Industry Association to coordinate the progress in microelectronics developments, the so-called SIA Roadmap [8]. The association stated in 1994:

"A central assumption of the Roadmap is an extension of industry history according to Moore’s law."

Gordon Moore (Fig.10), the co-founder of Fairchild and Intel Corporations, postulated in 1965, that the density of integrated circuits will double every year [9]. He adjusted his prediction in 1975 to a more conservative twofold increase in device density every 1½ year. That corresponds to a new DRAM generation every three years. This evolution was true for Intel's microprocessors until recently. The SIA Roadmap considers today only a doubling of the integration density every two years. So we see, that the progress in microelectronics has been slowed down over time.

Less known, but related to the prediction of Moore is Macrone's law [10], saying that a computer in a certain category will always cost a fixed amount of money. That means that Moore's law will only work, if the cost per logic gate can be reduced at about the same rate. Another prediction on cost had been made by Rock [10], who foresaw a twofold increase in the cost of silicon manufacturing equipment every four years. This means,
that Moore's law will only hold, if the volume of semiconductor manufacturing can follow at about that rate in order to amortize fab equipment and infrastructure. A result of the extremely high cost in semiconductor technology development are the alliances of major microelectronic companies today. The dramatic decrease in the cost per transistor is, besides the physical limits in device miniaturization, the reason for a possible end of Moore's law, according to Ross [10]. He made a rather pessimistic prediction in 1995, saying:

"The price per transistor will bottom out sometime between 2003 and 2005. From that time on, there will be no economic point in making transistors smaller. So Moore's law ends in seven years".

Somewhere somebody even said:

"The end of Moore's law, thank Good!".

But will it be so simple? Microelectronics has become a basic resource in our personal and professional lives. The achievements in microelectronic manufacturing have been raised to an incredible level in production volume and feature precision. Let us try to visualize that through a couple of illustrative comparisons to the macroscopic world.

The total silicon wafer production in 2000 is expected to be an equivalent of 51.8 million eight-inch wafers [11]. Three billion DRAMs will be sold for a projected 28 billion US$. Silicon is gained from sand, in the form of single-crystalline rods, which are diced into silicon wafers. The volume of sand, which would support the entire silicon wafer production in 1999, will fit into only about six family homes. This amount appears to us as being very small, and we may wonder if that can really be the basis of the enormous microelectronics industry. But the comparison to the volume of a house is somewhat misleading. A house has three dimensions of the same magnitude. Silicon wafers, in contrast, are circular in shape with a diameter of about 18 cm and a thickness of about 500 µm.

We could now imagine that all silicon wafers produced in one year be stacked onto each other. On the slide in Fig. 11 this has been done for the 1999 wafer production.

![Stack of silicon wafers from the 1999 production in comparisons.](image)

The diagram puts the height of the resulting stack of silicon wafers used in 1999 for the fabrication of integrated circuits in a relation to the highest mountain on earth, the highest building, and the size of a common man.

![Number of trench-capacitors on a 8-inch DRAM wafer and world population](image)
Such a stack of silicon wafers would reach a height of 25 km, about three times the height of Mt. Everest. This is a bit more impressive, than looking at the volume of sand that supports silicon manufacturing, but now we should take into consideration, that submicrometer features are formed on the silicon wafers.

Looking at the DRAM, 256 million trench capacitors are on a single chip in manufacturing today [8]. The chip size is 132 mm² in production. That amounts to 60 billion trenches on an eight-inch wafer, many more than there are people on earth. The chart in Fig.12 illustrates that the number of trenches on an eight-inch wafer became equal to the earth population in 1992, neglecting for a moment that eight-inch, high-volume wafer production began after 1992.

![Figure 13](Image)

**Figure 13** Envisioned strings of capacitor trenches from a single 12-inch DRAM wafer and from the 1999 DRAM annual production in comparison to length measures of the macroscopic world.

This result is already quite impressive. But one should further realize, that those trenches have minimum lateral dimensions, yet their depth is comparably large. One should therefore try to visualize the total length of those densely integrated trench capacitors in a DRAM. The diameter of a trench capacitor is only about 180 nm, but it reaches to a depth of 5 to 10 μm into the silicon, which translates into an aspect ratio of 25 or higher. One could now envision that all the trenches on a single DRAM wafer or from the annual DRAM production be lined up to form a continuous string (Fig.13). For instance, a string formed by the trenches on an advanced 300-mm, 1 Gb DRAM wafer would have the incredible length of 1000 km. That compares to a considerable fraction of the Great Wall in China. If one extends this illustration to the annual DRAM production, the result will exceed imagination. The trenches from the entire 1999-DRAM production would not only exceed the length of the equator many times, but this would also be the case for the distance between earth and moon. In fact, it would equal that distance by an incredible 10,000 times!

Similar measures can be estimated for the maximum length of interconnect wire on chips.

Finally, one should put the power dissipated on a silicon chip into perspective. Integrated devices are operated at only a few volts, and the electrical currents reach only a few milli-amps, but this takes place in an extremely small volume. The results are very high relative power levels in terms of power per volume or power per weight.

![Figure 14](Image)

**Figure 14** Power per weight figures of dissipation in an interconnect wire of average length on chip and of high-speed bipolar transistor in comparisons to the macroscopic world.
In the comparisons illustrated in the diagram in Fig. 14, power is related to the mass of the body in which it is dissipated or generated. Using this formula, a horse generates a power per weight of 1 W/kg, while that value increases to nearly 1000 W/kg for a common car. The power dissipated in an interconnect wire of average length on a silicon chip is more than ten times higher than that value. The power per weight of a rocket engine, however, is another two orders of magnitude larger, reaching more than 1 MW/kg [13]. But this extremely high value is small compared to the power dissipated in a bipolar transistor. A 500 times larger power/weight figure than that of a rocket engine results for a high-performance device! How is that possible? Well, the difference is in the environments the two systems are operating in. In contrast to the rocket engine, that has to operate in the atmosphere and in space, the transistor is imbedded into silicon, which has an excellent thermal conductivity. That allows one to operate a transistor at this extremely high power-per-weight level, yet at a moderate temperature of about 100 °C.

![Power Diagram](image)

Figure 15 Active and standby power of different microprocessor technologies [14].

Ladies and Gentlemen,

Those illustrations and comparisons have shown, which level of precision, which device density, and which product volume have been achieved in microelectronics. We have seen that over the past 40 years a fascinating technology has been shaped. But we have also seen that the pace of device scaling has been reduced over time. As reasons for this trend we have identified the extremely high cost of the process development, but we should also be aware of the physical limits of device miniaturization. The four most serious limitations to CMOS scaling will be discussed in the following. I want to talk about the first three limits only very briefly.

First, the threshold voltage of the MOS transistors cannot be reduced below a certain value. This leads to a strong increase in standby power with miniaturization, even though standby power is assumed to be negligible in CMOS scaling theory.

Second, an increasing fraction of the average gate delay applies to the interconnects. The delay associated with the interconnects cannot be reduced in scaling.

Third, the gate oxide measures only a few atomic layers in state-of-the-art CMOS devices. This leads to an undesirable leakage current through this oxide.

The final scaling limit to be discussed here is a particularly interesting one. It deals with the fact, that the number of impurities added to the silicon active layers of the devices becomes so small that the randomness of their
incorporation into the silicon lattice can no longer be neglected. In previous generations we could rely on doping impurities, electrons, and holes as statistical measures. Electrical characteristics were attributed to the average electron and the average hole in the silicon lattice or at the silicon surface. At the nanometer device dimensions, we are going to face in the near future, we will have to consider the individual electron and the individual hole. This is a tremendous challenge and possibly a limit to the mass production of the classical devices. Ironically, it is the step to nanotechnology, a future technology in which one intentionally wants to take advantage of single-electron events and quantum effects [15]. This is called dry nanotechnology.

Dry nanotechnology is the consequent continuation of microelectronic device scaling, but may lead to changes in system architecture, for instance through the availability of multiple logic levels, since quantum effects can be exploited. Ultimately, it is about precise placement of individual atoms, as illustrated by the atomic-scale abacus demonstrated by researchers at IBM and shown here in Fig. 17. The other type of nanotechnology is the so-called wet nanotechnology.

[16], which is going to emerge from biotechnology rather than from microelectronics. Both types of nanotechnology are in what we called earlier the initiation phase. They are expected to reach the development level, which we now experience in microelectronics, in the future and have the potential to exceed the computational performance of microelectronics by far.

But the outcome is not clear, and it will certainly take a while until we know better. For nanotechnologies to take over the business from microelectronics it is very important to realize, that they can do that only if they outperform microelectronics in all aspects. That means product volume, integration density, computational speed, and cost. The chart in Fig. 18 illustrates the estimate, that this may take about 20 years. Even if the progress in the development of microelectronic fabrication processes is going to saturate in a couple of years, there is still a lot of room for improvement in custom circuit design and system architecture. This is in the beginning just now. It is likely that it will take at least until 2020 that dry nanotechnology would become the dominant logic technology. It may take more than 10 years thereafter until wet nanotechnology comes strongly into the picture.

Besides these straightforward efforts to improve the performance of computing machines, there is a new trend to apply silicon technology to communications. This links back to the early days of electronics, when the development of electronic devices was devoted to the transmission of voice and data by wires or through the air by radio waves. If we talk about communications, and wireless communications in particular, we have to look back to the work of

![Figure 17: Atomic-scale abacus (IBM).]

![Figure 18: Speculative technological evolutions of microelectronics and dry and wet nanotechnologies.]

![Figure 19: Nicola Tesla 1856 - 1943]
Nikola Tesla (Fig. 19). He invented the induction coil, demonstrated the first radio transmission in 1893, and made long-distance radio transmission possible [17]. He attempted wireless communications in different ways, first through the surface layer of the earth and later in 1899 through the air by using his legendary communications tower on Long Island.

Tesla, not Marconi, is seen as the father of radio communications, as ruled by a US court.

Tesla did not only think about the exchange of information, but also about the distribution of energy around the globe, as well as about the societal effects of his invention. He stated:

"The greatest good will come from the technical improvements tending to unification and harmony, and my wireless transmitter is preeminently such. By its means, the human voice and likeness will be reproduced everywhere, and factories driven thousands of miles from waterfalls furnishing the power. Aerial machines will be propelled around the earth without a stop and the sun's energy controlled to create lakes and rivers for motive purposes and transformation of arid deserts into fertile land."

![Figure 20. Tesla's communication tower on Long Island.](image)

Figure 20. Tesla's communication tower on Long Island.

![Figure 22. Development trend of networked homes in the US.](image)

Figure 22. Development trend of networked homes in the US [19].

Tesla's thoughts on energy distribution 100 years ago were truly amazing. For them to eventually become reality we still have to be patient. Very real, however, are his concepts on wireless communications. New applications are just emerging in this field. We see them in enterprise systems in form of local and wide area networks, in handheld mobile devices for communications and data transfer, for global positioning and collision avoidance in automotive applications, and many others (Fig. 21). They are at the periphery of a network infrastructure, consisting of telephone and cable providers, cellular base stations, network nodes, and satellites. Those new communications markets grow at a much faster rate than microelectronics. In many areas, they are still in the initiation phase, but a
A large part of the communication business is already in the growth phase. There is a good chance that communications may reach or extend beyond the volume of stationary logic applications. For communications to sustain the rapid growth, it will be essential to prepare silicon technology for this market, for which the transistor originally was invented. Handheld wireless communications, in particular, can ideally be based on silicon fabrication processes.

Silicon technology provides the high product volume, low cost, low power consumption, and small form factor, which are important attributes in this market. One can take advantage here of new technological advancements, such as high-frequency silicon-germanium transistor, silicon-on-insulator substrates, and copper metallization. As an example, one can take a look at the developments of wireless networked homes in the US [19]. The concept behind the networked home is that services within the home are connected to each other and to the outside world. Connection can be achieved by phone line, through the power lines, or wireless. The number of home-networked households in the US is currently doubling every year, and for 2003 still a growth of 50% per year is forecasted. The wireless systems will increase from about 10% to 25% in 2003 (Fig.22). The growth in communications is currently clearly bypassing the growth in microelectronics, which is about 20% per year.

About the need for wireless communications there should absolutely be no question, if we take a look at the photo of the Boston Central Telephone Station in 1881 after a severe blizzard (Fig.23).

It has been a long way from Bell's first telephone for wired communications in 1875 (Fig.24) to the wireless transceiver chip shown in Fig.25. Many different components are part of the transceiver. More than 400 parts are assembled on a printed circuit board in a cellular hand-held phone. This type of assembly sets a lower limit for the size of the equipment.

Figure 24 Bell's first telephone, 1875.

Figure 25 Advanced SiGe RF front-end chip by IBM, 2000.

Figure 23 Boston central telephone station after blizzard, 1881 [20].

Figure 26 Evolution of form-factor of portable wireless units [20].
The trend clearly points in the direction to reduce the form factor (Fig. 26). From the Chicago Trial Equipment in 1978, which had a volume of 33,000 cm³, to today's portable phones with a size of about 250 cm³, to PCMCIA cards and soft radios at 1 to 2 cm³, enormous improvements have been made. The ultimate goal is the fully integrated radio transceiver. At frequencies above 15 GHz, the antenna and other components can also be integrated on the chip.

One example is smart tags that are charged with power and respond stored information through a wireless link. Others are combined with an integrated microsystem to provide wireless information about their location and the condition of their environment. Since the production of such microscale transceivers can be completed in batch processing in a silicon fabrication facility, the cost will be very low and a new market of disposable products can emerge. This opens up entirely new applications for instance in the biomedical and environmental fields.

One challenge, however, remains on the way to chip-scale transceiver systems. They will have to be fabricated in planar silicon process technology to retain the economic advantage. Planar technology, as we have discussed earlier, is designed to integrate electronic functions at an utmost density, and is not in all aspects well suited for the integration of radio-frequency transceivers. A solution to the problem can be expected from micromachining techniques (Fig. 27). They allow the structuring of the uniform silicon substrate or the fabrication of high-aspect-ratio structures above the silicon surface. This would make the third dimension fully available for component integration. Finally, micromechanical structures, such as microswitches, and electromechanical components could be integrated.

This brings me to some hypotheses:

As that becomes possible, one could consider chip-scale packaging and wireless power supply, and so reduce the volume of the radio to 0.1 cm³ or below. This will open the door to entirely new products and applications.

Figure 27 Examples of micromachined silicon technology structures [21], [22].

After having looked at the factors, that are driving microelectronics, and after having realized the level of precision and density, that can be achieved in planar silicon technology today, we should be convinced that this technology has an enormous momentum, in spite of the physical limits in device scaling. Microelectronics will maintain momentum at least over the next 20 years, until dry or wet nanotechnology have moved to the same level. In spite of the expected saturation of the integration density in microelectronics, silicon technology will remain a major industry due to the new directions, in particular
communications. Communications is emerging at an extremely rapid pace and will be more and more based on silicon technology. While the logic processor market aims for "a PC in every home", communication devices are expected in many forms and applications in private households. Applications in the commercial markets can be expected at least to the same degree, especially if disposable communications devices, combined with microsystems, become feasible. It is therefore very likely that communications will drive microelectronics in the future.

Shortcomings of silicon-based transceiver systems will be overcome through an application of micromachining techniques, which are compatible with microelectronics fabrication processes. Micromachining will thus become an enabling technology for future wireless communications.

Micromaching will also lead the way to chip-scale packaging of wireless systems. The fact, that wireless transceivers can be fabricated at an extremely small size and at very low cost, will open up entirely new markets, in which disposable products will dominate. Here are tremendous opportunities for innovation and new applications.

I would now like to conclude and make a brief statement about my plans for contributions in research and education in Delft, as well as some personal thoughts. The TU Delft, and the research school DIMES in particular, are very well suited to meet the challenges in microelectronics, to contribute to the transition to nanotechnology in the future, and to be a leader in research on communications technology based on silicon. Micromachining of silicon, high-speed device technologies, microwave techniques, high-frequency circuit design, system architecture, and CAD tool development are pursued at a high quality level at DIMES. Those disciplines form in a natural way the basis for the research directions in silicon RF technology for communications, as it was just lined out.

My ambition is therefore to build up a research theme "High-Frequency Technologies for Communications" at DIMES based on the existing infrastructure and by stimulating new directions. Micromaching techniques, chip-scale packaging, and concepts for wireless transponder and disposable systems are some of the new focus areas.

The main task in education should be to attract and prepare new talent in electrical engineering, and in microelectronics in particular, for the needs of the industry. Engineering does currently not enjoy a very high image, but that will have to change, looking at the challenges ahead. In order to manage our living conditions in the future, we will have to be able to deal in the best way with food supply and waste, with the efficient generation and distribution of energy, with the condition of our environment and climate, and many more tasks. All that will require high-level engineering. I believe, that communications technology can be instrumental in making our work more efficient and will allow us to decentralize work places. Communications technology can therefore help to reduce traffic, it can be useful in traffic logistics, it can be effective in monitoring our environment, and it can help to improve the food supply and waste management process. This message has to be brought to the schools in the Netherlands, and we will have to motivate more women to seek a career in engineering in order to provide long-term solutions to the serious shortage in engineers. As a short-term solution we can take advantage of the open borders within Europe and assist the industry in attracting microelectronic engineers through the Erasmus and Socrates programs to come to the Netherlands. Further, the university should help in finding and educating engineering talent from other foreign countries. This mission in education already makes the university and the industry to close allies.

The same applies to research. Industrial research in microelectronics has been scaled back since the late eighties. This puts now a much stronger attention to the
Research programs at universities, the T U Delft, and the research school DINES in particular, are in the best position to be a world-class research laboratory in silicon-based communications technology. I am proud to be part of this effort, and I am looking forward to work together with the people at the faculty ITS and at the research school DINES in the years to come.

What better place than Delft to take on those challenges!

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