

Design and Fabrication of On-Chip Cooing Devices Based on the Peltier Effect

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Contents

Abstract.....	1
Acknowledgements	1
Chapter 1 Introduction.....	1
1.1 Peltier cooling effect and its application.....	1
1.2 Thermoelectric materials.....	2
1.3 Challenges of the cooling devices	4
1.4 Overview of the report	5
Chapter 2 Design.....	6
2.1 COMSOL simulations	6
2.1.1 Cross section model	6
2.1.2 Top view model	10
2.2 Device layout.....	16
2.3 Test structures and alignment markers	18
2.4 Conclusion.....	21
Chapter 3 Patterning Bi ₂ Te ₃ and Sb ₂ Te ₃	23
3.1 Dry etching method	23
3.1.1 Reflow of the photoresist.....	24
3.1.2 Tungsten as a hard mask.....	26
3.1.3 Dry etching with improved W mask	31
3.1.4 Dry etching with Si ₃ N ₄ as the hard mask	32
3.2 Wet etching method.....	32
3.3 Conclusion.....	38
Chapter 4 Processing.....	39
4.1 Processing Challenges	39
4.2 Preliminary experiments	40
4.2.1 Deposition and uniformity of Bi ₂ Te ₃ / Sb ₂ Te ₃	40
4.2.2 Adhesion testing.....	41
4.3 Flow plan.....	42
4.4 Initial flow chart and processing	44

4.5 Final flow chart and recommendation	51
4.6 Conclusion.....	51
Chapter 5 Measurements	53
5.1 measurement setup.....	53
5.1.1 Sheet resistance.	53
5.1.2 Contact resistivity.....	54
5.1.3 Device resistance.....	55
5.1.4 Seebeck coefficient	56
5.2 Results.....	57
5.2.1 Measurement of the cross structure.....	58
5.2.2 Measurement of the cooling devices.....	58
5.3 Simulation result vs. Measurement result	61
5.4 Conclusion.....	63
Chapter 6 Conclusion	64
References.....	65
Appendix A.....	66
Appendix B	69
Appendix C	72
Appendix D.....	73

Abstract

The aim of this thesis project is to design and fabricate a high efficiency on chip cooling device based on the Peltier effect. Bismuth telluride (Bi_2Te_3) and antimony telluride (Sb_2Te_3) are employed to form thermocouple for their high Seebeck coefficient and high figure of merit. The models of the devices are simulated in the software program COMSOL, and based on simulation results, a set of masks are designed. The patterning methods are investigated, and wet etching is chosen for its simplicity and smooth edge, although the lateral undercut is 4-5 times of the layer thickness. The wet etchant is $\text{HCl}:\text{HNO}_3:\text{H}_2\text{O}=3:1:2$ for Bi_2Te_3 , and $\text{HNO}_3:\text{H}_2\text{O}=1:1$ for Sb_2Te_3 . The devices are tested on the probe station and under the thermal camera. The combined Seebeck coefficient is $282\mu\text{V/K}$. A maximum cooling temperature of 3.3K is observed.

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Chapter 1 Introduction

The aim of this thesis project is to design and fabricate a high efficiency on chip cooling device based on the Peltier effect, which describes the cooling phenomenon when a current is applied through a junction. The cooling device is designed for a CO₂ sensor in a breathing machine, with quick response due to the active heating and cooling. Bismuth telluride (Bi₂Te₃) and antimony telluride (Sb₂Te₃) are selected as the thermoelectric materials for the high Seebeck coefficient, α , and high figure of merit, Z.

The main challenges of this project are in the processing of the thermoelectric materials, which are the selection of the suitable substrate for Bi₂Te₃ and Sb₂Te₃, the method to pattern them and the capping of these materials. We start our project from solving these questions.

The cooling devices are first simulated to get the optimal dimensions, then based on the simulation result, a set of masks are designed. Several wafers are processed in the cleanroom, on which after the processing the parameters of Bi₂Te₃ and Sb₂Te₃ are measured, and the cooling ability is tested.

1.1 Peltier cooling effect and its application

The Peltier effect was discovered by Jean Peltier, a French watchmaker in the 19th century. It describes that if we put two conductors together and make a junction, heat would be generated or absorbed at the junction depending on the polarity of the injecting current. We could realize the heating and cooling function using the same device only by reversing the supply current. The Peltier effect is brought up because the energy of the charge carriers in the different conductors governing the conduction process differs from material to material; at one junction, this difference in energy must be provided by the lattice causing cooling of the junction, and at the other junction the difference in energy is released into the lattice, thereby causing heating of the junction.[1]

The Peltier effect drew much attention twenty years ago when people tried to develop a simple device which can heat in the winter and cool in the summer. However it faded out of our concern because the thermal efficiency is too low. Now Peltier devices are only used for battery powered traveler refrigerator and dew point humidity sensors. If we could improve the thermal efficiency, on-chip cooling based on the Peltier effect would be interesting.

As the growing of integrated circuits and the MEMS technology, on-chip cooling seems a good idea to add in a circuitry. On the one hand, the scaling down of ICs

increases the circuit density, and increases the power consumption per unit area, which could cause hot points on the chip. A Peltier device can provide a small cooling area such that the cool point may compensate the hot point, and hence provide a flatter thermal profile. On the other hand, adding resistors or conductors to a Peltier device can make an on chip humidity sensor, or a CO₂ sensor. The humidity could be measured by gauging the resistance or capacitance when we decrease the temperature causing the water in the air to condensate on the cooled surface. The temperature at which condensation takes place is the dew point. At the dew point, the resistance of the condensate water drop is a function of the drop thickness and the resistivity of the water, which is a function of the CO₂ concentration, and the capacitance of the drop is a function of the drop is a function of the drop thickness and the dielectric constant, which is also a function of the CO₂ concentration. Hence, the CO₂ concentration could be measured exploiting the relation between the resistance and the capacitance of the condensate water and dissolved CO₂ in the liquid film

Another application of the on chip cooling device is therapeutic. One group in University of Minnesota Medical School reported that the focal cooling of the neocortical epilepsy area to less than 24 degree C aborted seizures within a few seconds, without significant cortical damage. So an extremely thin thermoelectric device is needed for seizure detection and treatment system. [2]

In this project, the purpose of the on chip cooling device is to build a fast responding CO₂ sensor, with quick response due to the active heating and cooling, in a breathing machine to detect the CO₂ density the patient is breathing out.

In conclusion, the Peltier effect is an interesting phenomenon that a junction of conductors could heat and cool just by injecting a current and reversing the polarity. Peltier devices are used mainly for small refrigerators now, but it is significant to make Peltier devices for on chip cooling.

1.2 Thermoelectric materials

When we choose the suitable material for a Peltier cooling device, several parameters should be considered. First let us have a look at the expression of the cooling power q_c . [3]

$$q_c = (\alpha_2 - \alpha_1)IT_c - \frac{I^2 R}{2} - K(T_H - T_c)$$

The cooling power of a Peltier device contains three parts in the expression. The first part is the heat absorption due to the Peltier effect, which is determined by the Seebeck coefficient α of the two materials. T_c is the temperature of the cold junction, and I is the applied current. The Seebeck coefficient is defined as the output voltage divided by the temperature difference when the two ends of a thermal electric material are applied with different temperatures. $\alpha = \frac{\Delta V}{\Delta T}$. A material with a higher Seebeck coefficient gives more cooling power, and is more suitable for Peltier devices.

The second part is the heat generation due to the Joule heat. R is the resistance of the thermocouple, and is expressed as follows.

$$R = \frac{l1}{A1 * \sigma1} + \frac{l2}{A2 * \sigma2}$$

in which L is the length and A is the cross section area of the materials, and σ is the electrical conductivity. To diminish the influence of the Joule heat, material with a higher electrical conductivity is preferred since it gives lower resistance and less Joule heat.

The third part in the expression of the cooling power is the thermal conduction between the hot junction and the cold junction. K is the thermal conductivity of the thermocouple, which could be expressed as

$$K = \frac{A1K1}{l1} + \frac{A2K2}{l2}$$

in which A is the cross section area, L is the length and K is the thermal conductivity of the two materials to form the thermocouple. Much of the temperature difference generated by the current is lost by the thermal conduction through the material between the cold side and the hot side. Therefore, lower heat conductivity is required.

The maximum cooling temperature due to the Peltier effect is :

$$\Delta T_{\max} = \frac{1}{2} Z T_c^2, \text{ [Page 34 in reference 4]}$$

in which Z is defined as the figure of merit of the thermocouple, $Z = \frac{(\alpha_1 - \alpha_2)^2}{KR}$.

Hence, thermocouple materials with higher difference in Seebeck coefficient, lower total resistance and lower total thermal conductivity would show stronger Peltier cooling.

When we choose the suitable material for the thermocouple, we could refer to the figure of merit, z, of the thermoelectric material. z is defined as follows:

$$z = \frac{\alpha^2 \sigma}{\kappa} \text{ [Page 27 in reference 4]}$$

in which α is the Seebeck coefficient, σ is the electrical conductivity, and κ is the thermal conductivity. The material with a higher figure of merit, z, is preferred for the manufacturing of a Peltier cooling device.

The Seebeck coefficient α and the figure of merit Z of the commonly used materials are listed in table 1.1.

Table 1.1: Seebeck coefficient and figure of merit of materials

Material	Seebeck coefficient(uV/K)	Electrical conductivity(Ohm*um)	Figure of Merit ($10^{-3}K^{-1}$)
Poly-Si	190	58	0.037 [Page 65 in reference 4]
Bi ₂ Te ₃	-248	12.6	2.87[7]
Sb ₂ Te ₃	188	12.6	1.63[7]

Silicon has a high Seebeck coefficient, but the figure of merit is low because of the high thermal conductivity. Hence, silicon is not an appropriate material for on chip cooling. Bi_2Te_3 and Sb_2Te_3 have high Seebeck coefficients and high figures of merit, so they could be used for high efficiency on chip cooling devices. The Seebeck coefficient of Bi_2Te_3 is negative, and that of Sb_2Te_3 is positive. If we employ these two materials to form a junction, the combined Seebeck coefficient would be

$$\alpha_{\text{total}} = \alpha_{\text{Bi}_2\text{Te}_3} - \alpha_{\text{Sb}_2\text{Te}_3} = -248 - 188 = -436 (\mu\text{V} / \text{K})$$

These two materials have been studied extensively. One group in Cardiff University, UK, fabricated a device, shown in Fig1.1, with 700nm Bi_2Te_3 and Sb_2Te_3 film deposited by co-evaporation, and got a maximum cooling temperature of $\Delta T = 15.5\text{K}$ [8]; another group in Taiwan employed 8 μm thick Bi_2Te_3 and Sb_2Te_3 films on polyimide flexible substrate, patterned the film with dry etching, and got a maximum cooling temperature $\Delta T = 1.2\text{K}$ [9]. The most successful on-chip thermoelectric cooling device is developed by MicroPelt, a company in Germany. They deposited and patterned 8 μm Bi_2Te_3 film on one wafer, and fabricated the (Bi, Sb) $_2\text{Te}_3$ part on another wafer, after which the two wafers were bonded. The maximum cooling temperature was $\Delta T = 32\text{K}$ @ 85 degree C, vacuum[10]. The structures are shown in Fig1.2.

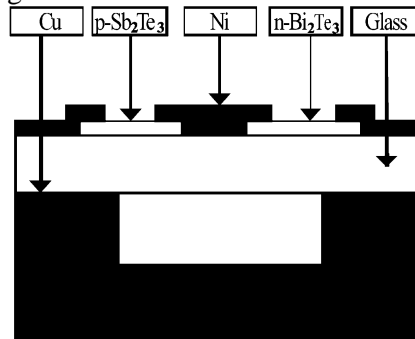


Fig 1.1 a lateral Peltier cooling device with a maximum temperature drop 15.5K

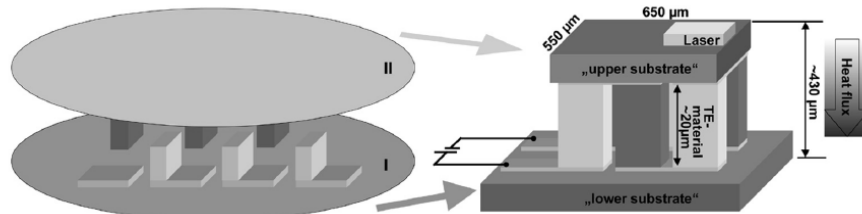


Fig 1.2 transversal cooling device by MicroPelt Company [5]

1.3 Challenges of the cooling devices

The main challenge of this project is the adhesion problem of Bi_2Te_3 and Sb_2Te_3 to the substrate. Bi_2Te_3 and Sb_2Te_3 adhere very well to metal electrodes, for example TiW. However, the adhesion of Bi_2Te_3 to Si [11] and to SiO_2 is poor; the film of Bi_2Te_3 delaminated in the areas with bare SiO_2 substrate during the development. [12] Based on Reference [7] and [14], polyimide and silicon nitride could be possible

substrates, but we have to investigate the adhesion in the experiment, and treat the material carefully during the process.

Patterning of the film is the second challenge. In the literature, usually two patterning approaches are reported, the first of which is lift-off [7]. However, the deposition of Bi_2Te_3 and Sb_2Te_3 could probably cause un-removable photoresist, so the photoresist should be carefully chosen. The other approach is etching, including wet-etching and dry-etching. According to the literature, the horizontal undercut is more than five times the thickness in the wet etching process, which is quite a lot given the thickness of the layers [12]. Ion beam dry etching seems a good choice, except for the sidewalls due to re-deposition during the process, which could probably cause problems in the later capping step.

Another challenge is the capping of the high ZT layers. Bi_2Te_3 and Sb_2Te_3 must be fully capped because they tend to react with other etchants in the following steps. SiO_2 is not an option for its poor adhesion, in this respect Si_3N_4 seems a good candidate. But there are two problems with Si_3N_4 as a capping layer, one of which is that the deposition temperature is always higher than 300 degree C, which is above the evaporation temperature of the materials (290 degreeC, [13]). The other problem is that the thermal conductivity of Si_3N_4 is very high. Introducing Si_3N_4 as the capping material could diminish the high figure of merit of Bi_2Te_3 and Sb_2Te_3 . Another suitable capping material is Parylene, which has never been used in similar devices before. Parylene is deposited at room temperature, and the step coverage of Parylene is excellent. An important benefit of Parylene is the low thermal conductivity, only $0.08\text{W}/(\text{m}\cdot\text{K})$, comparing with Si_3N_4 $20\text{W}/(\text{m}\cdot\text{K})$. The capping material must be deliberately thought over.

This thesis focuses on the three challenging aspects, the adhesion of the high ZT materials to the substrate, the patterning approach, and the capping material.

1.4 Overview of the report

This report consists of six parts. The principle and application of the Peltier effect, the choice of Bi_2Te_3 and Sb_2Te_3 as suitable material, and the challenges of this project are described in the first chapter, the introduction. The second chapter shows how the devices are designed, from the aspect of thermal model simulation using finite element software package COMSOL, and also from the aspect of transferring the devices and test structures into layout using Cadence. In the third chapter, the patterning method of the thermoelectric materials is presented and discussed. The forth chapter details the processing plan, the preliminary experiments and the final flow chart. The testing and characterization of the devices is reported in chapter five. Chapter six gives the conclusion and the recommendation of the flow process. At last, the reference literature is listed.

Chapter 2 Design

The thermal behavior of the Peltier cooling devices is simulated using the finite element software COMSOL to get a general idea of the thermal profile and the optimal dimensions. After that, the layout of several devices with optimal dimensions is implemented in Cadence. At last, different test structures for sheet resistance, contact resistance, Seebeck coefficient, etc. are added to the layout.

2.1 COMSOL simulations

Since silicon has a very high thermal conductivity it will diminish the temperature difference between the hot and cold ends. Therefore the substrate underneath the thermocouple(s) should be a membrane or a thin film instead of bulk silicon. In the cooling mode, the thermocouple absorbs heat at the cold end and releases heat at the hot end. Hence, it is better to put the hot end on the heat sink, which is bulk silicon, to absorb the excess heat and maintain the temperature. Therefore, polyimide is used for the membrane for its robustness and low thermal conductivity. We simulated the thermal profile in two models, the cross section model and the top view model.

2.1.1 Cross section model

The cross section profile is studied in this model. We use a silicon wafer as the support and the heat sink, and a 10 μm polyimide layer as the membrane. The Bi_2Te_3 and Sb_2Te_3 layers are located on the membrane, and have identical thickness of 1 μm and length 200 μm . The bottom electrode is made of 200nm tungsten, and the capping

SiO_2 is 500nm. We start with the following dimensions: the length of the thermocouple is 200 μm ; the distance between these two materials is 60 μm ; and the length of the membrane is 460 μm ($2 \times 200 + 60 \mu\text{m}$), as demonstrated in Fig 2.1. We

also assume the width of the device is 100um, and the contact area is 100um*20um.

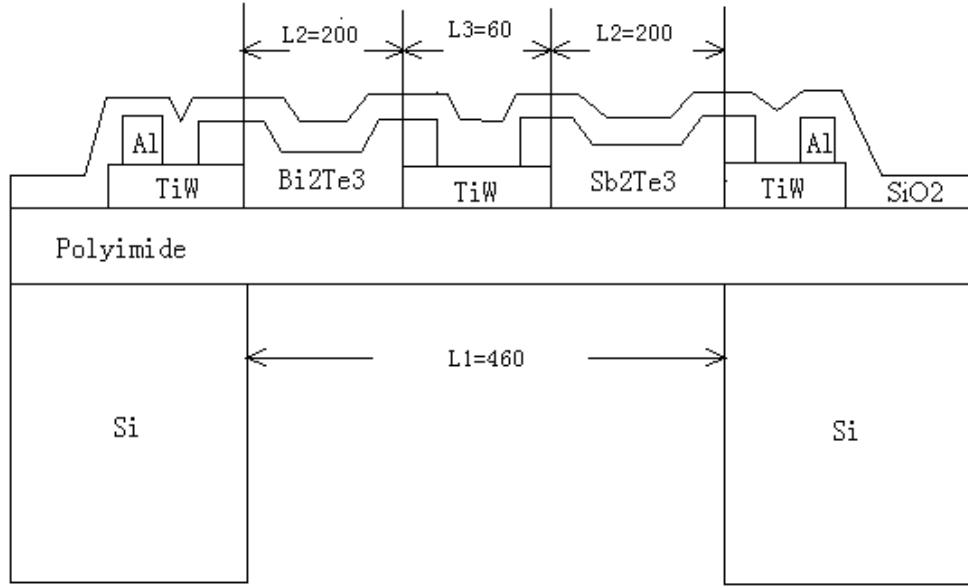


Fig 2.1 Demonstration of the cross section model

We could change the length of the membrane (L_1 in Fig 2.1), the length of the thermocouple (L_2 in Fig 2.1), and the distance of the 2 thermoelectric materials (L_3 in Fig 2.1), to see the influence on the thermal profile and the maximum cooling temperature. Based on the analysis, the optimum of the dimensions L_1 , L_2 , and L_3 could be determined.

Several boundary conditions and constants should be mentioned:

(1) The power per unit square absorbed at the interface area of TiW and Bi_2Te_3 due to Peltier effect is

$$q_0 = \frac{\alpha_{\text{Bi}_2\text{Te}_3} * T_c * I}{l_c * w_c}$$

in which $\alpha_{\text{Bi}_2\text{Te}_3}$ is the Seebeck coefficient of Bi_2Te_3 , T_c is the temperature of the cold junction, I is the applied current, l_c is the length of the contact area, and w_c is the width of the contact area.

The case for Sb_2Te_3 is quite similar. The heat power per unit absorbed due to Peltier effect at the interface is:

$$q_0 = \frac{\alpha_{\text{Sb}_2\text{Te}_3} * T_c * I}{l_c * w_c}.$$

in which $\alpha_{\text{Sb}_2\text{Te}_3}$ is the Seebeck coefficient of Sb_2Te_3 .

(2) The Joule heat power per unit volume released uniformly in the Bi_2Te_3 film is:

$$Q = \frac{I^2 * R}{\text{Volume}} = \frac{I^2 * \rho_{\text{BiTe}}}{w^2 * d^2}$$

in which, I is the applied current, ρ_{BiTe} is the resistivity of Bi_2Te_3 , w is the width of the Bi_2Te_3 structure, and d is the thickness of the structure.

The Joule power in Sb_2Te_3 film is

$$Q = \frac{I^2 * R}{\text{Volume}} = \frac{I^2 * \rho_{\text{SbTe}}}{w^2 * d^2}$$

in which ρ_{sbte} is the resistivity of Sb_2Te_3 .

(3) The contact resistance R_c between TiW and Bi_2Te_3 , and TiW and Sb_2Te_3 is neglected, since it is unknown and it affects little on the optimal dimensions of the device.

The devices are assumed in the vacuum, so all the outside boundaries are thermal isolated.

(4) Related constants are as follows:

ρ_{bite}	12.6e-6 Ohm*m
ρ_{sbte}	12.6e-6 Ohm*m
$\alpha_{\text{Bi}_2\text{Te}_3}$	248e-6 V/K
$\alpha_{\text{Sb}_2\text{Te}_3}$	188e-6 V/K
l	240e-6 m
w	100e-6 m
d	1e-6 m
T_c	273.15K
l_c	20e-6 m
w_c	100e-6 m
κ_{SiO_2}	1.4W/ (m*K)
$\kappa_{\text{Si}_3\text{N}_4}$	20 W/ (m*K)
κ_{BiTe}	1.2 W/ (m*K)
κ_{SbTe}	1.2 W/ (m*K)

The thermal profile simulate by COMSOL is shown in Fig2.2, in which we could get a general idea how the device works.

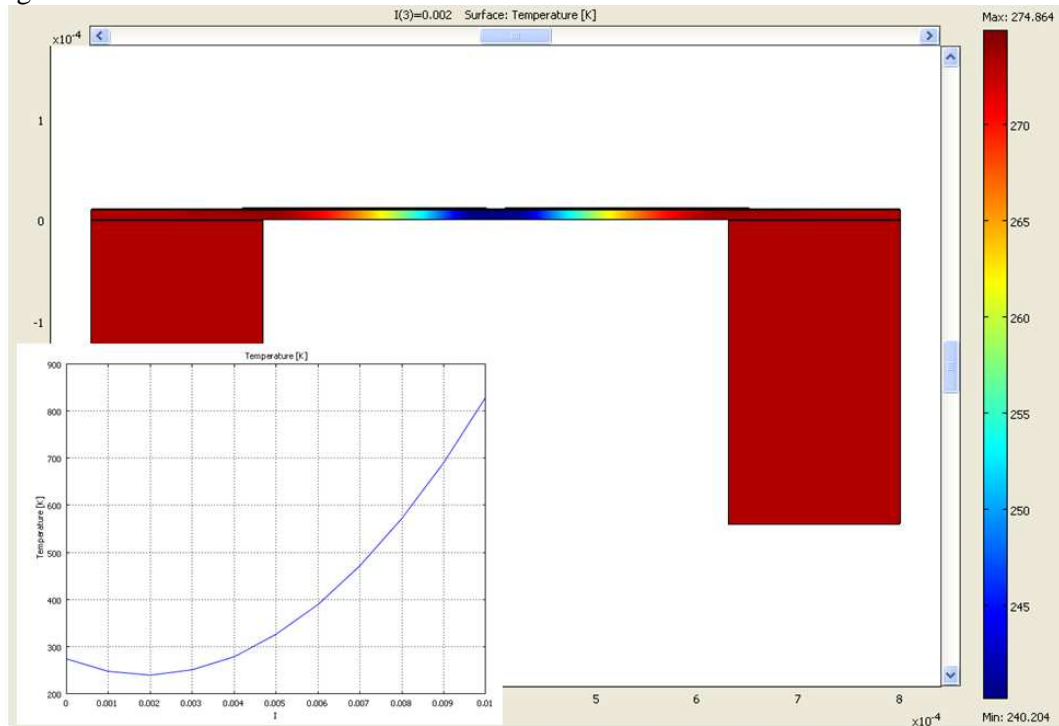


Fig 2.2 simulation result for the cross section model, with the maximum temperature drop 32.946K

Fig 2.2 shows that the cooling part is at the central electrode while the hot end has the same temperature as bulk silicon, since the bulk silicon acts as a heat sink.

The insert in Fig 2.2 shows the temperature of the central electrode as a function of the applied current. At 0mA, the temperature of the electrode is the same as the environment temperature, $T_c=273.5K$. As the applied current increases, the temperature decreases, since the cooling power of the Peltier effect is proportional to the input current. However, when the current exceeds 2mA the temperature increases with increasing current. At $I=10mA$, the electrode is even heated up to over 800K. The balance between the heat pumped away from junction, which is proportional to the applied current, and the joule heat conducted to the junction, which is proportional to square of the current, gives rise to the existence of minimum cooling temperature. For the device shown in Fig 2.1, the minimum electrode temperature is 240.204K, and the maximum cooling temperature is $\Delta T = 273.15K - 240.204K = 32.946K$

Now we change L_1 , the length of the membrane, and keep the other parameters unchanged, and check the result to get an optimal L_1 . The result is listed in Table 2.1.

Table 2.1: simulation result for models with different membrane lengths

L_1 (um)	Minimum temperature (K)	Temperature change (K)	Applied current (mA)
260	242.992	30.158	3
460	240.204	32.946	2
520	241.688	31.462	2
600	246.463	26.687	2

$L_1=460um$ gives the optimal result, when the edge of the membrane is just aligned to the edge of the TiW electrode ($L_1=2*L_2+L_3$ in Fig 2.1). This is because if the membrane is too small, the distance from the heat sink and the cooling electrode would be too short, leading to more thermal conduction; if the membrane is too big, the hot side of the Peltier device would not contact the heat sink, causing the temperature of both cold side and hot side to increase. Fig 2.3 shows the thermal profile with $L_1=260um$ and $L_1=600um$.

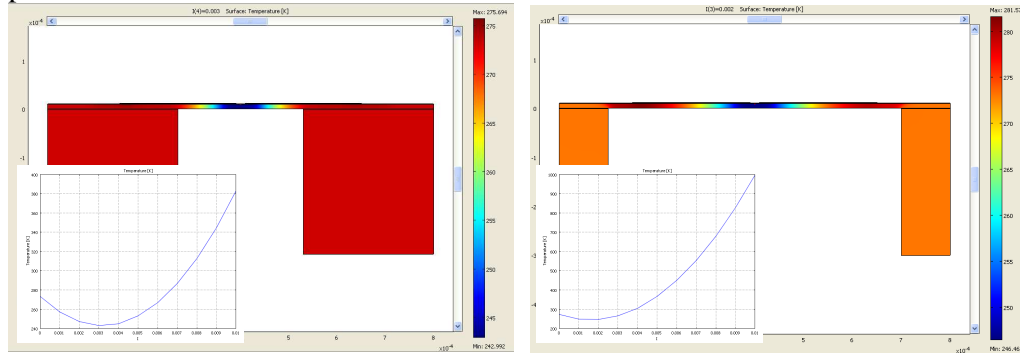


Fig 2.3 simulation result for left: $L_1=260um$, and right: $L_1=600um$

The optimum L_1 gives us a condition for L_2 , the length of the thermocouple and L_3 , the distance between the two thermocouples, which is $L_1=2*L_2+L_3=460um$. So when we increase L_2 , L_3 will decrease twice the increase value of L_2 . We change L_2 to 150um, 190um, and 205um, and get an optimum L_2 .

The simulation result is listed, in Table 2.2. The minimum temperature decreases as L2 increases, which means we should put the two thermal materials as close as possible. However, the minimum temperature does not change much.

Table 2.2: simulation results for models with different lengths of thermocouples

L2(um)	L3(um)	Minimum Temperature (K)	Temperature change(K)	Applied Current(mA)
150	160	242.428	30.722	2
190	80	240.36	32.79	2
200	60	240.204	32.946	2
205	50	240.18	32.97	2

2.1.2 Top view model

The top view thermal profile is studied in this model. We still use polyimide as a membrane, TiW as electrodes, and Al as bond pads. The size of the model is 890um*890um, and the square membrane size is 430um*430um. The length and the distance of the thermocouple are fixed, and the lengths of Bi_2Te_3 and Sb_2Te_3 are identical. The width of the thermocouples is the parameter we are studying. To simplify the model, we assume the contact width is the same as the width of the thermocouple, $w_c = W$. The width is first set to 110um, so we could get a brief idea of the thermal profile in the device as demonstrated in Fig 2.4

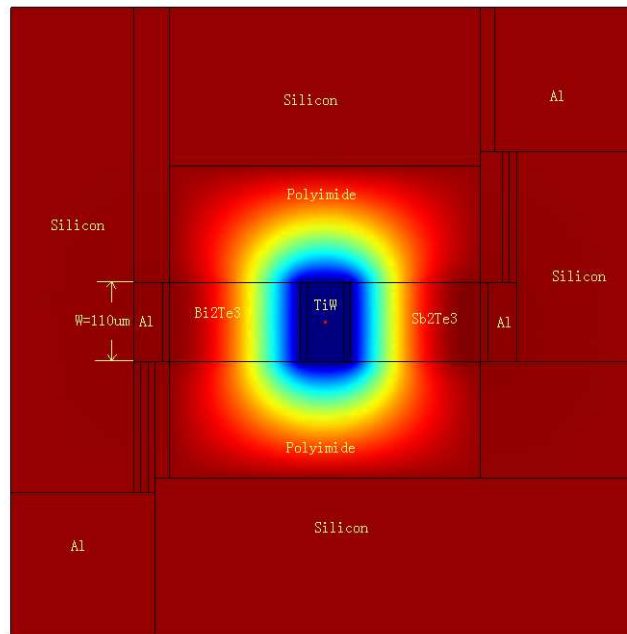


Fig 2.4 demonstration of the top view model

Several boundary conditions and constants must be mentioned

(1) The Joule heat per unit volume along the thermal material Bi_2Te_3 could be expressed as

$$Q = \frac{I^2 * R}{Volume} = \frac{I^2 * rho_{bite}}{w^2 * d^2}$$

in which I is the applied current, rho_bite is the electrical conductivity, w is the width of the thermocouple, and d is the thickness of the thermocouple.

Similarly, the Joule heat along Sb₂Te₃ could be expressed as

$$Q = \frac{I^2 * R}{Volume} = \frac{I^2 * rho_{sbte}}{w^2 * d^2}$$

in which rho_sbte is the electrical conductivity of Sb₂Te₃.

(2) The case for contact area between TiW electrode and the thermoelectric material is a little complex, since Peltier effect gives excess thermal generation and absorption other than Joule heat. Considering both effects, the thermal power per unit volume released in the contact area at the cold end of Bi₂Te₃ (in the middle of the membrane) is

$$Q = \frac{I^2 * rho_{bite}}{W^2 * d^2} - \frac{\alpha_{bite} * I * T_c}{lc * wc * d}$$

in which rho_bite is the electrical conductivity, and α_{bite} is the Seebeck coefficient of Bi₂Te₃, W is the width of Bi₂Te₃ thermocouple, and lc, and wc are the length and width of the contact. The contact width wc equals W.

At the hot end of Bi₂Te₃ (at the edge of the membrane), the power generated per unit volume is

$$Q = \frac{I^2 * rho_{bite}}{W^2 * d^2} + \frac{\alpha_{bite} * I * T_c}{lc * wc * d}$$

in which the plus sign means heat is released due to Peltier effect.

The case for Sb₂Te₃ is similar:

$$Q = \frac{I^2 * rho_{sbte}}{W^2 * d^2} - \frac{\alpha_{sbte} * I * T_c}{lc * wc * d}$$

$$Q = \frac{I^2 * rho_{sbte}}{W^2 * d^2} + \frac{\alpha_{sbte} * I * T_c}{lc * wc * d}$$

(3) The contact resistance between TiW and Bi₂Te₃ and Sb₂Te₃ is not counted in the model, since it is unknown and it does not affect the optimal dimensions. The Joule heat in TiW electrode is not taken in account either for the same reason.

The thermal isolation is assumed at the boundaries.

(4) Related constants are listed below.

rho_bite	12.6e-6 Ohm*m
rho_sbte	12.6e-6 Ohm*m
$\alpha_{Bi_2Te_3}$	248e-6 V/K
$\alpha_{Sb_2Te_3}$	188e-6 V/K
l	200e-6 m
d	1e-6 m
Tc	273.15K
lc	10e-6 m
κ_{BiTe}	1.2 W/ (m*K)
κ_{SbTe}	1.2 W/ (m*K)

The simulation result for the device in Fig 2.4 is shown below in Fig 2.5.

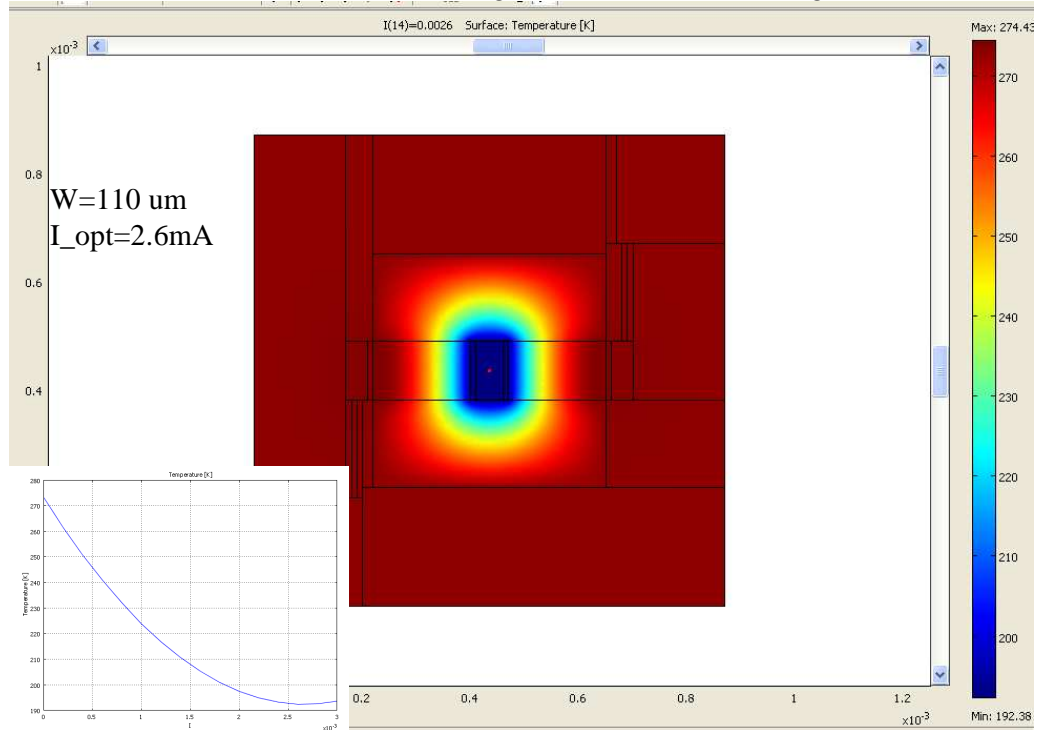


Fig 2.5 simulation result of the top view model, with the maximum temperature drop 80.77K

The temperature of the electrode at the centre of the membrane first decreases with the increasing current for the stronger heat power absorbed according to Peltier effect. If the input current is higher than 2.6mA, the temperature increases as the current goes up, because the Joule heat power is much larger than the Peltier cooling power. For the device in Fig 2.4, the best case of cooling happens at $I=2.6 \text{ mA}$, and gives a maximum temperature change $\Delta T = 273.15 - 192.38 = 80.77 \text{ K}$. The simulation result of the top view model with different thermocouple width is shown in Fig 2.6

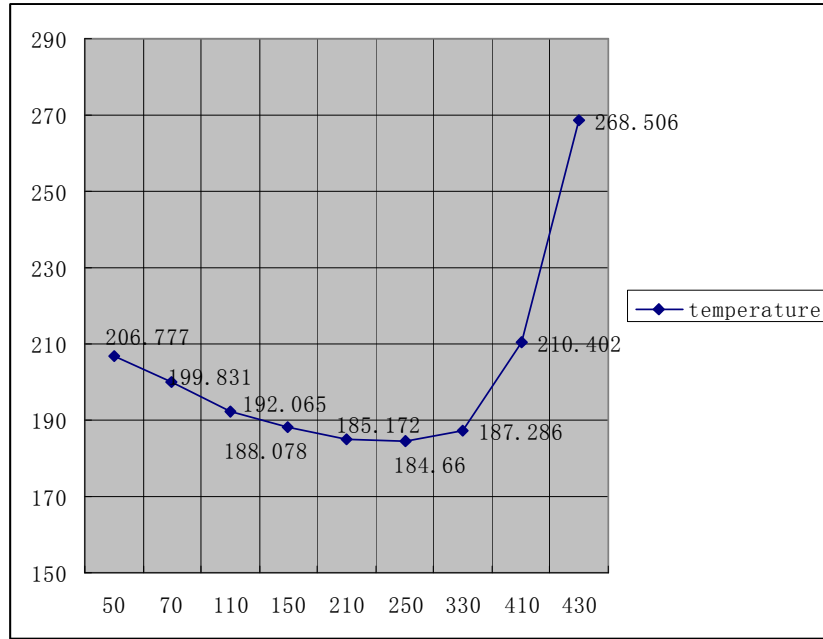


Fig 2.6 minimum temperature vs. the with of the thermocouple

The device gives the lowest temperature when the width is around half the size of the membrane ($1/2 * 430\mu\text{m}=215\mu\text{m}$).

The thermal profiles for $W=50\mu\text{m}$, $210\mu\text{m}$, $410\mu\text{m}$ and $430\mu\text{m}$ are shown in Fig. 2.7.

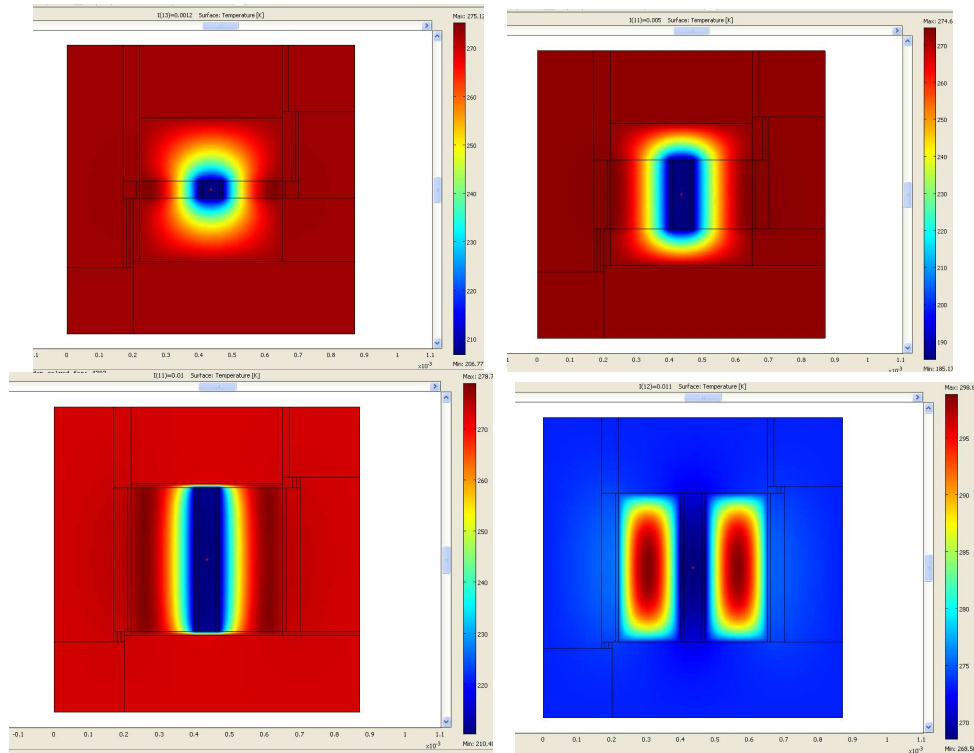


Fig 2.7 simulation result for top left: $W=50\mu\text{m}$, top right: $W=210\mu\text{m}$, bottom left: $W=410\mu\text{m}$, bottom right: $W=430\mu\text{m}$

Next, the effect of the scaling up the device is studied. The device in Fig 2.4 is taken as an example. If we increase the size of the structure in Fig 2.4 in all dimensions, except the thickness, by the same factor, for example, twice or 4times, the simulation result would not change since the heat absorbed at the cold junction is

$P = \alpha_{\text{bite}} * I * T_c$, which has nothing to do with the scaling of the size, and the Joule heat released along the thermoelectric material is

$$P = I^2 * \rho_{\text{bite}} * l_c / (w_c * d)$$

$$= (n * l_c) / (n * w_c) = \text{constant}$$

which is also a constant when we change the scale. The simulation result of the above case is in Table 2.3.

Now we must take the Joule heat of the contact resistance into account. So the new heat power generated at the contact area between the thermo electronic material and TiW at the cold end, in the centre of the membrane is expressed as:

$$Q = Q_{\text{Joule}} + Q_{\text{Peltier}} + Q_{\text{Joule,contact}}$$

$$= \frac{I^2 * \rho}{W^2 * d^2} - \frac{\alpha * I * T_c}{l_c * w_c * d} + \frac{I^2 * R_c}{d * l_c^2 * w_c^2}$$

in which R_c is the contact resistivity ($\text{ohm} * \text{m}^2$) between TiW and Bi_2Te_3 or Sb_2Te_3 . Since the resistance of the contact area is $R_c / (l_c * w_c)$, the larger contact area is the better for the cooling device.

The heat generated at the hot end contact area, at the edge of the membrane is:

$$Q = \frac{I^2 * \rho}{W^2 * d^2} + \frac{\alpha * I * T_c}{l_c * w_c * d} + \frac{I^2 * R_c}{d * l_c^2 * w_c^2}$$

The simulation result of different scales considering the contact resistivity is listed in Table 2.3.

Table 2.3: simulation results considering contact resistance

Without contact resistance				
Scale=n		Tmin=192.065		
With contact resistance				
Contact resistivity (Ohm*um^2)		Scale=1	Scale=2	Scale=4
Rc=50	I_opt	2.6mA	2.6mA	2.7mA
	T_min	192.38	192.144	192.021
Rc=500	I_opt	2.6mA	2.6mA	2.6mA
	T_min	195.213	192.852	192.262
Rc=5000	I_opt	1.8mA	2.4mA	2.6mA
	T_min	215.817	199.58	194.033

If we increase the size of the structure, the minimum temperature would decrease, so we could get a cooler junction in a larger device. This can be explained as follows.

When we scale all the lengths and widths with the factor of n, $n > 1$, $L_c = n * l_c$;

$W_c = n * w_c$; $D = d$.

Then the Peltier cooling power per volume is $P_{\text{peltier}} = \alpha_{\text{bite}} * I * T_c = \text{constant}$.

The Joule heat power per unit volume in Bi_2Te_3 / Sb_2Te_3 is

$$P = I^2 * \rho_{\text{bite/sbte}} * L_c / (W_c * D) = I^2 * \rho_{\text{bite/sbte}} * (n * l_c) / ((n * w_c) * d) = \text{constant}.$$

While the Joule heat power per unit volume due to the contact resistance is

$$P = I^2 \cdot R_c / (L_c \cdot W_c) = I^2 \cdot R / (n \cdot l_c) \cdot (n \cdot w_c) \propto n^{-2}$$

So the device with larger scale factor n gives a relatively smaller contact resistance compared to the heat pumping capacity, hence the device could cool better.

The last model we want to check is the Peltier device with a capacitor and interconnect on top, that is used in the CO₂ sensor to measure the change in capacitance and resistivity due to the presence of a condensed liquid film. The metal connects to the hot end and the cold end, and transfers a lot of heat due to its high thermal conductivity. An Al resistor with one end on the bulk silicon and the other end near to the cooling electrode is added to the model in Fig 2.4. The simulation result is shown in Fig 2.8.

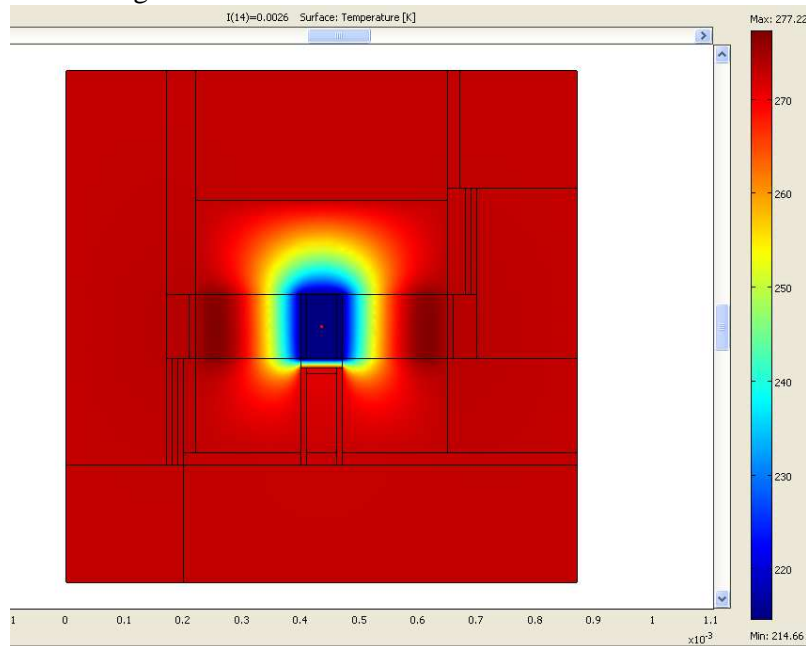


Fig 2.8 thermal profile for the top view model with an aluminium line between the hot and cold end

The minimum cooling temperature increases to 214.66K, and the maximum temperature drop is 58.49K, which is 28% less than before.

Conclusion:

2 kinds of models, which are the cross section model and the top view model, are simulated in this part to get an optimal dimension. Several heat generation effects are considered, which are the Peltier effect (both cooling and heating), the Joule heat in Bi₂Te₃ and Sb₂Te₃, and the Joule heat at the contact. Under the condition of thermal isolation, we got the maximum temperature drop of 50K (for cross section) and 103K (for top view). The difference of the result is because that they are different models, the cross section model assumes the width of every layer is infinite, and the top view model include one layer at one place and neglect the capping layer and the substrate. Both the models are not the reality. The best case for length of the square membrane is that when the edge of the membrane is just aligned to the contact between Bi₂Te₃/Sb₂Te₃ and TiW electrode at the hot end. The longer the thermoelectric material gives cooler result, so the length of Bi₂Te₃/Sb₂Te₃ should be as long as possible and

extreme case is that the length is half the membrane size. The optimal width of Bi_2Te_3 and Sb_2Te_3 is the half of the size of the membrane. For the size of the contact area between the thermoelectric material and the electrode, the larger is the better.

2.2 Device layout

The software program Cadence is used for the layout of the devices and test structures. To design a set of masks, a general idea of the flow process must be clear. We start with a wafer covered with polyimide or nitride as the substrate, and a layer of TiW is deposited on it, which is patterned into the electrodes later (Mask #1). The 1st thermoelectric material is deposited and patterned into half of the thermocouple (Mask#2), after that we cover the wafer with an intermediate layer. Then we open the intermediate layer at the place where the 2nd half of the thermocouple is (Mask #3), the 2nd thermoelectric material is deposited and isolated from the 1st material by the intermediate layer. The 2nd thermoelectric material is patterned into the 2nd half of the thermocouple (Mask #4). At this time, the Peltier junction is formed, which is capped and protected within Si_3N_4 or polymers. The next step is to open the bond pads (Mask #5), and metallization (Mask #6). At last, the backside of the wafer is opened to form a membrane (Mask #7).

There are two kinds of masks, the Light Field mask (LF), and the Dark Field mask (DF). For the Light Field mask, the figures in the layout are transferred to the metal figures on the mask, and since we are using positive photoresist, they are finally transferred to the remaining material on the wafer. So the figures on the wafer are exactly the same as them in the layout. While for the Dark Field mask, the figures in the layout are transferred into the openings on the mask and the openings on the wafer. The LF masks are usually used for patterning the materials and the DF masks are used to open the contacts. So the Mask #1, #2, #4, and #6 are the LF masks and the others are the DF masks.

The layers and the masks are listed in Table 2.4.

Table 2.4: layers and masks

Mask Number	LF or DF	Layer in layout	Mask name	The function of the mask
1	LF	MESA	TiW	Patterning TiW electrodes
2	LF	PS	BiTe	Patterning the 1 st material
3	DF	CO	CO	Opening contact on intermediate layer
4	LF	IN	SbTe	Patterning the 2 nd material
5	DF	CB	CB	Opening contact holes
6	LF	XTR1	IN	Patterning metal leads
7	DF	XTR3	MESA	Opening back side

The Peltier cooling devices are designed in several sizes. The basic one is as showed in Fig 2.4. The membrane size is 425um*430um, and the corner of the membrane is made round for better back etching profile. The edge of the membrane should be aligned to the contact area at the hot end of the thermocouple, so we design the edge of the membrane as close to the hot end as possible, leaving 25um space in case the non-ideal anisotropic RIE etching. The length of the thermocouple is 250um, and the width is half the membrane size, 210um. The distance of the two materials is 55um.

The contact area is $40\mu\text{m} \times 210\mu\text{m}$ for lower contact resistance, and the bond pads are $400\mu\text{m} \times 400\mu\text{m}$ for easier contact on the probe station. The layout of this device is shown in Fig 2.9.

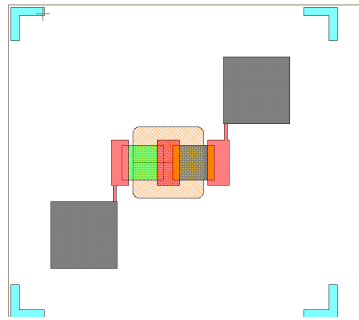


Fig 2.9 layout of the cooling device, size: small

The other two types of the devices are twice and 4 times of all the dimensions of the device above. In all designs the bondpad size and the 'safe distance' between edge of the membrane and the hot junction is equal, as shown in Fig 2.10. We expect that the device with larger size would show better cooling as simulated.

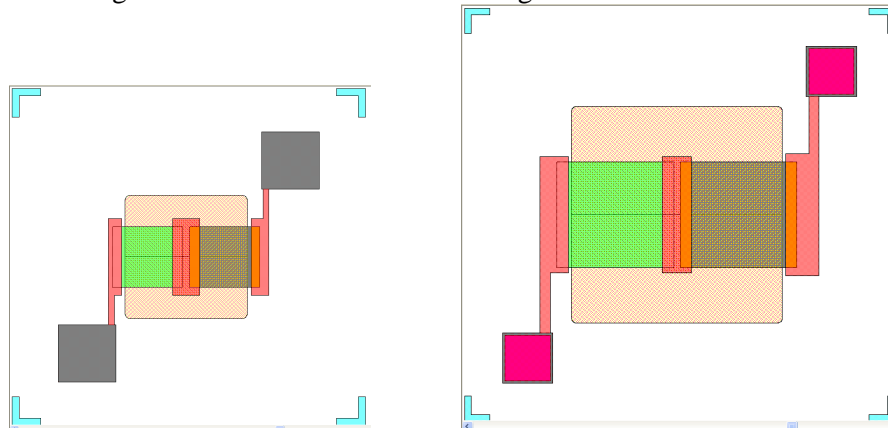


Fig 2.10 layout of the cooling device, left: size middle, right: size large

A six-end device is added to the design. The device is based on the device in Fig 2.10. Three Peltier junctions are arranged in parallel to investigate the effect of thermocouples connected in parallel on the cooling performance. The device is shown in Fig 2.11

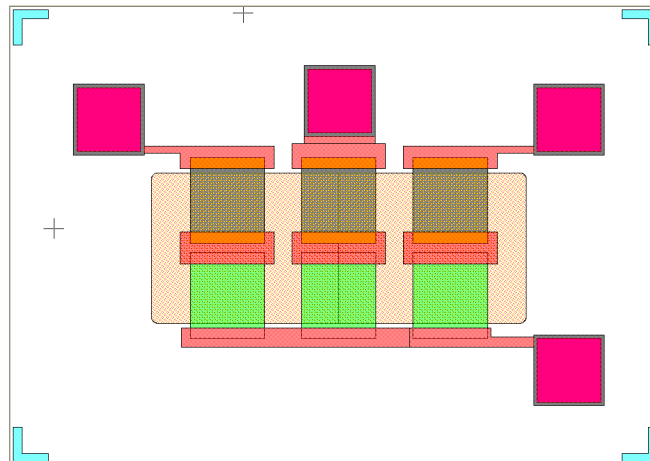


Fig 2.11 layout of the parallel thermocouples

At last a simple structure that mimics a CO₂ sensor is added (see Fig 2.12) to investigate the additional heat loss through the aluminium wires of capacitor. This device has the dimensions of the largest structure, since this structure is expected to offer the largest temperature drop.

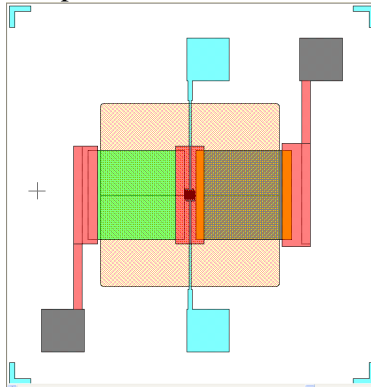


Fig 2.12 layout of the structure with additional Al lines to mimic a CO₂ sensor

In conclusion, seven layers in the layout are needed for the seven masks. Four cooling devices and a CO₂ sensor are designed on this set of masks.

2.3 Test structures and alignment markers

To control the process flow and to measure the material characters, we added a set of test structures.

(1) Process control

The steps in the processing, for example, the exposure time and the film step height can be controlled by the structures in Fig 2.13 and 2.14.

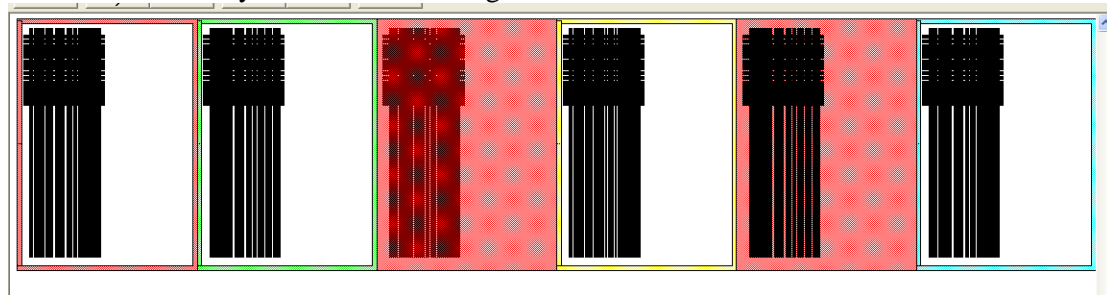


Fig 2.13 layout for the structures to test the exposure

In the case of over exposure, the narrow lines in Fig 2.14 will disappear. If the exposure time is too short, the dense net in the structure would become one huge square.

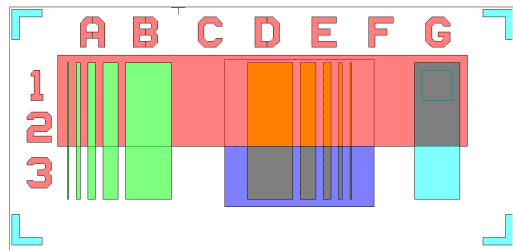


Fig 2.15 layout to measure the step height

We could measure the thickness of the TiW , Bi_2Te_3 , Sb_2Te_3 , intermediate layer and the top metal using the structure in Fig 2.15.

The next test structure to add in the design is the structure for SEM. We designed a long structure (several centimetres), which has the same cross section as the devices in Fig 2.11, (see figure 2.16). After the process is finished, we could break the wafer and check the cross section easily using this structure.

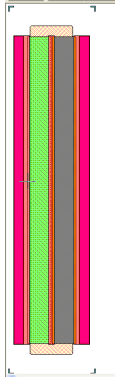


Fig 2.16 layout for the long structure for SEM

(2)Measure the characters

For thermoelectric materials, the most important character is the Seebeck coefficient. To measure the Seebeck coefficient α , we could heat one side of the thermoelectric material, and measure the temperature difference between the two ends, ΔT , and the output voltage of the two ends, ΔV . Then $\alpha = \frac{\Delta V}{\Delta T}$. To get a more precise result, a differential structure is taken, see Fig 2.17.

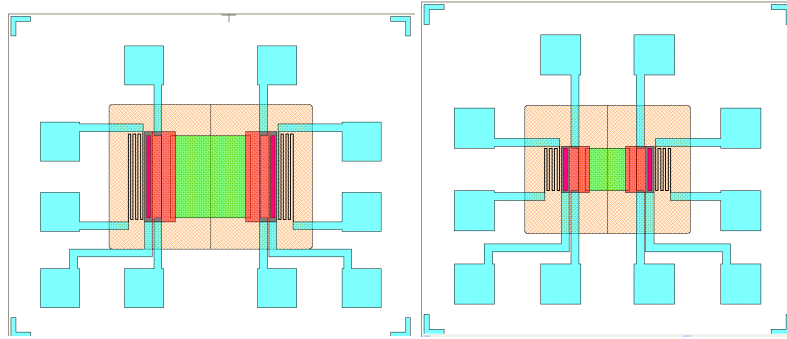


Fig 2.17 layout of the structure to measure the Seebeck coefficient

Another important parameter is the resistance, including contact resistivity and the sheet resistance. The structures in the bottom row of fig 2.18 are designed to measure the sheet resistance of TiW, Bi_2Te_3 , Sb_2Te_3 and Al using the Four Point Method. The contact resistivity between TiW and Bi_2Te_3 , Sb_2Te_3 , and Al can be measured with the devices in the upper two rows.

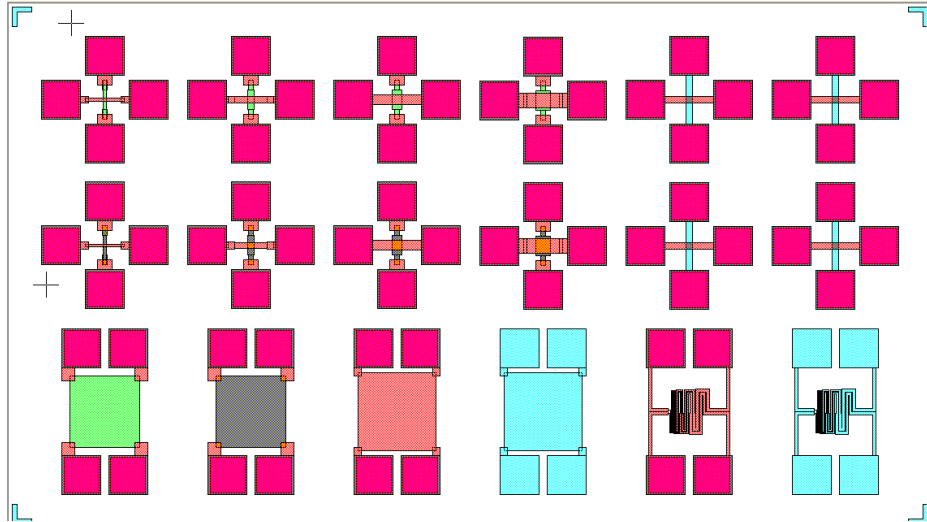


Fig 2.18 layout of the resistance test structures

Two structures to measure the temperature drop at the cold junction are shown in Fig 2.19 and Fig 2.20. Four strips of thermal materials form one thermal junction. If we apply current through the top and bottom strips, heat will be absorbed or generated at the central electrode due to the Peltier effect, and the output voltage due to the Seebeck effect could be measured at the left and right strips. This is a simple structure, but it is very useful in the measurement. While for the structure in Fig 2.19, we could not only apply current through the thermocouple to see the change in temperature, but also heat up one side of the thermocouple to measure the Seebeck coefficient.

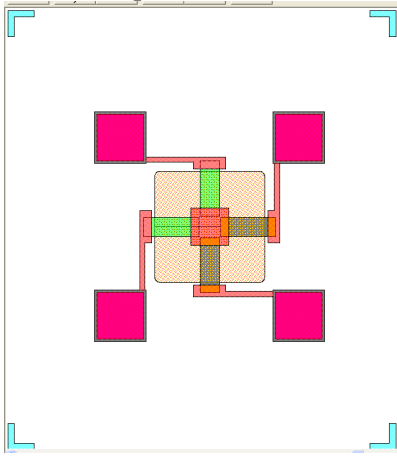


Fig 2.19 layout of the cross device

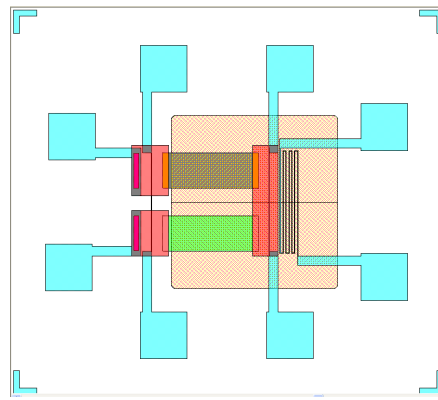


Fig 2.20 layout to measure the combined Seebeck coefficient

(3) The alignment markers.

We use TiW as the basic alignment markers, since it is the first patterned layer. Also, it is expected that TiW structures will remain visible during the processing, this is in contrary to the thermoelectric materials which might show poor adhesion and a large lateral etch. The markers for the other layers are divided in two types, one for LF masks (Fig 2.21, left), and the other one for DF masks (Fig2.21, right). The marker numbers for the masks are listed in Table 2.5, and the second mask in the process aligned to the markers on the first mask.

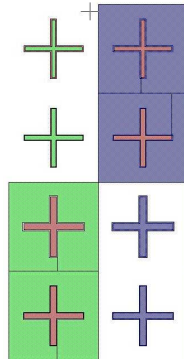


Fig 2.21 alignment markers for left: the LF mask, and right: the DF mask

Table 2.5: alignment markers for different masks

#	First mask	Second mask
1	TiW	BiTe (LF)
2	TiW	CO (DF)
3	TiW	SbTe (LF)
4	BiTe	SbTe (LF)
5	TiW	CB(DF)
6	TiW	MESA (DF)
7	TiW	IN (LF)

The markers array is shown in Fig 2.22.

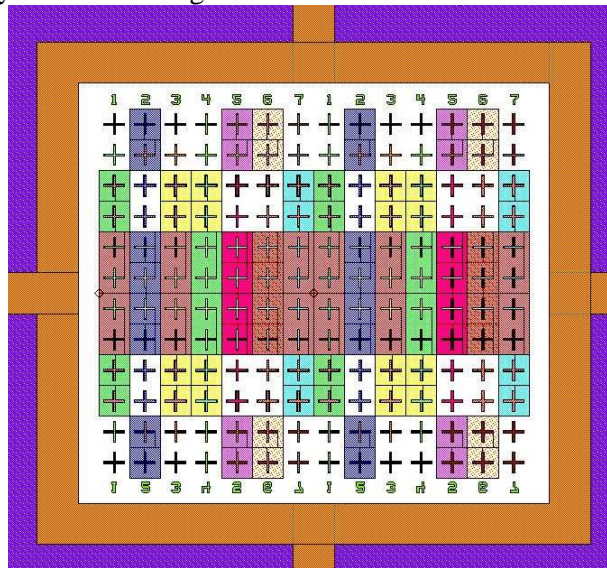


Fig 2.22 layout of the alignment marker array

2.4 Conclusion

The design of the Peltier cooling device starts with the thermal simulation with the software COMSOL, which gives not only the general idea of the thermal profile, but also the optimal dimensions of the device. According to the result, the layout is

designed using the software Cadence, including four cooling devices and one device to mimic the CO₂ sensor. After that, the test structures to control the process, for example, the exposure time and the step height, and to measure the Seebeck coefficient and the resistance are added in the design. At last, the markers are added.

Chapter 3 Patterning Bi₂Te₃ and Sb₂Te₃

The patterning of Bi₂Te₃ and Sb₂Te₃ is one of the main challenges of the thesis project, and it is discussed in this part. There are three potential methods; wet etching, dry etching and patterning with a shadow mask. Wet etching is convenient and fast, but Bi₂Te₃ and Sb₂Te₃ are so reactive that the lateral undercut is rather large [12]. Dry etching gives precise pattern, but the re-deposition at the side walls hampers subsequent layer coverage. The use of a shadow mask, in which method the material is patterned at the same time as it is deposited, might be a good alternative. However, the alignment is not as precise as lithography. The three patterning methods for Bi₂Te₃ and Sb₂Te₃ are listed in Table 3.1 with the advantages and disadvantages. Which one of the three is the best patterning method is an important question for this project.

Table 3.1: potential method for patterning Bi₂Te₃ and Sb₂Te₃

Etching method	Advantages	Disadvantages
Shadow mask	Smooth edge Patterned during deposition	Alignment problem
Dry etching	Precise dimension	Redeposition sidewalls
Wet etching	Easy method High etching rate Smooth edge	Large lateral etch

The shadow mask is a mask, which in this case is a 6-inch wafer, with patterned holes we put on the wafer during the deposition of the material, and the material is only deposited at the position of the holes, resulting in patterned material right after deposition. The structures are very smooth at the edge. However, it is difficult to align the shadow mask to the wafer. Also, the Si deep etching for the shadow mask causes sloping edge of the holes, making the pattern after deposition imprecise. Hence, the shadow mask method is not employed for processing the Peltier coolers. The shadow mask patterning method is discussed in Appendix A in details.

3.1 Dry etching method

Dry etch is a popular etching method with high anisotropy and high resolution, which makes small feature sizes feasible. Ion beam etching is one way to dry etch at low temperatures. It is based on the physical impact of high energy ions. Bi₂Te₃ and Sb₂Te₃ are etched in Argon ion beam. One concern of dry etching is the re-deposition of the etched material. During the etching, the atoms of Bi, Te and Sb receive a lot of kinetic energy and leave the surface of the wafer to deposit again along the edge of the photoresist. After stripping the resist, the redeposition side walls fall down on top of the patterned feature, and they are a big problem for capping. As we discussed before, Bi₂Te₃ and Sb₂Te₃ are already hard to cap because of the temperature limit and bad adhesion. The side walls give peaks at the edge of the feature, which causes

cracks in the capping layer, leading to air inclusions underneath the capping layer. The cracks makes the capped material vulnerable to be attacked by other etchants, and the air inclusions give rise to the possibility that Bi_2Te_3 and Sb_2Te_3 evaporate at a relatively high temperature causing the inclusions to rupture. The side wall problem had to be solved before we would decide to employ dry etching as the patterning method.

3.1.1 Reflow of the photoresist

One approach to diminish the sidewalls is to reflow the photoresist at 110 degreeC before dry etching. After reflow, the photoresist becomes thinner at the edge and thicker at the centre, and the edge of the photoresist is no longer vertical, as shown in Fig 3.1. The redeposition along the sloping edge of the photoresist could be removed during the Ion Beam Etching process when the atoms hit vertically on the side walls.

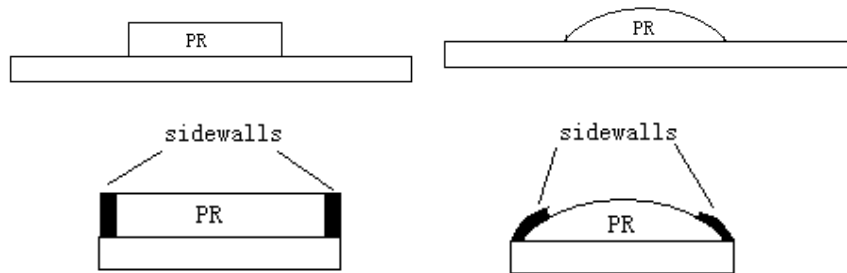


Fig 3.1 shape of the photoresist and the demonstration of the redeposition sidewalls, left: without reflow, right: after reflow

An experiment was designed to check this idea. The flow chart is in Appendix B-1.

After the reflow of the photoresist, the shape of the photoresist was checked using the step height measurement. The result is shown in Fig 3.2. The edge of the photoresist is no longer vertical, but sloping, and the photoresist grows from 0 to 1.3 μm step in 6 μm lateral displacement. It is not quite convincing if the photoresist has already reflowed or not, since the needle of the stepheight measurement station has also a sloping edge, which could also give sloping result even if the measured step is vertical, as in Fig 3.3. Hence, it is not accurate to check the reflow using the stepheight measurement, and we had to wait after the ion beam etching to directly check the sidewalls.

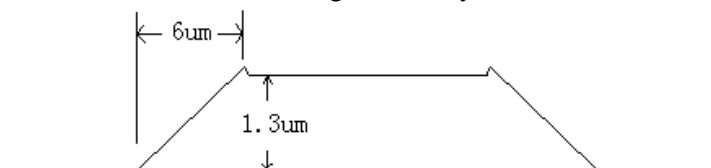


Fig 3.2 step height profile of the photoresist after reflow

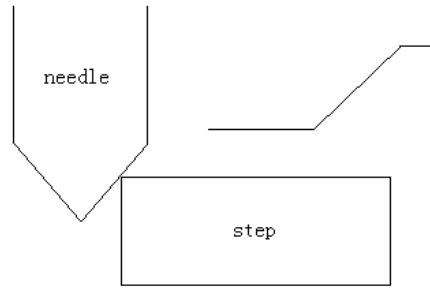


Fig 3.3 demonstration of the sloping edge of the needle, which results in sloping step height profile even if the step is sharp

The ion beam etching takes place in the Ion Beam Etser, and the etchant to etch Bi_2Te_3 and Sb_2Te_3 is Argon. The etch time for Bi_2Te_3 is 12min, and for Sb_2Te_3 is 10min. The process is controlled by scanning the exhaust with a spectrometer. The signals of the etched atoms are detected, for example, Bi, Te, and Sb; and we define the endtime when the etched signal of Bi_2Te_3 and Sb_2Te_3 decreases 2 decades as the end point. The signal of Ti and W is also detected. A typical record of the atom signal is shown in Fig3.4.

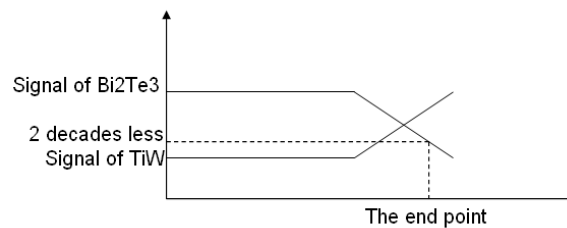


Fig 3.4 the signal of the atoms during the ion beam etching process, with a significant endpoint

The Scanning Electronic Microscope (SEM) is a tool to view features with a nm resolution. The SEM result for Bi_2Te_3 is shown in Fig 3.5, and for Sb_2Te_3 is in Fig 3.6.

In figure 3.5, we could observe obvious protuberance band on the edge of Bi_2Te_3 structure, especially at the corner. The band folds and forms hollow hills at the corner of the patterned structure, and if we cap it now, the vacancy under the hill and the evaporation of Te may cause rupture under the high temperature in the following process steps.

In figure 3.6, there is no obvious band on the edge of Sb_2Te_3 structures, but the peaks at the corner are difficult to envelop. For Sb_2Te_3 , the width of redeposition band is 1.1 μm , and the thickness of the photoresist we employed is 1.3 μm , which suggests evidence that the redeposition band is related to the photoresist.

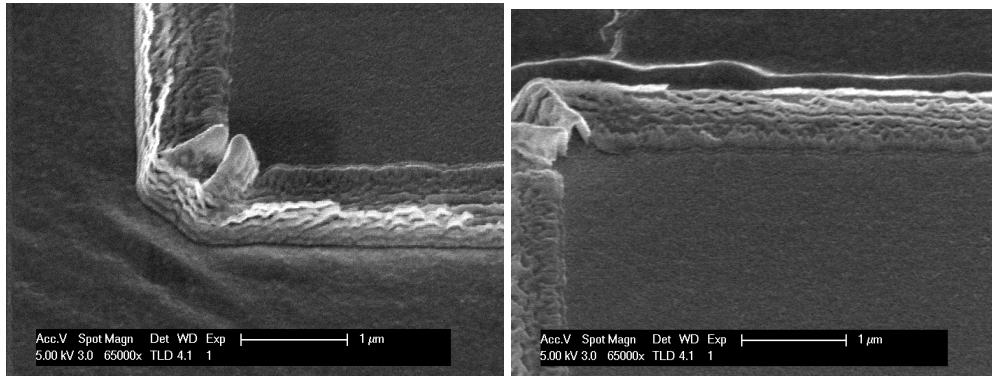


Fig 3.5 SEM photos of Bi_2Te_3 after ion beam etching, with folded redeposition band at the corner

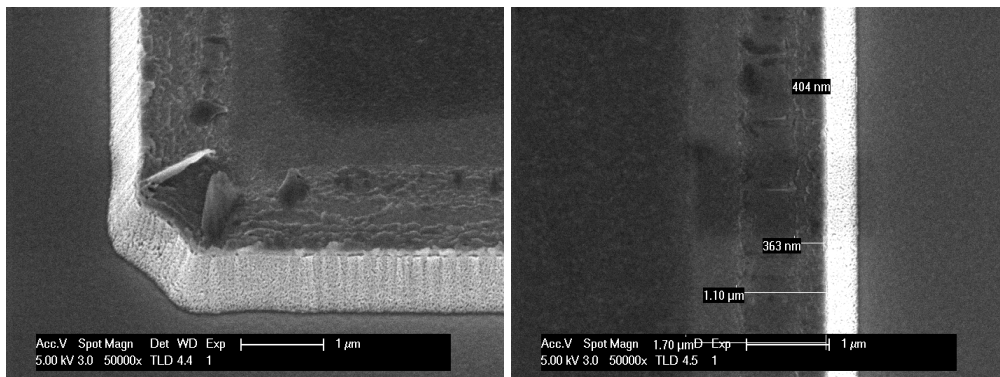


Fig 3.6 SEM photos for patterned Sb_2Te_3 , with peaks at the corner due to the redeposition

Simply reflowing the photoresist does not diminish the redeposition along the sidewalls during the ion beam etching. The etched materials redeposit along the thick photoresist even though the photoresist edge is sloping. What we need to do is to make the photoresist very thin to obtain smaller redeposition sidewalls. However, the thin photoresist is not strong enough to mask the patterned layer in the process. The reflowing of the photoresist is not feasible. Other approaches must be investigated.

3.1.2 Tungsten as a hard mask

An idea to avoid redeposition is to employ a thinner etching mask for less redeposition. Since the ion beam etching is of high selectivity of Bi_2Te_3 and Sb_2Te_3 to some other materials, such as TiW, W and Si_3N_4 , we may employ one patterned thin layer of these materials as the hard mask in the etching, and remove the hard mask layer afterwards. In this part, we employ W, but not TiW as the hard mask since Ti tends to diffuse into Bi_2Te_3 and Sb_2Te_3 .

The etch rate of W in Argon ion beam etching is only 0.1~0.01 times that of Bi_2Te_3 and Sb_2Te_3 . In this case, 100nm of W as the hard mask is enough for masking 1μm Bi_2Te_3 and Sb_2Te_3 . We take 150nm layer just in case of over etch. After etching, the 150nm mask will be left only 50nm, and the redeposition band will be less than 50nm wide, which is acceptable.

The initial thickness of the W mask is 150nm, and TiW layer is 200nm. The ion beam etch and the over etch consume 100-120nm W mask (10-12min (from Part 3.1) * 10nm/min), leaving the tungsten mask thickness only 30nm. The TiW layer is 6 times thicker than the remaining W layer after the ion beam etch. Hence the etching of the TiW when removing the W mask in the final step is minimized (See fig 3.7)

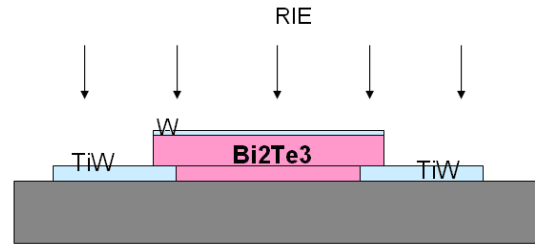


Fig 3.7 demonstration of removing W hard mask, which also etches the exposed TiW bond pads

The demonstration and the flow chart for ion beam etching Bi_2Te_3 / Sb_2Te_3 with W hard mask are in Appendix B-2.

The W mask is patterned and removed by one Reactive Ion Etching (RIE), which employs low temperature reactive plasma to etch the wafer via chemical reaction and physical impact. One advantage to etch the W mask using RIE is that TiW is etched slower than W. Hence, the TiW electrode is only slightly attacked by the RIE etch. The etchant also etches Si_3N_4 . Therefore, we must find a substitute method for the wafers with Si_3N_4 substrate.

After removing the W mask, the structures are checked under the microscope, shown in Fig 3.8. Bi_2Te_3 is coloured black instead of the usual silver-like white. The Sb_2Te_3 structures are very nice patterned, but we could see black spots at the corner of the structures, which is quite like the redeposition peaks.

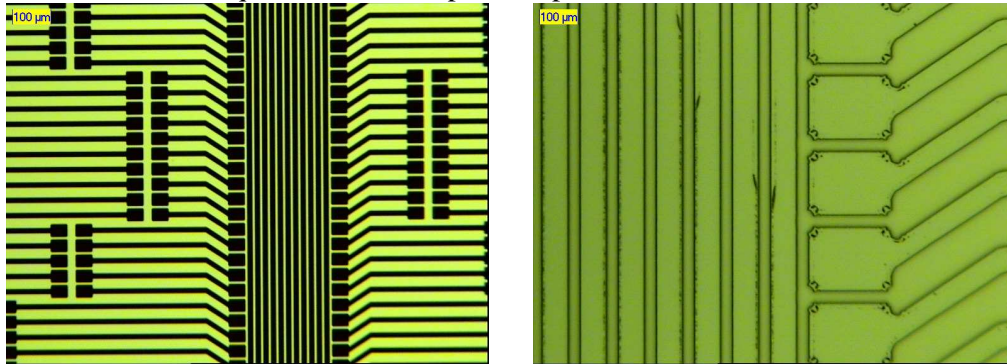


Fig 3.8 structures after removing W mask under the micro scope, left: for Bi_2Te_3 , right: for Sb_2Te_3

The surface of the patterned layers is checked with a SEM microscope. The result for Bi_2Te_3 is shown in Fig 3.9, and for Sb_2Te_3 in Fig 3.10.

For Bi_2Te_3 in figure 3.9, the cause of the black appearance is that the surface is not flat anymore, but crowded with little 'balls'. Positively there is no sign of redeposition at all. The possible reason of the rough surface may be, 1), the etching time

of Bi_2Te_3 is too long (13min in this case), and the W mask is etched through, causing the surface of Bi_2Te_3 under W mask attacked as well; 2), the etchant to remove the W mask in RIE also etches Bi_2Te_3 ; 3), W tends to diffuse into Bi_2Te_3 , so after W is completely removed, vacancies formed in Bi_2Te_3 that was formerly occupied by W. The first point could be investigated by depositing a thicker W mask. The second and the third hypotheses are both material properties and could only be investigated by changing the etchant and the masking material.

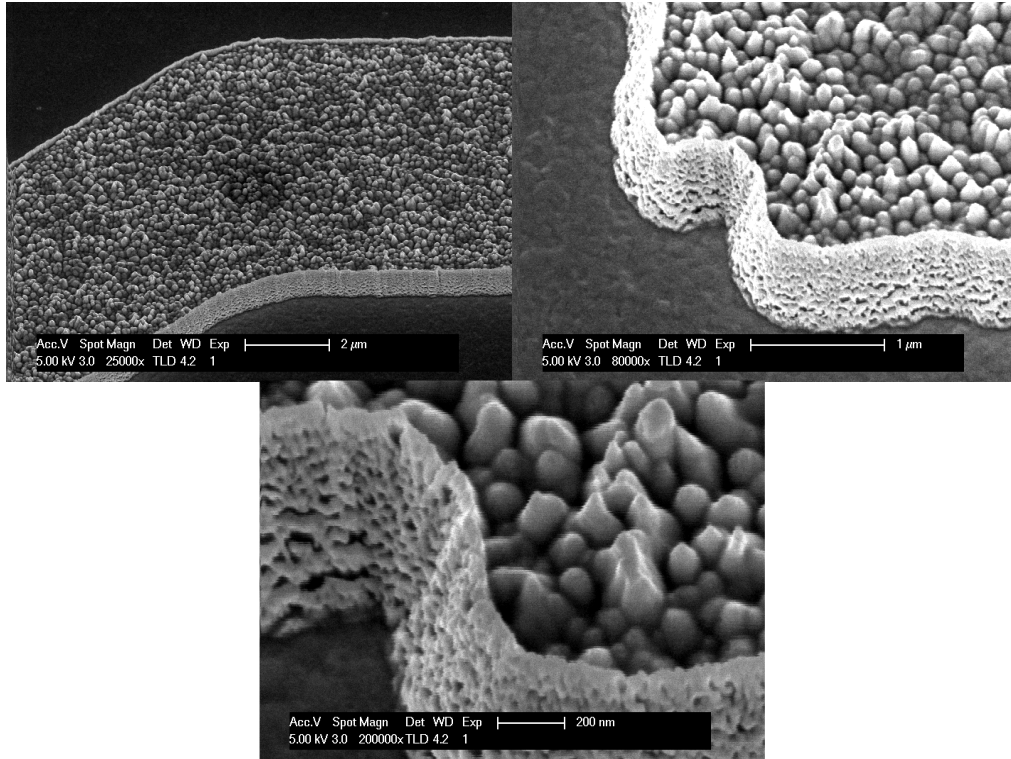


Fig 3.9 SEM photos for Bi_2Te_3 after removing the W mask, the surface of which is covered with small ‘balls’

For Sb_2Te_3 in figure 3.10, patterns of redeposition come up at the corner of the structure, but this time covered with a dielectric layer, which attracts a lot of electrons and is very bright in the photo. No dielectric material is introduced in the process except the photoresist, so naturally we strip the photoresist repeated plasma, but the dielectric layer is not removed, indicating that this irremovable dielectric layer is neither photoresist nor other polymer.

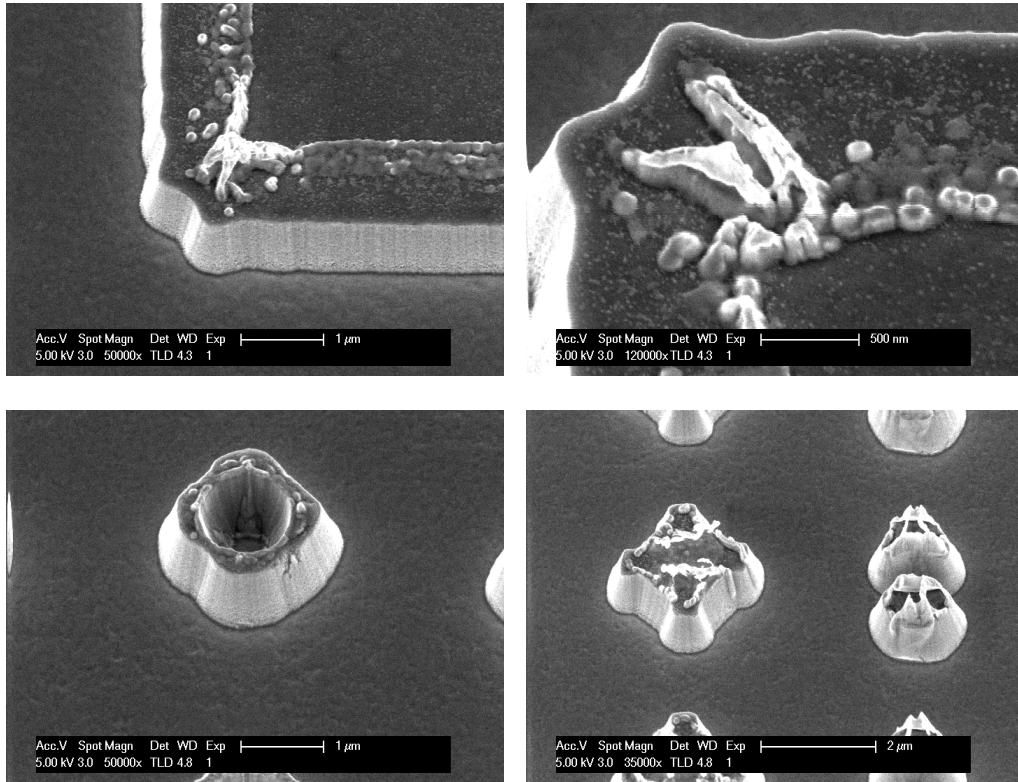


Fig 3.10 SEM photos for Sb_2Te_3 after removing the W mask, with irremovable dielectric residues at the corner

The composition of the dielectric layer is measured by SEM-EPMA (scanning electron microscopy / electron probe X-ray microanalysis). The SEM-EPMA is an advanced SEM machine with additional function to detect the elements in the selected surface. The result is shown in Fig 3.11. The dielectric layer mainly consists of W and O. The defects are tungsten oxide on top of tungsten.

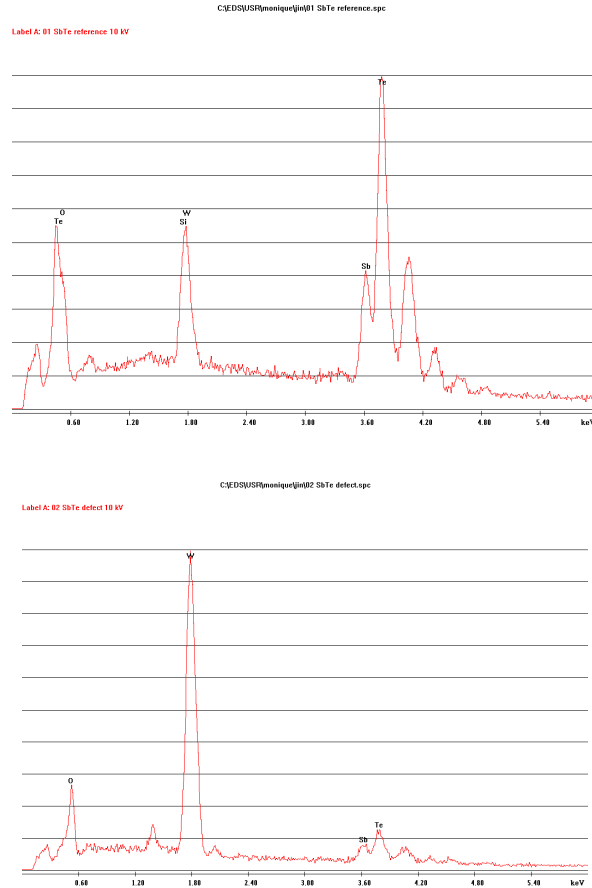
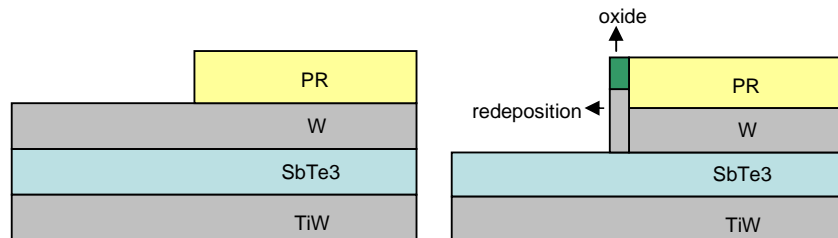


Fig3.11. Top: Reference of Sb_2Te_3 surface; Bottom: Result of the dielectric layer.

Tungsten oxide does not dissolve in water or acid and it is very hard to remove with dry method, except if we deoxidize it with H_2 . The reason why tungsten oxide comes up is demonstrated in Fig 3.12. When we pattern the W mask using RIE etching, the W redeposits along the photoresist and is oxidized by the descum O_2 plasma and the O_2 plasma to strip the resist. After the photoresist is removed, the tungsten oxide collapses to the surface of the W mask and protect the W underneath it from being etched. To avoid the formation of tungsten oxide, we should replace all the steps employing O_2 plasma. Wet etching W could be a substitute method with no redeposition and oxidation at all.



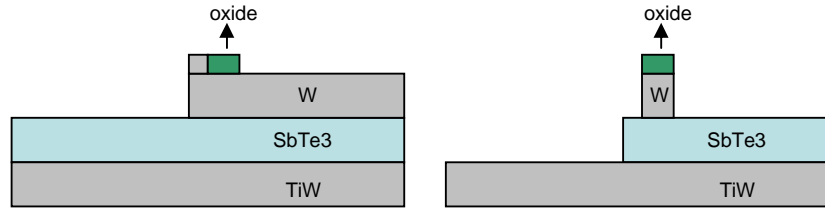


Fig 3.12 demonstration of the tungsten oxide formation

Dry etching with W as the hard mask is not as successful as we expected. The surface of Bi_2Te_3 is damaged after patterning, and irremovable tungsten oxide comes up on the surface of Sb_2Te_3 . Fortunately some ideas are brought up to improve the method. We will try thicker W mask for Bi_2Te_3 , and avoid O_2 plasma for Sb_2Te_3 in the following experiment.

3.1.3 Dry etching with improved W mask

To improve the W mask, the thickness is increased to 200nm to see if it is enough to protect the thermoelectric material layer, and the O_2 plasma is replaced by acetone strip. The new process flow is in Appendix B-3.

When we process the wafer with Sb_2Te_3 , all the structures come off in the acetone bath, leaving a smooth and shiny surface. We opened a window at the edge of the wafer through the metal layer to the nitride, and measured that the thickness of the remaining metal layer is 60nm, according to which the metal layer could only be TiW, indicating that the Sb_2Te_3 layer comes off from the TiW.

The adhesion of Sb_2Te_3 to TiW electrode is poor. A possible reason is that there is a layer of oxide on top of TiW, and Sb_2Te_3 and Bi_2Te_3 show poor adhesion to oxides. The oxide layer is caused by the O_2 plasma to clean the wafer, or the native oxidation. One solution to improve the adhesion is to sputter etch the wafer for a short while, just to remove several nanometres of oxide, and transfer into the deposition chamber immediately.

For Bi_2Te_3 wafers, after the RIE patterning the tungsten mask, Bi_2Te_3 layer turns black again, which means the black rough surface of Bi_2Te_3 is caused by the the etchant of TiW in the RIE etching machine, or the holes resulting from removing of the W atoms, which have diffused into Bi_2Te_3 layer. Increasing the tungsten mask thickness did not prevent Bi_2Te_3 from turning into black. One solution is to replace the RIE method by the wet etching method for removing W mask.

The wet etching experiment for W mask is a conducted as a separate experiment with small pieces, which is detailed in Appendix C.

Unfortunately, when we put the wafer with Bi_2Te_3 and W mask in the wet etchant bath after Ion Beam Etching, Bi_2Te_3 and W mask starts to peel off at the moment we put the wafer in the etchant. Wet etching to strip the tungsten mask does not work since no Bi_2Te_3 stays on the wafer after the etching.

To sum up, W mask for dry etching is not feasible. For Bi_2Te_3 , dry etching of the tungsten mask by RIE attacked Bi_2Te_3 , and wet etching of the W mask caused Bi_2Te_3 peeling off. W mask for Sb_2Te_3 caused the irremovable tungsten oxide and that Sb_2Te_3 easily comes off. We must try another hard mask other than tungsten for Ion Beam Etching unless we could successfully handle the adhesion problem of Bi_2Te_3 and Sb_2Te_3 .

3.1.4 Dry etching with Si_3N_4 as the hard mask

Si_3N_4 hard mask is similar to the W mask. The advantage of using Si_3N_4 as a hard mask in the Ion Beam Etching process is that it is not necessary to strip the Si_3N_4 layer at the last step, since Si_3N_4 is dielectric material with no danger of short circuit. The Si_3N_4 hard mask could also be patterned by RIE method with no lateral undercut. 100nm Si_3N_4 is enough to mask 1um Bi_2Te_3 and Sb_2Te_3 , and after 10min Ion Beam Etching, the 100nm Si_3N_4 would be almost gone, which will eliminate the negative effect to the cooling devices of Si_3N_4 due to its high thermal conductivity.

We process Bi_2Te_3 and Sb_2Te_3 on the same wafer one after another with a intermediate layer. The flow chart for dry etching with silicon nitride hard mask is in Appendix B-4

A sputter etch step is added just before the deposition of Bi_2Te_3 and Sb_2Te_3 , in order to get rid of thin oxide layer on top of TiW and to improve the adhesion.

The patterning goes well for the 1st material, Bi_2Te_3 , but after we deposit the 2nd material, Sb_2Te_3 , the deposited Sb_2Te_3 layer cracks and peels off.

Dry etching method for Bi_2Te_3 / Sb_2Te_3 with Si_3N_4 as the hard mask should be a feasible approach as long as we could get better adhesion of the material. This could be investigated in the future.

In conclusion, dry etching for Bi_2Te_3 and Sb_2Te_3 by Ion Beam Etching faces many problems. We tried to solve the redeposition problem, but more problems, such as the irremovable oxide, etchant that also attacks Bi_2Te_3 , and bad adhesion and capping, come up. The dry etching method for Bi_2Te_3 and Sb_2Te_3 is not ready for our process right now.

3.2 Wet etching method

Bi_2Te_3 and Sb_2Te_3 are reactive materials, which tend to react with many etchants. In the literature, several etchants are used, shown in Table 3.2. In table 3.2, the main problems in wet etching are the peeling off of Bi_2Te_3 and Sb_2Te_3 in the etchants and the large lateral undercut, which is over 5 times the vertical thickness. The concentration of the etchant affects the etching rate, as shown in the first figure in Table 3.2. Higher concentration causes cracks on the film since the etching rate is too fast, and lower concentration results in peeling of the film for the long etching time. The second figure in Table 3.2 shows the relationship between the selectivity and the

component ratio. The lower the HCl/HNO₃ ratio is, the higher the ration of the etch rate of Bi₂Te₃ to Sb₂Te₃ is. A set of experiments is designed and processed to check the etch rate of the etchants in Table 3.2.

The flow chart for the wet etching is described in Appendix B-5

The result of the wet etching in different etchants is shown in Table 3.3. We focus on the lateral etch, the etch rate and the cracks or peeling.

Table 3.2 possible wet etchants from literatures for Bi_2Te_3 and Sb_2Te_3

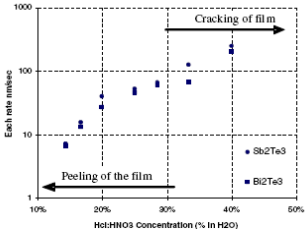
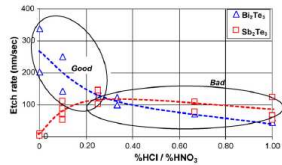
	Etchant	Composition	Target	Etchrate ($\mu\text{m}/\text{min}$)	Problems	Literature
1	Al Etch A	$\text{H}_3\text{PO}_4:\text{HNO}_3:\text{CH}_3\text{COOH}:\text{H}_2\text{O}$ =16:1:1:2	Bi_2Te_3 Sb_2Te_3	0.06 0.09	1, small spots left 2, cracks or peels 	[7]
2	Diluted Aqua Regia	$\text{HCl}:\text{HNO}_3:\text{H}_2\text{O}=3:1:2$	Bi_2Te_3 Sb_2Te_3	0.5 non	1, horizontal undercut > 5 times thickness because of grid boundaries 2, carbon based residues	[12]
3	$\text{HCl}-\text{HNO}_3$	$\text{HCl}:\text{HNO}_3:\text{H}_2\text{O}=3:5:13$	Bi_2Te_3 Sb_2Te_3	6 6	1, cracks occur (high concentration) 2, peelings occur (low concentration)	[14]
4	HNO_3	HNO_3 30% diluted in water	Bi_2Te_3 Sb_2Te_3	15 0.3	1, Selectivity is related to HCl/HNO_3 	[14]
5	$\text{H}_2\text{O}_2-\text{HCl}$	$\text{HCl}:\text{H}_2\text{O}_2:\text{H}_2\text{O}=1:1:2$	Bi_2Te_3	0.7		[6]

Table 3.3: etching result with wet etchants

Etchant	#	Composition	Target	Etch time	lateral etch	step	Problems
Al Etch A	1	H ₃ PO ₄ : HNO ₃ : CH ₃ COOH: H ₂ O = 16:1:1:2	Bi ₂ Te ₃ Sb ₂ Te ₃	15' 34'		0	1, Sb ₂ Te ₃ spots left 2, Bi ₂ Te ₃ not etched
Diluted Aqua Regia	2	HCl: HNO ₃ : H ₂ O =3:1:2 150+50+100ml=300ml	Bi ₂ Te ₃ Sb ₂ Te ₃ TiW	43" 1'10" 1'	5um 3 0	2nm	1, BiTe lateral etch 2, SbTe peel off heavily 3, TiW not etched
	3	HCl: HNO ₃ : H ₂ O =3:1:3 +50ml H ₂ O	Bi ₂ Te ₃ Sb ₂ Te ₃ TiW	45" 1'10" 1'10"	7 4.77 0		1, BiTe lateral etch 2, SbTe peel off
	4	HCl: HNO ₃ : H ₂ O =3:1:4 +50ml H ₂ O	Bi ₂ Te ₃ Sb ₂ Te ₃ TiW	55" 1' 1'10"	8.5 5 0		
	5	HCl: HNO ₃ : H ₂ O =3:1:5 150+50+250ml=450ml New solution	Bi ₂ Te ₃ Sb ₂ Te ₃ TiW	30" 33" 1'	9.5 5 0	928nm	
	6	HCl: HNO ₃ : H ₂ O =3:1:6 +50ml H ₂ O	Bi ₂ Te ₃ Sb ₂ Te ₃ TiW	1' 30" 1'	10 5 0		
	7	HCl: HNO ₃ : H ₂ O =3:1:7 +50ml H ₂ O	Bi ₂ Te ₃ Sb ₂ Te ₃ TiW	1'25" 55" 1'	18 6 0		1, only half of Bi ₂ Te ₃ layer is etched. The other half is not attacked at all 2, only half of SbTe ₃ layer is etched 3, etch rate too slow
	8	HCl: HNO ₃ : H ₂ O =3:1:8 +50ml H ₂ O =600ml	Bi ₂ Te ₃ Sb ₂ Te ₃ TiW	2'05" 2' 1'22"	16 5 0	Peel off	
diluted HNO ₃	9	HNO ₃ : H ₂ O =1:1	Bi ₂ Te ₃	5"	4.5um		1, HNO ₃ is a nice etchant for Sb ₂ Te ₃ .

		100+100=200ml	Sb ₂ Te ₃	6" 3'28" 5'30" 6'dip dip	5.5 8 7 4 4.5um	peel off	<p>The higher the concentration is, the shorter the etch time. A resistive white layer forms at beginning, it is necessary to dip in water every several seconds. The color change: black-white-green. Small structures are accessible</p> <p>2, It is not a perfect etchant for Bi₂Te₃. For high concentration, the etching is too fast, causing in bubbles, and finishes in seconds. For low concentration, Bi₂Te₃ peels off</p>
	10	HNO ₃ : H ₂ O =1:2 +100ml H ₂ O	Bi ₂ Te ₃ Sb ₂ Te ₃ TiW	30" 9' dip 7' 5'	8 5 2	bondpad off	
	11	HNO ₃ : H ₂ O =1:3 +100ml H ₂ O	Bi ₂ Te ₃ Sb ₂ Te ₃ TiW	3'30" 10' 5'30"	5 2	peel off half-etched	
	12	HNO ₃ : H ₂ O =1:4 +100ml H ₂ O	Bi ₂ Te ₃ Sb ₂ Te ₃ TiW	6'30" 6'	6	peeloff	
H ₂ O ₂ -HCl	13	HCl: H ₂ O ₂ : H ₂ O =1:1:2 100+100+200ml=400ml	Bi ₂ Te ₃ Sb ₂ Te ₃ TiW	1'14" 2'17" 2'30"	21 13 0	1162nm 968nm 0	<p>1, BiTe lateral etch 2, SbTe lateral etch 3, TiW bubbles</p>

From Table 3.3, we see two useless etchants, which are Al Etchant A, since it does not etch at all, and $\text{H}_2\text{O}_2\text{-HCl}$ for the large lateral undercut, which is 21 μm for Bi_2Te_3 , and 13 μm for Sb_2Te_3 (shown in Fig 3.13).

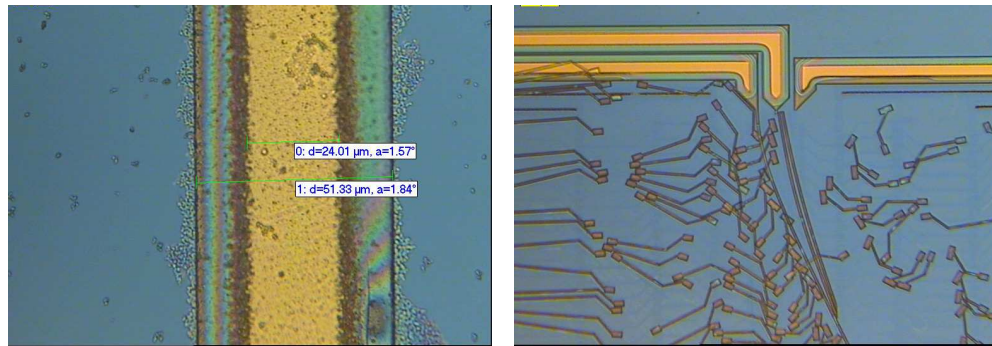


Fig 3.13 large lateral etch of etchant $\text{H}_2\text{O}_2\text{-HCl}$, left: for Sb_2Te_3 , right, for Bi_2Te_3 .

Diluted HNO_3 is a very nice etchant for Sb_2Te_3 , since the etching time is around 5 min, which is easy to control, and the lateral etch is 2 to 5 μm if we dip the wafer every several seconds in the water. The etchant causes an inhibitive layer on the surface of Sb_2Te_3 , which must be dipped off. We employ $\text{HNO}_3\text{: H}_2\text{O}=1\text{:}1$ as the etchant of Sb_2Te_3 , since for lower etchant concentration, the etching rate is too low. However, it is not a good etchant for Bi_2Te_3 , because the etching is too fast, finishing in 5 sec with huge amount of bubbles. It must be point out that when we etch Sb_2Te_3 layer in this etchant, the Bi_2Te_3 structure should be processed later than Sb_2Te_3 or fully capped, because Bi_2Te_3 also dissolves in this etchant,

The diluted Aqua Regia etches Bi_2Te_3 more gently, 43sec, also with bubbles, and the lateral etch is 5 μm . For lower concentration, the etching time would be longer, and the lateral undercut also increases to over 10 μm , shown in Table 3.3 and Fig 3.14. Although 43 sec is still a too short etching time to control, the diluted aqua regia with the composition $\text{HCl: HNO}_3\text{: H}_2\text{O} = 3\text{:}1\text{:}2$ is the best etchant for Bi_2Te_3 . Sb_2Te_3 layers peel off in the diluted Aqua Regia. When we etch Bi_2Te_3 , the Sb_2Te_3 structures should also be well covered.

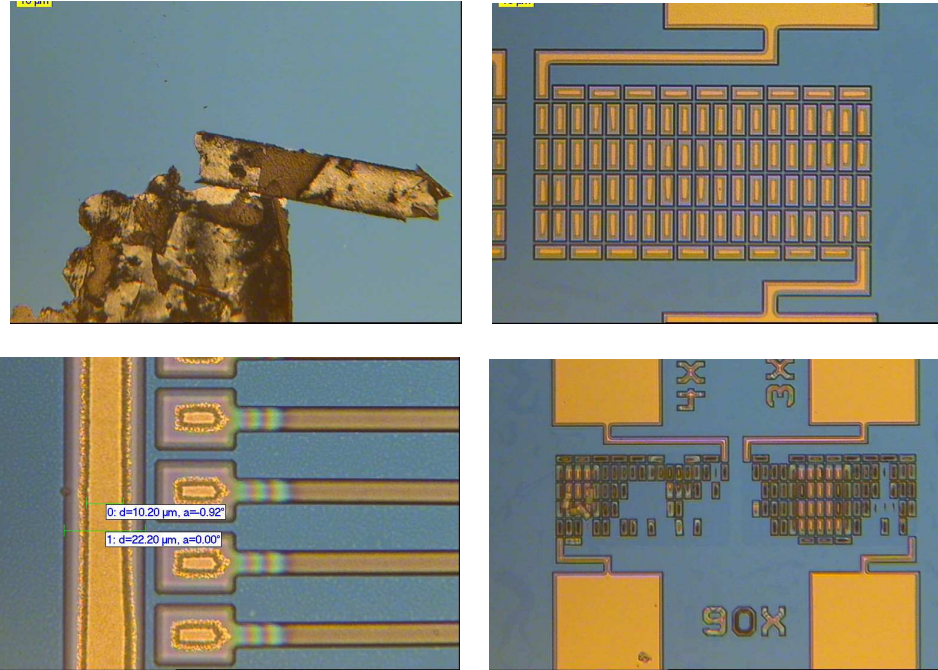


Fig 3.14, top left: Sb_2Te_3 peels off in Aqua Regia; top right& bottom left: Bi_2Te_3 after $\text{HCl}:\text{HNO}_3:\text{H}_2\text{O} = 3:1:2$; bottom right: Bi_2Te_3 after $\text{HCl}:\text{HNO}_3:\text{H}_2\text{O} = 3:1:6$.

In conclusion, the wet etchants for Bi_2Te_3 and Sb_2Te_3 are:

	Etchant	Etch time	Lateral etch
Bi_2Te_3	$\text{HCl}:\text{HNO}_3:\text{H}_2\text{O} = 3:1:2$	43sec	5um
Sb_2Te_3	$\text{HNO}_3:\text{H}_2\text{O} = 1:1$	6' dip	4um

The lateral etch is 4 to 5 times of the layer thickness. We could make the size of the Bi_2Te_3 and Sb_2Te_3 structures on the masks 5um larger etch side to compensate the lateral etch.

3.3 Conclusion

We discussed the patterning methods in this part of the report. Shadowmasking was not investigated, since it is not suitable for small features. Dry etching Bi_2Te_3 and Sb_2Te_3 by Ion Beam Etching is a precise and feasible method, but with redeposition problem, tungsten oxide problem, Bi_2Te_3 attacked by other etchant problem, and the adhesion problem. Finally we choose the wet etching method for patterning Bi_2Te_3 and Sb_2Te_3 . Although the lateral etch is 4-5 times of the layer thickness, the process is easy to control and less troublesome. We should make the structures on the masks larger than designed to compensate the lateral etch.

Chapter 4 Processing

In this part, the processing of the high efficiency Peltier cooling devices is presented and discussed. At first we review the challenges and potential problems for the $\text{Bi}_2\text{Te}_3/\text{Sb}_2\text{Te}_3$ processing. After that, we present the set of experiments that are designed to investigate these challenges. Based on the outcome of these experiments, we present the plan and the results of processing the actual device wafer. At last, we summarize the failures and the results of the process, and give a final flow chart.

4.1 Processing Challenges

As we have already mentioned in Part 1.3, the challenges of this project are mainly in three aspects.

The first one is the patterning of Bi_2Te_3 and Sb_2Te_3 . As we already discussed in Chapter 3, wet etching is taken as the patterning method, and the etchant is $\text{HCl}:\text{HNO}_3:\text{H}_2\text{O}=3:1:2$ for Bi_2Te_3 , and $\text{HNO}_3:\text{H}_2\text{O}=1:1$ for Sb_2Te_3 .

The second challenge is the substrate for $\text{Bi}_2\text{Te}_3/\text{Sb}_2\text{Te}_3$, since Bi_2Te_3 and Sb_2Te_3 shows very poor adhesion to normal IC substrate, silicon (Si) and silicon oxide (SiO_2). Based literatures [7] [14], we identified silicon nitride (Si_3N_4) and polyimide (PI) as possible substrates; however, the adhesion was still unknown. The way to check the adhesion is the tape test. We just deposit the material on the substrate and apply a piece of tape to see if the deposited layer adheres, which we could perform right after the deposition. The tape test is discussed in Part 3.2.

The next problem is the passivation layer of the thermoelectric materials. We must choose a suitable capping material considering the temperature limit for $\text{Bi}_2\text{Te}_3/\text{Sb}_2\text{Te}_3$, which is 290 degreeC [14], and the bad adhesion. SiO_2 is out of the picture for the bad adhesion to the thermoelectric materials. Si_3N_4 could be an option since silicon nitride (Si_3N_4) can be deposited at 250 degreeC using PECVD. Another interesting capping material, which has not been employed in the similar work before, is Parylene, with high step coverage, low deposition temperature and low thermal conductivity (0.08W/m*K vs. 20W/m*K). We will compare Parylene and Si_3N_4 during the process.

Another challenge that should be mentioned, which is also extensively discussed in literature [13] [15], is the deposition and crystallization of Bi_2Te_3 and Sb_2Te_3 . The un-crystallized material gives high electrical resistivity and low figure of merit Z. We should first make sure the material is crystallized after deposition. If it is not, treating with high temperature could crystallize the materials.

4.2 Preliminary experiments

Several basic experiments are designed and performed in this part, for example the deposition and the uniformity of Bi_2Te_3 and Sb_2Te_3 , the adhesion of the thermoelectric material to the substrate, which must be tried out before the real processing of the devices.

4.2.1 Deposition and uniformity of $\text{Bi}_2\text{Te}_3/\text{Sb}_2\text{Te}_3$

The figure of merit of Bi_2Te_3 and Sb_2Te_3 depends on the ratio of Sb/Bi and Te. The optimum ratio is not investigated in this study. Instead, a target that is readily available has been used for the adhesion and patterning experiments. The composition of the targets is,

Bi_2Te_3 : Bi 35.5, Te 64.5.

Sb_2Te_3 : Sb 27.5, Te 72.5.

Deposition takes place by sputtering at room temperature, but the substrate would get warm for the impact of the target atoms. The maximum temperature of the substrate is 60 °C for 1 μm deposition, which is low enough to make sure that the deposition of the second thermoelectric material would not affect the first material. The deposition pressure is 4.1e-3 mbar, and the deposition is at 88.41W.

The diameter of the Bi_2Te_3 and Sb_2Te_3 targets is only two inch, so the target spins in the chamber during the deposition. As a result, the deposited layer is not uniform everywhere, but like a CD-disk, as shown in Fig 4.1.

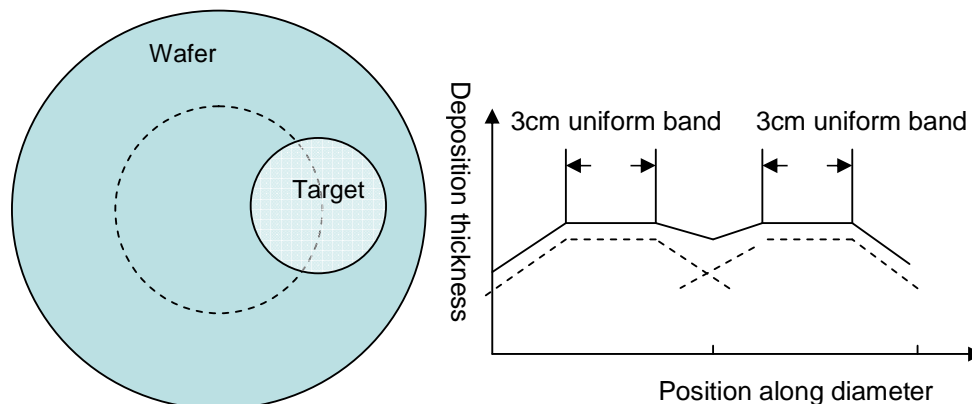


Fig 4.1 left: 6-inch wafer and the orbiting 2-inch target, right: thickness of the deposited layer vs. the position along the diameter of the wafer

After deposition, the uniformity is checked. Since the cases for Bi_2Te_3 and Sb_2Te_3 are similar, Bi_2Te_3 is taken as an example. We started with a wafer with half PI and half TiW substrate, and deposit Bi_2Te_3 on the wafer, in order to see the adhesion of Bi_2Te_3 on PI and TiW. We used the 4 point measurement machine to measure the sheet resistance at 49 different positions on the wafer automatically, and since the sheet resistance is related to the thickness of the layer, the thickness could easily be known. The result of the 4 point measurement machine is in Fig 4.2.

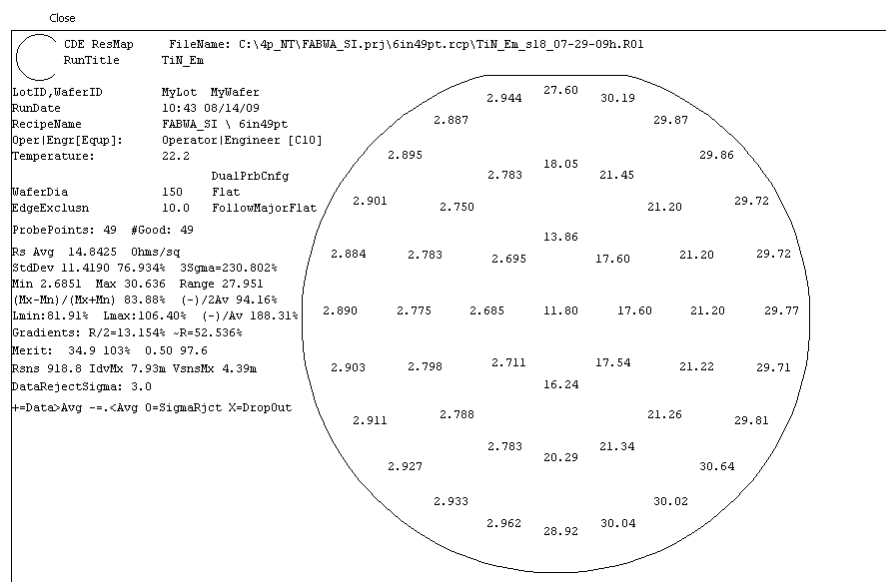


Fig 4.2 map of the sheet resistance on the wafer measured by 4-point measurement

There are two parts in Fig 4.2, which are divided by the centre line. The left part is polyimide+TiW+ Bi₂Te₃, which is of lower and uniform sheet resistance. The right part is polyimide+ Bi₂Te₃, which is of higher and non-uniform sheet resistance. The sheet resistance of the right part of wafer becomes larger towards the edge of the wafer, since the sheet resistance is proportional to 1/d. This result is not as expected, as it is supposed to consist of a uniform band like a CD disk, and thinner layers at other positions. Apparently, the opening angle of the sputter target is quite large, so the centre of the wafer is continuously exposed while other parts are only exposed when passing the target. The sheet resistance of Bi₂Te₃ layer is between 17.6 and 30.64 Ohm/Square, if we apply the resistivity value of Bi₂Te₃ 12.6 uOhm*m (Table 1.1), the thickness of the layer is between 0.42um to 0.74um, which varies almost 100%, resulting in poor uniformity.

A simple measurement to determine the sign of the Seebeck coefficient α is performed here using a heated needle. One probe on the probe station is heated at the power 1.9W, and the output voltage between the two probes is measured. For Bi₂Te₃, the output is 4.5~5mV, and for Sb₂Te₃, the output is -6~-17mV. The result tells us the sign of α value of Bi₂Te₃ is opposite to that of Sb₂Te₃.

4.2.2 Adhesion testing

The adhesion of Bi₂Te₃ and Sb₂Te₃ on PI, Si₃N₄, photoresist (PR), and TiW is checked with the tape test. When we stick the tape on the wafer and pull up the tape from one side, the top layer would come off from the wafer, if the adhesion is not very good. If the adhesion is good, the tape would not bring the top layer off. The results are listed in Table 4.1.

Table 4.1: tape test result

	Si ₃ N ₄	PI	PR	TiW
Bi ₂ Te ₃	Good	Good	Came off	Good
Sb ₂ Te ₃	Good	Good	Not measured	Good
TiW	Good	Good	Not measured	Not Measured

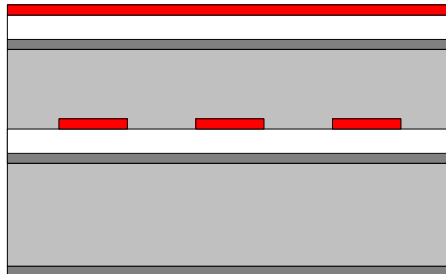
4.3 Flow plan

The general flow of the process is first to coat polyimide or silicon nitride as the substrate, then to make the bottom TiW electrodes, and to make the structure of the 1st thermoelectric material, then intermediate layer, and 2nd thermoelectric material, after that the basic device is finished, which is capped by a passivation layer. Then the metal bondpads are made on top of the wafer, and the last step is to etch through the wafer from the backside. The process is also demonstrated in Fig 4.3.

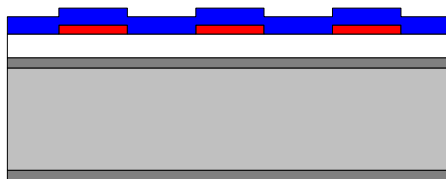
(1) coat PI or SIN as substrate



(2) deposit TiW

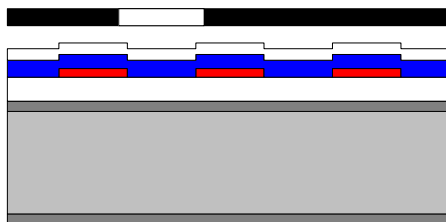


(3) pattern TiW as electrodes

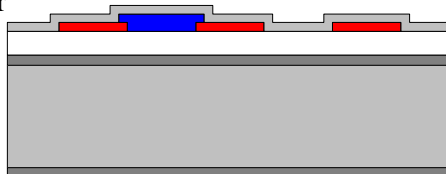


(4) deposit 1st material

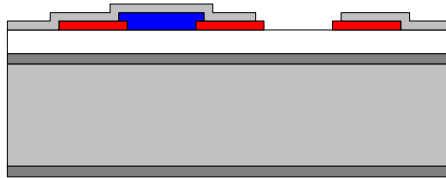
(5) patterning 1st material



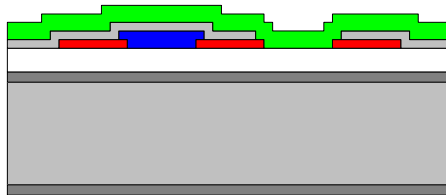
(6) capping the intermediate layer



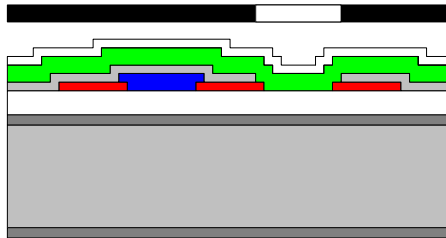
(7) opening windows for the 2nd material



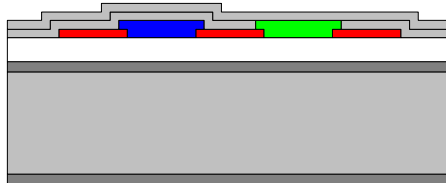
(8) deposit the 2nd material



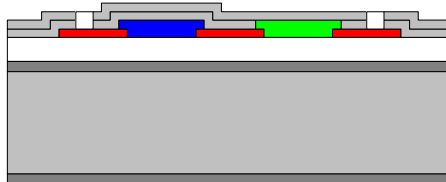
(9) patterning the 2nd material



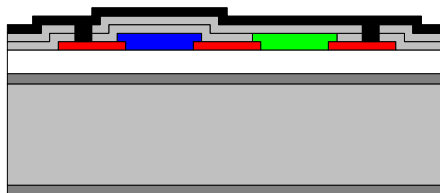
(10) coating the passivation layer



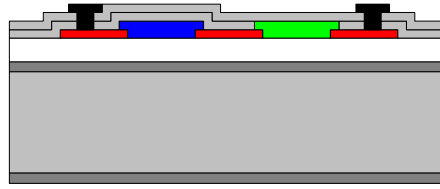
(11) opening contact of the metal bond pad



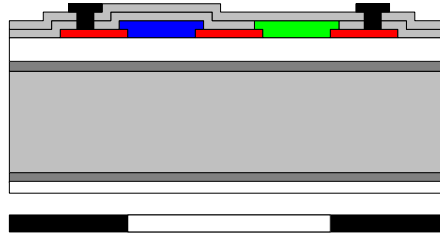
(12) depositing the metal layer



(13) patterning the bondpads



(14) back etching



(15) final devices

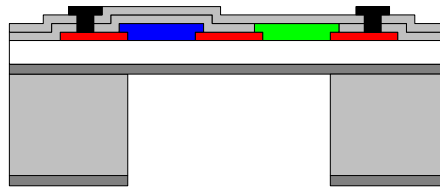


Fig 4.3 steps of the process flow

According to the adhesion and the etching method we discussed in Part 3.2, polyimide and silicon nitride could be used as the substrate. Polyimide is also needed for nitride substrate wafers for supporting the device after back etching, and Si_3N_4 could be deposited on top of polyimide as the nitride substrate. The patterning method is wet etching. The intermediate layer could be Si_3N_4 for its good adhesion and nice capping, or photoresist, which is low temperature process. There are also two options for passivation layer, the Parylene and Si_3N_4 . Attention should be paid to Parylene, since it has not been used for similar devices before. Parylene is a polymer with low coating temperature and excellent step coverage, and additionally a low thermal conductivity, which is necessary for high efficiency thermoelectric devices.

The materials mentioned above can be divided into two types, the polymer and the silicon nitride. The plan is to process the wafers with nitride substrate, nitride intermediate layer and nitride passivation layer, and the wafers with polyimide substrate, photoresist intermediate layer and Parylene passivation layer. These wafers are taken as the pioneer wafers. After processing, we will try to conclude which group is better or we combine the best materials and make a final flow chart.

4.4 Initial flow chart and processing

Based on what we have discussed, the initial flow chart is shown in Appendix D-1.

Special Details in Design (marked as A, B... in Appendix D-1) is explained as follows.

[A] Before the deposition of Bi_2Te_3 and Sb_2Te_3 , a prebake step is needed to remove the water in the substrate polyimide, since the water could evaporate in the following steps and destroy Bi_2Te_3 or Sb_2Te_3 . The prebake step could be taken on the 150 degreeC hot plate for 5mins.

A sputter etch step is also needed to remove the natural oxide layer on the surface of TiW electrode for better adhesion and lower contact resistivity.

[B] The nitride is deposited in the Novellus machine at 250 degreeC, which is lower than the recorded evaporation temperature of Te element. The thinner the nitride is, the lower the thermal conduction is. But the deposition of Si_3N_4 at 250 degreeC is not precisely controlled; 100nm is the thinnest thickness we could get.

[C] Because of the natural oxide layer on top of TiW electrodes, the sputter etch is needed before the Al deposition for better contact.

The problems we met in the process are as follows, also marked as 1, 2, and 3 ...in Appendix D-1.

[1] After the TiW layer is deposited on polyimide, there are some black ring shapes in the layer under the microscope, shown in Fig 4.4a. We also checked the layer under the SEM, shown in Fig 4.4b. The surface of TiW layer is smooth, and the rings are all covered by the metal layer. The rings are caused by the wrinkles on polyimide, and TiW layer is just following the polyimide surface perfectly.

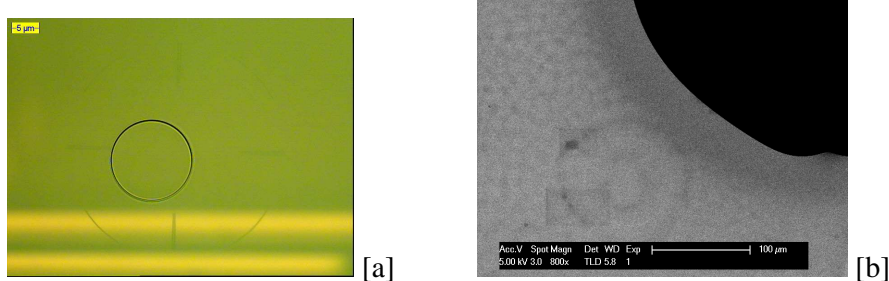


Fig 4.4 the rings on the TiW layer [a] under the microscope, [b] under the SEM

[2] The dry etching for TiW gives precise structures, but the F- or Cl- based etchant also attacks Si_3N_4 . So the TiW layer with Si_3N_4 substrate could not be etched by RIE. The original TiW layer is 200nm, as we designed. The stepheight of the wet etching TiW is 145nm, and the stepheight of the dry etching TiW is 270nm. The layer becomes thinner after the wet etching because of the lateral etch of the etchant and the peeling off of the photoresist, while it becomes thicker after the dry etching since the polyimide substrate is also impacted by the RIE etchant. (The layer doesn't become thicker, the step is higher)

To protect the substrate, we decide to use the wet etching method. If the TiW layer is increased to 250nm, the layer thickness after etching would be around 200nm, as we designed.

[3] The etching time for Bi_2Te_3 is 1min (continuous) with the lateral undercut 16um (at the edge) and 7um (in the middle), and 55sec (15sec step) with the lateral undercut 9um (at the edge) and 7um (in the middle). The etch is processed in such a small bath that the refreshment of the etchant at the centre of the wafer may be insufficient, so the etching takes place from the edge of the wafer to the centre, prolonging the etching time, causing the lateral etch of the edge much larger than what we got in Part

3.2, and also larger than the centre. If we process the wafer with 15sec step, meaning we take the wafer out every 15sec, the lack of the etchant at the wafer centre could be compensated by the flow of the etchant, and the etching is more uniform through the whole wafer.

[4] When we strip the primer on Si_3N_4 for the photoresist in the developer, 70% of the Bi_2Te_3 structures come off into the development bath, shown in Fig 4.5. The reason may be the pinholes in the Si_3N_4 lead the developer to the Bi_2Te_3 . 100nm Si_3N_4 seems not enough, we could try 100nm Si_3N_4 at 250 degreeC + 500nm Si_3N_4 at 300 degreeC, and remove the primer by O_2 plasma instead of development bath.

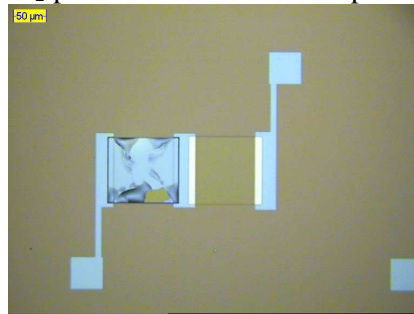


Fig 4.5 structure attacked by the developer when we strip the primer

[5] The Sb_2Te_3 etching takes 2min 30sec for the polymer wafer and 4min for the nitride wafer, excluding the time dipping the wafer into the wafer. The latter wafer takes more time because the concentration of the etchant is lower due to the consumption of the etchant and the water brought by the dipping. The lateral etch is 4.32um and 3.49um, which are as we expected. The Sb_2Te_3 etching is better than the Bi_2Te_3 etching in the process from the aspect of lateral undercut, shown in Fig 4.6.

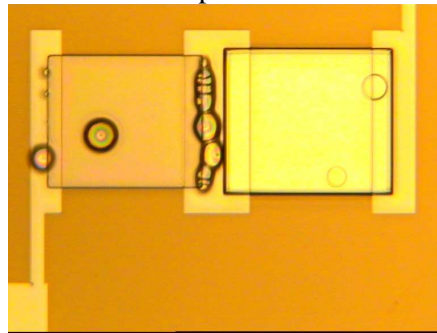


Fig 4.6 structure with patterned Bi_2Te_3 (left) and Sb_2Te_3 (right) after wet etching Sb_2Te_3 , with intermediate photoresist covering Bi_2Te_3

The SEM pictures for Bi_2Te_3 and Sb_2Te_3 after the wet etching are shown in Fig 4.7, of the structures on the wafer with photoresist intermediate layer. The photos are taken after the removal of the photoresist. There is no re-deposition at the edge of the structures, and the edge is smooth. For Bi_2Te_3 , the lateral undercut is large, and the partly etched area seems floating. It looks that Bi_2Te_3 layer cracks along the edge of TiW, but when we zoom in, the layer is still connected. For Sb_2Te_3 , the partly etched area is smaller.

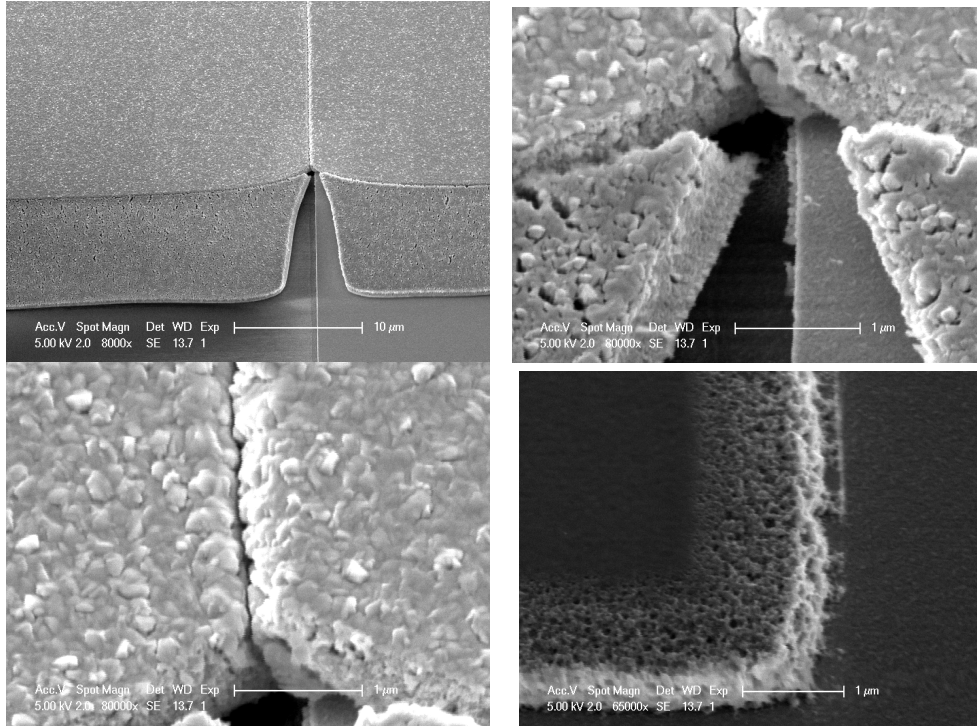


Fig 4.7 Top & bottom left: Bi_2Te_3 ; bottom right: Sb_2Te_3

Some of the remaining Bi_2Te_3 structures on the nitride wafer, as we described in problem [4], come off after the etching. Only 10% Bi_2Te_3 structures are left. In contrast, all Bi_2Te_3 structures on the wafer with PI substrate and photoresist intermediate layer are still on the wafer.

[6] The photoresist, probably the intermediate photoresist, could not be removed by acetone strip. One access step of 47min acetone soak could not remove the photoresist either, as shown in Fig 4.8. The problem could be that the sputter etch destroyed the photoresist.

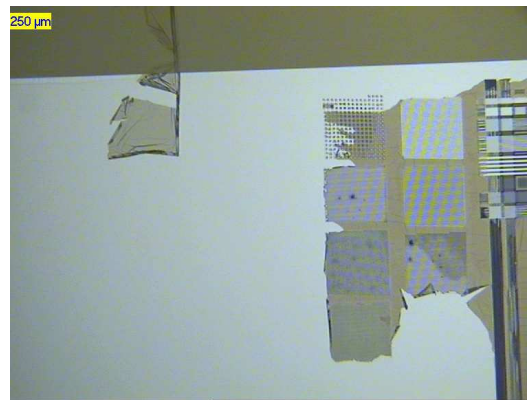


Fig 4.8 photoresist residues on the wafer, which could not be dissolved in acetone

To remove the unsolvable intermediate photoresist, the O_2 plasma strip in the Fusion machine is employed. The etching rate for O_2 plasma at 90 degreeC is rather slow. To increase the etching rate, we employed the O_2 plasma at 120 degreeC. The high temperature causes high stress in the TiW layer, resulting in wrinkles and cracks at the corner of the TiW structure. The narrow lines of TiW even come off the wafer and

curl up, as shown in the SEM pictures in Fig 4.9. Obviously, 120 degreeC is too high for TiW structures. The temperature of the O₂ plasma should not be over 90 degreeC.

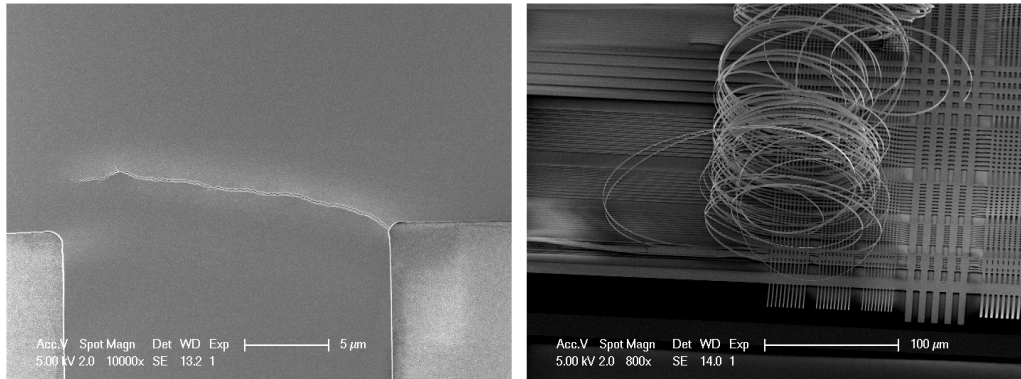


Fig 4.9, left: cracks in TiW after 5min of 120 degreeC O₂ plasma; right: TiW curls

After trial on other wafers, the suitable method to remove the intermediate photoresist is 110min O₂ plasma @ 90 degreeC.

[7] When we develop the photoresist to pattern Al, the Bi₂Te₃ structures and the Sb₂Te₃ structures under the 500nm SiO₂ + 100nm Si₃N₄ layer come off into the development bath. This time we are sure the capping thickness is enough, maybe the pinholes and the poor adhesion are the problem.

[8] After the wafer is coated Parylene, the backside was also covered by Parylene even though it was not planned. If we coat photoresist AZ9260 on the backside without removing Parylene, bubbles would come up during the exposure under Parylene. It may be because that Parylene releases gas under the light, and the gas goes under the Parylene since the adhesion between Parylene and the oxide on the backside is not good enough due to the lack of the primer. The bubbles not only happened under the high density exposure, but also under the light of the microscope. We could easily observe the forming of the bubble under the microscope, shown in Fig 4.10. The Parylene should be removed with a knife and a tape before coating the photoresist on the back side.

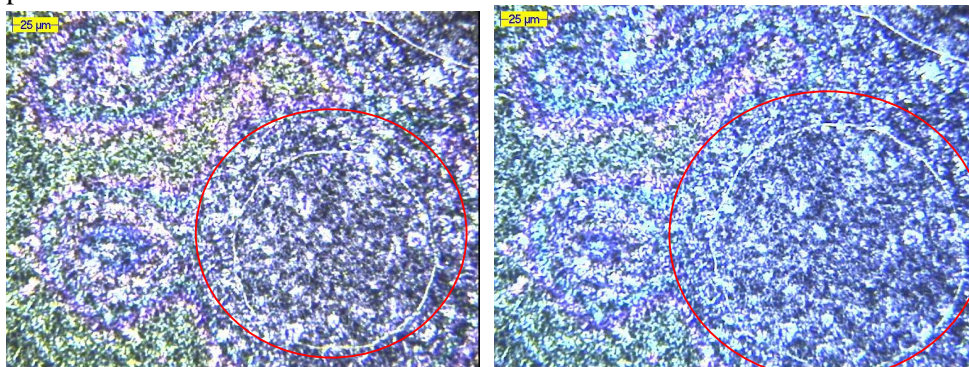


Fig 4.10 photos of the bubble under the Parylene, the small bubble (left) grows bigger (right) in a few seconds

[9] When we develop the photoresist AZ9260 for back side deep etching, it is necessary to coat the front side of the wafer with other photoresist since Al bond pads reacts with AZ 400K, the developer for AZ9260. The photoresist also protects the

structures, since Bi_2Te_3 and Sb_2Te_3 structures tend to peel off in the development bath, as we observed in problem [5].

[10] The one hour hard bake for AZ9260 is to evaporate the solvent in the photoresist, since we have experience that a wafer without hard bake got many random holes during the deep etch because the UV in the deep etch causes the solvent to explode. Half an hour hard bake would also work.

Some other experiment results:

[1] The wet etching time for TiW, Bi_2Te_3 , Sb_2Te_3 , and Al for the experimental wafers is listed in Table 4.2 as a reference for further research on this project.

Table 4.2: etching time of materials on different wafers

	#1	#2	#3	#4	#5	#7	#8
TiW	8'05"	8'05"	/	/	8'48"	8'48"	8'30"
Bi_2Te_3	1'	3'	55"	1'10"	1'45"	2'15"	2'50"
Sb_2Te_3	4'	2'	2'30"	2'15"	1'57"	2'	1'50"
Al	12'25"	12'	13'11"	10'40"	10'20"	/	13'

[2] We tried two cases, one of which is to first deal with Bi_2Te_3 , then Sb_2Te_3 , and the other of which is to first deal with Sb_2Te_3 , then Bi_2Te_3 , and there is no significant difference between the two cases.

[3] On the wafers with nitride intermediate layers and nitride capping layers, the Bi_2Te_3 and Sb_2Te_3 structures peel off heavily, the yield of some of the wafers is almost 0. The peeling off of the structures always happens at 1), removing the TCPS primer for intermediate Si_3N_4 layer, 2), etching the second thermoelectric material when the first material also comes off, 3), developing the photoresist for Al bond pads. It seems that there are pinholes in Si_3N_4 , through which the chemical contacts Bi_2Te_3 and Sb_2Te_3 and attacks them, since the peeling off happens to the structures underneath the nitride after the deposition of Si_3N_4 . The thickness of the nitride is not the reason of the pinholes, since for the third case, the capping layer is 100nm Si_3N_4 + 500nm SiO_2 , which is quite thick.

Strangely, while the tape test shows the good adhesion, and the developer did not attack the material when we patterned it, just after one Si_3N_4 capping layer, the characters change a lot, the adhesion becomes poor, and the thermoelectric material becomes easily attacked. In contrast, the structures on the wafers with photoresist and Parylene stay well. The peeling off may be not caused by the bad Si_3N_4 layer, but because the high temperature or the chemical process for the Si_3N_4 and SiO_2 deposition in Novellus machine affects or destroys Bi_2Te_3 and Sb_2Te_3 , although the deposition temperature of 250 degreeC is relatively low. If this is the case, the deposition temperature of Si_3N_4 and SiO_2 needs to decrease even more.

[4] On the wafers with photoresist intermediate layers and Parylene capping layers, the Bi_2Te_3 and Sb_2Te_3 structures are well patterned, without peeling off. However, after the sputter etch and the deposition of Al, the Parylene layer becomes rough, and the adhesion between Al and Parylene is so bad that after patterning, all Al structures delaminates only connecting to TiW at the bond pads. The Parylene layer is also destroyed, causing Bi_2Te_3 and Sb_2Te_3 structures attacked by the Al etchant. A structure covered with Parylene is shown in Fig 4.11, on which Al was deposited then

removed since the layer was too rough. We could see cracks in Parylene and Sb_2Te_3 layer clearly. The device is also checked under the SEM, and the photos are in Fig 4.12. In the photo, there are cracks in Parylene, of which the surface is not smooth, and the covered metal exposes at the cracks. The reason why Parylene is destroyed so badly is that we ordered the normal power Al deposition, which goes to high temperature during the deposition and destroyed the Parylene layer. The solution may be to deposit the Al layer using low power.

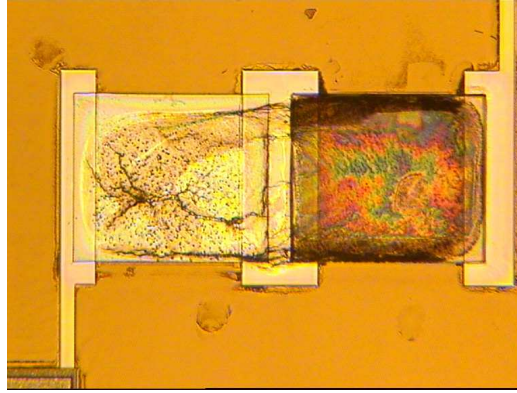


Fig 4.11 structure with a Parylene layer destroyed by the Al deposition

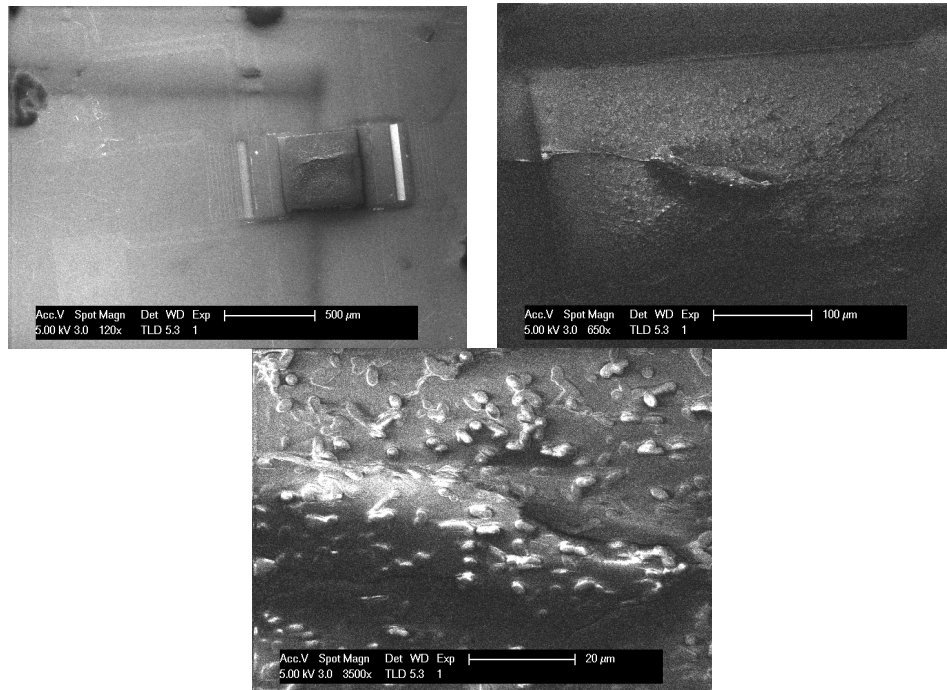


Fig 4.12 SEM photos for the destroyed Parylene surface

In conclusion, starting from the initial flow chart, several wafers in two groups, the nitride group and the polymer group, are processed. Most of the problems we met are solved, for example, the irremovable photoresist and the bubbles in the photoresist for back etching. However, the peeling off problem of the nitride wafers, and the Al deposition problem of the polymer wafer are still not solved, although possible solutions are brought up.

4.5 Final flow chart and recommendation

The final flow chart for the wafers with nitride substrate, nitride intermediate layer, and nitride passivation layer and the wafers with polyimide substrate, photoresist intermediate layer and Parylene passivation layer is shown in Appendix D-2.

The wafers with nitride have a low yield, since Bi_2Te_3 and Sb_2Te_3 structures tend to peel off in the chemical bath, including the developer bath and the wet etchant bath, after capping Si_3N_4 . We could replace the development bath for removal of the primer, but we could not avoid the etching of materials and developing of the photoresist. From this point of view, the approach with intermediate photoresist and Parylene is much better, since no peeling off happens on these wafers. However, the deposition of Al on Parylene causes cracks and rough surface of Parylene, we could try to deposit the Al using low power. The deposition of Al on Si_3N_4 is of no problem. For metallization step, the Si_3N_4 approach is better.

To sum up, from the process aspect, we would like to recommend the photoresist intermediate layer, and Parylene passivation layer. It does not matter if the substrate is polyimide or Si_3N_4 .

The five wafers we processed are listed in Table 4.3. There are two wafers with Si_3N_4 , wafer #1 and #8, with the yields zero. The two wafers with polymer, wafer #3 and #4, have higher yields, 100% and 70%. On wafer #4, the Al deposition destroys Parylene so badly that we have to leave this wafer without Al. There is another wafer, wafer #7, with Si_3N_4 intermediate layer but Parylene capping, with the yield of 60% and without Al layer. For wafer #3, there seems an oxide layer somewhere in the device that we need to breakdown in the measurement, and unfortunately the devices are not functional. Wafer #4 and #7 are functional.

Table 4.3 five wafers which are processed

	Substrate	Intermediate layer	Capping	With Al?	Yield (%)
#1	Si_3N_4	Si_3N_4	Si_3N_4	Y	0
#3	Polyimide	Photoresist	Parylene	Y	100
#4	Polyimide	Photoresist	Parylene	N	70
#7	Si_3N_4	Si_3N_4	Parylene	N	60
#8	Si_3N_4	Si_3N_4	Si_3N_4	Y	0

4.6 Conclusion

The main challenges of the processing the Peltier devices based on Bi_2Te_3 and Sb_2Te_3 are the adhesion, the patterning method, and the capping layer. First we checked adhesion of the materials to Si_3N_4 and polyimide by the tape test. Then the deposition and the crystallization of the Bi_2Te_3 and Sb_2Te_3 are discussed. After that, we studied the several patterning methods, and decided on the wet etching. We met some problems when we processed the wafers in two groups, the nitride group and the polymer group, according to the initial flow chart. Most of them are solved. The

structures on nitride wafers peel off severely, and the Al deposition on the polymer wafer kills the Parylene layer. We recommend the process flow with polymers, and we could improve it by depositing the Al layer with low power.

Chapter 5 Measurements

The devices are characterized on the wafer using probe station and a thermal camera. First some characters of the material are measured, for example, the sheet resistance, the contact resistivity, the Seebeck coefficient, and the total resistance of the device. Then the cooling is checked under using the cross structures in Fig 2.18. Also, the cooling temperature is measured with the thermal camera. Based on the experimentally determined material parameters, we simulate the device in COMSOL again, and the simulation result is compared with the measurement result.

5.1 measurement setup

The parameters of Bi_2Te_3 and Sb_2Te_3 , for example, the sheet resistance, the contact resistivity and the Seebeck coefficient, are measured on a probe station, using a multimeter and a curve tracer.

5.1.1 Sheet resistance.

For the sheet resistance we use the so-called Van der Pauw structure in Fig5.1, if we apply a current through the left two bondpads, and measure the output voltage for the right two bondpads, the sheet resistance of the centre material is calculated as follows.

$$R_{\square} = 4.53 \frac{V}{I}$$

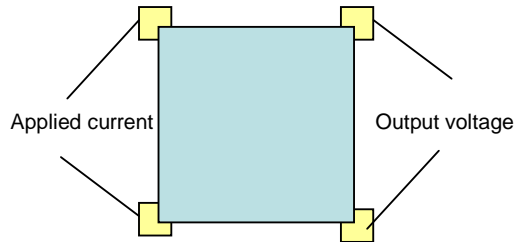


Fig 5.1 Van der Pauw structure to determine sheet resistance

The results of sheet resistance are in Table 5.1.

Table 5.1: sheet resistance of Bi_2Te_3 and Sb_2Te_3

	Sheet resistance(Ohm/square)			
TiW	3.6			
Al	0.2			
Bi_2Te_3 (literature)	12.6			
Sb_2Te_3 (literature)	12.6			
First Bi_2Te_3	Bi_2Te_3 (centre)	21.2	Sb_2Te_3 (centre)	/

Then Sb ₂ Te ₃	Bi ₂ Te ₃ (edge)	27	Sb ₂ Te ₃ (edge)	56
First Sb ₂ Te ₃	Bi ₂ Te ₃ (centre)	/	Sb ₂ Te ₃ (centre)	/
Then Sb ₂ Te ₃	Bi ₂ Te ₃ (edge)	27	Sb ₂ Te ₃ (edge)	63
First Bi ₂ Te ₃	Bi ₂ Te ₃ (centre)	19	Sb ₂ Te ₃ (centre)	74
Then 250~300 degreeC	Bi ₂ Te ₃ (edge)	28	Sb ₂ Te ₃ (edge)	76
Then Sb ₂ Te ₃				
Average	Bi ₂ Te ₃	24	Sb ₂ Te ₃	67

The values listed in Table 5.1 are mean values, averaged over typical 4 devices per location on the wafer. ‘/’ means the test structures were not functional. The literature values of Bi₂Te₃ and Sb₂Te₃ are calculated as follows.

$$R_{\square} = \frac{\rho}{d} = \frac{12.6\text{Ohm} * \text{um}}{1\text{um}} = 12.6\text{Ohm}$$

According to the result, it does not matter if we process with Bi₂Te₃ first or Sb₂Te₃ first. Apparently, the high temperature process does not affect the sheet resistance. The sheet resistance of both Bi₂Te₃ and Sb₂Te₃ are higher than the literature value. In particular for Sb₂Te₃, the measurement value is three to four times the literature value. The higher sheet resistance is most likely due to the fact that the composition differs from the materials in the literature. Also, because we use sputtered thin film materials, the layers might not be fully crystallized. We take the average value as the sheet resistance, which is 24Ohm/Square for Bi₂Te₃, and 67Ohm/Square for Sb₂Te₃.

5.1.2 Contact resistivity

The contact resistivity is measured using the so-called Kelvin structure in Fig 5.2. The current is applied through two adjacent bondpads, and the voltage is measured from the other two bond pads. The contact resistance is calculated as:

$$R = \frac{V}{I}.$$

The contact resistivity is:

$$R_c = \frac{R}{l * w}.$$

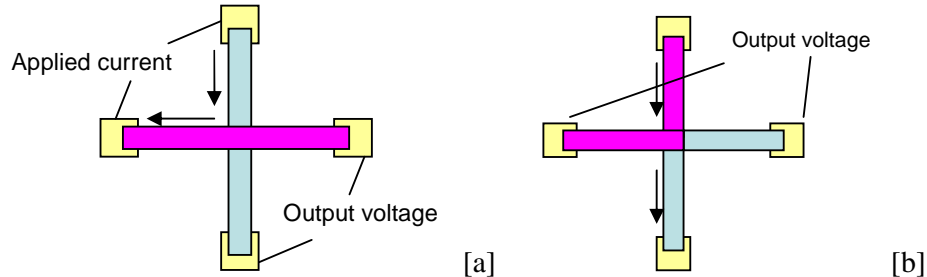


Fig 5.2 [a] the demonstration of the contact resistance measurement, [b] classical Kelvin structure for contact resistance measurement

The contact resistance and the contact area are listed in Table 5.2.

Table 5.2: contact resistance for Bi₂Te₃ and Sb₂Te₃ to TiW

Material	Resistance(Ohm)	Area(um)	Contact resistivity(Ohm*um ²)
Bi ₂ Te ₃ /TiW	0.7	52*58	2111
Bi ₂ Te ₃ /TiW	0.6	148*143	12698
Sb ₂ Te ₃ /TiW	13	14*29	5278
Sb ₂ Te ₃ /TiW	9	44*57	22572
Sb ₂ Te ₃ /TiW	7	85*98	57715
Sb ₂ Te ₃ /TiW	1.3	136*149	26343

The contact resistivity should be a constant, but the result varies a lot. There are two possible reasons. The first one is that for small contacts side effects at the circumference of the contact area might dominate the contact resistance. For large contact areas these side effects can be neglected since the circumference scales linearly with the contact dimensions whereas the contact area scales quadratically with the contact dimensions. So the contact resistance does not change much with the contact area. The second reason could be the shape of the Kelvin structures. Usually, a Kelvin structure is designed as in figure 5.2b in which the current flow is in a straight line. We deliberately chose our structures as in figure 5.2a to avoid the influence of misalignment on the contact area, which could certainly be present in the hard mask concept. However, now the current flow should follow a curved line which might result in an apparent contact area that is smaller than the geometric area. We take the average value for contact resistivity, which is 7404 ohm*um² for Bi₂Te₃/TiW, and 27977 ohm*um² for Sb₂Te₃/TiW.

5.1.3 Device resistance

For the devices, the resistance from one bondpad to another contains the following parts, 1 & 5 & 9, the TiW electrodes, 2 & 4, the contact resistance between TiW and Sb₂Te₃, 3, Sb₂Te₃, 6 & 8, the contact resistance between TiW and Bi₂Te₃, 7, Bi₂Te₃, shown in Fig 5.3.

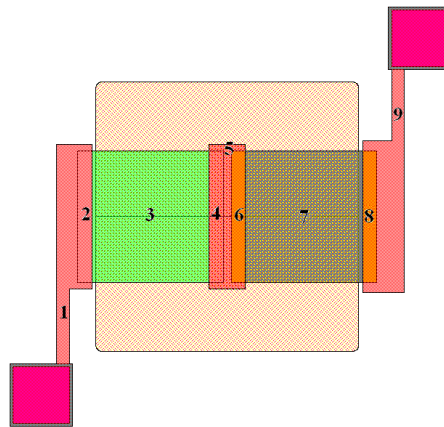


Fig 5.3 the nine parts in the device to form the total resistance from one bond pad to the other

The final size and the resistance of every part is shown in Table 5.3

Table 5.3: calculation of total resistance based on the size and measured resistivity

L		1	3	5	7	9
	Size(um/um)	205/40	895/825	50/840	888/821	205/40
	Sheet resistance(Ohm/Square)	3.6	67	3.6	24	3.6
	Resistance(Ohm)	18.5	72.7	0.2	26	18.5
		2	4	6	8	
	Size(um*um)	825*85	825*75	821*78	821*78	
	Contact resistivity(Ohm*um ²)	27977	27977	7404	7404	
	Resistance(Ohm)	0.39	0.45	0.11	0.11	
	Total resistance(Ohm)	136.96				
M		1	3	5	7	9
	Size(um/um)	480/80	480/410	50/420	467/398	480/80
	Sheet resistance(Ohm/Square)	3.6	67	3.6	24	3.6
	Resistance(Ohm)	21.6	78.4	0.4	28.2	21.6
		2	4	6	8	
	Size(um*um)	409*55	410*68	398*60	397*49	
	Contact resistivity(Ohm*um ²)	27977	27977	7404	7404	
	Resistance(Ohm)	1.24	1	0.3	0.4	
	Total resistance(Ohm)	153.1				

The biggest part in the total resistance is the resistance of Sb₂Te₃. The total resistance we measured on the probe station is 0.15K~0.37K ohm (average 0.25K) for the big structures, and 0.18-0.31K (average 0.22K) for the middle structures.

On average, the total resistance we measured are larger than calculated. The additional resistance comes from the contact resistance between the probes and the bond pads, and the error of the contact resistivity for Bi₂Te₃/TiW and for Sb₂Te₃/TiW.

5.1.4 Seebeck coefficient

The structure in Fig 5.4 (also in Fig 2.19) is used to measure the Seebeck coefficient. It comprises a thermocouple, a heater and two aluminium resistors to measure the absolute temperature at both sides of the thermocouple. First, the temperature coefficient of the resistance of aluminium is determined. This is done with the use of a probe station which could control the temperature of the wafer with a heated chuck. Since Al has a positive temperature coefficient, which means the resistance of Al resistor increases with increasing the temperature, we could determine the temperature difference by measuring the resistance difference. Hence we could heat one side of the thermocouple, and the temperature difference referred to the resistance difference and the output voltage are known. Then the Seebeck coefficient can be calculated.

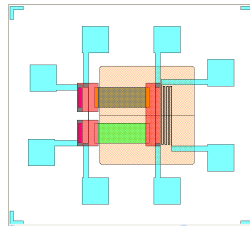


Fig 5.4 the layout of the structure for combined Seebeck coefficient measurement

At first, the chuck is set at different temperatures with the heaters off to gauge the resistance of the Al resistor on the membrane. The result is listed in Table 5.4. The output current decreases 1mA with the temperature increasing 5 K when we apply 1mV to the Al resistor. The current in the resistors is chosen such that self-heating is kept to a minimum. We can also see from Table 5.4 that the output current is quite sensitive if we move the needle, because the resistance of the Al resistor is rather low,. Consequently, the contact resistance between the needle and the Al bondpads affects the total resistance.

Table 5.4: V-I relation of the resistors

Temperature(DegreeC)	10	15	20	25	30	35	40
Applied voltage (mV)	1	1	1	1	1	1	1
Output current (uA)	71	70	69	68	67	65	61(needle moved)

In the next step, we keep the chuck at 15 degreeC with the heater off, so all the structures are at 15 degreeC, and we measure the resistance of the Al resistor. Then we apply 5.4mA current for 5 sec to the heater, and then measure the resistance of the Al heater and the open loop output voltage of the thermocouple. The result is listed in Table 5.5.

Table 5.5: input currents and output voltages with the heater on and off

Current(heater off)	43.9uA
Current(heater on)	42.8uA
Output voltage(heater off)	65uV
Output voltage(heater on)	1.47mV

The 1uA change in the current shows the temperature difference between the on and off status of the heater is about 5 K. The output voltage due to the Seebeck effect is 1.47mV-65uV=1.41mV.

The combined Seebeck coefficient is calculated as

$$\alpha = \frac{1.41mV}{5K} = 282\mu V / K .$$

Comparing with the literature value $\alpha_{total} = \alpha_{Sb2Te3} - \alpha_{Bi2Te3} = 188 + 248 = 436(\mu V / K)$, the Seebeck coefficient of the materials we used in the experiment is much smaller than the literature value. The reason may be 1 that the materials we used are thin films but not bulk materials, 2, that the material is not well crystallized, 3, the materials are attacked by the high temperature or the etchant.

Since the contact resistance between the needle and the bond pads affects gauging the resistor, the result is not quite accurate. A way to improve this is to measure the Seebeck coefficient with similar method after dicing and bonding the wafer to avoid the changing of the contact resistance.

5.2 Results

The refrigeration ability of the device is checked on the probe station with the multimeter using the cross structures, and the cooling temperature is measured under the thermal camera. The device is simulated again with the program COMSOL,

considering the parameters we measured, and the simulation result is compared with the measurement result.

5.2.1 Measurement of the cross structure

The cooling performance of the devices is determined on the probe station with the cross structures shown in Fig 5.5. When the current is applied through the top two bondpads, the central electrode will absorb or release heat due to the Peltier effect, causing the temperature to increase or decrease. Then the output voltage due to the Seebeck effect is measured at the bottom two bondpads, showing how much the central electrode cools or heats.

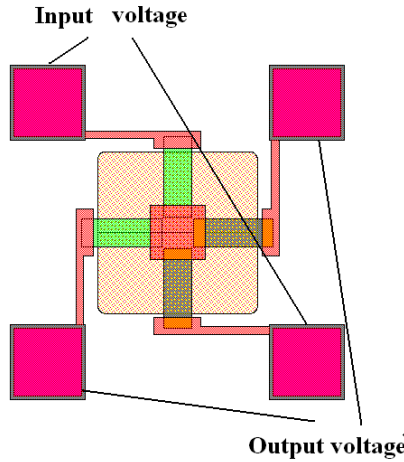


Fig 5.5 Test structures to measure the cooling performance of the thermocouples

The highest output voltage we could get due to the cooling is 0.94mV for the input voltage 1.2V (input current $I = 1.2V / 0.33K\Omega = 3.6mA$, the resistance is the average of measured value). On average, this voltage is around 0.2mV, with the input voltage around 0.6V (input current $I = 0.6V / 0.33K\Omega = 1.8mA$).

According to the combined Seebeck coefficient we got in Part 4.1, $\alpha = 282\mu V / K$, the maximum cooling temperature could be calculated.

$$\Delta T_{\max} = \frac{V}{\alpha} = \frac{0.94mV}{282\mu V / K} = 3.3K$$

$$\text{and } \Delta T_{\max} = \frac{V}{\alpha} = \frac{0.2mV}{282\mu V / K} = 0.71K$$

The maximum cooling temperature is much less than we expected.

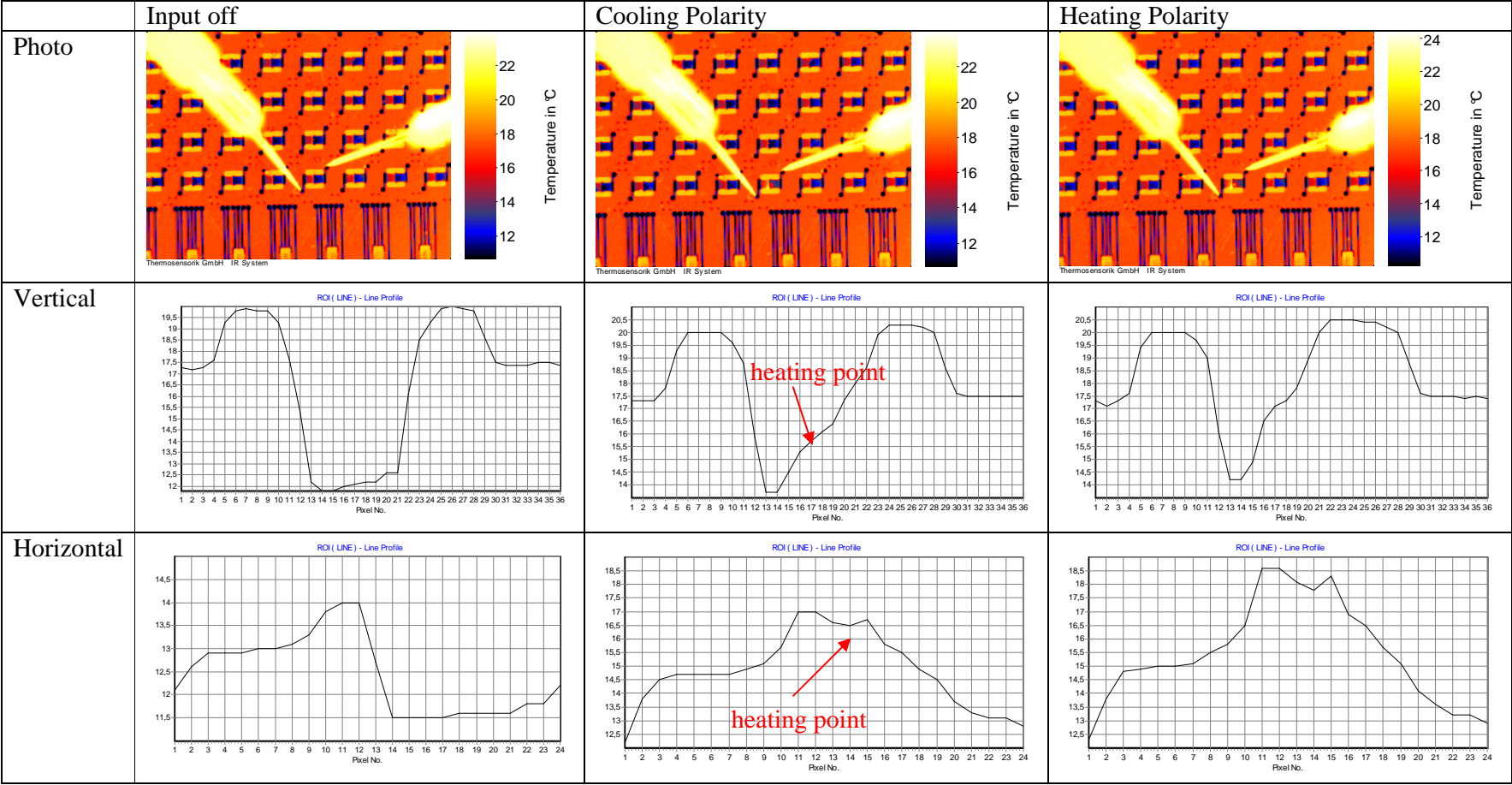
5.2.2 Measurement of the cooling devices

The cooling performance of the devices is also measured under the thermal camera. The thermal camera has a resolution of 0.1 degreeC. However the result is affected by the emission factor of the different materials on the wafer, so seeing through the thermal camera the temperature of the different materials is not the same.

In upper row of figure 5.6 three thermal images are depicted; one for zero input power (left), 1 V (with the current $I = 1V / 0.22K = 4.5mA$, the resistance is from Part 5.1) in cooling mode (middle) and 1 V in heating mode (opposite current flow) (right). In the two rows below line plots along the centre of the device in vertical and horizontal direction are given. In cooling mode, the temperature does not change with increasing input voltage at first. However, when the input is higher than 0.5V, the device temperature starts to increase with the input voltage. If we apply the input with opposite polarity, the temperature increases as soon as we apply input voltage. The heating point is at the bottom left corner of the right material (Sb_2Te_3), and the contact area of the central electrode with both the materials. Unfortunately, we could not observe cooling with these devices, when it should cool, we only see the jitter of the temperature profile. One possible problem is the resolution of the microscope is not good enough. Of course the cooling is not strong enough either. The temperature difference is only 1.5 K at 4.5mA input. The temperature difference just eliminates the effect of Joule heating, and is twice the cooling temperature. So the cooling temperature at input 1 V is only 0.75K, which is much lower than we expected.

The reason why the cooling is much smaller than the simulation result is that 1, the simulation is under the thermal isolation condition, and the air also conducts heat from the cooling part to the heat sink, 2, the Seebeck coefficient is lower than literature, 3, the resistance of Sb_2Te_3 is much higher than expected.

Fig 5.6 list of the result of thermal camera



5.3 Simulation result vs. Measurement result

Based on all the parameters we have got in the experiment (see table 5.6), we could simulate the device again. We measured the combined Seebeck coefficient as 282uV/K, and we assume that the ratio of the value for Bi₂Te₃ and Sb₂Te₃ is the same as in the literature, which is 248: 188. Hence we take 160 uV/K as the Seebeck coefficient of Bi₂Te₃, and 122 as of Sb₂Te₃. We employ the cross section model in fig 2.1, considering the Joule heat of the contact resistance, and change the passivation layer to 1.1um Parylene with 0.2 W/(m*K), as in the processing.

Table 5.6: measured value of Seebeck coefficient and resistivity

Alpha_bite(uV/K)	160
Alpha_sbte(uV/K)	122
Rho_bite(Ohm*um)	24
Rho_sbte(Ohm*um)	67

The simulation result is shown in Fig 5.7

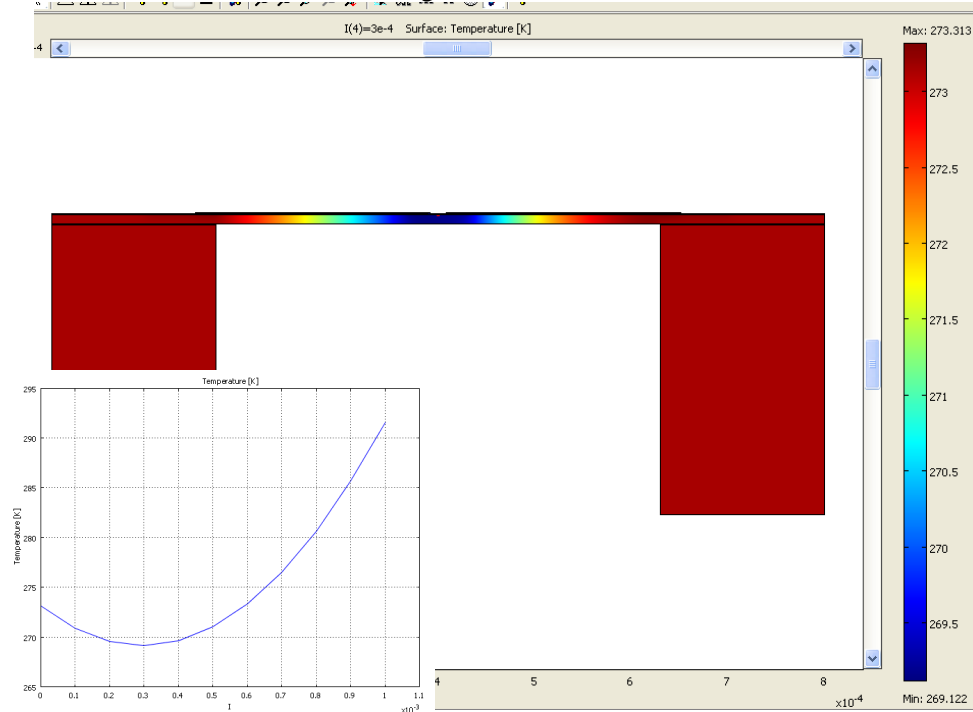


Fig 5.7 the simulation result of the model with all the parameters we got from the measurement

The minimum temperature is reached at an input current of 0.3mA, and the minimum temperature is 269.122K. The maximum temperature drop is only $\Delta T = 273.15K - 269.122K = 4.028K$. The initial results presented in chapter 2 showed a minimum temperature of 240.204K which corresponds to a temperature drop of 33K.

Clearly, the maximum temperature drop decreases significantly when we change the Seebeck coefficient and the resistivity of the thermoelectric material. This can be

understood when considering the equations for the maximum cooling temperature:

$\Delta T_{\max} = \frac{1}{2} Z T_c^2$ with $Z = \frac{(\alpha_1 - \alpha_2)^2}{KR}$, which indicate that the maximum cooling power is inversely related to the electrical conductance of the stack and quadratically with the Seebeck coefficient.

All the models we have simulated are in the condition of thermal isolation at the edge of the devices. However, the real measurements are performed in air, but not vacuum. The heat conduction through the air also affects the temperature difference due to Peltier cooling. Hence, we add 300um air under the cooling device and 200 um air on top of it, and simulate the model again to see the effect of the air conduction. The result is shown in fig 5.8.

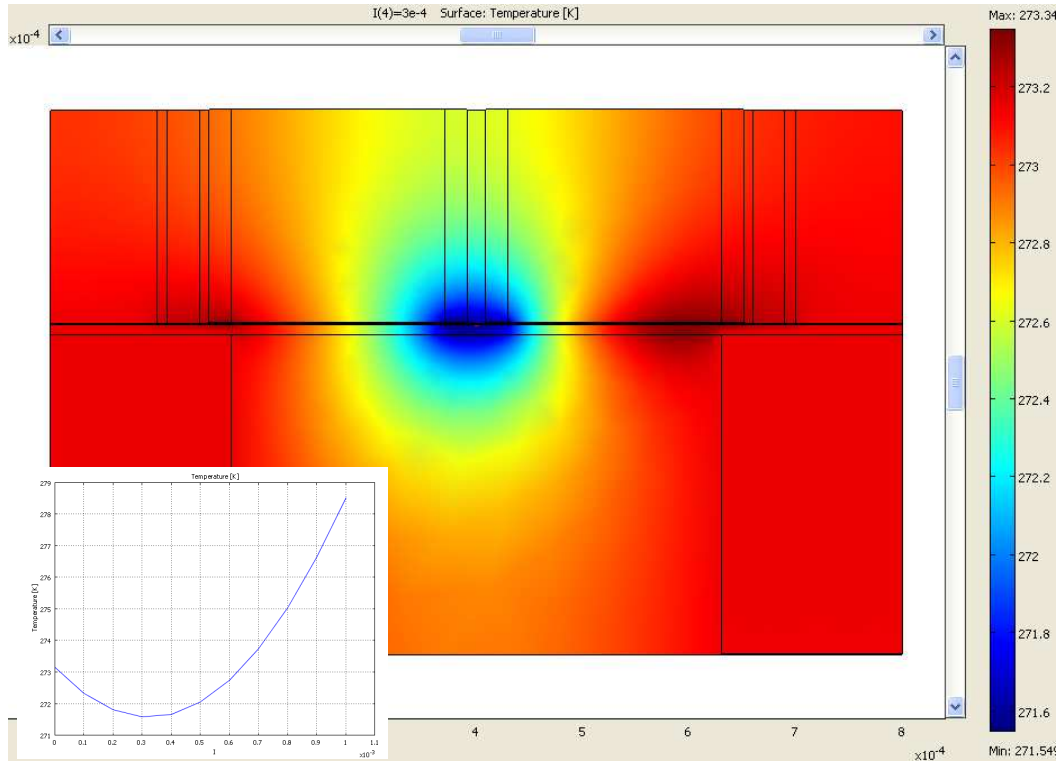


Fig 5.8 the simulation result of the model considering the heat conduction of air

The minimum temperature is 271.549K. The temperature drop decreases more when we take the air conduction into account. The maximum temperature drop is, $\Delta T = 273.15K - 271.549K = 1.6K$. The air consumes more than half of the temperature difference.

The maximum temperature drop we could get in the measurement is 3.3K, 0.7K and 0.75K, according to the measurement results, which is more or less the simulation result in Fig 5.8. The low Seebeck coefficient, the high resistance and the air heat conduction are the reasons for that the cooling temperature is not as much as we expected.

5.4 Conclusion

We have characterized the materials. The sheet resistance of Al is 0.2 Ohm, TiW 3.6 Ohm, Bi₂Te₃ 67 Ohm, Sb₂Te₃ 24Ohm. The contact resistivity of Bi₂Te₃ and Sb₂Te₃ to TiW vary much, and we take 7404 Ohm * um² for Bi₂Te₃ and 27977 Ohm * um² for Sb₂Te₃. The combined Seebeck coefficient is 282 uV/K. The cooling is measured on the probe station on the cross structures with a calculated cooling temperature 3.3K and 0.7K, and under the thermal camera with a cooling temperature of 0.75 K at 1V input. The device is simulated with COMSOL again with the measured value of the resistance and Seebeck coefficient, and the maximum cooling temperature is 4.028K, and 1.6K for the model considering the air conduction.

The low cooling effect is caused by thermal conduction through the air, the low Seebeck coefficient and the high resistivity.

Chapter 6 Conclusion

The Peltier effect describes that if we put two conductors together and make a junction, heat would be generated or absorbed at the junction depending on the polarity of the injecting current, which means that we could realize the heating and cooling function using the same device only by reversing the supply current. An on-chip cooling device based on Peltier effect is designed and fabricated in this project for the application of a CO₂ sensor. High figure of merit materials Bi₂Te₃ and Sb₂Te₃ are employed as the thermoelectric materials. However there are challenges to pattern and to fully cap the materials, and the adhesion of Bi₂Te₃ and Sb₂Te₃ to the substrate is a problem.

The thermal profile is first simulated using the software COMSOL, using the cross section model and the top view model, in order to gain insight in the design trade-offs of the cooling device and to decide the optimal dimension of the devices. According to the simulation result, a set of mask is designed in the software Cadence, including three sizes of devices, the test structures to determine the parameters of the material and to control the process, and the alignment markers.

Several preliminary experiments are performed to determine the best substrate material by the result of the adhesion test, in which test polyimide and silicon nitride gives nice adhesion, and to determine the etching method of Bi₂Te₃ and Sb₂Te₃. Much effort is paid to pattern the material. We discussed the shadow mask method, which is not feasible at last, and the dry etching method by Ion Beam Etcher, using photoresist, W or Si₃N₄ as hard mask, but the result is not satisfactory. Finally we decide to use wet etchant HCl: HNO₃: H₂O = 3:1:2 for Bi₂Te₃ and etchant HNO₃: H₂O = 1:1 for Sb₂Te₃, although the lateral undercut is 5 times the thickness of the etched layer, which is quite large.

Two types of processes are designed and processed in the cleanroom, one of which employs all polymer materials, which are polyimide substrate, photoresist intermediate layer, and parylene as passivation layer, and the other of which uses all Si₃N₄, including nitride substrate, nitride intermediate layer and nitride capping layer. Attention needs to be paid to Parylene, which is never used in similar devices before, and it is a polymer with low deposition temperature, excellent step coverage, and low thermal conductivity, which is very suitable to be applied in thermoelectric devices. During the processing, the structures tend to peel off in to the solvent, which means the adhesion and the capping are still problems. Fortunately we got 4 wafers with working devices eventually.

The devices are tested on the probe station and under the thermal camera. A maximum cooling temperature of 3.3K is observed. The problem is the thermal conduction of the air, the low Seebeck coefficient and the high resistance. Further research should focus on the thin film thermoelectric materials with improved Seebeck coefficient, electrical conductivity and contact.

The project is finished in Philips Research, Eindhoven.

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Appendix A

Shadow mask patterning

The shadow mask is the mask we put on the wafer while depositing. There are patterned holes on the shadow mask, and the material is only deposited at the position of the holes, as shown in Fig 1. The deposited structure is very smooth at the edge, allowing good step coverage for subsequent layers.

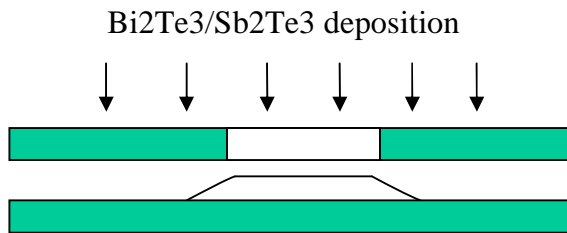


Fig 1 demonstration of the deposition with a shadow mask, resulting in patterned structures directly after deposition

Since we employ a six-inch silicon wafer in the process, it is logical to use another six-inch silicon wafer as the shadow mask to avoid thermal expansion effects. However, the thick wafer makes the viewing angle of the structure to the target small, causing thickness differences between the small and big structures, shown in Fig 2a. This problem could be solved by opening additional overlapping shallow holes where the structures are, improving the viewing angle, as shown in Fig 2b.

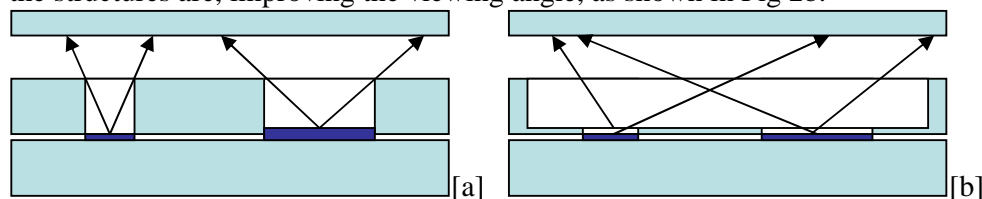


Fig 2a: the different viewing angles for the holes with different sizes on the shadow mask, causing non-uniformity, Fig 2b: the viewing angles are the same with thin shadow mask

We could first pattern the backside of the wafer, etch through the wafer with 2 steps of deep etch from the backside, and use the front side as the shadow mask. The detailed process is, as shown in Fig 3, (1), coating polyimide on the front side of a wafer with silicon oxide on both sides, and polyimide could support the wafer and release the stress during the Deep Si etch, (2), 1st patterning of photoresist, opening the oxide for the structures, (3), etch part of the silicon, (4), 2nd patterning for the big shallow holes, (5) etch through the wafer using Deep Si Etch, and the etching stops at

silicon oxide, (6), remove the polyimide, (7), remove the silicon oxide, (8), be clamped with the substrate as a shadow mask.

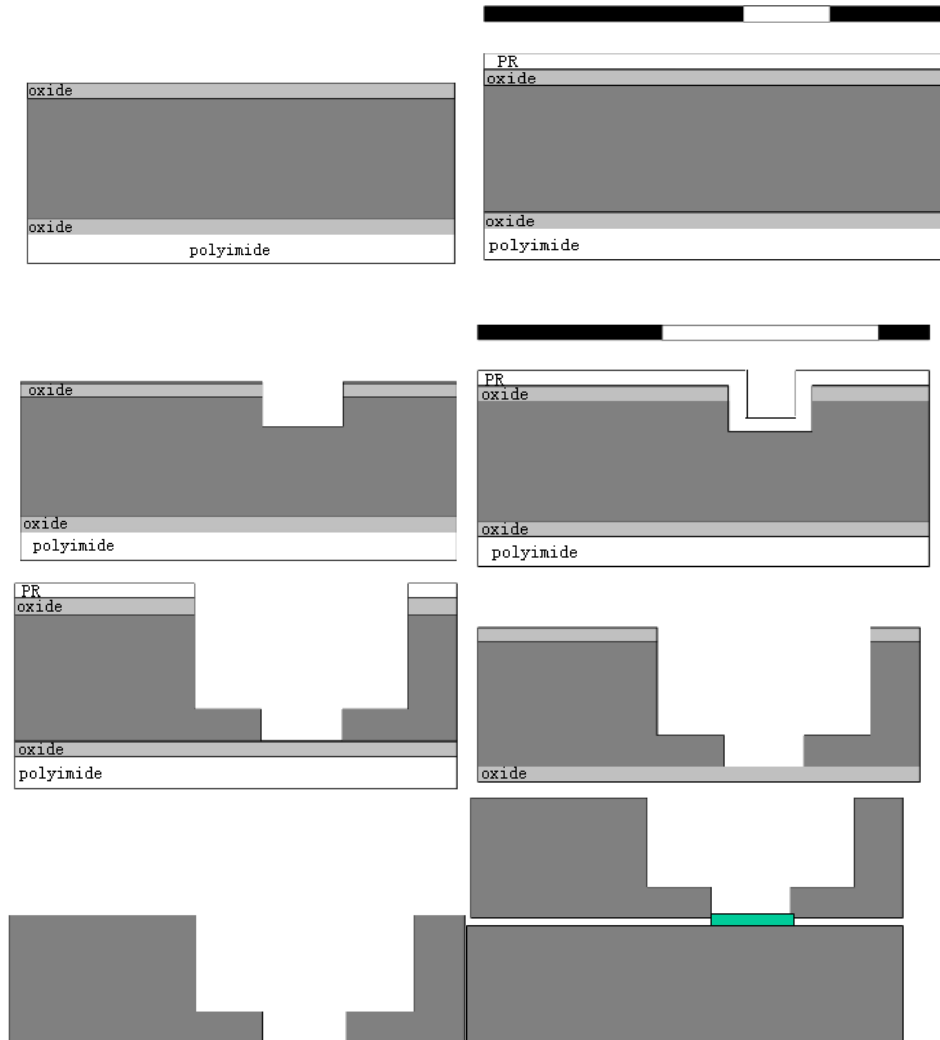


Fig 3 the demonstration of making a shadow mask

Another question of the shadow mask is how to align the shadow mask to the substrate, since the shadow mask is actually a wafer, and we could not use the normal marker alignment station for the alignment. The Bonder Aligner, which aligns two wafers precisely by the edge, could be used. Then we get two wafers clamped together, accurately aligned to etch other, and we glue the wafers together with the tape and transfer them to the deposition machine immediately.

Now we know the edges of the wafers are at the same position, but we are not sure if the alignment markers are also exactly at the same position. We need to introduce the laser markers. The position of the markers is set in the laser marker, and the strict position is found on the wafer, where a marker is written. Everything is aligned to this laser marker, and the position of everything is fixed. Then the edge of the wafers is aligned, meaning the structures are aligned, and the alignment problem is solved. There is still one detail to be settled, the sloping edge during the deep etching. The STS Deep Si Etcher gives quite sharp etching profile for the Si deep etching, with the sloping angle only 1 degree, but for the wafer thickness 670um, the lateral

displacement is $\Delta = 670\mu m * \tan(1^\circ) = 11\mu m$, each side, which means the smallest structures on the mask should be $2 * 11\mu m = 22\mu m$. If we employ the shadow mask as the patterning method, all the structures on the mask we designed in the last chapter should be rewritten and enlarged $11\mu m$ etch side to leave the lateral displacement in advance.

The deeper we discussed, the more problems the shadow mask method has. The sloping edge of the shadow mask makes it uncertain, since the real size of the opening on the mask is unknown, which makes the pattern imprecise. Also, how to clean the shadow mask completely after every time use also needs to be discussed. Hence we decide to move on to the traditional dry-etching and wet-etching method.

Appendix B

Flowcharts for patterning experiments

B-1 Flow chart for dry etching method with reflowed photoresist

The wafer is already deposited TiW and Bi₂Te₃ (or Sb₂Te₃) before the processing, and the substrate is polyimide.

- 1, Rinse in water: for adhesion.
- 2, Spincoat HPR 504: recipe 4000 - 1.3 um thick
- 3, Expose mask on contact aligner: 6.5 sec, hard contact
- 4, Develop photoresist on the ACS machine: HPR504 recipe
- 5, Reflow photoresist: 110 degreeC, 2 min**
- 6, Etch Bi₂Te₃ (or Sb₂Te₃): Ion beam Ester
Etch stop: signals of atoms
- 7, Strip photoresist: O₂ plasma.

B-2 Demonstration and the flow chart of dry etching with W hard mask

Demonstration	The flow chart
<div>Bi₂Te₃/Sb₂Te₃</div> <div>TiW</div> <div>PI</div> <div></div>	1, Bi ₂ Te ₃ / Sb ₂ Te ₃ deposition: 1 um
<div>W</div> <div>Bi₂Te₃/Sb₂Te₃</div> <div>TiW</div>	2, W mask deposition: sputter etch (20 sec) Tungsten deposition 150 nm
<div>PR</div> <div>W</div> <div>Bi₂Te₃/Sb₂Te₃</div> <div>TiW</div>	3, Photoresist patterning Rinse in water: for adhesion. Spincoat HPR 504: 4000rpm recipe - 1.3 um thick Expose mask on contact aligner: 6.5 sec, hard contact Develop photoresist on the ACS machine

W			4, Etch Tungsten: RIE
Bi ₂ Te ₃ /Sb ₂ Te ₃			+descum
TiW			Strip photoresist: acetone strip
W			5, Etch Bi ₂ Te ₃ (or Sb ₂ Te ₃): Ion beam Ester
Bi ₂ Te ₃		Sb ₂ Te ₃	Etch stop: signals of atoms
TiW			
Bi ₂ Te ₃		Sb ₂ Te ₃	6, Remove Tungsten mask: RIE
TiW			

B-3 Flow chart for dry etching with advanced W mask

- 1, Bi₂Te₃/ Sb₂Te₃ deposition: 1 μ m.
- 2, W mask deposition: sputter etch (20 sec) + Tungsten deposition 200 nm.
- 3, Bi₂Te₃ patterning
 - 1, Spincoat HPR 504: the 4000 recipe - 1.3 μ m thick
 - 2, Expose mask on contact aligner: 6.5 sec, hard contact
 - 3, Develop photoresist on the ACS machine: HPR504 recipe
 - 4, Reflow photoresist: 110 degreeC, 2 min
 - 5, Etch Tungsten: RIE, Tungsten recipe (*do NOT descum*)
+ *overetch*
 - 6, Strip photoresist: *acetone, bath*
 - 7, Rinse with water
 - 8, Etch Bi₂Te₃ (or Sb₂Te₃): Ion beam Ester
Etch stop: signals of atoms
 - 9, Remove Tungsten mask: RIE

B-4 Flow chart for dry etching with silicon nitride hard mask

We start with a wafer with SiO₂ on both sides. The flow chart for dry etching the thermoelectric materials with silicon nitride hard mask is as follows.

- 1, TiW deposition and patterning
- 2, Sb₂Te₃ deposition: sputter etch + 1 μ m Sb₂Te₃
- 3, Sb₂Te₃ patterning
 - 1, 100nm Si₃N₄@250 degreeC
 - 2, TCPS primer
 - 3, HPR504, recipe 4000
 - 4, Expose mask BITE, 6.5 sec, hard contact
 - 5, Develop photoresist in the bath
 - 6, Etching SiN: STS cluster

- 7, Strip resist: O₂ plasma 5min, 120 degreeC, acetone no useful
- 8, Etch Sb₂Te₃: Ion Beam Ester
- 4, 100nm SiN @ 250 degreeC, and opening the windows
- 5, Bi₂Te₃ deposition: sputter etch + 1um Sb₂Te₃
- 6, Bi₂Te₃ patterning:
 - 1, 100nm Si₃N₄@250 degreeC
 - 2, TCPS primer
 - 3, HPR504, recipe 2000
 - 4, Expose mask SBTE, 8.5 sec, hard contact
 - 5, Develop photoresist in the bath
 - 6, Etching SiN: STS cluster
 - 7, Strip resist: O₂ plasma 5min, 120 degreeC
 - 8, Etch Bi₂Te₃: Ion Beam Ester

B-5 Process flow for the wet etching

Three wafers with polyimide as substrate are taken for the wet etching experiment. TiW, Bi₂Te₃ and Sb₂Te₃ are deposited on the wafers separately, and the TiW is only used for comparing. The photoresist is coated on the wafers and patterned, and each wafer is cut into 20 pieces. The flow chart for wet etching wafers is as follows.

- 1, Rinse in water
- 2, Standard photoresist: spin coat photoresist HPR 504, recipe: 4000rpm
- 4, Expose mask on contact aligner
 - 6.5 sec , hard contact mode
- 5, Develop photoresist on ACS machine
- 6, Hard bake photoresist, 120 degree C, 2 min
- 7, Etch in Etchant
 - Etchant A: Al Etch A, etch stop: time stop, or bubble stop
 - Etchant B: Diluted Aqua Regia, etch stop: bubble stop
 - Etchant C: diluted HNO₃
 - Etchant D: H₂O₂-HCl
 - + 10% over etch
- 8, Strip photoresist: acetone strip

Appendix C

Wet etching of TiW

The wet etching experiment for W mask is conducted as a separate experiment with small pieces. To make sure that Bi_2Te_3 and Sb_2Te_3 would not be etched when we strip the W mask, small wafer pieces with Bi_2Te_3 , Sb_2Te_3 and TiW layer are put in the etchant together.

The wet etchant for TiW is H_2O_2 : NH_4OH : H_2O = 1:1:1. The etching result is listed in the following table. Bi_2Te_3 does not react with the etchant, but Sb_2Te_3 does, so only the W mask with Bi_2Te_3 could be stripped with the wet etchant.

Table: etching TiW, Bi_2Te_3 and Sb_2Te_3 in wet TiW etchant

Etchant for TiW, H_2O_2 : NH_4OH : H_2O = 1:1:1		
Etched material	Etching time	Result
TiW	2'41''	Photoresist comes off
	7'	Clear
Bi_2Te_3	15'	Nothing
Sb_2Te_3	15'	Surface becomes white and rough

Appendix D

Final flow charts

D-1 Initial flow chart for process the wafer

	For nitride wafers	For polymer wafers
1	Polyimide deposition	Polyimide deposition
	1, Clean the wafers: SSEC recipe: 150mm_SPM+Meg+DI 2, Spin Primer: VM652 primer open 10s@500+close 45@3000rpm 3, Spin polyimide: A115 polyimide open 15s@300+close 45s@1000 + close 2s@4000 rpm 4, Bake on hotplate, 120 C, 6min 5, Cure polyimide	1, Clean the wafers: SSEC recipe: 150mm_SPM+Meg+DI 2, Spin Primer: VM652 primer open 10s@500+close 45@3000rpm 3, Spin polyimide: A115 polyimide open 15s@300+close 45s@1000 + close 2s@4000 rpm 4, Bake on hotplate, 120 C, 6min 5, Cure polyimide
2	Deposit SiN	
	300nm @ 300 degreeC	
3	Deposit TiW 11-4	Deposit TiW *
	200nm	200nm [1]
4	TiW patterning	TiW patterning, dry etching
	1, HPR504, recipe 4000 2, Expose mask TiW 6.5 sec, hard contact 3, Develop HPR504, ACS 4, Hard bake, 2min, 120 degreeC 5, Wet Etching of TiW [2] NH ₄ OH: H ₂ O ₂ : H ₂ O =1:1:1 6, Strip resist: acetone	1, HPR504, recipe 4000 2, Expose mask TiW 6.5 sec, hard contact 3, Develop HPR504, ACS 4, Dry Etching of TiW, STS cluster Descum+RIE+Descum [2] 5, Strip resist: acetone
5	Bi₂Te₃ deposition, 1um	Bi₂Te₃ deposition, 1um
	1. Pre-bake: 150 degree C, 5min. [A] 2. Co-sputtering Bi ₂ Te ₃ , 1 um Sputter Etch a little + deposition [A]	1. Pre-bake: 150 degree C, 5min. [A] 2. Co-sputtering Bi ₂ Te ₃ , 1 um Sputter Etch a little + deposition [A]

6	Pattern Bi₂Te₃ 1, HPR504, recipe 4000 2, Expose mask BiTe 6.5 sec, hard contact 3, Develop photoresist in the bath 4, Hard bake, 2min, 120 degreeC 5, Wet etching [3] HCl: HNO ₃ : H ₂ O =3:1:2 6, Strip resist: acetone	Pattern Bi₂Te₃ 1, HPR504, recipe 4000 2, Expose mask BiTe 6.5 sec, hard contact 3, Develop photoresist in the bath 4, Hard bake, 2min, 120 degreeC 5, Wet etching[3] HCl: HNO ₃ : H ₂ O =3:1:2 6, Strip resist: acetone
7	Intermediate SiN 1. Pre-bake: 150 degree C, 5min. 2, 100nm SiN@250 degreeC [B] 3, TCPS primer 4, HPR504, recipe 2000 5, Expose mask CO 8sec, hard contact 6, Develop photoresist in the bath 7, opening pads: STS cluster 8, Strip resist: acetone 9, Remove primer: developer [4]	Intermediate PR 1. Pre-bake: 150 degree C, 5min. 2, HPR504, recipe 2000 3, Expose mask CO 8sec, hard contact 4, Develop photoresist in the bath
8	SbTe deposition, 1um 1. Pre-bake: 150 degree C, 5min. [A] 2. Co-sputtering SbTe, 1 um Sputter Etch a little + deposition [A]	SbTe deposition, 1um 1. Pre-bake: 120 degree C, 5min. [A] 2. Co-sputtering SbTe, 1 um Sputter Etch a little + deposition [A]
9	Pattern Sb₂Te₃ 1, HPR504, 2000rpm 2, Expose mask SbTe 8.5sec, hard contact 3, Develop photoresist in the bath 4, Hard bake: 120 degreeC, 2min 5, Wet etching [5] HNO ₃ : H ₂ O =1:1, dip in water 6, Strip resist: acetone	Pattern Sb₂Te₃ 1, HPR504, recipe 2000 2, Expose mask SbTe 8.5sec, hard contact 3, Develop photoresist in the bath 4, Hard bake: 120 degreeC, 2min 5, Wet etching [5] HNO ₃ : H ₂ O =1:1, dip in water 6, Strip resist: acetone [6]
10	Coat SiN and SiO₂ 1, 100nm SiN@250 degreeC 2, 500nm SiO ₂ @300 degreeC	Coat Parylene, 1um 1, Parylene primer 2, Coat Parylene, 1um
11	Open Contact 1, TCPS primer 2, HPR504, recipe 2000 3, Expose mask CB 8.5sec, hard contact	Open Contact 1, HPR504, recipe 2000 2, Expose mask CB 8.5sec, hard contact 3, Develop photoresist in the bath

	4, develop photoresist in the bath 5, Etch SiO ₂ : STS cluster 6, Etch SiN: STS cluster 7, Strip resist: acetone 8, Remove primer: acetone	4, Etch parylene: Applied 5000 5, strip resist: acetone
12	Al sputtering, 1um	Al sputtering, 1um
	1, Soft sputteretch [C] 2, Al sputtering: 1um	1, Soft sputteretch [C] 2, Al sputtering: 1um
13	Al patterning	Al patterning
	1, HPR504, recipe 2000 2, Expose mask IN 8.5sec, hard contact 3, Develop photoresist in the bath [7] 4, hard bake: 90 degreeC, 2min 5, Wet etching Al: PES@30degree 105nm/min +10% overetch 12-20 6, Strip resist: acetone	1, HPR504, recipe 2000 2, Expose mask IN 8.5sec, hard contact 3, Develop photoresist in the bath 4, hard bake: 90 degreeC, 2min 5, Wet etching Al: PES@30degree 105nm/min +10% overetch 1-7 6, Strip resist: acetone
14	Back etching	Back etching
	1, Spray AZ9260, 1250rpm 2, bake: 90degreeC, 5min 3, Expose mask MESA 40 sec, hard contact 4, Develop: AZ400K, 1-3, 5min 5, hardbake, 1h, 90degreeC 6, descum, 600W, 5min 7, SiO ₂ opening: Applied 5000 8, STS Deep Si Etch 9, Strip resist: acetone	1, remove back side parylene[8] 1, cover front side, HPR504,1000[9] 2, hardbake, 90degreeC, 1h 3, Spray AZ9260, 1250rpm 4, bake: 90degreeC, 5min 5, Expose mask MESA 40 sec, hard contact 6, Develop: AZ400K, 1-3, 5min 7, hardbake, 1h, 90degreeC[10] 8, descum, 600W, 5min 9, SiO ₂ opening: Applied 5000 10, STS Deep Si Etch 11, Strip resist: acetone

D-2 Final flow charts

Final flow chart for the wafers with nitride substrate, nitride intermediate layer, and nitride passivation layer and the wafers with polyimide substrate, photoresist intermediate layer and Parylene passivation layer

	wafers with Si_3N_4	wafers with SiO_2
1	Polyimide deposition	
	1, Clean the wafers: SSEC recipe: 150mm_SPM+Meg+DI 2, Spin Primer: VM652 primer open 10s@500+close 45@3000rpm 3, Spin polyimide: A115 polyimide open 15s@300+close 45s@1000+ close 2s@4000 rpm 4, Bake on hotplate, 120 C, 6min 5, Cure polyimide	
2	Deposit SiN, 300nm	none
	300nm@300 degreeC	
3	Deposit TiW, 250nm	
	250nm	
4	TiW patterning	
	1, HPR504, recipe 4000 2, Expose mask TiW, 6.5 sec, hard contact 3, Develop HPR504, ACS 4, Hard bake, 2min, 120 degreeC 5, Wet Etching of TiW, NH_4OH : H_2O_2 : H_2O =1:1:1 6, Strip resist: acetone	
5	Bi_2Te_3 deposition, 1um	
	1. Pre-bake: 150 degree C, 5min. 2. Co-sputtering Bi_2Te_3 , 1 um Sputter Etch a little + deposition	
6	Pattern Bi_2Te_3	
	1, HPR504, recipe 4000 2, Expose mask BiTe 6.5 sec, hard contact 3, Develop photoresist in the bath 4, Hard bake, 2min, 120 degreeC 5, Wet etching, HCl : HNO_3 : H_2O =3:1:2 6, Strip resist: acetone	
7	Intermediate 100nm SiN+500nm	Intermediate PR, 2000rpm

	SiO₂	
	1, 100nm SiN@250 degreeC 2, 500nm SiO ₂ @300 degreeC 3, TCPS primer 4, HPR504, recipe 2000 5, Expose mask CO 8.5sec, hard contact 6, Develop photoresist in the bath 7, opening pads: STS cluster 8, Strip resist: acetone 9, Remove primer: O ₂ plasma	1. Pre-bake: 150 degree C, 5min. 2, HPR504, recipe 2000 3, Expose mask CO 8sec, hard contact 4, Develop photoresist in the bath
8	SbTe deposition, 1um	
	1. Pre-bake: 150 degree C, 5min. 2. Co-sputtering SbTe, 1 um Sputter Etch a little + deposition	
9	Pattern Sb₂Te₃	Pattern Sb₂Te₃
	1, HPR504, 2000rpm, manual 2, Expose mask SbTe 8.5sec, hard contact 3, Develop photoresist in the bath 4, Hard bake: 120 degreeC, 2min 5, Wet etching HNO ₃ : H ₂ O =1:1, dip in water 6, Strip resist: acetone	1, HPR504, recipe 2000 2, Expose mask SbTe 8.5 sec, hard contact 3, Develop photoresist in the bath 4, Hard bake, 2min, 120 degreeC 5, Wet etching HNO ₃ : H ₂ O =1:1, dip in water 6, Strip resist: O ₂ plasma@90degree, 110min
10	Deposit 100nm SiN +500nm SiO₂	Coat Parylene, 1um
	1, 100nm SiN@250 degreeC 2, 500nm SiO ₂ @300 degreeC	1, Parylene primer 2, Coat Parylene, 1um
11	Open Contact	Open Contact
	1, TCPS primer 2, HPR504, recipe 2000 3, Expose mask CB 8.5sec, hard contact 4, develop photoresist in the bath 5, Etch SiO ₂ : STS cluster 6, Etch SiN: STS cluster 7, Etch SiO ₂ : STS cluster 8, Etch SiN: STS cluster 9, Strip resist: O ₂ plasma 5min @ 120 degreeC	1, HPR504, recipe 2000 2, Expose mask CB 8.5sec, hard contact 3, Develop photoresist in the bath 4, Etch parylene: Applied 5000 5, strip resist: acetone
12	Al sputtering, 1um	Al sputtering, 1um
	1, Soft sputteretch	1, Soft sputteretch

	2, Al sputtering: 1um	2, Al sputtering: 1um, low power
13	Al patterning	
	1, HPR504, recipe 2000 2, Expose mask IN 8.5sec, hard contact 3, Develop photoresist in the bath 4, hard bake: 90 degreeC, 2min 5, Wet etching Al: PES@30degree,105nm/min +10% overetc 6, Strip resist: acetone	
14	Back etching	
	1, cover front side, HPR504@1000 2, hardbake, 90degreeC, 1h 3, Spray AZ9260, 1250rpm 4, bake: 90degreeC, 5min 5, Expose mask MESA, 40 sec, hard contact 6, Develop: AZ400K, 1:3, 5min 7, hardbake, 1h, 90degreeC 8, strip HPR504, ACS 9, descum, 600W, 5min 10, SiO ₂ opening, Applied 5000 11, STS Deep Si Etch 12, Strip resist: acetone	

