A CMOS Bandgap Temperature sensor for Cryogenic Applications

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Abstract

Cryogenic temperature sensors are finding broadened applications. Such applications include: Cryosurgery [1.3], quantum computing, deep-space probes and planetary missions, satellite communications systems and space-based radar, ultra-high-speed/high sensitivity instrumentation systems, medical electronics (e.g. CT scanner), superconductor-semiconductor hybrids [1.4], very low-noise receivers (radio astronomy), cooled IR detector arrays etc [1.4].

Temperature sensors that operate at cryogenic temperatures are commercially available. Such sensors include: Platinum resistance sensors, diodes, thermocouples et c. These sensors can achieve high accuracy (better than 0.1 K) but at the cost of expensive calibration. The analog nature of these sensors, means they are prone to interference, which can considerably perturb the measuring result. Those disadvantages can be overcome by CMOS integrated cryogenic temperature sensors.

This thesis presents a CMOS bandgap based temperature sensor that is fully operational at cryogenic temperatures (77 K). The sensor was fabricated in CMOS 0.16 μm technology and achieves a temperature inaccuracy of ±0.25°C within the temperature range of −65 °C to 30 °C and an inaccuracy of ±0.15°C at 77K.
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1

Introduction

1.1 Operating Temperature Ranges for Electronic Devices

The proper operation of electronic devices is usually ensured within standard operating temperature ranges. Three main temperature ranges can be defined. Devices that operate in the military temperature range from $-55^\circ C$ to $+125^\circ C$ are called Normal Temperature Electronics (NTE). Most electronic devices used in everyday applications operate in this temperature range. Electronic devices can also be designed to operate at temperatures higher or lower than the military temperature range. Those that operate higher than the military temperature range typically up to $200^\circ C$, are called High Temperature Electronics (HTE) while those that operate below the military temperature range, even down to absolute zero ($-273^\circ C$) are called Low Temperature Electronics (LTE). Both High and Low temperature Electronics are referred to as Extreme Temperature Electronics. Figure 1 gives a diagrammatic explanation of these temperature ranges [1.1].

![Extreme Temperature Electronics Diagram]

- Normal-Temperature Electronics (NTE) = “military range” = $-55^\circ C$ to $+125^\circ C$
- Low-Temperature Electronics (LTE) = $< -55^\circ C$ to absolute 0 ($-273^\circ C$)
- High-Temperature Electronics (HTE) = $> +125^\circ C$, especially $> 200^\circ C$
- Wide-Temperature Electronics (WTE) = from below $-55^\circ C$ to above $+125^\circ C$

*Figure 1 Temperature range of operation for electronic devices [1.1].
1.2 What is Cryogenics?

Cryogenics basically involve reaching very low temperature and studying how materials and devices behave at these temperatures. Cryogenic temperatures are generally taken to include temperatures from $-150^\circ C$ down to absolute zero ($-273^\circ C$). At these temperatures property changes occur to most materials. For example, some metals become superconductive as they lose all their resistance and retain currents flowing in them even after power has been cut off. These changes in the properties of materials at cryogenic temperatures give cryogenics its importance. One of the motivation for operating electronics at cryogenic temperatures is performance improvements. Some desirable performances, such as gain and speed increase at low temperatures, while other undesirable ones, such as noise, leakage and parasitic capacitances decrease with temperature.

1.3 The need for CMOS based cryogenic temperature sensors

Techniques for temperature sensing which provides readouts at cryogenic temperatures are finding broadened applications in the scientific sphere. A good example of such an application is cryosurgery. Cryosurgery is a minimally invasive surgical technique which involves the use of extreme cold to destroy abnormal or diseased tissues [1.2]. An important criteria for cryosurgery success is the accurate measurement of the local cooling and rewarming rates of the affected area so as to prevent cryoinjury. Data of real-time temperature distribution of the affected area needs to be known. Current practices involve the use of discrete temperature sensors implanted at the tips of the cryoprobes [1.3]. These sensors are inconvenient and inefficient as they do not provide sufficient information to construct the local temperature distribution of the affected area [1.3]. Therefore, smart integrated temperature sensors are needed to tackle this problem.

Another major application for CMOS based cryogenic temperature sensors is quantum computing. Quantum computers typically need to run at temperatures close to absolute zero. This is because thermal fluctuations degrades quantum states. Therefore, quantum computing systems are cooled down to temperatures close to absolute zero (around $-269^\circ C$) to combat the quantum bits natural tendency to decay [1.5]. If quantum computers will eventually replace the existing digital electronic computers, then smart IC based temperature sensors are needed for good thermal control of the quantum computing system.

Other low temperature electronics applications include: deep-space probes and planetary missions, satellite communications systems and space-based radar, ultra-high-speed/high sensitivity instrumentation systems, medical electronics (e.g. CT scanner), superconductor-
semiconductor hybrids [1.4], very low-noise receivers (radio astronomy), cooled IR detector arrays etc [1.4].

Temperature sensors that operate at cryogenic temperatures are available commercially. Such temperature sensors include: Platinum resistors based temperature sensors, silicon diode temperature sensors, and thermocouples. Those sensors can achieve high accuracy (better than 0.1 K) but at the cost of expensive calibration. Moreover, due to the analog nature of these sensors, the leads between the sensor and the read-out circuitry are prone to interference, which can considerably perturb the measuring result. Those disadvantages can be overcome by CMOS integrated cryogenic temperature sensors. CMOS based temperature sensors have been in existence for a long time. However, existing CMOS IC based temperature sensors are designed to operate in the military temperature range. Temperature sensors fabricated in IC technology can be combined with interface circuits on a single chip [1.6]. Therefore, they are referred to as smart temperature sensors. Smart sensors have inherent advantages over conventional sensors: they can be assessed directly by a microcomputer in a standardized digital format, thus reducing the complexity and increasing the modularity of the system in which they are applied [1.6]. Moreover, the local processing of the sensor signal (amplification, analog-to-digital conversion) makes the measurement more robust to interference [1.7].

![Block diagram of integrated smart temperature sensor](image-url)

*Figure 2* Block diagram of integrated smart temperature sensor [1.6]
1.4 Objectives

Smart temperature sensors based on bipolar transistors have shown accuracy better than 0.1°C over the military temperature range after only a single-point room-temperature calibration, thanks to is reproducibility of bipolar transistor’s characteristics [1.8]. Also, bipolar based temperature sensors are completely compatible with CMOS technology. Therefore, if smart integrated cryogenic temperature sensors are to be built, bipolar based temperature sensors are a good option. In this project, the aim is to design a bipolar based temperature sensor that is fully operational at cryogenic temperatures. The objective is designing and characterizing this temperature sensor down to at least the temperature of liquid nitrogen (77 K).

1.5 Challenges

The design of an integrated circuit for operation at cryogenic temperatures involves several challenges. An important issue involved in this design is the unavailability of device models at cryogenic temperatures. Available models for the chosen technology (CMOS 0.16 μm) are limited to the military range of -55 °C to 125 °C. Therefore, a large part of this work is based on data from existing literature. Another challenge is that most devices exhibit different behaviours (if they function at all) when they are operated at cryogenic temperatures than when they are operated in the temperature range from -55 °C to 125 °C. Several properties of MOS and BJT devices change at these temperatures and must be taken into account in the design. The characterization of this temperature sensor after fabrication also poses another challenge, because reaching cryogenic temperature is not possible with the standard setup used for characterization of standard CMOS temperature sensors. Thus, this work requires the design and realization of custom made measurement test set-up.

1.6 Organization of the thesis

This section gives an overview of the organization of this thesis. Chapter 2 gives a review of the existing cryogenic temperature sensors. Also, an insight into behaviour of silicon and silicon devices (MOS and bipolar junction transistors) at cryogenic temperatures is given. Important properties of these devices that change at cryogenic temperatures and how they could affect our design choices are highlighted. Chapter 3 gives a detailed explanation of the circuit design and considerations. Various design choices and the reasoning behind such choices are explained. Precision techniques employed in the design such as chopping, dynamic element matching and current gain compensation and the impact they have on the circuit performance are all explained. Simulation results demonstrating the sensor functionality are also reported.
Chapter 5 gives an overview of the measurement set-up used for the characterization of fabricated sensors and the achieved results.

This thesis ends with Chapter 5 which gives the main conclusions of this work. Recommendations for further improvements of this work are also given in this chapter.

1.7 References


2

Cryogenic temperature sensors and Silicon device behaviour at cryogenic temperatures

In this chapter an overview of state-of-the-art cryogenic temperature sensors is given. Their characteristics in terms of operating temperature range, sensitivity, and accuracy is presented. Also, the behaviour of silicon and silicon devices (transistors) at cryogenic temperatures is explored by looking at the effect of low temperatures on metal-oxide-semiconductor (MOS) and bipolar junction transistors (BJT) and how this affects their electrical performance.

2.1 Cryogenic Temperature Sensors

Cryogenic temperature sensors have been in existence for a long time. A lot of the commonly used temperature sensors in the military temperature range are also applied at cryogenic temperatures e.g. thermocouples, platinum RTD’s, silicon diodes and special thermistors. In the following sections, an exploration of the state-of-the-art cryogenic temperature sensors is carried out.

2.1.1 Metallic Resistance Thermometry

Metallic resistance temperature sensors are based on the temperature dependent characteristic of the resistivity of metals. In general, metallic resistance temperature sensors have positive temperature coefficient (PTC) i.e. the electrical resistance of the constituent metal increases approximately with absolute temperature. Most metallic resistance based temperature sensors exhibit this linear temperature coefficient down to about 20 K below which their resistance becomes temperature independent and therefore can no longer be used to determine their temperature.
Two types of metallic resistance temperature sensors are commonly used in the cryogenic temperature range. They are platinum resistance thermometers and Rhodium-Iron resistance thermometers. An overview of these two temperature sensors is given in the following sections.

1. **Platinum resistance temperature sensors**

   Platinum resistance temperature sensors are an excellent choice for temperature sensing over a wide temperature span from 30 K to 873 K (-243 °C to 600 °C) [2.24]. Over this temperature range, platinum resistance temperature sensors provide high repeatability and a nearly constant sensitivity (dR/dT) [2.24].

   ![Figure 3 Typical resistance characteristic curve of a platinum temperature sensor (PT-100) [2.24]](image)

   ![Figure 4 Sensitivity of the above platinum temperature sensor (PT-100) [2.24] [2.15]](image)
Figure 3 shows a typical characteristic curve of a platinum based temperature sensor (PT-100) manufactured by Lakeshore Cryotronics Inc. [2.24]. This particular sensor was characterized down to 70 K. Platinum resistance temperature sensors that show a much more linear resistance than the one shown down to 14 K are available commercially. Platinum resistance temperature sensors typically show good matching from batch to batch, therefore more than one sensor can be combined to within $\pm 0.1 \, K$ accuracy of one other [2.24]. Below 20 K their sensitivity drops drastically because the platinum resistance becomes non-linear. Platinum resistance sensors are relatively inexpensive and require simple instrumentation.

2. Rhodium-Iron resistance temperature sensors

Rhodium-Iron (Rh-Fe) resistance temperature sensors are made from an alloy of Rhodium and Iron (Rhodium – 0.5% iron) [2.16]. They operate over a wide temperature range and even down to deep cryogenic temperatures (1.4 K– 500 K) [2.17]. They have a positive temperature coefficient and monotonic response over a wide temperature span [2.16]. They are stable to within a few tenth of a millikelvin with respect to time and thermal cycling [2.16]. They have a higher voltage sensitivity than platinum sensors below 20 K. Rhodium-Iron resistance temperature sensors are available commercially in configurations similar to platinum resistance temperature sensors. Their main disadvantage is the lack of uniformity of their resistance over batch to batch production [2.15] [2.16].

2.1.2 Non-metallic Resistance Thermometry

Certain semiconductors show good thermometric characteristics at low temperatures. In general, a semiconductor has less electrical conductivity than a metallic conductor but much higher than a typical insulator. Therefore, the resistivity of a semiconductor is usually several orders of magnitude larger than a metal conductor. Consequently, semiconductor resistance temperature sensors are usually short and have a large cross-sectional area so that their resistance is not too large [2.16]. The sensitivity $(1/R)(dR/dT)$ of a semiconductor resistance temperature sensor in its useful temperature range is usually larger than that of a metal of a metal resistance temperature sensor. Also, Semiconductor resistance temperature sensors have a negative temperature coefficient (NTC) [2.16]. Commercially available semiconductor resistance temperature sensors include germanium, carbon, carbon-glass, Ruthernium Oxide and Cernox™ temperature sensors.
1. Germanium temperature sensors

Germanium resistance temperature sensors (RTDs) have the highest accuracy, reproducibility, and sensitivity in the temperature range of 0.05 K to 100 K [2.17]. Germanium and Ruthenium Oxide are the only two cryogenic temperature sensors that can be used below 100 mK [2.17]. The resistance of germanium increases rapidly as temperature decreases. Figure 5 shows the temperature behaviour of some typical germanium temperature sensors [2.15].

![Figure 5 Typical resistance characteristic curve of germanium temperature sensors [2.18]](image)

Between 100 K and 300 K, the sensitivity dR/dT changes sign and dR/dT above 100 K is very small [2.18]. The sensor resistance varies from several ohms at its upper useful temperature to
several tens of kilohms at its lower temperature. Because device sensitivity increases rapidly with decreasing temperature, a high degree of resolution is achieved at lower temperatures, making these resistors very useful for sub-millikelvin control at 4.2 K and below. Germanium resistance temperature sensors have excellent stability, and ±0.5 mK reproducibility at 4.2 K [2.18]. The germanium resistor is usually the best choice for high-accuracy below 30 K [2.18].

They have a very small thermal time constant (about 200 ms at 4.2 K) because of their small mass. The operating temperature range of germanium temperature depends on the doping of the germanium used in such sensor [2.15].

2. Carbon resistance temperature sensors

Carbon resistance temperature sensors operate over the temperature range of 1 K to 100 K [2.15]. Their resistance increases exponentially with decreasing temperatures and have a high sensitivity at low temperatures. Their characteristics are however less reproducible than metallic resistance sensors and can have up to 2% change in resistance after every thermal cycle. Therefore, these sensors require a recalibration after every thermal cycle [2.15]. They are mostly used because of their low cost compared to other sensors [2.16]. They have a very fast thermal response (typically about 10 ms at 4.2 K) because of their small mass [2.15].

3. Ruthenium Oxide temperature sensors

Ruthenium oxide temperature sensors are thick film resistors. These composite sensors consist of bismuth ruthenate, ruthenium oxides, binders, and other compounds that allow them to obtain the necessary temperature and resistance characteristics [2.19].

![Figure 7 Typical resistance characteristic curve of Ruthenium Oxide temperature sensors [2.19]](image-url)
Figure 8  Sensitivity of the above Ruthenium Oxide temperature sensors [2.19]

Ruthenium Oxide temperature sensors are useful down to 10 mK. Most ruthenium oxide sensors have a maximum useful temperature limit well below room temperature, where the sensitivity changes from negative to positive [2.19]. They can be designed to have a monotonic characteristic from 10 mK to 300K. Along with Germanium temperature sensors, they are the only cryogenic temperature sensors that can be used below 100 mK [2.19].

4. Cernox™ resistance (Zirconium Oxy-Nitride) temperature sensors

Cernox™ temperature sensors can be used from 100 mK to 420 K with good sensitivity over the whole range [2.20]. Their temperature-sensing element is fabricated from zirconium reactively sputtered in a nitrogen-oxygen atmosphere which result in a thin film comprised of conducting zirconium nitride embedded within a zirconium oxide non-conducting matrix [2.21]. The resistance of the resulting material has a negative temperature coefficient making it useful as a temperature sensor. The ratio of conducting to non-conducting material can be adjusted to a given temperature range [2.21]. Cernox™ thin film resistance cryogenic temperature sensors have significant advantages over comparable bulk or thick film resistance sensors. They have high sensitivity, excellent short-term and long-term stability, small physical size, and a fast thermal response [2.20] [2.21]. They are easily mounted in packages designed for excellent heat transfer, yielding a characteristic thermal response time much faster than possible with bulk devices requiring strain-free mounting. Additionally, they have been proven very stable over repeated thermal cycling [2.20].
2.1.3 Diode Thermometry

The principle of diode thermometry is based on the temperature dependence of the forward voltage drop in a p-n junction which is biased at a constant current, typically 10 µA. Typically this voltage signal is relatively large, between 0.1 V and 6 V, making diodes easy to use with simple instrumentation. Commercially two types of diode temperature sensors are available: silicon diode and Gallium Aluminium Arsenide diodes. Commercially available diode
temperature sensors can operate within the temperature range of 1.4 K to 500 K [2.22]. Diodes are the most widely used cryogenic temperature sensors because they are highly stable and reproducible. Diode temperature sensors are better than most resistance temperature sensors for most practical applications [2.16]. Diodes are more sensitive and more nearly linear over useful temperature range than carbon, germanium and platinum resistance temperature sensors [2.16]. Their major advantage is that they maintain their resolution over a wide temperature range [2.16].

![Graph of voltage vs temperature for a silicon diode temperature sensor.](image1)

*Figure 11 Typical voltage characteristic curve of a silicon diode temperature sensor [2.22]*

![Graph of sensitivity vs temperature for the same sensor.](image2)

*Figure 12 Sensitivity of the above silicon diode temperature sensor [2.22]*
As seen from Figure 12, silicon diodes maintain a linear sensitivity at temperatures above 20 K while their sensitivity increases below 20 K. Gallium Aluminium Arsenide show a monotonic temperature response over their useful temperature range (1.4 K to 500 K) and have a high sensitivity below 50 K [2.23].

2.1.4 CMOS bandgap Temperature sensor

A CMOS based bandgap temperature sensors that was operational at cryogenic temperatures was demonstrated in [2.25]. The basic principles of operation of a CMOS bandgap temperature sensor is shown in Figure 13 and Figure 14.

![Figure 13 Operating principle of BJT temperature sensor [2.26]](image1)

Two diode-connected bipolar transistors are biased with a current ratio of 1: p to generate a $\Delta V_{BE}$ voltage as shown in Figure 13. The operational amplifier is used to create negative feedback to generate the $\Delta V_{BE}$ voltage. A second transistor can then be biased to generate the emitter-base voltage. The emitter-base voltage of diode-connected bipolar transistor is given as

![Figure 14 Temperature dependency of important voltages [2.26]](image2)
\[ V_{BE} = V_T \left( \exp \left( \frac{l_C}{l_S} \right) \right) \]  

(2.1)

where \( I_C \) is the collector current, \( I_S \) is the saturation current, \( V_{BE} \) is the emitter-base voltage and \( V_T \) is the thermal voltage given as \( V_T = kT/q \) where \( k \) is the Boltzmann constant, \( T \) is the absolute temperature and \( q \) is the electronic charge. The difference between 2 emitter-base voltages \( \Delta V_{BE} \) can then be derived as

\[ \Delta V_{BE} = V_{BE1} - V_{BE2} = \frac{kT}{q} \ln p \]  

(2.2)

The VBE voltage has a strong negative temperature coefficient of about -2 mV/°C while the \( \Delta V_{BE} \) has a positive temperature coefficient which is dependent on the current density ratio. By combining these two voltages, a temperature independent voltage \( V_{REF} \) can be generated and is given as

\[ V_{REF} = V_{BE} + \alpha \times \Delta V_{BE} \]  

(2.3)

where \( \alpha \) is a gain factor. A digital temperature reading \( \mu \) can then be determined by combining these voltages as follows [2.26]

\[ \mu = \frac{\alpha \times \Delta V_{BE}}{V_{BE} + \alpha \times \Delta V_{BE}} \]  

(2.4)

Since the \( \Delta V_{BE} \) has a linear dependency on temperature, it can also be used to measure temperature directly. The sensor designed in [2.25] converts \( \Delta V_{BE} \) directly to temperature. A very important issue reported in [2.25] was the failure of the operational amplifier used for creating feedback in the sensor at cryogenic temperatures. Therefore, a lot of effort is needed in designing an operational amplifier that has potential to survive at cryogenic applications. This is even more complicated with the lack of device models for cryogenic temperatures.

### 2.2 Silicon Behaviour at Cryogenic Temperatures

In this section, the low temperature behaviour of silicon is discussed. Many silicon properties are temperature dependent and as such will change as temperature is lowered. Bulk parameters of silicon such as the intrinsic carrier concentration, the effective density of states, the relaxation times of electron and holes, the absorption coefficient and the Fermi level all depend on the effective mass of silicon [2.2]. At low temperatures the effective mass of silicon changes and so also these properties. The electrical conductivity of silicon is dependent on the concentration of free carriers, and hence dopants ionization, and their mobility. These two factors are strongly dependent on temperature and on the dopant concentration. Free carriers in silicon can be
generated by phenomenon such as thermal excitation, impact ionization, tunnelling, doping or a combination of these [2.2]. At low temperatures, the thermal energy of free carriers in silicon decreases, causing incomplete ionization of impurity atoms. Below 30K, there are practically no free carriers causing the so-called freeze-out effect [2.2] [2.3] which gives rise to an exponential decrease in conductivity with decreasing temperature. The electron and hole carrier density can be modelled by the following equation:

\[ n = N_C e^{\frac{E_C - E_F}{kT}} \quad \text{and} \quad p = N_V e^{\frac{E_F - E_V}{kT}} \]  

(2.5)

where \( n \) is the electron density, \( p \) is the hole density, \( E_F \) is the Fermi level, \( N_C \) is the density of states in the conduction band, \( N_V \) is the density of states in the valence band, \( E_C \) is the conduction band energy level, \( E_V \) is the valence band energy level, \( k \) is the Boltzmann constant, and \( T \) is temperature. Fig. 2.2 shows a sketch of the temperature dependency of carrier density for a doped material. At room temperature, the internal energy of the silicon crystal is sufficient to cause ionization of dopant atoms. However, at temperatures below 30K, the internal energy of the silicon crystal can no longer provide sufficient energy to excite the impurity atoms, and nearly all of the electrons are bound to the impurity atoms and the silicon crystal act as an insulating material [2.2]. The intrinsic carrier concentration in silicon \( n_i (= n \times p) \) has a strong temperature dependence which is given by the following relation [2.4]

\[ n_i \propto T^{1.5} e^{-\frac{E_{g0}}{kT}} \]  

(2.6)

where \( E_{g0} \) is the energy band gap at \( T = 0 \) K. Therefore, the intrinsic carrier concentration decreases with decreasing temperature.

![Graph showing the behaviour of carrier density in silicon with temperature](image)

*Figure 15  Behaviour of carrier density in silicon with temperature [2.1]*
The average mobility of free carriers in silicon is determined by various scattering and drift mechanisms. Such mechanisms include lattice (phonon) scattering, surface scattering, neutral-impurity scattering, carrier-to-carrier scattering and velocity saturation. The effects of these mechanisms on the mobility of free carriers as a function of temperature is shown in Fig. 16.

Figure 16 Contribution of different phenomenon to the mobility of free carriers in silicon as a function of temperature [2.1]

Figure 17 Behaviour of mobility of free carriers in silicon with temperature [2.5]
In general, the mobility of free carriers in silicon increases at low temperatures as shown in Fig.17.

\[ E_g(T) = E_g(0) - \frac{\alpha_E T^2}{T + \beta_E} \tag{2.7} \]

where \( E_g(0) \) is the band gap energy at absolute zero on the Kelvin scale in the given material, and \( \alpha_E \) and \( \beta_E \) are material-specific constants [2.7]. Figure 19 shows a plot of the behaviour of the bandgap energy of three different semiconductors including silicon over temperature.

Figure 18 Behaviour of conductivity in silicon with temperature [2.2]
2.3 Low Temperature Behaviour of MOS Transistors

In this section, a description of the effect of low temperatures on the behaviour of the metal-oxide-semiconductor (MOS) transistor and how this impacts its electrical performance is given. The bulk MOS transistor has been observed to perform well down to cryogenic temperatures [2.8]. Fig. 20 shows the current-voltage characteristics of an NMOS and a PMOS device measured down to cryogenic temperatures [2.8] in 0.35 μm technology.

Figure 20 ID-VGS characteristic of an NMOS and a PMOS device [2.8]
The mobility of free carriers and consequently the current in MOS transistors increases at low temperatures. The effect of this is that the maximum achievable trans-conductance of MOS transistors also increase at low temperatures [2.8]. With regards to our design, an increasing trans-conductance at 77 K means the MOS transistors require less headroom which is good for our design since as will be shown we expect an increased threshold voltage at this temperature. Fig. 21 shows the normalized behaviour of the mobility and trans-conductance of an NMOS and a PMOS with temperature.

![Temperature behaviour of the trans-conductance and the mobility of an NMOS and a PMOS device in an unspecified technology](image)

**Figure 21** Temperature behaviour of the trans-conductance and the mobility of an NMOS and a PMOS device in an unspecified technology [2.8]

Another important parameter that determines the electrical performance of MOS transistors is the threshold voltage. The threshold voltage of MOS transistors $V_T$ can be expressed in the following equation [2.4]:

$$V_T = V_{FB} + 2\Phi_F + \gamma \sqrt{2\Phi_F}$$  \hspace{1cm} (2.8)

where $V_{FB} = \Phi_{gs} - \left(\frac{\Phi_{ox}}{C_{ox}}\right)$ is the flat band voltage, with the gate-substrate contact potential, $\Phi_{gs} = \Phi_F \ast \ln(N_A N_G/n_i^2)$, $N_A$ and $N_G$ the substrate and gate doping concentrations, respectively, $Q_{ss}$ the surface charge density, and $C_{ox}$ the oxide capacitance; $\gamma = C_{ox}(2q\varepsilon_{si}N_A)^{0.5}$ is the body effect parameter, with $\varepsilon_{si}$ the relative permittivity of Silicon; $\Phi_F = \Phi_T \ast \ln(N_A/n_i^2)$ is the Fermi energy with the thermal voltage $\Phi_T = kT/q$, and $n_i$ the intrinsic carrier concentration of silicon. We can clearly see that the temperature dependent parameters in equation 2.8 are $\Phi_{gs}$ and $\Phi_F$ which contain both $\Phi_T$ and $n_i$. The temperature dependency of these two parameters has been derived and can be expressed as [2.9]

$$\frac{\partial \Phi_{gs}}{\partial T} = \frac{1}{T} \left( \Phi_{gs} + \frac{E_g(0)}{q} + \frac{3kT}{q} \right)$$ \hspace{1cm} (2.9)

$$\frac{\partial \Phi_F}{\partial T} = \frac{1}{T} \left[ \Phi_F - \left( \frac{E_g(0)}{q} + \frac{3kT}{q} \right) \right]$$ \hspace{1cm} (2.10)
with the temperature dependency of the threshold voltage given as [2.9]

\[
\frac{\partial V_T}{\partial T} = \frac{\partial \phi_{gs}}{\partial T} + \frac{2 \partial \phi_F}{\partial T} + \frac{\gamma}{\sqrt{2\phi_F}} \frac{\partial \phi_F}{\partial T}
\]  

(2.11)

By using practical parameters from a 0.35 μm CMOS technology [2.9], the 3 terms in equation 2.11 where determined as -3.1, 2.7 and -0.43 mV/K which gives a net threshold temperature coefficient of -0.83 mV/K [2.9] [2.10]. The threshold voltage of MOS transistors is usually modelled to increase with decreasing temperatures [2.10]. Therefore, at 77 K we expect a substantial increase in the threshold voltage and this must be taken into account in our design.

The subthreshold leakage current of MOS transistors has an exponential dependence on temperature [2.11]. For \( V_{gs} = 0 \), the subthreshold current, \( I_{sub} \) may be modelled by the Shockley diode model using the following equation

\[
I_{sub} = I_0 \left( e^{\frac{V_{DS}}{\phi_T}} - 1 \right)
\]  

(2.12)

where \( V_{DS} \) is the drain-source voltage of the MOS transistor and \( I_0 \) is the reverse saturation current [2.11]. Figure 22 shows a plot of the behaviour of the sub-threshold current with temperature for different technology nodes. It can be seen from this plot that the sub-threshold leakage current increases with decreasing minimum length. Therefore, at 77K we expect a substantial decrease in the sub-threshold leakage current since we are using a standard 0.16 μm CMOS technology.

![Figure 22. Temperature dependence of the sub-threshold current [2.12]](image-url)
MOS transistors also show an increase in drain current for high drain-source voltage when operated at temperatures close to the temperature of liquid helium, i.e. 4.2 K [2.2]. This is known as the kink effect and is caused as a result of the charging of the silicon substrate by the holes generated by impact ionization (for an NMOS). As a result of this charging, the substrate potential increases with a reduction of the threshold voltage as a consequence. A lower threshold voltage results in higher drain current. This effect seems to occur only at temperatures close to the temperature of liquid helium (4.2 K), therefore not much attention is given to this in our design since we will be operating at 77 K.

![Graph](image)

*Figure 23 Experimental Id-Vd characteristics of NMOS transistor operated at 4.2 K [2.2]*

### 2.3.1 Summary

In this section, a summary of the expected behaviour of MOS transistors at the temperature of liquid nitrogen (77 K) is given.

- **Increased threshold voltage:** It was reported in the previous section that the threshold voltage has a negative temperature coefficient and therefore will increase significantly at low temperatures. At 77 K we expect a substantial increase and therefore must be taken into account in our design.

- **Increase in trans-conductance:** It was also revealed in the previous section that the trans-conductance of MOS transistors increases at very low temperatures. The effect of this is that the overdrive voltage of MOS transistors reduces as temperature decreases. This is particularly important as a corresponding increase in threshold is expected at 77 K.
- **Negligible leakage current**: It reported in the previous section that the sub-threshold leakage current as an exponential dependence on temperature. Therefore at 77 K, we expect a negligible leakage current.

### 2.4 Low Temperature Behaviour of Bipolar Junction Transistors

When bipolar junction transistors (BJT) are operated at very low temperatures, they experience changes in their characteristics. Silicon bipolar transistors experience a degradation in performance at cryogenic temperatures. There are 3 parameters whose temperatures dependence contribute to this degradation. They are 1) the dc-current gain, \( \beta \), 2) the base transit time, and 3) the base resistance [2.13]. The dc-current gain of silicon bipolar transistors decrease quasi-exponentially with decreasing temperature [2.14]. The temperature dependency of the dc-current gain can be modelled by the following relation:

\[
\beta \propto e^{\frac{q(\Delta E_{gb} - \Delta E_{ge})}{kT}}
\]  

(2.8)

where \( E_{ge} \) and \( E_{gb} \) are the apparent bandgap changes in the emitter and the base respectively. Since the emitter is usually more heavily doped than the base, \( \Delta E_{gb} < \Delta E_{ge} \). As temperature is lowered, \( \Delta E_{ge} \) increases more than \( \Delta E_{gb} \) in equation 2.8, and the exponent becomes more negative. Therefore, the dc-current gain decreases exponentially as temperature is decreased. Fig. 24 is a plot of the current gain of a silicon bipolar transistors at different temperatures obtained from literature [2.8].

![Figure 24 Plot showing the reduction in the current-gain of silicon bipolar with reducing temperatures [2.8]](image_url)
The reduction in current gain with reducing temperatures was confirmed by simulation as shown in Figure 25.

![CURRENT GAIN VS IE](image)

*Figure 25 Plot showing the reduction in the current-gain of silicon bipolar with reducing temperatures in CMOS 0.16 μm [2.8]*

Therefore, we expect a negligible dc-current gain a 77 K for the BJT’s in 0.16 μm CMOS technology.

The base transit time of silicon bipolar transistors increases at low temperatures due to freeze-out effect caused by donor concentration in the base [2.13]. Figure 2.23 shows the behaviour of the intrinsic base resistance of a silicon bipolar transistor over temperature. From this plot we observe that, above room temperature the base resistance of silicon bipolar transistors increases as result of enhanced phonon (lattice) scattering [2.14]. In the intermediate temperatures between 150K and 200 K, the base resistance goes through a minimum [2.13] [2.14]. However, at temperatures below 150K, the base resistance starts to increase in a quasi-exponential manner as a result of majority carrier freeze-out.
Figure 26 Plot showing the behaviour of the intrinsic base resistance with temperature [2.14]

The temperature behaviour of base resistance of bipolar transistors was simulated to verify this phenomena. Figure 27 shows the plot of the base resistance of bipolar transistors in 0.16 μm CMOS technology.

Figure 27 Plot showing the behaviour of the intrinsic base resistance with temperature in CMOS 0.16 μm technology [2.14]
The behaviour of the intrinsic base resistance in this technology follows the behaviour predicted in literature as the base resistance is expected to decrease down to about 150 K before increasing quasi-exponentially with decreasing temperature. Therefore, we must take this into account in our design.

Parasitic capacitances like the extrinsic base-to-collector capacitance and the junction depletion capacitances decreases at low temperatures as a result of increase in the built-in potential at low temperatures [2.14]. Also, the trans-conductance of the bipolar transistors improves at low temperatures.

2.4.1 Summary

In this section a summary of the expected behaviour of silicon bipolar transistors at cryogenic temperatures is given. From the previous sections we expect the following behaviour at 77 K.

- **Negligible dc-current gain**: It was reported the previous section that the dc-current gain of bipolar transistors decrease quasi-exponentially with decreasing temperature. For bipolar transistors in standard CMOS 0.16μm technology, we expect a negligible/non-existent dc-current gain at 77 K. This must be taken into account in our design as this is a major source of error in the temperature sensor. We intend to use a technique called current-gain compensation to mitigate this error. This would be discussed in further detail in the next chapter.

- **Increased base-resistance**: It was also reported in the previous section that the intrinsic base resistance of silicon bipolar transistors increases at sufficiently low temperatures below −150°C. Therefore we expect this behaviour also in the bipolar transistors in standard CMOS 0.16 μm technology at 77 K.

- **Increased trans-conductance**: The trans-conductance of silicon bipolar transistors is increases at low temperatures. This is especially important as the voltage noise of a bipolar transistor is a function of the trans-conductance. Therefore at 77 K, we expect a decrease in the noise of the bipolar transistor.

2.5 Conclusion

In this chapter, a detailed overview of the state-of-the-art cryogenic temperature sensors have been given. Their important characteristics have been explored. Also, an exploration of
silicon device behaviours at cryogenic temperatures was also carried out in this chapter. This is important to have an idea of what should be expected at cryogenic temperatures and would also help in forming our design choices.

2.6 References


3

Circuit design and considerations

This chapter describes the design principles and considerations involved in the design of the cryogenic CMOS sensing core. This design aims to investigate the accuracy of the emitter-base voltage and the difference between two emitter-base voltages of bipolar transistors biased at two different current densities down to cryogenic temperatures. It should be stated here that a large part of the design has been based on data from existing literature as the available models for the adopted technology are limited to military range of -55 °C to 125 °C.

3.1 Target Specifications

The design was done in standard CMOS 0.16 μm technology with a nominal supply voltage of 1.8 V. The temperature range of -196 °C to 27 °C has been chosen in line with the objective of operating the sensor at cryogenic temperatures. We expect a temperature inaccuracy of about 0.2°C in the military temperature range after one point trimming [3.10] and about 1 °C at -196 °C also after single-point trimming [3.6]. A summary of the target specifications is shown in Table 1.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
<th>Conditions</th>
</tr>
</thead>
<tbody>
<tr>
<td>Sensor type</td>
<td>BJT</td>
<td></td>
</tr>
<tr>
<td>CMOS Technology</td>
<td>0.16 μm</td>
<td></td>
</tr>
<tr>
<td>Inaccuracy</td>
<td>±0.2 °C @27 °C; ±1 °C @ −196 °C</td>
<td>After single point trimming</td>
</tr>
<tr>
<td>Temperature range</td>
<td>−196 °C to 27 °C</td>
<td></td>
</tr>
<tr>
<td>Resolution</td>
<td>0.01 °C</td>
<td>100 ms conversion time</td>
</tr>
<tr>
<td>Supply voltage</td>
<td>1.8 V</td>
<td></td>
</tr>
</tbody>
</table>
3.2 Bipolar Transistor Characteristics

Most smart temperature sensors are based on bipolar transistors. One reason for this is the reproducibility of their characteristics, which makes it possible to produce high accuracy smart temperature sensors. In other to design bipolar based temperature sensors, an appreciation of the characteristics of bipolar transistors is necessary for good understanding of their operation. In the following sections, a description of some characteristics of bipolar transistors with regards to temperature sensing is given.

3.2.1 Ideal Diode Characteristics

A bipolar transistor has 3 terminals that form 2 PN junctions, and so it is important to explore the characteristics of the PN junction diode. A PN junction diode is formed when a p-typed doped and an n-type doped material are placed together causing diffusion of majority carrier electrons from the n region into the p region and consequent diffusion of majority carrier holes from the p region into the n region. As a result of this diffusion, positively charged donor atoms are left behind in the n region while negatively charged acceptor atoms are uncovered in the p region which results in an electric field that causes a depletion region to be formed around the junction between the n and the p region. When no bias is applied, no current flows as the PN diode is in thermal equilibrium. When a positive external bias is applied, a diffusion current is induced because the electric field in the depletion region is reduced which allows electrons from the n region to diffuse into the p region and holes from the p region to diffuse into the n region [3.1]. The ideal diode equation which gives a good description of the current-voltage characteristics of a PN-junction diode can be written as:

\[ I_D = I_S \left( \exp \left( \frac{V_D}{V_T} \right) - 1 \right) \]  

(3.1)

where \( I_D \) is the diode current, \( I_S \) is the saturation current, \( V_D \) is the applied voltage and \( V_T \) is the thermal voltage given as \( V_T = kT/q \) where \( k \) is the Boltzmann constant, \( T \) is the absolute temperature and \( q \) is the electronic charge. The parameter \( I_S \) the saturation current is highly process and temperature dependent and therefore cannot be controlled accurately. When a voltage \( V_D \gg V_T \) is applied to the PN diode, the \( -1 \) term in the equation for the diode current can be neglected therefore the ideal current can be modified as:

\[ I_D = I_S \left( \exp \left( \frac{V_D}{V_T} \right) \right) \]  

(3.2)

A voltage can also be generated when a current is applied to the diode. When a current \( I_D \) is applied, a voltage \( V_D \) is generated which can be expressed as:

\[ V_D = V_T \left( \exp \left( \frac{I_D}{I_S} \right) \right) \]  

(3.3)

When two bias currents with a predefined ratio \( m:1 \) are applied to the diode, the resulting
difference between the two generated voltages can be derived as:

\[ V_{D1} - V_{D2} = \frac{kT}{q} \ln \frac{mI_{D1}}{I_{S1}} - \frac{kT}{q} \ln \frac{I_{D1}}{I_{S2}} \]  

(3.4)

If the two diodes are assumed to be matched i.e. \( I_{S1} = I_{S2} \) then the difference becomes:

\[ V_{D1} - V_{D2} = \frac{kT}{q} \ln \frac{mI_{D1}}{I_{S1}} - \frac{kT}{q} \ln \frac{I_{D1}}{I_{S2}} = \frac{kT}{q} \ln m \]  

(3.5)

This difference can be observed to be proportional-to-absolute temperature and also independent of the process dependent saturation current and as such can be used for temperature sensing purposes. Looking further into the characteristics of PN junction diode reveal non-idealities such as the generation and recombination currents which are not modelled in the ideal diode equation and which also have different temperature dependencies than the ideal diode equation making them less used for the purpose of temperature sensing [3.2]. If we take into account the recombination currents, the ideal diode equation can be re-written as:

\[ I_D \approx I_S \left( \exp\left( \frac{V_D}{nV_T} \right) - 1 \right) \]  

(3.6)

where \( n \) is the non-ideality factor which can vary between \( n \approx 1 \), when the diffusion current dominates due to large forward-bias voltages, and \( n \approx 2 \), when the recombination current dominates at low forward-bias voltages. The non-ideality factor \( n \) is a process dependent parameter, and so the ideal diode equation now becomes a function of two process dependent parameters, with the consequence that the PTAT voltage between two diode becomes dependent on the process dependent parameter \( n \).

### 3.2.2 Physics of Bipolar Transistors

Since a bipolar transistor consist of two PN diodes, the current-voltage characteristics of the collector current and the emitter-base voltage of a bipolar transistor exhibit the same exponential characteristics as the PN diode when the transistor is biased in the forward-active region. The non-idealities that affect the ideal PN diode current are however, not seen in the collector current of the bipolar transistor but contribute to its base current. This makes the current-voltage relation of the collector current and the base-emitter voltage of bipolar transistors more ideal than the PN diode. This makes bipolar transistors intrinsically better than PN diodes for temperature sensing purposes. In this section, an exploration into the characteristics of bipolar transistors is given. The PNP transistor is used since it is mostly available in most CMOS processes including the one used in this work. The sign convention adopted here is to take the polarity of voltages and currents as positive in the forward active region i.e. the emitter-base junction is forward-biased and the base-collector region is reversed-biased. This means that for a PNP transistor, the emitter-base voltage is positive in the forward active region and should be written as \( V_{EB} \) and \( \Delta V_{EB} \). However in this work, the more familiar notation \( V_{BE} \) and \( \Delta V_{BE} \) is used and should be taken as \( V_{EB} = |V_{BE}| \).
\[ I_C = I_S \left( \exp \left( \frac{V_{BE}}{V_T} \right) - 1 \right) \] (3.7)

where \( I_C \) is the collector current, \( I_S \) is the saturation current, \( V_{BE} \) is the emitter-base voltage and \( V_T \) is the thermal voltage given as \( V_T = kT/q \) where \( k \) is the Boltzmann constant, \( T \) is the absolute temperature and \( q \) is the electronic charge.

The parameter \( I_S \) the saturation current is highly process and temperature dependent and can modelled by the following equation [3.2] [3.3]:

\[ I_S = \frac{kT A_{BE} n_i^2 \mu_p}{Q_B} \] (3.8)

where \( A_{BE} \) is the area of the emitter-base junction, \( n_i \) is the intrinsic carrier concentration in the base, \( \mu_p \) is the average hole mobility in the base, and \( Q_B \) is the total base doping per unit area.

As with PN diodes, when \( V_{BE} \gg V_T \) or \( I_C \gg I_S \) the \(-1\) term in the equation for the collector current can be neglected and the collector current can be expressed as:
\[ I_c = I_s \left( \exp \left( \frac{V_{BE}}{V_T} \right) \right) \]  

(3.9)

from which the emitter-base voltage can be derived as:

\[ V_{BE} = V_T \left( \exp \left( \frac{I_c}{I_s} \right) \right) \]  

(3.10)

When two bipolar transistors are biased with a predefined current density ratio \( m : 1 \) as shown in Fig. 29, the resulting difference between the two generated voltages can be derived as:

\[ V_{BE1} - V_{BE2} = \frac{kT}{q} \ln \frac{mI_{C2}}{I_{S1}} - \frac{kT}{q} \ln \frac{I_{C2}}{I_{S2}} \]  

(3.11)

If the two transistors are assumed to be matched i.e. \( I_{S1} = I_{S2} \) then the difference becomes:

\[ \Delta V_{BE} = V_{BE1} - V_{BE2} = \frac{kT}{q} \ln \frac{mI_{C2}}{I_{S1}} - \frac{kT}{q} \ln \frac{I_{C2}}{I_{S2}} = \frac{kT}{q} \ln m \]  

(3.12)

The resulting difference can be observed to be proportional-to-absolute temperature and also independent of the process dependent saturation current and as such can be used for temperature sensing purposes.

### 3.2.3 The effect of saturation current on the \( I_C - V_{BE} \) characteristics

The equation of (3.12) was derived based on the assumption that \( I_C \gg I_S \). However for low bias currents, the ideal equation for the collector current given in (3.7) holds and equation (3.12) has to be modified to become [3.2]:

\[ \Delta V_{BE} = V_{BE1} - V_{BE2} = \frac{kT}{q} \ln \left( \frac{mI_{C2} + I_S}{I_{C2} + I_S} \right) \approx \frac{kT}{q} \ln \left( m - \frac{I_S}{I_{C2}} (m - 1) \right) \]  

(3.13)

The obvious consequence of this is that for an accurate PTAT voltage, the bias currents have to be much higher than the saturation current. This imposes a constraint on the choice of bias currents and bias ratio. However, there’s a limitation to how high the currents can be so as to avoid self-heating and a significant voltage drop on the transistor’s series resistance. Also, the saturation current has an exponential dependence on temperature, which becomes significant for higher temperatures. For low temperatures however, which is the focus of this work, the effect of saturation current is less important as a result of the aforementioned exponential dependence of saturation current on temperature. Therefore, at cryogenic temperatures the saturation current is almost negligible and does not impose a significant constraint on our choice of currents.
3.2.4 The effect of current-gain $\beta$ on the $I_C - V_{BE}$ characteristics

Substrate PNP bipolar transistors in CMOS processes are typically biased through their emitters because their collectors are grounded. This is especially important in the diode-connected configuration shown in Fig. 29 where the base is grounded i.e. the base-collector voltage is zero. The implication of this is that the base current is removed from the accurately controlled emitter current i.e. if $I_E$ is the emitter current, $I_C$ the collector and $I_B$ the base current, then we have that:

$$I_C = I_E - I_B$$  \hspace{1cm} (3.14)

and with the forward emitter current gain $\beta$ defined as $\beta = \frac{I_C}{I_B}$, equation (3.15) can be further expressed as:

$$I_C = \frac{\beta}{\beta + 1} I_E$$ \hspace{1cm} (3.15)

![CURRENT GAIN VS IE](image)

*Figure 30* Current-gain for different bias currents at different temperatures

The current gain of diode-connected bipolar transistors has been shown to vary with currents even at the same temperature. This can be clearly seen in Fig. 30 which is a plot of the current-gains of the PNP bipolar transistor used in this work at different current densities and at different temperatures. The plot reveal that an intermediate region exists where the current gain is hardly dependent on the bias current. By carefully choosing bias currents in this current range we can avoid or limit to a great extent this dependency of current-gain on the bias currents. The current-gain dependent collector current expressed in equation (3.15) would lead to a current-gain dependent emitter-base voltage which can be expressed as:
\[ V_{BE} = V_T \left( \exp \left( \frac{\beta I_E}{I_S} \right) \right) \]  

(3.16)

The effect of this is that an error is introduced into the \( \Delta V_{BE} \) voltage as derived below [3.4]:

\[ \Delta V_{BE} = \frac{kT}{q} \ln \frac{\beta_2(I_{E2})}{\beta_1(I_{E1})} + \frac{1}{I_{E2}} I_{E2} \]  

(3.17)

\[ \Delta V_{BE} = \frac{kT}{q} \ln I_{E2} + \frac{kT}{q} \ln \frac{\beta_2(I_{E2})}{\beta_1(I_{E1})} + \frac{1}{I_{E2}} I_{E2} \]  

(3.18)

where \( I_{E1} \) and \( I_{E2} \) are the two bias currents and \( \beta_1 \) and \( \beta_2 \) are the current-gains at those currents. The plots of Fig. 30 also reveal that the current gain of diode-connected PNP bipolar transistors degrades with decreasing temperature. A very low current-gain at low temperatures simply means a high base current that is almost equal to the collector current. The effect of this is that the error introduced into the emitter-base voltage and the \( \Delta V_{BE} \) voltage would get worse at low temperatures. As stated earlier, by choosing currents in the intermediate region of the plot and by using a circuit compensation technique, which will be discussed in a later section, this error can be greatly reduced.

### 3.3 Basic Principle of a Bipolar based CMOS Sensing Core

The circuit of Fig. 31 shows the general structure of a CMOS bipolar-based temperature sensing core. This circuit consists of a bias circuit and the bipolar core [3.2]. The bias circuit is needed to generate an accurate, well-controlled current. This well-controlled current is mirrored onto the current sources in the bipolar core which is then used to generate the emitter-base voltages in the bipolar transistors. The bias circuit consist of two diode-connected substrate PNP bipolar transistors biased using PMOS current sources with a predefined current density ratio. In the bias circuit, a high-gain amplifier creates a feedback loop which ensures that the difference in the emitter-base voltages of the two bipolar transistors is generated across the resistor.
The following derivations show how the well-defined current in the bias circuit is generated. $V_{BE,Q1}$ and $V_{BE,Q2}$ are the emitter-base voltages of the two diode-connected bipolar transistors in the bias circuit. $\Delta V_{BE,\text{bias}}$ is the difference between the two base-emitter voltages, $R_0$ is the resistor over which the current is generated, while $I_0$ is the generated current with a current density ratio of 1: $m$.

$$V_{BE,Q1} - V_{BE,Q2} = V_{R0,\text{bias}}$$  \hfill (3.19)

$$\Delta V_{BE,\text{bias}} = V_{R0,\text{bias}} = I_0 R_0$$  \hfill (3.20)

$$V_{BE,Q2} = \frac{kT}{q} \ln \frac{I_0}{I_S}$$  \hfill (3.21)

$$V_{BE,Q1} = \frac{kT}{q} \ln \frac{mI_0}{I_S}$$  \hfill (3.22)

$$\Delta V_{BE,\text{bias}} = V_{BE,Q2} - V_{BE,Q1} = \frac{kT}{q} \ln m$$  \hfill (3.23)

From equation (3.19), the generated current $I_0$ can then be written as:

$$I_0 = \frac{\Delta V_{BE,\text{bias}}}{R_0} = \frac{kT}{q} \ln \frac{m}{R_0} = \frac{kT \ln m}{q R_0}$$  \hfill (3.24)

It can be clearly seen that the generated current is proportional-to-absolute-temperature (PTAT). This PTAT/R current can then be mirrored onto the PMOS current sources in the bipolar core with a predefined current density ratio. Again, if we take this ratio to be 1: $m$, the emitter-base voltages generated in the two transistors in the bipolar core can be expressed as:

$$V_{BE,Q3} = \frac{kT}{q} \ln \frac{I_0}{I_S}$$  \hfill (3.25)
\[ V_{BE, Q4} = \frac{kT}{q} \ln \frac{m I_0}{I_s} \]  

(3.26)

where \( I_s \) is the saturation current. The difference in the emitter-base voltages of the transistors in the bipolar core can then be written as:

\[ \Delta V_{BE} = V_{BE, Q4} - V_{BE, Q3} = \frac{kT}{q} \ln m \]  

(3.27)

Equation (3.27) shows clearly that this voltage is also proportional-absolute-temperature (PTAT). As would be described in detail in the following sections, several sources of error are associated with the circuit of Fig. 31 and would have to be taken into consideration if the best performance is to be obtained from this circuit.

### 3.3.1 Finite Current-Gain Compensation

We have seen in earlier sections that because diode-connected PNP bipolar transistors are biased through their emitters, their current-gain is dependent on the bias current. This current dependency of current gain will lead to errors in both the emitter-base voltage and the \( \Delta V_{BE} \) voltage.

### 3.3.2 Error due to Finite Current-Gain

Because the current generated in the bias circuit is generated from the difference between two emitter-base voltages, it is affected by the dependency of current-gain on bias current as discussed in previous sections. Since this current is mirrored to bias the diode-connected PNP bipolar transistors in the bipolar core, this error would be seen in both the emitter-base voltage and the \( \Delta V_{BE} \) voltage generated in the bipolar core circuit of Fig. 4. The amount of error introduced into the \( \Delta V_{BE} \) voltage has been computed in a previous section and was derived as:

\[ \Delta V_{BE} = \frac{kT}{q} \ln I_{E2} + \frac{kT}{q} \ln \frac{\beta_2(I_{E2})}{\beta_1(I_{E1})} + \frac{1}{\beta_1(I_{E1}) + 1} \]  

(3.28)

where \( \beta_1 \) and \( \beta_2 \) are the current-gain of the two bipolar transistors at the bias currents. The second term in equation (3.28) expresses the error introduced into the \( \Delta V_{BE} \) voltage as a result of the dependency of the current-gain on the biasing current. Given that the sensitivity of \( \Delta V_{BE} \) can be written as \( \frac{d\Delta V_{BE}}{dT} = \frac{k}{T} \ln m \) from which we can derive that \( \frac{d\Delta V_{BE}}{\Delta V_{BE}} = \frac{dT}{T} \), with current gain at emitter currents of 200nA and 1\( \mu \)A being 4.55 and 4.62 respectively we obtain a voltage error in \( \Delta V_{BE} \) of about 71.75\( \mu \)V at 300K which corresponds to an error of about 0.52\(^\circ\)C in temperature. This obviously is a huge temperature error and therefore has to be compensated for. At low temperatures this error will increase significantly as current-gain drops substantially.
### 3.3.3 Base Current Compensation

It has been established that a significant error is introduced in the $\Delta V_{BE}$ voltage because substrate bipolar transistors are biased from their emitter rather than their collector. We can compensate for this error by generating an accurate collector current from the bias circuit to bias the bipolar transistors in the bipolar core. To do this the circuit of Fig. 32 was proposed [3.2]. In this circuit, a scaled version of the bias resistor is added to the base of the transistor that is biased with the higher current density. The generated collector current can be derived as follows:

\[
V_{BE,Q1} + I_{B,Q1} \frac{R_0}{m} = V_{BE,Q2} + I_0R_0
\]

with $I_{B,Q1} = \frac{mI_0}{\beta + 1}$

\[
V_{BE,Q1} + I_0 \frac{R_0}{\beta + 1} = V_{BE,Q2} + I_0R_0
\]

\[
\Delta V_{BE,bias} = V_{BE,Q1} - V_{BE,Q2} = I_0R_0 \frac{\beta}{\beta + 1}
\]

where $I_0$ can then be derived as:

\[
I_0 = \frac{\beta + 1}{\beta} \frac{\Delta V_{BE,bias}}{R_0}
\]

This current can then be used to generate the emitter-base voltages in the bipolar core. With Q3 biased with $I_0$, its emitter-base voltage can be written as:

\[
V_{BE,Q3} = \frac{kT}{q} \ln \left( \frac{I_0}{I_S} \frac{\beta}{\beta + 1} \right) = \frac{kT}{q} \ln \frac{\Delta V_{BE,bias}}{I_SR_0}
\]

We can see clearly that this voltage is independent of the current-gain and therefore the generated $\Delta V_{BE}$ voltage would also be independent of the current gain and its associated error.
3.3.4 Error due to Series Resistance

We have established in previous discussions that the base resistance of bipolar transistors increase quasi-exponentially at very low temperatures [3.10]. A simple model showing the effect of ohmic resistances in a PN bipolar transistor is shown in Fig. 33 [3.2] [3.4] where $R_e$ is the emitter resistance and $R_0$ is the base resistance. Taking into account these resistances the base-emitter voltage can be re-written as described below:

$$\begin{align*}
V_{BE} &= V'_{BE} + I_E R_E + I_B R_B,
\end{align*}$$

(3.34)
where $V'_{BE} = \frac{kT}{q} \ln \frac{I_C}{I_S}$ is the intrinsic base-emitter voltage of the bipolar transistor. We know that the emitter current can be related to the base current using the relation $I_B = \frac{I_E}{\beta + 1}$, therefore equation (3.34) can be re-written as follows:

$$V_{BE} = \frac{kT}{q} \ln \frac{I_C}{I_S} + I_E \left( R_E + \frac{R_B}{\beta + 1} \right) = \frac{kT}{q} \ln \frac{I_C}{I_S} + I_E R_S$$

(3.35)

The effect of both emitter and base resistances can therefore be lumped together into a single resistance called the series resistance $R_S$. The series resistance can then be written as $R_S = R_E + \frac{R_B}{\beta + 1}$. We can deduce from this expression that at low temperatures when the current-gain decreases the base resistance term of the series resistance will increase causing significant amount of errors in the emitter-base voltage. If we then take the difference between the emitter-base voltages of two bipolar transistors biased with a current ratio of 1: $m$, we can quantify the error introduced by the effect of series resistance as follows:

$$\Delta V_{BE} = V_{BE2} - V_{BE1} = \frac{kT}{q} \ln m + (m I_{E1} - I_{E1}) R_S$$

(3.36)

$$\Delta V_{BE} = \frac{kT}{q} \ln m + (m - 1) I_{E1} R_S$$

(3.37)

where the second term in equation (3.37) expresses the error due to the series resistance. The error in the $\Delta V_{BE}$ voltage due to the series resistance is modulated by the current ratio factor. Coupled with the expected increase in the series resistance at low temperatures, this source of error is a significant contribution to the inaccuracy of the $\Delta V_{BE}$ voltage. From equation (3.37), we notice that this error is dependent on the value of the bias current. This puts a constraint on our choice of currents as a large current density means a large error due to series resistance. By carefully deciding our choice of currents we can reduce this error substantially. As an example, for a 200nA bias current and a series resistance of 125Ω at 300K using a current ratio of 5, this corresponds to a 100µV error in $\Delta V_{BE}$ leading to a 0.72°C error in temperature.

### 3.3.5 The Current density ratio

Several constraints determines the choice of current and current density ratio. The unit current that is chosen would be amplified in the second bipolar transistor by the value of the current density ratio. A high current which is much higher than the saturation current is desired in order to minimize the errors due to saturation current. A high current density is also desired because a higher current means less noise. Since $\Delta V_{BE}$ is proportional-to-absolute-temperature and its value depends on the current density ratio, a high current density ratio is advantageous since we desire to measure down to cryogenic temperatures. However, a high current density means that the errors due to series resistance increases. We know that this error would get worse at low temperatures, therefore we need to find an optimum. Fig. 7 shows a plot of the simulation
of the maximum temperature error obtained over corners on $\Delta V_{BE}$ for a range of currents at different current densities ratio over the temperature range of $-55^\circ C - 25^\circ C$. This plot was generated by simulating the circuit of Figure 34.

![Figure 34 Simulated circuit used for obtaining the plot of Figure 35](image)

**Figure 34** Simulated circuit used for obtaining the plot of Figure 35

![Temperature Error vs Bias Current](image)

**Figure 35** Maximum temperature error on $\Delta V_{BE}$ obtained over temperature ($-55^\circ C - 25^\circ C$) for different bias currents and current density ratios
We see a substantial increase in the temperature error at low currents for the different current ratios due to the effect of saturation current. We also notice that the temperature error increases significantly at higher currents due to high injection effects. Therefore, the optimum current has to be in the middle range of currents. From all this consideration a current density ratio of 5 and a unit bias current of about 170 mA at room temperature was chosen.

### 3.3.6 Error due to Mismatch

The $\Delta V_{BE}$ voltage is generated by operating the two bipolar transistors at a well-defined current ratio. This can be obtained by employing two transistors with different emitter areas that are biased at different or the same currents or by using identical bipolar junction transistors that are biased at different current densities. With identical transistors biased with a current density ratio $m$: 1, the equation for the ideal $\Delta V_{BE}$ voltage is:

$$
\Delta V_{BE} = kT \frac{q}{q} \ln \left( \frac{mI_0}{I_s} \right) - kT \frac{q}{q} \ln \left( \frac{I_0}{I_s} \right)
$$

$$
\Delta V_{BE} = kT \frac{q}{q} \ln m
$$

(3.38)

As can be noticed, an error in the current density ratio (as well as the emitter ratio) used for the bias of the bipolar transistors can introduce inaccuracies in the generated $\Delta V_{BE}$ voltage. If a mismatch exists in the current ratio, we can qualitatively derive the error introduced into the generated $\Delta V_{BE}$ voltage as follows [3.3] [3.2]:

Using identical bipolar transistors and assuming that a mismatch $\Delta m$ exists in the current ratio, the generated $\Delta V_{BE}$ voltage becomes:

$$
\Delta V_{BE} = \frac{kT}{q} \ln (m + \Delta m)
$$

(3.39)

which can be further simplified as:

$$
\Delta V_{BE} \approx \frac{kT}{q} \ln m \ast \left( 1 + \frac{\Delta m}{m \ln m} \right) \text{ assuming } \Delta m \ll m
$$

(3.40)

$$
\Delta V_{BE} \approx \frac{kT}{q} \ln m + \frac{kT \Delta m}{q \ m}
$$

(3.41)

The last term in equation (3.41) represents qualitatively the error introduced into the $\Delta V_{BE}$ voltage as a result of mismatch in the bias current ratio. As an example, for a 10mK accuracy in temperature at 300K with a current ratio of 5, we can calculate that a maximum mismatch of about 0.05% is required. This error can be significantly reduced by employing dynamic element matching (DEM) which will be discussed in detail in next section.
3.3.7 Dynamic Element Matching (DEM)

Dynamic element matching (DEM) is used to reduce the mismatch between elements that are designed to be identical. In DEM technique, the position of each element is cyclically interchanged over time and the average taken [3.3]. Therefore, the overall accuracy of the average is better than the individual value of each element. In this design dynamic element matching is used not only to reduce mismatch in both the current sources of the bias circuit and the bipolar core but also used to reduce mismatch between the bipolar transistors in the bipolar core. Also, switches are placed between the banks of current sources in the bias circuit and the banks of current sources in the bipolar core to be able to interchange them. All this different schemes are used to greatly reduce the effect of mismatch in this design.

As shown in Fig. 36, each of the unit current sources can be directed to transistors Q1 or Q2. In each DEM cycle, a unit bias current source $I_{0,j}$ (1 ≤ j ≤ 1 + m) is directed to one of the bipolar transistors while the remaining current sources are directed to the other transistor giving a $\Delta V_{BE,j}$ that can be expressed as [3.2] [3.3]:

$$\Delta V_{BE,j} = \frac{kT}{q} \ln \left( \frac{\sum_{i=1,i\neq j}^{m+1} I_{0,i}}{I_{0,j}} \right) = \frac{kT}{q} \ln(m + \Delta m_j)$$ (3.42)

Figure 36 PTAT voltage generation with dynamic element matching of current sources
After \((1 + m)\) cycle, the average of the possible \(\Delta V_{BE}\) voltage can be written as:

\[
\Delta V_{BE,avg} = \frac{1}{m + 1} \sum_{j=1}^{m+1} \Delta V_{BE,j}
\]

(3.43)

It has been shown that first order errors are removed as a result of averaging but second order errors still remains which can be expressed as \([3.2]\):

\[
\left| \Delta V_{BE,avg} - \Delta V_{BE} \right|_{\Delta m=0} < \frac{1}{2}kT \left( \frac{\Delta m}{m} \right)^2
\]

(3.44)

where \(\Delta m/m\) is the mismatch between a current source and the average of the other current sources.

3.3.8 Error due to Offset Voltage

Any offset associated with the operational amplifier that is used to create feedback in the bias circuit will introduce error in the current generated from the bias circuit. Since this current is mirrored to bias the bipolar core, this error will affect the emitter-base voltages and the \(\Delta V_{BE}\) voltage that is generated by the transistors in the bipolar core. A qualitative derivation of the errors introduced is given below \([3.2]\).

If \(V_{OS}\) is the input offset associated with the operational amplifier, the generated bias current in the bias circuit becomes:

\[
i_0 = \frac{\Delta V_{BE,bias} + V_{OS}}{R_o}
\]

(3.45)

This current is then mirrored to bias the transistors in the bipolar core. The emitter-base voltage generated from this unit current source can be expressed as:

\[
V_{BE,Q3} = \frac{kT}{q} \ln \left( \frac{\Delta V_{BE,bias} + V_{OS}}{R_o I_S} \right) \approx \frac{kT}{q} \ln \left( \frac{\Delta V_{BE,bias}}{R_o I_S} \right) + \frac{V_{OS}}{\ln m}
\]

(3.46)

The second term in this equation indicates the error on the emitter-base voltage as a result of offset. With the sensitivity of the emitter-base given as \(-20mV/°C\) we have that for 0.01°C accuracy, a 20μV offset is required. Offsets in mV range are usually typical of CMOS operational amplifiers, therefore it is obvious that an offset cancellation scheme is need to achieve this level of offset.

3.3.9 Noise

The resolution of the temperature sensor is determined by the noise on the emitter-base voltage and the \(\Delta V_{BE}\) voltage generated in the bipolar core. The amount of noise sets the lower limit on the minimum detectable signal. As stated in an earlier section, the amount of noise also set a constraint on the choice of currents.
A simulation of the noise [°C r.m.s] at different current levels for different bias ratio is shown in Fig. 37. The noise [°C r.m.s] shown in figure 10 was derived by using the sensitivity of the ideal $\Delta V_{BE}$ voltage. In this design the target resolution is about 0.02°C r.m.s noise. The total noise in the bipolar core is dominated by the noise of the diode-connected bipolar transistors and the noise on the bias current on them. The noise generated by the bipolar transistors has comprises of the shot noise of the collector current, the thermal noise of the base resistance and the flicker noise of the bipolar transistors.

The intrinsic noise on the emitter-base voltage of a diode-connected bipolar transistor can be written as:

$$v_{n,BE}^2 = \frac{i_{n,c}^2}{g_m^2} + 4kTR_B B = 2BkT\left(\frac{kT}{ql_o} + 2R_B\right) = 2BkT\left(\frac{1}{g_m} + 2R_B\right)$$  (3.47)

where $g_m$ is the transconductance of the transistor and is given as $g_m = \frac{i_0}{V_T}$ with $V_T$ being the thermal voltage and $B$ is the noise bandwidth. If we take into account the flicker noise of the transistor, the total noise on the emitter-base voltage becomes:

$$v_{n,BE}^2 = \frac{i_{n,c}^2}{g_m^2} + 4kTR_B B + \frac{KI_B}{fA_e}$$  (3.48)

where the third term in equation (3.49) indicates the amount of flicker noise with $K$ being the flicker noise coefficient, $A_e$ the emitter area and $f$ the frequency. We see that at low temperatures when the current-gain decreases and the base current increases, the flicker noise component in equation (3.49) will increase.

The noise power on $\Delta V_{BE}$ is the sum of the noise power of the base-emitter voltages of the two bipolar transistors. Therefore, the noise on the $\Delta V_{BE}$ voltage can be expressed as:

$$v_{n,\Delta V_{BE}}^2 = \frac{i_{n,c}^2}{g_m^2} \left(1 + \frac{1}{m}\right) + 8kTR_B B + \frac{KI_B}{fA_e} (1 + m)$$  (3.49)

![NOISE VS BIAS CURRENT](image)

*Figure 37 Noise (°C r.m.s) for different current levels at different bias ratio at room temperature*
3.4 Realization

3.4.1 Operational Amplifier Design

Conventional amplifiers have been shown to experience a loss of gain at low temperatures [3.6]. Therefore, a high gain amplifier was chosen for use in this circuit. Fig. 39 shows the gain-boosted folded cascode operational amplifier designed for this temperature sensing core. As stated earlier the design is based on data from existing literature as the available models for the adopted technology are limited to military range of -55 °C to 125 °C. The input voltages is expected to vary from between 560mV at room temperature to about 1.2V at cryogenic temperatures, therefore an NMOS input pair is used to allow a high input common-mode range. The threshold voltage of MOS transistors has been observed to increase at low temperatures therefore, in order to have enough headroom for the cascode transistors at low temperatures, a folded cascode configuration was chosen. The currents through the input pair is about 175nA each at room temperature while the current in the two cascode branches is also about 175nA. The overall loop gain of the circuit is about 98dB at room temperature. Plots of the loop gain magnitude and phase of the extracted layout of the operational amplifier and also its behaviour over temperature is shown Fig. 40 and Fig. 41.
Figure 39 Gain-boosted folded cascode operational amplifier designed in this project

<table>
<thead>
<tr>
<th>Stability Response</th>
<th>Name</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Loop Gain (dB)</td>
</tr>
<tr>
<td></td>
<td>Loop Gain Phase</td>
</tr>
<tr>
<td></td>
<td>Loop Gain Phase 1/a</td>
</tr>
<tr>
<td></td>
<td>Loop Gain Phase 1/b</td>
</tr>
</tbody>
</table>

Figure 40 Plot of loop gain and phase of the schematic (blue curve) and extracted layout (red curve) of the circuit
3.4.2 Chopping

At frequencies close to DC, the performance of operational amplifiers can be degraded by effects such as offset, 1/f or flicker noise and thermal noise. Offset is an important source of error and is caused mostly by mismatch in transistors. The current generated in the bias circuit can be affected by offset. Chopping is a dynamic offset cancellation technique and therefore has the advantage that it can compensate for the drifts in offset and its temperature dependency. As well as offsets, chopping also helps in removing low frequency non-idealities like 1/f noise and baseband thermal noise. As we have noticed in previous discussions, offsets in the order of μV are required for high accuracy and therefore makes dynamic offset cancellation techniques like chopping necessary.
Figure 42 Bias circuit with chopper switches

Chopping involves the use of a square wave at a frequency say, $f_{chop}$ to modulate the inputs of the operational amplifier through an input chopper (polarity-reversal switch) and then demodulated back to baseband through the output chopper after amplification. The offset on the other hand is modulated only once and therefore shows up as a frequency component at the modulating frequency $f_{chop}$. The chopping technique also has an advantage for noise as choosing a chopping frequency that is greater than the $1/f$ corner frequency of the operational amplifier means that the wide band thermal doesn’t fold back into baseband [3.7]. Transmission gate switches are used as the chopper switches for both the input and the output choppers. Minimum sized switches are used for both the input and the output choppers. The use of minimum sized chopper switches helps to reduce charge injection and clock-feed through. A chopping frequency of 100 KHz is used in this design.
3.4.3 Circuit configuration of the designed temperature sensing core

Fig. 44 shows the overview configuration of the circuit of the temperature sensing core. Dynamic element matching is used for the current sources both in the bias circuit and the bipolar core. A controllable current gain compensation is used by connecting an NMOS switch to the scaled resistor in the bias circuit so that it can be turned on or off if necessary. N-Poly resistors are used with nominal value of the resistor $R_0$ being $250k\Omega$. NPN bipolar transistors with emitter area of $25m^2$ are used. Transmission gate switches are used in the DEM configuration because at low temperatures the emitter-base voltage would rise to about $1.2$ V. A shift register is used to give the control signals for the circuit. The operational amplifier is chopped to remove offset and low frequency noise. A supply voltage of $1.8$ V has been used.

![Figure 44 Circuit configuration of the designed temperature sensing core](image-url)
3.4.4 Fail-safe Mechanisms

In this design a number of fail-safe mechanisms have been put in place to ensure that the circuit continues its operation despite the failure of any part of the circuit. The mechanisms put in place are explained below:

1. **External Operation Amplifier**: From literature [2.14], we learn that operational amplifiers may suffer from gain loss at very low temperature. A probable cause of this could be that the transistors in the operational amplifier go out of saturation because they do not have enough headroom. Since we cannot simulate this due to non-availability of models, we have brought out the 3 pins of the internal operational amplifier such that in case of its failure, an external operational amplifier can be connected to it so that it can continue its operation.

2. **Multiplexer for default configuration**: As a result of the uncertainty at very low temperatures, there arose a doubt that the shift register might cease to function at low temperatures. A multiplexer has been employed in this design to put the circuit to a predefined default configuration just in case a mishap happens to the shift register. The output of the multiplexer is connected to the configuration signal of the circuit. In normal operation, the multiplexer select the output of the shift register. In case of malfunctions in the shift register, the multiplexer selects the default hardwired setting. Since this circuit contains only static combinatorial logic, it should be more robust to cryogenic non-idealities than the dynamically-loaded shift register. A ‘0’ at the input of the multiplexer puts the DEM control in this predefined default configuration while a ‘1’ ensures that the shift register can be used in normal operation.

3.4.5 Start-up

A start-up switch is added to this design to ensure that the PMOS current sources turn on when the supply is applied. An NMOS switch is used for this purpose. The drain of the switch is connected to the gate of the PMOS current sources while its source is connected to ground such that when the start-up switch is on, the gate of the PMOS current sources is connected to ground thereby turning them on.

![Figure 45](image)

*Figure 45* Start-up NMOS switch
3.4.6 Complete Circuit

The complete circuit of the CMOS temperature sensing core designed is shown in Fig. 46. It shows the two banks of the DEM scheme for the bias circuit and the bipolar core. It also shows the connection of the internal operational amplifier to the bond pads through transmission gate switches. The NMOS switch used for start-up is also shown as well as the controllable current gain compensation resistor with an NMOS switch connected in parallel to it.

![Figure 46 Complete circuit of the temperature sensing core](image-url)

*Figure 46 Complete circuit of the temperature sensing core*
3.4.7 Shift register Bits

As mentioned earlier, the signals going to the circuit are controlled by a shift register. The shift register employed in this design has 37 bits. The list of the control bits is shown in Table 1. B1_DEM are the control signals for the first bank of current sources with B2_DEM being the control signals for the other bank of current sources. These two banks can be interchanged to supply either the bias circuit or the bipolar core. The BANK SWAP signal is used for interchanging the two bank of current sources. The OTA CHOP control signal is used for controlling the chopping signals while the BETA ENABLE control signal is used for enabling or disabling the current-gain compensation. Because we intend to use an external operational amplifier, the OP-AMP SWITCH signal is added for connecting the external operational amplifier to the circuit. The full list is shown below.

Table 2 List of the control signals from the shift register

<table>
<thead>
<tr>
<th>Name of Control Signal</th>
<th>Control bits</th>
<th>Number of control Bits</th>
</tr>
</thead>
<tbody>
<tr>
<td>B1_DEM</td>
<td>0 – 5</td>
<td>6</td>
</tr>
<tr>
<td>B1_DEM_B</td>
<td>6 – 11</td>
<td>6</td>
</tr>
<tr>
<td>B2_DEM</td>
<td>12 – 17</td>
<td>6</td>
</tr>
<tr>
<td>B2_DEM_B</td>
<td>18 – 23</td>
<td>6</td>
</tr>
<tr>
<td>BANK SWAP</td>
<td>24 – 25</td>
<td>2</td>
</tr>
<tr>
<td>OTA CHOP</td>
<td>26 – 27</td>
<td>2</td>
</tr>
<tr>
<td>BETA ENABLE</td>
<td>28</td>
<td>1</td>
</tr>
<tr>
<td>START UP</td>
<td>29</td>
<td>1</td>
</tr>
<tr>
<td>B3_D</td>
<td>30 – 34</td>
<td>5</td>
</tr>
<tr>
<td>OP-AMP SWITCH</td>
<td>35 – 36</td>
<td>2</td>
</tr>
</tbody>
</table>
3.4.8 Pin Count of the Chip

As shown in Table 2, this design has 16 pins consisting of 3 supply pins, 3 ground pins, 6 analog pins and 4 digital pins. An ETF with 4 pins was incorporated into the chip making the chip’s pin count increase to 20. The full list of the pins is shown in Table 3.

Table 3 List of the Pins of the Chip

<table>
<thead>
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</tr>
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<td>GROUND</td>
</tr>
<tr>
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<td>SUPPLY</td>
</tr>
<tr>
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<td>DIGITAL GROUND</td>
<td>GROUND</td>
</tr>
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<td>OUTPUT1</td>
<td>ANALOG</td>
</tr>
<tr>
<td>VBE2</td>
<td>OUTPUT2</td>
<td>ANALOG</td>
</tr>
<tr>
<td>OUT</td>
<td>OP-AMP OUTPUT</td>
<td>ANALOG</td>
</tr>
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<td>OPAMP + INPUT</td>
<td>ANALOG</td>
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<tr>
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<tr>
<td>DOUT</td>
<td>DIGITAL OUTPUT</td>
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</tr>
</tbody>
</table>
### 3.4.9 Simulation Results

Fig. 47 and Fig. 48 shows some simulation results of this design. Fig. 47 is a DC simulation showing the emitter-base voltage and the $\Delta V_{BE}$ voltage over temperature. Net012 and 011 are the emitter-base voltages while their difference is the DVBE voltage. Fig. 48 is a transient simulation showing the digital signals and the two emitter-base voltages at room temperature.

![DC Response](image)

*Figure 47 DC simulation showing the emitter-base voltage and the $\Delta V_{BE}$ voltage over temperature*
Figure 48 Transient simulation showing the digital signals and the two emitter-base voltages at room temperature

Figure 49 Plot of noise power on $\Delta V_{BE}$ of the bipolar core before chopping
3.4.10 Layout

The layout of the circuit is shown in Fig. 51 and Fig. 52. A description of the various sections is shown on the diagram. A number of techniques and precaution was taken while making the layout of the chip. Multi-finger transistors was used so as to reduce both the source/drain junction area and the gate resistance [3.8]. Care was taken to ensure symmetry in the layout so as to avoid mismatch which can cause offset in the amplifier for example. Dummy transistors are added to each side of the transistors in the amplifier so as reduce asymmetry and mismatch [3.9] [3.8]. In larger transistors a common-centroid configuration is used for reducing mismatch in them by decomposing the transistor into halves and placing them diagonally opposite each other and then connecting them in parallel [3.8].
Figure 51 Layout of the temperature sensing core

Figure 52 Layout of the temperature sensing core with the Padrino
3.5 Conclusion

In this chapter, a detailed insight into the considerations involved in the design of the CMOS bipolar sensing core have been given. Various design choices and the reasoning behind such choices have been explained. Precision techniques employed in the design such as chopping, dynamic element matching and current gain compensation and the impact they have on the circuit performance are all explained. Simulation results demonstrating the sensor functionality have also been reported. The design was taped-out and is expected to function.

3.6 References


4

Measurements and Results

This chapter gives an overview of the measurement set-up used for the characterization of the fabricated sensors and the achieved results. Figure 53 shows the micrograph of the fabricated chip. The chip was fabricated in a standard 0.16-$\mu$m CMOS technology. The main components of the sensor (bipolar transistors, bias resistors, PMOS current sources operational amplifier) are all highlighted in the micrograph. Two sets of measurements were performed on the sensor. The first was carried out in an oven in which the sensor was characterized from $-65^\circ C$ to $30^\circ C$ while the second measurement was carried out at the temperature of liquid nitrogen ($-196^\circ C$). An overview of the two test set-ups will be given in the following sections.

Figure 53 Micrograph of the fabricated chip
4.1 Test Set-up for Oven Measurements

Figure 54 shows an overview of the test set-up that was used for characterizing the sensor in the oven. Two custom PCB’s were designed for the characterization of the sensor. The chips (device under test, DUT) are mounted on the custom PCB placed in the oven (PCB 2 in Figure 4.2), which is connected to instrumentation outside the oven and to the other PCB (PCB 1 in Figure 4.2). Two separate PCB’s are employed to keep a minimum number of electronics components on PCB 2, since any component on PCB 2 must withstand the wide temperature range to test the sensors. Components operational over the oven temperature range can be found, but very few components are specified for cryogenic temperatures and the setup is reused for the cryogenic measurement described in section 4.2. Because the temperature of the air inside the oven will fluctuate by some tenths of a degree, this PCB is mounted on a large aluminium block in thermal contact with the DUT’s to maintain a stable DUT temperature. The large thermal mass of the metal block acts as a thermal low-pass filter which attenuates the temperature fluctuation in the oven to milli-Kelvin level [4.1]. A calibrated PT-100 sensor is placed inside the metal block and its resistance is used to measure the temperature of the DUT’s. A thermal rubber is placed between the DUT’s and the metal block to ensure good thermal contact between the DUT’s and aluminium block. Because of the large mass, 2-3 hours are required for the block to stabilize at the desired temperature. Thus, to speed-up the measurements, multiple DUT’s are placed on PCB 2 for simultaneous characterization. Figure 55 shows a cross section of the mounting of the DUT’s on the aluminium block.

![Diagram of test set-up](image-url)
An Altera Cyclone IV FPGA development board was used to generate the digital control signals. A 24 MHz clock on the FPGA board is used as the master clock from which a 100-kHz clock is generated. The 100-kHz clock is used as the clock signal (CLK) for the shift registers in the DUT. The digital inputs (DIN) and the load signal (LOAD) for the shift registers in the chips are all referenced to this 100 kHz clock. All DUT’s on PCB 2 share the same digital control signals (CLK, DIN, and LOAD). PCB 1 contains IC’s such as the digital isolator, level shifter and the low drop-out regulator and is placed outside the oven because these IC’s are designed to work only in a limited temperature range. The digital signals from the FPGA are first passed through a digital isolator so that the noise from the FPGA does not couple into the DUT’s. A level shifter is used to convert signals from the 3.3-V FPGA levels to 1.8-V levels which is compatible with the DUT’s. As was mentioned in the design chapter, an external operational amplifier is also placed on the board as a fail-safe mechanism, to be used in case the internal amplifier fails at low temperatures. The analog, digital and the external amplifier supplies are generated from a 5 V external supply using a low drop-out output regulator. The generated analog and digital supplies are both 1.8 V while the supply for the external amplifier is 3.3 V.

The DUT outputs, $V_{BE1}$ and $V_{BE2}$, are buffered with amplifiers so that they can drive the load of the measurement equipment. A Keithley 2400 multi-meter is used to read these voltages and the resistance of the Pt-100 sensor. Since the DUT’s are measured simultaneously, a scan card is used with the Keithley 2400 multi-meter to multiplex the DUT’s outputs to the multimeter input. The oven, the Cyclone IV FPGA and the Keithley 2400 multi-meter are all controlled and synchronized by a LabVIEW program running on a PC.
4.2 Test Set-up for Cryogenic Measurements

The test set-up for the measurements at cryogenic temperatures was very similar to the set-up used for the measurements in the oven. In this case, the oven was replaced by a Dewar flask filled with liquid nitrogen, in order to measure the DUT’s at the temperature of liquid nitrogen (77K). As was done with the measurements in the oven, the DUT’s were placed on a custom made PCB (same PCB used for the oven measurements) which was then attached to the aluminium block. This was then placed in the Dewar flask before being filled with liquid nitrogen. A PT-102 sensor which is calibrated to 14K was placed in the aluminium block and used as the reference sensor [4.3]. The same FPGA control was used for this measurement and a Keithley 2400 was used to read out the base-emitter voltages just as for the oven measurements.

4.2.1 Summary of the Measurement Procedure for Cryogenic Measurements

- Attach the PCB containing the DUTs to the metal block (See Figure 55 and Figure 57)
- Place the calibrated platinum sensor in the metal block (See Figure 55 and Figure 57)
- Connect the Platinum sensor to a Keithley in a 4-wire configuration
- Use Labview to convert the resistance of the platinum sensor to temperature [see 4.3]
- Transfer this setup into the Dewar flask i.e. metal block and PCB (See Figure 58)
- Check the setup if everything works i.e. do a room temperature measurement
- If satisfied with previous step, transfer the liquid nitrogen from the sealed cryo-vessel into the Dewar flask until almost full or at least well above the metal block (See Figure 59)
- Monitor the temperature of the metal block through the resistance of the calibrated platinum sensor
- Allow the resistance (temperature) to stabilize at the temperature of liquid nitrogen (77 K). This would take few minutes
- Measurements can now begin
Figure 56 Dewar flask used for the cryogenic measurements

Figure 57 The set-up of the metal block and the PCB
Figure 58 Picture of the set-up inside the Dewar flask

Figure 59 Picture of the vessel containing the liquid nitrogen
4.4.2 Deductions from Cryogenic Measurements

After performing the cryogenic measurements, we can make the following inferences

- The PCB survived at 77 K and was functional after warming up to room temperature
- Normal twisted pair wires work at 77 K and were functional after warming up to room temperatures
- The chip that were functional at 77 K were also functional at room temperature

4.3 Issues

A major issue that was encountered during the course of this measurements was device breakdown. This was associated with the fact that the electrostatic discharge (ESD) protection on the pads connected to the VBE voltages were removed during the layout to prevent leakage current. It was also noticed that the ESD protection was inadvertently removed on all the analog pads of the chip. This led to the breakdown of many of the devices. Therefore, only 4 devices were characterized in this measurement.

4.4 Measurement Results

As discussed in chapter 3, techniques such as dynamic element matching, current-gain compensation and chopping of the bipolar transistors in the bipolar core have been used in the design of the temperature sensor. Therefore, we need to take into account these techniques during the measurements. In all the measurements performed, current gain compensation was used. Measurements was done by using the settings of the dynamic element matching circuit and of the chopping of the bipolar transistors. A total of 24 different settings were used, with the two base-emitter voltages measured for each setting. Measurements were carried out at the following temperatures: 30°C, 10°C, -10°C, -30°C, -50°C, and -65°C. All the devices that were measured worked and performed as expected within the temperature range of−65 °C to 30 °C. However, only 3 of the devices worked at the temperature of liquid nitrogen. The results of these measurements are shown and discussed in this section.

4.4.1 DEM Settings

This section discusses the procedure for choosing the dynamic element matching (DEM) configurations. As was discussed in chapter 3, the 2 bipolar transistors in the bipolar core are
biased with a 1:5 current ratio. The bipolar transistors can also be chopped in the current domain to obtain a 5:1 current ratio. Therefore, we have two phases in which dynamic element matching can be performed. One with a 1:5 current ratio (Phase A) and the other with a 5:1 current ratio (Phase B). A 1:5 current ratio gives a total of 6 clock cycles for the DEM configurations. However, due to the introduction of the bank swap mechanism, the number of configurations becomes doubled i.e. 12 in each phase. Therefore, in the two DEM phases we have a total of 24 DEM configurations. The sequence of controlling the switches for each DEM setting is shown in the Table 4.

![Diagram](image)

*Figure 60 Overview circuit of the sensor*

<table>
<thead>
<tr>
<th>Table 4 24 DEM settings</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Setting</strong></td>
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<tr>
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<td>10</td>
</tr>
<tr>
<td>11</td>
</tr>
<tr>
<td>12</td>
</tr>
</tbody>
</table>
S1 – S6 and S’1 – S’6 are the switches of the two banks. The emitter-base voltages were measured using these 24 settings and the results are shown in the following sections.

### 4.4.1 VBE’s and ΔVBE’s over temperature

Figure 61 and 62 shows the plot of the base-emitter voltages and the ΔVBE voltages measured for the 4 chips over the temperature range from $-65 \degree C$ to $30 \degree C$.

![VBE VS TEMPERATURE](image)

*Figure 61 The emitter-base voltages of the 4 chips over temperature*

The plot of the average VBE2 and VBE1 is shown Fig 62

![VBE VS TEMPERATURE](image)

*Figure 62 Average VBE’s of the 4 chips over temperature*
Using MATLAB, the slope of the average VBE1 and VBE2 line was calculated as -1.9 mV/°C and -2 mV/°C respectively which matches with the widely known VBE sensitivity of -2 mV/°C. A probable reason why the sensitivity of VBE1 is not exactly -2 mV/°C could be because the measurement was performed over a narrow temperature range of −65 °C to 30 °C.

Figure 63 shows the plot of the ΔVBE voltage over the temperature range of −65 °C to 30 °C.

![ΔVBE vs Temperature](image1)

**Figure 63** The ΔV<sub>BE</sub> voltage of the 4 chips over temperature

Figure 64 shows the plot of the average ΔVBE voltage over the temperature range of −65 °C to 30 °C.

![DVBE_avg](image2)

**Figure 64** Average ΔV<sub>BE</sub> voltage of the 4 chips over temperature
Using MATLAB, the slope of the average $\Delta V_{BE}$ line was calculated as 139.1 $\mu V/\degree C$. This matches closely with calculated sensitivity of $\Delta V_{BE}$ given as $\frac{d\Delta V_{BE}}{dT} = \frac{k}{m} \ln m$, and with $m = 5$, $\frac{d\Delta V_{BE}}{dT} = 138.9 \mu V/\degree C$.

Figure 65 and 66 shows a plot of the VBE voltages and the $\Delta V_{BE}$ voltages after the measurement at liquid nitrogen is added to the plot. It should be noted that only measurements from the 3 devices that worked at 77K are used in this plots.

![VBE VS TEMPERATURE](image1)

*Figure 65 The emitter-base voltage of the 3 chips over temperature*

![VBE VS TEMPERATURE](image2)

*Figure 66 Linear curve fitting of the VBE voltages*
The linear curve fitting of the average VBE lines seem to show the well reported curvature at low temperatures [4.4]. This assertion needs to be confirmed by doing a full temperature sweep at cryogenic temperatures.

![AVBE VS TEMPERATURE](image)

*Figure 67 The ΔV_{BE} voltage of 3 chips over temperature*

Figure 67 shows that the ΔVBE voltage of the 3 chips maintains the expected linear relation with temperature at 77 K.

### 4.4.2 Spreads in ΔVBE

The ΔVBE voltage has a linear relation with temperature and is therefore a good measure of temperature. In this section, the results obtained for the spread in the ΔVBE voltage for different configurations are given.

#### 1. Spread in Phase A

As was stated earlier, the 2 base-emitter voltages were measured over different settings. This section gives the spread obtained in the settings with a 1:5 current ratio. Figure 68 shows the plot of the spread in a typical setting in this phase.
From the measurements, it was observed that using a single setting in this phase gives a maximum spread of about 1 mV within the temperature range of $-65 \, ^\circ C$ to $30 \, ^\circ C$ and a maximum spread of 2.5 mV at 77 K. This spread can be greatly reduced by averaging over the 12 DEM settings in this phase. Figure 69 shows the plot of the average spread over all the 12 settings in this phase.
The effect of dynamic element matching explained in chapter 3 can be clearly noticed in figure 4.21 as the maximum spread reduces to about 80 µV in the temperature range of $-65 \degree C$ to $30 \degree C$ and 20 µV at 77 K after averaging over the 12 settings in this phase.

2. Spread in Phase B

This section gives the spread in each settings after current chopping for a 5:1 current ratio. The plot of the typical spread in an individual setting in this phase is shown in Figure 70. From the measurements, it was noticed that using a single setting in this phase gives a maximum spread of about 1 mV within the temperature range of $-65 \degree C$ to $30 \degree C$ and a maximum spread of 2.5 mV at 77 K.

![SPREAD IN ΔVBE](image)

*Figure 70 Plot of a typical spread of an individual setting in ΔVBE over temperature in phase B*

This spread can be greatly reduced by averaging over the 12 DEM settings in this phase. Figure 71 shows the plot of the average spread over all the 12 settings in this phase.
The effect of averaging can be clearly seen in Figure 71 as the maximum spread reduces to about 100 μV in the temperature range of −65 °C to 30 °C and about 37 μV at 77 K after averaging over the 12 settings in this phase. It can be noticed that the maximum spread in this phase is relatively higher than in phase A. One reason proposed for this could be due to the charge injection from the switches during the current chopping.

3. Total spread over all settings

Figure 72 shows the plot of the average spread in the ΔVBE voltage over all the 24 settings used in measuring the VBE voltages.
The overall effect of dynamic element matching can be seen in Figure 72 which shows the spread over the 24 DEM settings. This is in effect the average of the spread in the two DEM phases and results in a better spread than the average spread in each of them. A maximum spread of about 55 μV in the temperature range of −65 °C to 30 °C and about 23 μV at 77 K was obtained.

A point of note is that these measurements appear to be noisy. One reason for this is the noise associated with the measurement instrument. Buffer amplifiers were used to decouple the instrument from the DUT’s. Averaging within the instrument was also used to reduce the noise associated with the measurements. This procedures only work to an extent. It would be suggested that further improvements on this work should employ a digital output so as to obtain the desired resolution.

4.5 Temperature Error

As described in chapter 1, smart temperature sensors usually incorporate an analog to digital converter (ADC) to obtain a digital temperature reading. Figure 73 shows a diagrammatic description of such smart sensor.

Figure 73 Operating principle of a smart temperature sensor [4.4]

The ADC takes a voltage $V_{PTAT} = \alpha * \Delta V_{BE}$ as input and a temperature independent voltage $V_{REF}$ as reference.

$$V_{REF} = V_{BE} + \alpha * \Delta V_{BE} \quad (4.1)$$

where $\alpha$ is the gain factor chosen in such that the temperature coefficient of $V_{BE}$ and $\alpha \Delta V_{BE}$ have an equal magnitude and opposite sign i.e.

$$-\frac{\partial V_{BE}}{\partial T} = \frac{\alpha \partial V_{BE}}{\partial T} \quad (4.2)$$
Therefore,

$$\alpha = -\frac{\partial V_{BE}}{\partial T} \cdot \frac{q}{klnp} \quad (4.3)$$

The digital output of the ADC, $\mu$ is then

$$\mu = \frac{V_{PTAT}}{V_{REF}} = \frac{\alpha \cdot \Delta V_{BE}}{V_{BE} + \alpha \cdot \Delta V_{BE}} \quad (4.4)$$

To calculate $\alpha$, the slope of VBE and $\Delta VBE$ obtained in section 4.4.1 was used. The slope of VBE2 was given as -1.9 mV/°C while the slope of $\Delta VBE$ was given as 139.1 μV/°C. Using equation 4.3 we obtain a $\alpha$ of about 13.7. This is relatively low in comparison with the value of $\alpha$ obtained for BJTs in this process [4.4]. A probable reason for this could be because this measurement was carried out over a narrow temperature range of $-65 \degree C$ to $30 \degree C$ while $\alpha$ in [4.4] was obtained over the full temperature range of $-55 \degree C$ to $125 \degree C$. Figure 74 shows the plot of the average $V_{REF}$, $V_{BE}$ and VPAT of the chips over temperature.

![VPTAT, VBE, VREF VS TEMP.](image)

*Figure 74 Plot of VPAT, VBE and VREF vs Temperature*

The deviation from the straight line of $V_{REF}$ in Figure 4.26 at low temperature can be associated to the curvature of VBE at very low temperatures.

Figure 75 shows the plot of the output of the ADC obtained from equation 4.4.
The spread in $\mu$ is shown in Figure 76. One observation from the plot of Figure 76 is that the maximum spread in $\mu$ is obtained in Chip 2 is relatively higher than others. It should be noted that Chip 2 is the chip that doesn’t operate at 77 K. Therefore, the hypothesis at the moment is that this chip shows this large spread because it is perhaps faulty.
A 1-point trim can be performed on the plot of Fig 77 to reduce the temperature error. Figure 78 and Figure 79 show the plots of the temperature error after 1-point trimming at 30 °C and -30 °C respectively.
4.6 Performance Summary

In this section, a summary of the performance obtained from the measurements is given. The table below shows the summary.

Table 5 Performance summary

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<thead>
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<th>Parameter</th>
<th>Value</th>
<th>Conditions</th>
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<td>CMOS Technology</td>
<td>0.16 μm</td>
<td></td>
</tr>
<tr>
<td>Inaccuracy</td>
<td>±0.25 °C @ −</td>
<td>1-point trim</td>
</tr>
<tr>
<td></td>
<td>65 °C to 30 °C; ± 0.15 °C @ − 196 °C</td>
<td></td>
</tr>
<tr>
<td>Temperature range</td>
<td>−196 °C and −65 °C to 30 °C</td>
<td></td>
</tr>
<tr>
<td>Supply voltage</td>
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</tr>
<tr>
<td>Supply current</td>
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</tr>
<tr>
<td>Power consumption</td>
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<td></td>
</tr>
<tr>
<td>Chip area</td>
<td>0.68 mm²</td>
<td>Including padring</td>
</tr>
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</table>
4.7 Comparison with prior art

In this section, this work is compared with prior work demonstrating a cryogenic CMOS temperature sensor using BJT as sensing elements. The comparison is given in the table below.

Table 6 Comparison with prior art

<table>
<thead>
<tr>
<th>Parameter</th>
<th>This Work</th>
<th>[4.2]</th>
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<td>Sensor type</td>
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<td>BJT</td>
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<td>CMOS Technology</td>
<td>0.16 μm</td>
<td>130 nm</td>
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<tr>
<td>Inaccuracy</td>
<td>0.25 °C @ −65 °C to 30 °C; 0.15 °C @ −196 °C</td>
<td>1 °C</td>
</tr>
<tr>
<td>Temperature range</td>
<td>−196 °C and −65 °C to 30 °C</td>
<td>−180 °C to 0 °C</td>
</tr>
<tr>
<td>Supply voltage</td>
<td>1.8 V</td>
<td>1.2-1.3 V</td>
</tr>
<tr>
<td>Supply current</td>
<td>4.22 μA</td>
<td></td>
</tr>
<tr>
<td>Power consumption</td>
<td>7.59 μW</td>
<td>1 μW</td>
</tr>
<tr>
<td>Chip area</td>
<td>0.68 mm²</td>
<td>0.13 mm²</td>
</tr>
</tbody>
</table>

The result obtained shows an order of magnitude improvement at 77 K compared to a previous work on cryogenic CMOS temperature sensor based on bipolar transistors [4.2].

4.8 Conclusion

In this chapter, an overview of the measurement test set-up used for the characterization of the cryogenic sensor and the results obtained have been given. It was shown that the use of dynamic element matching and current chopping in this sensor greatly improves the accuracy of the sensor. A temperature inaccuracy of 0.25 °C was obtained in the temperature range of −65 °C to 30 °C while an inaccuracy of 0.15 °C was obtained at 77K.
4.9 References


5

Conclusion and Recommendations

This chapter gives the main conclusion of this work. Recommendations for further improvements of this work are also highlighted.

5.1 Conclusion

Temperature sensors for cryogenic temperatures have a wide range of applications. Such applications include Cryosurgery, quantum computing, deep-space probes and planetary missions, satellite communications systems and space-based radar. Conventional temperature sensors can achieve high accuracy (better than 0.1 K) but at the cost of expensive calibration. Their analog nature also mean they are very prone to interference. Those disadvantages can be overcome by CMOS integrated cryogenic temperature sensors.

In this work, a CMOS cryogenic temperature sensor based on bipolar transistors was designed. The sensor was fabricated and tested both within the military temperature range (-65 °C – 30 °C) and at 77 K (-196 °C). Measurement results show that the sensor worked at 77 K (-196 °C). A temperature inaccuracy of ±0.25°C was obtained in the temperature range of -65 °C to 30 °C while an inaccuracy of ±0.15°C was obtained at 77K. The result obtained shows an order of magnitude improvement at 77 K compared to a previous work on cryogenic CMOS temperature sensor based on bipolar transistors [5.1].

5.2 Recommendations

In this section, some recommendations on certain improvements which can be made regarding this work is given.

5.2.1 Design Improvements

Some improvements can be made in the design of this temperature sensor. Some of those improvements are highlighted below.
1. For this temperature sensor to be considered as a smart sensor, an analog to digital converter (ADC) needs to be added to the designed CMOS sensing core. As was noticed during the measurement, the analog nature of the sensor outputs means that they are prone to interference which can perturb the measurement results. This can be overcome by having a digital output from an analog to digital converter.

2. The ESD protection on the chip should be returned. Since this sensor is meant to be operated at cryogenic temperatures, leakage currents at this temperatures are negligible. Therefore, removing the ESD protections becomes unnecessary especially with the addition of an analog to digital converter.

3. Efforts need to be made in making device models at cryogenic temperatures. This would aid in both designing and confirming the results obtained at these temperatures.

5.2.2 Measurement Improvements

This sensor was characterized at cryogenic temperature (77 K) by using a custom-made measurement set-up. Efforts need to be made to characterize this sensor by performing a full cryogenic temperature sweep in a standard cryogenic chamber so as to determine the full functionality of this sensor at cryogenic temperatures.

5.3 References