

Frequency-Locked Turnstile Device for Single Electrons

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We have fabricated an array of ultras-small tunnel junctions which acts like a turnstile for single electrons. When alternating voltage of frequency f is applied to a gate, one electron is transferred per cycle through the device. This results in a current plateau in the current-voltage characteristic at $I=ef$. The overall behavior of the device is well explained by the theory of Coulomb blockade of electron tunneling. We discuss the accuracy limitations of this device.

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With present-day lithographic techniques it has become possible to fabricate tunnel junctions with capacitance C small enough to make the charging energy of a single electron, $E_C=e^2/2C$, much larger than thermal energies at dilution refrigerator temperatures. Typical capacitances are below 10^{-15} F for junction areas below $(100\text{ nm})^2$; hence $E_C/k_B > 1$ K. Under this condition the discreteness of electron tunneling leads to new phenomena, charging effects, as reviewed by Averin and Likharev.¹ In a pioneering paper, Fulton and Dolan² confirmed experimentally the existence of charging effects in small circuits of planar tunnel junctions. In linear arrays of small tunnel junctions charge is transferred by mutually repulsing charge solitons,³ resulting in time-correlated tunneling events with fundamental frequency I/e . Delsing *et al.*⁴ demonstrated this effect by application of a signal with frequency f , leading to resonances at current levels $I=ef$ and $2ef$. The resonances show up in the differential resistance only. In this paper, we present a new device in which a single electron is transferred per cycle of an externally applied rf signal. In this voltage-biased device a current flows which is equal to the frequency times the electron charge. The device is based on a turnstile effect resulting from the Coulomb blockade in linear arrays of tunnel junctions. It opens the possibility of a high-accuracy, frequency-determined current standard. In many respects resembling a single-electron-shift register, the device exemplifies the prospects of using charging effects for practical logic circuits.⁵

The Coulomb blockade of single-electron tunneling manifests itself in voltage-biased linear arrays as a voltage gap in their current-voltage (I - V) characteristic. This Coulomb gap arises because an electron has to occupy intermediate positions on the metal "islands" between the junctions to transfer through the array. For bias voltages well below e/C (C being the junction capacitance) the energy of these intermediate states is higher than the energy of the initial state. Conduction is

thus energetically suppressed. Consider the energy of a device constructed, as in our experiment, of both tunnel junctions and true capacitors, biased from several voltage sources. The energy associated with a given electron position is the sum of the capacitive energy for the resulting charge distribution and the work performed by the bias-voltage sources.³ If, under the influence of particular bias conditions, the absolute value of the charge on a junction of the array exceeds a critical charge, an electron can tunnel across this junction. The difference ΔE_k between the final and initial energy for the tunnel event across junction k of the array can be expressed as

$$\Delta E_k = -e(|Q_k| - Q_{ck})/C_k, \quad (1)$$

where Q_k and C_k are the charge and capacitance of junction k , respectively. The critical charge $Q_{ck} = e/2(1 + C_{ek}/C_k)$ depends, apart from the junction capacitance, only on the equivalent capacitance C_{ek} of the circuit in parallel with junction k . With this concept of a critical charge Q_c the principle of the present experiment can be understood. It is illustrated in Fig. 1. A linear array of four junctions of capacitance C is biased by a drive voltage V , which is applied symmetric to ground. The central island, between junctions 2 and 3, is capacitively coupled to a gate voltage V_g .^{2,5} If the gate capacitor C_g is chosen to equal $C/2$, all junctions have the same critical charge for tunneling, $Q_c = e/3$. For V and V_g within a certain window, the critical charge will be exceeded for the junctions in the left arm, but not for the junctions in the right arm. Once an elementary charge has entered the central island, part of it will polarize the gate capacitor, and the charge on all junctions will be lower than the critical charge. Therefore, the elementary charge is trapped on the central island until bias conditions are changed. It is also impossible for another charge to move to the central island. To make the charge leave by the right arm, the gate voltage is decreased. The junctions on the right arm will first exceed the critical charge because of the asymmetry caused by

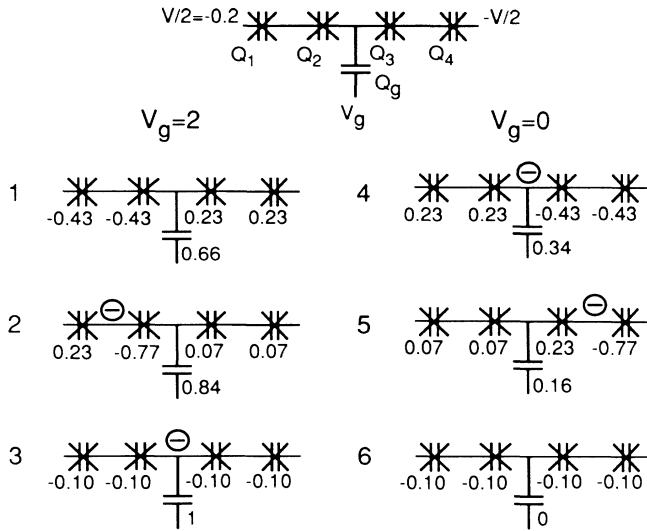


FIG. 1. Principle of controlled single-electron transfer through a linear array of small tunnel junctions. Junctions, with capacitance C , are denoted by crossed capacitor symbols, the gate voltage V_g is applied via a true (nontunneling) capacitance C_g . If $C_g = C/2$, tunneling across any junction can only occur if for that junction $|Q| > Q_c$, with $Q_c = e/3$. The voltages and charges are indicated in units of e/C and e . 1-6 indicate consecutive times in the cycle. Left: First half of the cycle, $V_g = 2$. An elementary charge (in the circles) ends up trapped on the central electrode. Right: Second half of the cycle, $V_g = 0$. The charge can only leave on the right-hand side. No further tunneling can occur in the emptied array.

the bias voltage. Cyclically changing the bias conditions by applying an alternating voltage in addition to a dc voltage to the gate capacitor moves one electron per cycle through the chain. We emphasize that after an arbitrary long time, the total charge transferred will be known to within a single electron. The principle will work for a general T-shaped structure of $2n$ junctions with a gate capacitance of about C/n . However, at least two junctions on each side are needed to avoid the unwanted entering or leaving of a charge.

We will discuss why the stochastic nature of electron tunneling need not perturb the deterministic transfer of electrons through the device. At finite temperature T the tunneling rate is for arbitrary ΔE given by¹

$$\Gamma = \frac{\Delta E/2E_C}{RC[\exp(\Delta E/k_B T) - 1]}, \quad (2)$$

where R is the tunneling resistance of the junction. This shows the two main prerequisites for deterministic electron transfer. The ac cycle should last long enough to let tunneling to and from the central island happen with high probability; i.e., f must be much smaller than $(RC)^{-1}$ to avoid cycles being lost. On the other hand, an electron trapped on the central electrode should have a negligible probability to escape by a thermally assisted transfer. At finite temperature there is a tradeoff be-

tween the two requirements: A thermally assisted escape will be more probable for lower frequencies. We will discuss the consequences of these limitations more quantitatively below. Finally, we note that Eq. (2) is strictly valid only for negligible tunnel conductance. Quantum charge fluctuations associated with a tunnel resistance not much larger than h/e^2 (Refs. 6 and 7) generally suppress the charging effects. We have not investigated the consequences of this aspect for the present experiment.

The physical layout of the device is very close to the circuit shown in Fig. 1, with four junctions of about 0.5 fF and $340 \text{ k}\Omega$ [$(RC)^{-1} \approx 5 \text{ GHz}$] and a gate capacitance C_g of 0.3 fF. The values of R and C were determined from the large-scale I - V curve,⁶ and C_g was determined from the period of the current modulation by the gate voltage. This period ΔV_g yields the gate capacitance as $C_g = e/\Delta V_g$. An important refinement over the circuit of Fig. 1 is the use of two small auxiliary gate capacitances (0.06 fF) to tune out noninteger trapped charges⁵ on the remaining two islands. This device was fabricated with nanolithographic methods, as described elsewhere,⁶ with planar aluminum-aluminum-oxide-aluminum junctions. It was thermally anchored to the mixing chamber of a dilution refrigerator, and a magnetic field of 2 T was applied to bring the junctions into the normal (i.e., nonsuperconducting) state. All leads were low-pass filtered by a stage which was also thermally anchored to the mixing chamber. In addition, the gate voltages were strongly attenuated. The gate voltages were applied by room-temperature dc voltage sources referenced to cryostat ground. In addition, an ac voltage could be applied to the central gate capacitor. The voltage bias was symmetric with respect to cryostat ground. The measurement was performed with a two-wire method: A field-effect-transistor-operational-amplifier circuit with virtually shorted input terminals, in series with voltage source and sample, was used to measure the current.

Figure 2 shows I - V curves of the device, without ac gate voltage applied (dotted curve) and with ac gate voltage of different frequencies between 4 and 20 MHz. Without ac gate voltage, a large zero-current Coulomb gap is present. With ac gate voltage of frequency f , wide current plateaus develop inside the Coulomb gap at a current level $I = ef$. The plateaus even extend to voltages outside the gap. In Fig. 2 the dc gate voltages were the same for each curve and the ac amplitude was adjusted for the widest plateau, which required more power at higher frequencies. Thermometer temperature varied from 10 to 40 mK, depending on applied ac power. Good plateaus were observed up to 40 MHz, but only for frequencies below about 10 MHz were part of the plateaus flat within experimental current noise (about 0.05 pA, dc to 1 Hz). Figure 3 shows the dependence of the I - V curve on ac amplitude at a frequency of 5 MHz. Clearly, the height of the plateaus is not dependent on

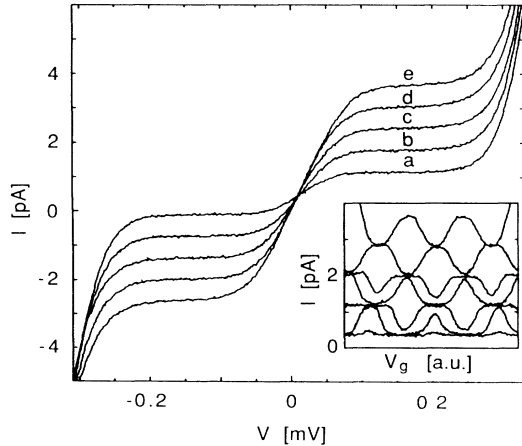


FIG. 2. Current-voltage characteristics without ac gate voltage (dotted curve) and with applied ac gate voltage at frequencies f from 4 to 20 MHz in 4-MHz steps (a-e). Current plateaus are seen at $I = ef$. Inset: Current vs dc-gate-voltage characteristics for $f = 5$ MHz. The curves tend to be confined between levels at $I = nef$ and $(n+1)ef$, with n an integer. The bias voltage was fixed at 0.15 mV. For the bottom curve, which is nearly flat, the ac-gate-voltage amplitude is 0. For the other curves the calculated ac amplitude at the sample increases from $0.60e/C$ for the lowest one to $3.4e/C$ for the upper one, where $e/C = 0.30$ mV.

the ac amplitude, although the width is. For high amplitudes, we have observed a tendency to form plateaus at $I = 2ef$. Another sample with $n = 3$ junctions in each arm showed the same behavior, although with somewhat rounded plateaus. We attribute this rounding to the larger capacitances (about 2 fF) of the junctions in this device.

A gate-voltage adjustment was necessary to obtain wide plateaus. A suitable procedure was to maximize the Coulomb gap without ac voltage, using the auxiliary gate voltages. Next, the current versus dc gate voltage would be recorded at fixed bias voltage, with ac gate voltage applied. This shows an oscillating behavior with minima and maxima at $I = ef$, $I = 2ef$, or even higher multiples, depending on the ac amplitude. An example is shown in the inset of Fig. 2. The I - V curves of Fig. 2 were obtained with dc gate voltage in the middle of a I - V_g plateau at $I = ef$, corresponding to half the elementary charge induced on the gate capacitor. When misadjusting both auxiliary gates on purpose, we could still obtain plateaus in the I - V curve, but not as wide as in Fig. 2.

The dependence of the I - V curves on ac amplitude, as shown in Fig. 3, is very well simulated by numerical calculations based on Eqs. (1) and (2). Results are shown in the same figure as dashed curves on the right of the measurements. No fitting parameters were used. The only adjustments made were assuming 1-dB attenuation in the ac voltage line to be present, in addition to the known attenuators, and introducing a higher tempera-

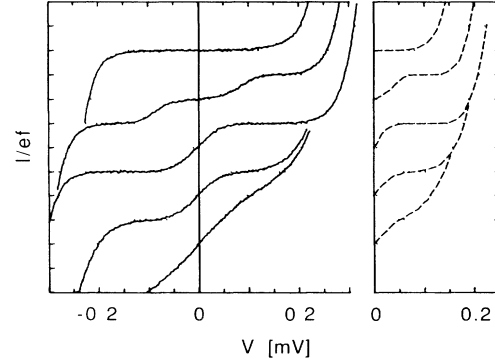


FIG. 3. Current-voltage characteristics at $f = 5$ MHz for different levels of applied ac gate voltage. The dotted horizontal lines are at intervals $ef = 0.80$ pA. The I - V curves have all been offset in the x direction by $15 \mu\text{V}$ to compensate for operational-amplifier voltage offset in the current measuring circuit and, individually, in the y direction to display them more clearly. From top to bottom the calculated ac voltage amplitudes at the sample are 0, 0.60, 0.95, 1.50, and 1.89, expressed in units of $e/C = 0.30$ mV. On the right, the corresponding simulated I - V curves are shown as dashed lines. For these calculations, 1 dB extra ac attenuation was assumed, and temperatures of 50 mK (upper three curves) and 75 mK (lower two) were used.

ture (50–75 mK) than the thermometer indicated during the experiments (10–20 mK) to roughly account for remaining noise or heating of the sample.

In Table I we compare the current step height I_s , obtained by taking half the measured current distance between the positive and the negative plateaus, with the prediction $I_s = ef$. Up to 10 MHz, regions could be found (around 0.15 meV) where the plateau was flat within the current noise. In those cases about fifty points were taken in the central parts of these regions to determine the average current with its standard deviation σ_m . Above 10 MHz, the current level at the inflection point was taken in a similar way. The measured current step coincides with ef within experimental accuracy, which is

TABLE I. Comparison of the measured current plateau I_s with the relation $I_s = ef$. σ_m is the standard deviation of I_s .

f (MHz)	I_s (fA)	σ_m (fA)	$ef - I_s$ (fA)
4.012	635	2	8
6.011	967	2	-4
8.031	1287	2	0
10.040	1610	2	-1
12.029	1930	2	-3
14.028	2243	2	5
16.026	2560	3	7
18.063	2890	3	4
20.011	3196	3	10
30.036	4856	3	-44

around 0.3%. We attribute the deviation of more than $3\sigma_m$ at 20 and 30 MHz to the difficulty of determining the inflection point. To discuss the expected intrinsic accuracy of the current step height, we return to the example shown in Fig. 1. For an electron transfer in the circuit shown in Fig. 1, the first tunnel event of each half of the cycle ($\Delta E = -0.1e^2/C$) can occur in two junctions with a rate $\Gamma = (10RC)^{-1}$. For a square-wave modulation this yields a probability to miss a cycle of about $\exp(-\Gamma/f) = \exp(-1/10fRC)$. For the device used in the experiments $(RC)^{-1} \approx 5$ GHz, so at 5 MHz this probability is $\exp(-100) \approx 10^{-44}$, while at 50 MHz it is already about 10^{-5} . Obviously, the required accuracy puts an upper limit to the allowed frequency. Next, to estimate the effect of thermal fluctuations, we compare the rate for unwanted tunneling events $\tilde{\Gamma}$ with the one for favorable events Γ . From Eq. (2) we find that the ratio is of order $\exp(-\Delta E/k_B T)$. For an accuracy of, e.g., 10^{-8} , it is necessary to have $\tilde{\Gamma}/\Gamma \approx 10^{-8}$, which, combined with the requirement $\Gamma/f = 10^3$, yields $\exp(-\Delta E/k_B T) = 10^{-11}$, or $k_B T \approx \Delta E/25$. Since typically ΔE is on the order of $0.1e^2/C$, for the present device this corresponds to temperatures of about 15 mK. Comparable problems with unwanted transitions could arise from insufficient screening from noise and interference in the experiments. The simulations in Fig. 3 suggest that in the present experiment these disturbances seem to be described well by a temperature of not more than 50 mK, which is already close to the temperature requirement derived above. More careful screening is possible. These limitations are relaxed by the use of smaller junctions. For junctions of 0.1 fF with the same resistance, the requirement that $f < 10^{-3}/RC$ corresponds to $f < 30$ MHz and $k_B T < 0.1e^2/C$ to $T < 75$ mK.

In conclusion, we have fabricated a device producing a current clocked by an externally applied high-frequency voltage. Charge transfer is controlled at the level of single electrons. The theoretical limitations on the accuracy are very promising. The good agreement between the I - V curves and the theory shows that the dc and ac behavior of small-capacitance, normal-metal tunnel junctions is well understood, and that device behavior can be reliably predicted.

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