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An integrated interface circuit with a capacitance-to-voltage converter as front-end for grounded capacitive sensors

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Abstract
This paper presents the analysis and design of an integrated interface for grounded capacitive sensors. To reduce the effects of parasitic cable capacitances, a feedforward technique has been applied. In combination with the use of a special front-end amplifier this yields high immunity for a parasitic cable capacitance. The major nonidealities of the interface circuit have been analyzed. The complete interface has been designed and implemented as an integrated circuit, using standard 0.7 μm CMOS technology. Experimental results, which are in good agreement with theoretical analysis and simulation, show that for sensor capacitance down to 10 pF, shielded connection cables up to 30 m can be handled with an absolute error of less than 0.3 pF. The measured nonlinearity of the interface amounts to about $3 \times 10^{-4}$ for 30 m of the cable. For 40 ms measurement time, the resolution amounts to about 16 bits.

Keywords: active shielding, capacitance-to-voltage converter, capacitive sensor, integrated interface

1. Introduction
Capacitive sensors are widely applied in, for instance, liquid-level gauges, pressure meters, accelerometers and mechanical high-precision positioners. In such applications, physical or mechanical quantities are converted into capacitance values, which are further processed by an electronic circuit, the modifier. Often, capacitive sensor elements are connected to the electronic interface circuitry with long wires of cables. To reduce the effects of interference, these connecting wires or cables are shielded. Provisions have to be taken to avoid the parasitic capacitances of these cables forming direct shunting components for the sensing elements because without such provisions any changes in these parasitic capacitances would seriously degrade the sensor-system performance.

When the capacitive sensor elements are floating, i.e. when none of the terminals has been connected to the ground, then they can be read by interface circuits that are intrinsically immune to stray capacitances to the ground [1]. Also it is possible to do two-step measurements in order to extract the value of a floating capacitance independent of the parasitic capacitance to the ground [2]. However, safety reasons and/or operating limitations might require that one of the electrodes of the sensing elements be grounded. This is the case, for instance, with level measurement of a conductive liquid in a grounded metallic container with a capacitive sensor [3, 4].

For grounded capacitive sensors, a usual way to reduce the effects of shunting parasitic capacitances is to apply active shielding (figure 1) [1]. In figure 1, $C_{p1}$ and $C_{p2}$ represent the capacitance between the core conductors of the coaxial cable with its shield and the capacitance of the shield to the ground, respectively.

There is a trade-off between the accuracy and the stability of this system. Especially, when the values of parasitic capacitances are not known or can vary over a wide range, it is difficult to optimize the system for its performance [5]. To solve this problem, in a recent publication [6], a novel interface has been introduced in which active shields have been
connected to a buffer voltage while using feedforward instead of feedback. It has been shown that with this technique there will not be any instability problems and there will be more design freedom to increase the accuracy.

However, the circuit described in [6] has been implemented with discrete components, and the capacitive sensing elements are directly connected to a capacitance-to-time converter. In the present paper, we will show that the use of a capacitance-to-voltage converter as front-end will significantly improve the system performance. The major nonidealities of the interface system will be discussed together with methods for reducing their influence. An integrated version of the improved interface for grounded capacitive sensor with feedforward-based active shielding will be presented. In order to reduce the effect of any low-frequency disturbing signals, including flicker noise, interference from the mains, and offset, the interface is equipped with a special kind of chopper, according to the (+ − − +) principle described in [7, 8]. Moreover, to remove any additive and multiplicative errors, which are mainly caused by uncertainty in design parameters and thermal drift, a three-signal auto-calibration technique [7] has been used. The interface has been designed and implemented using 0.7 μm standard CMOS technology. The experimental results are presented in section 4. As compared to previous work [6], these results demonstrate a significant improvement in immunity for parasitic capacitances, and a higher flexibility in adapting the front end to the maximum value of sensor capacitances.

2. System setup and front-end circuit

Figure 2(a) shows the complete setup, which consists of a multiplexer, a new capacitance-to-voltage converter, a voltage-to-period converter [6, 7] and a control unit. The output signal is shown in figure 2(b). According to the use of the three-signal auto-calibration technique [8], one measurement cycle consists of three phases in which a first reference capacitor Cref 1, a second reference capacitor Cref 2 and the sensor capacitor Cx are measured, respectively. Their values are linearly converted to the time domain and result in corresponding time periods Tref 1, Tref 2 and Tx of the output signal. For identification purposes, the time interval Tref 1 is split into two short periods [8]. For the three time intervals it holds that

\[ T_{ref1} = aC_{ref1} + b, \]  

\[ T_{ref2} = aC_{ref2} + b, \]  

\[ T_x = aC_x + b, \]  

where a and b represent the multiplicative and additive parameters of the capacitance-to-time converter. After measuring the length of the different periods with a microcontroller, the value of a parameter M is calculated using the equation

\[ M = \frac{T_x - T_{ref1}}{T_{ref2} - T_{ref1}} = \frac{C_x - C_{ref1}}{C_{ref2} - C_{ref1}}. \]  

From this value and supposing that the values of Cref 1 and Cref 2 are known, the input capacitance Cx can be extracted. From equation (4) it can be concluded that M and therefore also the measured value of Cx, are independent of a and b. Therefore, the measurement result is independent of any changes of the additive and multiplicative parameters of the interface circuit, as can be caused by process spread, temperature, and so on.

To get a good resolution, the difference (Cref 2 − Cref 1) between the values of the reference capacitors should be large enough. On the other hand, as will be explained in section 3.3, the values of Cref 1 and Cref 2 should be chosen in such a way that the interface circuit will work in its linear region.

Figure 3(a) shows the capacitor-to-voltage converter, for the case that the sensor capacitor Cx is selected. The switch pairs, (S1, S2), (S2, S4) and (S2, S3), all work in a break-before-make mode. This will guarantee that no charge is lost at the negative input of the amplifier. To understand how this SC circuit works, we first suppose that the cable capacitances C p1 and C p2 are zero and that the amplifier A1 and the switches are ideal.

During time interval T ref 1 (figure 3(b)), S1 is ON which sets V out to V dd /2. At the same time, via S3, the top electrode of the sensor capacitance C x is connected to the ground. During time interval T x, C x is connected to the negative input of the
amplifier. As a consequence, a charge $C_x V_{dd}/2$ will be pumped to $C_f$, which results in a jump $C_x V_{dd}/2C_f$ of the output voltage $V_{out}$. In a similar way, for the other time intervals, the value of $V_{out}$ can be found, as depicted in figure 3(b).

In the setup of figure 3(a), the excitation voltage for the capacitor $C_x$ can have one of three well-known values: 0 V, $V_{dd}$ and $V_{dd}/2$. Knowing this in advance, without using feedback, we can apply the same voltage to the shielding conductor. In this way, the effect of cable parasitic capacitances can be eliminated without having instability problem.

In our design, we need to cover sensor capacitances up to 330 pF. In such a case $C_f$ will be too big to be integrated. Therefore, for the capacitor $C_f$ we used an off-chip component. The value of this capacitor can be optimized to obtain the maximum output swing of the amplifier for the maximum value of $C_x$. Next, the following stage, the voltage-to-period converter, can be optimized independently of the sensor-capitance range. This also allows the end user to optimize the system performance for his specific application.

3. Effects of component imperfections

The major nonidealities are the amplifier offset, the switch-charge injection and the switch ON resistance. In this section the influence of these nonidealities will be discussed.

3.1. The offset

Figure 4(a) shows the front-end circuit for the case that the sensor-cable shield (point B) is driven with the same voltage as the cable core (point A). If we suppose that the switches and the voltage source are ideal, then $C_{Q2}$ cannot play any role.

The main objective of active shielding is keeping the voltage across $C_p1$ at zero, but when $\phi 2$ is high, the voltage across $C_p1$ equals the input offset voltage $v_{io}$ of the amplifier. The effect of this offset voltage is eliminated by the applied chopper, as will be shown now:

During time interval $T_1$ (figure 4(b)), $V_{out}$ will be set to $V_{out,0} = V_{dd}/2 + v_{io}$. At the same time, the top electrode of the sensor and the shield are connected to the ground. During time interval $T_2$ a charge $q_1$, which equals

$$q_1 = C_x V_{dd}/2 + (C_x + C_{p1}) v_{io},$$

will be pumped into $C_f$. This will result in an output voltage $V_{out,1}$, which equals:

$$V_{out,1} = V_{out,0} + \frac{C_x V_{dd}/2 + (C_x + C_{p1}) v_{io}}{C_f}.$$

In a similar way we will have

$$V_{out,2} = V_{out,0} + \frac{-C_x V_{dd}/2 + (C_x + C_{p1}) v_{io}}{C_f}.$$  

As we can see, due to the offset, the output voltage will not be symmetrical with respect to the level of $V_{out,0}$ anymore. However, the next stage, which is a voltage-to-period converter [5, 6], is designed to be only sensitive to the peak-to-peak voltage $V_{p-p}$, which equals

$$V_{p-p} = (V_{out,1} - V_{out,2}) = \frac{C_x V_{dd}}{C_f},$$

and is independent of offset.
3.2. Switch ON resistance, $R_{on}$

Figure 5 shows the circuit of figure 4 at the beginning of the time interval $T_4$ in which the capacitor $C_x$ has been charged to $V_{dd}$, and that this charge is going to be transferred to $C_f$. Since the points A and B are switched together to the same potential, after settling, the final charge of the parasitic capacitance $C_{p1}$ will be zero. Thus, all extra charge $C_xV_{dd}/2$ of $C_x$ has been transferred to $C_f$.

The range of the different capacitors in this circuit and also the switch size will determine the charge transfer speed and, in combination with the available time, also the accuracy of this transfer. If we use a coaxial cable, the safety ground could be used as the return path. However, in that case the current loop will be too big and undefined, and therefore susceptible to interference. It is better to use another wire to connect the ground of the capacitive sensor, which is implemented using a special ground electrode, to the ground of the interface. The best option is to use a triaxial cable instead of a coaxial cable. Then $C_{p2}$ can be in the same range as $C_{p1}$ (100 pF m$^{-1}$) or even larger. Usually in a low-cost system, a single wire twisted to the coaxial cable is used as the ground. In this case $C_{p2}$ will not be well defined.

In our setup, using a coaxial cable with a surrounding twisted wire as the ground, $C_{p2}$ is about 35 pF m$^{-1}$. To get an idea of the effect of the parasitic capacitances, we assume that the cable length $l = 40$ m, so that $C_{p1} = 4$ nF and $C_{p2} \approx 1.4$ nF Furthermore, we suppose that the sensor capacitance $C_x$ ranges from 10 pF to 330 pF and the switches are equal. In this case, the voltage transition at node B happens at a slower pace than that at node A. This means that, initially, $C_{p1}$ will pump some charge into $C_f$ in the same direction as $C_x$. Next, this undesired charge is removed with a time constant of about $\tau \approx 2R_{on}C_{p1}$. Figure 6 shows the simulation result for the case that $C_{p1} = 4$ nF, $C_{p2} = 1.4$ nF, $C_f = 1$ nF and $C_x = 100$ pF. If we suppose that this undesired charge is $k$ times as large as the desired charge $V_{dd}/2$ (see the right-hand side of figure 6), then the output voltage can be written as

$$V_{out}(t) = \frac{V_{dd}C_x}{2C_f}(1 + k \ e^{-t/\tau}).$$

Therefore, the absolute error $\Delta V_{out}$ at the end of a time interval $T_a$ amounts to

$$\Delta V_{out} = k\frac{V_{dd}C_x}{2C_f} e^{-T_a/\tau},$$

where $T_a = T_2 = T_4 = T_6 = T_8$ is the available time for charge transfer (figure 6).

Translating this error to capacitance read-out error results to

$$\varepsilon_{C,T.} = kC_x e^{-T_a/\tau},$$

where $\tau$ is the charge-transfer time constant mentioned in section 3.2. At first look, it might seem that by increasing the sensor capacitance, $C_x$, this error will increase too. However, in the assumed range of $C_x$, from 10 pF to 330 pF, the amount of undesired charge is almost independent of $C_x$. As a consequence, the value of $k$ is almost proportional to $1/C_x$. For instance, for $C_{p1} = 4$ nF and $C_{p2} = 1.4$ nF it is found (by simulation) that $k = 47, 10$ and 4 for $C_x = 10$ pF, 50 pF and 100 pF, respectively. Therefore, in equation (7), for the most part the sensitivities for the parameters $k$ and $C_x$ are compensating each other. Finally, since $T_a$ increases with increasing $C_x$ [7] this error should decrease by increasing $C_x$, which is in agreement with the measurement result presented in section 4.

In the interface circuit, we added the option of increasing $T_a$ by the factor of 2, by decreasing the integrator current $I_{int}$ in the voltage-to-period converter [6]. This option can be set with a pin called slow/fast mode. For the same error, in the slow mode the chip can handle twice as long a cable than in the fast mode. As an alternative, instead of increasing the available time $T_a$ we could also decrease the time constant $\tau$ by increasing the switch size by the same factor.

3.3. Switch charge injection

In order to be able to drive a parasitic cable capacitance of, for instance, 4 nF and yet have a short settling time, we need quite big switches. Consequently, the switch-charge injection, which includes channel-charge injection and clock feed-through, [9], can be significant. Figure 7 shows the relevant part of the interface for analyzing this effect.

The charge injection of $S_1$ will not induce any error in the output voltage because after it turns off $S_1$ turns on and $C_{in}$ will be connected to a well-defined potential. The error induced by charge injection of $S_1$ in the output voltage is always in one direction and similar to that of the offset voltage. This effect is
The interface has been designed and implemented using 0.7 μm standard CMOS technology. Figure 9 shows the chip photograph. The supply voltage is 5 V and the measured value for the supply current is about 0.7 mA. The current consumption slightly depends on $C_{p1}$ and will increase to 0.8 mA for $C_{p2} = 3.3$ nF.

In order to see the effect of incomplete settling, we measured different capacitors from 10 pF to 330 pF in the fast mode for two cases: (a) with emulation of 30 m of the coaxial cable with a twisted ground wire with equivalent discrete capacitors $C_{p1} = 3$ nF and $C_{p2} = 1$ nF, and (b) with a real cable of 30 m length with a twisted ground wire. The absolute error of these measurements along with the simulation result for $C_{p1} = 3$ nF and $C_{p2} = 1$ nF is shown in figure 10. It can be concluded that the simulation results and measurement results for an emulated cable, with the same parasitic capacitance, are in close agreement. For a real cable, the error is a little larger. Our investigations showed that this increased error was caused by frequency-dependent leakage of the cable shield to the grounded conductor.

Figure 11 shows a comparison of the error versus the input capacitance for the slow and fast modes (section 3.2) for a real cable with a length of 30 m. In the fast mode, the main source of error is due to uncompleted charge transfer.

Figure 12 shows the measured absolute error versus the input capacitance $C_x$ for four different lengths of the cable up to 40 m in the slow mode. From figure 12 it is easy to compare the results of the interface system presented in this paper with those of previous work [6]. According to this figure, for a sensor capacitance of 27 pF and a cable length of 30 m, the absolute error is about 0.25 pF. With comparable parameters, the system presented in [6] shows an error of more than 26 pF.

4. Experimental results

The relevant part of the CVC to analyze the charge-injection effect.

Figure 7. The relevant part of the CVC to analyze the charge-injection effect.

Figure 8. Simulated charge-injection-related error, $(C_{x,cal} - C_x)$, versus $C_x$ for $C_{ref2} = 330$ pF and for $C_{ref1} = 0$ pF and 10 pF, respectively.

Figure 9. Photograph of the chip which measures 1.4 mm × 1.7 mm. For the three time periods $T_{ref1}$, $T_{ref2}$ and $T_x$ of the output signal, these errors are almost equal. Therefore, these errors will mainly be removed by applying the three-signal auto-calibration technique. However, since the $C_{in}$ values (figure 7) are different for the three different phases of the measurements, the injected charges will show slight differences [9] so that after the three-signal auto-calibration some residual error remains. The largest error is found for the smallest value of $C_{in}$.

We simulated the effect of switch-charge injection for the complete interface with $C_{ref2} = 330$ pF and 20 pF ≤ $C_x$ ≤ 330 pF for two values of $C_{ref1}$: $C_{ref1} = 0$ pF and $C_{ref1} = 10$ pF. In order to analyze this effect independently from the error related to incomplete charge transfer, we used $C_{p1} = C_{p2} = 0$ pF. It can be proven that parasitic capacitances $C_{p1}$ and $C_{p2}$ do not affect the switch-charge injection. Figure 8 shows the absolute error $(C_{x,cal} - C_x)$ caused by charge-injection versus $C_x$. The value of $C_{x,cal}$ is calculated using the equation [7]

$$C_{x,cal} = \left( \frac{T_x}{T_{ref2} - T_{ref1}} \right) (C_{ref2} - C_{ref1}) + C_{ref1}. \tag{12}$$

From this figure, it can be seen that the residual error due to switch-charge injection can also be significantly reduced by increasing $C_{ref1}$ to, for instance, 10 pF. As we will see in the next section, even with $C_{ref1} = 0$ pF, for a long cable the error due to incomplete settling of the circuit is much larger than that caused by switch-charge injection. Therefore, for a long cable, we can simply select $C_{ref1} = 0$ pF, without introducing a significant error. However, for a short cable, depending

removed by the applied chopper. However, the charge-induced errors caused by $S_1$ and $S_2$ will add up and are significant. For the three time periods $T_{ref1}$, $T_{ref2}$ and $T_x$ of the output signal, these errors are almost equal. Therefore, these errors will mainly be removed by applying the three-signal auto-calibration technique. However, since the $C_{in}$ values (figure 7) are different for the three different phases of the measurements, the injected charges will show slight differences [9] so that after the three-signal auto-calibration some residual error remains. The largest error is found for the smallest value of $C_{in}$.
Figure 10. The simulated and measured absolute error versus the input capacitance for 30 m of the cable. The measurement results have been obtained with a real cable, or with emulation using equivalent capacitances ($C_{p1} = 3 \text{nF}$ and $C_{p2} = 1 \text{nF}$), respectively.

Figure 11. Comparison of the measured absolute error versus $C_x$ in slow and fast modes for 30 m of the cable with a twisted ground wire.

Figure 12. The measured absolute error versus $C_x$ for different lengths of the cable with a twisted ground wire.

Regarding the noise performance, it has been found that even for large values of the parasitic capacitance $C_{p1}$ and $C_{p2}$ (figure 4), these capacitances hardly affect the standard deviation. This shows that the noise performance is dominated by that of the voltage-to-period converter (figure 2) because otherwise, with increasing $C_{p1}$, due to the increased noise gain of amplifier $A_1$ (figure 4(a)), the output noise should increase [10]. Figure 13 shows the measured results for 100 measurements of a capacitance with a nominal value of 330 pF, for a measurement time of 40 ms including three-signal auto-calibration. The measured standard deviation amounts to 6.2 fF, which corresponds to about 16 bits of resolution.
of the nonlinearity are performed for absolute component accuracy, four different measurements for comparable conditions. The complete interface has been designed and implemented using 0.7 μm standard CMOS technology. The measurement results show good agreement with simulation results. It has been proven that, when we give the circuit enough time to settle, long connection cables can be used. Our measurements show that a capacitance as small as 10 pF with 30 m of the connection cable can be measured with an error of less than 0.3 pF. For this length of cable, for the range of Cx values from 10 pF to 330 pF, the measured nonlinearity is less than 3 × 10^-4. With a measurement time of 40 ms a resolution of almost 16 bits has been found.

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References


Figure 13. The measured value for a capacitor with a nominal value of 330 pF for a measurement time of 40 ms.