Design of
Electromagnetically Compatible
Electronics
Design of
Electromagnetically Compatible Electronics

Proefschrift

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Symbols and Abbreviations

\begin{itemize}
\item \(t\) Time
\item \(f\) Frequency
\item \(\omega\) Angular frequency
\item \(U\) Phasor of a time-harmonic electric potential
\item \(I\) Phasor of a time-harmonic electric current
\item \(E\) Phasor of a time-harmonic electric field intensity
\item \(H\) Phasor of a time-harmonic magnetic field intensity
\item \(D\) Phasor of a time-harmonic electric displacement
\item \(B\) Phasor of a time-harmonic magnetic field intensity
\item \(K\) Phasor of a time-harmonic magnetic current density
\item \(J\) Phasor of a time-harmonic electric current density
\item \(\varepsilon\) Electric permittivity
\item \(\mu\) Magnetic permeability
\item \(V_c\) Propagation speed of an electromagnetic wave
\item \(j\) Square root of \(-1\)
\item \(\delta(x)\) Dirac delta distribution
\item \(\partial\) Partial derivative operator
\item \(\mathcal{F}\) Fourier operator
\item \(D\) Spatial domain \(D\)
\item \(\partial D\) Boundary surface of spatial domain \(D\)
\item \(\nu\) Unit vector along the normal of a surface
\item \(\tau\) Unit vector along the tangential of a surface \(\partial D\)
\item \(\hat{x}\) Frequency domain equivalent of time domain function \(x(t)\)
\item \(\tilde{x}\) Frequency domain equivalent of discrete time domain function \(x(n)\)
\item \(x^*\) Complex conjugate of \(x\)
\item \(\mathbf{x}\) Vector “\(x\)”
\item \(\mathbf{X}\) Matrix “\(X\)” (Matrices are in bold capitals.)
\end{itemize}
<table>
<thead>
<tr>
<th>Symbol</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>$X^T$</td>
<td>The transpose of $X$</td>
</tr>
<tr>
<td>$X^H$</td>
<td>The Hermitian (complex conjugate and transpose) of $X$</td>
</tr>
<tr>
<td>$x_n$</td>
<td>Vector $x$ in tensor notation (index $n$ running from 1 to 3)</td>
</tr>
<tr>
<td>$\epsilon_{m,n,p}$</td>
<td>Levi-Civita tensor</td>
</tr>
<tr>
<td>$\delta_{m,n}$</td>
<td>Kronecker tensor</td>
</tr>
<tr>
<td>$G$</td>
<td>A Green’s function</td>
</tr>
<tr>
<td>$\Phi_J$</td>
<td>Electric current vector potential tensor</td>
</tr>
<tr>
<td>$\Phi_K$</td>
<td>Magnetic current vector potential tensor</td>
</tr>
<tr>
<td>$\varepsilon_{m,n}$</td>
<td>Electric permittivity tensor</td>
</tr>
<tr>
<td>$\mu_{m,n}$</td>
<td>Magnetic permeability tensor</td>
</tr>
</tbody>
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Chapter 1

Introduction

Most of us have experienced electromagnetic compatibility (EMC) problems in everyday life. For example, the ignition of a car that produces an annoying noise in the car stereo, or a mobile phone that does the same in audio equipment are results from electromagnetic interference (EMI). For that reason mobile phones are banned from intensive-care departments in hospitals to prevent interference with medical equipment. In general, devices are called electromagnetically compatible with each other when any unintended electromagnetic interaction between them does not interfere with their functioning.

EMI is comparable to separate groups of people conversing in close proximity to each other as depicted in Figure 1.1. Each group represents one electric device and the sound of the voices represents the electrical signals within the devices. As long as the noise from one group does not interfere with the conversation of the other, they are compatible or “sound compatible”. This means that the listeners may hear noise from other groups, but as long as the people within a conversational group are able to understand each other, there is no compatibility problem.

![Figure 1.1: Compatibility amongst groups of communicating people.](image)

An analogous situation can exist with electronic devices, where electric components “converse” with each other, not by acoustic, but rather by electric (electromag-
netic) signals that are guided by electrical interconnections. It should be noted that all conductors are able to act as parasitic antennas that may unintentionally interact with other devices. The components do not only receive the required signals but also “hear” parasitic signals from neighboring devices. As long as the parasitic exchange of signals between devices does not interfere with the intended “conversation” between components, these devices are electromagnetically compatible. The compatibility between devices therefore depends on the electromagnetic coupling between them, and their ability to discriminate between parasitic signals and the desired signal.

Figure 1.2 illustrates an electromagnetic incompatibility between a personal computer (PC) and an audio amplifier. Due to unintended electromagnetic coupling between the PC and the microphone wire, digital switching noise enters the amplifier. This high-frequency noise is above the audio frequency range, thus it is not audible. Due to the nonlinear behavior of the audio amplifier, however, it is converted to an audible signal. Hence, this incompatibility is caused by the combination of unintended coupling and nonlinear behavior of the amplifier.

Figure 1.2: EMC problem between a PC and an audio amplifier.

Systems therefore have to be made EM compatible with each other. The subject of this thesis is the inclusion of these compatibility requirements in the electronic circuit design process, and analysis and verification of EM compatibility by simulation. This chapter explains how we try to achieve this. Section 1.1 motivates why EM compatibility should become an integral part of the design of modern electronics. Section 1.2 gives an overview of the research involved in EM compatibility and the techniques that need to be developed for design of compatible systems. Section 1.3 presents the objectives of this thesis. Finally, Section 1.4 explains structure of this thesis.

1.1 EM Compatibility Requirements-Now and in the Future

In the past, EMC problems were better known as radio frequency interference (RFI) problems, referring to the most common type of EMC problems of those times: radios that suffered from interference generated by switches, engines, generators, and the ignition of internal combustion engines [1, 2]. EMC first became an issue in the military environment, where radio communication and radar equipment had to operate in close proximity to each other, and so EMC regulations were drafted [3, 4]. When digital electronics were introduced, more types of electromagnetic interference problems arose and the concept of electromagnetic compatibility was born.
Today the compatibility requirements for electronics are much tighter and they probably will become even tighter in the near future. The need for this is driven by more frequent use of electronics in places that demand high reliability, while the operating conditions become more demanding. For example in cars, electronic motor management, anti-locking braking systems (ABS) and electronic stability programs (ESP) prevent roll in corners and loss of traction on wet or uneven paved surfaces to improve safety and efficiency. To improve safety, these systems must be reliable. Airbus Industries builds fully computer-controlled airplanes, which improve safety by minimizing the chance of human error and a pilot does not require special training for each of their airplane types, because the controls have been unified. Such electronic systems must be extremely reliable and meet very strict electromagnetic compatibility requirements.

However, because of the increasing number of sources of interference, such as (wireless) computer networks, cellular phones, fast digital equipment and power electronics, it is increasingly difficult to meet these requirements. In the future, it is expected that the use of wireless equipment will rise sharply, while the bandwidth requirements and communication speed will also grow. On the other hand, signals become more vulnerable to interference, because of decreasing supply voltages, signal currents that are limited by decreasing transistor size, power limitations of battery powered equipment, and heat dissipation limitations of dense digital circuits. For example, the signal amplitude of digital signals in computers has dropped from about 5 Volt in the 1980s to about 0.9 Volt in 2004. Hence, the ad hoc design solutions of the past are no longer sufficient. To ensure the reliable operation of electronics, new design techniques are required that make EM compatibility an integral part of the design procedure, and simulation tools that provide insight in how EM interference effects a system.

### 1.2 Techniques for Developing EM Compatible Systems

From the moment electromagnetic compatibility became an issue in electrical engineering, many different disciplines were involved. In the 1920s, when radio first came into use, research into the cause of interference with radio broadcast reception [5] showed a wide variety of causes: natural lightning, the corona and leakage currents from high-voltage power lines, switching transients, electric motor commutation sparking, automobile ignition, the local oscillator of a neighboring radio, etc. EMC activities can be divided in four groups:

**Characterization and Reduction of EM Emission by High Voltage (i.e. > 1 KV) Systems.** High voltage systems, due to the corona and current transients (switching), are important sources of unintended EM emission. EMC research in this field involves: characterization of lightning as a source of EM interferences [6, 7], EM emission caused by switching currents, the corona [8] and other causes of EM emissions from high-voltage systems.

**Development of EM Compatible Electronic Systems.** The objective of this research is to develop the techniques required for the design of electronics that
comply with immunity as well as emission requirements. The disciplines involved are:

**Power electronics.** This research field includes reduction of unintended EM emission caused by switching currents of power regulators as for example explained in [9], EM immunity of power regulators for transients, etc.

**Analog and digital electronics.** Research in this area is on techniques for circuit as well as layout design [10, 11, 12] to optimize the immunity of the electronics and to minimize unintended emission of the electronics.

**Computer algorithms.** Compatibility problems introduce uncertainty in data and functioning of digital systems. In addition to using data error detection and correction techniques, the computer software must also be able to deal with instructions that aren't properly processed [13, 14, 15]. Special robust algorithms are required, for example in computer controlled airplanes.

**Verification of EM Compatibility.** Verification involves simulation and testing of the system for electromagnetic compatibility. Such simulations are a combination of circuit and electromagnetic simulations [16, 17, 18]. To test the EM compatibility of a device, unintended emission and immunity must be verified, which requires special antenna techniques for reliable and reproducible testing [19, 20].

**EMC-regulations.** These regulations ensure a proper balance between allowable emission and susceptibility to this emission. Therefore all countries nowadays have EMC regulations that prescribe limits on the allowable emission. The European Union also prescribes immunity requirements. Traditionally, the military and telecommunication industries [3, 4, 21, 22] have been the driving forces of EMC regulations, because their radar, radio, and television equipment is sensitive to interference. Many more industries are now involved due to the intensified use of electronics in industry, medical and life-sustaining equipment, cars, airplanes, etc. All regulations prescribe the limits as well as methods of verification. Due to the constant development of new telecommunication standards and equipment, these regulations are continuously changing.

Aside from these activities, research is also undertaken on the influence of EM fields on our health.

This thesis concentrates on the development of EM compatible analog electronics. In this field, currently most of the EMC research is done on verification of EM compatibility with the help of simulations and measurements [23, 24, 25]. Workbenches for printed circuit board (PCB) design have been developed with EMC design rule checkers and field simulators [26, 27, 28, 18, 16, 17]. More recently, research has been done on integrated circuit layout [29, 30, 31].

Very little research, however, has been done on design techniques. Therefore circuit and layout design decisions are based mainly on experience, trial and error, and rules of thumb [12]. Moreover, information processing, signal coding or circuit techniques are rarely taken into account. Therefore, many possible solutions are not considered, while design decisions cannot be based on performance and costs. This
results in inefficient and costly designs. For this reason new design techniques are required that make EMC an integral part of the design process. These techniques consider the available alternative solutions and enable evaluation of design solutions early in the design process. For example, to improve the compatibility of an amplifier, one has to evaluate the cost and performance of a solution like shielding, or a circuit solution like a differential current domain implementation, before implementing it. In order to do this, the influence of EM interaction must be included in circuit models, so that a designer can evaluate it. The relationship between design parameters (e.g., the length and orientation of a connection) and performance (e.g., crosstalk) must be examined to enable optimization.

The circuit extraction tools currently available for analyzing and verifying a physical layout [26, 27, 28, 18, 16, 17] are based on antenna simulation techniques. However, for circuit extraction these techniques have limited accuracy, because it is assumed that the port impedance of a network (e.g. interconnect) can calculated independently of the system (e.g. component) connected to that port, and it assumed that the port voltage can be calculated by making a quasi-static approximation of the electric field between the terminals of the port. Both assumptions lead to errors in the extracted circuit equivalent of a layout. The port impedance is not independent of the system connected to it, because that system takes part in the EM-interaction with the network. Hence, the port impedance of a network is not a property of only the network, but depends also on the system connected to it. By using a quasi-static approximation of the electric field between the terminals of a port, the phase difference between them is ignored. Such an approximation is valid for one port, but in a large circuit with many ports (of many components) these errors add up and cannot be ignored anymore. This problem is for example observed in the PEEC model [32]. In this thesis a new circuit extraction method is presented that solves both problems.

1.3 Objectives of this Thesis

The Electronic Research Laboratory at the Delft University of Technology has a long tradition of developing design methods and techniques to optimize analog electronics [33, 34, 35, 36]. The EM compatibility of electronics has become an important specification, and with the recent developments in mobile communication equipment, it is expected to become even more important in the future. This thesis is the start of a long-term research project that aims to develop design methods and techniques for EM compatible analog circuits that may be integrated in existing design methods. The goal of this thesis is to provide a base for a design method for optimal EM compatible circuit design. This design method must enable optimization of EM compatibility during every phase of the design, from first concept to final physical layout.

The first objective of this thesis is to provide a framework that decomposes the design of an optimal EM compatible system hierarchically in parts that each can be handled individually. Its hierarchical organization must ensure that the most effective measures are considered first, and EM compatibility can be optimized during each design phase.

The second goal of this thesis is the integration of electromagnetic and circuit theory. The objective is to make the effects of unintentional electromagnetic interaction
controllable during circuit and layout design. Therefore the influences of unintentional EM interaction must be represented by a circuit equivalent, so they can be considered during circuit design. Further techniques must be provided to control and simulate the unintentional EM interaction in the layout.

The existing computer software for calculating circuit equivalents of layouts are based on antenna calculations and make assumptions that are not valid for all types of layout. In this thesis a new circuit extraction method is presented that is able to generate an accurate and robust circuit equivalent for any type of layout. To determine the port impedance of a network, we include the system (e.g. component) that is connected to this port and determine the impedance “observed” by it. Hence, the port impedance measurement method is calibrated by the system that “observes” the port. The existing methods determine the impedance of a port from the voltage-current relationship measured at its terminals, using a quasi-static approximation of the electric field between the terminals. We determine the port impedances of a network from the power transfer between the systems (e.g. components) connected to the ports of the network. Therefore the port voltages in the derived equivalent circuit do not exactly represent the port voltages in the layout, but rather the power transfer through the ports. Hence, the extracted circuit describes the power transfer between systems. A comparison between measurement results and simulation results in this thesis demonstrate the accuracy of this method.

1.4 Structure of this Thesis

As the example in the introduction of this chapter illustrated, to study EM compatibility, in this thesis an electronic system is considered as an information (signal) processing system, where EM interaction does not corrupt the information processed. EM compatibility is improved by reducing the chance of corruption of the processed information. To determine the classes of techniques that can be applied to reduce the chance of corruption of information, we describe a system at four levels of abstraction, where each level allows a different class of techniques to achieve this. These levels are: information level, coding and modulation level, circuit level, and layout level. Each of these levels describes the system as an information processing system, but concentrates on a different aspect of information processing.

The information level considers the system as an information channel and determines the required information capacity, and the corresponding signal to interference noise ratio, for corruption-free information processing. The coding and modulation level describes the system by a functional block diagram and determines the optimal signal coding and signal processing function to optimize the compatibility with the help of communication theory [37, 38]. The circuit level describes the system by its circuit description and determines the optimal implementation that minimizes compatibility problems due to distortion (inter-modulation) and crosstalk by EM interaction [10, 39] and via common power supply [40, 41]. Finally the layout level describes the system by its physical layout and determines the optimal implementation by minimizing the EM interaction between the actual signal paths within a system. As this is the last level, it requires design as well as verification. The focus of this thesis is on the last two levels, where we try to integrate the layout and cir-
cuit levels. Therefore the most important contributions appear in the last chapters. Figure 1.3 shows an overview of the structure of this thesis.

In Chapter 2, the design process is divided into different phases that each correspond to one of the four levels. Each phase deals with a different class of techniques for optimizing compatibility. Chapter 2 analyzes the causes of compatibility problems at each level, and outlines how they can be anticipated upon.

![Diagram of the structure of the thesis]

Figure 1.3: Overview of the structure of this thesis.

In Chapter 3 the causes of compatibility problems within a circuit are analyzed. Therefore the circuit description is extended with models that describe the unintended EM interaction and the nonlinear behavior of semiconductor components. With these models the causes of compatibility problems are analyzed.

With the help of the models and analyses of Chapter 3, design techniques for improving EM compatibility are presented in Chapter 4. Because this thesis focuses on the union of circuit and layout design, this chapter does not treat optimization of entire circuits. It treats the optimization of signal transport within a circuit design, which is required to enable optimization of the layout. In addition, techniques are presented to eliminate interference due to nonlinearities of semiconductor components (e.g., nonlinear transfers and time constants).

Chapter 5 presents a model for circuit and layout design. In this chapter a circuit model is derived that describes the EM interaction within a circuit in terms of layout design parameters like the length and width of interconnections.

Chapter 6 presents a new layout design approach based on the signal flow within a circuit. With the help of the models derived in Chapter 5, the circuit design is
analyzed for structures that can cause undesired EM interactions within the circuit, in order to minimize their influence.

Finally Chapter 7 presents a new circuit extraction method for analysis and verification of a layout. The presented method has an improved accuracy and robustness over existing methods and is able to handle any type of layout. The extracted circuit is analyzed with the help of a circuit simulator like SPICE or Spectre\textsuperscript{TM}. To improve the accuracy of the field simulations required for the circuit extraction, a new anti-aliasing technique is introduced to suppress aliasing errors that are inherent to spatial discretization of the field equations.
Bibliography


Introduction


Chapter 2

Principles of Structured Design for EMC

Ideally, electronic systems have no influence on each other. However, in practice all systems are electromagnetically coupled, and signals from one system can affect neighboring systems. In this thesis, we call these signals “parasitic signals” to distinguish them from other types of interference such as noise. EM compatibility problems arise when parasitic signals interfere with signals or corrupt the processing of signals within a system. There are many techniques that can be applied to prevent signal corruption and render systems compatible with each other. Traditionally this requires a reduction of the EM interaction by shielding. However, the robustness of signals can also be improved by more signal power or by rejecting parasitic signals by additional filtering. To find an optimal solution (technically and economically), a deliberate choice must be made already at an early stage in the design process based on trade-offs between performance and costs for these different techniques.

This chapter presents the framework of a structured design method to efficiently find the best possible EM compatible solution. Different classes of techniques can be applied to improve compatibility. The techniques within each class share the same underlying principles. For example, techniques to minimize EM interaction and techniques to improve the robustness of signals are two such classes. This hierarchy is organized such that each technique depends only on design choices taken at higher hierarchical levels. It therefore serves as a road map to efficiently find the best solution. This method is explained in Section 2.1. The hierarchy and the relationships between these classes of techniques is presented in Section 2.2. Sections 2.3 to 2.6 present four main classes of techniques to improve the compatibility of a design. This thesis covers only a portion of the techniques required to develop a complete design methodology.

2.1 Principles of Structured Design

One of the main differences between an experienced and an inexperienced designer is that experience allows one to anticipate the performance, limitations and cost of many
design solutions. On the other hand, this experience may also hamper innovation, because a known, working solution is often preferred over a new one. An inexperienced designer, however, lacks this information and needs time to evaluate different solutions before finding a suitable. To find the best suitable solution, all potentially good solutions have to be evaluated, which is often impractical.

To improve this situation and help a designer find the best solution, we apply a structured design strategy. This method has been proven efficient for many design problems in analog circuit design [1, 2, 3, 4]. It provides a search method that guides the designer to the best suited solution. In addition to this, it provides the tools and techniques to evaluate the performance and limitations of the different design choices at an early phase in the design.

The backbone of this strategy is a hierarchical decomposition of the design problem, which serves as a decision tree for the design procedure. This hierarchy is found by sorting classes of design techniques according to the interdependence of their design parameters (see Figure 2.1). The arrows in Figure 2.1(a) indicate the interdependence of the design parameters. Figure 2.1(b) shows the hierarchically organized version, where every parameter only depends on design choices of higher hierarchical levels. This hierarchy gives the sequence in which the design choices have to be made to enable their optimization. By using this sequence, every design parameter depends only on previously taken decisions and can be optimized individually. At every level of this hierarchy, we group together the techniques that share the same underlying principles. For example, all techniques that reduce EM interaction, such as shielding, belong to one level. To enable optimization of the compatibility at every level in the hierarchy, we develop simplified design models that describe the performance of only the system as a function of the most important (i.e., key) design parameters. Note that at every level, these models must represent all mechanisms that can cause compatibility problems, so that they can be evaluated and anticipated. For example, the circuit models of components and interconnects that are used for circuit design

![Diagram of hierarchical organization of design parameters](image-url)

Figure 2.1: Hierarchical organization of design parameters.
must also describe the EM interaction between them. These models enable a designer to evaluate the performance of all implementations, such that a deliberate choice of the best-suited alternative can be made.

### 2.2 A Design Hierarchy for EM Compatibility

EM compatibility between electronic systems depends on a wide range of design parameters, from signal coding (bandwidth, dynamic range) to circuit layout (length, width, shape, material, etc.). To determine the best solution for a design, a structured design strategy is applied as explained in Section 2.1. This section presents the framework on which this strategy is based: a hierarchical decomposition of the design problem. Section 2.2.1 defines EM compatibility, which is the objective of the design strategy. A model of a general compatibility problem is given in Section 2.2.2. From this model, a hierarchical decomposition of the design problem is derived in Section 2.2.3.

#### 2.2.1 Definition of Compatible Systems

Ideally, electrical and electronic devices are able to operate in close proximity to other devices without having any influence on their functioning. This means that the information streams (signals) processed by these devices are isolated from one another. Due to EM interaction between systems, this complete isolation is rarely possible in practice. According to the IEEE definition [5], systems are EM compatible when they are able to function satisfactorily in each other’s vicinity. For electronic systems, we use a more precise definition: systems are compatible with each other when the EM interaction between them does not corrupt the information streams (signals) that each system processes. This means that the processed signals may suffer from interference as long as the information conveyed is not corrupted. In terms of the conversing people from Figure 1.1, the groups are compatible (according to our definition) when the people within each group can understand each other.

#### 2.2.2 A Model of Interfering Systems

The basic purpose of almost any electronic system is the transport and processing of information streams. These information streams can be text, video, sound, control information, etc. Compatibility problems arise when parasitic signals from a neighboring system corrupt this information. This is comparable to co-channel interference within communication systems, except that it is caused by undesired EM interaction between systems.

To formalize this mechanism, we represent an electronic system by one or more information channels as shown in Figure 2.2. The channel is the information processing system (amplifier, radio transmitter, digital computer, etc.) that receives information from a source (microphone, keyboard, antenna, etc.) and delivers the processed information to a receiver (speaker, display, antenna, etc.). Ideally, these channels are completely isolated from one another, but due to (undesired) EM interaction between them, parasitic information channels arise (as depicted Figure 2.2) that can
cause compatibility problems. To improve compatibility, the capacity of these parasitic channels must be minimized. Therefore, the separation between the information streams in neighboring channels must be maximized. This is the core objective of compatibility. The following section gives an overview of the techniques that can be used to achieve this.

2.2.3 Hierarchical Decomposition of Techniques for Improving Compatibility

To improve compatibility, the separation between information streams (signals) within a system must be optimized. This separation is determined by the representation of the information stream (signal coding) within a system and the construction of the system itself.

Separation of information streams (signals) is achieved by assigning to each stream a different subdomain, which is coded or processed. For example, separation in the frequency domain is achieved by assigning each signal to a different carrier frequency. The hierarchy of techniques for improving compatibility therefore treats all domains into which information streams are separated. We consider four different levels: the information, coding and modulation, circuit, and layout level. Figure 2.3 shows the information stream (signal) and system representations. To explain the domains available for separation and techniques to improve this separation, we again use the metaphor of conversing people depicted in Figure 1.1. At the information level, the system is represented by a set of information channels operating on information streams. The domains available for separation are the channel and symbol domains. The channels are comparable to the room occupied by the groups of conversing people. The symbols correspond to the words they speak (e.g., each can group can use a different language). Techniques for improving compatibility in this example are signal processing techniques to discriminate between symbol streams, such as adaptive noise cancellation as described in [6].

At the coding and modulation level, the channel is described by a functional block diagram, while the information streams are represented by signals. The domains available for separation are the signal coding domains, such as the time and frequency domains. This is comparable to letting people speak in turn during a conversation and the ability of the human brain to discriminate between different voices. Techniques
to improve compatibility at this level are orthogonal signal coding (modulation) and increased selectivity of the signal processing functions (e.g., with filters).

At circuit level, the channel is described by a schematic diagram and the information stream by electrical signals. The electrical domain, which consist of current and voltage domains, is available for separation of signals. Crosstalk (as explained in Chapter 4) can be minimized by separating signals into current or voltage domains. In addition, any separation made at the other levels must be obeyed. This means minimization of (nonlinear) distortion to maintain separation between modulated signals and elimination of parasitic signal paths, which are often caused by biasing circuitry.

At layout level, the channel is described by the physical layout and the information streams by electromagnetic waves (guided by the interconnect). The domain available for separation is the spatial domain. Shielding techniques and optimization of the interconnect minimize undesired EM interaction. This is comparable to giving each group of conversing people their own isolated room.

### 2.3 Information Level

Compatibility between information channels is achieved when channels do not corrupt each other’s information streams. From rate distortion theory [7] it is known that corruption-free processing is only possible when the information capacity is large enough. Compatibility problems arise when the capacity is reduced beyond the level required for corruption-free information processing, due to parasitic information streams (as shown in Figure 2.2). This section analyzes these compatibility problems and presents techniques to prevent them. Section 2.3.1 develops an information theory model of the EMC problem. The reduction in channel capacity is determined in Section 2.3.2. Finally, Section 2.3.3 explores basic techniques that improve compatibility.
2.3.1 An Information Model for Compatibility Analysis

Any electronic system can be modeled as a number of information channels. The interconnections within a system transport the information, while other electronic operations (like amplification, modulation) change the representation of the information, split or combine information streams, etc. To analyze EM compatibility, we extend the channel model of Shannon [8, 9] with the parasitic channels as depicted in Figure 2.4. The system consists of an information source, a channel (the electronic system the processes the information), and an information receiver. The EM interaction is represented by parasitic channels that cause (in addition to noise) the injection of parasitic information streams in each channel. The output of each channel therefore is the sum of the required information, parasitic information and noise. The parasitic information and the noise both reduce the channel capacity. However, unlike noise, parasitic information is deterministic and can be estimated. This allows us to reduce the impact of parasitic information streams, for example with adaptive noise-cancellation techniques. The information receiver consists of an estimator and a detector. The estimator produces an approximation of the symbol streams sent by the information source and therefore must reject the parasitic information stream and the noise. The detector uses these estimations to decide which symbols have been sent.

![Information channel model for EMC analyses.](image)

**Figure 2.4:** Information channel model for EMC analyses.

2.3.2 Reduction of the Channel Capacity Due to Parasitic Information Streams

The received information is corrupt when the receivers in Figure 2.4 are not able to reconstruct the information sent by the sources. This happens when the capacity of the channels is too small due to the presence of parasitic information. This section determines the capacity reduction due parasitic streams. First a qualitative analysis is given of the capacity of a noisy channel, after which the capacity reduction due to parasitic information is treated.
The Influence of Noise and Parasitic Information on Information Processing

The fact that it is really possible to transmit symbols over a noisy channel without errors is an amazing result from the information theory developed by Shannon [8]. He explained this as follows: assume that the noise and information sources are ergodic, so that a very long time sample is (with probability 1) typical of an ensemble. Both messages as well as channel noise are represented by vectors in a $2BT$ dimensional space (see [10]), where $B$ is the channel bandwidth and $T$ the duration of the messages. This dimension equals the minimum number of samples that according to Nyquist is required to reconstruct the message. The length of the message and noise vectors are proportional to the root mean square (rms) of the signal and noise power (variance). Because the received messages are a summation of the message and noise, they are confined within a noise sphere around the end points of the message vectors. For a white Gaussian additive channel connected to a source that sends all messages with an equal probability, the optimal detector selects the message vector with the smallest Euclidean distance to the received vector [11]. The chance of errors becomes arbitrar-

![Figure 2.5: Corruption free transport in a noisy channel.](image)

(a) Corruption free transport. (b) Corrupted transport.

ily small if the messages are selected such that these noise spheres can only hold the end point of one message, as illustrated in Figure 2.5(a), while larger noise spheres make some messages indistinguishable, as shown in Figure 2.5(b). For corruption-free transport, the radius of the noise spheres must be limited. In principle, a noise vector can be of any length, because the instantaneous noise power is not limited. For very long messages ($T$ very large), however, the length is proportional to the noise power, which is limited. Therefore error-free information transmission can be achieved for infinite long messages. In practice, however, message lengths are limited and errors do occur. As depicted in Figure 2.6, parasitic signals add to the noise vector. As this figure shows, the sphere of a possible end point for a given message vector is proportional to the square root of the sum of the power of the noise and the parasitic message. However, unlike noise, a parasitic signal can be estimated, which allows for conservation of the channel capacity, as shown in the next sections.
Capacity Reduction Due to Unknown Parasitic Signals

This section shows how we can determine the reduction in channel capacity when nothing is known about the parasitic information stream. The channel capacity per symbol is defined as the maximal mutual information $I(x, y)$ (see [12]):

$$C_s = \sup_{p(x)} [I(x, y)] = \sup_{p(x)} [H(x) - H_y(x)], \quad (2.1)$$

maximized over all possible probability density functions $p(x)$ of the input symbols $x$. The function $H(x)$ is the average entropy (information content) of the input symbols $x$, and $H_y(x)$ is the entropy of $x$ that is lost when the output symbol $y$ is known. Hence, $H_y(x)$ is the information about $x$ that is lost during transport and processing due to noise, limitation in bandwidth and dynamic range. Multiplication of this capacity per symbol gives the maximal information rate. Under the assumption that the information stream, the noise, and parasitic information stream are all independent, the reduced channel capacity is given by:

$$C_r = 2B \sup_{p(x)} [I(x, y)] = 2B \sup_{p(x)} [H(x) - H_y(x)]$$

$$= 2B \sup_{p(x)} [H(y) - H_x(y)] = 2B \sup_{p(x)} [H(y) - H(n + d)]$$

$$= 2B \sup_{p(x)} [H(x + n + d) - H(n + d)], \quad (2.2)$$

where $B$ is the bandwidth, $n$ and $d$ are the information contents of the noise and parasitic symbols respectively. To calculate this channel capacity for a continuous (non-discrete) channel, the entropy (information) rate of continuous symbol streams must be determined. However, for continuous symbol streams (signals), the contents is infinitely large. For example, one sample requires an infinite number of digits to be represented. Shannon recognized this problem and solved it by introducing a noisy observer. Nowadays the “differential” entropy rate is used [13], which is defined as:

$$R_{\text{diff}} = -2B \int_{-\infty}^{\infty} p(x) \log_2 p(x) dx. \quad (2.3)$$

This is not the absolute entropy rate; this value can only be used to determine the difference in entropy rates between streams. The reason we stress this here is that many textbooks on information theory do not clarify this property. The capacity of the channel is maximally reduced when both the noise and parasitic information are
Gaussian. Because (2.2) defines this capacity as a difference in entropy rate, (2.3) can be applied to determine the reduced capacity. This is given by

$$C_r = \frac{1}{2\pi} \int_0^{2\pi B} \log_2 \left[ 1 + \frac{S_x(\omega)}{S_n(\omega) + S_d(\omega)} \right] d\omega,$$

where $S_x(\omega)$, $S_n(\omega)$ and $S_d(\omega)$ are the power density spectra of the source information, the noise and the leaking information streams, respectively. Hence, the parasitic signal has the same effect as noise. The channel capacity reduction equals

$$C_{\text{red}} = \frac{1}{2\pi} \int_0^{2\pi B} \log_2 \left\{ 1 + \frac{S_x(\omega)S_d(\omega)}{S_n(\omega)[S_n(\omega) + S_x(\omega)]} \right\} d\omega \approx \frac{1}{2\pi} \int_0^{2\pi B} \log_2 \left\{ 1 + \frac{S_d(\omega)}{S_n(\omega)} \right\} d\omega,$$

$$S_n(\omega) \ll S_x(\omega), S_d(\omega) \ll S_x(\omega),$$

where the last approximation assumes that the information stream $x$ has much more power than the noise $n$ and the disturbance $d$ stream. This is valid only for a good design. Thus, there is a significant reduction in capacity when the parasitic information stream power is larger than the noise from other mechanisms.

**Capacity Reduction in the Presence of Known Parasitic Information**

When the parasitic information is known, it can be compensated for, as discussed in the next section. This means that the parasitic message vector in Figure 2.6 is subtracted from the received signal, so that (ideally) no signal capacity is lost. However, in practice the estimation of the parasitic signal is never exact. Let $d$ be the parasitic information and $d_e$ the estimation used for compensation. Because it is not exact, some error $n_e$ remains:

$$d_e = d - n_e.$$  

The capacity of the channel now increases to:

$$C_r = \frac{1}{2\pi} \int_0^{2\pi B} \log_2 \left[ 1 + \frac{S_x(\omega)}{S_n(\omega) + S_{nc}(\omega)} \right] d\omega,$$

where $S_{nc}(\omega)$ is the power density spectrum of the error $n_e$ in the estimation. From (2.5) it follows that when the estimation error is below the noise level, the full capacity is almost restored. However, this method only works if the dynamic range of system is large enough to accommodate the sum of the parasitic and required information.

### 2.3.3 Measures to Improve Compatibility

From the analysis of the previous sections one can conclude that compatibility amongst channels is achieved when the parasitic information streams do not reduce the capacities below the information rates of the connected sources. Compatibility can be
improved with three different methods: reduction of the capacity of parasitic channels, reservation of extra capacity for parasitic information, and compensation of the parasitic information.

The capacity of parasitic channels is reduced with techniques like filtering and the reduction of EM interaction, which are treated in the next chapters.

Reservation of extra capacity requires extra channels, dynamic range and bandwidth such that information can be processed together with parasitic information without corruption. For example immunity can be improved with the help of extra error correction information used in digital communication or extra wire connections for rejection of common mode interference by a differential circuit implementation. To prevent interference within shared paths, separation in signal coding may be required such as time or frequency domain multiplexing.

Finally, compensation can be applied with the help of an estimation of the parasitic information. This method reduces the capacity loss given by (2.7) and is illustrated in Figure 2.7. The output stream $y_2$ of Channel 2 is the sum of the input stream $x_2$,

\[ y_2 = x_2 + d. \]

Figure 2.7: Reduction of capacity loss with the help of compensation.

noise and the parasitic stream $d$ from Channel 1. The estimator senses Channel 1 and makes an estimation $d_e$ of the parasitic stream $d$, which is subtracted from stream $y_2$. For example, this kind of compensation is applied by an adaptive noise canceler [14] used for coronary care. We used it to improve the compatibility of a microphone preamplifier in Section 4.4. The effectiveness depends on the accessibility of the parasitic information (Channel 1 in this figure) and characterization of the parasitic channels. Crosstalk within a system, for example, can be better compensated than interference from an unknown external system. This method is best suited for linear additive channels, whose dynamic range is large enough to handle the parasitic and intended information signals simultaneously. It cannot compensate for modulation of the channel transfer by a parasitic signal or intermodulation products.

2.3.4 Conclusion

Compatibility problems between channels arise due to the reduction in capacity caused by parasitic information streams. These parasitic streams enter the channel by means of parasitic channels. To attain compatibility, the channel capacity must be large enough to process all of the information without distortion, even in the presence of parasitic information. Figure 2.8 shows an overview of principles to minimize the
reduction in capacity. The ideal solution is reducing the parasitic channel capacity to zero, such that the channels are isolated and no capacity reduction takes place. If parasitic channels are accepted, the receiver needs to separate the required streams from the parasitic streams. In this situation, the channel capacity may be reduced and measures are required to ensure that enough capacity remains. The channel is most affected when nothing is known about the parasitic information stream. Any reduction in capacity can be minimized when the parasitic signal can be compensated for.

In practice, compatibility is always achieved by a combination of methods. The capacity of the parasitic channels is reduced, although complete isolation is practically impossible.

### 2.4 Coding and Modulation Level

Coding and modulation (which in the remainder of the text is referred to as signal coding) determines the signal representation of information. In this section, a system with all signal processing electronics is considered to consist of one or more signal paths. To improve compatibility, signal coding is applied to these paths such that the chance of errors due to noise and parasitic signals is minimized. Therefore this coding must enable discrimination between intended and parasitic signals. The techniques required are similar to the signal multiplexing techniques used in telecommunication, except that the coding of parasitic signals is typically unknown. This section briefly describes how these techniques can be used to improve compatibility.
Section 2.4.1 determines the causes of corruption within signal paths. Section 2.4.2 describes the basic principles that are required to adapt signal coding to the paths such that compatibility is improved.

2.4.1 Causes of Corruption within Signal Paths

This section determines the causes of compatibility problems within signal paths, which are important for the optimization of signal coding. Coding is fully adapted to a signal path if none of the information is lost, even in the presence of parasitic signals. The mechanisms that can cause these losses are: noise, EM interaction between paths, and distortion. The last two mechanisms can deteriorate compatibility and are therefore treated in this section.

Separate signal channels are created with the help of separate paths and coding (multiplexing). Figure 2.9 shows how \( n \) channels are created with the help of two signal paths and multiplexing. Compatibility problems arise when due to EM coupling and distortion the separation between these \( n \) channels is lost. As illustrated in this figure, EM coupling causes parasitic paths that may lead to interference between the signals in each path. With proper signal coding, however, interference can be prevented by separating required and parasitic signals in a signal coding domain. For example, when the signals are separated in frequency domain, filters can be used to discriminate between parasitic and intended signals.

Distortion within each channel, however, can deteriorate this separation. For example, nonlinearities cause intermodulation products which interfere with other channels. In this figure, this is illustrated by a graph of a power density spectrum, where the arrows in the spectrum of Path 2 indicate conversion due to distortion. We distinguish two types of distortion: distortion in amplitude and time. Amplitude distortion is mainly caused by nonlinear semiconductor components and results in modulation between signals. Distortion in the time domain occurs when the processing or transfer time varies or when a signal travels over multiple paths simultaneously. This type of deterioration is well known for radio channels, but also happens in electronic circuits. The time constants of class-B biased transistors, for example, are signal dependent. This example is treated in Chapters 3 and 4. These mechanisms can deteriorate separation in time (phase) domain.

Figure 2.9: Causes of crosstalk within a signal path.
A common compatibility problem is the combination of EM coupling and distortion. An example of this is a mobile phone that interferes with an audio system. To describe this mechanism, one cannot use common linear analysis methods, but it can be solved with the method of Blachman [15] for noise analyses in nonlinear systems. Due to parasitic paths, an output signal $y_i(t)$ of a signal path $i$ in Figure 2.9 is a function of all input signals $x_j(t)$:

$$y_i(t) = F_i[x_1(t), \cdots, x_2(t), N_i(t)],$$  \hspace{1cm} (2.8)

where $N_i(t)$ is noise generated within signal path $i$. In a proper design, the interfering signals $x_j(t)|_{j \neq i}$ are much smaller than the required signal $x_i(t)$. Therefore, similar to the description of noise in a nonlinear system [15], the signal from a nonlinear channel can be decomposed in the following components:

$$y_i(t) \approx F_i[x_i(t)] + C_i(t) + N_i(t) + \sum_{j \neq i} [D_j(t) + I_j(t)],$$  \hspace{1cm} (2.9)

where $C_i(t)$, $F_i[x_i(t)]$, $N_i(t)$ and $I_i(t)$ are the deterministic (DC offset), (required) signal, noise and signal $\times$ noise components, respectively. The parasitic signals are now separated into parasitic signals $D_j(t)$ and input-modulated parasitic signals, $I_j(t)$. The noise and parasitic signals also modulate each other of course. However, except for the DC offset, these components can be is ignored as the required signal $F_i[x_i(t)]$ is much larger. Therefore, in a nonlinear system, the interference noise is approximated by the sum of a DC offset, the parasitic signals itself, and input-modulated interference signals.

### 2.4.2 Coding of Information Streams

Information coding ideally minimizes the chance of errors during transmission over a signal path. To optimize compatibility, this coding must enable discrimination between intended and parasitic signals [10, 16]. A circuit design has to be optimized for the chosen signal coding.

This section briefly explains the principles of optimizing a code to be used in the presence of parasitic signals. For this purpose we use a vector representation of the signal. This vector representation enables us to determine the circuit requirements to optimize the processing.

The following sections first explain this vector representation followed by a discussion of the optimization of the signal coding.

#### Coding of Information

The construction of a signal can be defined by two steps: first the information stream is mapped on a signal, and then this signal is assigned to the amplitude or phase of the signal carrier. We will explain both steps briefly here. This procedure is illustrated in Figure 2.10.

A discrete information source, as explained in Section 2.3.1, produces a stream of symbols. To map these symbols on a signal, each symbol is assigned a number, which is called symbol coding in this figure. These symbol numbers are used as weight factors for orthonormal weight functions. The resulting signal representation $x(t)$ is
commonly used in communication theory [10, 16]. This signal is used to modulate the amplitude or phase of the final signal $s(t)$.

Assume that an information source produces $2N$ symbols, represented by two groups of $N$ numbers $\{a_1^{(o)} \ldots a_N^{(o)}\}$ and $\{a_1^{(e)} \ldots a_N^{(e)}\}$. These groups of numbers are mapped onto a signal of duration $T$ as follows:

$$
    x(t) = \sum_{i=1}^{N} [a_i^{(o)} \psi_i^{(o)}(t) + a_i^{(e)} \psi_i^{(e)}(t)] \quad 0 \leq t \leq T,
$$

(2.10)

where $\psi_i^{(o)}$, $\psi_i^{(e)}$ are the odd and even orthonormal expansion functions of duration $T$. Any discrete signal can be represented in this manner. For example, when the functions $\psi_i^{(o)}$ and $\psi_i^{(e)}$ are chosen to be pulse functions, the signal becomes a baseband pulse amplitude modulated (PAM) signal, while sine and cosine functions with a frequency of $i\frac{\pi}{T}$ result in a kind of spread spectrum signal. By using orthonormal base functions, one can always recover the original symbols by taking the inner product of this signal with the same expansion functions. For continuous signals the summation in (2.10) becomes an integral, but the representation is the same. Moreover, Nyquist’s theorem states that continuous signals with a finite bandwidth ($B$) and duration ($T$) can always be represented in the same manner when $N \geq 2BT$.

The final signal representation is found by assigning the phase $\theta(t)$ and/or amplitude $a(t)$ of a carrier to this signal. The resulting signal is a bandpass or low-pass signal, given by:

$$
    s(t) = \Re[a(t)e^{j[\theta(t)+2\pi f_c t]}],
$$

(2.11)

where $j = \sqrt{-1}$ and $\Re(\cdot)$ evaluates the real part of its argument.

**Optimization of the Coding for Compatibility**

For compatibility, the vector representation of the previous section makes two very important properties visible: the allowable parasitic signal power and the required optimal coding. The signal is represented by a vector $[a_1^{(o)}, a_1^{(e)}]^T$ of dimension $2N$. Corruption takes place when the received signal vectors become indistinguishable due to added noise and parasitic vectors. As explained in Section 2.3.2, the distance between the end points of all possible signal vectors determines the length of the noise and parasitic signals that are allowed (see Figure 2.5). Because we used orthonormal expansion functions, the squared length between these vectors is a measure of the allowable noise and parasitic signal power. Optimal coding therefore maximizes the distance between these vector end points.
The choice of orthonormal expansion functions determines the signal coding domain that is used. These functions can be pulse, sine, cosine or Walsh functions, for example. They must suit the channel characteristics and make them distinguishable from parasitic signals. Two situations have to be distinguished: interference from a signal with known coding and interference from a signal with unknown coding. When the coding of the parasitic signal is known, expansion functions can be chosen that are orthogonal to those of the parasitic signal, as illustrated in Figure 2.11(a). This means that the coding equals the coding domain of the parasitic signal (for example, the frequency or time domain) but that a different part of the domain is used. When nothing is known about the parasitic signal, any choice may suffer severely from a parasitic signal. The safest solution is to spread the signal energy over a complete signal domain like spread spectrum coding, as illustrated in Figure 2.11(b). With this choice, the parasitic signal acts as noise, limiting the capacity but the chance that the complete communication is blocked is minimized. The second choice that has to be made is whether the chosen coding is used for amplitude or phase modulation of the final signal $s(t)$ from Equation (2.11). This choice depends on the channel characteristics and not on the parasitic signal. A signal path that is highly nonlinear may be better suited for phase (time domain) modulation for example. To prove that this choice does not depend on the parasitic signal properties, we determine the desired ($S$) to parasitic ($D$) signal ratio $\frac{S}{D}$ for an amplitude and phase modulated signal. Assume that a signal $s(t)$ suffers from a parasitic signal $d(t)$. For a good design, where the parasitic signal is much smaller than the signal, this ratio for the amplitude equals approximately:

$$\frac{S}{D}[a_r(t)] \approx \frac{a_s(t)}{a_d(t) \cos(\theta_s(t) - \theta_d(t))} \quad \text{for} \quad a_d(t) \ll a_s(t). \quad (2.12)$$

For the phase this ratio is approximately:

$$\frac{S}{D}[\theta_r(t)] \approx \frac{a_s(t)}{a_d(t) \sin(\theta_d(t) - \theta_s(t))} \quad \text{for} \quad a_d(t) \ll a_s(t) \quad (2.13)$$

Because the phases of both signals are not related, both are equal in strength. Therefore there is no advantage in choosing one particular domain. However, which domain

![Figure 2.11: Optimal coding for known and unknown interference.](image)
is chosen is very important for the circuit implementation of a system. When the phase domain is used, the linearity of a system is not very important, but the processing time must very consistent. When the amplitude domain is applied, linearity is very important. These implications are treated in Chapters 3 and 4.

2.5 Circuit Level

The circuit level is where functions like amplification, mixing, etc. are implemented. These functions are responsible for the creation of the required signal coding and for separation between signals in domains such as the time and frequency domain. This is the separation discussed in the previous section. There are types of compatibility problems that should be anticipated during circuit design, such as distortion of signals, crosstalk via power supply lines, and crosstalk between interconnections.

For optimal compatibility, parameters like amplitude and phase linearity are very important to minimize problems, e.g. intermodulation that deteriorates separation in the signal coding domain. For parasitic signals, this can be especially difficult, because a system is often not designed for the type of signals that interfere with it. For example, an audio amplifier that receives high-frequency parasitic signals from a cellphone should ideally be linear for the audio signal as well as the high-frequency interfering signal. This is very difficult to achieve in practice and special measures are required to maintain signal separation in the frequency domain (e.g., to prevent intermodulation).

The interconnections within a circuit can be divided in two classes: signal paths and power supply lines (biasing circuitry). These power supply lines are an additional network that connect all circuits within a system. Therefore, they can easily become a network for parasitic signal paths. To prevent interference problems, special care (a differential implementation) is required to isolate them from the signal paths.

Finally, EM coupling within a circuit layout must be anticipated during circuit design. This means that a good balance between sensitivity to signal corruption and emission has to be found when choosing the signal power (amplitude). In addition, the best suitable electrical domain (current or voltage) for the signal has to be chosen, because both differ in their sensitivity to emission and reception of parasitic signals.

These three types of design considerations are treated in more detail in Chapters 3 and 4.

2.6 Layout Level

The physical layout can be divided in two parts: the layout of the circuit components and that of interconnect. The circuit components are responsible for signal processing, while the interconnect transports signals between components. For optimal compatibility, the layout has to be optimized such that the EM interaction between signal paths is minimized. This means that the layout of the components has to be optimized such that the EM emission and reception at their interfaces with the interconnect (i.e., terminals) is minimized. The layout of interconnect has to be optimized such that EM interaction between signal paths is minimized.
Traditionally, the focus of layout tools is on the design of nets, where each net interconnects all component terminals that belong to the same circuit node. For example, the common ground is one net. For optimal compatibility, however, the focus must be on signal transport between components. Thus instead of nets, individual signal paths have to be designed. Therefore, layout tools and techniques are required that optimize the signal transport and minimize the EM interaction between signal paths. Chapter 5 presents models that describe the coupling between signal paths, and Chapter 6 presents design techniques for the optimization of a layout for signal transport. Chapter 7 presents a numerical method to analyze and verify the compatibility of the physical layout for a design.

2.7 Summary

To optimize the compatibility between systems, one must optimize the separation between the information signals they process in every domain available. For an electronic system, the available domains are the signal coding, electrical and spatial domains.

The optimal signal coding is one that is orthogonal to the parasitic signals such that a decoder can reject them. For unknown sources of interference, however, such a code cannot be found and the signal has to be distributed over the complete domain (as in spread spectrum) to minimize the chance of signal corruption. The circuit implementation must be optimized for the chosen signal codings to ensure their separation. Parasitic signals that are outside the signal range of a system require special attention.

To optimize separation in the spatial domain, (i.e., where signals are separated in signal paths), techniques can be applied that compensate for the interfering signals. In addition to this, the sensitivity of the electric signals to EM interaction can be reduced by using the separation between the current and voltage domain. Finally, the EM interaction between signal paths must be minimized. This implies that the layout design tools and techniques should focus on optimal design of signal paths instead of on nets.
Bibliography


Chapter 3

Circuit Modeling and Representation of EM Compatibility

A circuit design is an implementation of the diagram (system algorithm) of a system which describes the signal processing at the functional level. The position of circuit design within the design hierarchy is depicted in Figure 3.1. As indicated in this figure, the signals are given an electric representation (i.e., current, voltage) and the signal processing functions are given a circuit representation. To enable a designer to anticipate EM compatibility issues during the design of the circuit, the influence of these choices on the EM interaction and signal distortion needs to be evaluated.

This chapter determines the influence of these design choices and component limitations on the EM compatibility of a design. For this purpose, the component and interconnection models are extended for the EM interaction. To enable distortion
analysis, the nonlinear models of components are utilized. Chapter 4 uses this foundation to develop design techniques to optimize compatibility.

Section 3.1 determines the classes of compatibility problems and the circuit mechanisms that cause them. Section 3.2 extends the commonly used models of components and interconnections to include the EM interactions between them. Section 3.3 extends the small-signal model of nonlinear components for distortions mechanisms. Section 3.4 uses these extended models to determine the influence of circuit design choices, like electrical signal coding and differential circuit implementation, on the undesired EM interactions within a circuit. Finally, Section 3.5 determines how nonlinear circuits can be implemented such that distortion does not cause compatibility problems.

3.1 Circuit Level Compatibility Deterioration Mechanisms

As explained in Section 2.4.1, EM compatibility problems are caused by the loss of separation between signal paths (cross-talk) or within the signal coding domain (distortion, intermodulation). This section divides circuit design choices in classes, and determines their influence on the separation in these two domains for each class.

3.1.1 The Influence of Circuit Design Choices on Compatibility

The implementation of a system algorithm as a circuit design can be decomposed into three parts: electrical coding of the signals, circuit implementation of the signal paths (signal transport), and circuit implementation of the signal processing. These three parts are illustrated in Figure 3.2.

The electrical coding determines the electrical representation (e.g., current voltage) of the signal amplitude. Due to differences in the coupling mechanisms for current and voltage-domain signals, the chosen electrical domain can have a large impact on the EM crosstalk.

Signal paths are implemented by pairs of circuit nodes (positive and negative terminals). Each signal path can be assigned a separate pair of nodes (e.g., a differential implementation) or a they may share nodes (e.g., single-ended implementation). Due to the finite impedance of an implemented shared conductor (shared node), these choices can have a large impact on the EM coupling between paths.

Finally each system level function is implemented by a circuit diagram. This implementation not only determines the processing of desired signals, but also that of parasitic signals. Therefore this implementation determines the sensitivity of a circuit to detection of parasitic signals.

3.1.2 Partitioning of the Circuit Description

To enable EM-compatibility analysis during circuit design, the models of the applied components must describe the desired behavior as well as the mechanisms that cause compatibility problems. For this purpose, the design is decomposed in two
Partitioning of the Circuit Description

(a) Electrical coding of a signal.
(b) Circuit implementation of signal paths.
(c) Circuit implementation of signal processing functions.

Figure 3.2: Circuit implementation of a functional diagram.

parts (see Figure 3.3): circuit components and the interconnections). The existing

circuit models of both parts are extended for the mechanisms that can cause EM
compatibility problems. This partitioning has two advantages: the circuit nodes of
the original description have corresponding nodes in the extended description, so that
circuit analysis of both circuit descriptions can be readily compared. And the mod-
els of both parts are extracted separately. This is an advantage because both parts
require different analysis methods that are easily combined. Interconnect is mainly
responsible for parasitic signal transport, which is analyzed with the help of electro-
magnetic field analysis. Circuit components are responsible for nonlinear distortion of
signals, which is analyzed with the help of semiconductor physics. The circuit model
extraction of both parts is discussed in the next sections.
3.2 Modeling of EM Interactions Between Components and Interconnections

Interconnections transport signals within a system. Ideal interconnections have no transport time and no coupling with one another and are represented as circuit nodes. However, they suffer from EM interactions with each other in practice, have a finite transport time, and can act like a parasitic antenna that emits and receives EM signals. Circuit components are often a lot smaller, but their finite size also causes undesired EM interactions. To anticipate possible EM compatibility problems during circuit design, these effects have to be included in the circuit models of components. This section presents these model extensions.

The model is determined by the electrical size of a component. This is the size compared to the wavelength of the highest frequency component of a signal. For an electrically small layout (much smaller than this wavelength), the influence of the traveling time of a signal through a layout can be ignored, which enables the definition of an electric potential difference. For an electrically large layout, electrically small sub-domains have to be defined in which a local electric potential can be defined. This subject is treated in more detail in Section 5.2.3. The definition of electrically small can be given for the time as well as for the frequency domain. In the time domain the distance between two points is considered electrically small if the time it takes a signal to travel this distance can be neglected in comparison to the fastest transient of that signal. In the frequency domain a distance between two points is considered electrically small if it is much smaller than the wavelength of the highest frequency component of that signal. As an engineering approximation, a component is considered to be electrically small if it is less than one tenth of a wavelength. The EM interaction within electrically small layouts is most often described by a lumped-element network [1, 2], while the interaction within electrically large circuits is often represented by an extended version of this network [3], where electrically large components are divided into electrically small sub-parts that are represented by a distributed network. The advantage of such a description is that it can be analyzed by any circuit simulator. A drawback of these representations is that they become too complex to provide a designer insight in the coupling mechanisms within a large layout and are less suited for circuit extraction based on EM energy exchange. Circuit extraction based on EM energy exchange is a new method (presented in Chapter 7) aimed to improve the accuracy of the extracted circuit by using the EM energy exchange between components as a basis for calculating the circuit parameters. For this purpose, a port model is applied, which simplifies the circuit extraction and the circuit description by describing only the interaction between circuit components, and not between individual pieces of interconnect like a lumped element model does. This port model can be simplified even further in the case of weak EM-coupling and when circuits are electrically small in two or three dimensions, as described by the following subsections.

3.2.1 Simplified Modeling of EM Coupling

In Section 3.2.3 it will be shown that the coupling between any two components can always be represented by a port model. In many situations, however, systems are
weakly coupled due to separation by a large distance or shielding. For these situations, a simplified model can be derived that is much simpler to analyze. We derive this model for two coupled one-port components, but it can easily be extended for n-port coupled systems. Figure 3.4 depicts the exact representation of two components that suffer from EM interaction. The controlled sources in this figure are given by the

\[
\begin{align*}
U_1 &= Z_{11}I_1 + Z_{12}I_2 \\
U_2 &= Z_{21}I_1 + Z_{22}I_2,
\end{align*}
\]

where the transimpedances \( Z_{12} \) and \( Z_{21} \) describe the coupling and \( Z_{12} = Z_{21} \), assuming reciprocity (valid for passive devices). The EM interaction between the components does not only result in an interfering signal, as described by the transimpedance, but it also changes the input impedance. Thus, \( Z_{11} \neq Z_1 \) and \( Z_{22} \neq Z_2 \). To make this change visible within the circuit, voltages \( U_1 \) and \( U_2 \) are divided into a part caused by the original impedance and the portion induced by the EM interaction:

\[
\begin{align*}
U_1 &= Z_{11}I_1 + U'_1(I_1, I_2) \\
U_2 &= Z_{22}I_2 + U'_2(I_1, I_2),
\end{align*}
\]

Here \( U'_1 \) and \( U'_2 \) are caused by the EM interaction. This model is depicted in Figure 3.5. These controlled voltage sources can be described as:

\[
\begin{align*}
U'_1 &= Z'_{11}I_1 + Z_{12}I_2 \\
U'_2 &= Z_{21}I_1 + Z'_{22}I_2
\end{align*}
\]

Here, \( Z'_{11} \) and \( Z'_{22} \) are the changes in the input impedance due to coupling. This representation separates the influence of the EM interaction (\( U'_1 \) and \( U'_2 \)) from the desired circuitry but is still exact. These changes are caused by reflection of the emitted signal by the neighboring component. This reflected signal travels the paths between the two components twice, therefore a weak coupling allows us to ignore
this reflected signal. The interaction in this approximation is represented by the transimpedances only:

\[
U'_1 = Z'_{11}I_1 + Z_{12}I_2 \approx Z_{12}I_2, \quad (3.7)
\]

\[
U'_2 = Z_{21}I_1 + Z'_{22}I_2 \approx Z_{21}I_1. \quad (3.8)
\]

The resulting weak coupling approximation is often used to represent the received interference from an external transmitter as depicted in Figure 3.6. Due to the large distance between the transmitter and the circuitry it interferes with in Figure 3.6(b), the influence of the interaction on the radiation impedance of the antenna and the impedances of the circuit components can be ignored. Only the received interference needs to be taken into account (source \(U_d\) in Figure 3.6(c)). In this approximation,

![Diagram of a circuit that is interfered by a radio transmitter](a) A circuit that is interfered by a radio transmitter.

![Diagram of a component that is weakly coupled a radio transmitter](b) A component that is weakly coupled a radio transmitter.

![Diagram of modeling of weak external coupling](c) Modeling of weak external coupling.

Figure 3.6: Approximated circuit model of components weakly coupled to external circuitry.

the two system are analyzed independently (i.e., superposition applies). This approximation makes it possible to specify EM compatibility requirements for each individual apparatus.

### 3.2.2 Representation of Radiating and Receiving Electrically Large Circuits

The weak coupling approximation of the previous section can be extended to a representation that includes radiation as well. The reception is represented by the source \(U_d\) from the weak coupling approximation shown in Figure 3.6. An approximation
of the radiated far-field is made with the help of the radiated power (which is explained in Section 7.2.3). The radiated power is found by separating the radiation resistance from the network impedance. In a matrix description of a port model, this is described as follows:

$$\hat{U} = \hat{Z}^i \hat{I} + R^A \hat{I} + \hat{U}_d,$$

(3.9)

where $\hat{U}$ and $\hat{I}$ are vectors that describe the port voltages and currents of the system, $\hat{Z}^i$ is the impedance matrix of the system without radiation losses, $R^A$ is the radiation resistance matrix of the network, and $\hat{U}_d$ is the vector of received voltages. This follows from the transimpedance with the external system as described in Figure 3.6. With this representation, the radiated power is given by:

$$P_{rad} = \frac{1}{2} \hat{I}^H R_a \hat{I},$$

(3.10)

where $H$ is the Hermitian operator that determines the complex conjugate transpose of a vector or matrix. Note that for a one-port system, this expression reduces to $P_{rad} = \frac{1}{2} |\hat{I}|^2 R_a$, the power dissipated by a radiation resistor.

### 3.2.3 Modeling of Three-Dimensional Electrically Large Components

In Section 5.2.3, it is shown that as soon as a phase difference arises between the two terminals of a component due to the time delay of a signal (e.g., between two circuit nodes), the voltage difference between them and the current through the component are not defined. Both can be defined if the distance between the terminals is electrically short, so that the phase difference is negligible. This approximation is often called the quasi-static approximation, because the electromagnetic fields between the terminals are approximated as static, but time-varying fields.

For an electrically large circuit layout, this implies that the electric potential cannot be defined between any two points in the layout. To solve this problem, we define electrically small islands around the terminals of the circuit components (as depicted in Figure 3.7), in which the electric potential and current are defined locally. Due to the electrically large distance between ports 1 and 2 in Figure 3.7, it is not possible to define a voltage difference between one terminal of port 1 and one of port 2. The interaction between these ports can be described by a port model as depicted in Figure 3.8. This port model describes the interaction between the components within the electrically small islands by a matrix description (e.g., an impedance, admittance or scattering matrix description). It should be noted that this model is only accurate if the port domains are electrically small. In the Chapters 5 and 7, the parameters of this port model are calculated.

### 3.2.4 Modeling of One-Dimensional Electrically Large Components

One-dimensional electrically large components like transmission lines, quarter-wavelength transformers, coupled lines, etc., can often be described by a transmission line or an ensemble of transmission lines as described in literature [4, 5]. This transmission line
Figure 3.7: electrically large system with locally defined ports.

Figure 3.8: One-, two- and n-port representation of circuit components and interconnect.
description is a port model, like the ones we presented in the previous section. It
only describes the transfer between the ports at both ends of the line, while a voltage
difference between two end points of the line cannot be defined due to the electrically
large length of the connection.

For EM compatibility analysis, the transmission line model needs to be extended
to capture EM interaction with other components. Strong EM interaction between
connections in parallel, for example in a bundled cable, can be described by coupled
lines. This is already well covered by transmission line theory (see for example [6]).
Well-designed electrically long connections are often only weakly coupled to other
components, such that the approximation explained in Section 3.2.1 can be applied.
Figure 3.9 shows two weakly coupled lines, where the received signals are described
by controlled voltage sources. The radiated power is part of the transmission line

\[
\begin{align*}
 \mathbb{U}_1(I_1, I_2) & \quad \mathbb{U}_2(I_3, I_4) \\
 I_1 & \quad I_2 \\
 \mathbb{U}_3(I_5, I_6) & \quad \mathbb{U}_4(I_7, I_8) \\
 I_5 & \quad I_6 \\
 \end{align*}
\]

Figure 3.9: Modeling of weakly coupled lines.

losses. It must be noted that radiation losses do not scale linearly with the length of
line. Therefore, it is not possible to define a radiation resistance per unit length. In
Chapter 5, it is shown that for an electrically short line the radiation losses increase
quadratically with the length.

3.2.5 Modeling Electrically Small Components

The EM interaction between electrically small interconnections and components can
be approximated by lumped-element circuit models. Because of the electrically small
dimensions, the electric field interactions (i.e., displacement currents) and the mag-
netic field interactions (i.e., induced voltages) are, to first order approximation, in-
dependent. Figure 3.10 shows the model extension of two coupled components. Any
magnetic interaction between the current loops in a circuit is described by self-
inductance \( L \) and mutual inductances \( M \), while displacement currents are de-
scribed by capacitors. The weak coupling to an external transmitter is described by
controlled voltage sources \( U_{d1} \) and \( U_{d2} \) as explained in Section 3.2.1. The radiated
fields are determined by the radiated power, which follows from the radiation resis-
tances \( R_A \). The calculation of these circuit parameters is treated in Chapter 5. More
information about model extension of electrically small components can be found in
Goedbloed [7] and Paul [4].
In conclusion, a lumped-element model can only be derived for electrically small circuit layouts. The interaction within an electrically large circuit is described by a port model that describes the interactions between electrically small islands that are defined in the layout. If the coupling is weak, reflected fields can be ignored such that coupling is represented by controlled sources that are independent of the system they interfere with.

### 3.3 Modeling Circuit Nonlinearities

Nonlinearities are often an undesired side effect that causes deformation (distortion) of signals, which can lead to compatibility problems like inter-modulation. The nonlinear components can be intentionally nonlinear, like diodes etc., or unwanted: when it is due to a nonlinear conductivity, permittivity or permeability of the materials they are made of, or due to undesired nonlinear junctions like corroded contacts (see [8]). The commonly applied circuit models of nonlinear components describe their linearized dynamic behavior (i.e., hybrid-π model of transistors) or their static nonlinear behavior, but do not describe their dynamic nonlinear behavior. The response of a nonlinear system to a parasitic signal can only be determined with the help of a circuit simulator (e.g., Spice, Spectre™, etc.). However, such simulations provide little insight in the mechanisms that cause compatibility problems and are often very inefficient. For example, to determine the quadratic detection of a high-frequency signal, they require a very long transient simulation. To develop and optimize a circuit topology for EM compatibility, we need simple design models that represent the dynamic nonlinear behavior. Therefore we have extended the existing small-signal models of nonlinear components for nonlinear distortion.

The main problem of dealing with nonlinear dynamic systems is that the superposition principle does not hold, so that its analyses cannot be readily decomposed into simpler parts. The two most promising methods to deal with this problem are: application of Volterra approximation (see [9]), and describing the stationary nonlinear circuit as a time-varying linear circuit (see [10, 11, 12, 13, 14, 15, 16]). The Volterra approximation is best suited for distortion analyses (see [17, 18]). With the help of the Volterra expansion, the distortion can be represented by additional sources that are added to the small signal linearized circuit representation of components (e.i.,
hybrid-π model of transistors). Figure 3.11 shows an example of an extended small signal model of a junction diode. The admittance $\hat{Y}_{\text{diode}}$ of the diode is approximated by a first-order Taylor expansion, linearized around the center frequency $\omega_c$:

$$\hat{Y}_{\text{diode}}(\omega, \omega_c) = \frac{1}{\tilde{R}(\omega_c)} - \frac{1}{j(\omega - \omega_c)\tilde{C}(\omega_c)} + j\omega \tilde{C}_C.$$ \hfill (3.11)

In this equation $\tilde{R}$ is the diffusion resistor, $\tilde{C}$ the diffusion capacitance, and $\tilde{C}_C$ the junction capacitance. For a zero-center frequency ($\omega_c = 0$) $\tilde{R}$ and $\tilde{C}$ equal the diffusion resistance and capacitance that is commonly specified for junction diodes (see [19, 20]). The controlled current source $\hat{I}_{dd}(j\omega)$ represents the nonlinear part of the diode current, which is responsible for the distortion of a signal. Appendix A describes how this current can be determined with the help of the Volterra approximation. Appendix B describes the extended hybrid-π model of a bipolar transistor.

### 3.4 The Effects of Circuit Design Choices on EM Interaction

The EM coupling within a circuit and between circuits is determined by the layout of the components and interconnections. The influence of this EM interaction on crosstalk between signals, however, is determined by the circuit implementation and electrical coding of signals. For example, a current-domain signal is only sensitive to current-domain parasitic signals.

This section uses the models presented in Section 3.2 to determine the influence of circuit design choices on the EM compatibility of a design. These results are used in Chapter 4 for optimization of the compatibility.

#### 3.4.1 Causes of Parasitic Signal Paths

The interconnections transport signals and power within a system. Compatibility problems can arise when part of the signal energy arrives at the wrong destination (e.g., due to crosstalk). This section gives an overview of the causes; the next sections analyze these causes in more detail.

We distinguish between difference- and common-mode signals and signal paths. Both types are illustrated in Figure 3.12. The desired signal and power supply paths are difference-mode paths; all remaining paths are common mode with respect to these desired paths, and are therefore called common-mode paths. In this figure, the signals $S_1$ and $S_2$ are difference-mode signals. The six conductors that connect these circuits implement five signal paths: two desired signal paths, one power supply, and
two redundant (unused) paths. Parasitic signals $S_{\text{par};2}$ and $S_{\text{par};3}$ travel by these redundant paths, and are common mode with respect to the desired paths. The parasitic signal current ($I_{CM_{\text{par};3}}$ of $S_{\text{par};3}$, for example) is a common-mode current for the two signal paths.

![Circuit Diagram](image)

**Figure 3.12: Deterioration of compatibility of the topology.**

Coupling between paths can be galvanic, via the impedance in a common lead (i.e., common ground) or non-galvanic, via EM coupling only. Four types of coupling are distinguished: undesired non-galvanic and galvanic coupling between common-mode signal paths, and undesired non-galvanic and galvanic coupling between difference-mode signal paths. These four types are treated in the next section. The coupling between common- and differential-mode paths is not treated explicitly, because this mechanism is a difference-mode coupling mechanism. Common-mode paths may be galvanically or non-galvanically coupled to difference-mode paths, in the same way as difference-mode paths are coupled to one another, as described in the next sections.

### 3.4.2 Galvanically-Coupled Common-Mode Paths

Common-mode paths are redundant. They are deliberately created paths that do not transport signals or power. They arise when more conductors are applied to implement the paths than is necessary. Figure 3.13 illustrates the implementation of signal paths, which includes power supply paths as well.

The system topology in Figure 3.13(a) can be implemented with maximal redundancy (as depicted in Figure 3.13(b)), so that common-mode (redundant) paths arise like the one used by parasitic signal $S_{\text{par};1}$. Every signal path is assigned its own pair of conductors. In Figure 3.13(c), all common-mode paths are eliminated by letting all paths share conductors. In general, the number of (redundant) common-mode paths $N_r$ is:

$$N_r = N_c - N_s - 1,$$

(3.12)

where $N_c$ is the number of conductors applied to implement the $N_s$ signal and power supply paths. Common-mode (redundant) paths are introduced to eliminate coupling by shared conductors (e.g., common ground). However, this requires good isolation between the redundant ports and the signal ports in each sub-circuit. For example, parasitic signal paths $S_{1\text{par};1}$ and $S_{2\text{par};1}$ in Figure 3.13(b) have to be eliminated. Therefore, a trade-off exists between the isolation of common-mode and difference-mode paths one the one hand and coupling by a shared conductor on the other.
3.4.3 Non-Galvanically Coupled Common-Mode Paths

The previous section treated common-mode paths that were caused by galvanic coupling. In addition to this, EM interaction between paths causes non-galvanic common-mode coupling. While redundant paths are often anticipated in a design (power supply rejection, etc.), non-galvanic coupling is easily overlooked. For example, the digital interface to an analog sensor shown in Figure 3.14 can suffer from this type of coupling. Due to common-mode EM coupling between the sensor wires and the digital output, a common-mode signal \( U_{cm;1} \) at the output induces a common-mode current \( I_{cm;1} \) at the input and output of the interface.

Figure 3.15(a) shows a generic model for common-mode coupling within a circuit. Common-mode sources \( U_{cm;1} \) and \( U_{cm;2} \) are the parasitic voltage signals induced by common-mode currents \( I_{cm;1} \) and \( I_{cm;2} \):

\[
U_{cm;1} = Z_{CM;11}I_{cm;1} + Z_{CM;12}I_{cm;2} \\
U_{cm;2} = Z_{CM;21}I_{cm;1} + Z_{CM;22}I_{cm;2},
\]  

(3.13)  

(3.14)
(a) Generic model of common-mode coupling.

(b) Strongly coupled electrically short interconnect.

Figure 3.15: Models for common-mode coupling.
Circuit design choices and EM interaction

(a) Difference-mode coupled paths.

(b) Model of electrically small coupled paths.

Figure 3.16: Difference-mode EM coupling.

where $Z_{CM;11}$ and $Z_{CM;22}$ are the impedances of the parasitic common-mode dipoles in Figure 3.15, and $Z_{CM;12}, Z_{CM;12}$ are transimpedances that describe the coupling between the two common-mode dipoles ($Z_{CM;12} = Z_{CM;21}$ because of reciprocity). When the connections are electrically small, the lumped-element model of Figure 3.15(b) can be applied, which models the coupling with capacitances and mutual inductances as determined using a computer simulator [21, 3].

In contrast to difference-mode coupling, this common-mode coupling is very difficult to eliminate during layout design. Therefore, it needs to be anticipated during the circuit design process. This means that common-mode signals in connection have to be minimized by carefully balancing signals, while common-mode ports within the circuit design (as illustrated in Figure 3.13(b)) must be eliminated by a differential implementation and a high common-mode rejection ratio.

3.4.4 Galvanic Difference-Mode EM Coupling

Difference-mode coupling is direct coupling between signal paths, as illustrated in Figure 3.16. Figure 3.16(b) shows a model of electrically small coupled paths. If the paths are small enough they, can be considered coupled loops, where the coupling can be described as:

\[
U_{dm;1} = Z_{DM;11}I_{dm;1} + Z_{DM;12}I_{dm;2}
\]

(3.15)

\[
U_{dm;2} = Z_{DM;21}I_{dm;1} + Z_{DM;22}I_{dm;2},
\]

(3.16)

This model can be applied for galvanically coupled and non-galvanically coupled interconnects. It must be noted that the two coupled paths in Figure 3.16(a) form a four-port network, which we approximate as two coupled one-port networks.
Because the parasitic signals are immediately added to the signal paths, they cannot be as easily discriminated during circuit design. However, by choosing the right electrical coding, interaction can be minimized. This section determines the electrical coding for paths that are coupled by a shared conductor; the next section treats non-galvanically coupled paths.

Coupled Electrically Short Interconnects

To determine the influence of electrical coding, we determine the signal-to-interference-noise ratio for current and voltage domain signals between two coupled signal paths. For electrically small connections, the lumped-element model depicted in Figure 3.4.4 is used. Galvanic coupling arises when the currents of two or more signal paths share the same conductor. A signal in one path induces currents and voltages in this shared conductor, which acts as a parasitic source for the neighboring path. Because the impedance of this shared conductor dominates the inductive or capacitive coupling, the signal-to-interference-noise ratio of signal path 1 to signal path 2 due to coupling can be approximated by:

\[
(S/N)_{U_{L1}} \approx \frac{|1 + j\omega C_{2l} Z_{S2}|^2}{|1 + j\omega C_{1l} Z_{S1}|^2} \frac{|Z_{S2}/[(sC_{2l})^{-1} + Z_{L2}/(sC_{2l})^{-1}]| |U_{S1}|^2}{|Z_{gc} + j\omega[(C_{C1} + C_{CL}) Z_{L2} Z_{S1} + L_C]|^2 |U_{S2}|^2}. \tag{3.17}
\]

When both signal paths are in the voltage domain such that \(Z_L \gg Z_S\), this ratio is given by:

\[
(S/N)_{U_{L1}} \approx \frac{|Z_{L2}/[(s(C_{2l} + C_{2l})]^{-1}]| |U_{S1}|^2}{|Z_{gc} + j\omega[(C_{C1} + C_{CL}) Z_{L2} Z_{S1} + L_C]|^2 |U_{S2}|^2}. \tag{3.18}
\]

When both signals are in the current domain such that \(Z_L \ll Z_S\), this ratio is given by:

\[
(S/N)_{I_{L1}} \approx \frac{|Z_{S2}/[(s(C_{2l} + C_{2l})]^{-1}]| |Z_{S1} Z_{L2} I_{S1}|^2}{|Z_{gc} + j\omega[(C_{C1} + C_{CL}) Z_{L2} Z_{S1} + L_C]|^2 |Z_{S2} Z_{L1} I_{S2}|^2}. \tag{3.19}
\]

The best isolation is obtained when both signal paths are in either the current or the voltage domain. However, when one path carries a current-domain signal while the
other is in the voltage domain, it can be readily seen that the path in the current
domain receives almost no parasitic signal, while the signal in the voltage domain
suffers severely from the current domain’s parasitic signal. Hence, current-domain
signals have the highest immunity, but also the highest emissions. The reverse is true
for voltage-domain signals. A voltage domain signal has low emissions, because of
the negative reflection coefficient of a voltage detector. The emission of the reflected
signal is anti-phase to the emission of the input signal and tends to reduce it.

### 3.4.5 Non-Galvanic Difference-Mode Coupling

In the case of non-galvanic EM coupling (which is depicted in Figure 3.18), the EM
coupling is a lot weaker than via a shared conductor. This coupling is (in princi-
ple) only caused by mutual inductance, \( M \), and capacitance \( C_M \). The signal-to-

\[
\left( \frac{S}{N_d} \right)_{ZL1} \approx \frac{|U_{S1}|^2}{|U_{S2}|^2} \frac{|(j\omega C_M)^{-1}(Z_{S2} + j\omega L_2 + Z_{L2}) - j\omega M Z_{L2} + Z_{L2}(Z_{S2} + j\omega L_2)|^2}{|j\omega M(Z_{L2} + (j\omega C_M)^{-1}) - Z_{L2}(Z_{S1} + j\omega L_1)|^2}. \tag{3.20}
\]

For signal transport in the current domain \((Z_L \ll Z_S)\), this equation reduces to:

\[
\left( \frac{S}{N_d} \right)_{ZL1} \approx \frac{|I_{S1}|^2 |(j\omega C_M)^{-1} + Z_{L2}|^2}{|I_{S2}|^2 |Z_{L2}|^2}. \tag{3.21}
\]

For current-domain signal transport, we note that the detector (load) must have a
much lower impedance than the differential capacitive coupling between the paths.
For signal transport in the voltage domain \((Z_L \gg Z_S)\), this equation reduces to:

\[
\left( \frac{S}{N_d} \right)_{ZL1} \approx \frac{|U_{S1}|^2 |(j\omega C_M)^{-1} - j\omega M + Z_{S2} + j\omega L_2|^2}{|U_{S2}|^2 |MC_M Z_{L2} + Z_{S1} + j\omega L_1|^2}. \tag{3.22}
\]

For voltage-domain signal transport, we note that the source must have a much lower
impedance than the differential capacitive coupling between the paths. Again, the
isolation between the paths is optimized when the signals are transported either only
in the current or voltage domain. When one path uses current-domain signals while
the other uses voltage-domain signal transport, the current-domain signal is least
affected by any interference.
3.4.6 Coupled Electrically Long Interconnections

Coupled electrically long interconnections can be modeled by coupled transmission lines. These signal paths do not allow for current or voltage-domain signal transport, because after traveling a quarter of a wavelength, a voltage signal becomes a current signal and vice versa. However, the transmission line impedances can be chosen in advance by the designer and have an influence on the EM interaction. This section determines the influence of these design choices.

We analyze two lossless coupled lines. The differential equations that describe the signal transport by such lines can be represented by the circuit representation shown in Figure 3.19. The differential equations that describe the currents and voltages in these two lines are given by:

\[
\partial_x \begin{bmatrix} \hat{U}_1(x) \\ \hat{U}_2(x) \end{bmatrix} = -j\omega \begin{bmatrix} L_1 & L_M \\ L_M & L_2 \end{bmatrix} \begin{bmatrix} \hat{I}_1(x) \\ \hat{I}_2(x) \end{bmatrix},
\]

(3.23)

\[
\partial_x \begin{bmatrix} \hat{I}_1(x) \\ \hat{I}_2(x) \end{bmatrix} = -j\omega \begin{bmatrix} C_1 & C_M \\ C_M & C_2 \end{bmatrix} \begin{bmatrix} \hat{U}_1(x) \\ \hat{U}_2(x) \end{bmatrix}.
\]

(3.24)

where \(L_1, L_2, C_1, C_2\), are the inductance and capacitance per unit length for the two lines, and \(L_M, C_M\) are the mutual inductance and capacitance. Hence, the lumped-network elements of the short coupled lines model are replaced by distributed elements.

In a single transmission line, two individual signals can propagate: one traveling forward and one in the reverse direction. Through each line of two coupled transmission lines, however, four individual signals can propagate. Two signals can propagate in each direction with different speeds and line impedances. To get an impression of the signal-to-disturbance ratio, we determine the signal-to-disturbance ratio of a symmetrically coupled line \((L_1 = L_2 = L, C_1 = C_2 = C)\). In this situation, the two sets of traveling signals are the common-mode and differential-mode signals. If we assume that \(L_m \ll L, C_m \ll C\), while the source and load are both matched to the common-mode line impedance \(Z_c = \sqrt{\frac{L+L_m}{C+C_m}}\); the voltage across load \(Z_{L1}\) is

![Figure 3.19: Circuit representation of coupled lines.](image-url)
approximately given by:

\[
U_{L1} \approx \frac{e^{-\hat{\gamma}_c L}}{4} \left( U_{s1} \left[ 2 + \frac{L}{L_m} - \frac{C}{C_m} + j\omega \sqrt{LC} \left( \frac{L}{L_m} + \frac{C}{C_m} \right) \right] - U_{s2} \left[ \frac{L}{L_m} - \frac{C}{C_m} + j\omega \sqrt{LC} \left( \frac{L}{L_m} + \frac{C}{C_m} \right) \right] \right),
\]

where \( \hat{\gamma}_c \) is the common-mode propagation constant, given by:

\[
\hat{\gamma}_c = j\omega \sqrt{\frac{L + L_m}{C + C_m}}.
\]

The signal-to-interference-noise ratio due to coupling is approximately:

\[
\frac{U_{L1}(U_{s1})}{U_{L1}(U_{s2})} \approx -\frac{U_{s1}}{U_{s2}} \frac{2 + \frac{L}{L_m} - \frac{C}{C_m} + j\omega \sqrt{LC} \left( \frac{L}{L_m} + \frac{C}{C_m} \right)}{\frac{L}{L_m} - \frac{C}{C_m} + j\omega \sqrt{LC} \left( \frac{L}{L_m} + \frac{C}{C_m} \right)} \approx -\frac{U_{s1}}{U_{s2}} \frac{2}{\frac{L}{L_m} - \frac{C}{C_m} + j\omega \sqrt{LC} \left( \frac{L}{L_m} + \frac{C}{C_m} \right)}. \]

Hence, the coupling is determined by the ratios of the mutual inductance and capacitance and the self-inductance and capacitance of the lines (\( \frac{L}{L_m} \) and \( \frac{C}{C_m} \)). In practice, this means that the coupling is determined by the ratio of the distance between the transmission lines and the distance between the conductors of any one line. For frequencies above \( \frac{1}{2\pi \sqrt{LC}} \), the coupling increases with frequency. Thus, the lower the characteristic impedance, the smaller the coupling if the separation is kept the same.

Thus, for electrically small interconnects, current-domain transport is the least sensitive to interference. The voltage-domain signal generates the least emission. For electrically long interconnects, a low transmission line impedance tends to minimize coupling between lines at the cost of power consumption.

### 3.4.7 Coupling between Current and Voltage Domains

In the previous sections, it was shown that separation between signals in electrically short circuits can be optimized by transferring them in either the current or voltage domain. However, the current or voltage detector required seems physically impossible, because it not does take any energy from the signal. This section qualitatively discusses how separation between these two domains can be approximated, and what factors deteriorate this separation.

Both an ideal current and an ideal voltage detector reflects all of the signal energy received. Detecting without consuming energy is not possible, but in Appendix C it is shown that this ideal behavior can be imitated with the help of feedback. In a voltage or current amplifier, the circuit detects a signal and uses its energy. The feedback network copies the detected signal and sends it back, thereby compensating the consumed signal energy. Hence, the feedback network mimics the reflection mechanism. The same argument holds for an ideal current or voltage source that also uses feedback to create a zero or infinitely large impedance. Feedback is therefore essential to separate the voltage and current domains. It is the limited loop gain and bandwidth of the feedback loop that limits this separation.
The second mechanism that deteriorates the separation between current and voltage domains is electrical size. This is illustrated with the help of the transmission line model shown in Figure 3.20. In this figure, symbol $\Gamma_d$ is the reflection coefficient of the detector, where $\gamma$ is the propagation coefficient of the transmission line. During transport, signal energy is converted from a voltage (electric field domain) to a current (magnetic field domain) and vice versa. As this figure shows, the current and voltage at the input of the line do not equal those at the output of the line. For very short interconnections ($e^{-\gamma L} \approx 1$) this difference can be ignored. For longer interconnects, however, it affects the isolation between the two domains. Therefore, separation between the current and voltage domains depends on feedback to imitate current or voltage sources and detectors and requires electrically short interconnections.

Because of the immunity to induced voltages, current-domain signals are applied in process industry in almost all analog sensors. Also in integrated circuits, reference signals are most often transported in the current domain for the same reason.

### 3.5 Deterioration of Coding Compatibility

Nonlinear behavior of a circuit causes compatibility problems when it causes parasitic and desired signals to become indistinguishable, for example when a parasitic signal causes an amplifier to clip or when quadratic detection demodulates an AM modulated parasitic carrier. As explained in Section 2.4.2, to prevent these compatibility problems, the transfer of a system must be reversible, so that the original signal can be recovered. This section describes the requirement a circuit topology must meet to ensure reversible transfer.

The exponential transfer of a bipolar transistor and the quadratic transfer of a MOS and JFET transistor are reversible within their operating range. To determine which topologies ensure a reversible transfer, we consider three basic configurations of these nonlinear components: a cascade of nonlinear operations; addition (or subtraction) of nonlinear operations; and multiplication of nonlinear operations. The latter two operations correspond to the four basic operations of addition, subtraction, multiplication, and division (multiplication with the inverse operation). Therefore any other topology can be decomposed into these three operations. Figure 3.21 illustrates these three operations and shows an example implementation for each of them. It can be readily shown that a cascade of nonlinear operations as depicted in Figure 3.21(a) is always reversible if each of the nonlinear operations is reversible. A transfer that
Deterioration of Coding Compatibility

Figure 3.21: Three basic combinations with nonlinear components.

consists of more than one added or multiplied stages in parallel (Figure 3.21(b) and Figure 3.21(c)) is not necessarily reversible. For example, the functions $y = ae^x + be^{-x}$ and $y = a \ln(x)be^{-x}$ are not injective and therefore can lead to loss of information.

Thus separability can be lost due to a nonlinear operation if:

- the input signal range of a nonlinear component is exceeded (saturation, frequency limitation); or
- a static non injective transfer is created by combining two or more nonlinear operations in parallel (see Figure 3.21(b) and 3.21(c)).

These are the only possible situations that can lead to non-reversible signal operations. Therefore saturation must be prevented and special care is required when implementing nonlinear operations in parallel. It must be noted that although after a nonlinear operation, a parasitic signal may be theoretically separable from the intended signal, in practice it can be very hard to implement.

3.6 Conclusions

Deteriorating compatibility between two or more systems is caused by the leakage of signal energy between the systems due to crosstalk or distortion. Figure 3.22 illustrates the possible causes.

Crosstalk is caused by undesired EM interaction between interconnections and components, and by signal transport over deliberately created common-mode (redundant) signal paths. The difference-mode EM interaction between signal paths is minimized by choosing current-domain signals. This requires electrically short interconnections and circuits that with the help of feedback imitate ideal current sources
and detectors. Common-mode EM interaction and the transport along common-mode paths is minimized by the rejection of common-mode signals and the elimination of common-mode currents. In contrast to difference-mode EM interaction, common-mode EM interaction is difficult to eliminate in a layout, and therefore it must be minimized during circuit design.

Distortion can cause a loss of separation in the coding and modulation domains. This is prevented by implementing only reversible nonlinear operations. Therefore limiting and clipping has to be prevented, and special care is required when implementing sums or products of nonlinear operations.
Bibliography


Chapter 4

EM Compatible Circuit Design

To improve the compatibility of a circuit design, both loss of separation in signal coding due to distortion (like intermodulation) and unintentional signal transport (like crosstalk) have to be reduced. This chapter presents design techniques to accomplish both. Because the focus of this thesis is on integrating layout and circuit design, which are treated specifically in the next chapters, this chapter only treats design principles that improve compatibility of circuit design. Optimization of particular circuit functions is left for future research.

Section 4.1 presents a design strategy that decomposes the circuit design procedure into smaller more readily solvable steps. Section 4.2 treats the minimization of unintentional signal transport (like crosstalk). The minimization of loss of separation in signal coding domain (like intermodulation) due to distortion is treated in Section 4.3. Finally Section 4.4 presents a design example to illustrate these techniques.

4.1 Circuit Design Approach for Optimal Compatibility

A circuit design is the implementation of a system or subsystem. To simplify the design procedure, we decompose it in two design phases: electric system design and circuit design. The electric system design focuses on minimization of EM interaction (like crosstalk), while the circuit design is focused on minimization of compatibility problems due to non-linearities, as will be explained in this section. Figure 4.1 gives an overview of the design procedure. At the coding and modulation level (which was treated in Chapter 2), compatibility is optimized by the separation of desired and parasitic signals by their signal coding. The electric functional diagram is a refinement of the functional diagram, where all functions are implemented with the help of basic sub-circuits (e.g., amplifiers, mixers, etc.) that can be readily implemented in a circuit. It should therefore meet the same requirements as the functional diagram which was treated in Section 2.4 (e.g., optimize separation in signal coding domain). Such a diagram defines the implementation of all signal paths between functions (e.g.,
balanced or unbalanced, use of shared conductors, etc.) and the electric coding of signals (i.e., current or voltage domain). These design choices should minimize EM interaction like crosstalk. During the circuit design phase, the basic sub circuits are implemented. These determine the quality of the signal processing (like linearity, etc.) and isolation of redundant paths as qualified by the common mode rejection. This design phase is used to minimize compatibility problems caused by distortion.

Thus improvement of signal coding and processing and the minimization of EM interaction (like crosstalk) is mainly achieved during implementation of the electric system diagram. Minimization of compatibility problems due to distortion and isolation of redundant (common mode) signal paths is mainly implemented during circuit design. Both design phases are treated in more detail in the following sections.

4.2 The Design of Compatible Signal Paths

During implementation of the electric function diagram (see Figure 4.1), the signal path topology and electrical coding are determined. In Section 3.4.1 it was shown that these design choices impact the sensitivity of a circuit to EM interaction. However they also influence the complexity and cost of a design. The minimization of undesired EM interaction within a circuit requires elimination of conductors that are shared between signal paths (e.g., a fully differential implementation). Such an implementation however may be more expensive due to the printed circuit board (PCB) area or chip area required for the extra interconnections. In this section, the minimum number of interconnections required for an EM compatible implementation are determined. It should be noted that upper limits on the EM coupling allowed between signal paths are determined from (predefined) EMC requirements. These upper limits are the boundary conditions required for the design of an EM compatible layout.

4.2.1 Design of the Signal-Path Topology

A design with the minimal number of connections is obtained by letting all signal paths share conductors (for example using a common ground). The coupling that arises between the paths due to the impedance in these common leads, may render an incompatible circuit. Therefore, additional conductors are introduced for two reasons: 1) reduction of coupling between paths (by elimination of shared conductors), and 2) enabling the discrimination of parasitic signals that are induced in the interconnect. The common leads should only be eliminated if their impedance exceeds
the maximally allowable shared impedance that follows from the required signal to interference noise ratio determined from predefined EMC requirements.

To eliminate parasitic signals that induced in the interconnect, the minimum number \( N_{\text{req}} \) of paths required equals the sum of the desired \( N_{\text{des}} \) signal paths for signal transport and the number of parasitic signals \( N_{\text{par}} \):

\[
N_{\text{req}} = N_{\text{des}} + N_{\text{par}} \quad (4.1)
\]

This minimum \( N_{\text{req}} \) is obtained when the signals transported by the paths are linearly independent. In practice, the distance between the paths is often small enough to assume that they all receive the same parasitic signal \( N_{\text{par}} = 1 \). Figure 4.2 illustrates the design procedure for two signal paths (carrying signals \( S_1, S_2 \)) that suffer from one external interferer \( S_D \). To enable discrimination of the interference, these paths are implemented using three signal paths (four conductors) as given by (4.1). The matrix operations \( M \) and \( M^{-1} \) ensure elimination of the interference signal. The signals \( x_1 \cdots x_3 \), transported by these paths are given by:

\[
\begin{bmatrix}
  x_1 \\
  x_2 \\
  x_3 
\end{bmatrix} =
\begin{bmatrix}
  M_{11} & M_{12} \\
  M_{21} & M_{22} \\
  M_{31} & M_{32} 
\end{bmatrix}
\begin{bmatrix}
  S_1 \\
  S_2 
\end{bmatrix} +
\begin{bmatrix}
  C_1 \\
  C_2 \\
  C_3 
\end{bmatrix} S_D,
\]

(4.2)

where \( C_1 \cdots C_3 \) are the coefficients the describe the coupling between the interference signal \( S_D \) and the signal paths. For optimal separation, the signal path encoding coefficients \( M_{i,j} \) are chosen such, that the desired and interfering signals are orthogonalized. The interaction is minimized when each path in the circuit design is assigned to two neighboring conductors, so that the surface area enclosed by the current loop of the signal paths (see Section 6.1.1) is minimized. For example the following choices are made: \( x_1 = S_1 \left( M_{11} = 1 \right) \) and \( x_3 = S_2 \left( M_{32} = 1 \right) \). Because no signal is applied to signal-path 2 \( \left( M_{21} = M_{22} = 0 \right) \), signal \( x_2 \) equals the received parasitic signal \( \left( C_2 S_D \right) \). The inverse matrix \( M^{-1} \) therefore equals:

\[
M^{-1} =
\begin{bmatrix}
  1 & -C_1C_2^{-1} & 0 \\
  0 & -C_3C_2^{-1} & 1
\end{bmatrix}
\]

(4.3)

In this example, only the influence of the external interferer has been eliminated. To reduce the influence of coupling via the common leads, additional conductors are required.

![Figure 4.2: Two connected circuits with external disturbance source.](image-url)
4.2.2 Design of Electrically-Short Signal Paths

Because the signal transport time can be ignored for electrically short paths, the coupling between them can be represented by lumped elements. This description is used to determine layout requirements of electrically short paths.

To obtain an EM compatible layout with a minimum number of interconnections, only those shared conductors that cause too much EM coupling are eliminated. In this section an upper limit to the impedance in the common lead of two signal paths is determined. In addition to this, upper limits to the allowed EM coupling between signal paths are described, which are the boundary condition required for an EM compatible layout design.

Galvanically-Coupled Paths

The coupling between galvanically coupled paths is mainly determined by the impedance of the shared conductor, which approximately equals the transimpedance (e.g., $Z_{12}$ of the impedance matrix) between the two paths. The signal to interference noise therefore limits the allowed impedance of this shared conductor and the capacitive coupling between paths.

Figure 4.3 shows a circuit equivalent of two paths that share a conductor with an impedance of $Z_{gc} + j\omega Lc$. Due to this impedance and the capacitive coupling represented by $C_{CL}$, the load $Z_{L1}$ of path 1 not only receives the required signal from source $U_{s1}$, but also an interfering signal from source $U_{s2}$ of path 2. The amount of interference from signal source $U_{s2}$ that arrives at load $Z_{L1}$ depends on the coupling and the chosen electrical coding. With the help of the circuit model of two coupled signal paths in Figure 4.3, a limit for the impedance in the common lead and capacitive coupling is given in Table 4.1 as function of the minimal required signal-to-interfering noise $S/N$ for signal path 1. Similar requirements can be determined for signal path 2. As this table shows, the impedance in the common lead has to be much smaller then the source or load impedance of the neighboring path when they both carry a signal in the same electrical domain (current or voltage). The worst-case arises when a voltage domain signals suffers from interference caused by a current domain signal in a neighboring path. Current domain signals, however, have the lowest susceptibility to voltage and current domain signals. Therefore, current domain signals are preferred when sharing conductors.

![Figure 4.3: Circuit model of galvanically-coupled paths.](image)
Table 4.1: Maximal impedance in the common lead.

<table>
<thead>
<tr>
<th></th>
<th>Current</th>
<th>Voltage</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>electrical domain</strong></td>
<td><strong>neighboring signal</strong></td>
<td><strong>desired signal</strong></td>
</tr>
<tr>
<td>$Z_{sc} + j\omega L_C$</td>
<td>$\frac{Z_{S2} + Z_{L2}}{Z_{S2} + Z_{L2}} \left</td>
<td>\frac{Z_{S1}}{Z_{S2}} \right</td>
</tr>
<tr>
<td><strong>Voltage</strong></td>
<td>$</td>
<td>Z_{sc} + j\omega L_C</td>
</tr>
</tbody>
</table>

Non-Galvanically-Coupled Paths

The coupling between non-galvanically-coupled paths is mainly determined by the mutual inductance and difference-mode capacitance (e.g., $C_M$ in Figure 4.4). This section will derive upper limits for these coupling parameters for a given maximally allowed signal to interference ratio. These requirements are derived for the two coupled paths depicted in Figure 4.4. Table 4.2 shows the maximal allowed inductive and capacitive coupling between these two signal paths for a given signal to interference noise ratio $\frac{S}{N}$ for signal path 1, where the interfering signal comes from signal paths 2. It must be noted that this table does not prescribe an upper limit to the inductance and capacitance for every situation, because current domain signals mainly suffer from capacitive coupling, while voltage domain signals mainly suffer from inductive coupling. As this table shows, the best isolation is obtained when the signals of both paths are exclusively in current or voltage domain. In current domain, the voltage between the conductors of each path vanishes, so that the displacement current vanishes, while the induced voltage is not detected. In voltage domain, the signal currents vanish, so that the induced voltage vanishes, while the displacement currents are not detected.

In conclusion: Current domain signals mainly suffer from capacitive coupling and are preferred when inductive coupling dominates. Voltage domain signals mainly suffer from inductive coupling and are preferred when capacitive coupling dominates.
Table 4.2: Maximal capacitive and inductive coupling.

<table>
<thead>
<tr>
<th>electrical domain</th>
<th>Current</th>
<th>Voltage</th>
</tr>
</thead>
<tbody>
<tr>
<td>neighboring signal</td>
<td>$C_M &lt; \left(\frac{S}{B}\right)^{-0.5} \frac{</td>
<td>S_{ij}</td>
</tr>
<tr>
<td>desired signal</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

| Voltage | $M < \left(\frac{S}{B}\right)^{-0.5} \frac{|U_{ij}|}{\omega_{\text{MAX}}|I_{ij}|}$ | $C_M < \left(\frac{S}{B}\right)^{-0.5} \frac{|U_{ij}|}{|U_{ij}|} \frac{1}{\omega_{\text{MAX}}|Z_{S}|}$ |
|---------|-----------------|-----------------|
| | $M < \left(\frac{S}{B}\right)^{-1} \frac{|U_{ij}|}{|U_{ij}|} \frac{Z_{L}}{\omega_{\text{MAX}}}$ | |

4.2.3 Design of Electrically-Long Paths

For electrically-long paths, the current or voltage domains cannot be used separately, because there is a constant energy exchange between the voltage (electric field) and current (magnetic field) in a traveling wave. To prevent distortion due to reflection and dispersion, the load or source impedance (at least on one side) must be matched to the line impedance. The remaining design parameters that can be applied to optimize compatibility are the line characteristic impedance and the impedance of load or source on one side of the line.

In section 3.4.6, it is shown that the ratio of the mutual and line capacitances determines the crosstalk between electrically-long paths. A lower characteristic impedance therefore enables an implementation with lower crosstalk. Standing waves have to be prevented to reduce emission, which requires a matching of both the load or source impedance to the line characteristic impedance.

4.3 Design of Compatible Signal-Processing Functions

To improve the compatibility, circuits have to be optimized for the separation of parasitic and desired signals. In addition to this, they must isolate common-mode (redundant) paths from (difference mode) signal paths (see Section 3.4.2), which are often implemented differentially. This section briefly discusses circuit design considerations to meet these requirements. We distinguish between the design of nonlinear functions like mixers, which change the signal coding (e.g., modulation of an information signal on a carrier) and linear operations like filters and amplifiers that perform signal conditioning and do not change the signal coding. Both types require a different design approach as discussed in the following sections.
4.3.1 Implementation of Nonlinear Signal-Processing Functions

As explained in Section 3.5, nonlinear signal processing functions cause a loss of separability between signals when they are non-reversible. A limiter for example, performs a non-reversible operation, while an ideal logarithmic amplifier performs a reversible operation. Both require a different design approach, which is briefly discussed here.

Implementation of Non-reversible Nonlinear Functions

It is rarely possible to remove a parasitic signal after a non reversible operation. For example, the phase jitter that a parasitic signal causes after limiting, cannot be removed or equalized. Therefore, parasitic signals have to be attenuated as much as possible before they enter non-reversible operations.

Implementation of Reversible Nonlinear Functions

Reversible operations, like the compression and decompression functions applied in hearing instruments to increase the dynamic range, do not deteriorate the separability between parasitic and desired signals (i.e., they are reversible). These functions are similar to linear operations. The implementation of such functions must make sure that this reversibility is maintained even in the presence of parasitic signals. Therefore the saturation of transistors and diodes must be prevented. In Section 3.5, it is noted that all nonlinear components (e.g., transistors, diodes) have a reversible transfer function when saturation is prevented. However, special care is required when addition or multiplication is used, because that may result in a non-reversible transfer function. For example, the differential voltage-to-current transfer function of a differential pair is reversible, but the differential voltage-to-common-mode current transfer function is not reversible.

4.3.2 Implementation of Linear Signal-Processing Functions

Ideal linear circuits do not degrade signal to noise ratio and will not change their coding (i.e., they are reversible), so that compatibility problems caused by nonlinear signal processing do not occur. Practical linear circuits that are designed using nonlinear components (e.g., diodes transistors) may not be linear for parasitic signals, and consequently special measures are required to prevent compatibility problems. To accomplish this, a circuit must be linear and time invariant for intended and parasitic signals. The transfer function therefore must be linear, and the time constants (poles and zeros) have to be independent of the signal.

Minimization of Distortion in Time Domain

Distortion in the time domain arises when the time constants (poles and zeros) of a circuit varies. Signals that store their information using time as a variable, such as phase modulated (PM), and frequency modulated (FM) signals or digital signals can suffer from this type if distortion. Within an electronic circuit, this type of distortion is mainly caused by non linearity in capacitors (e.g., junction and diffusion capacitors) and transconductance of transistors.
This type of distortion can be minimized by class-A biasing, so that the signal amplitude is kept small compared to the biasing, and a differential implementation, so that the even terms in the nonlinearity of the capacitance and transconductance are eliminated [1].

Minimization of Deterioration in Amplitude Domain

Because all active linear circuits are built from nonlinear components, linearization techniques are applied to extend their linear range. The most common used technique is feedback. However feedback is only applicable to a bandwidth when the active components have sufficient gain, and beyond the bandwidth limits of a circuit a nonlinear transfer function remains. This section discusses three linearization techniques that can be applied to minimize compatibility problems due to distortion: linearization with the help of feedback, decomposition of a linear function in a sum of nonlinear operations, and decomposition of a linear function in a cascade of nonlinear operations.

Compensation with the Help of Feedback In [2] it is shown that when the loop-gain of a feedback is large, the nonlinearity in the output stage is the main cause of signal distortion. For parasitic signals above the circuit’s bandwidth however, the nonlinearity in the input stage can become the dominant cause of signal distortion. This situation arises when the nonlinearity in the input stage demodulates a high frequency carrier signal to a parasitic signal that is within the circuit’s bandwidth (i.e., quadratic detection of an AM modulated carrier). In this situation the parasitic signal detected by the input stage is amplified most and dominates (see [3]).

To improve the compatibility for parasitic signals within the circuit’s bandwidth, the output stage needs to be linearized, while the input stage needs to be linearized to improve compatibility for parasitic signals above the circuit’s bandwidth.

A Linear Function as a Sum of Nonlinear Functions To reduce the signal distortion caused by non linear components, a linearized transfer function can be created by summing the weighted non linear transfer functions of the components. For example the balanced implementation of a differential pair attenuates the even part of the I-U transfer function of a transistor, so that a more linear odd transfer function remains. In a similar manner the higher order terms of the I-U transfer function can be attenuated as depicted in Figure 4.5. By scaling of the input signal and transfer function of two differential stages, the third order part of the transfer function is eliminated, so that an almost linear transfer function remains, as depicted in Figure 4.6. The advantage of the this method is that it can linearize the I-U transfer function for differential signals over a wider frequency range then can be obtained with feedback [4].

A linear Function as a Cascade of Nonlinear Functions A linear function can be implemented as a cascade of nonlinear operations. A number of nonlinear functions is concatenated, so that the overall function is linear. This method is used in translinear circuits like current mirrors and the Gilbert cell. These circuits require two matched nonlinear functions where one is the inverse of the other. The inverse
function of a nonlinear component is always created with the help of feedback. These circuits are more sensitive to EM interference than the previous two types of circuits because of the following two reasons: above the bandwidth of the feedback loop, a highly nonlinear system remains; parasitic signals injected between the two nonlinear functions are nonlinearly transferred to the output. Consider for example the current mirror depicted in Figure 4.7(a), which consists of a compression and an expansion function. The compression function is created with the help of feedback. Above the bandwidth of the compression or expansion function, the overall transfer function becomes highly nonlinear. The quadratic detection (demodulation of an amplitude
carrier by the even part of the transfer function) above the circuit’s bandwidth can reduced with the help of a balanced configuration as depicted in Figure 4.7(b).

Nonlinear distortion therefore can be best suppressed by a summation of nonlinear transfer functions that allow compensation over a wider frequency range. For example quadratic detection (demodulation of an amplitude modulated carrier by the even part of the transfer function) is best attenuated by a differential implementation.

4.4 Design Example of a Compatible Low-Power Microphone Amplifier Input Stage

This section demonstrates some of the techniques presented in the previous sections, applied to an ultra low power (a few micro watts) preamplifier for hearing instruments [5]. This amplifier is implemented in a Dimes-03 bipolar process [6], which has a feature size of 1µm and the maximum transition frequency of the npn transistors is 7 GHz. We improved the design for EM immunity with the help of a compensation technique. The immunity of the design has been verified with the help of a GHz TEM-mode (GTEM) cell measurement setup. This a closed pyramid shaped measurement setup, in which a calibrated plane (TEM-mode) EM wave is generated to test a circuit’s immunity. These measurement results are presented in Section 4.4.3.

4.4.1 Electrical System Design

A difficult compatibility problem arises when a hearing instrument comes in very close proximity to a transmitting cellular (GSM) phone. This situation arises when the user of a hearing instrument makes a call with such a phone. Without special measures, the amplifier of a hearing instruments is, due to quadratic detection (demodulation of an amplitude modulated carrier by the even part of the transfer function) of the cellular phone signal, saturation against one of the supply rails and stops functioning. To solve this compatibility problem, we applied a combination of two techniques: suppression of the quadratic detection by implementing an amplifier with an odd transfer function and compensation of the detected signal.

Suppression of the Detection Mechanism

Quadratic detection results from rectification, caused by the even part of the Taylor expansion of the transfer function of the amplifier. It is suppressed by eliminating these even terms. Presuming that the transfer function of the original input stage is given by: $I = f(u)$, then the even part of this transfer is eliminated by implementing the following transfer:

$$I_{\text{odd}}(u) = \frac{1}{2}[f(u) - f(-u)].$$ (4.4)

This implementation requires to identical input stages. Figure 4.8 shows the electrical system design of a trans-conductance amplifier obtained with this method. For differential mode signals, such a transfer function can be easily implemented (e.g., with a differential implementation). However, the interfering signals that are received
Design Example of an Microphone Input Stage

Figure 4.8: Trans conductance amplifier with odd order symmetric transfer function.

by the wires of the microphone are common mode. The detection by rectification of these signals can only be eliminated over a limited bandwidth, so that additional compensation of the detected signals is required.

Compensation for the Received Interference

Compensation is implemented using estimation of the detected interference obtained from a dummy amplifier. This dummy amplifier reproduces the detected interference, which is then subtracted from the desired signal. Figure 4.9 shows the principle of this technique. In this figure, the induced interference is indicated by \( U_{EM} \) and the input signal by \( U_{in} \). The compensating (dummy) amplifier should receive exactly the same interference as the amplifier, therefore it is connected to a dummy signal source (e.g., microphone) that does not produce any signal, but has the same impedance and physical layout.

4.4.2 Circuit Implementation

Standard microphones used in hearing instruments deliver a single-ended voltage signal. However, low voltage circuits are best implemented in the current domain as shown by Serdijn [7]. This allows for a wider dynamic range and makes the design less sensitive to interference as explained in Section 4.2.2. We have therefore chosen a transadmittance input stage.

Because of the low-power and high dynamic range requirement, a Class AB amplifier implementation is used (as depicted in Figure 4.10). This amplifier consists of two nonlinear stages. The upper stage, \((Q_1 \text{ and } R_1)\) correspond to the upper nonlinear amplifier in Figure 4.8, and \(Q_2 \text{ and } R_2\) form the lower nonlinear amplifier. As shown in [8] and [5], for a particular choice of the (quiescent) bias currents and resistor values \((R_1, R_2)\) a Class AB amplifier becomes almost linear. The distortion is minimized
when the circuit is biased so that \( I_{\text{bias}} \cdot R = 0.6 \frac{kT}{q} \), where \( I_{\text{bias}} \) is the bias current of both transistors, \( R = R_1 = R_2 \), and \( \frac{kT}{q} \) is the thermal voltage. As shown in [5], for this particular bias point not only the even order terms of the Taylor expansion of the transfer function cancel, but also the third order term, leaving only the small fifth-order and higher order terms. Figure 4.11 shows the total harmonic distortion (THD) as a function of \( \frac{I_{\text{bias}}}{kT} R = gm \cdot R \). This graph shows that in class A mode the distortion also vanishes. For hearing instruments, however, the first distortion minimum is preferred for its power efficiency. It must be noted that the bias current should be PTAT to cancel the third order term of the transfer function (see [6]).

**Compensation for the Detected Interference**

In principle compensation should be applied to the complete amplifier. However, measurements (as presented in [9] and [3]) have shown that it is mainly the first stage that is responsible for the quadratic detection (see Section 4.3.2). Hence, compensation is applied to the first stage only, thereby saving power and chip area.

### 4.4.3 Measurement Results

The circuit has been tested in two different ways. During the first test, the suppression of high frequency interference due to the odd order transfer function and
compensation have been tested. For this test, a well-defined high frequency signal was fed into the input of the amplifier. During the second test, the effectiveness of the compensation method is tested for signals received by the interconnect. This depends on the symmetry of the interconnect and the amount the interference that enters the circuit via others terminals than the input. Therefore, the amplifier was placed in a well-defined, strong electromagnetic field.

Figure 4.12 shows the measurement results for both the compensated and uncompensated situations. No compensation means that the interference is added only to the input signal of the amplifier, not to the compensating (dummy) amplifier. In the compensated situation, the same interference is also fed to the compensating (dummy) amplifier. The interference was a 15 kHz, 80% AM modulated signal with a carrier frequency swept from 500 MHz to 4 GHz. The amplitude of the applied interference carrier equals the signal amplitude. As shown in Figure 4.12, the signal amplification (normalized to 0 dB) is almost unaffected by the interference. Averaged over the frequency band of the amplifier, the interference signal at the output of the amplifier is about 15 dB below the signal level. On average, compensation attenuates the detected signal by 22 dB. Finally, a plane wave of 15 V/m has been applied to the amplifier. The generated field is a 15 kHz, 80% AM modulated carrier swept from 1 GHz to 4 GHz. The same measurements were also performed below 1 GHz. However, the interference level stayed below the noise level for carrier frequencies below 900 MHz. During these tests, the situation of an amplifier with a microphone connected has been simulated. Because the microphone (including wires) acts like a small monopole antenna at the input of the amplifier, monopole antennas of 15 cm
in length were used for the measurements. In the non-compensated situation, only one antenna was connected to the signal input of the amplifier. Compensation was achieved by connecting a similar monopole antenna to the compensating input of the amplifier. To make sure that both amplifiers receive the same interference, both antennas were wrapped around each other. Figure 4.13 shows the results of these measurements. The result again is improved by the compensation. Due to the second monopole antenna, the compensating amplifier is able to reduce the interfering signal about 12 dB. However this suppression is much (10 dB) lower than in the previous measurements. This is caused by the fact that the complete circuit, including biasing, receives the interference, while only the input is compensated. Table 4.3 summarizes the results.

4.5 Conclusions

To optimize the compatibility of signal transport within a circuit design, a differential implementation is optimal because it isolates the common power supply from the signal paths. Extra common mode signal paths can be introduced to also enable compensation of interference received by signal paths. For electrically-short paths,

\footnote{The measurement amplifier was limited to 500 kHz. Simulations indicate a bandwidth of 3.9 MHz.}

\footnote{This is a simulation value, because the signal is below the -90 dBm level of the analyzer.}
current domain signals offer the highest immunity to interference. However, voltage
domain signals offer the lowest emissions, because they minimize the signal current.
To minimize emission from electrically-long paths, the source and load impedances
should match the line characteristic impedance. To improve EM compatibility, this
line impedance should be low.

Reversible signal processing operations are preferred over non-reversible operations
like switching and limiting operations, because reversible operations ensure separation
between parasitic and desired signals. A linear operation is approximated best by a
differential class A biased implementation. A differential implementation suppresses
detection by rectification over a wide frequency range. Because linearization with the
help of feedback is limited to the circuit’s bandwidth, multiple differential gain stages
(with and overall linear transfer function) should be used to prevent compatibility
problems due to distortion of signals above this bandwidth.

---

Table 4.3: Measurement results.

<table>
<thead>
<tr>
<th>Component</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Supply voltage</td>
<td>1.5 V</td>
</tr>
<tr>
<td>Amplification</td>
<td>13µS</td>
</tr>
<tr>
<td>THD</td>
<td>&lt; −75dB</td>
</tr>
<tr>
<td>Bandwidth</td>
<td>&gt; 500KHz</td>
</tr>
<tr>
<td>Power consumption</td>
<td>3µW</td>
</tr>
<tr>
<td>Quiescent noise level</td>
<td>20µV</td>
</tr>
<tr>
<td>Suppression by compensation</td>
<td>22 dB</td>
</tr>
<tr>
<td>Suppression by compensation in a field</td>
<td>12 dB</td>
</tr>
</tbody>
</table>
Bibliography


Chapter 5

Modeling Physical Layouts and Analysis of EM Compatibility

Chapter 3 presents circuit models that describe the undesired EM interactions within circuits, but it does not explain how the parameters for the models are determined. This chapter (and Chapter 7) outlines the extracting procedure for model parameters from the physical layout of a circuit. The models presented in this chapter describe the relationship between layout geometry (orientation, width, length, etc.) and circuit parameters such as inductance (self and mutual), capacitance etc. They are meant for hand calculation, to assist a designer during design of the layout. The models described in Chapter 7 have been developed for layout verification with the help of computer simulation. They are optimized for accuracy and do not describe the relationship between geometry and circuit parameters.

Commercial electromagnetic (EM) simulation software packages are not very suitable for extracting circuit model parameters, because they usually provide results as n-port parameters (e.g., s-parameters). Therefore, analytical methods are often used as an alternative, like those described in [1, 2, 3, 4] and for microstrip structures in [5, 6]. However, these analytical methods can only be applied to simple geometries and can therefore only take into account limited layout information.

Before parameters of an equivalent circuit model can be extracted, the layout structures that cause undesired EM interaction must first be identified. These are structures such as pairs of wires or wire loops which act as antennas, called ‘parasitic antennas’ in this thesis. To derive a complete model that includes all undesired EM interactions, we need a method that identifies all parasitic antennas within a design. Moreover, the points where these antennas are connected to other circuitry must be defined. This chapter presents a new method of finding these parasitic antennas. It can be used for hand analysis, but it is best suited for computer automation. For each parasitic antenna identified, analytic expressions are derived that describe its EM interaction with the surrounding environment as a function of the most important
layout parameters (e.g. orientation, length, separation, distance to a shielding plane, etc.).

Section 5.1 presents a search method for finding all parasitic antennas in a layout. Two main categories of parasitic antennas are distinguished: loops and dipoles (see Section 5.1). Section 5.2 describes the approximations that are applied to derive a simple analytical expression for the EM coupling between parasitic antennas. Section 5.3 describes the EM interaction between parasitic dipole antennas, Section 5.4 that between loop antennas, and Section 5.5 that between loop and dipole antennas.

5.1 Identification of Parasitic Antenna Mechanisms in Layouts

In circuit theory, a signal path is simply a closed current loop that includes the signal source as well as a load (receiver). Its implementation in a layout is an electromagnetic channel, where the transported EM signal energy is ideally confined between the two conductors of the path. However, in practice this energy is not completely confined and the signal path can become a parasitic antenna. In addition, each signal path can be part of a larger (common-mode) antenna; we will explain how this works below.

For physical design, all potential parasitic antennas need to be identified as well as their interactions. This section therefore presents a search method that determines the parasitic antennas connected to each signal port (e.g., the terminals of an input stage). The interaction between these antennas is analyzed in subsequent sections of this chapter.

Two types of interaction are distinguished: common mode and difference mode interaction. In our definition, there is no such thing as a desired common-mode signals. We consider all intentional electrical signals as difference-mode signals; common-mode signals are common mode with respect to these intentional signals. Common-mode interaction is the reception and radiation of undesired common-mode signals, while difference-mode interaction is undesired radiation and reception of desired difference-mode signals. Both are treated in detail in the next two subsections.

5.1.1 Common-Mode Coupling Mechanisms

The common-mode signals considered in this subsection are not part of the current loop of a signal path. They are always parasitic and radiated or received due to unbalanced signal processing in the circuit. The common-mode parasitic antennas that couple these common-mode signals to the circuit therefore only contribute to the redundant signal paths, as explained in Section 3.4.1. We distinguish two types of common-mode antennas: dipole and loop antennas. Layout designers often do not consider them, and therefore they can be quite large and effective. This section presents procedures to find these parasitic antennas in a circuit layout: by hand in simple circuits, and by automated searching in larger circuits.

To extract all possible common-mode parasitic antennas from a circuit layout, we apply methods from graph theory [7]. We translate the circuit around a component into a directional graph as illustrated in Figure 5.1.
Figure 5.1: Translation of a layout into a directional graph.
The first step identifies each common-mode path and represents it by the two conductors that connect the components. A common-mode path equals a two-conductor signal path that can carry a common-mode signal. For example, $I_{CM4}$ in Figure 5.1(a) is the common-mode current that flows through a common-mode path. In general, if $n$ conductors are connected to a component or sub-circuit, there are $n - 1$ common-mode paths (pairs of conductors that can carry a common-mode signal).

Even when several paths have a shared conductor (like common ground), they are represented as separate common-mode paths, as depicted in Figure 5.1(b). Finally, the resulting schematic is translated into a directional graph, where the common-mode paths are the branches and the components or subcircuits are nodes. To enable the use of graph theory, each common-mode path is assigned an arbitrary direction, as depicted in Figure 5.1(c). This graph is used to determine parasitic common-mode antennas. For example, in Figure 5.1(c), component $A$ may be connected to the parasitic loop antenna created by the branches $\{1, 2, 3, 5\}$. It must be noted that the chosen direction is independent of the signal flow, which is bidirectional.

To find these parasitic antennas, we represent this graph mathematically by an incidence matrix $W$, where each column corresponds to a common-mode path (branch) and each row to a component/sub-circuit (node). Each column contains a 1 at the node where the corresponding path starts and a $-1$ at its end; all other entries are zero. For the circuit in Figure 5.1, the incidence matrix $W$ is:

$$W = \begin{bmatrix} -1 & 1 & 0 & 0 & 0 & 0 \\ 1 & 0 & 1 & 0 & 0 & 0 \\ 0 & -1 & 0 & 0 & 1 & 1 \\ 0 & 0 & -1 & -1 & -1 & 0 \\ 0 & 0 & 0 & 1 & 0 & -1 \end{bmatrix}$$

components, \hspace{1cm} (5.1)

common-mode paths.

In first-order approximations, the complete network rarely needs to be taken into account. Due to the relatively high impedance of many components, the network around a component or sub-circuit that contributes to the parasitic antenna is limited. Figure 5.2 illustrates how the high common-mode impedance of some parts reduces the effective parasitic antenna size. The hashed components in this figure have a high common-mode impedance and limit the parasitic antennas connected to the

Figure 5.2: Limitation of the parasitic antennas due to isolation by the components or sub-circuits.
gray component/sub-circuit. Because the minimal absolute impedance of a half-wave dipole in vacuum is about \( |73 + 42.5j| \approx 84\Omega \) (and in other media even lower), common-mode impedances much higher than 84\( \Omega \) can be considered as isolation in a first-order approximation. That is, the impedance to common-mode current flow provides isolation.

**Common-Mode Dipole Antennas**

Parasitic dipole antennas consist of two or more isolated parts of interconnect, components or subcircuits. The component that is connected to such a dipole connects these two or more isolated parts. In graph theory, this implies that the common-mode paths connected to this component has to be “graph cut”. A graph cut is a set of branches that, when removed, divides a connected graph into two isolated graphs. For example, the sets \{3\} and \{1, 2\} are graph cuts of the circuit in Figure 5.3. It is easily verified that each set of common-mode paths that is connected to one component and constitutes a graph cut must be part of a dipole antenna. The reverse is also true: if a component or sub-circuit is connected to a parasitic dipole, the common-mode paths connected to it must be a graph cut. Thus, if a set of branches connected to one component contains a graph cut, it is a parasitic dipole.

For a simple circuit like the one shown in Figure 5.3, the graph cut and parasitic dipole can be found by close inspection. However, graph theory gives a systematic method which can also be implemented in an automated search algorithm. A vector representation of the graph cuts is required. Let \( \mathbf{e}_i \) be a vector that represents a common-mode path as given in the incidence matrix (5.1) and \( EG = \{ \mathbf{e}_1, \mathbf{e}_2, \cdots, \mathbf{e}_m \} \) the set of common-mode paths. Thus \( \mathbf{W} = (\mathbf{e}_1, \mathbf{e}_2, \cdots, \mathbf{e}_m) \). We define the graph cut vector \( \mathbf{S} = (S(\mathbf{e}_1), S(\mathbf{e}_2), \cdots, S(\mathbf{e}_m))^T \), where

\[
S(\mathbf{e}_i) = \begin{cases} 
1, & \text{if } \mathbf{e}_i \in S \text{ with similar orientation} \\
-1, & \text{if } \mathbf{e}_i \in S \text{ with opposite orientation} \\
0, & \text{if } \mathbf{e}_i \notin S
\end{cases}
\]

In Figure 5.3, the vectors \( (0, 0, 1, 0, 0, 0)^T \) and \( (1, 1, 0, 0, 0, 0)^T \) define two graph cuts. To find a base that spans the vector space of all graph cuts, we define an incidence matrix as follows:

\[
\mathbf{W} = \begin{bmatrix}
\mathbf{W}_T & \cdots & \mathbf{W}_N \\
\cdots & \mathbf{e}_n & \cdots,
\end{bmatrix}
\]

\[(5.3)\]
where we organized $W$ so that the first $n-1$ common-mode paths form a tree, where $n$ is the number of components/sub-circuits (nodes in the graph). A tree is a connected sub-graph that does not contain any closed loops. In Figure 5.3, for example, the set of common-mode paths $\{1, 2, 3, 4, 5\}$ is a tree. The sub-matrix $W_T$ is an $n-1 \times n-1$ matrix that consists of the column vectors of a tree after one arbitrary row is removed. $W_N$ is the remaining $m-n+1 \times n-1$ matrix after removing the same row. For example, the incidence matrix of Figure 5.3 is given by:

$$W = \begin{bmatrix} 1 & 0 & 0 & 0 & 0 & 0 & 1 \\ 0 & 1 & 0 & 0 & 0 & 0 & -1 \\ -1 & -1 & 1 & 0 & 0 & 0 & 0 \\ 0 & 0 & -1 & 1 & 0 & -1 & 0 \\ 0 & 0 & 0 & -1 & 1 & 0 & 0 \\ 0 & 0 & 0 & 0 & -1 & 1 & 0 \end{bmatrix}, \quad (5.4)$$

where the first five columns are a tree. If the last row is removed, $W_T$ and $W_N$ for this circuit are given by:

$$W_T = \begin{bmatrix} 1 & 0 & 0 & 0 & 0 \\ 0 & 1 & 0 & 0 & 0 \\ -1 & -1 & 1 & 0 & 0 \\ 0 & 0 & -1 & 1 & 0 \\ 0 & 0 & 0 & -1 & 1 \end{bmatrix}, \quad W_N = \begin{bmatrix} 0 & 1 \\ 0 & -1 \\ -1 & 0 \\ 0 & 0 \end{bmatrix}. \quad (5.5)$$

With graph theory, it can be proven that a base for the graph cuts is given by:

$$SG = [I_{n-1}(W_T^{-1}W_N)^T], \quad (5.6)$$

where $I_{n-1}$ is a $n-1 \times n-1$ unit matrix. Each column of this matrix $SG$ is a base vector of the graph cut space. For our circuit, this results in the following matrix:

$$SG = \begin{bmatrix} 1 & 0 & 0 & 0 & 0 \\ 0 & 1 & 0 & 0 & 0 \\ 0 & 0 & 1 & 0 & 0 \\ 0 & 0 & 0 & 1 & 0 \\ 0 & 0 & 0 & 1 & 0 \\ 0 & 0 & 0 & -1 & -1 \\ 1 & -1 & 0 & 0 & 0 \end{bmatrix}. \quad (5.7)$$

It is readily verified that each column defines a graph cut. To determine if the grayed component or sub-circuit in Figure 5.3 is connected to a parasitic dipole, we must inspect the common-mode paths connected to this component. Each combination of the columns of $SG$ that results in a cut and is only part of the paths connected to this component defines a dipole. In Figure 5.3, the set of paths is $\{1, 2, 3\}$. Addition of the first two columns in (5.7) gives the graph cut $(1, 1, 0, 0, 0, 0, 0)^T$, the third column defines the graph cut $(0, 0, 1, 0, 0, 0, 0)^T$, and addition of the first three columns results in $(1, 1, 1, 0, 0, 0, 0)^T$. More graph cuts that involve the paths $\{1, 2, 3\}$ cannot be found. The last graph cut isolates the component and is therefore not a valid dipole component. Hence, this component is connected to a parasitic dipole. One
part of the dipole is connected to path \{3\}, and the other part is connected to the paths \{1,2\}. Graph cuts can be found that decompose the graph into more than two components. However, the only graph cuts that contribute to parasitic dipoles are those that decompose the circuit into two isolated parts and do not isolate the component/sub-circuit.

In Equation (5.3), the first \(n-1\) (\(n\) is the number of components/sub-circuits) columns are an arbitrary tree. Before the dipoles can be identified, this tree must be found. A tree is a connected graph that always consists of exactly \(n-1\) branches (paths). To determine if a sub-graph is a tree, we use the following theorem: Let \(W_U\) be a \(n-1 \times n-1\) sub-matrix consisting of \(n-1\) arbitrary selected columns of the incidence matrix \(W\), where we have removed one arbitrary row. Then the determinant \(|W_U| = \pm 1\) if and only if the \(n-1\) selected columns are a tree. Otherwise this determinant is zero. Hence a search algorithm can run through all permutations of \(n-1\) common-mode paths and use this criterion to detect if a tree is found. More efficient methods may exist, but they are beyond the scope of this thesis.

**Common-Mode Loop Antennas**

Common-mode loops arise when the common-mode paths form a closed loop and where none of the components or subcircuits in that loop provides enough isolation to block the induced current. For example, the paths \{1,2,7\} in Figure 5.3 form a parasitic loop antenna. Parasitic common-mode loop antennas often occur in circuits, as any feedback amplifier (see Figure 5.4) has a common-mode loop that can easily become a parasitic antenna. To find these parasitic loops systematically, we again use graph theory. The loops (which are called circuits in graph theory) are represented in a similar manner as cuts. We represent a loop (circuit) by the following vector: 

\[
(C) = (C(e_1), C(e_2), \ldots, C(e_m))^T,
\]

where

\[
C(e_i) = \begin{cases}
1 & \text{if } e_i \in C \text{ with equal orientation} \\
-1 & \text{if } e_i \in C \text{ with opposite orientation} \\
0 & \text{if } e_i \notin C
\end{cases}
\]  

(5.8)

With the same definitions as given in Equation (5.3), the loops in a circuit are given by:

\[
CG = \begin{bmatrix} 
-W_T^{-1}W_N \\
I_{m-n+1}
\end{bmatrix},
\]  

(5.9)
where $I_{m-n+1}$ is a $m-n+1 \times m-n+1$ unit matrix. Each column of $CG$ is a base vector of a loop in the circuit. For the circuit in Figure 5.3, one will find the following common mode loops:

$$CG = \begin{bmatrix}
0 & -1 \\
0 & 1 \\
0 & 0 \\
1 & 0 \\
1 & 0 \\
0 & 1 \\
\end{bmatrix}. \quad (5.10)$$

These are the two loops in Figure 5.3. The common-mode loop antennas connected to component 3 must include branches in the set of paths connected to this component. These are the paths $\{1,2,3\}$. Therefore the parasitic loop antenna from which this component may suffer is given by $(-1,1,0,0,0,0,1)^T$. In this situation, these base vectors find two separate loops in the circuit, and therefore a linear combination of these vectors does not lead to another valid loop. However, when a circuit contains adjacent loops, a linear combination of the base vectors of $CG$ will find the larger loop that surrounds the smaller adjacent loops or the inner loops. However, only the loops that include the components under investigation are of interest.

### 5.1.2 Difference-Mode Coupling Mechanisms

In this thesis, the difference-mode loops are the signal paths in the circuit; they are the two conductor connections that transport the signals between the components. Figure 5.5 shows the difference-mode loops in a sample layout. Each signal path in

![Figure 5.5: Difference-mode current loops in a circuit layout.](image)

Figure 5.1 is a difference-mode loop itself and no search algorithm is required to find it.

To identify the common-mode and the difference-mode antennas, we need to know the signal paths. To automate the search for these paths, information about the signal paths needs to be provided in addition to the netlist. There are two methods to specify this information: 1) the conductor pair that transports the signal can be specified for each signal path, or 2) the terminal pairs that form the signal ports can be specified
for each component/subcircuit. For example, each transistor is specified if it is used as a common- base/gate, emitter/source or collector/drain stage.

5.2 Approximate Classification of EM Coupling Mechanisms in Circuits

In many situations it is practically impossible to derive an exact analytical expression for the EM interactions between two parts of a circuit. Therefore, approximations must be applied that incorporate only the dominant EM coupling mechanisms. This section explains these approximations and the layout geometries to which they apply. The coupling mechanisms of interest are only those that transport signal energy via dynamic EM fields.

Three types of approximations are applied to simplify the analysis: loop and dipole approximations based on the separation between electric and magnetic field interactions, weak and strong coupling regimes based on the signal strength of the transmitters, and quasi-static approximations based on the electrical size of the physical layout. The following sections discuss these approximations in more detail.

5.2.1 Loop and Dipole Approximations

If (a part of) the layout is electrically small, the parasitic antennas that are present can be divided in parasitic electric loops and electric dipole antennas. A loop antenna consists of a closed current path of low impedance, as depicted in Figure 5.6(a). This means that all components within the loop must have a low impedance for the signal frequency at which the loop is analyzed except for the component attached to its terminals. Because of this low impedance, the electric field can be ignored, while the magnetic field, generated by the current flowing in the loop, dominates. Over an electrically short distance the loops mainly interact via the magnetic field, like coupled coils. At an electrically large distance, the EM interaction can be approximated by a magnetic dipole as described in [8] (page 725, formulas 26.3-1 to 26.3-6).

An electric dipole antenna consists of two isolated current paths of low impedance, as depicted in Figure 5.6(b). Each current path must have a low impedance for the signal frequency at which the dipole is analyzed, so that the electric field component along each current path can be ignored. Since the two paths are isolated, only a weak displacement current remains. Hence the magnetic field vanishes, leaving only the electric field interaction. Over an electrically short distance, the dipoles interact mainly via the electric field, like capacitors. At an electrically large distance, the EM interaction can be approximated by an electric dipole as described in [8] (page 725, formulas 26.3-1 to 26.3-6). Figure 5.6(c) illustrates how a signal path can both be part of a parasitic dipole and a loop antenna. The dashed lines indicate the magnetic and electric fields generated in the circuit. The difference-mode signals \( I_{\text{loop}1} \cdots I_{\text{loop}4} \) within the loops are inductively coupled to each other. The two loops connecting each component can be considered two halves of a dipole. The common-mode currents \( I_{\text{dipole1}}; I_{\text{dipole2}} \), indicated by the arrows on the loops, are displacement currents.
Figure 5.6: Weak and strong coupling approximations.
5.2.2 Weak and Strong Coupling Approximations

When the (undesired) coupling between two parasitic antennas is weak, the part of the signal energy that is returned to the transmitting antenna due to reflections can be ignored. In this situation, the antenna impedance is independent of the presence of other antennas. This approximation is often used to represent the influence of external transmitters (e.g., radio stations) and can be applied when the antennas are not directional and the distance between the antennas is much larger than their largest dimension. Under such conditions, the field power radiated by one antenna is diffused over a large area before it reaches the other antenna.

The circuit models that follow from this approximation were presented in Section 3.2.1. These models are shown in Figure 5.7. In Figure 5.7(a), the received signal is represented by a controlled source. This model is valid for weak as well as strong coupling. For the approximation of weak coupling, however, the reflected signal can be ignored (e.g., the effect of current \( \hat{I}_1 \) on the controlled source \( \hat{Z}_{12} \hat{I}_2 \)). Often

\[
\begin{align*}
U_1 & \quad \hat{Z}_{11} \quad \hat{I}_1 \\
\hat{Z}_{21} & \quad \hat{Z}_{22} \\
\hat{I}_2 & \quad U_2
\end{align*}
\]

Figure 5.7: One-sided weak coupling approximation.

only one of the antennas is connected to a strong source like a radio transmitter, while the other antenna is not. In this situation the weak coupling approximation becomes a one-sided approximation as depicted in Figure 5.7(b).

5.2.3 Quasi-Static and Dynamic Modeling

For EMC analysis, we need a circuit model that describes the desired and undesired EM interactions with the help of circuit models, so that circuit analysis and design tools can be applied. Dynamic electromagnetic signals, however, are in principle not described in terms of voltages and currents, because an electric potential (voltage) is only defined for static fields. However, when the electromagnetic fields change slowly with time, they can be approximated as (slowly) changing static fields. This is called a quasi-static approximation, and is required when applying circuit theory to circuits that process dynamic signals. This approximation only applies to electrically small components: components whose physical dimensions are small compared to the wavelength. As an engineer’s approximation, the quasi-static approximation only applies to components that are smaller than one-tenth of a guided wavelength. This section describes the different circuit models that can derived for electrically small and large circuits. The next sections discusses the limitations of the quasi-static approximation and the derivation of these models in more detail.
Because the electrical size determines the type of model to be used, three different classes of models are distinguished: models for three-dimensional, two-dimensional and one (or zero) dimensional electrically small layouts, as depicted in Figure 5.8. A layout that is electrically small in all three dimensions, as that depicted in Figure 5.8(a), can completely be described by a circuit representation like the one shown. In this approximation, the interconnect is represented by nodes in a lumped-element network.

The electric potential across the length of a layout that is electrically small in only two dimensions and long in the other dimension (as depicted in Figure 5.8(c)) is not defined. The electric potential can therefore only be defined in an electrically small plane perpendicular to the length direction, which results in a transmission-line model as that depicted in Figure 5.8(d). The voltage differences between the terminals \{A, B, C\} and between \{D, E, F\} are defined in this figure, but a voltage
difference across the transmission line, for example between the nodes \{A, D\}, is not defined.

Finally, a layout that is electrically small in one dimension or zero dimensions, like the one depicted in Figure 5.8(e), does not allow a global definition of the electric potential. To handle such a configuration, we define electrically small domains around the components, like \{D1, D2, D3\} in Figure 5.8(e). Within these domains, electric potentials are locally defined. The coupling between the components is described by a port model as depicted in Figure 5.8(f). This port describes the linear relation between the local voltages and currents, for example an admittance or impedance matrix. The derivation of this model is treated in Appendix D.

Ruehli [9] uses a different method to derive a circuit description of an electrically large circuit. He utilizes the so-called retarded-potential function (see Kraus [10] for example) in his partial equivalent electrical circuit (PEEC) model. This retarded potential is not a real potential function and does not represent a measurable quantity. However, in electrically small domains locally, it is approximately a real potential function. This model results in a very complex circuit equivalent that is intended for use in a circuit simulator.

**Limitations of The Quasi-Static Approximation**

Circuit theory can only be applied to a component when port conditions for its terminal pairs are met. In principle, these port conditions can only be met by static currents and voltages, because any phase difference between a current signal that enters and leaves the two terminals of one component violates Kirchoff’s current law. In the quasi-static approximation, however, it is assumed that this phase difference is negligible. This section discusses the limitations of this approximation.

Kirchoff’s current and voltage both law fail when a phase difference arises across the terminals of a component. This is illustrated with the help of an electrically long surface-mounted resistor in series with a microstrip line as depicted in Figure 5.9. In this configuration, the resistor can be considered as a lossy transmission line. It

![Figure 5.9: An electrically long resistor in series with a microstrip line.](image)

is obvious that Kirchoff’s current law is violated due to a phase difference between the current signal that enters and leaves the resistor terminals. To show that the electric potential difference $U_{\text{diff}}$ across the resistor is not defined, we integrate the electric field between the two terminals over two different paths: $I_{p1}$ and $I_{p2}$ (see Figure 5.9). Integration over $I_{p1}$ equals subtraction of the transmission-line
voltages at both terminals, while integration over \( I_P \) equals integration of the current-resistance product over the length of the resistor. Both should result in the same voltage difference, but as Figure 5.10(a) shows, the results are completely different when the resistor is electrically long. The potential difference is therefore not defined.

This graph was calculated for a resistor with a resistance of \( 1k\Omega m^{-1} \), an inductance of \( 100nHm^{-1} \), and a capacitance of \( 1nFm^{-1} \). The sine wave excitation has a peak voltage of 0.5 V and a frequency of 1 GHz. However, when the resistor is short enough,
of signals between electrically small ports (pairs of terminals). In addition, it is important to note that one can calculate the voltage difference between the terminals of a component most accurately when the path of integration for the electric field is aligned with the current path between the terminals (path $I_{p_2}$). With this alignment the energy exchange (described by the voltage-current relationship) approximates the electromagnetic energy exchange between the physical components most accurately. This subject is discussed again in Section 7.1.3.

**Circuit Extraction Requirements for Kirchoff’s Laws**

To derive a useful equivalent circuit, we need to extract a circuit that obeys Kirchoff’s current and voltage laws. This section determines the circuit extensions that are required for it to obey these laws. First the requirements for Kirchoff’s voltage law are determined, followed by the requirements for the current law.

The static electric potential $U_{1,2}$ between two points $x_1$ and $x_2$ is given by the line integral of the electric field: $U_{1,2} = -\int_{x_1}^{x_2} E_n(x) \tau(x) dl$, where $\tau(x)$ is a unit vector, tangential to the integration path. Kirchoff’s voltage law states that the sum of the voltages within a closed loop is zero, thus also a closed line integral of the electric field:

\[
\int_{\partial D_C} \hat{E}_r \tau_r dl = 0 \Rightarrow \int_{D_C} \epsilon_{j,n,r} \partial_n \hat{E}_r \nu_j dA = 0 \\
\Rightarrow j\omega \int_{D_C} \mu_{j,p} \hat{H}_p \nu_j dA = 0 \quad (5.13)
\]

Here $D_C$ is the area (domain) enclosed by the loop, $\partial D_C$ the boundary of this area and $\nu$ a unit vector perpendicular to the surface enclosed by the loop. The last step follows from Maxwell’s second equation. This integral determines the total magnetic flux through the area enclosed by the loop. Thus Kirchoff’s voltage law only holds when the time derivative of the enclosed magnetic flux by any loop in the circuit vanishes. When this condition is not met, the induced voltage has to be modeled by (mutual) inductances that describe the contribution of the enclosed magnetic flux. For that reason, an inductance is inserted in every loop in Figure 5.11(b) to represent the magnetically induced signals.

A similar relation follows from Kirchoff’s current law. According to that law, the sum of all currents in a node is zero. With the help of Ampere’s law for static currents, this current law can be formulated as: $\int_{x \in \partial D_n} \epsilon_{k,m,p} \nu_m(x) \hat{H}_p(x) dA = 0$, where $\partial D_n$ is the surface of the closed domain $D_n$ that encloses the node $n$ to which Kirchoff’s current law is applied and $\nu(x)$ a unit vector perpendicular to the surface $\partial D_n$. Thus, the vectorial integral of the tangential magnetic field over a closed domain around a node must vanish. With the help of Maxwell’s first equation, we derive the following condition:

\[
\int_{x \in \partial D_n} \epsilon_{k,m,p} \nu_m(x) \hat{H}_p(x) dA = 0 \Rightarrow \int_{x \in D_n} \epsilon_{k,m,p} \partial_m \hat{H}_p(x) dV = 0 \\
\Rightarrow \int_{x \in D_n} \sigma_{k,r}(x) \hat{E}_r(x) + j\omega \epsilon_{k,r}(x) \hat{E}_r(x) dV = 0 \quad (5.14)
\]
The last term is the sum of the vectorial conduction and displacement currents, which is integrated over the enclosed domain. Hence, the sum of both the displacement and conduction currents must vanish to meet Kirchoff’s current law. A capacitance is therefore inserted between every two nodes of the equivalent circuit depicted in Figure 5.11(b) to represent the displacement currents.

![Figure 5.11](image_url)

(a) 3D electrically small layout.  
(b) Circuit model.

Figure 5.11: Quasi-static model including induced voltages and displacement currents.

### 5.2.4 Overview of Approximation for EM Coupling

Depending on the size of the parasitic antennas and the distance between them, different analytic approximations can be applied to describe the coupling. An overview of these approximations is shown in Table 5.1. The columns are the parasitic sending or receiving antennas, while the rows are the parasitic receiving or sending antenna. Two types of antennas are distinguished: parasitic loop and dipole antennas. Figure 5.12

<table>
<thead>
<tr>
<th>Send or receive antenna</th>
<th>Loop antenna coupling</th>
<th>Dipole antenna coupling</th>
</tr>
</thead>
<tbody>
<tr>
<td>Dipole antenna coupling</td>
<td><strong>Strong coupling</strong></td>
<td>Coupling by controlled sources</td>
</tr>
<tr>
<td>Dynamic</td>
<td>Coupled dipole antennas, approximated by controlled sources</td>
<td>Coupled electric dipoles or transmission lines</td>
</tr>
<tr>
<td><strong>Weak coupling</strong></td>
<td>Coupled loop antenna and dipole antenna, approximated by controlled sources</td>
<td>Coupled loop and dipole antenna, approximated by controlled sources</td>
</tr>
<tr>
<td>Dynamic</td>
<td>Coupled loop antenna and dipole antenna, approximated by controlled sources</td>
<td>Coupled loop and dipole antenna, approximated by controlled sources</td>
</tr>
<tr>
<td><strong>Quasi static</strong></td>
<td>Negligible</td>
<td>Capacitive coupling</td>
</tr>
<tr>
<td>Dynamic</td>
<td>Coupled loop and dipole antenna, approximated by controlled sources</td>
<td>Capacitive coupling</td>
</tr>
<tr>
<td><strong>Quasi static</strong></td>
<td>Negligible</td>
<td>Capacitive coupling</td>
</tr>
<tr>
<td>Dynamic</td>
<td>Coupled loop antenna and dipole antenna, approximated by controlled sources</td>
<td>Capacitive coupling</td>
</tr>
<tr>
<td><strong>Dynamic</strong></td>
<td>Coupled electric dipoles or transmission lines</td>
<td>Coupled electric dipoles or transmission lines</td>
</tr>
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<td>Negligible</td>
<td>Capacitive coupling</td>
</tr>
<tr>
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</tr>
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</tr>
<tr>
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</tr>
<tr>
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</tr>
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</tr>
<tr>
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<td>Coupled loop antenna and dipole antenna, approximated by controlled sources</td>
<td>Capacitive coupling</td>
</tr>
<tr>
<td><strong>Quasi static</strong></td>
<td>Negligible</td>
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</tr>
<tr>
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<td>Negligible</td>
<td>Capacitive coupling</td>
</tr>
<tr>
<td>Dynamic</td>
<td>Coupled loop antenna and dipole antenna, approximated by controlled sources</td>
<td>Capacitive coupling</td>
</tr>
</tbody>
</table>

Table 5.1: Overview of EM coupling approximations.
Classification of EMC Coupling Mechanisms

<table>
<thead>
<tr>
<th>Condition</th>
<th>Circuit model</th>
</tr>
</thead>
<tbody>
<tr>
<td>Electrically small size and distance.</td>
<td></td>
</tr>
<tr>
<td>( d \ll \lambda )</td>
<td></td>
</tr>
<tr>
<td>( s \ll \lambda )</td>
<td></td>
</tr>
<tr>
<td>Electrically small distance.</td>
<td></td>
</tr>
<tr>
<td>( d \ll \lambda )</td>
<td></td>
</tr>
<tr>
<td>( s \ll \lambda )</td>
<td></td>
</tr>
<tr>
<td>Electrically small size.</td>
<td></td>
</tr>
<tr>
<td>( d \gg \lambda )</td>
<td></td>
</tr>
<tr>
<td>( s \ll \lambda )</td>
<td></td>
</tr>
</tbody>
</table>

Figure 5.12: Quasi-static approximations for coupling between loops.

illustrates the approximations that can be applied for the coupling between two parasitic loop antennas. The wavelength is denoted by \( \lambda \), thus \( \ll \lambda \) means electrically small and \( \gg \lambda \) not electrically small. When the distance \( d \) as well as the size \( s \) is electrically small, the coupled loops are described as coupled coils. When the distance is electrically small but the size electrically large, the coupling is described by a distributed capacitive and inductive coupling, like coupled transmission lines. When the distance is electrically large but the size electrically small, the coupling can be approximated by coupled magnetic dipoles.

The coupling between parasitic loop and dipole antennas is described in a similar manner, and is depicted in Figure 5.13. When both the distance \( d \) and the size \( s \) of a parasitic loop and dipole antenna are electrically small, there is almost no coupling. This is because both antennas interact via a different field; the dipole uses the electric field, while the loop uses the magnetic field. When the distance is short and the size is electrically large, the coupling is approximated by a distributed capacitance and mutual inductance, like coupled transmission lines. When the parasitic antennas are electrically small but their distance is electrically large, the coupling is approximated by coupling between an electric and magnetic dipole.

Similar approximation can be applied to describe the coupling between parasitic dipole antennas, as shown in Figure 5.14. When both the distance \( d \) and size \( s \) of a parasitic dipole antennas are electrically small, the coupling can be described as capacitors. When the distance is short and the size is electrically large, the coupling
is approximated by a distributed capacitance and mutual inductance, like coupled transmission lines. When the parasitic antennas are electrically small but their distance is electrically large, the coupling is approximated by coupling between electric dipoles.

When both the distance $d$ between and the antenna size $s$ of the parasitic antennas are large, no quasi-static approximation can be applied. Often numerical methods have to be used to analyze the coupling.

### 5.3 Calculation of Electric Dipole Coupling Parameters

Parasitic dipole antennas consist of two or more isolated current paths of low impedance that act as a receiving or sending antenna. Exact calculations of the coupling are complex and rely in many situations on computer simulations. This section presents simple approximations that do not account for all geometric effects. However, these approximations do have the right order of magnitude and show how the coupling depends on the most important design parameters like distance, length, etc.

As shown in Section 5.1.1, parasitic dipoles mainly arise as common-mode coupling paths. Figure 5.15 shows two parts of a circuit that suffer from common-mode dipole coupling. The components or sub-circuits $C_1 \cdots C_6$ in this figure are represented by

<table>
<thead>
<tr>
<th>Condition</th>
<th>Circuit model</th>
</tr>
</thead>
<tbody>
<tr>
<td>Electrically small size and distance.</td>
<td>almost none</td>
</tr>
<tr>
<td>$d &lt;&lt; \lambda$</td>
<td></td>
</tr>
<tr>
<td>$s &lt;&lt; \lambda$</td>
<td></td>
</tr>
<tr>
<td>Electrically small distance.</td>
<td></td>
</tr>
<tr>
<td>$d &lt;&lt; \lambda$</td>
<td></td>
</tr>
<tr>
<td>$s \gg \lambda$</td>
<td></td>
</tr>
<tr>
<td>Electrically small size.</td>
<td></td>
</tr>
<tr>
<td>$d \gg \lambda$</td>
<td></td>
</tr>
<tr>
<td>$s &lt;&lt; \lambda$</td>
<td></td>
</tr>
</tbody>
</table>
squares, and the conductor pairs of the signal paths between them are represented by line pairs. In this figures, ports 2 and 5 of the component are connected due to parasitic common mode coupling. In the impedance matrix representation on the right, this coupling is represented by the transimpedances $Z_{25} = Z_{52}$.

The appropriate approximation depends on the electrical size and the electrical distance between the antennas as explained in Section 5.2. These approximations are treated in the following sections.

### 5.3.1 Quasi-Static Electric Dipole Coupling Parameters

In a quasi-static approximation, it is assumed that both the antenna size and the distances between them are electrically small, which reduces the coupling to capacitive coupling. The capacitances are derived from a static approximation of the electric field between the conductors.

#### Calculation of the Capacitance

To calculate the capacitance between conductors, a voltage difference $\Delta U$ is applied between the conductors to determine the resulting additional charge $\Delta Q$ on the conductors. The capacitance $C$ is defined as $\Delta Q = C\Delta U$. Figure 5.16 illustrates this procedure. The non-conductive domain $D$ contains three conductors...
Figure 5.15: Circuit translation of common-mode dipole coupling.

Figure 5.16: Three conductors in an open domain.
Electric Dipole Coupling Parameters

C_1 \cdots C_3$. The domain of these conductors are indicated as $D_{C_1} \cdots D_{C_3}$ with boundaries $\partial D_{C_1} \cdots \partial D_{C_3}$. The electric field $\vec{E}$ is described as the negative divergence of the electric potential $\hat{U}$ field: $\vec{E} = -\partial_n \hat{U}$. We assume that the domain $D$ does not contain charge, so that the potential $\hat{U}$ is defined by equation:

$$\partial_n \partial_m \varepsilon_{n,m}(x) \hat{U}(x) = 0 \text{ for } x \in D$$

(5.15)

$$\hat{U}(x) = \hat{U}_i \text{ for } x \in D_{C_i}$$

(5.16)

where $\hat{U}_i$ is the potential of conductor $C_i$ and $\varepsilon_{n,m}(x)$ is the permittivity tensor of $D$. The charge on the conductors follows from Gauss’ law:

$$Q_i = -\int_{x \in D_{C_i}} \partial_n \partial_m \varepsilon_{n,m}(x) \hat{U}(x) dV = -\oint_{x \in \partial D_{C_i}} \partial_m \nu \varepsilon_{n,m}(x) \hat{U}(x) dA$$

(5.17)

where $\nu$ is the unit normal on the conductor surface, directed outwards. The difficulty of this procedure is that it is hard to solve Equation (5.15) directly for practical configurations. However, with the help of conformal mapping techniques we can derive analytical solutions. For example Gevorgian [11, 12] has used this technique to derive accurate expressions for the capacitance of coplanar strip lines.

Calculating Capacitance with the Help of Conformal Mapping

For two or more wire structures that are uniform in one direction, like the coax cable, we can use conformal mapping techniques [13]. It is assumed that the domain $D$ is homogeneous and preferably isotropic, so that potential function $\hat{U}$ is a harmonic function, which enables the use of conformal mapping to solve the differential equation.

Example: Calculating the Capacitance of Two Wires in Parallel

In [2] the capacitance between two wires in parallel is calculated under the assumption of a constant charge distribution over the surface over the wire, while in [13] a conformal map is used to map the two wires onto a parallel plate capacitor. Both are approximations that can only be applied if the diameter of the conductors is much larger than the distance between them. In this example we use an exact method, which predicts a much smaller capacitance than these approximations.

With the help of the mapping function $z = \frac{z_1 - z_2}{z_1 + z_2}$, the two-wire geometry depicted in Figure 5.17 is mapped onto a geometry similar to the coaxial line, where $z_1 = x_1 + jx_2$ is a point in the (complex) plane of the actual geometry and $z = x_1 + jx_2$ a point in the transformed plane. The constant $a$ is given by $a = 0.5d - r_g r_2^{-1}$, where $d$ is the distance between the two wires and $r_g$ the radius of a wire. The resulting radii of the inner and outer conductor of the coaxial line are:

$$r_1 = \frac{d}{2r_g} \left[1 - \sqrt{1 - \left(\frac{d}{2r_g}\right)^2}\right],$$

(5.18)

$$r_2 = \frac{d}{2r_g} \left[1 + \sqrt{1 - \left(\frac{d}{2r_g}\right)^2}\right].$$

(5.19)

The right conductor is transformed into the inner conductor and the left into the outer conductor. The potential function within a coaxial cable is known (see for example
Smythe [14]), therefore the back transformation gives the potential function between the two wires:

\[ \hat{U}(x) = U_1 + \frac{U_2 - U_1}{\ln(r_2) - \ln(r_1)} \ln \left( \frac{(r_1 - a)^2 + r_2^2}{(r_1 + a)^2 + r_2^2} \right) - \ln(r_1). \]  

(5.20)

From this potential function we can determine the charge distribution around the wire, which is displayed in Figure 5.18. This graph depicts the charge distribution

![Figure 5.18: Charge distribution around one conductor of a wire pair.](image)

for the wire on the right in Figure 5.17. As can be seen in this figure, when the wires are close to one another (\( \frac{d}{rg} \leq 3 \)), the charge is concentrated almost completely on the inner side of the conductors, while at a larger distance, opposite charges are present on the inner and outer side of the wire. Integrating this charge around the wire for a unit voltage difference gives us the capacitance:

\[ Q = 2a r_g \frac{U_2 - U_1}{\ln(r_2) - \ln(r_1)} \int_0^{2\pi} \left\{ \frac{a^2 - r_g^2 - 0.25d^2}{r_g^2 + a^2 - ad + 0.25d^2 + (d - 2a)r_g \cos(\theta)} \right\} d\theta \]  

(5.21)

This integral results in a analytical expression, but one that is too large to write here. We therefore only plot this capacitance as a function of the radius/distance ratio in Figure 5.19. This graph shows the capacitance for \( r_g = 1 \) and \( \varepsilon_g = 1 \). To obtain the capacitance for a practical situation, one has to multiply the value given in this graph...
Electric Dipole Coupling Parameters

Figure 5.19: Capacitance per unit length of a wire pair.

with the real values of \( r_g \) and the permittivity \( \varepsilon \).

Conformal mapping is a very powerful method to find an analytical approximation for transmission lines and other geometries. The Schwarz-Christoffel mapping \([15, 16]\) can find a mapping that translates any closed polygon onto a disk or infinite strip (in principle). Recently this method has been implemented in mathematical software like Scilab\(^1\). A limitation, however, is that it only applies to homogeneous or layered media, where layered media like printed circuit boards or integrated circuits are approximated as being infinitely wide.

**Capacitance of Conductors above a Shielding Plane**

In electronics it is common to use a shielding planes such as a common ground plane for signal paths. The capacitance between a wire and such a plane is twice the capacitance between the wire and its “reflection” in the conducting plane. This conducting plane is a plane of symmetry, and the fields on both sides are symmetric. The plane of symmetry can be considered as an electric or a magnetic wall or barrier (see De Hoop \([8]\)). An electrical conductor shielding plane acts as an electric wall,

\[ \frac{C}{\varepsilon} \]

\[ \begin{array}{c}
5 \\
10 \\
15 \\
20 \\
\end{array} \]

\[ \begin{array}{c}
0.05 \\
0.1 \\
0.15 \\
0.2 \\
\end{array} \]

\[ d \\
r_g \]

Figure 5.20: A conductor above a shielding plane.

so that with respect to this plane an “odd” symmetric electromagnetic field can be defined (see De Hoop \([8]\)). “Odd” means that the components of electric field, current and flux density that are in parallel to the plane have opposite signs on both sides of this plane, while the perpendicular components have equal signs. For the magnetic field and flux, the reverse is true: only the perpendicular components have opposite signs. This “odd” field satisfies both the electromagnetic equations and the boundary conditions of the conducting plate. Hence we can consider an odd field as one being generated by the actual sources (currents and charges) and their reflection in the

\(^1\)See http:\/\/www.scilab.org
shielding plane, but then with opposite currents and charges, because the fields have “odd” symmetry with the plane.

Figure 5.20 shows a wire and its reflection in the shielding plane. The electric fields and charges equal those of the equivalent configuration, where its reflection in the plane has the opposite charge. Hence, the charge on the wire is the same as in the situation with two wires, where the image is the second wire. However, for the same charge we need to apply half the voltage, therefore the capacitance is twice that of the parallel wires.

Emission and Reception by Electric Dipoles

During layout, the signal paths are often optimized, however the common-mode parasitic antennas associated within these paths are often neglected. Therefore they can become large and effective radiators. To reduce this effect, the size of the antenna can be reduced (see Section 6.1.3), or a shielding plane can be added. Also the silicon substrate of a chip reduces the radiation of such antennas. This section derives approximations for the radiated and received signals for each of these situations.

Emission by an Electric Dipole  The radiated field of an electrically short dipole antenna is well known from antenna theory [17, 18]. In a circuit layout, however, the parasitic antennas often have a totally different configuration. To determine radiated and received signals of a parasitic dipole, we decompose the layout of the two conductors into a part where the currents run anti-parallel and a part where they run in the same direction. This is illustrated in Figure 5.21. The section where the currents run in the same direction is the parasitic dipole, which in this example has the length $L_1$. The anti-parallel part can be considered as a loop current with surface area $L_2 \times d$ in this figure. The fields radiated by the part in antiparallel can be ignored compared to the part where the currents are aligned, because the fields radiated by the antiparallel part cancel each other. To motivate this, we compare the power radiated by the dipole and antiparallel part of the parasitic antenna. The power radiated by the dipole antenna equals

$$P_{\text{dip}} \approx \frac{1}{6\pi} \frac{\omega^2 \mu \sqrt{\mu \varepsilon}}{L_1^2} |\hat{I}_{\text{avg}}|^2.$$  (5.22)

The contribution of the anti-parallel part to the radiated power equals

$$P_{\text{ap}} \approx \frac{4}{15\pi} \frac{d^2}{L_2} \omega^2 \mu \sqrt{\mu \varepsilon} |\hat{I}_{\text{avg}}|^2.$$  (5.23)
For an electrically small layout, where \( d \ll \lambda \), only the fields radiated by the dipole components need to be taken into account. Hence in a layout where the parasitic dipole can take almost any geometry, we only need to consider the dipole part to estimate the radiated field.

An upper limit for the radiation resistance \( R^A \) of this dipole is given by

\[
R^A < \frac{1}{6\pi} \omega^2 \mu \sqrt{\mu \varepsilon} L_i^2.
\]

(5.24)

This radiation resistance is determined under the assumption that the current through the dipole antenna is constant and equal over the whole dipole conductor. In practice, the average current is smaller, therefore (5.24) can be considered as an upper limit. For practical dipole antennas, a sinusoidal distribution is assumed for a half-wavelength dipole antenna, and a triangular current distribution is assumed for shorter dipoles. In both approximations, the current is highest at the source and vanishes at the end point of the antennas [19, 2].

**Emission from a Dipole on Top of a Shielding Plane**  In a layout the radiation from parasitic dipoles can be reduced by decreasing the length of the dipoles, or application of a shielding plane as close as possible to the signal paths. Such a plane reflects the radiated waves but with an opposite phase, so that the reflected wave partly cancels the emitted one. Figure 5.22 shows three interconnected components which form a parasitic dipole above a ground plane. To determine the radiated field, the shielding plane is approximated by an infinite large conducting plate which is a fair approximation when the plate is much larger than the interconnect. Again it is considered to be a plane of symmetry (see Figure 5.20) so that the field can be approximated by the field radiated by two antennas: the parasitic dipole and its image in the shielding plane but with anti-phase currents. In this approximation, it is assumed that fields in the half space below the board vanish. The current vector potential above the printed circuit board is given by:

\[
\hat{\Phi}_{ext}^f(x) = i_{ap} \int_{x' \in D_{C} \cup D_{C_i}} \hat{J}_n(x') i_{ap} \frac{\exp(-\hat{\gamma}|x - x'|)}{4\pi|x - x'|} \exp(-\hat{\gamma}|x - x'|) \approx L_i i_{ap} i_{n} \frac{\exp(-\hat{\gamma}|x|)}{4\pi|x|} 2j(2\pi \frac{I_{avg}}{\lambda |x|}),
\]

(5.25)

where \( D_{C_i} \) is the domain of “image” of the antenna in the shielding plane and \( t \) the thickness of the board. In this approximation, the electromagnetic field in the cylindrical coordinate system of Figure 5.22 is given by:

\[
\hat{E}_{r} = j \hat{I}_{avg} L_i \frac{\exp(-\hat{\gamma}|x|)}{4\pi} \frac{2t}{\lambda} \left[ \frac{1}{\varepsilon} + j \omega \frac{6}{\varepsilon^2} \right] \cos(\varphi) \sin(\varphi) \cos(\theta)
\]

(5.26)
\[ E_{\varphi}^{gp} \approx \hat{I}^{avg} L_1 \frac{\exp(-\gamma r)}{4\pi} \frac{2t}{\lambda} \left\{ -\frac{1}{j\omega \varepsilon r^3} \sqrt{\frac{2 \mu}{\varepsilon r^2}} \cos(2\varphi) \cos(\theta) \right. \\
+ \frac{j\omega \mu}{r} [1 - \cos(2\varphi)] \cos(\theta) \right\} \] (5.27)

\[ E_{\theta}^{gp} \approx \hat{I}^{avg} L_1 \frac{\exp(-\gamma r)}{4\pi} \frac{2t}{\lambda} \frac{1}{r^2} \sqrt{\frac{2 \mu}{\varepsilon r^2}} \cos(\varphi) \sin(\theta) \] (5.28)

\[ H_{r}^{gp} \approx \hat{I}^{avg} L_1 \frac{\exp(-\gamma r)}{4\pi} \frac{2t}{\lambda} \frac{2}{r^2} \sin(\varphi) \sin(\theta) \] (5.29)

\[ H_{\varphi}^{gp} \approx \hat{I}^{avg} L_1 \frac{\exp(-\gamma r)}{4\pi} \frac{2t}{\lambda} \frac{2}{r^2} \cos(\varphi) \sin(\theta) \] (5.30)

\[ H_{\theta}^{gp} \approx \hat{I}^{avg} L_1 \frac{\exp(-\gamma r)}{4\pi} \frac{2t}{\lambda} \frac{2}{r^2} \left[ \sin^2(\varphi) - \cos^2(\varphi) \right] \\
- \frac{2j\omega \sqrt{\mu \varepsilon}}{r} \sin(\varphi) \cos(\theta) \] (5.31)

These equations, however, are only valid in the space above the printed circuit board, e.i., \(0 < \theta < \pi\). Thus the radiated field is attenuated by at least a factor of \(2\lambda^{-1}\) compared to the non-shielded situation. The far-field components equal the fields calculated and measured by Hill [20] for a strip line, which is about the same configuration.

The total radiated power is given by

\[ P^{\text{ap}} \approx \frac{8}{15\pi} \frac{t^2}{\lambda^2} \omega^2 \mu \sqrt{\mu \varepsilon} L_1^2 |\hat{I}^{avg}|^2 , \] (5.32)

Thus the radiated field can be reduced considerably if a thin printed circuit board with a shielding plane is applied. It must be noted that the permittivity of the printed circuit board (PCB) is ignored (typically fiberglass-epoxy with \(\varepsilon_r \approx 4\)). Because of the lower propagation speed of fields in the PCB, the effective thickness of the PCB increases, but it also traps part of the radiated energy. Hence it can increase the real radiated power by at most a factor of \(\varepsilon_r\), where \(\varepsilon_r\) is the relative permittivity of the PCB material.
Signal Received by a Dipole To determine the signal received by a dipole antenna, we use the approximation derived in Section D, given by Equation (D.8). In this approximation, a unit current source is applied at the terminals of the parasitic dipole antenna. The inner product of the resulting current through the interconnect and the incident field equals the voltage across the terminals. For an electrically short antenna, this voltage approximately equals

\[ \hat{U}_{E;ant} \approx -\frac{\bar{I}}{I_{src}} \int_{x \in D_{ant}} \hat{E}_m \tau_m dl, \]

(5.33)

where \( \tau \) is a unit vector, tangential to the conductor and aligned with the current, and \( I_{src} \) the source current. The ratio of the average and source current is often taken to be between \( \frac{2}{\pi} \) for a half-wavelength dipole antenna and 0.5 for a short dipole antenna [19, 2]. The induced voltage depends on the alignment of the antenna with the field polarization; therefore the maximal induced voltage for a parasitic dipole equals:

\[ |\hat{U}_{E;ant;MAX}| \approx \frac{\bar{I}}{I_{src}} |\hat{E}|L, \]

(5.34)

where \( L \) is the maximal diameter of the dipole. With (5.24), this received signal can be described in terms of the radiation resistance:

\[ |\hat{U}_{E;ant;MAX}| \approx \frac{1}{\omega} \sqrt{\frac{6\pi R_A}{\mu_0 \varepsilon_0 |\hat{E}|}}. \]

(5.35)

The advantage of expressing the received voltage in terms of the radiation resistance is that only one parameter (the radiation resistance) is needed to describe both the radiation and reception limitations of the parasitic antenna.

Signal Received by a Dipole on Top of a Shielding Plane To reduce the received signal, the antenna size can be reduced or a shielding plane can be added. The plane reflects a wave with the tangential components in anti-phase, thereby attenuating the incident fields. To determine the resulting signal, it we assume that the parasitic antenna receives a field that is generated by an external source and its image in the shielding plane. The electric current components tangential to the plane are in anti-phase as depicted in Figure 5.24. To estimate the reduction in field strength, we determine the reduction for a plane wave as depicted in Figure 5.25. Due to the shielding plane, the resulting electric field incident on the antenna equals:

\[ \hat{U}_{E;ant} \approx -\frac{\bar{I}}{I_{src}} \int_{x \in D_{ant}} \hat{E}_m \tau_m \left[ 1 - \cos\left(2\pi \frac{2t}{\lambda \sin(\varphi)}\right) \right] dl, \]

(5.36)

where \( \varphi \) is the angle of the incident field and \( t \) the distance between the shielding plane and the antenna. Thus for a wide range of angles, the incident field is attenuated by a factor of \( \left[ 1 - \cos\left(2\pi \frac{2t}{\lambda \sin(\varphi)}\right) \right] \). However, for very small angles of \( \varphi \), the field can be amplified two times, because the reflected field may arrive in phase. However, the vast majority of signals are attenuated. Note that the permittivity of the PCB layer is again ignored. Due to the lower propagation speed of EM fields in the PCB, the thickness seems to increase by \( \sqrt{\varepsilon_r} \) and therefore the received signal is at most \( \varepsilon_r \) times larger.
5.3.2 Dynamic Electric Dipole Point-Source Coupling Parameters

When the distance between two parasitic dipoles is large but the dipoles are electrically small, a point source approximation can be applied. Because the distance is much larger than the antenna size, the coupling is weak. Figure 5.26 shows two dipoles at a distance $|r|$. With the weak approximation as described in Section 5.2.2, the transimpedance $\hat{Z}_{12}, \hat{Z}_{21}$ can be described by ignoring the reflected field. With the Equation (D.9), this transimpedance for the configuration in Figure 5.26 is given
by:

\[
\hat{Z}_{1,2} = \hat{Z}_{2,1} \approx \frac{\hat{I}_{1;\text{avg}} \hat{I}_{2;\text{avg}}}{\hat{I}_{1;\text{src}} \hat{I}_{2;\text{src}}} L_1 L_2 \exp\left(-j2\pi r\lambda^{-1}\right) \frac{j\omega \mu}{4\pi r} \left\{\sin[\phi_1 + \phi_2 \sin(\theta_1 - \theta_2)] \sin(\phi_1)\right\},
\]

(5.37)

where the fraction \(\frac{\hat{I}_{1;\text{avg}} \hat{I}_{2;\text{avg}}}{\hat{I}_{1;\text{src}} \hat{I}_{2;\text{src}}}\) is the product of ratios of the excitation current and the average antenna current when a current source is applied to the antennas. For most dipole antennas, this ratio is approximately 0.5 · 0.5 = 0.25 [19, 2], and for practical layouts it is even smaller as they are rarely symmetric. When the dipoles are perfectly aligned (\(\phi_1 = 0.5\pi, \phi_2 = 0\)), the coupling is maximal. Note that for electrically short dipoles, the coupling is equivalent to that of a differentiating network with a transport delay.

When shielding planes are applied, the antennas have a much weaker coupling. The greatest coupling occurs when the two dipoles are aligned with each other and the shielding planes reflect the signal towards the other antenna. In this situation, the transimpedance is given by:

\[
\hat{Z}_{1,2}^{\text{MAX}} = \hat{Z}_{2,1}^{\text{MAX}} \approx \frac{\hat{I}_{1;\text{avg}} \hat{I}_{2;\text{avg}}}{\hat{I}_{1;\text{src}} \hat{I}_{2;\text{src}}} L_1 L_2 \frac{2 t_1 t_2 \omega^3 \mu}{\pi^2 V_c^2} \exp\left(-j2\pi r\lambda^{-1}\right) \frac{j\omega \mu}{4\pi r},
\]

(5.38)

where \(t_1\) and \(t_2\) are the thicknesses of the printed circuit board layers and \(V_c\) is the speed of the waves, which equals the speed of light. Here we see that the coupling is highly dependent on frequency. On both sides, the attenuation due to the shielding plane decreases with frequency due the increasing phase difference between the antenna and its image in the shielding plane. This difference is further increased by the permittivity of the PCB material, which seems to increase the thicknesses \(t_1, t_2\) by \(\sqrt{\epsilon_{r1}}, \sqrt{\epsilon_{r2}}\).

5.3.3 Dynamic Electric Transmission-Line Coupling Parameters

When electrically long connections are aligned with one another and their common-mode distance is electrically short, EM coupling cannot be approximated by the capacitive coupling as in Section 5.3.1. In this situation, the parallel signal paths are considered as open transmission lines that act as a series impedance as depicted in Figure 5.27. The mutual admittance \(\hat{Y}_{12}\) is given by [6]:

\[
\hat{Y}_{12} = \hat{Y}_{21} = j\hat{Y}_0 \left[\tan\left(\frac{2\pi}{\lambda} L_1\right) + \tan\left(\frac{2\pi}{\lambda} L_2\right)\right],
\]

(5.39)

where \(\hat{Y}_0\) is the characteristic admittance of the transmission line. The following relation is used to determine the mutual capacitance or inductance per unit length and the propagation speed \(V_c\) of the signal through the transmission line:

\[
\hat{Y}_0 = \sqrt{\frac{C}{L}} = \frac{1}{LV_c} = CV_c,
\]

(5.40)
where $C$ and $L$ are the inductance and capacitance per unit length. For signals propagating through a homogeneous line, the technique explained in Section 5.3.1 and 5.4.1 can be used. For non-homogeneous lines, like slotted lines and microstrip lines, the wave propagates simultaneously through different media. It is not a transverse electromagnetic wave, so that the inductance and capacitance become frequency dependent as explained in Gupta [5].

### 5.3.4 Dynamic Electric Dipole Coupling Parameters

When both the antenna and the distance between the antennas are electrically large, the quasi-static approximation cannot be applied, except in some special cases like the half-wave dipole and the mono-pole antenna [19, 2]. Therefore, simulation techniques like those discussed in Chapter 7 have to be applied. However, a proper layout, may not contain such antennas, because they can be very effective.

### 5.4 Calculation of Loop Coupling Parameters

Loops are closed current paths of low impedance. A circuit can contain two types of loops: difference-mode signal paths and common-mode loops, as explained in Section 5.1.1. Coupling between difference-mode signal path loops requires extra attention because it causes direct coupling between transported signals, which cannot be rejected as easily as common-mode signals. The following subsections describe closed-form approximations for some common coupled loops based on the quasi-static approximation discussed in Section 5.2.

#### 5.4.1 Quasi-Static Loop Coupling Parameters

When both the electrical distance and the size of the loops are small, the coupling mechanisms can be approximated as inductive coupling. Because the signal sources are connected to loops of low impedance, the electric fields remains small and the displace currents can be ignored, but coupling by the magnetic field remains. With
this approximation, the Maxwell equations reduce to:

\begin{align}
-\epsilon_{k,n,p} \partial_n \hat{H}_p + \sigma_{k,r} \hat{E}_r &\approx -j \varepsilon_{ext}, \\
\epsilon_{j,n,r} \partial_n \hat{E}_r + j \omega \mu_{j,p} \hat{H}_p &= 0.
\end{align}

The coupling is determined by the voltage induced within a loop due to a magnetic field generated by the currents flowing in some other loop. In a circuit model, this coupling is represented by mutual inductances. If \( \hat{I}_i \) is the current in loop \( i \) and \( \hat{U}_i \) the voltage induced in this loop, then the coupling is described as: \( \hat{U}_i = j \omega \sum_{j=1}^{n} L_{ij} \hat{I}_j \), where \( L_{ij} \) is the mutual inductance between loops \( i \) and \( j \). The mutual inductance between two loops can be determined with the help of the Neumann formula \[4\]. Consider for example the two loops depicted in Figure 5.28. The mutual inductance between these loops, according to Neumann, is given by:

\[ L_{i,j} = \mu \oint_{x \in \partial C_1} \oint_{x' \in \partial C_2} \frac{\tau_n(x) \tau_n(x')}{4\pi |x - x'|} dl dl', \]  

where a homogeneous isotropic magnetic permeability \( (\mu_{j,p}(x) = \delta_{j,p} \mu) \) is assumed. The advantage of this expression over the other methods is that only the conductor surface needs to be considered, instead of the whole area enclosed by the loop. This expression has been derived under the assumption that the wires are thin compared to the distances between them, but it can easily be extended to other situations. It must be noted that the complete current paths (\( C_1 \) and \( C_2 \) in Figure 5.28) contribute to the mutual inductance, which includes resistors and even the gap between the plates of capacitor. In Appendix E, an analytical method is described to determine the coupling between interconnections within a layout.

The following subsections treat two important problems in the design of an EM compatible layout: inductive coupling between overlapping and non-overlapping signal paths and the radiation and reception of loops.

**Mutual Inductance of Enclosed and Non-Enclosed Loops**

In circuit layouts, it can happen that the layout of one signal path overlaps with other paths. They therefore share magnetic flux, which results in strong magnetic coupling. The inductive coupling between overlapping paths is about ten times stronger than that between non-overlapping paths. To demonstrate this, the coupling between two circular loops, which are depicted in Figure 5.29 is determined. Within the loop, the magnetic field is much stronger than outside it. The magnetic field component,
perpendicular to the plane of the page in this figure is given by:

$$
\hat{H}(r_1, d) = I \frac{(d - r_1) E\left(\frac{-4dr_1}{(d-r_1)^2}\right) - (d + r_1) K\left(\frac{-4dr_1}{(d-r_1)^2}\right)}{2\pi(d - r_1)(d + r_1)},
$$

(5.44)

where $r_1$ is the radius and $d$ the distance from the center. The function $E(m)$ is the full elliptic integral of the first kind [21] and $K(m)$ that of the second kind [22]. This field is plotted in Figure 5.30 for a radius of 2 and a current $I = 1$. At the same distance from the edge, the field inside the loop is 5 to 10 times larger than outside the loop. This will be the same for the coupling. An analytic expression for the coupling between the two loops can only be found for $d = 0$. For $d > 0$, numerical methods are required. The result for $r_1 = 2, r_2 = 1$ is shown in Figure 5.31. A comparison of Figure 5.31(a) and 5.31(b) reveals that the coupling of the enclosing loops is about 10 times larger. Hence enclose paths should be avoided.

**Emission and Reception by Parasitic Loops**

In principle, any difference-mode signal path is a closed conductor loop that can act as a parasitic loop antenna. Although their reception is small in a good design, the signals received are in difference mode and thus they cannot easily be rejected. Hence the radiation and reception by these paths requires extra care in the design. This section determines the radiation and reception of these parasitic antennas and the reduction that can be obtained with the help of a shielding plane.

**Emission by a Parasitic Loop** To determine the fields radiated by an electrically small current loop, we again apply the source-type integral equations [8] (page 725,
Loop Coupling Parameters

1.2
1.6
2.0
0
0.4
0.8
0.2 0.6 1

(a) Mutual inductance of enclosing loops.

(b) Mutual inductance of non-enclosing loops.

Figure 5.31: Mutual inductance between two loops.

formulas 26.3-1 to 26.3-6). For an electrically small current loop with an orientation as depicted in Figure 5.32, the current vector potential can be approximated by:

\[
\hat{\Phi}_k \approx \hat{I}_{k,p,m} \frac{x_m}{|x|} A_p \frac{x_m}{|x|} \left( \hat{\gamma} + \frac{1}{|x|^2} \right) \exp\left(-\hat{\gamma}|x|\right) \frac{4\pi}{|x|},
\]  

where \( A \) is the vectorial area of the loop. The power emitted by such a parasitic loop antenna is approximately given by:

\[
P \approx |I|^2 \omega^4 \mu (\varepsilon \mu)^{1.5} \frac{A^2}{6\pi},
\]  

where \( A \) is the area defined by the loop. Note that this power is highly frequency dependent. The corresponding radiation resistance \( R^A \) is given by:

\[
R^A \approx \omega^4 \mu (\varepsilon \mu)^{1.5} \frac{A^2}{6\pi}
\]  

Emission from a Parasitic Loop on Top of a Shielding Plane To limit the radiated field by a loop, one can minimize its enclosed area \( A \) and apply a shielding as depicted in Figure 5.33. The image of the loop in the ground partly compensates...
the radiated fields. The reduced EM emission is given by:

\[
\hat{E}_\theta^{\text{loop}} = \omega \mu \frac{2t}{\lambda} \hat{I} A_3 \frac{\exp(-\hat{\gamma} r \sin(\varphi))}{4\pi r^2}
\]

\[
\hat{E}_r^{\text{loop}} = -j \frac{2t}{\lambda} \hat{I} A_3 \frac{\exp(-\hat{\gamma} r \cos(\varphi))}{4\pi r^3}
\]

\[
\hat{E}_\varphi^{\text{loop}} = -j \frac{2t}{\lambda} \hat{I} A_3 \frac{\exp(-\hat{\gamma} r \sin(\varphi)^2)}{4\pi \cos(\varphi) \left( \frac{1}{r^3} + \frac{\hat{\gamma}}{r^2} \right)},
\]

where \( t \) is the thickness of the substrate between the shielding plane and the loop. As these equations show, a strong reduction can be obtained when the distance \( t \) is considerably smaller than the wavelength. These expressions only hold on the loop side of the shielding plane, while it is assumed that the fields on the other side vanish. Moreover, the influence of the substrate permittivity is ignored. The permittivity increases the effective thickness \( t \) about \( \sqrt{\varepsilon_r} \) times but also traps part of the radiated field. Therefore the radiated field may be at most \( \varepsilon_r \) times larger.

**Signal Received by a Parasitic Loop** The received signal due the external field follows directly from Faraday’s law. It is linearly dependent on the surface area \( A \) of the loop. The maximal induced voltage equals

\[
\hat{U}_{\text{Max}} \approx j \omega \mu A |H| = \frac{j \omega A |E|}{V_c},
\]

where \( |H| \) and \( |E| \) are the absolute electric and magnetic field intensities and \( V_c \) is the traveling speed of the EM wave. Again with (5.47), this received signal can be expressed in terms of the radiation resistance:

\[
|\hat{U}_{\text{Max}}| \approx \frac{1}{\omega} \sqrt{\frac{6\pi R A}{\mu(\varepsilon \mu)^{1.5}}} |\hat{H}| = \frac{1}{\omega} \sqrt{\frac{6\pi R A}{\mu \sqrt{\varepsilon \mu}}} |\hat{E}|,
\]

which is equal to (5.24). Hence, it does not matter whether the parasitic antenna is a dipole or loop if the sensitivity of a signal path is specified using the radiation resistance.
Signal Received by a Parasitic Loop on Top of a Shielding Plane  The loop area $A$ can be decreased and a shielding plane can be applied in order to reduce the received signal strength. This section determines the influence of a shielding plane.

Faraday’s law shows that a loop is sensitive to the magnetic field perpendicular to the enclosed surface. This field can be reduced by a shielding plane under the loop as depicted in Figure 5.34. Because the field above a conductive plane is odd, the reflected fields seem to be generated by the image of the source in the plane, where currents tangential to the plane are reversed. The resulting induced voltage is given by:

$$
\hat{U}_{Max} \approx j\omega\mu A|H| = \frac{j\omega A|E|}{V_c} \left[1 - \cos\left(2\pi \frac{2u}{\lambda \sin(\varphi)}\right)\right] \cos(\varphi),
$$

where $t$ again is the distance between the loop and the shielding plane. Strong suppression is obtained when $t$ is much smaller than the wavelength.

5.4.2 Dynamic Loop Coupling Parameters between Electrically Small Loops

When the distance between two parasitic loop antennas is large but the loops are electrically small, their coupling can be approximated by coupled magnetic point sources. Because the distance is much larger than the antenna size, this is a weak coupling. Figure 5.35 shows two loops at a distance $|\mathbf{r}|$. With the weak approximation as described in Section 5.2.2, the transimpedance $\hat{Z}_{12}, \hat{Z}_{21}$ can be described by ignoring the field reflected by these loops and only taking the far field component into account.
With the help of Equation (D.9) we obtain the transimpedance for the configuration in Figure 5.26:

\[
\hat{Z}_{1,2} = \hat{Z}_{2,1} \approx A_1 A_2 j \omega \mu \gamma^2 \frac{\exp(-j2\pi r \lambda^{-1})}{4\pi r} \sin[\varphi_1 + \varphi_2 \sin(\theta_1 - \theta_2)] \sin(\varphi_1),
\]

(5.54)

where \( \gamma = j2\pi \lambda^{-1} \) is the propagation factor and \( A_1, A_2 \) is the area enclosed by the two loops. The coupling is greatest when the loops are perfectly aligned (\( \varphi_1 = 0.5\pi, \varphi_2 = 0 \)). To reduce this coupling, the loop areas can be decreased or a shielding plane applied. In case of a shielding plane, the coupling is maximal when the two loops are aligned with each other and the shielding planes reflect the signal towards the other antenna. In this situation, the transimpedance is given by:

\[
\hat{Z}^\text{MAX}_{1,2} = \hat{Z}^\text{MAX}_{2,1} \approx \omega \mu \frac{4t_1 t_2}{\lambda^2} A_1 A_2 \frac{\exp(-\gamma r) \sin(\varphi)^2 \gamma}{4\pi} \frac{1}{\cos(\varphi) r^2}
\]

(5.55)

where \( t_1 \) and \( t_2 \) are the thicknesses of the dielectric of the two PCB layers. Again it is noted that the smaller the thickness of the dielectric, the smaller the coupling. The permittivity of the PCB is ignored; this will increase the coupling by \( \varepsilon_r \) at most.

### 5.4.3 Dynamic Loop Coupling between Electrical Long Loops

Electrically long loops are signal paths that are almost always described as transmission lines. Expressions describing the coupling between these lines can be found in textbooks on microwave theory [16, 6, 23]. The results are very similar to those we found for the quasi-static situation. In [16] it is shown for microstrip lines that this coupling is determined by the ratio of the distances between the strips and the strip-to-ground-plane distance. The closer the strip lines are to the ground plane, the smaller the coupling, just as we found in previous paragraphs for the shielding plane. For more information about coupling between transmission lines, please refer to the books mentioned above.

Very little research has been done in the area of radiation and reception, however. In [20], the fields generated and received by a microstrip line, which is equal to the radiation and reception of a dipole above a ground plane are described (as discussed in Section 5.3.1). Further research is required, however.

### 5.5 Calculation of Loop-Electric Dipole Coupling

Most parasitic dipoles are almost only common-mode antennas, while many loop antennas are difference-mode signal paths. Coupling between these two types of antennas results in common-mode to difference-mode conversion. This type of coupling requires extra care, especially for systems with large common-mode signals. This section determines the coupling between these antennas.

#### 5.5.1 Quasi-Static Loop-Dipole Coupling Parameters

The coupling between parasitic loop and dipole antennas in the quasi-static approximation is very weak, because both radiate and receive a different type of field. At
an electrically small distance, the electric dipole is mainly sensitive to radiation and
reception of electric fields, while the loop is sensitive to those of magnetic fields. In
an electrically small situation this coupling can often be ignored.

5.5.2 Dynamic Loop - Dipole Coupling Parameters

The coupling between loop and dipole antennas arises at an electrically larger dis-
tance, because an exchange between electric and magnetic field energy only takes
place during propagation. This section treats the coupling between electrically small
antennas. For larger antennas, numerical methods (as treated in Chapter 7) have to
be applied.

Figure 5.36 shows a coupled loop and dipole antenna. Weak coupling is assumed,
because the distance is large compared to the antenna size. In this approximation,

\[ Z_{12} = Z_{21} \approx j \omega \mu \gamma A \frac{\exp(-\gamma r)}{4\pi r} \sin(\varphi_1) \sin(\varphi_2) \sin(\theta_2), \]

where only the far-field components are taken into account. The coupling is highest
when the dipole antenna is aligned with the loop (\( \varphi_2 = \pm \frac{\pi}{2}, \theta_2 = \pm \frac{\pi}{2} \)) and at the
same height as the loop \( \varphi_1 = \frac{\pi}{2} \).

5.6 Summary

In this chapter a new method has been presented for identifying EM-coupling mech-
anisms in a layout. We distinguished two types of coupling mechanisms: difference-
mode coupling (e.g., coupling with intentional signals) and common-mode coupling
(e.g., coupling with signals that are common mode with respect to intentional sig-
nals), which correspond to two groups of parasitic antennas: difference-mode parasitic
antennas (e.g., the intended signal paths) and parasitic common-mode antennas. Es-
pecially these parasitic common-mode antennas require extra care, because they are
easily overlooked and can be large and effective.

To identify parasitic common-mode antennas, we have presented a new search
method based on graph theory. Therefore the circuit’s netlist must be replaced by
a signal-path list that describes the connectivity and the signal flow in a layout.
With the help of graph theory, two types of common-mode parasitic antennas are
found: loops, which correspond to graph circuits, and dipoles, which correspond to graph cuts. The advantages of this search method are that no parasitic antenna is overlooked and the search can be done with a computer.

A circuit representation that shows the EM interaction between these parasitic antennas must accurately describe the EM energy exchange between circuit components. This implies that the current flow between circuit nodes, and the voltage difference across circuit nodes is only defined if the distance between these nodes is electrically short in the layout (e.g., if the time a signal requires to cross the distance is short compared to the signal’s fastest transient). Therefore only an electrically small layout can be represented by a lumped-element network. Larger layouts require a transmission line or port representation that describes the interaction between electrically small sub-domains which contain the circuit components.

In a layout, two types of parasitic antennas are found: loops and dipoles. The approximations that can be applied to describe their interactions depend on their electrical size and distance. Electrically small loops and electrically short dipoles can be approximated by magnetic and electric dipoles respectively, which simplifies the analysis considerably. In this chapter it has been shown that the most effective methods to reduce the EM interactions are: application of a shielding plane as close as possible to the parasitic antennas, reduction of the size of the parasitic antennas by folding and minimizing their length and area, re-routing of the signal paths such that none circumvents the other, preventing the use of shared current paths, orthogonalizing the signal paths such that they do not run in parallel, and maximizing the distance between the paths.

The radiation and reception of both loops and dipoles can be described by their radiation resistance. This parameter can be used to specify the quality requirements that a layout must meet, for example in an application note.
Bibliography


Chapter 6

EM Compatible Layout Design

In Chapter 5 it was shown that together the floorplan, routing and the implementation of the interconnect determine the possible undesired EM-interaction of a system. To optimize a layout for compatibility, one needs to take into account the coupling between signal paths and its effect on the transported signal needs. This chapter presents a design approach to optimize the compatibility by minimizing the coupling between signal paths. It is meant as a design guide. The design procedure is organized such that the most effective optimizations like eliminating the use of shared conductors are done first, and the least effective last. During each step from floorplan to final layout, the compatibility is improved with the help of the models developed in Chapter 5. An optimization algorithm based on this approach that is suited for automation is outside the scope of this thesis.

EM compatibility for (mainly PCB) layouts, such as design guides and rules of thumb can be found in [1, 2]. A good guideline for PCB layout design is given by Montrose [3], but it does not explain how to optimize a layout. A first step towards optimization are the algorithms discussed in [4, 5, 6]. These are rule based, where a cost function is introduced for each net (i.e., for each group of galvanically coupled terminals). This cost function is a measure of the unintended EM coupling and used to limit this coupling during automatic routing. However, although these algorithms calculate the coupling to a net they do not consider complete signal paths. Therefore, they may still generate solutions with a large area for the loop of signal paths. Moreover, they do not take into account the sensitivity of the signals to radiation and reception.

In this chapter, the implementation of a layout is divided into two main steps. The first step is the design of the topology, which consists of placement of the components and routing of the signal paths. Coupling is minimized with methods like separating sensitive and high-power signal paths, prevention of shared conductors, prevention of overlap amongst paths, etc. The second step is the implementation of these signal paths, which is their construction. The ideal construction is a radiation- and reception-free transmission line. During this step, the available technology is used to create approximations of this ideal signal path, which are then compared.
Section 6.1 treats the layout topology. This includes the placement of components and routing of the signal paths. The construction of the signal paths is treated in Section 6.2.

6.1 Design of the Layout Topology

To optimize a layout, one needs to minimize the unintended coupling between signal paths. This means orthogonal orientation, increasing the distance between signal paths and minimizing the emission and reception. The coupling between signal paths cannot be minimized in the same manner for all paths. For example, it is not possible to maximize the distance between all paths, and so the optimum is necessarily a compromise.

This section treats the placement of components and routing of the interconnect such that the influence of unintended coupling is minimized. The components are placed such that a good compromise is found between the area occupied by the layout and reduction of coupling between signal paths. In this section it is assumed that all signal paths are implemented by separate conductor pairs, even when the signal ports share a terminal, as depicted in Figure 6.1. This implementation guarantees that the loop area is minimized and therefore has the least undesired EM coupling. In the next section, a shared conductor may be used when these signal paths are constructed.

6.1.1 Gathering Information Required for EM Compatible Layout Design

Normally, a layout is designed from a netlist of all the components and their interconnections. Auto-routing algorithms for improving the EM-compatibility of a layout, as described in [7, 8, 6, 9, 5], use this netlist to route the layout. To improve the EM compatibility, these algorithms try to reduced the unintended coupling between nets (which are groups of galvanically coupled terminals). When the signal paths are implemented with strip or microstrip lines such that the nets correspond to the signal paths, these algorithms can improve the compatibility. In many other implementations (like integrated circuits), however, reduction of coupling between nets does not automatically imply reduction of coupling between signal paths. Moreover, these algorithms lack information about the sensitivity of signal paths to radiation and reception. Hence, they require more information to optimize the compatibility of a design. This section defines the information required for optimization of a layout. The methods presented in this chapter are based on the implementation of signal paths
instead of the commonly used implementation of nets. The following subsections determine the information needed to identify these signal paths and their requirements on impedance, maximal-allowed coupling, radiation resistance, signal transport time, etc.

**Identification of Signal Paths in the Netlist**

A netlist describes the signal paths that are present in a circuit, but additional information is required to describe the sensitivity for emission, reception and coupling with other signal paths. To illustrate this, consider the balanced voltage amplifier, which is depicted in Figure 6.2(a). To make the signal paths visible, we have redrawn the schematic of Figure 6.2(a) as depicted in Figure 6.2(b). The dashed ellipses in this figure enclose signal paths 1 to 6. For automatic routing of these signal paths, they need to be described as signal ports and paths. From Figure 6.2(b) for example, we can see that the terminal set \{t1p1, t2p1\} belongs to port p1, which is connected to the conductor set \{c1s1, c2s1\} that belongs to signal path s1. Thus a netlist becomes a port list of connected signal ports. Note that in this respect the supply lines are a (special) signal path too. Furthermore, signal paths can share a conductor. For example, ground in non-balanced circuits is shared by many signals.

As described in Section 3.4.1, we distinguish difference and common mode signals and signal paths. The desired signal paths and power supply are difference mode paths; all remaining paths are common mode with respect to these desired paths and therefore called common mode paths. The common mode paths can be found with the methods described in Section 5.1. Figure 6.3 shows the two types of common mode paths present in the difference amplifier. The dashed lines in Figure 6.3(a) represent the common mode input and output path which together can become a common mode dipole antenna. The dashed loop in Figure 6.3(b) indicates the common mode loop that is present in the design. In a proper design, the difference mode paths suffer more from EM coupling to other paths than from EM emission and reception,
Figure 6.3: Common mode paths of a difference amplifier.

because the loop area enclosed by the conductors of such a path is kept as small as possible. As described in Section 3.2.1, EM emission and reception is the weak coupling approximation of EM interaction with an external system. EM coupling is the EM interaction within a circuit. The routing of difference mode paths therefore focuses on minimization of coupling. However, common mode paths suffer much more from radiation and reception, because they can be electrically large. An open common mode path in a layout like that depicted in Figure 6.3(a) can have a size of the order of a wavelength, certainly when cables are involved. The same holds for common mode loops, like those depicted in Figure 6.3(b). During layout, these loops should not become efficient antennas.

Signal Path Requirements

The signal path requirements that need to be known for layout are: line impedance, power handling capability, signal transport time, allowed radiation, allowed reception and coupling to other paths. Especially the signal path impedance is important, because when the signal path is electrically long, it must match the input and/or output impedance to prevent power loss and distortion (see [10]). The power handling capability becomes significant when high currents and/or voltages are involved. The signal transport time is important for time-critical systems like high-speed digital circuits (see [3]). For example, clock and data signal paths to a storage element must have the same delay time to ensure proper synchronization. In this thesis, we focus on the parameters that are important for EM compatibility: the allowed radiation, reception and coupling to other paths.

Each path, whether difference or common mode, has a different sensitivity for these mechanisms. This depends on the signal power and the coding (modulation) of the signal. Let for example $U_i^E$ be the voltage induced in path $i$ of the amplifier
shown in Figure 6.2(b). The output of this amplifier is approximately given by:

\[
U_O \approx AU_i + A(U_1^E + U_2^E) + \frac{A}{gm_{Q_1,Q_2}rd_{Q_1,Q_2}} U_3^E \\
+ \left(1 - \frac{A}{gm_{Q_1,Q_2}rd_{Q_1,Q_2}gm_{Q_3,Q_4}rd_{Q_3,Q_4}}\right) U_4^E \\
+ \frac{A}{gm_{Q_1,Q_2}rd_{Q_1,Q_2}gm_{Q_3,Q_4}rd_{Q_3,Q_4}} U_5^E + U_6^E, 
\]  

(6.1)

where \( A \) is the amplification factor of the amplifier, determined by the resistive feedback network, \( gm_{Q_i,Q_j} \) the small-signal transconductance of the transistors \( i \) and \( j \), and \( rd_{Q_i,Q_j} \) is the small-signal transistor output resistance. As can be seen from this expression, signal paths 1 and 2 are most sensitive to reception (because they see the most gain), while the signal paths 4 and 6 are likely to radiate energy, because they carry the largest amplitude signals.

In addition, signal coding and (unintended) signal conversion must be taken into account. For example, in principle a narrowband high-frequency signal and a low frequency baseband signal should not interfere with one another. However, unintended non-linear frequency conversion, which is explained in Section 3.3 can result in unintended interference.

To account for these effects, we need a list that describes the coupling that is allowed between signal paths and their allowable sensitivity to radiation and reception. From simulation with the models given in Chapter 3, we will derive seven coupling parameters, six mutual impedance or admittance parameters, and the radiation resistance. The coupling between signal paths is described by the difference mode to difference mode, common mode to difference mode, and common mode to common mode parameters. The definitions for these coupling modes are illustrated in Figure 6.4. The quasi-static coupling mechanisms of the two signal paths \( S_1 \) and \( S_2 \) in

Figure 6.4: Common mode and difference mode coupling between signal paths.

Figure 6.4(a) are illustrated in Figure 6.4(b). With the definitions for common and difference modes indicated in this figure, the difference mode coupling parameters are
described by the difference mode transimpedance $\hat{Z}_{21}^{dm}$ and admittance $\hat{Y}_{12}^{dm}$:

$$\hat{Z}_{21}^{dm} = \frac{\hat{Y}_{22}^{dm}}{\hat{I}_{12}^{dm}} |U_{22}^{dm} = 0, U_{12}^{dm} = 0$$ (6.2)

$$\hat{Y}_{21}^{dm} = \frac{\hat{I}_{12}^{dm}}{\hat{U}_{12}^{dm}} |U_{22}^{dm} = 0, U_{12}^{dm} = 0$$ (6.3)

where $\hat{U}_{22}^{dm}$ and $\hat{I}_{12}^{dm}$ are the difference voltages and currents induced in signal path 2, respectively, by inductive and capacitive coupling. Note that the difference voltage and current are induced at different places in the circuit. Therefore $\hat{Z}_{21}^{dm} \neq 1/\hat{Y}_{21}^{dm}$. However, reciprocity still holds, so $\hat{Z}_{21} = \hat{Z}_{12}$ and $\hat{Y}_{21}^{dm} = \hat{Y}_{12}^{dm}$.

In a similar manner, the conversion of common mode to difference mode signals is specified by:

$$\hat{Z}_{21}^{cmdm} = \frac{\hat{U}_{22}^{cmdm}}{\hat{I}_{12}^{cmdm}} |\hat{I}_{22}^{dm} = 0, \hat{I}_{12}^{dm} = 0$$ (6.4)

$$\hat{Y}_{21}^{cmdm} = \frac{\hat{I}_{12}^{cmdm}}{\hat{U}_{12}^{cmdm}} |\hat{U}_{22}^{dm} = 0, \hat{U}_{12}^{dm} = 0$$ (6.5)

where again $\hat{Z}_{21}^{cmdm} \neq 1/\hat{Y}_{21}^{cmdm}$. However, when the signal paths are asymmetric, $\hat{Z}_{21}^{cmdm} \neq \hat{Z}_{12}^{cmdm}$ and $\hat{Y}_{21}^{cmdm} \neq \hat{Y}_{12}^{cmdm}$. This is because the paths for common mode and difference mode signals differ. Therefore, limits to the common to difference mode coupling must be specified separately for both paths.

Finally, limits to the common mode coupling must be specified:

$$\hat{Z}_{21}^{cm} = \frac{\hat{U}_{22}^{cm}}{\hat{I}_{12}^{cm}} |\hat{I}_{22}^{dm} = 0, \hat{I}_{12}^{dm} = 0$$ (6.6)

$$\hat{Y}_{21}^{cm} = \frac{\hat{I}_{12}^{cm}}{\hat{U}_{12}^{cm}} |\hat{U}_{22}^{dm} = 0, \hat{U}_{12}^{dm} = 0$$ (6.7)

where again $\hat{Z}_{21}^{cm} \neq 1/\hat{Y}_{21}^{cm}$. Reciprocity holds for this situation, thus $\hat{Z}_{21}^{cm} = \hat{Z}_{12}^{cm}$ and $\hat{Y}_{21}^{cm} = \hat{Y}_{12}^{cm}$.

In addition to these parameters, limitations on the difference to common mode coupling could be specified, but this type of coupling is rarely a problem in practice. Because each of these parameters can be strongly frequency dependent, all limitations should be specified as a function of frequency.

Consider for example the difference amplifier in Figure 6.5, where we added signal path 7 between two digital components (Dig 1 and 2). Because of the sensitivity of signal paths 1 and 2, limitations to the coupling are described as follows:

$$|Z_{17}^{dm}| < 1 \cdot 10^{-4} \Omega \text{ for } 1 < f < 2 \cdot 10^9 H z$$ (6.8)

$$|Z_{27}^{dm}| < 1 \cdot 10^{-4} \Omega \text{ for } 1 < f < 2 \cdot 10^9 H z$$ (6.9)

$$|Y_{17}^{cmdm}| < 1 \cdot 10^{-6} S \text{ for } 1 < f < 2 \cdot 10^9 H z.$$ (6.10)

In the quasi-static approximation, the requirements (6.8) and (6.9) define limits to the quasi-static mutual inductance: $L_{17}^{dm} < 10^{-4} \frac{H}{\Omega} \approx 8 f H$, $L_{27}^{dm} < 8 f H$. Requirement (6.10) prescribes in this quasi-static approximation a limit to the common mode
Figure 6.5: Extraction of allowed coupling between signal paths.

to difference mode capacitive coupling: \( C_{\text{cmdm}} \approx \frac{1}{4\pi \cdot 10^{-6}} \approx 80 \text{ } \mu \text{F} \). These parameters can be readily translated into layout requirements. When the circuit is expected to be electrically large (i.e., so that the signal paths become transmission lines), these requirements are translated into limitations on the mutual inductance and capacitance per unit length.

In a similar manner, the sensitivity for radiation and reception of each signal path must be specified. These requirements can be specified with the help of the radiation resistance. For example, the US FCC prescribes a radiation limit of 200 \( \mu \text{V} \text{m}^{-1} \) for class B equipment in the frequency range of 216 MHz \( \cdots \) 1 GHz at a distance of 3 meters from the radiating circuit. Now assume that signal path 6 of the difference amplifier carries a signal current \( I_{\text{MAX}} \) of 10 mA (max.), within the same frequency range. Then according to (7.2) and (7.4), the radiation resistance \( R^A \) must be smaller than:

\[
R^A_6 < \sqrt{\frac{\mu_0}{\varepsilon_0} \frac{E_{\text{MAX}}^2 d^2 4\pi}{G_A |I_{\text{MAX}}|^2}} \approx 5.58 \Omega,
\] (6.11)

where \( \mu_0 \) and \( \varepsilon_0 \) are the permeability and permittivity of vacuum, \( E_{\text{MAX}} \) is the maximum electric field allowed, \( d \) the distance from the circuit and \( G_A \) the gain of the parasitic antenna, which for parasitic dipole and loop antennas is smaller than 1.64 [11]. From this radiation resistance, we can determine the maximum size of the parasitic antennas. For example, from (5.47) it follows that the largest loop area of an electrically small signal path must be smaller than:

\[
A < \sqrt{\frac{R^A 6\pi}{\omega^2 \mu_0 (\mu_0 \varepsilon_0)^{1.5}}} \approx 12 \cdot \text{cm}^2,
\] (6.12)

which is just on the edge of being electrically small. The requirements become much stricter when the parasitic antenna is a dipole antenna, such as the common mode antenna in Figure 6.3(a). From (5.24) it follows that the length of a parasitic dipole
antenna $l$ must be smaller than:

$$l < \sqrt{\frac{R^A 6\pi}{\omega^2 \mu_0 \sqrt{\mu_0 \varepsilon_0}}} \approx 25.2 \cdot 10^{-3} m. \quad (6.13)$$

Also, limitations to reception can be expressed in terms of the radiation resistance. Assuming that the induced voltage from a field of $2 V m^{-1}$ at a frequency of $300 \text{ MHz}$ (min.) in the signal path is limited to $3 mV$, then from (5.52) it follows that the radiation resistance of this path must be smaller than:

$$R^A < \frac{\mu \sqrt{R_E}}{6\pi} \left( \frac{U_{\text{MAX}} \omega}{|E_{\text{MAX}}|} \right)^2 \approx 1.8 m\Omega. \quad (6.14)$$

Thus, to optimize a design for EM compatibility, in addition to the netlist, one needs to know the signal paths and redundant signal paths need to be known. The allowed coupling is specified in terms of transimpedances and transadmittances for each of these paths, and the sensitivity to radiation and reception is specified with the help of the radiation resistance. The limitations of each of these parameters must be specified as a function of frequency.

### 6.1.2 Hierarchical Placement and Routing

Optimally placing and routing all components for a large circuit is a rather complicated task. To simplify this task, we hierarchically divide it into a number of simpler tasks. The top level determines the shape and pinning and therefore must be routed first. Starting with the top level, we place and route complete sub-circuits. Then sub-circuits within these circuit blocks are routed until all components have been placed and routed. This procedure is illustrated in Figure 6.6. However, this sequence, requires a good estimate of the area occupied by each (sub)-circuit, which has to be determined from the schematics by calculation of the area required for the individual components and adding an extra margin for the interconnections. The guidelines to improve the EM compatibility, given in the following sections, are equal for each level of the hierarchy.

### 6.1.3 Placement of the Components

The location of the components on a chip or printed circuit board (pcb) determines the starting and end points of the signal paths and therefore to a large extent the route they must take. This section gives guidelines on placement to optimize routing.
for EM compatibility. Common mode and difference mode coupling place different demands on the placement of components. To minimize difference mode coupling, such placement must take into account the lengths of signal paths, the distance between them, the loop area and the orientation. To minimize common mode coupling, placement must be chosen such that common mode loops and dipoles are minimized or eliminated. This section presents techniques to achieve this.

Placement for Minimization of Difference-Mode Coupling

In [12] and [5], algorithms are presented that take into account the length of traces between circuits during placement of components. In [12], the length and loop area of signal paths is minimized by placing in clusters the components that have high connectivity. These algorithms, however, only have information about the netlist. Therefore further optimization of signal paths is not possible. To minimize difference mode radiation, reception and coupling, we must minimize the loop area consumed by the signal paths. This means minimizing their length and the distance between the conductors that interconnect them. Consider for example the difference amplifier displayed in Figure 6.2(a). A possible placement of the components is shown in Figure 6.7, where the biasing of the input is omitted for clarity. In this figure, circuit symbols indicate the placement of the components, and a possible routing of the signal paths has been drawn based on this placement. As noted in Section 6.1.1, the input signal path is most sensitive to reception and coupling, while the output signal path is most sensitive to reception. Due to the large distance between the two input transistors, a large loop area in the signal path is created, which makes it sensitive to reception (dashed loop in the drawing). It is common practice to place a positive supply line at the top of a schematic and the negative supply at the bottom so that all (bias) current flows from top to bottom. This topology has also been copied to

![Figure 6.7: Placement of the components of a difference amplifier.](image)
the layout. However, for EM compatibility it creates large current loops, as indicated in this figure. This makes the circuit sensitive to EM coupling and increases the loop inductance. An improved placement that minimizes the signal and supply path areas is shown in Figure 6.8. Note that these choices do not only allow minimization of the loop area of the supply and signal paths but also of the supply path: it does not circumvent the signal paths. This reduces the inductive coupling more than ten times, as previously illustrated in Figure 5.31.

To minimize the unintended coupling even further, we need to take into account length, distances and orientations. Equation (5.43) shows that mutual inductance is linearly dependent on the ratio of the length to distance. The capacitance is linearly dependent on the length to distance ratio, and thus the coupling can be minimized by keeping the connections short and maximizing the distance between them. Moreover, when signal paths have an orthogonal orientation, their mutual inductance is almost zero. This can be used to minimize coupling between sub-circuits. Consider for example the mixed-mode circuit in Figure 6.9. In this figure, the analog and digital parts have already been separated in the layout so that no coupling due overlapping signal paths can occur. However, the signal paths in both circuits are aligned in such a way that their is still inductive coupling. To reduce this coupling even further, we have orthogonalized the signal flow as depicted in Figure 6.10. Ideally, when the signal paths are fully orthogonalized, there is no inductive coupling between the two circuits.

It is not possible to minimize coupling between all signal paths. During placement, the coupling radiation and reception that is allowable must be taken into account. The list created in Section 6.1.1 is therefore sorted for the sensitivity of coupling
Design of the Layout Topology

Analog circuit
Digital circuit

Figure 6.10: Orthogonalized signal flow to minimize inductive coupling.

between signal paths. The components connected to the most sensitive signal paths are given first. This minimizes the length of the sensitive path and maximizes the distance to signal path 7 in Figure 6.5.

In practice, other non-EMC requirements like timing and thermal effects must be taken into account as well. For example, in fast digital circuits, the data paths and clock paths must have the same length to ensure that the data is fetched at the right moment. These requirements are beyond the scope of this thesis. More information about these issues can be found in [7] and [3].

Placement for Reduced Common Mode Coupling

To minimize common mode coupling, one must minimize the influence of common mode parasitic loop and dipole antennas like those illustrated in Figure 6.3. As explained in Section 5.3 and 5.4, the cross-section of a dipole and the enclosed surface area of a loop must be minimized in order to minimize the common mode coupling. A common mode dipole can be folded to reduce its cross section, while the loop area of a common mode loop is reduced by flattening it as much as possible. In Figure 6.8 for example, the difference mode as well as common mode loops are minimized. Unfortunately, the microphone in combination with the battery or loudspeaker can create a very effective dipole, as indicated in Figure 6.3(a). To minimize this dipole, it is folded as shown in Figure 6.11. This automatically implies that all terminals are placed on one side of the circuit.

Figure 6.11: Folding of a common mode parasitic dipole.
To prevent common mode coupling within a circuit, one must ensure that common mode signal paths that require isolation do not have overlapping areas. Thus, no overlap may exist between circuits that process different signals. Such overlap causes strong coupling between loops as illustrated in Figure 5.31. For example, the signal paths in Figure 6.12(a) cross a neighboring circuit, and a strong common mode coupling arises. In Figure 6.12(b), the coupling is considerably reduced by giving each circuit a separate non-overlapping area. As such optimization cannot be done in a similar manner for each common mode path, we organized the list of common mode paths in Section 6.1.1 such that the paths that are most sensitive to radiation and reception are treated first.

6.1.4 Minimization of Coupling between Paths in Difference Mode

Difference mode coupling is coupling between intended signal paths, which therefore must be kept to a minimum. This section presents three methods to do so: elimination of the use of shared conductors, minimization of overlap between signal paths, and orthogonalization of signal paths. These techniques are mainly intended for the layout of electrically small circuits. Due to the transmission line implementation of electrically large circuits, their difference mode coupling is mainly determined by the quality of the transmission lines. This is the subject of Section 6.2.

This section only treats guidelines for the routing of the conductors of signal paths. It is assumed that the area enclosed by each signal path is minimized. Thus, the conductor pairs in each signal path are aligned and placed close to each other. This allows minimization of the coupling, radiation and reception during construction, as described in Section 6.2.

The following sections treat the three methods for reducing of the coupling between signal paths.

Elimination of Conductor Sharing between Signal Paths

Because a shared conductor acts as a shared impedance, it causes a strong coupling compared to other coupling mechanisms. This mechanism dominates because the
impedance of a conductor is (in practice) almost always larger than a transimpedance
due to non-galvanic EM coupling with other paths. Ideally, all shared conductor paths
would be eliminated from a design. This can be only done by giving each signal its
own return conductor.

For example, currents of different paths can (accidentally) flow through the same
part of a common ground conductor. Figure 6.13(a) shows two signal paths $S_1$ and

![Diagram of two signal paths with a shared conductor.](image1)

\[ (a) \text{ Two signal paths with a shared conductor.} \]

$S_2$ and supply paths that all share the "ground" conductor. In Figure 6.13(b) this
problem is solved by giving each signal its own return conductor path. As the ground
conductors have the same potential, they can be connected to both sides of the path.
Still, the additional ground conductor reduces the shared impedance considerably and
thereby the unwanted coupling. To illustrate this, we reduce the coupling between
two signal paths with one shared conductor by giving each signal path a separate
return conductor. Figure 6.14 shows two signal paths with a shared conductor and
the equivalent circuit of this layout. The signal source $X_{S1}$ is connected to signal

![Diagram of supply and signal paths without shared conductors.](image2)

\[ (b) \text{ Supply and signal paths without shared conductors.} \]

Figure 6.13: Prevention of coupling due to shared conductors.

![Diagram of two signal paths coupled by a shared conductor.](image3)

\[ (a) \text{ Layout of signal paths coupled by shared conductor.} \]

![Diagram of the circuit equivalent of the coupled paths.](image4)

\[ (b) \text{ Circuit equivalent of the coupled paths.} \]

Figure 6.14: Inductive coupling due to a shared conductor.
path $S_1$ and likewise $X_{S_2}$ to path $S_2$. The inductive impedance of these paths is determined by the loop area enclosed by these paths. In this figure, the enclosed area is dashed for signal path $S_1$ and shaded in gray for signal path $S_2$. Because these paths enclose each other (total overlap of enclosed areas), there is maximal inductive coupling. The shared inductance $L_S$ almost equals the inductance $L_2$ of signal path $S_2$, because signal paths $S_1$ fully encloses the magnetic flux generated by $S_2$.

Because the area enclosed by path $L_1$ is larger than that enclosed by signal path $L_2$, its inductance is considerably higher. This follows immediately from the inductance formulas of Grover [13] and Wheeler [14, 15]. Assuming that conductors of these signal paths have Manhattan shapes (orthogonal layout) like integrated circuits or printed circuit boards, then (according to [13]) the inductance per unit length of signal path $L_1$ is given by:

$$L_1 \approx \left[ \ln \left( \frac{d_1 + W}{W + t} \right) + 1.5 + \ln(k) \right] 4 \cdot 10^{-7} [H m^{-1}],$$

(6.15)

where $d_1$ is the distance between the conductors, $W$ the width and $t$ is the thickness of the conductors. Constant $k$ is given in table 3, page 20 of Grover [13]. For most printed circuit boards, when $t \ll W$, $k \approx 0.22313$. Let us assume that the traces have a width of $W = 2 mm$ and the traces of signal path $S_2$ are $d_2 = 1 mm$ apart, while those of $S_1$ are $d_1 = 10 mm$ apart. Then the inductance $L_1 \approx 1.21 \mu H m^{-1}$, while the inductance of signal path $S_2$ $L_2 \approx L_S \approx 0.15 \mu H m^{-1}$ is considerably smaller.

When this shared impedance is eliminated, the paths are ideally separated. However, when the (formerly) shared conductor is shortened on both ends, the configuration of Figure 6.15 arises. Galvanic coupling still exists. However, as shown by (6.15), the signal paths have a much lower inductance than the larger loop created by the two ground conductors. Therefore, the shared impedance is reduced considerably.

A ground plane is often implemented as a shared conductor for many signal paths. This situation is comparable to that in Figure 6.15. Again the signal current follows the conductor part that is physically closest to it. This is often called the proximity principle. Therefore, the ground plane gives a similar result as in Figure 6.15.

The removal of shared conductors can increase the number of connections considerably, which may not be feasible due to limitations of the chip or printed circuit board area. Therefore, the list of Section 6.1.1 can be used to modify the paths that are most sensitive to coupling.

Note that it may be possible to eliminate shared conductors in an automated routing algorithm. However, the algorithm must have knowledge of the signal paths present in the system. This is not possible with the currently available software, which only uses the netlist [5, 16, 8].

### Minimization of Overlap between Signal Paths

Overlap between signal paths arises when the enclosed area of one signal overlaps other signal paths. As shown in Figure 5.31, overlap results in inductive coupling that is relatively strong compared to other types of non-galvanic coupling and therefore has to be minimized. This overlap is already considerably reduced by eliminating the use of shared conductors in the previous paragraph, because the reduction of loop area reduces the overlap. Moreover, enclosure of signal paths is eliminated as in the examples in Figure 6.14(a) and 6.15(a).
Design of the Layout Topology

Figure 6.15: Reduced inductive coupling due to a shared conductor.
Theoretically, the overlap between signal paths can always be reduced to crossing of signal paths. Each signal path is a two-conductor connection and can be considered as one entity that may not be divided into two conductors. Supply lines are treated in a similar manner, because the currents they carry may also interfere with signals.

To implement this, however, the terminals of components must be placed such that signal ports are grouped. Figure 6.16 shows a layout where overlap between signal paths arises due to a bad choice of terminal layout. This figure shows a common terminal layout of an integrated circuit with two operational amplifiers. The supply terminals $V_{ss}$ and $V_{dd}$ have been chosen such that overlap between the supply lines and the signal paths cannot be prevented (the area enclosed by the supply paths is gray in this figure). Moreover, by placing the single-ended output terminal of the amplifier on the other side of the component package, a similar loop is created in the output signal paths. Without adding more terminals, the layout can be improved by grouping the terminals of all signal ports as shown in Figure 6.17. In this figure, the overlap is reduced to one crossing of signal paths. By placing the supply terminals next to each other, overlap between the supply and signal paths is prevented. By placing the output terminals of the operational amplifiers next to the negative input, the loop area of the signal paths is minimized, while overlap is prevented.

Note that this prevention of overlap can always be implemented if sharing of conductors has been eliminated. Again, this is only possible if enough chip or printed circuit board area is available for the layout. Otherwise it must be applied only to the most sensitive signal paths.
Orthogonalization of Signal Paths

In addition to elimination of shared conductors and prevention of overlap, orthogonalization of the signal paths can be applied to reduce the coupling between signal paths even further. This procedure is explained in Section 6.1.3, where this orthogonalization is already being taken into account during placement of the components. Figure 6.10 shows how the signal paths of two sub-circuits are orthogonalized to minimize coupling. On a printed circuit board of an integrated circuit, this method can only be used to reduce coupling between two groups of signal paths. Therefore it useful in mixed-mode circuits for example, to reduce the coupling between the analog and digital part. Alternatively it may be used to reduce the coupling between a dipole antenna and circuit, by placing the antenna orthogonal to the traces in the circuit.

6.1.5 Minimization of Coupling between Paths in Common Mode

In Section 5.1.1, methods were explained to detect common mode parasitic antennas. As explained in that section, the signals radiated and received by these parasitic antennas are always parasitic. They arise due to a non-balanced circuit implementation. A properly designed circuit is not very sensitive for both radiation and reception of these common mode signals. However, the parasitic common mode antennas in a layout can easily become large and efficient. Therefore the influence of these parasitics has to be minimized. This section explains techniques to accomplish this.

Two methods for reducing common mode coupling were already presented in Section 6.1.3. These are minimization of the cross section of parasitic dipole antennas as illustrated in Figure 6.13 and reduction of the loop area as illustrated in Figure 6.11. To reduce the effectiveness of parasitic dipoles even further, a shielding plane can be applied. The shielding plane must be placed at a distance much shorter than $\lambda/4$. The reduced radiation for parasitic dipole and loop antennas is described by Equations (5.26)- (5.31) and (5.48)- (5.50). The reduction in induced voltage for the parasitic dipole and loop is described by (5.36) and (5.53).

In addition to the effectiveness of these antennas, the coupling to the circuit can also be reduced by adding circuit components that do not alter the circuit itself but only the coupling to the parasitic antennas. These measures are covered by literature on EMC [1, 2]. This section briefly reviews two of the most important methods. Which measures can be used depends on the distance between the terminals of the parasitic antenna. When the distance is electrically short, the parasitic antennas can be shortened for common mode signals. This is illustrated in Figure 6.18. The parasitic dipoles created by the microphone wires, speaker wires, and the battery are shortened for high-frequency signals by the decoupling capacitors. This current runs through the ground strip, isolated from the circuit. It is assumed that the decoupling capacitors in this figure have no influence on the (low frequency) signals, processed by the amplifier. Furthermore, the ground plate must be electrically short to be effective. This is a very primitive approach for filtering the signals. Better designs for distributed filters can be found in the literature on EMC. EMC filters are also commercially available optimized for the most important transmitters like mobile phones. However, when the distance between the input ports is too large or the path between the port runs over the circuit, the antenna can be given a high common mode
impedance. This is illustrated in Figure 6.19. Ideally the common mode transformers in this circuit have no influence on difference mode signals in the paths. However, for a common mode parasitic signal, a high impedance is created that isolates the parasitic dipole or loop antenna.

Summarizing, there are two methods to minimize the influence of common mode parasitic antennas: reducing their effectiveness in the layout, and isolating them from the circuit by filtering them at the terminals.

### 6.2 Implementation of the Layout

In Section 6.1, the signal paths were routed such that coupling is minimized. In principle each signal path is implemented by a two-conductor connection, where the conductors run in parallel so that any construction (planar, microstrip, coax) is possible. This construction must be chosen such that the requirements for maximal allowed coupling, radiation and reception are met. To help a designer finding the best construction, this section discusses the coupling, radiation and reception parameters of different signal path constructions. It only discusses planar constructions (i.e., those suitable for printed circuit boards and integrated circuit boards). Only a coaxial design (e.g., one conductor completely that encloses the other), such as semi-rigid
coaxial cable, performs best for all coupling parameters. For a planar implementation, it will be shown that an optimal solution does not exist. Each construction can be optimized for only one coupling parameter. For example, minimal differential capacitive coupling can rarely be achieved in conjunction with minimal inductive coupling. The minimal coupling to be obtained depends on the available technology (number of metal layers, feature size). The following sections discuss the coupling parameters that can be obtained with signal paths implemented in one, two or three metal layer processes. Section 6.2.1 treats the construction of an ideal signal path, which serves as reference for practical signal paths. The subsequent sections treat the practical implementation of signal paths.

6.2.1 An Optimal Signal Path Implementation

The ideal signal path would have no length, so that transport time and EM coupling vanished. In practical circuits, where signal paths have finite dimensions, the ideal signal path is a leakage-free EM channel: a two-conductor connection that does not radiate or receive EM signals. It should be linear and free of dispersion, so that only one propagation mode is allowed. This ideal can only be obtained when one of the two conductors completely encloses the other, like the rectangular and coax connection depicted in Figure 6.20. The EM radiation and reception vanish if the outer conductor has infinite conductivity, because the transported EM wave (electric signal) is shielded by the outer conductor. In Appendix F it is proven that any other configuration, where one conductor does not fully enclose the other, suffers from radiation and reception. As a second condition we want medium between the conductors to be linear and homogeneous, while the cross section \(d\) in Figure 6.20 must be electrically small, to ensure one propagation mode.

The ideal connection is an electrically thin connection with an outer conductor that completely encloses the inner one. To approximate such a connection on chip or printed circuit board, the “inner” conductor must be surrounded by “outer” conductors as much as possible. The field radiated by the currents flowing through the “inner” and “outer” conductors must cancel each other. Therefore the “outer” conductors have to be aligned as closely as possible to the “inner” conductor. The closer the electrical distance between the “inner” and “outer” conductors, the smaller the phase error between the fields generated by the forward and reverse currents flowing through them, thus the better these fields compensate each other.

Figure 6.20: Closed signal path implementation.
In the following subsections, the coupling parameters are determined for planar implemented interconnections. The coupling is described with the help of the transimpedance and transadmittance parameters presented in Section 6.1.1 (see page 116). The common-mode (cm), difference-mode (dm), and common-difference-mode (cmdm) transimpedance and transadmittance are described by the mutual inductances and capacitances, respectively (e.g. $Z_{12}^{cm} = j\omega L_{12}^{cm}$, $Z_{12}^{dm} = j\omega L_{12}^{dm}$, $Z_{12}^{cmdm} = j\omega L_{12}^{cmdm}$, $Y_{12}^{cm} = j\omega C_{12}^{cm}$, $Y_{12}^{dm} = j\omega C_{12}^{dm}$, $Y_{12}^{cmdm} = j\omega C_{12}^{cmdm}$).

### 6.2.2 Single Layer Signal Path Implementations

In a case where only one metal layer is available, the construction with the lowest radiation resistance is an acoplanar waveguide implementation, where the “inner” conductor is guided by two “outer” conductors as depicted in Figure 6.21(b). The two outer conductors are one current path that carry the return current. A better single layer construction does not exist, because no other planar construction surrounds the inner conductor better. In this table, $d$ is the distance between the centers of the traces, $l$ the length of the path, $\omega$ the signal frequency ($\text{radsec}^{-1}$), $\mu$ the magnetic permeability and $\varepsilon$ the electric permittivity. These expressions have been determined for a homogeneous medium. In practice the resistance will be slightly higher due to the higher permittivity $\varepsilon$ of the substrate. The coplanar stripline has a much smaller radiation resistance than the coplanar stripline, due to its balanced construction. The return current is divided over the two outer conductors, so that the signal current flows in two adjacent current loops with opposite direction. The fields generated by these adjacent loops attenuate each other. The radiation resistance of the coplanar stripline is two times that of a micro-stripline (see [17, 18]).

![Figure 6.21: Layout of single layer signal paths.](image-url)

Table 6.1: Radiation resistance of single layer planar interconnect.

<table>
<thead>
<tr>
<th></th>
<th>coplanar stripline $\approx \frac{d^4 \omega^4 \mu^2 \varepsilon^2}{125 \sigma}$</th>
<th>coplanar waveguide $\approx \frac{3d^4 \omega^6 \mu^3 \varepsilon^2}{6801 \sigma}$</th>
</tr>
</thead>
</table>
Table 6.2: Inductive coupling parameters of single layer planar interconnect.

<table>
<thead>
<tr>
<th></th>
<th>coplanar stripline</th>
<th>coplanar waveguide</th>
</tr>
</thead>
<tbody>
<tr>
<td>$L_{12}^{dm}$</td>
<td>$\approx \frac{\mu}{2\pi} \frac{r^2d^2}{r^2 + \sqrt{r^2 + l^2}}$</td>
<td>$\approx \frac{3\mu}{8\pi^2} \frac{l^2d^2}{r^2 + 5r^2 - l^2} + \frac{15\mu}{r^2 + 5r^2 - l^2} d^4$</td>
</tr>
<tr>
<td>$L_{12}^{cmdm}$</td>
<td>$\approx \frac{2\mu}{2\pi} \left( \frac{\sqrt{r^2 + l^2}}{r} - 1 \right)$</td>
<td>$\approx \frac{\mu}{8\pi} \frac{l^2d^2}{r^2 + 5r^2 - l^2} + \frac{15\mu}{2\pi^2} \frac{l^2d^2}{r^2 + 5r^2 - l^2}$</td>
</tr>
<tr>
<td>$L_{12}^{cm}$</td>
<td>$\approx \frac{\mu}{2\pi} \left[ 2r - 2\sqrt{l^2 + r^2} + \frac{\mu}{8\pi} \frac{l^2d^2}{r^2 + \sqrt{l^2 + r^2}} \right]$</td>
<td>$\approx \frac{\mu}{2\pi} \left[ 2r - 2\sqrt{l^2 + r^2} + \frac{\mu}{8\pi} \frac{l^2d^2}{r^2 + \sqrt{l^2 + r^2}} \right]$</td>
</tr>
</tbody>
</table>

In Table 6.2, the inductive coupling of the two interconnection types is compared. As this table shows, the difference-mode and common-difference-mode inductive coupling between coplanar waveguides is considerably smaller than that between coplanar striplines, due to the balanced layout. The expressions in this table have been derived for an interconnection of finite length. In Chapter 4 of Grover [13], expressions are given for the mutual inductance per unit length of infinitely long interconnections. It can be verified that in the limit of $l \to \infty$, the equations of Table 6.2 are equal to those of Grover.

Closed-form expressions for capacitive coupling are hard to find. We therefore created a small simulator (based on the moment method) that uses a piecewise linear approximation for the charge distribution on the conductors. With this simulator we compared the capacitive coupling between coplanar striplines and coplanar waveguides. Figure 6.22 shows the inductive and capacitive coupling parameters of two coplanar stripline and two coplanar waveguides with a trace width $w$ of 1 mm, a length $l$ of 10 cm, and a distance $d$ between the traces of 1.1 mm as a function of the distance $r$ between the paths (see Figure 6.22). The Figures 6.22(a) and 6.22(b) show that the inductive coupling of the coplanar waveguide is about ten times less than the coupling between coplanar striplines. However, the capacitive coupling (see Figure 6.22(d) and 6.22(e)) increased by about the same factor. Therefore the coplanar stripline is preferred for current domain signals, while the coplanar waveguide is preferred for voltage domain signals.

To verify the accuracy of the simulator, we calculated the capacitance per unit length of a coplanar line, for which an exact closed-form expression exists (see [19, 20]). Figure 6.23 shows that simulated value is in good agreement with the exact value.

### 6.2.3 Double Layer Signal Path Implementations

The signal paths that can be constructed with two metal layers are a microstrip line and a coplanar waveguide with ground plane (see Figure 6.24). The latter has the lowest radiation resistance due to the additional return conductors. However, the coplanar waveguide with ground plane has a higher radiation resistance than the coplanar waveguide without ground plane. In this section, we compare the EM coupling parameters of the microstrip line and the coplanar waveguide with the coupling parameters of the coplanar waveguide. To analyze the performance of the copla-
Figure 6.22: Mutual inductive and capacitive coupling between coplanar striplines and coplanar waveguides.
Figure 6.23: Simulated versus exact capacitance of a coplanar stripline.

Figure 6.24: Layout of a coplanar waveguide with ground plane.

A coplanar waveguide with ground plane, it is considered as a microstrip and a coplanar waveguide in parallel as illustrated in Figure 6.25. The radiated power $P_{rad}$ and radiation resistance $R_A$ per unit length of these two transmission lines are given by:

\[
\begin{align*}
P_{rad} &= f^2 \left[ \left( \frac{Z_c}{Z_c + Z_m} \right)^2 R_m^A + \left( \frac{Z_m}{Z_c + Z_m} \right)^2 R_c^A \right], \\
R_A &= \left[ \left( \frac{Z_c}{Z_c + Z_m} \right)^2 R_m^A + \left( \frac{Z_m}{Z_c + Z_m} \right)^2 R_c^A \right].
\end{align*}
\]

In this equation, $R_m^A$, $Z_m$, and $R_c^A$, $Z_c$ are the radiation resistance and characteristic impedance of the microstrip and coplanar waveguide, respectively. If the radiation resistance of both lines were in the same order of magnitude, the combined radiation resistance would drop. However, the microstrip line has a considerably higher radiation resistance than the coplanar waveguide. The combined radiation resistance is therefore higher. Hence, the ground plane increases the radiation resistance, because it makes part of the signal current flow through a path with a much higher radiation resistance.

The microstrip, however, forms one radiative loop with an radiation resistance of:

\[
\rho_{a:microstrip} \approx \frac{\pi \omega^4 \mu^2 \epsilon^{\frac{1}{2}}}{7.5 \pi} L^2,
\]

\[
\text{\cite[17, 18]{footnote}}
\]
where $t$ is the thickness of the substrate. Figure 6.26 compares the radiation resistance of a stripline with that of a coplanar waveguide with ground plane as a function of the frequency, where the width $w$ is 1 mm, the distance between the traces $d$ equals 1.1 mm, the thickness $t$ of the substrate is 0.5 mm, and the length $L$ is 10 cm. To calculate

\[ r(f) = \begin{cases} 5 \times 10^6 & \text{for stripline}, \\ 1.5 \times 10^7 & \text{for compound}, \\ 2 \times 10^7 & \text{for coplanar waveguide with ground plane}. \end{cases} \]

Figure 6.26: Radiation resistance of the stripline versus a shielded stripline.

the compound radiation resistance, the impedance parameters given in [21, 22, 23] and [20, 19] have been used. It must be noted that when the ground plane under a coplanar waveguide is disconnected from the signal ground, no signal current can flow through it, so that it becomes a shielding plane. In that situation it can only lower the radiation resistance of the coplanar waveguide.

Closed-form expressions of the inductive coupling parameters of these lines are complicated; we therefore integrated the Neumann integral (5.43) numerically, using the geometrical mean distance as explained in Chapter 4 of Grover [13]. To determine the capacitive coupling parameters, we used the same simulator as in the previous paragraph. Figure 6.27 shows the results for two signal paths with a trace width $w$ of 1 mm, a length $l$ of 10 cm, and a distance $d$ between the traces of 1.1 mm. It is assumed that the neighboring paths have separate ground conductors. A comparison of Figure 6.27(a) and 6.27(b) with Figure 6.27(d) and 6.27(e) shows that the lines with lower inductive coupling have a higher capacitive coupling and vice versa. For
Figure 6.27: Comparison of the mutual inductances and capacitances of a coplanar waveguide, a microstrip and a coplanar waveguide with ground plane.
current domain signals therefore the microstrip line is preferred over the coplanar waveguide, while for voltage domain signals, the coplanar waveguide is preferred.

### 6.2.4 Triple-Layer Signal Path Implementations

With three metal layers, a stripline and a shielded stripline can be constructed, as depicted in Figure 6.28. The shielded stripline can be considered as a coplanar waveguide and a stripline in parallel. However, this shielded stripline suffers more from inductive coupling than the stripline, just like the shielded coplanar waveguide. In this section, the coplanar waveguide, stripline and shielded stripline are compared. Due to the large top and bottom conductor, the power radiated by the stripline and shielded stripline can be ignored. This type of signal path therefore performs the best of all planar paths. The shielded stripline analyzed in this section is not equal to a stripline guarded by vias from top to bottom plate. With vias, a coaxial line can be approximated, so that coupling almost vanishes.

To calculate the coupling parameters of the shielded stripline depicted in Figure 6.28, we considered it to be the sum of a coplanar waveguide and a stripline (see Figure 6.29). The coplanar waveguide in Figure 6.29 is considered to be embedded in an infinitely large substrate. To calculate the coupling parameters, we used the expression given by [24, 25] and [22, 23]. Because closed-form expressions for the coupling parameters are hard to determine, we used the same numerical methods as in the previous paragraphs. Figure 6.30 shows the coupling parameters of two signal paths with a trace width $w$ of 1 mm, a length $l$ of 10 cm, and a distance $d$ between the traces of 1.1 mm. The thickness of the substrate is 1 mm. A comparison of Figure 6.30(a) and 6.30(b) with 6.30(d) and 6.30(e) shows that again the lines with the least inductive coupling have the most capacitive coupling and vice versa. The coplanar striplines (see Figure 6.21(a)) have the least capacitive coupling and are therefore best suited for current domain signals; striplines have the lowest inductive coupling and are therefore best suited for voltage domain signals. Additional shielding conductors do not improve the microstrip.

In conclusion, signal paths are most often implemented by microstrip lines, because of their compact and cheap implementation. For a low-radiation resistance, however, microstrip lines are the worst implementation. The best planar implementation is...
Figure 6.30: Mutual inductances and capacitances of a coplanar waveguide, a stripline and a shielded stripline.
the stripline, because it is almost fully shielded. However, in practice it is difficult to properly connect components to a stripline. The coplanar waveguide is therefore a good alternative. It combines a low radiation resistance with a simple construction. A drawback of the coplanar waveguide is that often it requires very small conductors to keep the impedance reasonable. For example on a FR4 substrate ($\varepsilon_r = 4.5$), a 50 ohm microstrip line has a width of 1.57 mm, while a 50 ohm coplanar waveguide with a spacing of 0.2 mm has a width of only 0.69 mm. The radiation resistance of a coplanar waveguide can be lowered even further with the help of a shielding plane which is not connected to the signal path. However, a ground plane that is connected to the signal path increases the radiation resistance.

6.3 Conclusions

Before a layout can be optimized for EM compatibility, the netlist of connected component terminals must be replaced by a list of signal paths (conductor pairs) connected to signal ports (terminal pairs) of components or subcircuits. The EMC layout requirements are described consisting of allowed mutual impedances, admittances between signal paths, and their radiation resistances. This radiation resistance not only describes the far-field radiation but also the reception. The layout is mainly optimized during placement of the components, when signal paths are orthogonalized and the cross section of parasitic common mode antennas is minimized. Currently no automated placement and routing tools are available, which using signal path descriptions can optimize the EM compatibility of a layout. More research is therefore required to develop such tools.

While microstrip constructions are most popular for signal path implementation, they suffer a lot from inductive coupling, radiation and reception. For planar implementation, three conductor signal paths have the least parasitic coupling, where a center conductor is guided by two outer conductors, like the coplanar waveguide and stripline. Because the stripline cannot be combined with surface-mounted components, the coplanar waveguide can be a good alternative. Such shielding is at the expense of extra chip or PCB area for the extra conductors and to obtain the required line impedance.
Bibliography


Chapter 7

A New Circuit Extraction method for Simulation of Electromagnetic Compatibility

A physical design should be simulated using a simulator model (e.g., in SPICE, Spectre) in order to verify its electromagnetic compatibility (EMC) before it is implemented. This simulation must be detailed enough to capture any unintended EM interactions as well as the effects of parasitic signals on the circuit’s behavior. In this work, such simulation is performed in two steps. First, an equivalent circuit model is extracted from the layout. This extracted circuit is then simulated with a circuit simulator. The extracted circuit includes the EM interaction, so that the influence of the EM interaction as well as the (non-linear) processing of interfering signals by the circuit components can be analyzed with the help of a circuit simulator. This chapter presents a new circuit extraction methodology that improves the accurate over existing methods and that is able to handle any type of layout.

There are many EM simulation tools on the market today that analyze physical layouts through numerical simulation of Maxwell’s equations. Examples of such tools are: FLO/EMC [1], which is based on a transmission-line representation of the Maxwell equations; SimLab, which is based on the partial equivalent circuit model (PEEC) developed by Ruehli at IBM [2]. Other simulators are based on the method of moments (MOM) equation solver [3], Fasterix [4] is based on quasi-static MOM, while finite element analysis (FEM) is used by EMax of Ansys and FeMAX [5] simulators. Most of these simulators can solve the EM fields within a circuit to a high level of accuracy. However, the methods used for translation of these results into a circuit equivalent are not suited for all types of layout. Often it is assumed that the impedances of a port of a network can be calculated independently of the component connected to it. However, the component takes part in the electromagnetic interaction with the network and therefore the port impedance “observed” by the component is also dependent on the component itself. A circuit extraction program
uses an excitation source to “measure” the impedance of a port in simulation. This excitation source therefore must have the same physical properties as the component that is connected to that port. However, most circuit extraction programs use an excitation source with different physical properties and therefore observe a different impedance. Only in special cases like a transmission layout, where the EM interaction with the excitation source is similar to the EM interaction with the component, accurate results can be obtained. The impedance of a port is determined from the voltage-current relationship measured at the terminals of a port. To determine the voltage, a quasi-static approximation of the electric field between the terminals of a port are made. This approximation introduces a small phase error that can be ignored for one port. However, in large circuits with many components, the accumulated error cannot be ignored and causes problems in simulation of the extracted circuit [6].

This chapter presents a new circuit extraction method that is able to extract an accurate equivalent circuit for any type of layout of any size. It includes the physical properties of the network and the components in the simulation, such that extracted network impedances equal the impedance “observed” by the component. In stead of “measuring” the current-voltage relationship in simulation, the impedance is calculated from the EM power transfer between the circuit components and the currents flowing through them. Therefore the voltages in the extracted circuit do not exactly represent the port voltages in the layout, but rather the power flow through these ports. By relating the impedances to the power transfer, the phase error introduced by the quasi-static electric field approximation is eliminated. A comparison of measurement and simulation results at the end of this chapter demonstrates the accuracy of this method.

To simplify the simulation method, the most important geometrical effects of the components are parameterized, so that the results for a wider range of component (physical) layouts, can be obtained with a few simulations. To calculate the EM-interaction numerically, a boundary-element MOM numerical method is used. Unfortunately, such methods suffer from aliasing errors that are caused by the spatial sampling of the EM fields. These errors can reduce the accuracy of the simulation considerably. To improve the accuracy a new spatial anti aliasing filter is introduces, whose bandwidth is adapted to the applied grid spacing for optimal accuracy.

Section 7.1 presents a circuit model that represents all intended and unintended EM coupling, and describes the applied circuit extraction method. Section 7.2 formulates the circuit extraction problem mathematically with the help of Green’s theory. Section 7.3 treats a numerical MOM implementation, where a spatial anti aliasing filter is introduced to improve the accuracy. Finally, Section 7.4 uses these methods to calculate the impedance of a loop antenna. This example demonstrates the influence of different load geometries on the impedance and compares simulation with measured results.

7.1 Circuit Extraction Using EM analysis

An extracted circuit must represent three types of unintended EM-interactions: reception, emission and coupling. Reception and emission describe the EM interaction with the external and often unknown environment, using the weak coupling approximation described in Section 3.2.1 and 5.2.2. EM coupling is the unintended interaction
within a circuit. To make the influence of these interactions visible for the designer, the extracted circuit is an extended version of the original simulation netlist. The extracted circuit therefore uses the same nodes as the original design and only adds components and nodes to represent unintended interaction.

The electric potential difference can only be defined over electrically short distances (see Section 5.2.3), and therefore port representations are applied to electrically large sub-circuits (see Section 3.2.3).

Subsection 7.1.1 gives an overview of the current simulation techniques that are applied to different layout geometries. Subsection 7.1.2 describes a circuit representation for EM compatibility parameters like emission, reception and coupling. Finally Subsection 7.1.3 introduces a new circuit extraction method for calculation of an equivalent circuit from a numerical EM field simulation.

### 7.1.1 Overview of EM Simulation Techniques for Circuit Extraction

The circuit model in this thesis has been derived from an EM-simulation of an impedance measurement. A source is applied at the terminals of a circuit and a response is “measured” in simulation. In case of an electrically small circuit layout,

![Flowchart of simulation techniques for circuit extraction.](image)

quasi-static approximations can be used to determine the capacitive (electric) and inductive (magnetic) coupling independently (branch A Figure 7.1). The mathematical formulation used to compute the equivalent circuit parameters depend upon the materials properties of the medium surrounding the interconnection (i.e., homogenous or non-homogenous).

A layout that is electrically large (branch B in Figure 7.1) is treated in one of two ways. For components that are electrically large in one dimension (e.g., a ca-
ble interconnection at high frequency), a transmission line approximation can be used. Multi-dimensional electrically large circuit layouts require antenna simulations to extract their EM-coupling parameters. For both quasi-static and dynamic EM simulations, the field equations can be solved numerically using the integral form of Maxwell’s equations (employing Green’s function theory) when the medium is homogeneous or layered [7]. This has a numerical advantage over the differential formulation, because only the current- and charge-carrying conductors need to be discretized and stored in memory, which saves memory and improves the speed of simulation. This method is not suited for non-homogeneous, non-layered media however, which require a differential formulation.

### 7.1.2 Circuit Model Representation for EMC Simulations

To extract a circuit model that is an extension of the original simulation netlist, we partition the components and interconnections as explained in Section 5.2.3. The extracted model must represent all three unintended EM-interactions: reception, emission, and unintended coupling. This section describes the circuit representation of these interactions.

The nodes in the model must correspond to the terminals of the circuit components (e.g., terminals of the resistors, capacitors, coils, diodes, transistors, etc.), where it is assumed that the components themselves are electrically small. The interconnect can always be represented by a port model as explained in Section 3.2.3. Figure 7.2 illustrates the translation of a layout into a port model. The terminals for each

![Figure 7.2](image-url)
in Figure 7.2(b), where each port comprises two terminals. The received parasitic signals are represented by dependent voltage sources \( \hat{U}_{par} \) in series with each port, as follows from the weak coupling approximation explained in Section 5.2.2. The emission is described by a radiation resistance, which is part of the impedance matrix that relates the port voltages of the interconnect. This port representation can be used for electrically large as well as electrically small layouts. However, when the layout is electrically small, a lumped-element equivalent network can be derived.

The corresponding mathematical description of this model is given by:

\[
[U_1, U_2, \ldots, U_n] = [U_{par,1}, U_{par,2}, \ldots, U_{par,n}] + [Z_{i1}^i, Z_{i2}^i, \ldots, Z_{in}^i] [I_1, I_2, \ldots, I_n]^T + [A_{11}^A, A_{12}^A, \ldots, A_{1n}^A; A_{21}^A, A_{22}^A, \ldots, A_{2n}^A; \ldots; A_{n1}^A, A_{n2}^A, \ldots, A_{nn}^A] [I_1, I_2, \ldots, I_n]^T
\]

(7.1)

where \( U_i \) and \( I_i \) are the voltages and current across and through port \( i \), \( U_{par,i} \) the parasitic signal induced for this port due to an external parasitic source, \( Z_{ij}^i \) transimpedances between the ports \( i \) and \( j \), and \( R_{ij}^A \) the radiation resistances. With the radiation resistance matrix \( R_{ij}^A \), an estimate of the far-field radiation of the circuit is made. It should be noted that (7.1) gives all the desired EMC parameters: reception (\( U_{par} \)), emission (\( R^A \)) and coupling (\( Z^A \)).

The far-field emission follows from the total emitted power \( P_R \), which is given by:

\[
P_R = \frac{1}{2} \Re [\mathbf{I}^T \mathbf{R}^A \mathbf{I}],
\]

(7.2)

where \( \mathbf{I}^* \) is the complex conjugate of \( \mathbf{I} \) and \( \Re [x] \) the real part \( x \). The maximal electric \( E^{\text{max}} \) and magnetic \( H^{\text{max}} \) far fields equal approximately:

\[
H^{\text{max}} \approx \left( \frac{\varepsilon_0}{\mu_0} \right)^{\frac{1}{2}} \frac{1}{\sqrt{4\pi}} d^{-1} \sqrt{G_a \cdot P_R} \approx 14.5 \cdot 10^{-3} d^{-1} \sqrt{G_a \cdot P_R}
\]

(7.3)

\[
E^{\text{max}} \approx \left( \frac{\mu_0}{\varepsilon_0} \right)^{\frac{1}{2}} \frac{1}{\sqrt{4\pi}} d^{-1} \sqrt{G_a \cdot P_R} \approx 5.5d^{-1} \sqrt{G_a \cdot P_R},
\]

(7.4)

where \( G_a \) is the power gain of the parasitic antenna with respect to an isotropic radiator, \( \varepsilon_0 \) and \( \mu_0 \) the permittivity and permeability of free space, and \( d \) is the distance from the parasitic antenna. Parasitic antennas often behave like loop or dipole antennas that have a gain \( G_a \) of about 1.5 to 1.64 [8]. This far-field approximation is only valid at a distance of several wavelengths from the parasitic antenna. For example, the FCC emission limits for class B equipment is \( 200 \mu\text{V} \cdot \text{m}^{-1} \) at a distance of 3 meters for a frequency range of 216 \( \cdots \) 960MHz. From (7.4) it follows that the radiated
power therefore must be less than 7.25nW, which limits the radiation resistance and signal current as follows from (7.2).

In principle, the non-galvanic interaction between circuit components within the environment should be taken into account as well. When the components are much smaller then the interconnect, this interaction can often be ignored. For physically larger components like coils and transformers this interaction must be taken into account. However, due to the complex geometry of these components, it is practically very difficult to enter the geometry in a simulator. The next section introduces approximation techniques to simplify the analysis of this interaction.

### 7.1.3 Modeling EM Interaction between Components and their Associated Interconnect

A circuit description describes the energy exchange between components with the help of impedances. These impedances are defined as the relation between the current that flows through a component and the voltage across its terminals. The impedance values are conventionally determined under the assumption that the EM interaction is confined between the component's terminals. However, for EM compatibility analysis the non-galvanic interaction due to radiation and reception must be taken into account, too. To enable analysis with the help of a circuit simulator, this non-galvanic interaction should be included in the circuit description. We therefore let the voltages in the equivalent circuit be a measure of the total transferred EM energy, which includes radiation and reception. This section describes a method to calculate such an equivalent circuit. It must be noted that because the EM-interaction depends on the layout of both component and interconnect, the impedance matrix of the interconnect is also dependent on the geometry of the components attached to it. Hence, this impedance matrix is not a property of only the interconnect, but also of the components connected to it. It is the impedance matrix that is “observed” by the components.

The extracted circuit consists of two impedance matrices: $\hat{Z}_c$, the impedance matrix of the circuit components, and $\hat{Z}_\text{net}$, the impedance matrix of the network (interconnections). We let the circuit component matrix $\hat{Z}_c$ be a diagonal matrix, where the diagonal consists of the impedance matrices of the individual components in free space (the components in Figure 7.2(b)). The network impedance matrix $\hat{Z}_\text{net}$ describes the coupling between these components, which is a combination of coupling via the interconnect and the direct EM-interaction between the components due to emission and reception. In this definition we have chosen the component impedance matrix to be independent of the interconnect, so that it is the components their property and not a function of the interconnect.

The most straightforward method for calculating the individual transimpedances of the impedance matrix of the interconnect, removes all components and calculates the open port voltages due to a current excitation applied to each port. The components themselves, however, also influence the EM interaction between them. Therefore the network impedance matrix $\hat{Z}_\text{net}$ must be determined with all components inserted. For calculation of the impedance matrices, $n$ different current excitations are required, where $n$ equals the number of ports (terminal pairs) of the network. During each excitation, the current flowing through one port is defined by an EM boundary condition (see Section 7.2.2), while the current flowing through the other
ports and the power emitted by each component is determined with the help of an EM field simulation. We describe the currents flowing through all components for each of these excitations with the help of a current matrix $\hat{I}$. Element $\hat{I}_{ij}$ of this matrix equals the current flowing through port $i$ during excitation $j$. The power transferred to each component is described by a voltage matrix $\hat{U}$, where element $\hat{U}_{ij} = \hat{P}_{ij}/\hat{I}_{ij}^*$ equals the power $\hat{P}_{ij}$ emitted by component (or component part) $i$ during excitation $j$, divided by the complex conjugate of the current $\hat{I}_{ij}$ flowing through this component.

We describe the circuit extraction procedure with the help of the layout depicted in Figure 7.3(b). This layout consists of a resistor and a transistor that are connected with each other. First the impedance of the individual components is determined.

![Figure 7.3: Calculation of an equivalent circuit of a two component network.](image)

The components are placed in free space as illustrated in Figure 7.3(a), a current excitation is applied, and the power emitted by each component is calculated. The current excitation is obtained by defining the tangential magnetic field $\partial \hat{H}$ over the surface of the component, as will be explained in Section 7.2.2. The radiated power is determined by integration of Poynting’s vector over a surface $S$ that encloses the components (Surfaces $S_1 \cdots S_3$ in Figure 7.3(a)). Because the voltage across the port terminals of these components in the equivalent circuit must represent the total power transfer through surfaces $S_1 \cdots S_3$, the emitted power is used to calculate the
impedance. The impedance of the resistor in Figure 7.3(a) is therefore defined as:

\[ \hat{Z}_{C:11} = \frac{1}{\hat{I}_1} = \frac{\hat{P}_{\text{rad}}}{\hat{I}_1^*} = \frac{\hat{P}_{\text{rad}}}{|\hat{I}_1|^2}. \] (7.5)

The transistor is a two-port system, therefore two different excitations are required to calculate its impedance matrix. The impedance matrix of this component is given by:

\[
\begin{bmatrix}
\hat{Z}_{C:22} & \hat{Z}_{C:23} \\
\hat{Z}_{C:32} & \hat{Z}_{C:33}
\end{bmatrix}
= \begin{bmatrix}
\hat{U}_{22} & \hat{U}_{23} \\
\hat{U}_{32} & \hat{U}_{33}
\end{bmatrix}
\begin{bmatrix}
\hat{I}_{22} & \hat{I}_{23} \\
\hat{I}_{32} & \hat{I}_{33}
\end{bmatrix}^{-1}
= \begin{bmatrix}
\hat{P}_{\text{rad}:22}/\hat{I}_{22}^* & \hat{P}_{\text{rad}:23}/\hat{I}_{23}^* \\
\hat{P}_{\text{rad}:32}/\hat{I}_{32}^* & \hat{P}_{\text{rad}:33}/\hat{I}_{33}^*
\end{bmatrix}
\begin{bmatrix}
\hat{I}_{22} & \hat{I}_{23} \\
\hat{I}_{32} & \hat{I}_{33}
\end{bmatrix}^{-1}. \] (7.6)

The transistor has two ports that we number 2 and 3 (port 1 is the resistor). The currents \(\hat{I}_{22}, \hat{I}_{32}\) are the currents flowing through these two ports due to a current defined for port 2. The currents \(\hat{I}_{32}, \hat{I}_{33}\) are the currents flowing through the same ports due to a current defined for port 3. Because nothing is attached to these components, only a displacement current can flow through their terminals. It must be noted that the port voltages are only defined in the equivalent network and not in the layout. In the layout, only the radiated power and current is defined.

Next, the network impedance \(\hat{Z}_{\text{net}}\), which describes coupling between the components, is determined. The components are placed in the network as depicted in Figure 7.3(b) and the same procedure is repeated. Because this is a three-port network, three different current excitations are required, which equal the current excitations that were applied to determine the impedances of the individual components. The impedance is again calculated from the power that is transferred through the surfaces \(S_1 \cdots S_3\). This power consists of the emitted (and dissipated) power \(\hat{P}_{\text{rad}}\) and the power \(\hat{P}_{\text{int}}\) transferred to the other components. The total impedance \(\hat{Z}_{\text{tot}}\) therefore equals the component impedance and the network impedance in parallel:

\[
\begin{bmatrix}
\hat{Z}_{\text{tot}:11} & \hat{Z}_{\text{tot}:12} & \hat{Z}_{\text{tot}:13} \\
\hat{Z}_{\text{tot}:21} & \hat{Z}_{\text{tot}:22} & \hat{Z}_{\text{tot}:23} \\
\hat{Z}_{\text{tot}:31} & \hat{Z}_{\text{tot}:32} & \hat{Z}_{\text{tot}:33}
\end{bmatrix}
= \begin{bmatrix}
\hat{P}_{\text{11}}/\hat{I}_{11}^* & \hat{P}_{\text{12}}/\hat{I}_{12}^* & \hat{P}_{\text{13}}/\hat{I}_{13}^* \\
\hat{P}_{\text{21}}/\hat{I}_{21}^* & \hat{P}_{\text{22}}/\hat{I}_{22}^* & \hat{P}_{\text{23}}/\hat{I}_{23}^* \\
\hat{P}_{\text{31}}/\hat{I}_{31}^* & \hat{P}_{\text{32}}/\hat{I}_{32}^* & \hat{P}_{\text{33}}/\hat{I}_{33}^*
\end{bmatrix}
\begin{bmatrix}
\hat{I}_{11} & \hat{I}_{12} & \hat{I}_{13} \\
\hat{I}_{21} & \hat{I}_{22} & \hat{I}_{23} \\
\hat{I}_{31} & \hat{I}_{32} & \hat{I}_{33}
\end{bmatrix}^{-1}. \] (7.7)

The network impedance that describes the coupling between these components equals:

\[
\begin{bmatrix}
\hat{Z}_{\text{net}:11} & \hat{Z}_{\text{net}:12} & \hat{Z}_{\text{net}:13} \\
\hat{Z}_{\text{net}:21} & \hat{Z}_{\text{net}:22} & \hat{Z}_{\text{net}:23} \\
\hat{Z}_{\text{net}:31} & \hat{Z}_{\text{net}:32} & \hat{Z}_{\text{net}:33}
\end{bmatrix}
= \begin{bmatrix}
\hat{Z}_{\text{tot}:11} & \hat{Z}_{\text{tot}:12} & \hat{Z}_{\text{tot}:13} \\
\hat{Z}_{\text{tot}:21} & \hat{Z}_{\text{tot}:22} & \hat{Z}_{\text{tot}:23} \\
\hat{Z}_{\text{tot}:31} & \hat{Z}_{\text{tot}:32} & \hat{Z}_{\text{tot}:33}
\end{bmatrix}^{-1}
- \begin{bmatrix}
\hat{Z}_{C:11} & 0 & 0 \\
0 & \hat{Z}_{C:22} & \hat{Z}_{C:23} \\
0 & \hat{Z}_{C:32} & \hat{Z}_{C:33}
\end{bmatrix}^{-1}. \] (7.8)
The resulting equivalent circuit is depicted in Figure 7.4. If the interaction is only confined between the component’s terminals, then the terminals of the ports in the equivalent circuit equal the intersections of the component terminals and the surfaces $S_1 \cdots S_3$. However, when the non-galvanic interaction is included, the terminals correspond to the complete surface $S$, because the power transferred through these surfaces equals the power that is transferred through the ports in the equivalent circuit.

It must be noted that there is a small but fundamental difference between our and the classical definition of the potential difference between the terminals of a port. The electrostatic’s definition of the electric potential difference between two points defines it as the work that is performed to move a unit point charge between the two points, as can be found in any textbook on physics. We created a dynamic extention of this definition, where we again probe the performed work (radiated power) for a unit current flowing through a component. However, this time the current consists of conduction as well as displacement current. Because the power equals the integral of Poynting’s vector over the surface $S$, it can be considered as a weighted average of the tangential electric field, where the tangential magnetic field (which is related to the current flowing through the component by Ampere’s law) acts as a weight function. Dividing this power by the total current, normalizes the current to one. Our definition and the electrostatic definition become equal when the displacement current vanishes and the component and surface $S$ that encloses it become infinitely thin, so that a line equal to the trajectory of the unit point charge of the electrostatic definition remains. The advantage of our method over the existing methods is that the energy exchange in the equivalent circuit equals that in the physical layout, so that the energy conservation law is always obeyed. This definition is limited to layouts where the port conditions for the current flowing through a port of a component are met.

The method of using power transfer calculations for circuit extraction has been successfully applied to transmission lines by Marks [9] and Fache [10]. Thus the energy transfer can be applied to unite electromagnetic, microwave and circuit theory.

The Dependence of Interaction on Electrical Size

Often it is assumed that the EM interaction between a component and the network it is part of is confined to the terminals of the port during impedance calculation by most commercial software (e.g., HFSS). This is a good approximation when the component is electrically small. To motivate this, this section shows that radiation vanishes when the distance between the terminals of a component is electrically small. From
the reciprocity theorem [11] (page 824, formula 28.4-6), it follows that the reception (and thereby the total interaction outside of a terminal pair) must vanish as well.

Let the two conductors depicted in Figure 7.5 form a part of the terminals at the port of a component. The smaller the electrical distance \( |d| \) between these wires, the less they radiate. This can be proven with the help of the electric current vector potential \( \Phi^J(x) \). The electromagnetic field quantities can be expressed as a linear function of this vector potential [11] (page 716, formula 25.1-7). In the thin-wire approximation, this current vector potential (see [11] (page 725, formulas 26.3-1 to 26.3-6)) is approximated by a line integral over the center of the conductors:

\[
\Phi^J_r(x) \approx \int_{x \in D_c} I_r(x') \frac{\exp(j2\pi \frac{|x-x'|}{\lambda})}{4\pi|x-x'|} dx,
\]

where \( \lambda \) is the wavelength and \( D_c \) the domain of the conductors. As this equation shows, the electric current potential is a wave emerging from the two conductors. The wave fronts emerge as circles around the two conductors. Note that in Figure 7.5, the current \( I^+(x_1, -0.5|d|, 0) = -I^-(x_1, 0.5|d|, 0) \), so these waves are in opposite phase. Only when \( |d| \ll \lambda \), these two waves almost fully cancel each other and (7.9) can be approximated by

\[
\Phi^J_r(x) \approx \int_{x \in D_{c,l}} I_r(x') \frac{\exp(j2\pi \frac{|x-x'|}{\lambda})}{4|\lambda||x-x'|} \left( \frac{j2\pi d_r x_r}{\lambda|x-x'|} + \frac{d_r x_r}{|x-x'|^2} \right) dx.
\]

Because \( \Phi^J_r(x) \) vanishes when \( |d| \to 0 \), the smaller \( |d| \), the less radiation, and more the EM energy exchange is confined between the conductors. Not all connections to the port of a component can be represented by two conductors in parallel, like we did here. However, components are always part of a current loop, where the opposing sides of the loop can be given this representation. Thus, only for any electrically small configuration (i.e., small \( \frac{|d|}{\lambda} \)) the classical current-voltage relation be applied.

### 7.2 Calculating the Extracted Circuit Parameters

The previous section outlined the procedure for calculation of a lumped element circuit description based on the EM energy within the physical layout. To implement this procedure, a mathematical formulation must be determined that is discretized...
Calculating the Extracted Circuit Parameters

and solved numerically by a computer algorithm. This section derives an integral formulation of this procedure, with the help of Green’s function theory. The numerical implementation is treated in Section 7.3. For electrically small circuits, a quasi-static approximation is applied, which was already treated in Sections 5.3.1 and 5.4.1. Numerical implementations of these procedures can be found in the literature, for example in [12, 4]. We will only treat the extraction of electrically large physical layouts.

Two types of electrically large layouts are distinguished: those that are electrically large in one dimension (e.g., long cables), and those that are electrically large in two or more dimensions. The one dimensional electrically large layout is represented by a transmission line description. For two- or three-dimensional electrically large layouts, a port representation is applied.

### 7.2.1 Calculation of Transmission-Line Parameters of an Electrically Long Layout

For an electrically long layout, the three-dimensional space is divided in two parts: the length axis, and a two-dimensional cross-section perpendicular to this axis, as illustrated in Figure 7.6. Within this cross-section, quasi-static approximation is then applied so that the signal propagation can be represented by traveling current and voltage waves. It is assumed that signal energy propagates through this cross-section as in a transmission line, where the layout is uniform along the length axis. When the medium is homogeneous (e.g., coaxial cables and striplines) the mode is TEM or quasi TEM, so that the transmission line can be described by an RLCG model. For non-homogeneous lines like microstrips and slotlines, however, two or more modes propagate simultaneously, and transmission-line parameters are frequency dependent (dispersion). We do not treat the extraction of these parameters in this thesis. More information can be found in the following books: [13, 14].

![Figure 7.6: Modeling of an one dimensional electrically large layout.](image)

### 7.2.2 Calculation of the Port Model Parameters of a Multi-Dimensional Electrically Large Layout

When a layout is electrically large in two or more dimensions, a port representation is applied, as described in Section 3.2.3 and 7.1.2. The parameters of this port model are derived from the EM energy exchange between the components and their associated interconnect as explained in Section 7.1.3. Two different classes of simulation methods may be used to determine the solutions of Maxwell’s equations in point simulations and those based on integral equations derived with Green’s theory. The first method...
can in principle be applied to any medium and geometry. It is implemented with the help of finite difference [15], finite integral [16], or finite element methods [5, 17]. A drawback of these methods is that the complete 3D space for simulation must be discretized and stored in memory. Due to computer memory limitations and the accumulation of numerical errors, the physical size that can be handled by these methods is limited. For larger-scale systems, simulation based on integral equations is preferred [18, 19, 20, 2]. The advantage are that only the discretized space occupied by the current carrying conductors are stored in memory, and the algorithm suffers less from the accumulation of numerical errors. However, it can only be applied to homogenous or layered media, because for other media the Green’s functions cannot be determined. Because of its efficiency and ability to handle larger systems, we use this integral method.

We apply Huygens’ principle [21, 22] to derive the required mathematical procedure. As explained in Section 7.1.3, the impedance of the components and the network are determined from a number of field simulations that calculate the power radiated by the components due to a predefined current flowing through one of the components. Assume that the complete system is held in an arbitrarily large closed domain \(D\), as depicted in Figure 7.7. The domain of the current-carrying conductors and components is denoted by \(D_c\), with surface \(\partial D_c\). The domain of the component with the predefined current (i.e., the excitation source) is excluded from \(D_c\) and is denoted by a separate domain \(D_s\), with surface \(\partial D_s\). The domain outside of the interconnect and components is denoted by \(D' = D \setminus D_c \cup D_s\). The unit vector \(\nu\) is perpendicular to all of the surfaces and directed inwards to domain \(D'\). The surface \((S\) in Figure 7.3(b)) through which the radiated power is calculated is chosen to be the surface of the components and \(\partial D_s\) of the component that carries the excitation current. The closed surface \(\partial D_c\), divides the space in a part \(D_c\) that contains the conductors and almost all components, and a part that consist of free space and the component with a predefined excitation current. The field radiated by the component with the excitation current is known, so the currents flowing through the conductors and other components have to be determined from the EM boundary conditions applied to surface \(\partial D_c\). To derive the required expression, we apply Lorentz reciprocity theorem to domain \(D'\), assuming that all the media in domain \(D'\) are linear, isotropic.
Calculating the Extracted Circuit Parameters

and equal in two reciprocal states $A$ and $B$ as defined below (see De Hoop [11] (pages 870-878)):

\[
\int_{x \in \partial D \cup \partial D_s} \varepsilon_{n,m,k}(\hat{E}_m^A \hat{H}_k^B - \hat{H}_m^A \hat{E}_k^B)\nu_n ds = \\
\int_{x \in D'} \hat{J}_n^A \hat{E}_n^B - \hat{J}_m^B \hat{E}_m^A - \hat{K}_r^A \hat{H}_r^B + \hat{K}_u^B \hat{H}_u^A dv, \tag{7.11}
\]

where the vectors $\hat{H}$ and $\hat{E}$ are the magnetic and electric field components and $\hat{J}$ and $\hat{K}$ are the electric and magnetic current densities. The indices $n, m, k, r, u$ are the tensor indices that each range from 1 to 3 for the three spatial dimensions. The states $A$ and $B$ are chosen such that we arrive at an expression for the electric field in $D'$ as function of the fields at the boundary of the conductors. They are:

**State A:** The actual state with the conductors, and components present (see Figure 7.8(a)).

**State B:** A computational state in which everything (e.g. the conductors and all components) has been removed. In this state, only an electrical point source is applied to domain $D'$ (see Figure 7.8(b)).

\[\text{(a) State A: The actual configuration.} \quad \text{(b) State B: Conductors and components replaced by an electric point source.}\]

Figure 7.8: The two reciprocal states of the physical layout that are applied to the Lorentz reciprocity theorem.

With these choices, the reciprocity Equation (7.11) reduces to:

\[
\hat{E}_r^A(x)\chi(x) = \int_{x' \in \partial D \cup \partial D_s} -[\varepsilon_{n,m,k} \nu_m \hat{E}_k^A(x')] \hat{G}_{r,n}^{EK:B}(x, x') \\
+ [\varepsilon_{n,m,k} \nu_m \hat{H}_k^A(x')] \hat{G}_{r,n}^{EJ:B}(x, x') ds, \tag{7.12}
\]

where $\hat{G}_{r,n}^{EK:B}(x, x')$ and $\hat{G}_{r,n}^{EJ:B}(x, x')$ are Green’s tensors of the electrical field in state $B$ for magnetic and electric currents, respectively. These tensors equal the electric field, due to an electric and magnetic point source in state $B$. Note that all conductors have been removed in state $B$, and hence these Green’s tensors are determined for an
interconnect free layout. The function \( \chi(x) \) is defined by:

\[
\chi(x) = \begin{cases} 
1 & x \in D' \\
\frac{1}{2} & x \in \partial D_c \cup \partial D_s \\
0 & x \in D_c \cup D_s 
\end{cases}
\] (7.13)

Because of the high contrast between free space and the conductors, the Leontovich boundary condition \([23, 24]\) is applied to the boundary \( \partial D_c \):

\[
\epsilon_p q r \nu q \hat{E}_r(x) \approx \hat{Z}_c \epsilon_p q r \nu q \epsilon r m n \nu m \hat{H}_m(x), x \in \partial D_c,
\] (7.14)

where \( \hat{Z}_c \) is the wave impedance of the conductor in domain \( D_c \). This impedance is given by

\[
\hat{Z}_c = \sqrt{j \omega \mu_c (\sigma_c + j \omega \epsilon_c)^{-1}},
\]

where \( \mu_c, \epsilon_c \), and \( \sigma_c \) are the permeability, permittivity, and conductivity of the conductor, respectively.

To derive the final integral equation, the following surface currents are defined:

\[
\partial \hat{J}^A_n(x) = \epsilon n m k \nu m \hat{H}^A_k(x), x \in D_c \cup D_s
\] (7.15)

\[
\partial \hat{K}^A_n(x) = \epsilon n m k \nu m \hat{E}^A_k(x), x \in D_c \cup D_s.
\] (7.16)

As can be seen from (7.12), \( \partial \hat{J}^A_n(x) \) and \( \partial \hat{K}^A_n(x) \) act like magnetic and electric surface currents. Moreover, from Ampere’s law it follows that the integral of the electric surface current \( \partial \hat{J}^A_n(x) \) around a conductor equals the total current through this conductor, as illustrated in Figure 7.9. With these choices, the total integral equation becomes:

\[
\epsilon p q r
\int_{x' \in \partial D_c} \left[ \partial \hat{J}^A_n(x') \hat{G}^{EJ:B}_{r,n}(x, x') + \partial \hat{K}^A_n(x') \hat{G}^{EK:B}_{r,n}(x, x') \right] ds
- Z_c \partial \hat{J}^A_n(x) \approx -\epsilon p q r \hat{E}_r(x).
\] (7.17)

The electric field \( \hat{E}_r(x) \) is the field generated by the source, which follows from

\[
\begin{split}
\end{split}
\]

Figure 7.9: Surface current around a conductor or component.

substitution of (7.15) and (7.16) in (7.12):

\[
\hat{E}_r^s(x) = \int_{x' \in \partial D_s} \left[ \partial \hat{J}^A_n(x') \hat{G}^{EJ:B}_{r,n}(x, x') + \partial \hat{K}^A_n(x') \hat{G}^{EK:B}_{r,n}(x, x') \right] ds.
\] (7.18)

Equation (7.17) is the integral equation which is solved for the induced surface current \( \partial \hat{J}^A_n(x) \). For excitation, two surface currents are available: a magnetic surface current \( \partial \hat{K}^A_n(x') \), which is the tangential electric field, and the magnetic surface current \( \partial \hat{J}^A_n(x) \). The first one is used to simulate a voltage source excitation, the latter for a current source excitation, as illustrated in Figure 7.10(b) and 7.10(a).
Calculating the Extracted Circuit Parameters

\[ J \frac{\partial}{\partial \tau} S \hat{H} \partial (a) \text{ Defining the current through a component.} \]

\[ \frac{\partial}{\partial \nu} L - 0 \cdot 5 L \hat{E} A k \tau k d l = - \int_{-0.5L}^{0.5L} \epsilon_{k,l,n} \partial \hat{K}^A_n \nu_l \tau_k d l, \quad (7.19) \]

where \( L \) is the length of the component, \( \nu \) is the normal on the surface (directed outwards), and \( \tau \) is a tangential unit vector aligned with the electric field. The electric field generated by the source is given by:

\[ \hat{E}_r^s(x) = \int_{x' \in \partial D_s} \left[ \partial J^A_n(x') \hat{G}^{EJ,B}_{r,n}(x,x') + \partial \hat{K}^A_n(x') \hat{G}^{EK,B}_{r,n}(x,x') \right] ds. \quad (7.20) \]

The contribution of the magnetic field (electric surface current \( \partial \hat{J}^A_n(x') \)) to the radiated field must be calculated in simulation. The contribution of the electric field (magnetic surface current \( \partial \hat{K}^A_n(x') \)) to the radiated field can be approximated by an electric current. This equivalence is illustrated in Figure 7.11. The magnetic surface current loop in Figure 7.11(a) defines the voltage across the component in Figure 7.10(b). De Hoop [11] has shown that the field radiated by a small current

\[ \hat{I} = j \omega \mu \hat{K} L |A| \]

\[ (a) \text{ Magnetic surface current.} \quad (b) \text{ Equivalent electric current.} \]

Figure 7.11: Equivalent current source of an magnetic surface current.

Voltage source excitation

Voltage source excitation is commonly used in antenna simulations with MOM (see for example [18]). A voltage source excitation defines a tangential electric field by its associated magnetic surface current (7.16) as shown in Figure 7.10(b). The voltage defined by this source is found by integrating the electric field over the component:

\[ \hat{U} = - \int_{-0.5L}^{0.5L} \hat{E}^A_k \tau_k d l = - \int_{-0.5L}^{0.5L} \epsilon_{k,l,n} \partial \hat{K}^A_n \nu_l \tau_k d l, \quad (7.19) \]

The contribution of the magnetic field (electric surface current \( \partial \hat{J}^A_n(x') \)) to the radiated field must be calculated in simulation. The contribution of the electric field (magnetic surface current \( \partial \hat{K}^A_n(x') \)) to the radiated field can be approximated by an electric current. This equivalence is illustrated in Figure 7.11. The magnetic surface current loop in Figure 7.11(a) defines the voltage across the component in Figure 7.10(b). De Hoop [11] has shown that the field radiated by a small current

\[ \hat{I} = j \omega \mu \hat{K} L |A| \]

\[ (a) \text{ Magnetic surface current.} \quad (b) \text{ Equivalent electric current.} \]

Figure 7.11: Equivalent current source of an magnetic surface current.

loop equals that of a magnetic dipole. In exactly the same manner it can be shown that the field radiated by a small magnetic surface current loop equals that of the current \( \hat{I} = j \omega \mu \hat{K} L |A| \), as depicted in Figure 7.11(b). This current is aligned with
the vectorial area $A$ of the loop and proportional to the volume $|L A|$ of the component. This current can be considered a displacement current through the component. However, the permittivity $\varepsilon$ is the permittivity of the domain (air) outside of the component. For most applications, this current is therefore much smaller than the currents through the component. For this reason the contribution of the tangential electric field can often be ignored.

Current Source Excitation

To simulate a current source excitation, a boundary condition is chosen that defines the surface current $\partial J_n^A(x)$ as depicted in Figure 7.10(a). The source current $I_s$ equals the integral of this surface current over a closed path around the source:

$$I_s = \oint_{x \in s} \partial J_n(x)n(x) \, dl,$$

where $n(x)$ is the tangential unit vector aligned with the direction of the current.

$$\hat{E}_r^s(x) = \int_{x' \in \partial D_s} [\partial J_n(x')\hat{G}_{r,n}^{EB}(x,x') + \partial K_n(x')\hat{G}_{r,n}^{EK}(x,x')] \, ds$$

The magnetic current, which represents the electric field, should in principle be solved from the simulation. As illustrated in Figure 7.11, the contribution of this magnetic current to the radiated fields equals an electric current that for most applications is much smaller than the current through the component. Therefore its contribution can often be ignored.

Hence, the field radiated by a component with a predefined current (current source) is almost independent of the system response and therefore known in advance. However, the field radiated by a component with a predefined voltage (voltage source) is mainly determined by the current flowing through it and therefore has to be determined from the simulation.

Inclusion of the Component Geometry in the Excitation Source

To be able to determine the EM interaction between a component and the network surrounding it, we need to give the excitation source the same geometry as the component. However, this requires a complex three-dimensional simulation based on the geometrical information for each component. We use an approximation only representing the most important geometrical aspects.

Voltage source excitation is the method applied most often for impedance calculation, as described in [18, 2, 8, 25]. However, the radiated field is determined by the current through the source, which must be solved by the simulator. Therefore, the complete geometry of the component must be simulated as well. However, when the component is electrically small and the current flowing through the component is defined (current excitation) by a boundary condition of the tangential magnetic field, the radiated field is almost independent of the system response, as explained above. Consequently, the field radiated by the current-carrying component needs to be determined, but the geometry of the component itself does not need to be included in the simulation. This strongly simplifies the simulation, as we may a current...
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source excitation. To simplify this calculation even further, we identify the solenoidal current component and approximate it by a magnetic current source $\hat{K}$ as depicted in Figure 7.12. In this figure, $A$ is the vectorial area of the current loop, $I$ is the electric current, and $K$ is the equivalent magnetic current source of the loop. With this approximation for example, the field from a coil can be described as the sum of the field from a magnetic and an electric current source, as shown by Figure 7.13. In this figure, the magnetic current is $K = NIA$, where $N$ is the number of turns of the coil. Figure 7.14 shows the simplified source representation of a component lifted a bit above a printed circuit board (PCB). The current flow is approximated by a number of adjacent current loops. Because the oppositely directed currents in adjacent branches of neighboring loops cancel each other, the resulting net current flows above the PCB surface. The fields generated by these loops are approximated by those from a magnetic current source, so that the resulting model has an electric current in the plane of the interconnect, with magnetic current sources on top of it, as shown in Figure 7.14(c).

Figure 7.12: Solenoid current approximated by a magnetic current.

Figure 7.13: Component modeling with current sources.

Figure 7.14: Modeling a current-carrying component with the help of electric and magnetic current sources.
Impedance Extraction

As explained in Section 7.1.3, impedance extraction consists of two steps: calculation of the component impedance in free space, and then calculation of the network impedance. Both are determined from the power that is radiated by the component carrying a predefined current. This power is determined by integrating Poynting’s vector $\hat{S}$ over the surface $\partial D_s$ of the component as shown in Figure 7.15. The complex power radiated by this component is given by:

$$\hat{P} = \int_{x \in \partial D_s} \epsilon_{n,m,k} \nu_n \hat{E}_m \hat{H}_n^* ds.$$  \hspace{1cm} (7.23)

With the definition of the surface current (7.15), this power can also be written as:

$$\hat{P} = -\int_{x \in \partial D_s} \partial \hat{J}_m^* \hat{E}_m ds.$$  \hspace{1cm} (7.24)

It should be noted that for static fields, this integral is equal to the current times voltage. This expression is especially useful when current source excitation is applied, where $\partial \hat{J}^*$ is defined by the excitation or calculated from simulation, just like the electric field. When voltage source excitation is applied, a magnetic current $\partial \hat{K}$ is given by the excitation and the magnetic field follows from the simulation. For this type of excitation, the power radiated by the component (7.23) is given by

$$\hat{P} = -\int_{x \in \partial D_s} \hat{H}_m^* \partial \hat{K}_m ds.$$  \hspace{1cm} (7.25)

The radiated power and the current through the component are used to calculate the impedance of the component and the network as explained in Section 7.1.3.

7.2.3 Calculation of the Parasitic Emission

One of the important EMC parameters is the emission of a system, which is limited by national regulations. This section describes two methods to determine this radiation: direct calculation of the radiated field with the help of an EM simulation, and estimation of the radiated field from the radiated power with the help of the
extracted radiation resistance. The first method is the most accurate, but it makes it
difficult to determine the contribution of each part of a circuit to the emission. The
second method only gives an estimate of the far-field emission, but the extracted ra-
diation resistances enable us to determine the contribution of each circuit part. The
first method is best suited for verification of a final layout. The latter gives more
insight in the causes of parasitic emission and is therefore better suited for analysis
and design.

**Accurate Calculation of the Emission**

To determine the total emission from a circuit, we apply the source-type integral
equation [11] (pages 870-878), which describes the radiated fields as a function of
the circuit currents. In a proper circuit design, parasitic EM coupling and emission may
not significantly effect its functioning. The circuit currents can be readily obtained
from a circuit simulation. The radiated electric field is given by:

\[
\hat{E}_r(x) = \int_{x' \in D_c} \hat{J}_n(x') \hat{G}^{E,I}_{r,n}(x, x') dv,
\]  

(7.26)

where \(\hat{J}_n(x')\) is the current density through the conductors, and \(\hat{G}^{E,I}_{r,n}(x, x')\) is
Green’s tensor of the electric field due to electric currents. Because the cross-section
of a conductor is very small compared to the distance at which the field is observed,
we can approximate (7.26) by:

\[
\hat{E}_r(x) \approx \int_{x' \in D_c} \hat{I}_n(x') \hat{G}^{E,I}_{r,n}(x, x') dl,
\]  

(7.27)

where \(\hat{I}_n(x')\) is the current through the conductors. A similar expression can be
obtained for the magnetic field, where Green’s tensor of the electric field is replaced
by that for the magnetic field. For homogeneous and layered media like printed circuit
boards, this Green’s tensor is known (e.g. see Kong [26]).

**Approximated Field, Based on the Radiation Resistance**

The EM field emitted by a radiating circuit is decomposed into three components:
the near, intermediate and far field. The circuit stores and retrieves energy to and
from the near and intermediate field components, which in an equivalent circuit is
represented by capacitances and (mutual) inductances. These parts do not contribute
to the real part of Poynting’s vector so they do not contribute to radiation losses.
Poynting’s vector of the far-field component is real valued, and hence this component
is responsible for the radiation losses. At a short distance from the circuit, the near-
and intermediate-field components are most dominant, but they rapidly decay with
distance, so that at a larger distance, only the far field remains. In antenna theory [25],
the boundary \(d_n\) between the near-field and far-field region is given by:

\[
d_n = \frac{2L^2}{\lambda},
\]  

(7.28)

where \(L\) is the largest dimension of the antenna, and \(\lambda\) is the wavelength. Most EMC
regulations prescribe the radiation limits for a relative large distance from an appliance,
so the far field is often the most important component. Because the near and
intermediate fields do not contribute to the radiation losses, the radiation resistance is only related to the far field. A first-order approximation of the far fields as a function of the radiation resistance is given by (7.2), (7.3) and (7.4). This approximation assumes that the antenna has the directivity of an optimized loop or dipole antenna. Therefore, the parasitic antennas of most layouts will emit a weaker field (at most 30%).

The radiation resistance is extracted from the network impedance found in Section 7.2.2. To separate it from ohmic losses, we set the ohmic losses in (7.17) to zero, so that the real part of the extracted impedance matrix becomes approximately equal to the radiation resistance. This implies that the conductivity \( \sigma \) of the conductors becomes infinitely large, \( \sigma \rightarrow \infty \), so that the wave impedance of the conductor \( Z_c \) in (7.17) vanishes. This reduced equation is used to determine the radiation resistance.

### 7.2.4 Calculation of the Parasitic Reception

The last EMC parameters that must be determined are the signals received from some external unknown source (for example a radio transmitter). These received signals are described by a voltage vector that represents the induced voltages as sources in series with the terminals of the interconnect as explained in Section 7.1.2. This description follows from the weak coupling approximation as described in Section 5.2.2.

An expression for these voltages is derived in Appendix D.3. This expression is given by:

\[
\hat{U}_{\text{par},i} \exp(j \omega t) \approx - \int_{x_{\text{in}}}^{x_{\text{out}}} \left( \hat{Z}_c \hat{H}_m^A + \hat{E}_m^A \right) \partial j_{Bi}^{Ri} dA, \tag{7.29}
\]

where \( \partial j_{Bi}^{Ri} \) is the surface current induced in the conductors due the current source of \( \hat{I}_i = \exp(j \omega t) \) applied at port \( i \) of the interconnect. \( \hat{H}_m^A \) and \( \hat{E}_m^A \) are the external magnetic and electric fields that induce the signal, \( \partial D_s \) is the surface of the conductors, and \( \hat{Z}_c \) is the wave impedance of the conductors that vanishes for very good conductors. Hence, for good conductors, the induced voltages at port \( i \) equal the integral of the inner product of the electric field from the external source and the current through the interconnect caused by a unit current source applied at the port \( i \). Therefore, before the induced voltage can be obtained, first the currents induced in a network due to application of a current source have to be determined. The first step in this calculus was already performed during calculation of the interconnect and component impedances. Hence, only one EM simulation is required to determine both the coupling and reception.

### 7.3 Numerical Implementation of the Circuit Extraction

To solve equation (7.17), we first translate it into a matrix equation that is solved numerically. We apply an implementation of the method of moments, first applied to electromagnetic problems by Harrington [18]. One of the limitations of this method when applied to thin conductors like interconnects and many antennas is that a dense
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matrix is obtained. This makes the method sensitive to numerical errors as explained in [27, 28]. With solution techniques like conjugate gradient and similar iterative methods [29, 30], these matrices can be solved accurately. However a numerical implementation requires us to sample the fields and currents, and approximate them by a sum of weighted base functions. Therefore, an error remains that is not related to limited accuracy of number representation but caused by limitations of the field representation (expansion functions) and aliasing errors [27, 31]. These errors also limit the convergence of the field calculation algorithm. The following paragraphs first briefly explain the applied discretization procedure to derive the required matrix representation and then present a method to improve its accuracy by suppression of aliasing errors.

7.3.1 Discretization of the Integral Equation

The integral Equation (7.17) is of the form:

\[
\hat{E}^i(x) = L(\partial \hat{J}(x'), x), x \in \partial D_c, \quad (7.30)
\]

where \( \hat{E}^i(x) \) is a known field, generated by the applied sources, \( L \) is a linear operator (Green’s integral), and \( \partial \hat{J}(x') \in D_c \) is the surface current (tangential magnetic field) that has to be solved. This equation must be satisfied at every point on the surface of the conductors \( \partial D_c \). To verify Equation (7.30) numerically and with a finite number of points, both sides are weighted with a finite number of weighting functions \( W_n(x) \):

\[
\int_{x \in \partial D_c} \hat{E}^i(x) \cdot W_n(x) ds = \int_{x \in \partial D_c} L(\partial \hat{J}(x'), x) \cdot W_n(x) ds, n \in [1 \ldots N], \quad (7.31)
\]

This is a weakened form of Equation (7.30), and therefore its accuracy is limited by the choice and number of weighting functions. It must be noted that this is an observation problem, similar to the sampling of a signal. With a finite number of points (samples), two functions are observed and compared. Therefore, the Nyquist sampling theorem applies to this problem as well, except that this is a sampling in the spatial rather than the time domain.

The fields and currents are also represented by a finite number of samples. These are approximated by a summation of weighted basis functions:

\[
\hat{E}^i(x) \approx \hat{e}^i_m \Psi_m(x), x \in \partial D_c \quad (7.32)
\]

\[
\partial \hat{J}(x) \approx \hat{j}_m \Psi_m(x), x \in \partial D_c \quad (7.33)
\]

Substitution of these approximations in (7.31) leads to the final discretized version of (7.30):

\[
\hat{e}^i_m \int_{x \in \partial D_c} \Psi_m(x) \cdot W_n(x) ds = \hat{j}_m \int_{x \in \partial D_c} L[\Psi_m(x')], x \cdot W_n(x) ds, n \in [1 \ldots N], m \in [1 \ldots M]. \quad (7.34)
\]

In the Galerkin method, the weighting functions are equal to the expansion functions \( \Psi_m(x) = W_n(x) \). Because the base functions are chosen beforehand, this equation
is rewritten into the required matrix form as follows:

\[ \hat{E}_n^i = \hat{L}_{n,m} \hat{j}_m^i, \quad (7.35) \]

where

\[ \hat{E}_n^i = \hat{e}_m^i \int_{x \in \partial D_c} \Psi_m(x) \cdot W_n(x) \, ds \quad (7.36) \]

\[ \hat{L}_{n,m} = \int_{x \in \partial D_c} L(\Psi_m(x'), x) \cdot W_n(x) \, ds \quad (7.37) \]

These are the matrix equations that are solved numerically. It must be noted that they can only be solved uniquely when the number of weighting functions \( N \) is equal to or larger than the number of expansion functions \( M \). We use Galerkin’s method, which means \( M = N \) and the weight functions equal the expansion functions.

### 7.3.2 Suppression of Aliasing Errors

Discretization of the fields as done in (7.32) implies that the fields are sampled. The domain that is sampled depends on the expansion function applied. For example if pulse-shaped expansion functions are used, each weight factor represents a particular spatial position, so that the sampling is in the spatial domain. When, however, spatial sine and cosine expansion functions are used, each weight represents a different spatial frequency so that the (spatial) frequency domain is sampled. In either case, the sampling causes aliasing errors when Nyquist’s sampling criterion is not met. A spatial anti-aliasing filter is therefore required before the field can be sampled [32]. We developed an optimized spatial filter that is adapted to the grid spacing for optimal accuracy. This method is based on the moving average filter technique that is obtained by weakening of the Green’s integration kernel (see Zwamborn and Van der Berg [33]) and is treated in Appendix H.

To illustrate the differences in results between an integral equation solved with aliasing suppression compared to one solved with almost no aliasing suppression, we have calculated the induced current on a flat square metal plate. The current is induced by a plane wave of \( 1 \text{Vm}^{-1} \), whose Poynting vector is normal to the surface of the plate. The length of the plate equals one wavelength. Figures 7.16(a) and 7.16(b) show the surface currents calculated without anti-aliasing suppression, while the Figures 7.17(a) and 7.17(b) are calculated with sinc-shaped spatial anti-aliasing is treated in Appendix H.

The differences between the two results are caused by aliasing of the numerical noise and rounding off errors, due to the singularity of Green’s function. It must be noted that in this case, the incident electric field is a plane wave and does not need any filtering.

To suppress aliasing errors during simulation, spatial filters are required at two positions of the calculation procedure. The weight procedure (Equation (7.31)) requires an anti-aliasing filter, because it uses a finite number of samples to compare two fields. The expansion procedure (Equations (7.32) and (7.33)) also requires such a spatial filter, because it uses a finite number of samples to represent the fields. According to Nyquist’s criterion, at least two samples per wavelength are required of the highest spatial frequency component present in the sampled field distribution.
Figure 7.16: The surface currents on a flat squared metal plate induced due to a plane wave, calculated without aliasing suppression.

Figure 7.17: The induced surface currents on a flat squared metal plate induced due to a plane wave, calculated with aliasing suppression.
spatial anti-aliasing filter therefore needs to be adapted to the grid spacing, such that its bandwidth is at least half the spatial sampling frequency (i.e., grid spacing). Most commercial simulation software (e.g., HFSS) apply an implicit spatial anti-aliasing filter during simulation. These tools approximate the currents by surface patches, which average the field over each surface patch, so that a moving average anti-aliasing filter is obtained. A drawback of this method is that the relation between the grid and the required filtering is unclear, so that suppression of aliasing errors is not always guaranteed. A dedicated anti-aliasing filter as treated in Appendix H prevents the chance of aliasing errors.

7.4 Example of a Circuit Extraction for a Loop Antenna

This section calculates an equivalent circuit model for a loop antenna. It demonstrates the influence of the component geometry on the extracted equivalent circuit. It shows that the non-galvanic EM interaction (i.e., via emission and reception) between the component and the layout can have a significant influence on the measured impedance of a network [34]. We have not been able to compare our results with those from NEC and Momentum of Agilent because of convergency problems with these simulators. However, a comparison with measurements demonstrates the accuracy of our method.

7.4.1 Antenna Impedance Extraction for Different Component Geometries

The impedance of the microstrip loop antenna without ground plane displayed in Figure 7.18 is determined in this section. The complete configuration is held within an arbitrarily large closed domain, \( D \). The domain of the microstrip is denoted by \( D_c \) with surface \( \partial D_c \). The domain of the source is denoted by \( D_s \) with surface \( \partial D_s \). The domain outside the microstrip is denoted by \( D' = D \setminus (D_c \cup D_s) \). The normal \( \nu \) on the surfaces \( \partial D_s \) and \( \partial D_c \) is directed inwards to domain \( D' \). We assume that this antenna is in free space.

Integral equation (7.12) is solved in the cylindrical coordinate system \((\rho, \varphi)\), where \( \rho \) equals the radius measured from the center of the microstrip antenna and \( \varphi \) the angle

![Figure 7.18: Microstrip loop antenna.](image)
Example of a Circuit Extraction of a Loop Antenna

measured from the center of the source domain. The integral equation in cylindrical coordinates is given by

\[-\hat{E}_\rho = \hat{\eta}^{-1} \partial_\rho \hat{B}_\rho - \hat{\zeta} \hat{\Phi}_\rho^J,\]

(7.38)

\[-\hat{E}_\varphi = \hat{\eta}^{-1} \partial_\varphi \hat{B}_\varphi - \hat{\zeta} \hat{\Phi}_\varphi^J,\]

(7.39)

where \(\hat{\eta} = j\omega \varepsilon + \sigma\) and \(\hat{\zeta} = j\omega \mu\) and \(\hat{\Phi}^J\) the current vector potential. The vector function \(\{\hat{B}_\rho, \hat{B}_\varphi\}\) is defined by:

\[\hat{B}_\rho = \rho^{-1} \left[ \partial_\rho (\rho \hat{\Phi}_\rho^J) + \partial_\varphi \hat{\Phi}_\varphi^J \right],\]

(7.40)

\[\hat{B}_\varphi = \rho^{-1} \hat{B}_\rho.\]

(7.41)

The current vector potential \(\{\hat{\Phi}_\rho^J, \hat{\Phi}_\varphi^J\}\) is given by

\[\hat{\Phi}_\rho^J(\rho, \varphi) = \int_{\rho', \varphi' \in \partial D_c} \left[ \hat{G}^\rho_\rho(\rho, \varphi, \rho', \varphi') \partial J_\rho(\rho', \varphi') \right.\]

\[+ \hat{G}^\rho_\varphi(\rho, \varphi, \rho', \varphi') \partial J_\varphi(\rho', \varphi') \left. \right] \rho' d(\rho', \varphi') \]

(7.42)

\[\hat{\Phi}_\varphi^J(\rho, \varphi) = \int_{\rho', \varphi' \in \partial D_c} \left[ \hat{G}^\varphi_\rho(\rho, \varphi, \rho', \varphi') \partial J_\rho(\rho', \varphi') \right.\]

\[+ \hat{G}^\varphi_\varphi(\rho, \varphi, \rho', \varphi') \partial J_\varphi(\rho', \varphi') \left. \right] \rho' d(\rho', \varphi'),\]

(7.43)

where the \(\hat{G}\) functions are the Green's tensors. For a homogeneous medium, these are given by

\[\hat{G}^\rho_\rho = \hat{G}^\varphi_\varphi = \frac{\exp(-\hat{\gamma} d)}{4d} \cos(\varphi - \varphi'),\]

(7.44)

\[\hat{G}^\rho_\varphi = \hat{G}^\varphi_\rho = \frac{\exp(-\hat{\gamma} d)}{4d} \sin(\varphi - \varphi'),\]

(7.45)

where \(\hat{\gamma} = \sqrt{\hat{\eta} \hat{\zeta}}\) is the propagation constant of the medium and \(d = \sqrt{\rho^2 + \rho'^2 - \rho \rho' \cos(\varphi - \varphi')}\) is the distance between the point of observation \((\rho, \varphi)\) and the source \((\rho', \varphi')\).

### 7.4.2 Simulation and Measurement Results

The microstrip antenna impedance is calculated for four different types of sources. Each source represents a different type of antenna load. Figure 7.19 shows the applied sources.

The source in Figure 7.19(a) is a uniform current source, the source in Figure 7.19(b) is a voltage source, which equals a short-circuit with a uniform electrical field defined on the surface of the short. The sources in Figure 7.19(c) and 7.19(d) are both current sources, where the source of Figure 7.19(c) is a uniform current source with an additional solenoid current and the source of Figure 7.19(d) is a thin-line current. The impedance has been calculated for a microstrip loop antenna with a radius of 15 mm and a strip width of 3 mm. The uniform current source and the
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Figure 7.19: The applied sources.

Figure 7.20(b) shows the same current for a voltage source excitation, both for a frequency of 10 GHz. The imaginary and the radial part of the surface currents are both negligible.

A significantly different result was obtained for sources of Figure 7.19(c) and 7.19(d), as is shown in Figure 7.20(b). For the non-uniform source of Figure 7.19(d), the higher impedance can be explained by the different current distribution at the end of the microstrip. Because the current at the microstrip ends is concentrated in the middle of the strip, the effective width is smaller, which decreases the displacement current. Hence, for an accurate impedance calculation, we must include the geometry of the de component.

To verify the accuracy of our method, we calculated the impedance of a similar microstrip loop without ground plane, and compared it to the impedance measured with a network analyzer. The radius of the applied strip was 12 cm and the strip width 7 mm. The microstrip loop was connected to the network analyzer by 50 Ohm microstrip lines. In simulation, this connection is represented by a current source of the same width, which was given a predefined current as boundary condition. The results of the simulation and measurements are compared in Figure 7.22. These graphs show that current excitation with inclusion of the component geometry leads to very accurate results for the radiation resistance in Figure 7.22(a) as well as the reactive part of the impedance in Figure 7.22.

These simulations results show that current source excitation is a very good alternative to the commonly used voltage source excitation. The advantages are that it allows a simplified representation of complicated component geometries like coils. The impedance calculation based on energy transfer corresponds very well to the
Figure 7.20: The calculated impedances.
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Axial surface current (10 GHz)

(a) Current source excitation.

Axial surface current (10 GHz)

(b) Voltage source excitation.

Figure 7.21: Calculated surface currents for current and voltage excitation.
Example of a Circuit Extraction of a Loop Antenna

Figure 7.22: Calculated versus measured loop impedance.
measured impedances. In our first attempts to calculate the impedance, we calculated the electric potential difference between the terminals of the microstrip loop by a line integration of the electric field. For frequencies higher than 4 GHz however, these calculations showed poor correspondence to the measurement results. As soon as we based the impedance measurement on energy transfer, a strong improvement in accuracy was obtained. The advantage is that energy transfer can be calculated at any frequency, while the electric potential is only defined in an electrically small domain. Moreover, the electric field strength can show singularities at the edges of the microstrip due to charge accumulation. These singularities decrease the accuracy of a numerical integration of the electric field due to the finite word length of digital computers. The Poynting vector does not suffer from these singularities, so that the radiated power can be determined more accurately.

The applied simulator has been written from scratch in C++ with the help of Prof. P.M. van der Berg of the Electromagnetic research group of Delft University of Technology. It is based on the work of Zwamborn [20], which we translated into cylindrical coordinates. The accuracy of the method has been increased by application of an improved spatial anti-aliasing filter, which was required to handle the very small grid spacings around the source domain. The simulator contains over 4400 lines of code and currently can only handle loop and rectangular dipole microstrip configurations in free space. For future use, however, the numerical conjugate gradient field solver has been designed independently of the coordinate system, grid spacing and media. It operates on a pure virtual class from which the different coordinate systems and grid spacings are derived. This architecture allows extension of the field solver to handle other physical layouts.

7.5 Conclusions

Because the EM interaction between a component and its associated network is not confined to the terminals, the extracted network parameters must represent the total energy exchange between components. The components and the network therefore do not have a unique port impedance, as they are also determined by the system that “observes” this impedance. Therefore the physical layout of the network as well as the components connected to it, have to be included in the calculation of an equivalent circuit.

The extracted circuit resembles the behavior of the physical layout best, when its parameters are derived from the EM power transfer between the components in stead of the voltage-current relationship measured at their terminals.

For simulation of the EM interaction between a component and its physical surroundings, we can significantly simplify the simulation procedure by using current excitation instead of the commonly applied voltage excitation. If the current flowing through a component is defined instead of the voltage across it, the field it radiates becomes almost independent of the system response. To simplify the inclusion of the component geometry, we approximated the fields radiated by the solenoidal and axial components of the current through the component with the help of a magnetic and an electric current source, respectively. With these approximations, a 3-dimensional geometry can often accurately be simulated using a 2-dimensional simulator.
For numerical EM calculation, spatial sampling of the electromagnetic waves and the electric current is required. This causes aliasing errors reducing the accuracy of the simulator. To solve this problem, a spatial anti-aliasing filter is required. EM simulators apply surface patches for discretization, which act as a moving-average anti-aliasing filter. By weakening of Green’s kernel with a sinc function, however, an almost ideal anti-aliasing filter is obtained. The advantage of this method is an improved stability of the simulator that can be adapted to any discretization. The effectiveness of this method was demonstrated using a loop antenna as an example.
Bibliography


Chapter 8

Conclusions and Future Research

8.1 Conclusions

The currently available design techniques for improving EM compatibility mainly focus on the design of the physical layout. To find an efficient solution however, EM compatibility should be considered during every phase of the design, so that signal coding and circuit solutions are taken into account as well. The order in which the design decisions are taken has to be organized, so that each decision only depends on previously taken decisions. This allows optimization of each individual decision and minimizes the number of design iterations.

In this thesis, techniques are presented to improve compatibility during each design phase. The main contributions of this thesis are:

1. Introduction of information theory in EMC analysis, so that system requirements (i.e., bandwidth, dynamic range and required channel separation) can be determined prior to circuit design.

2. A new technique for extraction of an equivalent circuit from a layout, which is based on the energy exchange between components. To improve the accuracy of the port impedance calculations, the geometry of the components connected to the ports is taken into account as well.

3. Introduction of optimal spatial filtering for suppression of aliasing errors in EM field calculations, based on the method of moments. This technique enables optimal suppression of aliasing errors, adapted to the applied grid spacing.


5. Introduction of signal flow based routing of interconnect as a replacement for the connectivity based routing. This method enables automated routing, while optimizing EM compatibility.
To improve compatibility, one should minimize the reduction of information capacity due to parasitic signals (interference). Known parasitic signals, that are obtained with an estimator, can be compensated (e.g., noise cancellation) so that they only reduce the dynamic range of a system. Unknown parasitic signals reduce the capacity approximately with the effective bit rate of the parasitic signals itself. To minimize this loss of capacity (improve compatibility), one has to optimize the separation between signals in every domain that they are processed and/or transported in. These are the spatial domain (physically separated signal paths), coding domain (time, frequency), and the energetic domain (current, voltage).

The signal coding should be optimized for separation between parasitic and desired signals. When the coding of the parasitic signal is known, the coding of the desired signal should be orthogonalized to that of the parasitic signal. When the coding of the parasitic signal is not known, the optimal coding distributes the signal energy as much as possible over the coding domain (e.g., spread spectrum), so that the chance of a blocked channel due to a parasitic signal is minimized.

The circuit design should minimize the influence of EM interaction and distortion on the EM compatibility. The strongest EM interaction between signal paths is caused by shared conductors, which can be eliminated by a differential implementation. For electrically short paths, the influence of EM coupling is reduced by application of pure current domain or pure voltage domain signals. Voltage domain signals cause the least emission, because the emission from the signal reflected by a voltage detector compensates the emission from the incident signal. Current domain signals offer the highest immunity when the coupling is dominated by inductive coupling, while voltage domain signals offer the highest immunity when capacitive coupling dominates. For electrically long paths, the influence of EM coupling can be reduced by choosing a low line impedance so that the ratio of this line impedance to the mutual impedance between lines is reduced. Matching of the terminating impedances to the line impedance of an electrically long connection is preferred to prevent extra emission due to standing waves.

To prevent loss of separation between signals due to distortion, separation in the signal coding domain should be preserved. Non-switching or non-saturating non-linear operations are therefore preferred over switching or saturating operations. For linear operations, distortion in the time and frequency domains should be prevented. Distortion in the time domain is reduced by minimizing the dependence of the biasing of transistors on the processed signals. This can be achieved with a class-A differential implementation and the use of overall feedback. Distortion in the amplitude domain is reduced with the help of overall feedback and linearization of the open loop transfer (e.g., using a sum of non-linear transfers with transistors). The latter method is especially useful for suppressing detected high frequency interference.

To improve the compatibility of a layout, the unintended EM interaction between signal paths has to be minimized. To enable this minimization during placement and routing, the commonly used net-based routing methods have to be replaced by a signal-path-based method. For optimization of the layout, information about the performance degradation due to EM coupling has to be extracted from the circuit design for each signal path. This information is required to rank the signal paths according to their sensitivity to EM coupling, and to organize the floor plan so that the most sensitive paths have minimal EM coupling. To achieve the best performance,
the most effective measures to reduce EM coupling should be taken first. To reduce difference-mode EM coupling, the most effective measures are: elimination of shared conductors, minimization of overlap between signal paths, application of a shielding plane, decreasing the distance between the two conductors of each signal path, and orthogonalization of the orientation of signal paths. For a planar layout like that of printed circuit boards and integrated circuits, the lowest difference-mode EM coupling and the sensitivity for external fields is obtained by a slotted line implementation of the signal paths. The most effective methods to reduce common-mode coupling are: applying a shielding plane and reducing the effective size of parasitic common-mode antennas, folding of potential dipole antennas, and reducing the enclosed area of potential loop antennas. An efficient method to find potential common-mode parasitic antennas in a layout is to use graph theory. A graph, obtained by drawing all common-mode paths between circuit components, reveals potential parasitic dipoles as graph cuts, and potential loops as graph circuits.

The extracted circuit description of a layout, which is required to analyze and verify the compatibility, is most accurate when it describes the EM power transfer between circuit components. The EM energy exchange between components is often not confined to the conductors connected to them, and therefore the voltages measured between their terminals are not an accurate measure of the transferred EM power. The impedance calculation of the components and the interconnections therefore should be based on the EM power exchange-current relationship instead of on the commonly used voltage-current relationship. The port impedance of a network is not a property of the network only, but is also determined by the physical properties of the component connected to it. Therefore the port impedance that is “observed” by the connected component should be calculated. A comparison of simulation and measurement results in this thesis demonstrates that with impedance calculations based on EM-power exchange, a very accurate equivalent circuit description can be obtained. For an accurate numerical EM-field simulation, the Nyquist sampling theorem must be obeyed in the time domain as well as the spatial domain. The accuracy and numerical stability of an EM field simulator can therefore be improved by applying a spatial anti-aliasing filter. This filter is required to suppress the aliasing errors that are caused by the spatial discretization of the EM fields. In this thesis it is shown that a more accurate algorithm is obtained when the commonly used spatial moving average filter is replaced by a dedicated anti-aliasing filter, adapted to the grid spacing.

8.2 Future Research

The layout techniques currently available are netlist based, which limits their ability to minimize undesired EM interaction. Therefore new (automated) layout techniques have to be developed that are based on the signal flow within a layout. This requires an extension of the circuit description to make the signal flow an input to an automated router. Placement and routing algorithms have to be developed that minimize the coupling between signal paths.

The circuit extraction software currently available is mainly based on microwave and antenna simulation methods, which calculate the port voltages and currents at the ports of a network. This approximation can be accurate for microwave and antenna
applications, but not always for the layout of other electronics. For these situations we have developed a circuit extraction method that is based on the total EM energy exchange between components. A similar method has been developed by others for simulating transmission lines. To enable accurate circuit extraction of every type of layout, these methods have to be merged and extended to develop an accurate general-purpose circuit extraction method based on the EM energy flow between components.

Currently most of the research related to EM compatibility focuses on layout and verification techniques. With the growing use of wireless and high-speed communication equipment, however, the possibilities to shield and isolate systems from high-frequency parasitic signals becomes increasingly limited. The selectivity of antennas is limited, and shielding against transmitters in close proximity is practically not always feasible. Therefore signal coding and signal processing techniques will become more important factors in EM compatibility. More circuit techniques have to be developed to discriminate against parasitic signals and to eliminate unwanted signal detection due to distortion. In addition, new signal codes are required that are less vulnerable to compatibility problems (these could be implemented with today’s powerful signal processors).
Appendix A

Nonlinear Circuit Model of a Junction Diode

The common models that are used for hand calculation of junction diodes, describe the static large signal behavior or dynamic small signal behavior. To calculate the dynamic nonlinear behavior, one has to rely on simulation models. For circuit design the linearized model is preferred, because superposition applies, which simplifies calculations. Nonlinearities, however, can cause compatibility problems like intermodulation of intentional and interfering signals. Therefore a circuit model is required that describes both the dynamic and nonlinear behavior. To help a designer gain insight in the component’s behavior, the model should be simple enough for hand calculation.

The model derived in this appendix, only applies to mild nonlinearities, that can be approximated by the first three terms of a Taylor or Volterra expansion. To derive this model, we apply the methods presented in [1] to the ambipolar transport equation that describes the conduction mechanism of diode. To improve the accuracy for high frequency signals, a third order Volterra approximation is taken around a carrier frequency $\omega_c$. In the following sections we first present a mathematical description of the voltage current transfer of a diode and next derive from this description a small signal nonlinear circuit model.

A.1 A Mathematical Description of the Current-Voltage Transfer of a Junction Diode

In textbooks on semiconductor physics [2, 3], the small signal model of a diode is derived with the help of a first order Taylor approximation of the nonlinear part of the conduction mechanism of a diode around a bias point. To derive a model that describes the dynamic nonlinear behavior, we follow the same procedure, but make no approximation for the nonlinear mechanisms.

For simplicity, we consider only one dimension of the conduction mechanism of a diode with a uniform doping profile in the $P$ and $N$ regions. A cross section of such a diode in thermal equilibrium is depicted in Figure A.1. Because the Fermi energy level of electrons in the $N$ region is higher than in the $P$ region, a depletion layer of
positive charge in the $N$ region and negative charge in the $P$ regions is formed, which causes a potential difference that compensates this energy difference. Due to this charge a voltage potential across the depletion layer arises that ensures a constant Fermi level (thermal equilibrium) through the whole crystal.

The current that flows through a diode due to application of a time varying voltage, is the sum of a diffusion current due to charge that crosses the depletion region, and a current associated with the modulation of the depletion width. We consider both mechanisms separately.

### A.1.1 Diffusion Current

To derive a nonlinear dynamic circuit model for the diffusion current, we describe this conduction mechanism as a cascade of two independent mechanisms: the nonlinear injection mechanism of minority carriers into the $P$ and $N$ region and the linear diffusion mechanism of these carriers within the two regions. The injection process is considered to be instantaneous (not frequency dependent), while the diffusion process has a memory and therefore is frequency dependent. The injected excess minority charge carriers diffuse and recombine in the $P$ and $N$ regions. Figure A.2 shows how the concentration of these excess carriers decreases as they diffuse into both regions. Note that this figure depicts only the excess (e.g. additional) minority charge.

### A.1.2 Depletion Width Modulation

When the voltage across the diode varies, the amount of injected charge varies. Due to the relative slow diffusion and recombination process excess charge is stored in the $N$ and $P$ regions, which due to altering of the forward voltage, changes as indicated by the shaded regions in Figure A.2. This charge storing mechanism results in a
frequency dependent diode impedance. We describe this process as a linear filter that follows the nonlinear injection mechanism.

### A.1.3 Total Diode Current

The total diode current equals the sum of this diffusion current and a current associated with the depletion width modulation. Figure A.3 represents the diode as voltage controlled current source. The diffusion current is represented by a cascade of a non frequency dependent nonlinear block and a frequency dependent linear block. The depletion width modulation is a frequency dependent nonlinear block. The minority

![Mathematical circuit model of a diode.](image)

**Figure A.3:** Mathematical circuit model of a diode.

electron concentration $n_p$ and hole concentration $p_n$ at the edges $X_N$ and $X_P$ (see Figure A.2) of the depletion region respectively equal (see [3]):

$$n_p = n_{p0}(e^{U_f/T} - 1),$$  

(A.1)

$$p_n = p_{n0}(e^{U_f/T} - 1),$$  

(A.2)

where $n_{p0}$ and $p_{n0}$ are the electron and hole concentration in the $P$ and $N$ regions when the applied voltage $U_f$ is zero respectively, and $U_T$ is the thermal voltage.

After crossing the depletion layer this excess minority charge diffuses and recombines in the $P$ and $N$ regions. This process is described by the Ambipolar transport equations for both regions (see [3]):

$$D_n \frac{\partial^2 n_p(x,t)}{\partial x^2} - \frac{1}{\tau_n} n_p(x,t) = \partial_t n_p(x,t),$$  

(A.3)

$$D_p \frac{\partial^2 p_n(x,t)}{\partial x^2} - \frac{1}{\tau_p} p_n(x,t) = \partial_t p_n(x,t),$$  

(A.4)

where $D_n$ and $D_p$ are the diffusion constants of electrons and holes. The time constants $\tau_n$ and $\tau_p$ are the average life time of electrons and holes in the $P$ and $N$ regions respectively. In these equations the electric field in both regions is assumed to be negligible. At the edges $W_P$ and $W_N$ (see Figure A.1), where the external connections are made, the excess concentration are assumed to be zero. Application
of these boundary conditions to (A.3) and (A.4) yields:

\[ \tilde{n}_p(j\omega, x) = n_{p0} \frac{\mathcal{F}\left[\exp\left(\frac{U_f(t)}{U_T}\right) - 1\right] \sinh\left[\frac{\sqrt{1+j\omega\tau_n}}{L_n} (x - W_P - x_P)\right]}{\sinh\left[\frac{\sqrt{1+j\omega\tau_n}}{L_n} (-W_P)\right]}, \quad (A.5) \]

\[ \tilde{p}_n(j\omega, x) = p_{n0} \frac{\mathcal{F}\left[\exp\left(\frac{U_f(t)}{U_T}\right) - 1\right] \sinh\left[\frac{\sqrt{1+j\omega\tau_n}}{L_p} (W_N + x_N - x)\right]}{\sinh\left[\frac{\sqrt{1+j\omega\tau_n}}{L_p} W_N\right]}, \quad (A.6) \]

where \( L_n = \sqrt{D_n \tau_n} \) and \( L_p = \sqrt{D_p \tau_p} \) are the diffusion lengths of electrons and holes, \( j\omega \) the complex frequency in radians-seconds\(^{-1}\) and the operator \( \mathcal{F}[\cdot] \) the Fourier operator. Note that positions \( W_P \) and \( x_P \) are negative in Figure A.1. If we ignore the recombination of electrons and holes in the depletion region, the diode current is given by:

\[ \dot{I}(j\omega) = qAD_n \partial_x n_p(j\omega, x) \bigg|_{x=x_P} - qAD_p \partial_x p_n(j\omega, x) \bigg|_{x=x_N} \]

\[ = qA \mathcal{F}\left[\exp\left(\frac{U_f(t)}{U_T}\right) - 1\right] \{D_n n_{p0} \left[\frac{\sqrt{1+j\omega\tau_n}}{L_n} \coth\left[\frac{\sqrt{1+j\omega\tau_n}}{L_n} (-W_P)\right]\right] +
\]

\[ D_p p_{n0} \left[\frac{\sqrt{1+j\omega\tau_n}}{L_p} \coth\left[\frac{\sqrt{1+j\omega\tau_n}}{L_p} W_N\right]\right]\}, \quad (A.7) \]

where \( A \) is the surface area of a cross-section of the diode. This is a nonlinear dynamic description of the diode current. The commonly used linear small signal model is found by a first order Taylor approximation of the exponential part.

The depletion width modulation causes an additional current, that depends on the stored charge in the depletion region. If we assume that all donor and acceptor atoms are ionized in the depletion region, the amount of space charge on each side of the depletion region equals:

\[ Q(t) = A \sqrt{2q\varepsilon_s [U_{bi} - U_f(t)]} \frac{N_A N_D}{N_A + N_D}, \quad (A.8) \]

where \( N_A \) and \( N_D \) are donor and acceptor concentration, \( \varepsilon_s \) the permittivity of the semiconductor and \( U_{bi} = U_T \ln\left(\frac{N_A N_D}{n_i^2}\right) \) (\( n_i^2 \) is the intrinsic electron concentration), which is called the build in voltage. This charge results in a additional current \( I_c(j\omega) \) given by:

\[ I_c(j\omega) = -\mathcal{F}[\partial_t Q(t)], \quad (A.9) \]

Note that the applied source must add charge to decrease the space charge \( Q(t) \) in the depletion layer, hence the negative sign in (A.9).

This current is dominant for a reversed biased diode \((U_f < 0)\), while the diffusion current is dominant for a forward biased diode \((U_f > 0)\) (see [2]). The current of Equation (A.9) around the transition from forward to reverse cannot be deduced, because Equation (A.9) is not valid for a forward biased diode. When the forward voltage equals the build in voltage, the depletion layer ceases to exist \((Q(t) = 0)\). This causes a singularity for the expression of the current due to depletion width modulation (A.9), which is not true in reality.
Although components in low power circuits are often biased in this region, we could not find any information in literature about what happens around the transition from forward to reverse biasing. We therefore looked at the models of PN junctions in the Gummel-Poon and the more recent Mextram [4, 5] compact bipolar transistor model. Both models use an equal description for the forward and reverse junction. Both models use a first order approximation of (A.9) for a reversed and (A.7) for forward biased diode. Around the transition point, however the Gummel-Poon model simply uses a linear interpolation between both expressions, while the Mextram model allows for a weak singularity. This can result in a complete different impedance for both models around this transition. A closer look, however, shows that this difference does not appear for a standard diode. The singularity can only appear for transistors and transistors used as diode. The cause of this singularity is explained in Appendix B.

In our model, we will simply add both current for a reversed biased diode. The model of a forward biased must ignore the current associated with depletion width modulation. During design we need to determine whether or not this source should be included. The complete mathematical model of the diode in frequency domain is shown in Figure A.4.

![Circuit Diagram](image)

Figure A.4: Complete mathematical circuit model of diode.

This circuit shows that we can view the response of a forward biases diode as a being generated by an nonlinear instantaneous reacting function followed by linear filter. The diode, therefore, will behave as a nonlinear element at any frequency. Even above the frequency a diode is designed for, EM interference due to nonlinear detection can be expected.

### A.2 Derivation of a Circuit Model

To derive an equivalent circuit that simulates the diode behavior described by equations (A.7) and (A.9), an approximation is required that can be represented by circuits elements. We will first derive the well known linearized model and next extend it to a nonlinear model.
A.2.1 First Order Linearized Model

A first order linearized model can be derived by a first order approximation of both the nonlinear and frequency dependent part of the diode. The nonlinear part is linearized around a bias point. The voltage $U_f$ across the diode therefore consists of a bias voltage $U_0$ with an added small signal $u_f$:

$$U_f(t) = U_0 + u_f(t) \quad (A.10)$$

The injected access minority charges (A.1) and (A.2) in a first order Taylor approximation become:

$$n_p(t) = n_{p0} \left[ \exp \left( \frac{U_0}{kT} \right) \exp \left( \frac{u_f(t)}{kT} \right) - 1 \right] \approx n_{p0} \frac{u_f(t)}{kT} + n_{pdc} - n_{p0} \quad (A.11)$$

$$p_n(t) = p_{n0} \left[ \exp \left( \frac{U_0}{kT} \right) \exp \left( \frac{u_f(t)}{kT} \right) - 1 \right] \approx p_{n0} \frac{u_f(t)}{kT} + p_{ndc} - p_{n0} \quad (A.12)$$

A similar approximation can be given for the linear frequency dependent part, by applying a first order approximation around a frequency of zero:

$$\hat{I}(j\omega) \approx I_0 + qA \mathcal{F} \left[ \frac{U_f(t)}{V_T} \right] \left( D_n n_{pdc} \frac{1}{L_n} \coth \left( \frac{W_n}{L_n} \right) + D_p p_{ndc} \frac{1}{L_p} \coth \left( \frac{W_p}{L_p} \right) ight. \left. + j\omega \left\{ \frac{\tau_n D_n n_{pdc}}{L_n} \left[ \coth \left( \frac{W_n}{L_n} \right) + \frac{W_n}{L_n} \sinh \left( \frac{W_n}{L_n} \right)^{-2} \right] \right. \right. \left. \left. + \frac{\tau_p D_p p_{ndc}}{L_p} \left[ \coth \left( \frac{W_p}{L_p} \right) - \frac{W_n}{L_n} \sinh \left( \frac{W_n}{L_n} \right)^{-2} \right] \right\} \right) \right) \quad (A.13)$$

where $I_0$ is the bias current. A first order approximation of the depletion width modulation results in the following additional current:

$$\hat{I}_c(j\omega) \approx \mathcal{F} \left[ \partial_t U_f(t) \right] A \sqrt{\frac{q\varepsilon_s}{2(U_{bi} - U_0)}} \frac{N_A N_D}{N_A + N_D} \quad (A.14)$$

Note that this current is only added when the diode is biased in reverse. This formulation is readily translated into the standard circuit description of a diode, shown in Figure A.5, where we left out the bias current for convenience. The resistance and capacitance in this linearized model are given by equations (A.15) and (A.16).

$$R = \left[ \frac{qA}{U_T} D_n n_{pdc} \frac{1}{L_n} \coth \left( \frac{W_n}{L_n} \right) + \frac{qA}{U_T} D_p p_{ndc} \frac{1}{L_p} \coth \left( \frac{W_p}{L_p} \right) \right]^{-1} \approx \frac{U_T}{I_0} \quad (A.15)$$

Figure A.5: First order small signal model of a diode.
The first order approximation of the current voltage relationship becomes:

\[
C = \frac{qA}{2CT} \left\{ \frac{\tau_n D_n n_{pdc}}{L_n} \left[ \coth\left( \frac{W_p}{L_n} \right) + \frac{W_p}{L_n} \sinh\left( \frac{W_p}{L_n} \right)^{-2} \right] \\
+ \frac{\tau_p D_p p_{pdc}}{L_p} \left[ \coth\left( \frac{W_N}{L_p} \right) - \frac{W_N}{L_p} \sinh\left( \frac{W_N}{L_p} \right)^{-2} \right] \right\} \\
+ A \sqrt{\frac{q\varepsilon_s N_A N_D}{2(U_b - U_0) N_A + N_D}} \tag{A.16}
\]

The last capacitive component on the right hand side of (A.16) is only added when the diode is reversely biased. We could not find much information about the behavior of a diode around the transition between forward and reverse biasing and therefore did some measurements on two standard diodes, which results are shown in Figure A.6. Figure A.6(a) shows the results on a 1N4007 switching diode. This diode is has a transparent package therefore light did have some influence on the conductance of the diode. Figure A.6(b) shows the results on a 1N5408, which is a power diode in a non transparent package. The measurement results show a smooth transition in the impedance for both diodes when going from reverse to forward biasing. The impedance lowers fast around \( U_f = 0 \) due to the diffusion current, which indicates that we can ignore the current due to depletion width modulation around this point.

The model shown in Figure A.5, which is commonly used in analog circuit design, is derived by applying a first order approximation around a frequency of zero rad/sec. However, in case of a high frequency system that handles a signal with a carrier frequency \( \omega_c \), a first order approximation around the carrier frequency is preferred. The first order approximation of the current voltage relationship becomes:

\[
\hat{I}(j\omega) \approx I_0 + qA \mathcal{F} \left[ \frac{U_f(t)}{U_f} \right] \left( D_n n_{pdc} \frac{1}{L_n} \coth\left( \frac{W_p \sqrt{1+j\omega_c \tau_c}}{L_n} \right) \\
+ D_p p_{pdc} \frac{1}{L_p} \coth\left( \frac{W_N \sqrt{1+j\omega_c \tau_c}}{L_p} \right) \\
+ \frac{\tau_n D_n n_{pdc}}{L_n} \left[ \frac{1}{\sqrt{1+j\omega_c \tau_c}} \coth\left( \frac{W_p \sqrt{1+j\omega_c \tau_c}}{L_n} \right) + \frac{W_p}{L_n} \sinh\left( \frac{W_p \sqrt{1+j\omega_c \tau_c}}{L_n} \right)^{-2} \right] \\
+ \frac{\tau_p D_p p_{pdc}}{L_p} \left[ \frac{1}{\sqrt{1+j\omega_c \tau_c}} \coth\left( \frac{W_N \sqrt{1+j\omega_c \tau_c}}{L_p} \right) - \frac{W_N}{L_p} \sinh\left( \frac{W_N \sqrt{1+j\omega_c \tau_c}}{L_p} \right)^{-2} \right] \right) \right]. \tag{A.17}
\]

This description can be translated in a bandpass model as shown in Figure A.7. The constant resistance has become a complex impedance \( \tilde{R} \) in parallel to a complex bandpass capacitance \( \tilde{C} \) and a normal capacitance \( C_c \). We use the tilde \( \tilde{\cdot} \) to indicate that these passband resistor and capacitor play a similar role but are not equal to the resistor and capacitor in the baseband model (Figure A.5). The values of these components are given by:

\[
\tilde{R}(\omega_c) = \frac{4A}{U_f} \left( D_n n_{pdc} \frac{1}{L_n} \coth\left( \frac{W_p \sqrt{1+j\omega_c \tau_c}}{L_n} \right) \\
+ D_p p_{pdc} \frac{1}{L_p} \coth\left( \frac{W_N \sqrt{1+j\omega_c \tau_c}}{L_p} \right) \right), \tag{A.18}
\]
Nonlinear Circuit Model of a Junction Diode

(a) Impedance of a 1N4007.

(b) Impedance of a 1N5408.

Figure A.6: Impedance measurement results of two diodes.
Derivation of a Circuit Model

\[ \tilde{C}(\omega_c) = \frac{qA}{L} \frac{1}{2} \left\{ \frac{\tau_n D_A n_{pdc}}{L_n} \coth \left( \frac{-W_P \sqrt{1+j\omega_c \tau_n}}{L_n} \right) + \frac{W_P}{L_n} \sinh \left( \frac{-W_P \sqrt{1+j\omega_c \tau_n}}{L_n} \right)^{-2} \right\} \]
\[ + \frac{\tau_p D_A p_{pdc}}{L_p} \left\{ \frac{1}{\sqrt{1+j\omega_c \tau_p}} \coth \left( \frac{W_N \sqrt{1+j\omega_c \tau_p}}{L_p} \right) - \frac{W_N}{L_p} \sinh \left( \frac{W_N \sqrt{1+j\omega_c \tau_p}}{L_p} \right)^{-2} \right\}, \]
\[ \text{(A.19)} \]

and

\[ C_C = A \sqrt{\frac{q\varepsilon_s}{2(U_{bi} - U_0)} \frac{N_A N_D}{N_A + N_D}} \]
\[ \text{(A.20)} \]
is the capacitance depletion width modulation. Note that capacitor \( C_C \) is in our model only present when the diode is reverse biased. The admittance of a diode in this bandpass situation is given by

\[ \tilde{Y}_{\text{diode}}(\omega, \omega_c) = \tilde{R}(\omega_c)^{-1} + j(\omega - \omega_c)\tilde{C}(\omega_c) + j\omega C_C. \]
\[ \text{(A.21)} \]

Due to the first order Taylor approximation made to both the non linear and frequency dependent parts, the validity of these models is limited in both amplitude and frequency domain.

A.2.2 Linear Diode Model With Extended Frequency Range

To get an impression of the behavior of the diode over a wider frequency range, a better approximation of the linear part of the current voltage relation ship is required. We will improve in this paragraph the approximation of the baseband model shown in Figure A.5. The model is described by the first order approximation (A.13). This approximation can be improved by adding a few extra terms to the Taylor approxi-
Nonlinear Circuit Model of a Junction Diode

Assuming that both $N$ and $P$ are relative long compared to the diffusion lengths $L_P$ and $L_N$ thus $W_N \gg L_P$, $-W_P \gg L_N$ this rather complex equation can be simplified to:

\[
\dot{I}(j\omega) \approx I_0 + qA F \left[ \frac{U_d(U)}{U_T} \right] \left( D_n n_{pdc} \frac{1}{L_n} + D_p p_{pdc} \frac{1}{L_p} \right) + j\omega \left( \frac{\tau_n D_n n_{pdc}}{L_n} + \frac{\tau_p D_p p_{pdc}}{L_p} \right) \left( \frac{\dot{W}}{W} \right) + j\omega^2 \left( \frac{\tau_n^2 D_n n_{pdc}}{L_n} + \frac{\tau_p^2 D_p p_{pdc}}{L_p} \right)
\]

where we added the fourth term of the Taylor expansion as well. The expression of current due to modulation of the depletion width, given by (A.8), does in our approximation not show any frequency limitations.

A equivalent circuit in standard frequency independent elements that simulate the behavior described by (A.23) and (A.8) does not exist. By introducing a frequency dependent resistor and inductor as shown in Figure A.8, however, this behavior can be simulated. The frequency dependent resistor and inductor in this circuit are given by Figure A.8: Frequency extended small signal circuit model of diode.
Derivation of a Circuit Model

by (A.24) and (A.25).

\[
R(\omega) = 8\omega^{-2} \left[ \frac{\tau^2 D_n p_{dc} n}{L_n} + \frac{\tau^2 D_p p_{dc}}{L_p} \right]^{-1} \tag{A.24}
\]

\[
L(\omega) = 16\omega^{-4} \left[ \frac{\tau^2 D_n p_{dc} n}{L_n} + \frac{\tau^2 D_p p_{dc}}{L_p} \right]^{-1} \tag{A.25}
\]

The small signal model, depicted in Figure A.8 and described by (A.23), show that for higher frequencies the net resistance decreases, while the parallel inductance increases. This implies that the impedance does not decrease with frequency as predicted by a first order R-C network. Note that the inductance of the coil is very high for low frequencies. This description suggest the existence of a resonance frequency which, however, is caused by the truncation of the Taylor series. Equation (A.7) shows that the impedance has no resonance frequency but decreases monotonous with frequency.

A.2.3 Small Signal Nonlinear Model

The model shown in Figure A.8 is a linearized model that still does no account for the nonlinear behavior of the diode. To approximate the nonlinear behavior we need to include more terms of the Taylor expansion of the nonlinear part. These additional terms cannot be modeled by linear impedances. To describe them with the help of a circuit model, we use a controlled current source, like we did in the mathematical (see Figure A.4). Figure A.9 shows a nonlinear circuit model of a diode. In this model the

![Figure A.9: Small signal circuit model of the nonlinear diode.](image)

linear part is described by equivalent circuit components, while the nonlinear part is represented by a controlled current source. This model is only valid for so called weak nonlinearities and is also used for distortion analysis as shown in [6]. To determine the nonlinear current we use a Volterra series approximation, which is able to cope with the nonlinear part as well as the frequency dependent behavior of the current-voltage relationship.

With the help of Volterra theory [7] the additional diode current \( \hat{I}_{dd}(j\omega) \) can be expressed in frequency domain as:

\[
\hat{I}_{dd}(j\omega) = \sum_{n=2}^{\infty} \int_{-\infty}^{\infty} \cdots \int_{-\infty}^{\infty} \left[ \frac{1}{(2\pi)^n} \hat{G}_n(j\omega_1, \ldots, j\omega_n) \right] \prod_{m=1}^{n} \hat{U}_f(j\omega_m) \delta(\omega - \sum_{p=1}^{n} \omega_p) d(\omega_1, \ldots, \omega_n), \tag{A.26}
\]

where \( \hat{G}_n(j\omega_1, \ldots, j\omega_n) \) are the Volterra kernels of order \( n \) of the nonlinear part of the diode conductance. Note that the linear term, e.g. the first order kernel \( \hat{G}_1(j\omega_1) \) in the
summation of (A.26) is omitted, because this term is modeled by linear components as depicted in Figure A.9. We decompose these nonlinear diode conductance Volterra kernels in two components:

\[ G_i(j\omega_1, \ldots, j\omega_i) = G_{d,i}(j\omega_1, \ldots, j\omega_i) + G_{c,i}(j\omega_1, \ldots, j\omega_i) \]  

(A.27)

\( G_{d,i}(j\omega_1, \ldots, j\omega_i) \) is the nonlinear contribution from the diffusion current and \( G_{c,i}(j\omega_1, \ldots, j\omega_i) \) the contribution from the depletion width modulation. In our approximation, the latter is only present for a reverse biased diode.

**Diffusion Current Contribution to the Nonlinear Transfer**

The mathematical model in Figure A.4 shows that the diffusion current conduction mechanism can be considered as a cascade of a nonlinear minority charge injection function and a linear diffusion function. We therefore determine the transfer as the product in frequency domain of the nonlinear transfer and diffusion process, which is modeled as a linear filter.

The injected minority charge described by (A.1) and (A.2) are assumed to be weakly nonlinear and instantaneously reacting to the input voltage. These functions therefore can be approximated by the first three terms of a Taylor expansion:

\[ n_p(t) = n_{p0} \left[ \exp \left( \frac{U_0}{T} \right) \exp \left( \frac{u_f(t)}{U_T} \right) - 1 \right] \approx n_{pdc} \left[ U_T^{-1} u_f(t) + \frac{1}{2} U_T^{-2} u_f^2(t) + \frac{1}{6} U_T^{-3} u_f^3(t) \right] + n_{pdc} - n_{p0} \]  

(A.28)

\[ p_n(t) = p_{n0} \left[ \exp \left( \frac{U_0}{T} \right) \exp \left( \frac{u_f(t)}{U_T} \right) - 1 \right] \approx p_{ndc} \left[ U_T^{-1} u_f(t) + \frac{1}{2} U_T^{-2} u_f^2(t) + \frac{1}{6} U_T^{-3} u_f^3(t) \right] + p_{ndc} - p_{n0} \]  

(A.29)

To determine the Volterra kernels in frequency domain, the frequency equivalent of these function are required. Because this process is assumed to be instantaneous, the kernels are constant and equal the Taylor coefficients. The injected charge in frequency domain can be described as:

\[ \hat{n}_p(j\omega) \approx n_{pdc} \sum_{n=1}^{3} \left[ \frac{U_T^{-n}}{n!(2\pi)^{n-1}} \right] \int_{-\infty}^{\infty} \prod_{m=1}^{n} \hat{u}_f(j\omega_m) \delta(\omega - \sum_{k=1}^{n} \omega_k) d(\omega_1, \ldots, \omega_n) + 2\pi (n_{pdc} - n_{p0}) \delta(\omega) \]  

(A.30)

\[ \hat{p}_n(j\omega) \approx p_{ndc} \sum_{n=1}^{3} \left[ \frac{U_T^{-n}}{n!(2\pi)^{n-1}} \right] \int_{-\infty}^{\infty} \prod_{m=1}^{n} \hat{u}_f(j\omega_m) \delta(\omega - \sum_{k=1}^{n} \omega_k) d(\omega_1, \ldots, \omega_n) + 2\pi (p_{ndc} - p_{n0}) \delta(\omega) \]  

(A.31)
These injected charge currents are “filtered” by the diffusion processes as indicated by Equation (A.7). We can define two filters, one for the injected electrons:

$$\hat{H}_{d,n}(j\omega) = D_n \frac{\sqrt{1+j\omega \tau_n}}{L_n} \coth \left[ \frac{\sqrt{1+j\omega \tau_n}}{L_n} (W_P) \right]$$  \hspace{1cm} (A.32)$$

and one for the injected holes in the diode:

$$\hat{H}_{d,p}(j\omega) = D_p \frac{\sqrt{1+j\omega \tau_p}}{L_p} \coth \left[ \frac{\sqrt{1+j\omega \tau_p}}{L_p} W_N \right]$$  \hspace{1cm} (A.33)$$

With the help of Volterra theory [7], the Volterra kernels of the diffusion current contribution can be written as:

$$\hat{G}_{d,k}(j\omega_1, \ldots, j\omega_n) = qA \frac{U_{j\omega}}{kT} \left[ n_{pdc} \hat{H}_{d,n}(j \sum_{i=1}^k \omega_i) + p_{n_{dc}} \hat{H}_{d,p}(j \sum_{i=1}^k \omega_i) \right]$$  \hspace{1cm} (A.34)$$

With this Volterra kernel, the contribution of the diffusion current to the nonlinear source is given by:

$$\hat{I}_{dd,\text{diffusion}}(j\omega) \approx \sum_{n=2}^3 \frac{1}{2\pi j \omega_n} \int \cdots \int \hat{G}_{d,n}(j\omega_1, \ldots, j\omega_n) \prod_{m=1}^n \hat{U}_f(j\omega_m) \delta(\omega - \sum_{p=1}^n \omega_p) \, d(\omega_1, \ldots, \omega_n),$$  \hspace{1cm} (A.35)$$

The circuit models shown in the Figures A.5, A.7 and A.8 where derived with the help of a first or fourth order approximation of the diffusion process. Such an approximation could also be applied to (A.32) and (A.33). The Volterra kernels become in such an approximation:

$$\hat{G}_{d,k}(j\omega_1, \ldots, j\omega_k) = \frac{U_{j\omega}}{kT} \hat{Y}_{\text{diode}}(\sum_{p=1}^k j\omega_p),$$  \hspace{1cm} (A.36)$$

where $\hat{Y}_{\text{diode}}(j\omega)$ is the linearized diode admittance of the diode

$$\hat{Y}_{diode}(j\omega) = \frac{qA}{kT} \left( D_n n_{pdc} \frac{\sqrt{1+j\omega \tau_n}}{L_n} \coth \left[ \frac{\sqrt{1+j\omega \tau_n}}{L_n} (W_P) \right] \right. \right.$$

$$\left. + D_p p_{n_{dc}} \frac{\sqrt{1+j\omega \tau_p}}{L_p} \coth \left[ \frac{\sqrt{1+j\omega \tau_p}}{L_p} W_N \right] \right),$$  \hspace{1cm} (A.37)$$

It must be noted that the depletion with coordinate $W_P$ is a negative number (see Figure A.1).

**Depletion Width Modulation Contribution to the Nonlinear Transfer**

To the nonlinear part of the current, due to modulation of the depletion width, we apply the same Volterra approximation as we applied to the diffusion current. As we noted before, this term is only present in a reverse biased diode.
The space charge stored in the depletion layer as described by equation Equation (A.8), can be approximated by a Taylor series expansion as follows:

\[
Q(t) \approx A \sqrt{2q\varepsilon_s(U_{bi} - U_0) \frac{N_A N_D}{N_A + N_D}} 
\left[ 1 - \frac{1}{2(U_{bi} - U_0)} u_f(t) - \frac{1}{8(U_{bi} - U_0)^2} u_f^2(t) - \frac{1}{16(U_{bi} - U_0)^3} u_f^3(t) \right]
\]  

(A.38)

The Volterra kernels in frequency domain of this charge equal the constants of this Taylor expansion. The required Volterra kernels follow from (A.9) and (A.38):

\[
\hat{G}_{c,n}(j\omega_1, \cdots, j\omega_n) = j\omega_n \frac{\Gamma(n - \frac{1}{2})}{n!2\sqrt{\pi} (U_{bi} - U_0)^n} A \sqrt{2q\varepsilon_s(U_{bi} - U_0) \frac{N_A N_D}{N_A + N_D}} \prod_{i=1}^{n-1} \delta(\omega_i),
\]

(A.39)

where \(\Gamma(\cdot)\) is the Euler gamma function [8], which can be viewed as generalization of factorial function. The first Volterra kernel of this series equals the admittance of the capacitance \(C_C\) defined by (A.20) in the first order approximation. The kernels defined by (A.39), therefore can be simplified to:

\[
\hat{G}_{c,n}(j\omega_1, \cdots, j\omega_n) = j\omega_n C_C \frac{2\Gamma(n - \frac{1}{2})}{n!2\sqrt{\pi} (U_{bi} - U_0)^{n-1}} \prod_{i=1}^{n-1} \delta(\omega_i),
\]

(A.40)

With this function we can determine the contribution of the depletion width modulation to the nonlinear current source:

\[
\hat{I}_{dd,depletion}(j\omega) \approx \sum_{n=2}^{3} \frac{1}{2\pi n} \int_{-\infty}^{\infty} \int_{-\infty}^{\infty} \hat{G}_{c,n}(j\omega_1, \cdots, j\omega_n) 
\prod_{m=1}^{n} \hat{U}_f(j\omega_m) \delta(\omega - \sum_{p=1}^{n} \omega_p) d(\omega_1, \cdots, \omega_n),
\]

(A.41)

The total current due to nonlinearities is given by (A.26). Because we assumed a weak nonlinearity, the nonlinear part can be approximated by a second or third order Volterra series approximation, which is still useful for hand calculation.
Bibliography


Appendix B

Bipolar Transistor Nonlinear Design Model

For EM-compatible circuit design, transistor models are required that are valid over a wide frequency range and takes the signal deformation due to nonlinearities into account. Such models do exist for simulation purposes, but these are too complicated analysis by hand. To provide insight in the cause of EM interference, we will develop a nonlinear dynamic model of a bipolar transistor, which is suited for hand calculations.

Wamback [1] has developed a nonlinear design model, based on the Gummel-Poon simulation model that is used in Spice. However, the validity of the Gummel-Poon model is limited to about one tenth of the transistor’s transition frequency. In this appendix we will develop a model that can be applied up to the transistor’s transition frequency. We will derive the model from a simplified physical description of a transistor. Our model does not account for all specific physical aspects included in the Gummel-poon model, but it is accurate enough for most hand calculations.

Because the nonlinear behavior is approximated by a third order Volterra approximation, this is a small signal model. In the following paragraphs we follow the same procedure as in Appendix A. First we develop an “exact” mathematical nonlinear model, that is accurate but not suited for design. From this model, less accurate circuit models are derived. Note that we put “exact” between quotes, because the mathematical model is based on simplified physics.

In this appendix we use a NPN transistor for derivation of the model, the derived models however are also valid for PNP transistors.

B.1 A Mathematical Transistor Circuit Model

For the derivation of a nonlinear circuit model of a bipolar transistor, we develop in this section an “exact” mathematical model. This model serves as a base for the design models derived in succeeding sections. We simplify the physics, therefore not all aspects of a practical transistor are included. The mayor aspects, required for design purposes, however are included.
B.1.1 Conduction Mechanisms of an Active Transistor

Consider the cross-section of a NPN transistor shown in Figure B.1. In normal operation, the base-emitter PN junction is forwardly biased and the base-collector PN junction is reversely biased. In this mode, electrons from the emitter are injected into the base region, while holes are injected into the emitter region. A good transistor has a small base region, so that the majority of these electrons reach the base-collector region before they recombine. This junction is reverse biased such that these electrons are immediately pulled to the collector. Because the majority of the injected charge reaches the collector, the base current is kept small. This mechanism gives the transistor its current gain.

A general model of a bipolar transistor in normal operation is shown in Figure B.2. Both junctions are modeled in the same manner as the mathematical model of a diode as explained in Appendix A. The voltage across the junctions is the input of a nonlinear function that controls the current through the junctions. As indicated in Figure B.2, the nonlinear function of the base-emitter function is divided in a nonlinear part that controls the charge across the depletion layer and a linear part that represents the diffusion process in the base region (see Appendix A). The biggest part of the charge that crosses the base emitter junction is pulled away by the reverse biased base collector. This is modeled in Figure B.2 by the fraction $\alpha$ of the base-emitter current that flows through the collector-base junction. This fraction $\alpha$ is called the base current gain. For an ideal transistor $\alpha$ approaches one, so that the net base current would become zero. The Voltage across the collector-base junction, causes depletion width modulation of the collector-base junction (capacitance) as well as base width modulation (Early effect). Both effect are modeled by additional control lines to the two controlled current sources.
B.1.2 Mathematical Description of the Transistor Model

Figure B.3 shows the minority charge access carriers in all three regions of an NPN transistor:

**Base Region.** The emitter injects electrons into the base region, which diffuses towards the reverse biased base-collector junction. Because the base collector junction is reversely biased, almost all free electrons are pulled towards the collector region.

**Emitter region.** The forward biased base-emitter junction injects holes into the often short emitter, which diffuses towards the connected wire.

**Collector region** Because the base-collector junction is reversely biased, almost no holes enter the collector region. Only electrons from the base junction, which become part of the majority in the collector region.

The current through both junctions can be determined in the same manner as for a normal diode (see Appendix A, we therefore will only give the results in this appendix. To determine the functions in our general transistor model Figure B.2, we need to determine the following relations:

- The current through the base-emitter junction as a function of the base-emitter voltage (diffusion current) and collector-base voltage (early effect).
- The current through the collector-base junction as function of collector-base voltage (depletion width modulation).
- The base current gain $\alpha$, which is the fraction of the current through the base-emitter junction that reaches the collector.

$$
\hat{I}_E(j\omega) = qA_{BE} F \left[ \exp \left( \frac{U_{BE}(t)}{U_T} \right) - 1 \right] \left\{ D_n n_p 0 \frac{\sqrt{1 + j\omega \tau_n}}{L_n} \coth \left( \frac{\sqrt{1 + j\omega \tau_n}}{L_n} W_B(U_{CB}, j\omega) \right) \right\}
+ D_p p_n 0 \frac{\sqrt{1 + j\omega \tau_p}}{L_p} \coth \left( \frac{\sqrt{1 + j\omega \tau_p}}{L_p} W_E \right) 
- \frac{\sqrt{1 + j\omega \tau_n}}{L_n} D_n n_p 0 qA_{BE} \sinh \left( \frac{\sqrt{1 + j\omega \tau_n}}{L_n} (W_B(U_{CB}, j\omega)) \right) \right]^{-1}, \quad \text{(B.1)}
$$

Figure B.3: Minority charge distribution of an active transistor.

**Emitter Current Dependence On $U_{BE}$**

The current through the base-emitter junction equals the emitter current $I_E$ and in our simplified model is given by (see Equation (A.7)):
where \( A_{BE} \) is the surface area of a cross-section of the base emitter junction, \( q \) the absolute charge of an electron, \( \mathcal{F} \) the Fourier operator and \( W_B \) and \( W_E \) are the lengths of the base and emitter region respectively (see Figure B.3). The constants \( \tau_n, D_n \) and \( \tau_p, D_p \) and \( L_p \) are the average life time, diffusion constant and diffusion length of free electrons in the base region and holes in the emitter region respectively.

**Collector Current Dependence on \( U_{CB} \)**

The collector-base junction is reversely biased, therefore the diffusion current should be negligible. In this situation, the contribution of the junction width modulation is dominant. This current is due to the modulation of the amount of charge in the collector-base depletion region (see Equation (A.8) and (A.9)):

\[
\hat{I}_{C; U_{CB}} = A_{CB} \mathcal{F} \left[ \sqrt{2q\varepsilon_s \left[ U_{bi; BC} + U_{CB}(t) \right] \frac{N_{A:B} N_{D:C}}{N_{A:B} + N_{D:C}}} \right],
\]

where \( A_{CB} \) equals the surface area of a cross-section of the collector-base junction, \( N_{A:B} \) and \( N_{D:C} \), the acceptor concentration in the base region and donor concentration in the collector respectively. The constant \( \varepsilon_s \) is the permittivity of silicon and \( U_{bi; BC} \approx U_T \ln \left( \frac{N_{A:B} N_{D:C}}{n_i^2} \right) \) \( (n_i \) is the intrinsic electron concentration) is the build in voltage of the base collector junction.

**Emitter Current Dependence on \( U_{CB} \) (Early Effect)**

The depletion width of the collector-base junction reduces the effective base width \( W_B \) as can be seen in Figure B.3. The emitter current depends on the this base width as shown by Equation (B.1), therefore modulation of base width by the collector-base voltage results in modulation of the emitter current. The effect is known as the Early effect, which is normally modeled as an output resistance between collector and emitter.

The base-width as a function of the base-emitter voltage can be expressed as:

\[
W_B(U_{CB}, j\omega) = \mathcal{F} \left[ W_{BN} - \sqrt{2\varepsilon_s (U_{bi; BC} + U_{CB}(t)) \frac{N_{D:C}}{q(N_{A:B} + N_{D:C})}} \right],
\]

where \( W_{BN} \) is the base width when the collector-base depletion layer is zero. Substitution of this expression in (B.1) leads to the complete relation. We ignored the influence of the base-emitter junction width modulation, because this junction is forward biased so that its influence is negligible.

**Base Current Gain Factor**

The difference between a transistor and two diodes in ant series is that the majority of the charge that passes the emitter-junction also crosses the base-collector junction. For an ideal transistor the collector current equals the emitter current such that the base current would become zero. The deviation from this ideal is described by the base current gain \( \alpha(j\omega) \):

\[
\alpha(j\omega) = \frac{\partial I_C}{\partial I_E}
\]

(B.4)
A Mathematical Transistor Circuit Model

As can be found in most books about semiconductors like [2, 3], this factor differs from one due to three major effects:

- The emitter current consists of two parts: holes injected into the emitter and electrons into the base region. Only the latter contributes to the collector current, while the hole current contributes to the remaining base current. The ratio of electron current over the total emitter current is called "Emitter injection efficiency factor" $\gamma(j\omega)$.

- Within the base region (a small) part of the injected electrons recombine and never reaches the collector. The ratio of current that reaches the collector over the injected current is called: “Base transport factor” $\alpha_T(j\omega)$.

- During injection, the electrons have to cross the depletion region between base and emitter, where also recombination losses occur. The ratio of the current that reaches the base over the total current through this depletion layer is called “Recombination factor” $\delta(j\omega)$.

The total base current gain $\alpha$ is the product of these factors:

$$\alpha(j\omega) = \gamma(j\omega)\alpha_T(j\omega)\delta(j\omega)$$

Most books on semiconductor physics do explain these factors, but they often omit the frequency dependence. If we assume that the transistor is biased forwards ($Exp(U_{BE,0}U_T^{-1}) \gg 1$) a fair approximation of the emitter injection efficiency factor $\gamma(j\omega)$ is given by:

$$\gamma(j\omega) \approx \frac{1}{1 + \frac{D_p p_0 \sqrt{1+j\omega \tau_p L_p^{-1}}} {D_n n_0 \sqrt{1+j\omega \tau_n L_n^{-1}}} \coth(\sqrt{1+j\omega \tau_p L_p^{-1}W_E}) \coth(\sqrt{1+j\omega \tau_n L_n^{-1}W_B})}$$

Under the same conditions the Base transport factor $\alpha_T(j\omega)$ can be approximated by:

$$\alpha_T(j\omega) \approx \exp(-j\omega \tau_F) \cosh(\sqrt{1+j\omega \tau_n L_n^{-1}W_B})$$

where $\tau_F$ is the time required to pass the base region. This time delay in the base region is much larger than in the emitter or collector region, because the electrons are only in the base region a minority carrier. The recombination factor is given by:

$$\delta(j\omega) \approx F \left[\frac{1}{1 + \frac{I_{r0}}{I_{s0}} \exp(-U_{BE}(t)/2U_T)}\right]$$

where $I_{r0}$ is the recombination current and $I_{s0}$ the emitter current for zero $U_{BE}$. This implies that the current gain is modulated by the base-emitter voltage. The higher the base-emitter voltage, the closer this recombination factor approaches one.

With these definitions, the mathematical transistor model is complete and we are able to develop design models.
B.2 Derivation of a Nonlinear Design Model

We want a nonlinear design model that suits the techniques available for linear circuits. This is possible if we assume a weak nonlinear behavior that can be approximated by the first three terms of a Volterra series. The following sections, first determine a linearized model of the mathematical model, which is known as the transport model (T-model). The relation between the T-model and the often used hybrid-π is demonstrated. These linear models are extended to a nonlinear model in the last section.

B.2.1 The Transport Transistor-Model

A transistor model that comes very close the physical model of a transistor is the transport (T)-model [4]. This is the linearized version of our general model shown in Figure B.2. A big advantage of the T-model model is, due to its close resemblance of the physics, the wide frequency range for which it is valid. As shown in [4] and [5], it is a very simple model that is able to predict the behavior up the transition frequency. Although suited for design, it is not as popular as the hybrid-π model, because it is not unilateral. We will derive the hybrid-π model as an approximation of the T-model, such that the limitations of the hybrid-π model are clarified.

Assume that the transistor is biased around a bias point \( \{U_{BE,0}, U_{CB,0}, I_{E,0}, I_{C,0}\} \). We are interested in the small changes around this bias point:

\[
U_{BE}(t) = U_{BE,0} + u_{BE}(t) \quad \text{(B.9)} \\
U_{CB}(t) = U_{CB,0} + u_{CB}(t) \quad \text{(B.10)} \\
I_{E}(t) = I_{E,0} + i_{E}(t) \quad \text{(B.11)} \\
I_{B}(t) = I_{B,0} + i_{B}(t) \quad \text{(B.12)} \\
I_{C}(t) = I_{C,0} + i_{C}(t) \quad \text{(B.13)}
\]

The emitter current depends on \( U_{BE} \) as well as \( U_{CB} \). In a first order linearized approximation this current equals:

\[
\hat{I}_E(j\omega) = \left. I_{E,0} + \hat{i}_E(j\omega) \right|_{u_{CB}=0} + \left. \hat{i}_E(j\omega) \right|_{u_{BE}=0} \quad \text{(B.14)}
\]

The Base-Emitter Impedance

The part of the emitter current that depends upon \( \hat{u}_{BE} \) is similar to a current of a forwards biased diode. In a first order approximation of (B.1) this current is given by:

\[
\hat{i}_E(j\omega) \Big|_{u_{CB}=0} \approx qA_{BE} \frac{\partial i_{BE}(j\omega)}{\partial U_T} \left( D_n n_{pd} \frac{1}{L_n} \coth \left( \frac{W_{BE,0}}{L_n} \right) + D_p n_{pd} \frac{1}{L_p} \coth \left( \frac{W_{BE,0}}{L_p} \right) \right) \\
+ j\omega \frac{1}{2} \left( \frac{\tau_D n_{pd}}{L_n} \left[ \coth \left( \frac{W_{BE,0}}{L_n} \right) - \frac{W_{BE,0}}{L_n} \sinh \left( \frac{W_{BE,0}}{L_n} \right)^2 \right] \\
+ \frac{\tau_D n_{pd}}{L_p} \left[ \coth \left( \frac{W_{BE,0}}{L_p} \right) - \frac{W_{BE,0}}{L_p} \sinh \left( \frac{W_{BE,0}}{L_p} \right)^2 \right] \right) \right), \quad \text{(B.15)}
\]
where \( n_{pdc} \) and \( p_{ndc} \) are approximately the injected electron and hole concentration at bias level. These are given by:

\[
\{n_{pdc}, p_{ndc}\} = \{n_0, p_0\} \exp \left( \frac{U_{BE,0}}{U_T} \right)
\]  

(B.16)

Note that we linearized the frequency dependent part around a frequency of zero. This part of the emitter current can be modeled as a resistor and capacitor in parallel, with the following values:

\[
R_{BE} = \left[ \frac{qA_{BE}}{2U_T} D_n n_{pdc} \frac{1}{L_n} \coth \left( \frac{W_{B,0}}{L_n} \right) + D_p p_{ndc} \frac{1}{L_p} \coth \left( \frac{W_{E}}{L_p} \right) \right]^{-1} \approx \frac{U_T}{I_E} 
\]  

(B.17)

\[
C_{BE} = \frac{qA_{BE}}{2U_T} \left\{ \frac{\tau_n D_n n_{pdc}}{L_n} \left[ \coth \left( \frac{W_{B,0}}{L_n} \right) - \frac{W_{B,0}}{L_n} \sinh \left( \frac{W_{B,0}}{L_n} \right)^{-2} \right]
\right.

+ \left. \frac{\tau_p D_p p_{ndc}}{L_p} \left[ \coth \left( \frac{W_{E}}{L_p} \right) - \frac{W_{E}}{L_p} \sinh \left( \frac{W_{E}}{L_p} \right)^{-2} \right] \right\} 
\]  

(B.18)

A good transistor must have a high current gain, therefore the base transport factor (B.7) must be close to one. This implies that \( W_{E,0} \ll L_n \), so that (B.18) can be approximated by:

\[
C_{BE} \approx \frac{qA_{BE}}{2U_T} \frac{\tau_n D_n n_{pdc}}{L_p} \left[ \coth \left( \frac{W_{B,0}}{L_n} \right) - \frac{W_{B,0}}{L_n} \sinh \left( \frac{W_{B,0}}{L_n} \right)^{-2} \right],
\]  

(B.19)

hence due the small base, the contribution of the electron current to the junction capacitance \( C_{BE} \) vanishes and only the contribution of the hole current is left. For a reasonable current gain; the emitter injection efficiency factor (B.6) has to be close to one. Hence the hole current has to be small such that \( C_{BE} \) is much smaller than the capacitance of a normal conducting diode. For compatibility analyses this is important, because it implies less attenuation of nonlinear distortion than predicted by the hybrid-\( \pi \) model.

**Contribution of the Early effect**

Due to the early effect, e.g. base width modulation, the emitter current is also modulated. The influence can be determined by substitution of (B.3) in (B.1). In a first order approximation approximation this current equals:

\[
\hat{i}_E(j\omega) \bigg|_{U_{BE}=0} \approx \hat{u}_{CB}(j\omega)
\]

\[
\frac{qA_{BE} D_n n_{p0}}{2L_n^2} \sqrt{\frac{2\epsilon_n}{q(U_{bi,c} + U_{CB,0}) N_{D,C}}} \left[ \exp \left( \frac{U_{BE,0}}{U_T} \right) - 1 \right]
\]

\[
\left\{ \sinh \left( \frac{W_{B,0}}{L_n} \right)^{-2} + j\omega \tau_n \sinh \left( \frac{W_{B,0}}{L_n} \right)^{-3} \left[ \sinh \left( \frac{W_{B,0}}{L_n} \right) - \frac{W_{B,0}}{L_n} \cosh \left( \frac{W_{B,0}}{L_n} \right) \right] \right\}
\]

\[
- \frac{\coth \left( \frac{W_{B,0}}{L_n} \right)^{-2} - j\omega \tau_n \sinh \left( \frac{W_{B,0}}{L_n} \right)^{-3} \left[ 3W_{B,0} + \frac{W_{B,0}}{4L_n} \cosh \left( \frac{2W_{B,0}}{L_n} \right) - \sinh \left( \frac{2W_{B,0}}{L_n} \right) \right]}{\sinh \left( \frac{W_{B,0}}{L_n} \right)^{-2}},
\]  

(B.20)
where $W_{B:0}$ is the base width for a given biasing and $U_{bi:BC}$ is the build voltage of the base-collector junction. This complex equation can be simplified if we assume properly biasing and a small base width, e.g. $\exp \left( \frac{U_{BE}}{U_T} \right) \gg 1$ and $W_{B:0} \ll L_n$. In this situation the current due to the Early effect simplifies to:

$$
\hat{i}_E(j\omega)_{\mid U_{BE}=0} \approx \hat{u}_{CB}(j\omega)
$$

where $W_{p;BC}$ is the width of the part of the depletion layer of the collector-base junction that resides in the base region (see Figure B.1). This effect is modeled as an output resistor $R_o$ between collector and emitter that equals:

$$
R_o \approx \frac{2W_{B:0}^2(U_{bi:BC} + U_{CB:0})}{I_{C:0}L_n W_{p;BC}}
$$

This output resistance is normally specified as $R_o = \frac{U_A}{I_{C:0}}$ where $U_A$ is the Early voltage. When the transistor has a high current gain, the electron current is dominant so that this Early voltage equals:

$$
U_A \approx \frac{2W_{B:0}^2(U_{bi:BC} + U_{CB:0})}{L_n W_{p;BC}}
$$

**The Base-Collector Impedance**

Similar to the emitter current, the collector current of the linearized model can be written as a function of both the base-emitter voltage and collector-base voltage:

$$
\hat{I}_C(j\omega) = I_{C:0} + \frac{\hat{I}_C(j\omega)_{\mid u_{CB}=0}}{u_{CB}} + \hat{I}_C(j\omega)_{\mid u_{BE}=0}
$$

The influence of the collector-base voltage on this current is due to the depletion width modulation. This current (see (B.2)) equals the current of a reverse biased diode. In a first order approximation it is given by:

$$
\hat{I}_C(j\omega)_{\mid u_{BE}=0} \approx j\omega u_{CB}(j\omega) A_{CB} \sqrt{\frac{q\varepsilon_s N_{A:B} N_{D:C}}{2(U_{bi} - U_0) N_{A:B} N_{D:B}}}
$$

This contribution corresponds to a capacitor $C_{BC}$ between base and collector:

$$
C_{BC} = A_{CB} \sqrt{\frac{q\varepsilon_s N_{A:B} N_{D:C}}{2(U_{bi} - U_0) N_{A:B} N_{D:B}}}
$$

The contribution of the base-emitter voltage to the collector current is the fraction of the emitter current that reaches the collector:

$$
\hat{I}_C(j\omega)_{\mid u_{CB}=0} = \alpha(j\omega) \hat{i}_E(j\omega)_{\mid U_{CB}=0}
$$
where $\alpha(j\omega)$ is the base current gain factor (B.5). The transport delay is the most dominant frequency dependence of the base current gain, while the modulation of the recombination factor (B.8) is ignored compared to the modulation of the total collector current. The base current gain factor, therefore, is approximated as:

$$\alpha(j\omega) \approx \alpha_0 \exp(-j\omega\tau_f)$$  \hspace{1cm} (B.28)

The complete T-model is shown in Figure B.4. This is a linearized model that is valid up to the transistor’s transition frequency shown in [4]. It is suited for linear design techniques. However, due to the controlled current source between emitter and collector and the capacitor $C_{CB}$, this model is not unilateral. Therefore this model is not handy for design purposes.

### B.2.2 The Hybrid-$\pi$ Transistor-Model

For circuit design purposes, the hybrid-$\pi$ model is often preferred, because of its handy unilateral approximations. In this section, we will show that the hybrid-$\pi$ model can be considered as a low-frequency approximation is of the transport model.

The main difference between that hybrid-$\pi$ model and the T-model is the approximation of transport delay through the base region. In the hybrid-$\pi$ model this is approximated as:

$$\exp(-j\omega\tau_f) \approx 1 - j\omega\tau_f$$  \hspace{1cm} (B.29)

The complete translation is shown on Figure B.5. As shown in the first scheme in Figure B.5, a first order approximation is applied to the delay. In the first step, the complex part of the current through this source is splitted and modeled as an additional capacitor between base and emitter (ignoring the current $R_{CE}$). Note that $I_E$ in these figures is the current through $R_E$ only. In the last step the current source is splitted in two equal currents, where the first one is modeled as a negative resistance between base and emitter, which results in a higher net base emitter resistor. The resulting model is exactly the hybrid-$\pi$ model. This model is valid when the first order approximation (B.29) is valid. We can conclude that the hybrid-$\pi$ can be considered as a low frequency approximation of the T-model suited for circuit design much that stay much below the transition frequency.
B.2.3 Derivation of Nonlinear-Transistor-Design Models

In this section we will extend the linearized T-model and hybrid-$\pi$ model to a nonlinear model. The two main nonlinearities in a bipolar transistor are:

- the injection mechanism of the base-emitter junction;
- the depletion width modulation of the collector-base junction.

In principle the early effect is also nonlinear, however this contribution should be small for a good transistor in normal operation.

To model these nonlinearities, we apply the same method as we did for the diode in Appendix A. We split each transfer in a linear and nonlinear part. The linear part is modeled by an equivalent circuit, hence the circuits derived in the previous sections, while the nonlinear part is modeled as controlled current source that add the nonlinear terms of the current. The nonlinearities are approximated by a third order Volterra series.

Nonlinear Contribution of the Base-Emitter Junction

The nonlinear emitter current as a function of the base emitter voltage is approximated by:

$$\hat{i}_E(j\omega) \approx \sum_{n=1}^{3} \frac{1}{(2\pi)^{n-1}} \int \cdots \int_{-\infty}^{\infty} \hat{G}_{E,n}(j\omega_1, \ldots, j\omega_n) \prod_{m=1}^{n} \hat{u}_BE(j\omega_m) \delta(\omega - \sum_{p=1}^{n} \omega_p) d(\omega_1, \ldots, \omega_n), \quad (B.30)$$
where $\hat{G}_{E,n}(j\omega_1,\ldots,j\omega_n)$ is the Volterra kernel of order $n$ of the emitter current. Equation (A.36) shows a very simple approximation of the Volterra kernels of the diffusion current in a diode. The same approximation applies to the emitter current, hence $\hat{G}_{E,n}(j\omega_1,\ldots,j\omega_n)$ is approximated as:

$$
\hat{G}_{E,n}(j\omega_1,\ldots,j\omega_n) \approx \frac{1}{n!} \hat{Y}_{BE}(j\omega_1,\ldots,j\omega_n) \approx \frac{1}{n!} \hat{Y}_{BE}(\sum_{p=1}^{n} j\omega_p),
$$

(B.31)

where $\hat{Y}_{BE}(j\omega)$ is the linearized admittance of the base-emitter junction, e.g. $\hat{Y}_{BE}(j\omega) = R_{BE} + j\omega C_{BE}$. This current results in one additional source in the T-model as shown in Figure B.6. This nonlinear source $\hat{i}_{E,\text{nl}}(j\omega)$ equals:

$$
i_{E,\text{nl}}(j\omega) \approx \frac{1}{2\pi j^{n-1}} \int \cdots \int_{-\infty}^{\infty} \hat{G}_{E,n}(j\omega_1,\ldots,j\omega_n) 
\prod_{m=1}^{n} \hat{u}_{BE}(j\omega_m) \delta(\omega - \sum_{p=1}^{n} \omega_p) d\omega_1 \cdots d\omega_n,
$$

(B.32)

Note that we only add the nonlinear terms, as the linear term is modeled by linear network elements. In the hybrid-$\pi$ model we splitted the emitter current in a base current and a collector current. Two 100% correlated nonlinear sources appear in the hybrid-$\pi$ model as shown in Figure B.7. In most cases this current is the most important nonlinear contribution.
Nonlinear Contribution of the Collector-Base Junction

The main nonlinear contribution of the collector-base junction is the depletion with modulation of this junction. The linear part of this current is modeled by $C_{BC}$, the nonlinear part is given by:

$$
\hat{i}_{C,nl}(j\omega) \approx \sum_{n=2}^{3} \prod_{m=1}^{n} \hat{u}_{CB}(j\omega_m) \delta(\omega - \sum_{p=1}^{n} \omega_p) \int_{-\infty}^{\infty} \hat{G}_{C,n}(j\omega_1, \ldots, j\omega_n) d(\omega_1, \ldots, \omega_n), \quad (B.33)
$$

where $\hat{G}_{C,n}(j\omega_1, \ldots, j\omega_n)$ are the Volterra kernels of this nonlinear current. This current equals the nonlinear current of a reverse biased diode which is given by (A.40). For the base collector junction these kernels are given by:

$$
\hat{G}_{C,n}(j\omega_1, \ldots, j\omega_n) = j\omega_n C_{CB} \frac{2\Gamma(n - \frac{1}{2})}{n! 2 \sqrt{\pi} (U_{bi;BC} + U_{CB})^{n-1} j} \prod_{i=1}^{n-1} \delta(\omega_i), \quad (B.34)
$$

where $\Gamma(\cdot)$ is the Euler gamma function. Also this nonlinear contribution is modeled as a controlled current source, this time controlled by the collector-base current. To both the T-model and the hybrid-π model this current is added across the collector-base junction. Figure B.8 shows the complete nonlinear T-model. The complete nonlinear hybrid-π model is shown in Figure B.9.

![Complete nonlinear T-model](image)
Figure B.9: Complete nonlinear hybrid-π model.
Bibliography


Appendix C

Low Noise Current and Voltage Sensing Circuits

Voltage and current detecting circuits rely on feedback to discriminate between current and voltage domain. These circuits are often used to make the signal transfer independent of the source impedance. However, because these circuits ideally reflect all signal energy, one would expect a very bad signal to noise ratio. Because the signal power at the input vanishes, the detector’s own noise should dominate. With the help of feedback, however, voltage and current detectors can be imitated that have a high signal to noise ratio.

In this appendix, we will show how noise and interference can be minimized by using current or voltage domain signal transport, and we will determine the requirements (loop gain, bandwidth) for building proper current or voltage detecting circuits. In this appendix we consider the system level only, no circuit implementations are considered.

C.1 Minimization of the Noise in Signal Paths

In quasi static electrical domain, the two energetic quantities (current and voltage) can both be used for coding of a signal. Although both represent a different type of energy storage, the signal to (interference) noise ratio is independent of the detected quantity. Only the transmitted quantity, which is determined by the source impedance $Z_S$, determines the influence of the noise sources. We explain this with the help of the electrical signal path depicted in Figure C.1. Assume the source is noise free,
while the signal path suffers from (interference) noise in voltage ($U_n$) and current ($I_n$) domain. The signal path conductor impedance is denoted by $Z_C$, the detector impedance by $Z_D$ and the signal source impedance by $Z_S$. The signal to noise ratio, measured by the detector in Figure C.1 is given by:

$$\frac{P_S}{P_n} = \frac{\sigma^2_{U_n}}{\sigma^2_{U_n} + |Z_S + Z_C|^2 \sigma^2_{I_n} + 2\text{Re}\{\text{cov}[U_n^*, I_n(Z_S + Z_C)]\}}$$

where $\sigma^2_{U_n}$ and $\sigma^2_{I_n}$ are the equivalent voltage source and current source power respectively of the signal source. The function $\text{cov}(\cdot, \cdot)$ is the covariance. We assumed that the noise sources are independent of the signal source. It must be noted that the detected signal to noise ratio is independent of the detector impedance $Z_D$. The influence of the current noise $I_n$ vanishes when the source impedance $Z_S$ becomes zero. The influence of the voltage noise vanishes when the source impedance $Z_S$ becomes infinitely high. The detector impedance $Z_D$ is adapted to source impedance for an optimal signal transfer. If the source impedance not well defined, a voltage or current detector can be applied to optimize the transfer (see [1]).

In conclusion, the source impedance can be used to minimize the influence of noise sources, while the detector impedance can be used to minimize the influence of the source impedance on the transfer.

### C.2 Current and Voltage Detection with the Help of Feedback

Because information is carried by energy, one would expect that any detector absorbs signal energy. An ideal voltage or current sensor however, does not require any energy from a source, because it reflects all signal energy. This would lead to a very bad signal to noise ratio, as the input noise of the detector will dominate. Hence also the rate of transferred information vanishes. A closer look at a voltage or current detector that applies feedback however, shows that the absorbed energy is not zero. Only the net energy that is transported, can be arbitrary close to zero. Such a detector imitates the reflection process. The signal is sensed (absorbing signal energy) and an exact copy of the signal is send back (reflected) to the source. Without feedback, low noise current or voltage detection is not possible, because the feedback is required to compensate (e.g., reflect) the absorbed signal energy. Figure C.2 shows the principle of a system with active reflection. The input signal is sensed and with some phase shift $\varphi$ reproduced by a controlled source. This reproduced signal is send back to the signal source. We used an artificial directional coupler at the input to separate the forward and reflected signal. The reflected signal must have exactly the same amplitude as the input signal, so that the net energy transfer vanishes. An infinitely high input impedance (e.g. voltage sensing) is obtained when the reproduced signal is in phase with the input signal (e.g., $\varphi = 0 + n \cdot 2\pi$, where $n$ an integer). A zero input impedance (e.g., current sensing) is obtained when the reflected signal is in anti
phase with the input signal, thus $\varphi = \pi + n \cdot 2\pi$. Any other phase difference results in a pure reactive input impedance. We will analyze this method, using a well known voltage and current amplifier.

### C.2.1 Voltage Sensing

To determine the dependency of voltage detector on loop gain and bandwidth, we determine the reflection coefficient of the feedback voltage amplifier depicted in Figure C.3. The active part is a non ideal voltage amplifier with DC-loop gain $A$ and one dominant pole $\omega = -1/\tau$. It has a finite input impedance $Z_i$. The signal source is connected by a transmission line to the amplifier; the source impedance matches the characteristic impedance $Z_0$ of the transmission line. To simplify the analysis, we assume that when the loop-gain vanishes, nothing is reflected. Therefore, $Z_0 = Z_i + Z_1/Z_2$ when $A = 0$. It can be readily verified that the reflection coefficient of the amplifier equals:

$$\Gamma = \frac{-1}{1 + \frac{2\omega}{A\beta Z_i} + j \omega \tau \frac{2 \omega}{A\beta Z_i}}, \quad (C.2)$$

where $A\beta$ is the DC loop gain:

$$A\beta = \frac{Z_2}{Z_1 + Z_2} \quad (C.3)$$

For a high DC-loop gain $A$, the reflection coefficient approaches the required -1. The bandwidth for which the amplifier acts as a voltage detector is $Z_i/(2Z_0)$ times the
overall bandwidth of the amplifier. For most applications, this bandwidth is higher than the bandwidth of the amplifier itself. However, low noise and precision amplifiers that are build with MOS transistors, require large input transistors, that can result in a low high input impedance $Z_i$ at higher frequencies. They may become bad voltage detectors for frequencies lower than the signal bandwidth.

### C.2.2 Current Sensing

A similar results can be derived for a feed back current amplifier as shown in Figure C.4. This time we implemented the active part with a large transconductance $G$, so that the loop gain is independent of the load impedance. Again, we assume that the source impedance matches the characteristic impedance of the transmission line. To simplify the analyses, we assume that the current amplifier input (load) is matched for a zero DC-loop gain. Thus $Z_i/(Z_1 + Z_2) = Z_0$, when $G = 0$. The reflected coefficient of the amplifier equals:

$$
\Gamma = \frac{1}{1 + \frac{1}{G\beta} + j\omega \tau \frac{1}{G\beta}}, \quad (C.4)
$$

where $G\beta$ equals the DC loop gain:

$$
G\beta = GZ_0 \frac{Z_1}{Z_1 + Z_2} \quad (C.5)
$$

For a high DC-loop gain, the reflection coefficient becomes 1, which corresponds to the required short. However, for higher frequencies the loop gain decreases and the circuit becomes a less accurate current sensor. Due to the applied simplification of $Z_i/(Z_1 + Z_2) = Z_0$, (C.4) does not show the bandwidth for which this sensor is still a good current detector. However, it can be readily verified that $Z_i$ must be larger than $Z_1 + Z_2$ to ensure a low input impedance within the signal bandwidth of the amplifier. Thus for a current amplifier, the input impedance of the gain stage must be higher than the impedance of the feedback network.
C.3 Conclusions

The signal source impedance can be used to reduce the influence of current noise or voltage noise. A low signal source impedance reduces the influence of current noise and vice versa for voltage noise. The detector impedance can be used to optimize the signal transfer. A current or voltage detector can be applied to minimize the influence of the signal source impedance on the signal transfer. A low noise current or voltage detector can only be implemented with the help of feedback. For a current amplifier, the input impedance of the gain stage must be higher than the impedance of the feedback network. For a voltage amplifier, the input impedance of the gain stage must be higher than the signal source impedance.
Bibliography

Appendix D

A Thevenin Port Representation of Electrically Large Interconnect in the Presence of External EM Fields

Within an electrically large system, the electric potential is not globally defined (see Section 5.2.3). The electric potential difference can only be defined in an electrically small domain. To derive a circuit representation of an electrically large system, it must be partitioned in electrically small sub-domains, where Kirchoff’s current and voltage laws are defined locally.

In this appendix, we present a Thevenin port model where each port corresponds to an electrically small sub-domain. We therefore follow the method presented by Quack and de Hoop [1] (pages 943-958). The presented model is a kind of antenna model, where the interconnect is considered a receiving antenna for (parasitic) EM fields (e.g., from a radio transmitter). The interconnect is represented as an Thevenin Port voltage source, where the voltage sources represent the received fields.

D.1 Derivation of a Thevenin Representation of the Interconnect Layout

To derive a port description of an electrically large layout, we define electrically small domains as depicted in Figure D.1, where the electric potential is defined locally.

The potentials defined in these domains are comparable to the retarded potential function applied in Ruehli’s PEEC model. However, the retarded potential is defined globally, while we define an electric potential for each domain locally. Each domain contains one circuit domain, and the terminals of these components are the terminals
Figure D.1: Port representation of an electrically large layout.
of the ports. In Figure D.1, domain $D$ is the domain of the interconnect, $D_E$ that of the components and $D_O$ is the space outside of the circuit, where the external fields are generated. We derive the Thevenin description with the help of the Lorentz’s reciprocity theorem. This theorem relates two different electromagnetic states $A$ and $B$ of the same system. State $A$ is chosen to be the actual state where the interconnect acts as a parasitic receiving antenna for the externally generated fields. State $B$ is chosen to be a computational state, where the interconnect is the radiator due to a source applied to one of the ports of the interconnect (see [1] (pages 943-958)). This source “measures” the voltage or current induced in state $A$. The medium is assumed to be self adjoint (symmetric permeability and permittivity tensor) in both states, while the domain $D$ is free of sources, therefore the reciprocity theorem [2, 3] reduces to

$$\epsilon_{n,m,p} \int_{x \in \partial D_O} \nu_n (\hat{E}_m^A \hat{H}_p^B - \hat{E}_m^B \hat{H}_p^A) dA = \epsilon_{n,m,p} \int_{x \in \partial D_E} \nu_n (\hat{E}_m^A \hat{H}_p^B - \hat{E}_m^B \hat{H}_p^A) dA,$$

where $\{\hat{E}^A, \hat{H}^A\}$ and $\{\hat{E}^B, \hat{H}^B\}$ are the electric and magnetic fields in state $A$ and $B$ respectively, $\epsilon_{n,m,p}$ is the Levi Civita tensor, $\nu$ the normal vector on the surfaces $\partial D_E$ and $\partial D_O$ (see Figure D.1). This theorem relates the tangential electromagnetic fields in the two states that are transferred through the closed surfaces $\partial D_E$ and $\partial D_O$. In [1] (pages 943-958) it is shown that the surface integral over the electrically small component domains (i.e., the right hand side of (D.1)) can be approximated as follows:

$$\epsilon_{n,m,p} \int_{x \in \partial D_E} \nu_n (\hat{E}_m^A \hat{H}_p^B - \hat{E}_m^B \hat{H}_p^A) dA \approx \sum_{n=1}^{N} (\hat{U}_n^A \hat{I}_n^B - \hat{U}_n^B \hat{I}_n^A),$$

where $\hat{U}$ and $\hat{I}$ are the port voltages and currents as depicted in Figure D.1. Because interconnect is a linear system, the relation between the voltages and currents can be represented by an impedance matrix: $\hat{U}_i = \sum_{j=1}^{N} \hat{Z}_{i,j} \hat{I}_j$. Because of reciprocity, this impedance matrix is always symmetric $\hat{Z}_{i,j} = \hat{Z}_{j,i}$. To proof this, let the two reciprocal states $A$ and $B$ of a system be equal, while all external sources are removed, so that the left hand side of (D.1) vanishes. Substitution of the impedance matrixes for both states in (D.2) yields

$$\sum_{j=1}^{N} \hat{Z}_{i,j} \hat{I}_j^A \hat{I}_i^B = \sum_{j=1}^{N} \hat{Z}_{i,j} \hat{I}_j^B \hat{I}_i^A$$

for an arbitrary chosen current vector $\hat{I}$ in both states. Because both states are equal, the impedance matrix has to be symmetric.

To derive a Thevenin representation of the receiving interconnect, state $A$ as taken to be the actual state in which and external field is present. State $B$ is a computational state, without external fields, while an excitation source is applied to one of the ports. Substitution of the impedance matrix for state $B$ in equation (D.1), using approximation (D.2) yields

$$\sum_{i=1}^{N} (\hat{U}_i^A - \sum_{j=1}^{N} \hat{Z}_{i,j} \hat{I}_j^A) \hat{I}_i = -\epsilon_{n,m,p} \int_{x \in \partial D_O} \nu_n (\hat{E}_m^A \hat{H}_p^B - \hat{E}_m^B \hat{H}_p^A) dA,$$
where \( \{ \hat{E}_m^B, \hat{H}_p^B \} \) are the fields generated by the current sources \( \hat{I}_i^B \) applied at the ports in state \( B \). Because this expression must be valid for arbitrary excitations \( \hat{I}_i^B \), the following Thevenin representation can be derived

\[
\hat{U}_i^A = \sum_{j=1}^{N} Z_{i,j} \hat{I}_j^A + \hat{U}_i^E \tag{D.4}
\]

The Thevenin voltages \( \hat{U}_i^E \) are given by:

\[
\hat{U}_i^E = -\frac{1}{\hat{I}_i^B} \epsilon_{n,m,p} \int_{x \in \partial D_O} \nu_n (\hat{E}_m^A \hat{H}_p^B - \hat{E}_m^B \hat{H}_p^A) dA, \tag{D.5}
\]

where \( \{ \hat{H}_p^B, \hat{E}_m^B \} \) are the fields generated by a current \( \hat{I}_i^B \) applied to port \( i \). To determine the Thevenin voltage of each port, a current has to be applied to each port individually. An equivalent circuit of the Thevenin description (D.4) is depicted in Figure D.2. It must be noted that in the derivation of this model, we assumed a weak coupling to the external radiator. The influence of the interconnect on the external radiator is ignored.

**D.2 Calculation of the Thevenin Voltages for a Known Radiator**

Assume that the source of the external fields is known i.e., all information of the radiating antenna is known. The source voltages, defined in (D.5) is a surface integral over an arbitrary surface \( \partial D_O \) between the external radiating sources and the interconnect. To derive an expression for the Thevenin voltages, this boundary is chosen to be the surface of the radiating antenna. We defined the following surface current density \( \partial J^A_n = \epsilon_{n,m,p} \nu_m, \hat{H}_p^A \). For a good conductor, this surface current density approximately equals the conductor current divided by the conductor’s perimeter. Because of the high contrast, the Leontovich boundary condition [4, 5] can be applied: \( \epsilon_{p,q,r} \nu_q, \hat{E}_r^A \approx \hat{Z}_c \epsilon_{p,q,r} \nu_q \partial J^A_n \), where \( \hat{Z}_c = \sqrt{j \omega \mu (j \omega \varepsilon + \sigma)^{-1}} \) is the wave impedance of the conductor. The advantage of this boundary condition is that only the fields at the surface need to be considered. Substitution of these boundary conditions in (D.5) yields

\[
\hat{U}_i^E \approx -\frac{1}{\hat{I}_i^B} \int_{x \in \partial D_O} (\hat{Z}_c \hat{H}_m^B + \hat{E}_m^B) \partial J^A_m dA. \tag{D.6}
\]

This is an integral over the conductor (e.g., an external antenna) of the external radiator, where \( \partial J^A \) is the surface current through this conductor. The fields \( \{ \hat{H}_m^B, \hat{E}_m^B \} \)
are radiated by the interconnect due to an applied unit current source $I^B_i$, while the external radiator is absent. For a good conductor $Z_c$ vanishes, so that only the radiated electric field $E_m^{Bi}$ needs to be considered.

### D.3 Calculation of the Thevenin Voltages for an Unknown Radiator

EMC regulations often specify only the external electromagnetic fields a system must be able to resist and rarely its source, so that (D.6) is not applicable. To derive an expression for the induced voltage in this situation, the boundary surface $\partial D_O$ is chosen to be surface of the conductors of the interconnect (i.e., the receiver). Again we define a surface currents as the tangential fields radiated by the interconnect in state $B$: $\partial j_n^{Bi} = -\epsilon_{n,m,p} \nu_m \hat{H}_p^{Bi}$, where we the minus sign accounts for the orientation of the normal vector, which in Figure D.1 is directed inwards the conductors of the interconnect. With the Leontovich boundary condition the induced voltage can be expressed as

$$\hat{U}_E^i \approx -\frac{1}{I^B_i} \int_{x \in \partial D_O} (\hat{Z}_c \hat{H}_m^A + \hat{E}_m^A) \partial j_m^{Bi} dA,$$

(D.7)

where $\partial j_m^{Bi}$ is the surface current due to a current source $I^B_i$ applied at port $i$ in state $B$ and $\hat{Z}_c$ is the wave impedance of the conductor of the interconnect. The fields $\{ \hat{H}_m^A, \hat{E}_m^A \}$ are the fields generated by the unknown external source or as defined by an EMC standard.

In the thin wire approximation, with a good (metal) conductors ($\hat{Z}_c \approx 0$), this integral reduces to:

$$\hat{U}_E^i \approx -\frac{1}{I^B_i} \int_{x \in \partial D_O} \hat{E}_m^A i_m^{Bi} dl,$$

(D.8)

where $\hat{I}_m^{Bi}$ is the current through the thin conductors. In the low frequency approximation, the current through the conductor is constant so that (D.8) reduces to

$$\hat{U}_E^i \approx -\int_{x \in \partial D_O} \hat{E}_m^A \tau_m dl.$$  

(D.9)

This is the well known line integral from electrostats, to calculate the voltage induced over a conductor.

Thus interconnect, in the presence of an externally generated EM field, can be represented as Thevenin source. This representation assumes a weak coupling, so that the influence of the interconnect on the radiator is ignored. In a similar manner, a Norton current source description can be derived.
Bibliography


Appendix E

Analytic Expressions for the Mutual Inductance between Interconnections

For design and optimization of an EM compatible layout, analytical expressions of the inductive coupling between interconnections are required. Grover [1] describes this coupling for some common geometries, but assumes an infinite length of the conductors and lists the inductance per unit length. This appendix describes an analytical approximation for the inductive coupling between conductors with a geometry that is common in printed for circuit boards integrated circuits. We derive these expressions for interconnection with and without a shielding plane nearby.

E.1 Mutual Inductance in the Absence of a Shielding-Plane

To determine the mutual inductance between circuits, Equation (5.43) needs to be evaluated. This integral however cannot always be evaluated analytically. To over-

![Figure E.1: Approximation of coupled circuits.](image-url)
come this problem, a piecewise straight wire approximation of the layout geometry is made. Consider for example the circuit depicted in Figure E.1. The dotted line indicates the piece wise straight wire approximation of the conductors. The contribution of each straight wire to the total mutual inductance can be determined analytically. Let the contribution of wire piece $i$ and $j$ of two loops 1 and 2 be denoted by $L_{1,2;i,j}$, then the total inductance is given by:

$$L_{1,2} \approx \sum_{i=1}^{n} \sum_{j=1}^{m} L_{1,2;i,j} \quad (E.1)$$

The direction of the currents must be taken into account: the contribution of pieces in parallel is negative and of those that are anti parallel is positive. The contribution of those that are orthogonal is zero. An analytical expression can be derived for pieces of wires in parallel. The mutual inductance of the two pieces in Figure E.2 is given by:

$$L_{1,2;1,2} = \frac{\mu}{8\pi} \left[ 2(d_1 - d_2 + d_3 - d_4) 
- (l_1 + l_2 - 2r_2) \ln(2d_2 - l_1 - l_2 + 2r_2) 
+ (-l_1 + l_2 - 2r_2) \ln(2d_3 + l_1 - l_2 + 2r_2) 
+ (l_1 - l_2 - 2r_2) \ln(2d_1 - l_1 + l_2 + 2r_2) 
+ (l_1 + l_2 + 2r_2) \ln(2d_4 + l_1 + l_2 + 2r_2) \right], \quad (E.2)$$

Figure E.2: Inductance contribution of two pieces of wire.
where \( d_1 \cdots d_4 \) are the distances between the endpoints of the wires pieces:

\[
d_1 = \sqrt{r_1^2 + \left(-\frac{l_1}{2} + \frac{l_2}{2} + r_2\right)^2} \quad (E.3)
\]
\[
d_2 = \sqrt{r_1^2 + \left(-\frac{l_1}{2} - \frac{l_2}{2} + r_2\right)^2} \quad (E.4)
\]
\[
d_3 = \sqrt{r_1^2 + \left(\frac{l_1}{2} - \frac{l_2}{2} + r_2\right)^2} \quad (E.5)
\]
\[
d_4 = \sqrt{r_1^2 + \left(\frac{l_1}{2} + \frac{l_2}{2} + r_2\right)^2} \quad (E.6)
\]

, where \( r_1 \) and \( r_2 \) are the horizontal and vertical components of \( r \). These expressions can be used to derive an analytical approximation of the inductive coupling, when the distance between the wires is larger than their radius. Grover [1] assumes an infinitely long wire and determines the inductance per unit length. To verify our expression, we compare the mutual inductance \( L_{1,2} \) per unit length predicted by (E.2) for infinitely long wires in parallel and compare that with the expression given by Grover. From Equation (E.2) this inductance is given by:

\[
L_{1,2} = \frac{1}{l} L_{1,2;1,2} = \frac{1}{l} \frac{\mu}{8\pi} \left[ 4(r - \sqrt{r^2 + l^2}) + 2l \ln \left( \frac{\sqrt{r^2 + l^2} + l}{\sqrt{r^2 + l^2} - l} \right) \right] \quad (r \ll l) \\
\approx \frac{\mu}{4\pi} \left[ -2 + \ln \left( 2 + \frac{4}{r^2} \right) \right], \quad (E.7)
\]

where \( l \) is the length and \( r \) the distance between the conductors. This is exactly the mutual inductance listed in Grover [1].

The self-inductance \( L_{ii} \) is more difficult to find, because then the current distribution must be taken into account. Approximation for many geometries are described by Grover [1]. As a rule of thumb, \( 1nH \) for each \( mm \) of wire length is used in many books on EMC like [2, 3]. This rule of thumb is applicable to wires with a cross section of \( 0.5 \cdots 2 mm^2 \) that are part of a loop much larger than their diameter. For much thinner connections, like those in integrated circuits, the inductance can be higher.

### E.2 Mutual Inductance in the Presence of a Shielding-Plane

Often a shielding-plane is present in the form of a low ohmic substrate for integrated circuits or a ground-plane for printed circuit boards. These shielding-planes reduce the inductive coupling. This section determines this reduction.

The current flowing in the image (see Figure 5.20) of the loop in the shielding-plane has an opposite direction and reduces part of the radiated magnetic field. Figure E.3 show two coupled loops with a shielding-plane. The mutual inductive coupling between two loops above a ground plane can be approximated by:

\[
L_{i,j} = \mu \oint_{x \in \partial C_1} \oint_{x' \in \partial C_2} \frac{\tau_n(x)\tau_n(x')}{4\pi} \left( \frac{1}{|x - x'|} - \frac{1}{|x - x' - 2t_3|} \right) ddll', \quad (E.8)
\]

where \( t \) is the thickness of the substrate between the loop and shielding-plane. The mutual inductance contribution of two pieces of wire in two different loops (E.2) is
now reduced to:

\[ L_{1,2;1,2} \approx \frac{\mu t^2}{2\pi r_1^2} (-d_1 + d_2 - d_3 + d_4), \]  

(E.9)

where it is assumed that \( t \ll r_1 \). Thus a considerable reduction in coupling can be obtained with a shielding-plane if the distance between the shielding place and loops is much smaller than the distance between the loops.
Bibliography


Appendix F

A Proof that any Cable With a Non-Closed Shield Radiates

A coaxial cable with a perfect conducting shield does not radiate, because the outer conductor shields the transported EM wave (signal). In practice, such an implementation is often technically not feasible. Therefore an approximation of a shielded implementation is made, for example with the help of a ground plane. The question is, is it possible to eliminate radiation and reception with such an approximation? In this appendix we will proof that this is not possible without closing the shield. However, a good approximation can be obtained.

To prove this, the condition for a non radiating construction is determined with the help of Huygens Principle [1]. Because of reciprocity, a non radiating configuration also cannot receive signals. Figure F.1 show a part of a two conductor radiation free interconnection. For such an interconnection, the fields generated by the electric current density $\hat{J}^I$ through the inner conductor are fully compensated by the electric current density $\hat{J}^O$ through the outer conductor. If the outer conductor is closed,
generated by sources behind a closed surface that divides the configuration space in two disjoint regions, can be represented as due to equivalent surface sources located on that surface (see also [2, 3, 4]). Reversing the direction of these equivalent surface sources, results in a field that exactly compensates the fields generated by the sources behind that surface (e.g., the currents through the inner conductor). A method to find the current density $\hat{J}^O$ that fully compensates these fields, is described in [5] (pages 870-878).

The reason that only a closed surface around the inner conductor can compensate the field is that the required surface current density $\hat{J}^O$ for a particular closed surface is unique. Assume that a second distribution $\hat{J}^{O'}$ exists that would generate exactly the same compensating fields. Because the electromagnetic fields are a linear function of the current vector potential $\Phi^J(x)$ (see [5] (page 716, formula 25.1-7)), subtraction of the current vector potentials, generated by these two current distributions must result in a zero vector potential:

$$\Phi^J_n(x) = \int_{x' \in D^O} \hat{J}^O_m(x') \hat{G}^{\Phi;J}_{n,m}(x,x')dV$$

$$- \int_{x' \in D^O} \hat{J}^{O'}_m(x') \hat{G}^{\Phi;J}_{n,m}(x,x')dV$$

$$= \int_{x' \in D^O} [\hat{J}^O_m(x') - \hat{J}^{O'}_m(x')] \hat{G}^{\Phi;J}_{n,m}(x,x')dV = 0 \quad (F.1)$$

for all $x$ outside the closed outer conductor surface domain $D^O$. The function $\hat{G}^{\Phi;J}_{n,m}(x,x')$ is the Greens tensor function of the current vector potential.

Equation (F.1) must even be true at the surface itself, therefore $\hat{J}^O(x') - \hat{J}^{O'}(x')$ must be zero. Hence the required current distribution is unique. A non closed outer conductor like the connection depicted in Figure F.2, is not a closed surface, thus cannot provide the required unique current distribution to compensate the fields radiated by the currents through the inner conductor.

![Figure F.2: Partial cancellation of fields in non radiation free connection.](image)
Bibliography

[1] C. Huygens, *Trait de la lumiere; o sont expliques les causes de ce qui luy arrive dans la reflexion et dans la refraction et particulierement dans l'irrange refraction du cristal d'Islande; avec un discours de la cause de la pesanteur*. Leide : Van der Aa (Pierre), 1690.


Appendix G

Numerical Implementation of a Loop Antenna Impedance Extraction

As explained in Section 7.1.3, for an accurate extraction of an equivalent circuit from a layout, one needs to take into account the total EM-energy exchange between a component and the circuit layout it is part of. Both have to be included in the EM simulation that is used for this extraction. We therefore use the circuit components to “measure” in simulation the impedances of the equivalent circuit of the layout. In this appendix we discuss the numerical implementation of the example treated in Section 7.4. For this example, the impedance extraction (see Section 7.1.3) requires two simulations: one of the component in free space, and one with the component connected to the loop antenna. The first simulation is required to determine the impedance of the component itself, and can be considered a calibration of the measurement device. In both simulations, the component is used as an excitation source by defining the current that flows through the component as a predefined boundary condition. The impedances are determined from the total power that is delivered by the component. The first step is a straightforward calculation, therefore we will discuss the second step only.

The power delivered by component is calculated in two steps: first the current that component induces in the antenna is calculated, and next the power that is delivered by the component is calculated from the EM fields that are generated by the currents flowing through the antenna and the component. To reduce aliasing errors caused by the finite grid, we apply a spatial anti aliasing filter as described in Appendix H (see also [1, 2, 3]). The matrix is solved with the help of the conjugate gradient method that was developed by van der Berg and Zwamborn [4, 5]. In the following sections we discuss the mathematical formulation of the problem and the numerical implementation. The simulation results are discussed in Section 7.4.
G.1 Mathematical Formulation of the Simulation Problem

Figure G.1 shows the simulated antenna configuration. In this figure $D_C$ is the domain of the antenna conductor and $\partial D_C$ is the surface of this conductor, for which the electric surface current density $\partial \mathbf{J}$ has to be solved. The domain $D_S$ is the domain of the component (excitation source), which in this figure is a continuation of the strip conductor of the loop antenna. The vector $\nu$ is the normal vector on the surfaces $\partial D_C$ and $\partial D_S$. The surface current is solved from the integral Equation (7.17), which is solved in the cylinder coordinate system $(\rho, \varphi)$, where $\rho$ is the radius measured from the center of the loop, and $\varphi$ the angle measured from the center of the source domain. It must be noted that because of this coordinate system, no tensor notation is applied in this appendix. The integral equation in cylinder coordinates equals

$$-\hat{E}_\rho^i = \hat{\eta}^{-1} \partial_\rho \hat{B}_\rho - \hat{\zeta} \hat{\Phi}_\rho^j$$

$$-\hat{E}_\varphi^i = \hat{\eta}^{-1} \partial_\varphi \hat{B}_\varphi - \hat{\zeta} \hat{\Phi}_\varphi^j,$$ (G.1)

$$-\hat{E}_\rho^i = \hat{\eta}^{-1} \partial_\rho \hat{B}_\rho - \hat{\zeta} \hat{\Phi}_\rho^j$$

$$-\hat{E}_\varphi^i = \hat{\eta}^{-1} \partial_\varphi \hat{B}_\varphi - \hat{\zeta} \hat{\Phi}_\varphi^j,$$ (G.2)

where $\hat{\eta} = s \varepsilon + \sigma$ and $\hat{\zeta} = s \mu$. The parameters $\varepsilon, \sigma, \mu$ are the permittivity, conductivity and permeability of the medium in domain $D'$ and $s$ is the Laplace variable. We assume a homogenous isotropic medium. The vector function $\{\hat{B}_\rho, \hat{B}_\varphi\}$ equals

$$\hat{B}_\rho = \rho^{-1} [\partial_\rho (\rho \hat{\Phi}_\rho^j) + \partial_\varphi \hat{\Phi}_\varphi^j]$$

$$\hat{B}_\varphi = \rho^{-1} \hat{B}_\rho.$$ (G.3)

(G.4)

The current vector potential $\{\hat{\Phi}_\rho^j, \hat{\Phi}_\varphi^j\}$ equals

$$\hat{\Phi}_\rho^j(\rho, \varphi) = \int_{\rho', \varphi' \in \partial D_c} \left[ \hat{G}_{\rho, \rho}^{\rho, \rho}(\rho, \varphi, \rho', \varphi') \partial J_\rho(\rho', \varphi') \right. \left. + \hat{G}_{\rho, \varphi}^{\rho, \varphi}(\rho, \varphi, \rho', \varphi') \partial J_\varphi(\rho', \varphi') \right] \rho' d(\rho', \varphi')$$ (G.5)

$$\hat{\Phi}_\varphi^j(\rho, \varphi) = \int_{\rho', \varphi' \in \partial D_c} \left[ \hat{G}_{\varphi, \rho}^{\varphi, \rho}(\rho, \varphi, \rho', \varphi') \partial J_\rho(\rho', \varphi') \right. \left. + \hat{G}_{\varphi, \varphi}^{\varphi, \varphi}(\rho, \varphi, \rho', \varphi') \partial J_\varphi(\rho', \varphi') \right] \rho' d(\rho', \varphi'),$$ (G.6)
where the \( \hat{G} \) functions are Green’s functions that for a homogeneous medium equal

\[
\hat{G}^{\rho,\rho} = \hat{G}^{\varphi,\varphi} = \frac{\exp(-\hat{\gamma} d)}{4d} \cos(\varphi - \varphi') \tag{G.7}
\]

\[
\hat{G}^{\rho,\varphi} = -\hat{G}^{\varphi,\rho} = \frac{\exp(-\hat{\gamma} d)}{4d} \sin(\varphi - \varphi'), \tag{G.8}
\]

where \( \hat{\gamma} = \sqrt{\hat{\eta} \hat{\zeta}} \) the propagation constant of the medium and

\[
d = \sqrt{\rho^2 + \rho'^2 - \rho \rho' \cos(\varphi - \varphi')} \]

the distance between the points \((\rho, \varphi)\) and \((\rho', \varphi')\).

In equation (G.1) and (G.2), \( \{\hat{E}_\rho, \hat{E}_\varphi\} \) is the incident electric field that is generated by the excitation source (i.e., the circuit component). This integral equation relates this known field to the unknown surface current for every point on the surface of the stripline conductor. The unknown current therefore can be solved from this equation.

### G.2 Matrix-Form Formulation of the Simulation Problem

To prevent aliasing errors due to discretization of the integral equations, a spatial aliasing filter is applied to left and right hand side of the integral equations (G.1) and (G.2). In Appendix H it is shown that this can be implemented by weakening the Greens kernels (G.7) and (G.8) of the integral equation and that are used to determine the incident field \( \hat{E}_i \). We applied the weakened Greens kernel as given by (H.25).

To translate the integral equations (G.1) and (G.2) into a matrix form, we apply the procedure discussed in Section 7.3.1.

![Figure G.2: Rooftop expansion functions](image)

For expansion of the current and fields, and weighting of the integral equations, we follow the procedure of Zwamborn [5] and apply rooftop expansion functions (see Figure G.2). These expansion functions result in a piece-wise linear approximation of the field and current in one direction and a stepwise approximation in the other direction. The piece-wise linear approximation is used in the direction where the derivative of the field or current needs to be evaluated, so that the same numerical accuracy is obtained for both directions. To describe these rooftop function mathematically, we define a pulse and the triangle function. The pulse function \( \Pi(y|\Delta y) \) is defined as:
\[
\Pi(y|\Delta y) = \begin{cases} 
1 & \text{if } -\frac{1}{2}\Delta y < y < \frac{1}{2}\Delta y, \\
\frac{1}{2} & \text{if } |y| = \frac{1}{2}\Delta y, \\
0 & \text{elsewhere.}
\end{cases}
\] (G.9)

The triangular function \(\Lambda(y|\Delta y_1, \Delta y_2)\), with support \(\Delta y_1 + \Delta y_2\) is defined as:

\[
\Lambda(y|\Delta y_1, \Delta y_2) = \begin{cases} 
1 + \frac{y}{\Delta y_1} & \text{for } -\Delta y_1 < y \leq 0 \\
1 - \frac{y}{\Delta y_2} & \text{for } 0 < y < \Delta y_2 \\
0 & \text{elsewhere.}
\end{cases}
\] (G.10)

Using these functions, the rooftop functions are defined as follows:

\[
\psi_{\rho; m\rho, m\varphi}(\rho, \varphi|\Delta \rho_{m\rho}, \Delta \varphi_{m\varphi}) = \Pi(\varphi - \varphi_{m\varphi} + \frac{y}{2}\Delta \varphi_{m\varphi}|\Delta \varphi_{m\varphi}) \Lambda(\rho - \rho_{m\rho}|\Delta \rho_{m\rho}, \Delta \rho_{m\rho+1}) \\
\psi_{\varphi; m\rho, m\varphi}(\rho, \varphi|\Delta \rho_{m\rho}, \Delta \varphi_{m\varphi}, \Delta \varphi_{m\varphi+1}) = \Pi((\rho - \rho_{m\rho} + \frac{y}{2}\Delta \rho_{m\rho}|\Delta \rho_{m\rho}) \Lambda((\varphi - \varphi_{m\varphi}|\Delta \varphi_{m\varphi}, \Delta \varphi_{m\varphi+1}) \\
\] (G.11)

To enable a numerical comparison of the left and right hand side of the integral equations (G.1) and (G.2) with a finite number of points, both sides are weighted by these rooftop functions. This integral equations are approximated as follows:

\[
\int_{(\rho, \varphi) \in D_C} \hat{E}_\rho(\rho, \varphi) \psi_{\rho; k\rho, k\varphi}(\rho, \varphi) \rho d(\rho, \varphi) = \hat{\eta}^{-1} \int_{(\rho, \varphi) \in D_C} [\hat{B}_\rho(\rho, \varphi) \partial_\rho(\rho \psi_{\rho; k\rho, k\varphi}(\rho, \varphi)) + \hat{\zeta} \hat{G}_\rho(\rho, \varphi)(\rho \psi_{\rho; k\rho, k\varphi}(\rho, \varphi))] d(\rho, \varphi) \\
\] (G.13)

\[
\int_{(\rho, \varphi) \in D_C} \hat{E}_\varphi(\rho, \varphi) \psi_{\varphi; k\rho, k\varphi}(\rho, \varphi) \rho d(\rho, \varphi) = \hat{\eta}^{-1} \int_{(\rho, \varphi) \in D_C} [\hat{B}_\varphi(\rho, \varphi) \partial_\varphi(\rho \psi_{\varphi; k\rho, k\varphi}(\rho, \varphi)) + \hat{\zeta} \hat{G}_\varphi(\rho, \varphi)(\rho \psi_{\varphi; k\rho, k\varphi}(\rho, \varphi))] d(\rho, \varphi). \\
\] (G.14)

We assume that the surface current density vanishes at the edges of the conductor, so that one partial differential operator can be moved to a weighting function, thereby relaxing the required numerical accuracy. Equations (G.13) and (G.14) become:

\[
\int_{(\rho, \varphi) \in D_C} \hat{E}_\rho(\rho, \varphi) \psi_{\rho; k\rho, k\varphi}(\rho, \varphi) \rho d(\rho, \varphi) = \hat{\eta}^{-1} \int_{(\rho, \varphi) \in D_C} [\hat{B}_\rho(\rho, \varphi) \partial_\rho(\rho \psi_{\rho; k\rho, k\varphi}(\rho, \varphi)) + \hat{\zeta} \hat{G}_\rho(\rho, \varphi)(\rho \psi_{\rho; k\rho, k\varphi}(\rho, \varphi))] d(\rho, \varphi) \\
\] (G.15)
\[
\int_{(\rho,\varphi)\in D_C} \hat{E}_i^j(\rho, \varphi) \psi_{\varphi; k_p, k_{\varphi}}(\rho, \varphi) \rho d(\rho, \varphi) = \tilde{\eta}^{-1} \int_{(\rho,\varphi)\in D_C} [\hat{B}_q(\rho, \varphi) \partial_\varphi \psi_{\varphi; k_p, k_{\varphi}}(\rho, \varphi) + \hat{G}_q(\rho, \varphi) \psi_{\varphi; k_p, k_{\varphi}}(\rho, \varphi)] \rho d(\rho, \varphi)
\]

(G.16)

The electric field and the surface current density is approximated by a finite expansion over the rooftop functions, to enable a numerical representation:

\[
\partial \hat{J}_p(\rho, \varphi) \approx \sum \partial \hat{J}_{p; n_p, n_\varphi} \psi_{\rho; n_p, n_\varphi}(\rho, \varphi)
\]

(G.17)

\[
\partial \hat{J}_\varphi(\rho, \varphi) \approx \sum \partial \hat{J}_{\varphi; n_p, n_\varphi} \psi_{\varphi; n_p, n_\varphi}(\rho, \varphi)
\]

(G.18)

\[
\hat{E}_i^j(\rho, \varphi) \approx \sum \hat{E}_{i; n_p, n_\varphi} \psi_{\rho; n_p, n_\varphi}(\rho, \varphi)
\]

(G.19)

\[
\hat{E}_{\varphi}^j(\rho, \varphi) \approx \sum \hat{E}_{\varphi; n_p, n_\varphi} \psi_{\varphi; n_p, n_\varphi}(\rho, \varphi)
\]

(G.20)

With the rooftop expansion functions, the “sample” values are defined as follows:

\[
\partial \hat{J}_{p; n_p, n_\varphi} = \partial \hat{J}_p(\rho_{n_p}, \varphi_{n_\varphi} - \frac{1}{2} \Delta \varphi_{n_\varphi})
\]

(G.21)

\[
\partial \hat{J}_{\varphi; n_p, n_\varphi} = \partial \hat{J}_\varphi(\rho_{n_p}, \varphi_{n_\varphi} - \frac{1}{2} \Delta \varphi_{n_\varphi})
\]

(G.22)

\[
\hat{E}_{i; n_p, n_\varphi} = \hat{E}_i^j(\rho_{n_p}, \varphi_{n_\varphi} - \frac{1}{2} \Delta \varphi_{n_\varphi})
\]

(G.23)

\[
\hat{E}_{\varphi; n_p, n_\varphi} = \hat{E}_{\varphi}^j(\rho_{n_p}, \varphi_{n_\varphi} - \frac{1}{2} \Delta \varphi_{n_\varphi})
\]

(G.24)

Substitution of these current and field expansions into (G.15) and (G.16) yields the desired matrix representation. To ensure that numerical errors are not increased for very small grid sizes, each point on the left and right hand side of (G.15) and (G.16) are normalized to the volume of the rooftop expansion function at that point. This yield the following matrix equation:

\[
\frac{1}{6} \left( \frac{\Delta \rho_{k_p}}{\Delta \rho_{k_p} + \Delta \rho_{k_p+1}} \hat{E}_{i; k_p, k_{\varphi} - 1, k_{\varphi}} + 4 \hat{E}_{i; k_p, k_{\varphi}} + \frac{\Delta \rho_{k_p+1}}{\Delta \rho_{k_p} + \Delta \rho_{k_p+1}} \hat{E}_{i; k_p, k_{\varphi} + 1, k_{\varphi}} \right) = \hat{\Phi}_{i; k_p, k_{\varphi}} + \frac{2 \eta^{-1}}{\Delta \rho_{k_p} + \Delta \rho_{k_p+1}} \left( \hat{\Phi}_{i; k_p-1, k_{\varphi}} - \frac{\Delta \rho_{k_p}}{\Delta \rho_{k_p} + \Delta \rho_{k_{\varphi}} + 1} \ln \left( \frac{\Delta \rho_{k_p}}{\rho_{k_p} - \Delta \rho_{k_p}} \right) \right)
\]

\[
\left\{ \begin{array}{l}
\frac{1}{\Delta \rho_{k_p}} \left[ \frac{\rho_{k_p}}{\Delta \rho_{k_p}} \ln \left( 1 - \frac{\Delta \rho_{k_p}}{\rho_{k_p}} \right) + 2 \right] \\
+ \frac{2}{\Delta \rho_{k_p} + \Delta \rho_{k_p+1}} \left( \rho_{k_p} - \Delta \rho_{k_p} \right) \ln \left( 1 + \frac{\Delta \rho_{k_p+1}}{\rho_{k_p}} \right) \\
\frac{1}{\Delta \rho_{k_p+1}} \ln \left( 1 + \frac{\Delta \rho_{k_p+1}}{\rho_{k_p}} \right) - 2
\end{array} \right\}
\]

\[
+ \frac{2 \eta^{-1}}{\Delta \rho_{k_{\varphi}} (\Delta \rho_{k_p} + \Delta \rho_{k_{\varphi}+1})} \left[ (\hat{\Phi}_{i; k_p, k_{\varphi}} - \hat{\Phi}_{i; k_p, k_{\varphi} - 1}) \right] . \left( \hat{\Phi}_{i; k_p+1, k_{\varphi} - 1} - \hat{\Phi}_{i; k_p+1, k_{\varphi} - 1} \right) \cdot \left[ \begin{array}{c}
\frac{1}{\Delta \rho_{k_p}} \ln \left( 1 - \frac{\Delta \rho_{k_p}}{\rho_{k_p}} \right) \\
\frac{1}{\Delta \rho_{k_p+1}} \ln \left( 1 + \frac{\Delta \rho_{k_p+1}}{\rho_{k_p}} \right)
\end{array} \right]
\]

(G.25)
\[
\frac{1}{6} \left( \frac{\Delta \varphi_{k\varphi}}{\Delta \varphi_{k\varphi} + \Delta \varphi_{k\varphi+1}} \hat{E}_i^{k\varphi;k\varphi-1} + 4 \hat{E}_i^{k\varphi;k\varphi+1} \frac{\Delta \varphi_{k\varphi+1}}{\Delta \varphi_{k\varphi} + \Delta \varphi_{k\varphi+1}} \right) + 2 \hat{G}_i^{k\varphi;k\varphi} = \left( \frac{1}{\Delta \varphi_{k\varphi}} \right) \frac{\hat{E}_i^{k\varphi;k\varphi}}{\Delta \varphi_{k\varphi+1}} \]}

\[
\hat{E}_i^{k\varphi;k\varphi} = \frac{1}{(\Delta \varphi_{k\varphi} + \Delta \varphi_{k\varphi+1}) \rho_{k\varphi} \Delta \rho_{k\varphi}} \left( 1 - \frac{\rho_{k\varphi} \Delta \rho_{k\varphi}}{\rho_{k\varphi} \Delta \rho_{k\varphi}} \right)
\]

\[
\left( \hat{\Phi}_{k\varphi;k\varphi-1}, \hat{\Phi}_{k\varphi;k\varphi}, \hat{\Phi}_{k\varphi;k\varphi+1} \right) \approx \left( \frac{1}{\Delta \varphi_{k\varphi}} + \frac{1}{\Delta \varphi_{k\varphi+1}} \right) \left( \frac{1}{\Delta \varphi_{k\varphi}} \right) \left( \frac{1}{\Delta \varphi_{k\varphi+1}} \right) \]}

\[
\frac{2 \hat{G}_i^{k\varphi;k\varphi+1}}{(\Delta \varphi_{k\varphi} + \Delta \varphi_{k\varphi+1}) \rho_{k\varphi} \Delta \rho_{k\varphi}} \left( \frac{1 - \frac{\rho_{k\varphi} \Delta \rho_{k\varphi}}{\rho_{k\varphi} \Delta \rho_{k\varphi}}}{1 - \frac{\rho_{k\varphi} \Delta \rho_{k\varphi}}{\rho_{k\varphi} \Delta \rho_{k\varphi}}} \right) \]}

\[
\left( \hat{\Phi}_{k\varphi;k\varphi-1} - \hat{\Phi}_{k\varphi;k\varphi+1} \right) \Delta S = \frac{1}{(\Delta \varphi_{k\varphi} + \Delta \varphi_{k\varphi+1}) \rho_{k\varphi} \Delta \rho_{k\varphi}} \left( \frac{1 - \frac{\rho_{k\varphi} \Delta \rho_{k\varphi}}{\rho_{k\varphi} \Delta \rho_{k\varphi}}}{1 - \frac{\rho_{k\varphi} \Delta \rho_{k\varphi}}{\rho_{k\varphi} \Delta \rho_{k\varphi}}} \right) \]}

The current vector sample values in this equation are approximated by the following numerical integrals:

\[
\hat{\Phi}_{k\varphi;k\varphi} \approx \sum_{n\varphi,n\varphi} \hat{G}_{k\varphi;k\varphi,n\varphi,n\varphi} \partial \hat{J}_{k\varphi,n\varphi,n\varphi} \Delta S
\]

\[
\hat{\Phi}_{k\varphi;k\varphi} \approx \sum_{n\varphi,n\varphi} \hat{G}_{k\varphi;k\varphi,n\varphi,n\varphi} \partial \hat{J}_{k\varphi,n\varphi,n\varphi} \Delta S
\]

where \( \Delta S \) is the area of each patch. The Greens functions that are used to calculate these current vector potentials are defined as follows.

\[
\hat{G}_{m\varphi,m\varphi,n\varphi,n\varphi} \approx \cos(\varphi_{m\varphi} - \frac{1}{2} \Delta \varphi_{m\varphi} - \varphi_{n\varphi} + \frac{1}{2} \Delta \varphi_{n\varphi})
\]

\[
\hat{G}_{m\varphi,m\varphi,n\varphi,n\varphi} \approx \sin(\varphi_{m\varphi} - \frac{1}{2} \Delta \varphi_{m\varphi} - \varphi_{n\varphi}) \hat{G}(d_{m\varphi,m\varphi,n\varphi,n\varphi})
\]

\[
\hat{G}_{m\varphi,m\varphi,n\varphi,n\varphi} \approx - \sin(\varphi_{m\varphi} - \varphi_{n\varphi} + \frac{1}{2} \Delta \varphi_{n\varphi}) \hat{G}(d_{m\varphi,m\varphi,n\varphi,n\varphi})
\]

\[
\hat{G}_{m\varphi,m\varphi,n\varphi,n\varphi} \approx \cos(\varphi_{m\varphi} - \varphi_{n\varphi}) \hat{G}(d_{m\varphi,m\varphi,n\varphi,n\varphi})
\]

where \( d_{l\varphi,l\varphi,n\varphi,n\varphi} \) are the distances between the grid point and \( [\hat{G}(d)] \) is the weakened Greens function defined by (H.25).
To solve this matrix equation, the conjugate gradient algorithm of van der Berg and Zwamborn [5] has been applied. This is an iterative algorithm that guarantees convergence to the desired answer. The advantages of this algorithm are its memory efficiency, stability and that the remaining error is used as a termination criteria of the iteration loop, so that accuracy is guaranteed. We defined the matrix definitions (G.25) and (G.26) as operators, that can be evaluated on the fly in simulation. The algorithm of van der Berg and Zwamborn requires only this operator and the adjoint of this operator to determine the induced surface currents. Therefore the total matrix does not need to be stored in memory. The memory usage is a linear function of the number of grid points in stead of a quadratic function.
Bibliography


Appendix H

Suppression of Aliasing Errors in EM Field Simulations

Computer simulations of electromagnetic problems require that the fields and currents are represented by a finite number of samples. The domain that is sampled depends on the expansion functions that are applied for representation of the fields and currents. For example pulse shaped expansion functions results in spatial sampling, sine and cosine expansion functions results in frequency domain sampling. In either case, the sampling can cause aliasing errors. Hence, a spatial anti aliasing filter is required before sampling [1] to prevent simulation errors. In the following sections we determine the cause of aliasing errors and propose an optimal spatial filter technique, which is adapted to the grid spacing. Simulation results that demonstrate the accuracy improvements are shown in Section 7.3.2.

H.1 The Cause of Aliasing Errors

In this section we analyze the cause of aliasing errors with the help of the source type representation of EM fields. This representation formulates the EM fields as a convolution of the electric currents that generate the EM fields and Green’s functions for the surrounding medium. For an isotropic and homogeneous medium, the EM fields can be formulated as follows [2]:

\[
\hat{E}_k(x, j\omega) = \hat{\eta}^{-1} \left[ \partial_k \partial_p \hat{\Phi}^J_p(x, j\omega) - \hat{\gamma}^2 \hat{\Phi}^I_p(x, j\omega) \right]
\]

\[
\hat{H}_j(x, j\omega) = \epsilon_{j,r,s} \partial_r \hat{\Phi}^J_p(x, j\omega),
\]

where \( \hat{\eta} = j\omega \varepsilon + \sigma \), \( \varepsilon \) and \( \sigma \) the permittivity and the conductivity of the medium and \( \hat{\gamma} \) the propagation constant, which for a lossless domain equals \( \frac{j\omega}{c} \), where \( c \) is the phase velocity of the wave. The electric current vector potential \( \hat{\Phi}^J_p(x, j\omega) \) equals

\[
\hat{\Phi}^J_p(x, j\omega) = \int_{x'\in\Omega} J_p(x', j\omega) \frac{\exp(-\hat{\gamma}|x - x'|)}{4\pi|x - x'|} dV'.
\]

The other symbols in (H.1) through (H.3) have their usual meaning.
Aliasing errors are introduced in a numerical implementation of (H.1) and (H.2) when the current vector potential (H.3) is calculated. A closer inspection of (H.3) reveals that this equation can be written as a one-sided Fourier transform. Although this is quite uncommon in electromagnetic field theory, we will show that such a description can profitably be used to cope with aliasing errors. Therefore we average the current density \( J \) that generates the EM fields over a sphere around a point \( x \) where the EM field is observed:

\[
\hat{Q}_p(x, r, j\omega) = r \frac{1}{4\pi r^2} \int_0^{2\pi} \int_0^\pi J_p(x, r, \varphi, \theta) \sin(\varphi) r^2 d\varphi d\theta,
\]

(H.4)

where

\[
J_p(x, r, \varphi, \theta) = J_p(x + i_1 r \sin(\varphi) \cos(\theta) + i_2 r \sin(\varphi) \sin(\theta) + i_3 r \cos(\varphi))
\]

(H.5)

The vectors \( i_1 \ldots i_3 \) are the orthogonal base vectors of the Cartesian reference frame. This function equals \( r \) times the average current density, averaged over a sphere around \( x \). With the aid of (H.4) the current vector potential (H.3) is rewritten as:

\[
\hat{\Phi}^J(x, j\omega) = \int_0^\infty \hat{Q}_p(x, j\omega, r) \exp(-j\frac{\pi}{c} r) dr.
\]

(H.6)

This is a Fourier integral. In a numerical implementation the current vector potential can be approximated as follows (trapezium rule):

\[
\hat{A}_p^*(x, j\omega) = \Delta r \sum_{i=1}^\infty \hat{Q}_p^*(x, j\omega, i\Delta r) \exp(-j\frac{\pi}{c} i\Delta r)
\]

\[
+ \Delta r \frac{1}{2} \hat{Q}_p^*(x, j\omega, 0),
\]

(H.7)

where \( \Delta r \) is the grid distance and \( \hat{Q}_p^* (x, j\omega, r) \) is the numerical approximation of \( \hat{Q}_p(x, j\omega, r) \). To find the aliasing error, this equation is reformulated as:

\[
\hat{A}_p^*(x, j\omega) = \Delta r \int_{-\infty}^{\infty} U(r) \hat{Q}_p^*(x, j\omega, r) \exp(-j\frac{\pi}{c} r)
\]

\[
\sum_{i=-\infty}^{\infty} \delta(r - i\Delta r) dr,
\]

(H.8)

where \( U(r) \) is defined as:

\[
U(r) = \begin{cases} 
0 & r < 0 \\
\frac{1}{2} & r = 0 \\
1 & r > 0 
\end{cases}
\]

(H.9)
With the help of standard Fourier transforms, (H.8) can be represented by the following convolution:

\[
\tilde{A}_p(x, j\omega) = \frac{\Delta c}{2\pi} \int_{-\infty}^{\infty} \tilde{A}_p(x, j(\omega - \omega')) \frac{2\pi c}{\Delta r} \sum_{n=-\infty}^{\infty} \delta(\omega' - n \frac{2\pi c}{\Delta r}) d\omega' = \sum_{n=-\infty}^{\infty} \tilde{A}_p(x, j(\omega - n \frac{2\pi c}{\Delta r})) , \tag{H.10}
\]

where \(\tilde{A}_p(x, j\omega)\) is defined as:

\[
\tilde{A}_p(x, j\omega) = \int_{0}^{\infty} \hat{Q}_p(x, r, j\omega) \exp(-j \frac{\omega}{c} r) dr. \tag{H.11}
\]

From (H.10) it is clear that the approximation \(\tilde{A}_p(x, j\omega)\) of \(\hat{\Phi}_J^p(x, j\omega)\) is a repetition of \(\tilde{A}_p(x, j\omega)\) in frequency domain. The surface current is real valued, this implies that for any point \(x\), \(\hat{\Phi}_J^p(x, j\omega) = \hat{\Phi}_J^p(x, -j\omega)\). Hence, if we ignore the errors due to overlap with the repeated spectra, \(\tilde{A}_p(x, j\omega)\) is only known for \(-\frac{\pi c}{\Delta r} < \omega < \frac{\pi c}{\Delta r}\). However the overlap cannot always be ignored in practice, and aliasing errors are introduced.

### H.2 Prevention of Aliasing Errors

To prevent aliasing errors in (H.10), the function \(\hat{Q}_p(x, r, j\omega)\) needs to be filtered such that \(\tilde{A}_p(x, j\omega)\) is forced to zero for \(|\omega| > \frac{\pi c}{\Delta r}\), while for \(|\omega| \leq \frac{\pi c}{\Delta r}\) the function \(\tilde{A}_p(x, j\omega)\) is not distorted. This implies \(\tilde{A}_p(x, j\omega)\) has to be multiplied by \(\Pi(\omega|\Delta\omega)\), defined as:

\[
\Pi(\omega|\Delta\omega) = \begin{cases} 
1 & |\omega| < \frac{1}{2} \Delta\omega \\
\frac{1}{2} & |\omega| = \frac{1}{2} \Delta\omega \\
0 & \text{elsewhere}
\end{cases} \tag{H.12}
\]

We define the filtered version of \(\hat{Q}(x, r, j\omega)\) as the convolution of \(\hat{Q}(x, r, j\omega)\) and some kind of filter function \(w(r)\):

\[
[\hat{Q}(x, r, j\omega)] = \int_{-\infty}^{\infty} U(r') \hat{Q}(x, r', j\omega) w(r - r') dr', \tag{H.13}
\]

where the brackets indicate the filtered version. From standard Fourier analyses it is known that \(w(r)\) is given by:

\[
w(r) = \frac{1}{2\pi c} \int_{-\infty}^{\infty} \Pi(\omega|\frac{2\pi c}{\Delta r}) \exp(j \frac{\omega}{c} r) d\omega = \frac{1}{\Delta r} \sin(\frac{2\pi r}{\Delta r}) \tag{H.14}
\]
Suppression of Aliasing Errors

The filtered current vector potential is given by:

\[
\hat{\Phi}_p(x, j\omega) = \int_{-\infty}^{\infty} \int_{-\infty}^{\infty} U(r') \hat{Q}_p(x, r', j\omega) w(r - r') U(r) \exp(-j\frac{\pi}{r} r) dr = \int_{-\infty}^{\infty} \hat{Q}_p(x, r', j\omega) U(r') \left[ \int_{-\infty}^{\infty} w(r - r') U(r) \exp(-j\frac{\pi}{r} r) dr \right] dr', \quad (H.15)
\]

where we have used the fact that \( w(r) \) is even. Two situations have to be distinguished: when the current density is known and the radiated fields are calculated, and the situation where an incident EM field is given and the induced electric currents need to be calculated. In the latter situation, the reverse operator is required. From (H.10) it is clear that for a correct numerical implementation of the aliasing filter, in the first situation the current must be filtered, while in the latter situation the incident EM field must be filtered. It must be noted that we are not talking about the bandwidth of the currents or fields in time domain but rather in spatial domain.

A commonly applied anti aliasing filter technique is the weakening of Green’s function. To determine the effect of this filtering on the accuracy, we introduce a weakened Green’s function as follows:

\[
\hat{G}(x, x', j\omega) = \int_{x'' \in \mathbb{R}^3} w(x'') \frac{\exp(-\frac{1}{4\pi}(x - x' + x''))}{4\pi |x - x' + x''|} dv'', \quad (H.16)
\]

where \( w(x'') \) is the filter function. When this Green’s function is applied in a numerical implementation, the current vector potential if filtered spatially after “sampling”:

\[
[\hat{A}_p(x)] = \Delta x_{1..3} \sum \sum \sum_{k,l,m=-\infty}^{\infty} j_p(x'_{k,l,m}, j\omega) \left[ \hat{G}(x, x'_{k,l,m}, j\omega) \right] = \int_{x'' \in \mathbb{R}^3} u(x'') \Delta x_{1..3} \sum \sum \sum_{k,l,m=-\infty}^{\infty} j_p(x'_{k,l,m}, j\omega) \hat{G}(x + x'', x'_{k,l,m}, j\omega) dv''
\]

\[
= \int_{x'' \in \mathbb{R}^3} u(x'') \hat{A}_p(x + x'') dv'', \quad (H.17)
\]

where

\[
x_{k,l,m} = i_1 k \Delta x_1 + i_2 l \Delta x_2 + i_3 m \Delta x_3 \quad (H.18)
\]

From (H.14) it is clear that for homogeneous isotropic media, the ideal filter function for a given grid spacing \( \Delta r \) is given by:

\[
w(r, \varphi, \theta) = \frac{1}{r \sin(\theta)} \delta(\theta) \frac{1}{r} \delta(\varphi) \frac{1}{\Delta r} \sin \left( \frac{\pi}{\Delta r} r \right) \quad (H.19)
\]

The use of this filter implies that also the calculated EM field is filtered. However, because it does not filter the current, the current distribution still needs an anti
aliasing filter. For solving the induced current from a given incident field however, this version of Green’s function suppresses aliasing errors in the calculated fields and currents, without decreasing the accuracy. This function could also be used to assign a filtered version of the incident field from a known current source in such a simulation. Another well known numerical problem is the singularity of Green’s function. In reality this problem does not exist, because the current density is a three dimensional spatial distribution. However, the numerical problem is caused by the necessary approximation of the current. A successful method to solve both, i.e. the aliasing and the singularity problem was shown by Van der Berg and Zwamborn [3] and [4]. In this procedure the fields assigned to the sample points are averaged over a sphere around the sample point. The filter function in (H.16) for this weakening process is given by:

\[
w(x) = \begin{cases} 
\frac{3}{4\pi(\Delta r)^2} & |x| \leq \Delta r \\
0 & \text{elsewhere}
\end{cases}
\]  

(H.20)

Because averaging over a ball means also averaging in the radius direction, the bandwidth is also limited. In the radius direction, the filter function for this kind of weakening is given by:

\[
w(r) = \frac{1}{2\Delta r} \Pi(r, 2\Delta r)
\]  

(H.21)

This results in the current vector potential multiplied by:

\[
W(\omega) = \frac{\sin(\hat{\gamma} \Delta r)}{\hat{\gamma} \Delta r}
\]  

(H.22)

Although this is not the ideal filter function as is given by (H.14), the largest part of the aliasing error is removed. The resulting weakened Green’s function is given by:

\[
[\hat{G}(d)]=
\begin{cases} 
1 - (1 + \hat{\gamma} \Delta \rho) \exp(-\hat{\gamma} \Delta \rho) & d = 0 \\
\hat{\gamma} d - (1 + \hat{\gamma} \Delta \rho) \exp(-\hat{\gamma} \Delta \rho) \sinh(\hat{\gamma} d) & 0 < d \leq \Delta \rho \\
\exp(-\hat{\gamma} d) \left[ \cosh(\hat{\gamma} \Delta \rho) - \frac{\sinh(\hat{\gamma} \Delta \rho)}{\hat{\gamma} \Delta \rho} \right] & d \geq \Delta \rho.
\end{cases}
\]  

(H.23)

Aliasing errors are best suppressed by the filter function given by (H.14). This function requires filtering over the entire space and cannot be normalized, therefore we approximate this function by a version that is limited to a radius \( R \). This filter function equals

\[
w(r) = \begin{cases} 
\frac{1}{\Delta r} \frac{\sin(\pi r)}{\pi r} & |r| \leq R \\
0 & |r| > R
\end{cases}
\]  

(H.24)
Suppression of Aliasing Errors

With this filter Green’s function becomes:

\[
G(r) = \frac{\left(\frac{\Delta r}{\bar{\gamma}}\right)^2}{4\left[\sin\left(\frac{\Delta r}{\bar{\gamma}} R\right) - \left(\frac{\Delta r}{\bar{\gamma}} R\right)\cos\left(\frac{\Delta r}{\bar{\gamma}} R\right)\right]} \cdot \frac{1}{\Delta r\left(\bar{\gamma}^2 + \left(\frac{\Delta r}{\bar{\gamma}}\right)^2\right)}
\]

\[
\begin{cases}
1 - \left(\frac{\Delta r}{\bar{\gamma}}\right) \sin\left(\frac{\Delta r}{\bar{\gamma}} R\right) + \cos\left(\frac{\Delta r}{\bar{\gamma}} R\right) & r = 0 \\
\left(r \frac{\Delta r}{\bar{\gamma}}\right)^{-1} \sin\left(r \frac{\Delta r}{\bar{\gamma}}\right) - \exp(-\bar{\gamma} r) \sinh(\bar{\gamma} r) & 0 < r \leq R \\
\frac{\exp(-\bar{\gamma} r)}{r} \left[\left(\frac{\Delta r}{\bar{\gamma}}\right)^{-1} \cos(\bar{\gamma} R) \sinh(\bar{\gamma} R) - \gamma^{-1} \sin(\bar{\gamma} R) \cos(\bar{\gamma} R)\right] & r > R
\end{cases}
\]

(H.25)

Figures H.1(a) and H.1(b) show the filtering results for \( R = \Delta r \) and \( R = 10\Delta r \). In practice a weakening radius of \( \Delta r \leq R \leq 2\Delta r \) works very good. When the weakened Green function is compared to the non-weakened version, it is noticed that only the real part for \( r < R \) of both functions really differ, while for \( r > R \) the difference between both functions becomes very small. However the aliasing suppression is improved considerably. Section 7.3.2 shows simulation results of the accuracy improvements obtained with this filter.
Bibliography


Summary

The design techniques currently available for improving EM compatibility focus mainly on the physical layout, while other design phases are scarcely taken into account. To find an efficient solution, EM compatibility should also be considered during those phases. This requires that during each design phase the chance for corruption of the information carried by the signals is minimized by improving the separation between signals. To distinguish between the different classes of techniques that can be applied to improve signal separation (i.e., to improve compatibility), we considered a circuit at four different levels: the information level, coding/modulation level, circuit level, and layout level. Each level treats a different domain in which the separation between desired and parasitic signals can be improved. This thesis concentrates on circuit and layout design techniques. The techniques presented can be used to anticipate layout-related compatibility problems like EM coupling during circuit design. The layout design is optimized for the circuit topology by minimization of coupling due to overlap between signal paths and coupling via shared conductors.

The capacity of an information channel is reduced by the presence of parasitic (interference), and compatibility problems arise when these parasitic signals reduce the capacity beyond the level required for information processing and transport. To improve compatibility, additional capacity can be reserved to anticipate the loss due to interference, redundancy can be added to the signals to improve the ability to recover the information, and the loss of capacity can be reduced by adaptive noise canceling with the help of an estimation of the interfering signal. These techniques, however, put higher demand on the dynamic range of the system as it must be able to handle parasitic and desired signals simultaneously.

At the coding/modulation level, a system is represented by a functional block diagram. Compatibility problems arise when the parasitic and desired signals become indistinguishable during processing, while the desired signal cannot be recovered. To improve compatibility, one has to optimize the separation between the desired and parasitic signals. Therefore, the coding of desired signals should be made orthogonal to the coding of parasitic signals whenever possible. However, when the coding of the parasitic signals is unknown, interference is minimized by coding that distributes the signal energy as much as possible over the complete signal domain (e.g., spread spectrum). The signal processing should (preferably) be implemented with reversible (i.e., non-switching, non-saturating) operations to maximize separation between signals.

At the circuit level, the system is represented by a schematic diagram. Compatibility problems arise due to crosstalk and loss of orthogonality between desired and parasitic signals due to distortion (e.g., intermodulation, quadratic and envelope
To improve EM compatibility, one has to minimize the influence of coupling between interconnections, coupling via common-mode paths, and the loss of separability between signals due to distortion. For electrically short interconnections (short with respect to the signal wavelength), the influence of EM interaction is reduced by minimization of the net signal energy transported using current or voltage domain signals. Current domain signals offer the highest immunity, because induced parasitic voltages are rejected. Voltage domain signals are the least sensitive to emission, because a voltage detector has an very high impedance (e.g., it is an open) and reflects an electric signal completely. The emission from the reflected signal compensates the emission from the input signal. For electrically long interconnections (transmission lines), the source and load impedance must match the line impedance to minimize the extra emission caused by standing waves. To minimize coupling between signal paths, their characteristic impedance should be low compared to their transimpedance. Extra (redundant) signal paths can be added that are used to estimate and compensate for parasitic signals that are introduced by interconnections. To reduce common-mode coupling between sub-circuits via common-mode paths and the power supply, a differential implementation is preferred. It isolates these paths from the signal paths. To prevent a loss of separation between signals due to distortion, non-linear operations should be made reversible (i.e., non-switching, non-saturating). For linear operations, a differential class-A implementation with overall feedback is preferred, because it minimizes bias modulation by the signal, while the odd transfer of the differential implementation minimizes quadratic detection. In addition, the gain stage can be linearized by decomposing it as a sum of non-linear functions, to reduce distortion of parasitic signals above the loop bandwidth.

At the layout level, the design is represented by the integrated circuit or printed circuit board layout. Compatibility problems arise due to undesired EM interaction between components and interconnections, radiation and reception. To improve the compatibility of a layout, the difference-mode and common-mode coupling mechanisms between signal paths must be minimized. To minimize difference-mode coupling, netlist-based layout methods have to be replaced by signal-path-based methods. This means that instead of nets, signal paths have to routed. The most important measures to minimize EM coupling between signal paths are elimination of shared conductors and minimization of overlap between signal paths. In addition to this, the coupling between subsystems is further reduced by orthogonal orientation of their signal paths. One of the best planar implementations of signal paths is the coplanar waveguide, which is considerably better than the commonly used microstrip. To minimize common-mode coupling between paths, common-mode parasitic dipoles have to be folded.Overlap between, and the enclosed area of common-mode parasitic loops also has to be minimized. The common-mode and difference-mode couplings can be reduced even further with the help of a shielding plane (e.g., ground plane) at an electrically short distance from the interconnect. These common mode parasitic antennas are not always easy to find in complex circuits. With the help of graph theory, however, parasitic dipoles can be detected as graph cuts, while parasitic loops can be found as graph circuits.

Finally, the EM compatibility of a design must be analyzed and verified. This is done with the help of a circuit description that is extracted from the layout. It is analyzed with a circuit simulator like Cadence's Spectre™ or SPICE. Many EM
simulation techniques based on finite-difference or integral methods have been developed that are suitable for analyzing a circuit layout. However, translation of the EM simulation results into circuit parameters is difficult. Circuit extraction methods typically calculate the current that flows through a component and the voltage across it in order to determine its interaction with the environment. This method implicitly assumes that the EM interaction is concentrated between the component’s terminals. However, this assumption is only true if the radiation and reception of the component itself can be ignored. For accurate circuit extraction, the extracted circuit must represent the complete EM energy exchange between the components. Therefore we developed a new circuit extraction program which derives a circuit description that is not based on the extracted current and voltages, but rather on the extracted currents flowing through the components and power exchange between the components. Because the components connected to a network take part in the EM interaction with that network, the port impedance of a network is also determined the physical properties of the component that “observes” this port. Our circuit extraction program therefore determines the network port impedances as “observed” by the component connected to it. A method of moments based simulator that uses the conjugate gradient method to solve the currents that flow through the circuit is applied. To reduce the complexity of including different component geometries in the simulation, a current excitation is used instead of the commonly used voltage excitation. A comparison of simulation and measurement results in this thesis shows the accuracy of this method. Discretization of EM fields for numerical simulation requires spatial sampling, which can introduce aliasing errors. To suppress these errors, today’s simulators often apply weakening functions that act like moving average anti-aliasing filters. It is shown in this thesis that the convergence and accuracy of a field simulator can be further improved with a sinc-shaped spatial anti-aliasing filter that is adapted to the discretization.
Samenvatting

De huidige ontwerptechnieken voor het verbeteren van EM-compatibiliteit richten zich voornamelijk op de fysieke inrichting van een systeem en laten de overige ontwerpfasen vrijwel buiten beschouwing. Echter om tot een efficiënte oplossing te komen, dient EM-compatibiliteit ook gedurende andere ontwerpfasen meegenomen te worden. Dit houdt in dat tijdens elke ontwerpfase de kans op het verlies van de door de signalen gedragen informatie wordt geminimaliseerd door middel van het verbeteren van de scheiding tussen de signalen. Om de diverse klassen van technieken voor het verbeteren van de scheiding tussen signalen te vinden, beschouwen we een systeem op vier verschillende niveaus: het informatieniveau, codering- en modulatieniveau, circuitniveau en het niveau van de fysieke inrichting. Elk van deze niveaus beschouwt een ander signaaldomein waarbinnen de scheiding tussen signalen kan worden verbeterd. In dit proefschrift concentreren we ons op het circuitniveau en die van de fysieke implementatie. De gepresenteerde technieken helpen om tijdens het circuitontwerp te anticiperen op fysieke implementatiegerelateerde compatibiliteitsproblemen, zoals EM-koppeling. De fysieke inrichting wordt geoptimaliseerd voor een circuitontwerp, door EM-koppeling ten gevolge van overlap tussen signaalpaden en het delen van geleiders tussen signaalpaden te minimaliseren.

De capaciteit van een informatiekanaal wordt gereduceerd door aanwezigheid van parasitaire informatie (interferentie), en we spreken van een compatibiliteitsprobleem wanneer de capaciteit beneden het niveau komt dat nodig is voor foutvrije verwerking en transport van informatie. De compatibiliteit wordt verbeterd door het toevoegen van extra kanaalcapaciteit, het toevoegen van extra redundante informatie voor foutcorrectie en het toepassen van adaptieve filtertechnieken, die de verloren kanaalcapaciteit terug winnen door de parasitaire informatie te schatten en te verwijderen. Deze laatste techniek vereist echter een groter dynamisch bereik, omdat een systeem zowel de gewenste als de interfererende informatie gelijktijdig moet verwerken.

Op het niveau van codering en modulatie wordt een systeem beschreven door een functieblokdiagram. Op dit niveau manifesteert een compatibiliteitsprobleem zich als een probleem waarbij gedurende de signaalverwerking een gewenst en een interfererend signaal niet meer van elkaar te onderscheiden zijn, en het gewenste signaal niet meer teruggewonnen kan worden. Om de compatibiliteit te verbeteren moet de scheidbaarheid tussen signalen worden geoptimaliseerd. Daarom dient de signaalcodering van het gewenste signaal te worden georthogonaliseerd t.o.v. interfererende signalen, wanneer deze bekend zijn. Wanneer de codering van een interfererend signaal onbekend is, kan het beste een codering worden gekozen, die het signaalvermogen zoveel mogelijk over het coderingsdomijn uitspreidt (bijv. spread spectrum), waardoor de
kans op volledige verstoring wordt geminimaliseerd. Om verlies aan scheibbaarheid tijdens bewerkingen te voorkomen, moeten deze onkeerbaar zijn voor het te verwerken signaal (d.w.z. geen schakelende of begrenzende bewerkingen).

Op circuitniveau wordt een systeem gerepresenteerd door een schakelschema. Op dit niveau manifesteren compatibiliteitsproblemen zich als overspraakproblemen en verlies van scheibbaarheid tussen signalen door vervorming (bijv. intermodulatie, kwadratische- en onbundelde detectie). Om compatibiliteit op dit niveau te verbeteren moet zowel de invloed van koppeling tussen de signaalpaden, koppeling via gemeenschappelijkemodus paden als het verlies van scheibbaarheid door (niet lineaire) vervorming worden geminimaliseerd. De koppeling voor elektrisch-korte-verbindingen (d.w.z. kort t.o.v. de golflengte) wordt geminimaliseerd door de vermogensoverdracht te minimaliseren, middels toepassing van stroom- of spanningdomeinsignalen. Stroomdomeinsignalen leveren de hoogste immuniteit op, omdat ze ongevoelig zijn voor geïnduceerde spanningsignalen. Spanningdomeinsignalen veroorzaken de minste emissie, omdat een spanningdetector een zeer hoge ingangsimpedantie heeft (d.w.z. het is een open) en het ingangssignaal volledig reflecteert. De emissie van het gereflecteerde signaal heft de emissie van het ingangssignaal grotendeels op. Voor elektrisch-korte-verbindingen dient de impedantie aan beide uiteinden aangepast te worden aan de karakteristieke impedantie van de verbinding, om extra emissie ten gevolge van staande golven te voorkomen. Voor minimale koppeling tussen signaalpaden dient de ratio van karakteristieke impedantie en de transimpedantie tussen de paden zo laag mogelijk zijn. Extra redundante signaalpaden kunnen worden toegevoegd om schatting en compensatie van interfererende signalen mogelijk te maken. Om koppeling tussen deelcircuits via gemeenschappelijkemodus paden en de voeding te reduceren, heeft een differentiële implementatie de voorkeur. Dit isolert deze paden van het signaalpad. Om verlies van de scheibbaarheid tussen signalen te gevolge van distorsi te voorkomen, dienen alle signaalbewerkingenfuncties onkeerbaar te zijn. Lineaire bewerkingen hebben bij voorkeur een differentiële klasse-A implementatie met over-all terugkoppeling, zodat instelstromen minimaal afhankelijk zijn van het signaal, en kwadratische detectie wordt geminimaliseerd. In aanvulling daarop kan niet lineaire vervorming voor frequenties hoger dan de busbandbreedte worden gereduceerd door de versterkertrappen te lineariseren door een lineaire functie op te bouwen als gewogen som van de niet lineaire overdrachten van de individuele transistoren.

Op het niveau van de fysieke opbouw, wordt een ontwerp gerepresenteerd door een bouwtekening. EM-compatibiliteitsproblemen worden veroorzaakt door ongewenste EM interactie tussen componenten en bedrading, emissie en ontvangst. Om de compatibiliteit te verbeteren moet zowel de differentiëlemodus- als gemeenschappelijke-moduskoppeling tussen signaalpaden worden geminimaliseerd. Voor de reductie van differentiëlemoduskoppeling dienen de ontwerp methoden die zijn gebaseerd op de netwerkbeschrijving te worden vervangen door methoden die gebaseerd zijn op een beschrijving van de signaalpaden tussen componenten. Dit betekent dat in plaats van netten, signaal paden moeten worden ontworpen. De belangrijkste manieren om koppeling tussen signaalpaden te reduceren zijn het elimineren van gemeenschappelijke geleiders en het vermijden van overlap tussen signaalpaden. Verdere reductie wordt verkregen door signaalpaden orthogonaal ten opzichte van elkaar te positioneren. Een van de beste plenaire implementaties van een signaalpad is de coplanaire golfgeleider, welke aanzienlijk beter presteert dan de gangbare microstripconstructie.
Reductie van koppeling in de gemeenschappelijke modus wordt verkregen door het
opvouwen van parasitaire dipoolantennes, reductie van het oppervlak dat wordt om-
sloten door parasitaire lusantennes en reductie van overlap tussen parasitaire hussen.
Met behulp van een afschermvlak (bijv. grondvlak) op elektrisch korte afstand tot
het bedrading, kan een aanzienlijke additionele reductie in de koppeling worden ver-
kregen. In complexe circuits zijn gemeenschappelijke-modes antennes vaak moeilijk
te herkennen. Echter met behulp van grafentheorie kunnen alle mogelijke parasitaire
dipoolantennes worden gedetecteerd als graafneden, en parasitaire lusantennes als
graafcircuits.

Tot slot moet de compatibiliteit van het ontwerp worden geanalyseerd en gever-
ifieerd. Hiervoor wordt een equivalentcircuit van het fysieke ontwerp geëxtraheerd,
welke met behulp van een circuitsimulator zoals Spectre™ van Cadance of SPICE
wordt geanalyseerd. Veel van de ontwikkelde EM-simulatietechnieken die zijn geba-
seerd op eindige differentie- of integraalmethoden kunnen een fysiek ontwerp goed
simuleren. Echter de vertaling van de EM-veldsimulatieresultaten in een equivalente
circuitbeschrijving is vaak moeilijk. De meest gangbaremethode is om quasistatische-
spanningen en stromen uit de simulatiegegevens te extraheren, waaruit vervolgens
equivalente impedanties berekend worden. Impliciet wordt dan aangenomen dat de
interactie vrijwel uitsluitend tussen de aansluitklemmen van het component plaats-
vindt. Deze aanname is alleen juist wanneer de emissie en ontvangst door het com-
ponent zelf kan worden verwaarloosd. Voor nauwkeurige circuitextractie echter, dient
de volledige EM-energie overdracht tussen een component en zijn omgeving te worden
meegenomen. Wij hebben daarom een nieuwe extractiemethode ontwikkeld, die niet
op de stroomen en spanning overdracht is gebaseerd, maar aan de hand van de totale
EM-energieoverdracht tussen de componenten en de stroom die door deze compo-
nten vloeit. Omdat de componenten aangesloten op een netwerk deelnemen in de EM
interactie met dat netwerk wordt de poort impedantie van een netwerk medebepaalt
door de fysieke eigenschappen van het component dat deze poort “observeert”. Ons
circuit extractie programma bepaalt daarom de poort impedanties van een netwerk,
zoals deze worden “geobserveerd” door de componenten die daarop zijn aangesloten.
Wij hebben een op de momentenmethode gebaseerde simulator gebruikt die met be-
hulp van de geconjugeerde gradiëntmethode de stromen in het circuit berekent. Om
de complexiteit, die wordt veroorzaakt door het meenenemen van de geometrie van de
circuitcomponenten in de EM-veldsimulatie te reduceren, hebben wij stroomexcitatie
in plaats van de gangbare spanningexcitatie toegepast. Een vergelijk van de simulatie-
resultaten met de meetresultaten toont aan dat dit een nauwkeurige methode is. Voor
computerberekening van EM-velden, is discretisatie van de stromen en velden nodig,
welke aliasingfouten (vouwvervorming) tot gevolg kan hebben. Om dit type fouten te
voorkomen, passen moderne veldsimulatoren ruimtelijke middeling van het veld toe in
een beperkt gebied rondom elke bemonstering. Dit is een vorm van ruimtelijk filteren.
Wij laten zien dat een betere nauwkeurigheid en snellere convergentie verkregen kan
worden met behulp van een optimaal ruimtelijk anti-aliasingfilter, welke is aangepast
deur de ruimtelijke bemonsterspatiëriëring.
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