Wideband High Power Amplifier Design

A thesis submitted to the Electrical Engineering, Mathematics and Computer Science Department of Delft University of Technology in partial fulfillment of the requirements for the Degree of Master of Science in Microelectronics

by

Jing LI

Supervisors:

Dr. ing. Leo C.N. de Vreede, TU Delft
M.Sc. David A. Calvillo-Cortés, TU Delft
Ir. Rob Heeres, NXP Semiconductors
Ir. Thomas Roedle, NXP Semiconductors

Delft University of Technology, the Netherlands

@Copyright by Jing LI, August 2011
Abstract

High power wideband amplifiers are demanded in many application areas, such as software defined radio, electronic warfare (EM), instrumentation systems, etc. This thesis project aims to build a high power wideband amplifier suitable for base station instrumentation purposes. It is discussed that balanced amplifiers are very suitable for this purpose due to their remarkable properties. To enable both LDMOS as well as GaN technology for true wideband operation, two bandwidth extension design methods are studied and developed within this thesis work. 3 dB quadrature couplers, which are important components in the realization of the balanced amplifiers, are demanded. In this thesis, two kinds of broadband 3-dB quadrature couplers, of which one is pretty novel, are designed and implemented. In view of lower cost of the implementation of Wilkinson dividers compared to 3-dB quadrature couplers, two broadband Wilkinson dividers are employed instead of the 3-dB quadrature couplers at the appropriate places in the total topology in order to reduce the cost and lower the complexity of the amplifier implementation. Hence, Wilkinson dividers are designed and implemented. The final design is implemented with Cree GaN devices. Simulation results have shown that the saturation output power in the bandwidth (0.7~2.6 GHz) is 54.9±0.9 dBm, and it becomes worse (53±1 dBm) from 2.6 GHz to 2.8 GHz.

Besides the high power wideband amplifier design, additional investigation on adaptive matching using duty-cycle control in Class-E power amplifier is presented. It is proved that parallel Class-E PAs seem to provide the best performance in terms of a wide impedance tuning range to achieve high efficiency and high output power.
Completion of this project and this thesis is a one year long and eventful journey. I would like to give thanks to all those who supported me along the way. Without their help, it is impossible for me to finish the project alone.

First and foremost, I would like to express my high appreciation to Dr. Leo de Vreede, my supervisor, who leads me into the world of microwave circuit design, for his outstanding guidance, continuous support, valuable discussion, constant encouragement and never ending patience throughout my master project. I learned a lot from him.

My sincere gratitude goes to David Calvillo Cortes, who is my mentor. He gave me countless help during my research work. He has shown great patience during endless discussions, and is always willing to share his knowledge and experience. I learned from him not only the knowledge but also conscientious attitude on the research. I am grateful to other people in our group for their help during the past year. They are Keon Buisman, Gennaro Gentile, Rui Hou, Cong Huang, Marco Pelk, Marco Spirito, Atef Akhnoukh, Morteza Alavi, Mauro Marchetti. Special thanks to the senior students of our group, Kanjun Shi, Bo Wu, Yinan Wang. I can also learn knowledge when talking with them. I would like to thank my colleagues, Rahul Todi, Serban Motoroiu, Ajay Kumar Manjanna, for their wonderful company.

I would like to thank NXP semiconductors, which sponsors my project. Thanks go to Rob Heeres, my supervisor of NXP, for his support and suggestions during the whole year.

I also would like to thank all my friends in Delft. The activities with them made my life colorful. Among them, special thanks to Wenlong Jiang. His company during the past two year in the Spacebox made my life not too boring and hard. Sincerely hope that he will have a gorgeous future in the USA.
Finally, I would like to express my deepest gratitude to my parents. Their support, patience, understanding and love give me the strength to overcome all the difficulties.

Jing LI

Delft, the Netherlands

August 17th, 2011
Contents

Abstract............................................................................................................................................ iii

Acknowledgments................................................................................................................................... v

1 Introduction..................................................................................................................................... 1
  1.1 Motivation................................................................................................................................... 1
  1.2 Active Load-Pull Systems............................................................................................................. 1
  1.3 The injection amplifier requirements ......................................................................................... 2
  1.4 Thesis Research Goal and Strategy ............................................................................................ 3
  1.5 Thesis Organization.................................................................................................................... 4

2 Theory for RF Amplifiers............................................................................................................... 5
  2.1 Power Amplifier Basics............................................................................................................... 5
    2.1.1 Power Amplifier Considerations.......................................................................................... 5
      2.1.1.1 Output Power............................................................................................................... 5
      2.1.1.2 Power Gain.................................................................................................................. 6
      2.1.1.3 Gain Flatness................................................................................................................. 6
      2.1.1.4 Efficiency..................................................................................................................... 6
      2.1.1.5 Linearity....................................................................................................................... 7
      2.1.1.6 Stability....................................................................................................................... 8
    2.1.2 Power Amplifier Classification............................................................................................ 8
      2.1.2.1 Transconductance PAs.............................................................................................. 9
      2.1.2.2 Switch Mode PAs........................................................................................................ 11
    2.2 Conclusion............................................................................................................................... 14

3 High Power Amplifiers.................................................................................................................. 15
  3.1 3-dB Quadrature Couplers......................................................................................................... 15
  3.2 Wilkinson Power Dividers.......................................................................................................... 22
### 3.3 Balanced Amplifiers

- 3.3.1 Background Theory ................................................................. 23
- 3.3.2 Advantages and Disadvantages .................................................. 24
- 3.3.3 Effect of Imperfect Balance ......................................................... 27
- 3.3.4 Alternative Configuration of the Balanced Amplifier ...................... 27

### 3.4 Power Amplifier Topology on This Work ........................................... 29

### 3.5 Conclusion ....................................................................................... 31

### 4 Wideband Power Amplifier Design ...................................................... 33

#### 4.1 RF Power Transistor Technologies .................................................. 33

#### 4.2 Bode-Fano Limitation on Matching ................................................ 35

#### 4.3 Wideband Matching Networks ......................................................... 37
- 4.3.1 Multi-section LC Matching Networks ....................................... 37
- 4.3.2 Multi-section Quarter-wavelength Transformers .......................... 39

#### 4.4 Bandwidth Enhancement Techniques .............................................. 39
- 4.4.1 Reactive Matching ........................................................................ 39
- 4.4.2 Lossy Matching ............................................................................ 40
- 4.4.3 Feedback ....................................................................................... 43

#### 4.5 Design Version I Using NXP LDMOS Die Transistors ..................... 44
- 4.5.1 DC Characteristics ....................................................................... 45
- 4.5.2 Load-line Analysis ...................................................................... 46
- 4.5.3 Using a R-L Shunt Matching Network ....................................... 48
- 4.5.4 Using a R Shunt Matching Network .......................................... 51
- 4.5.5 Conclusion from previous designs ............................................. 55

#### 4.6 Design Version II Using Cree GaN Packaged Transistors ............... 56
- 4.6.1 DC Characteristic ....................................................................... 57
- 4.6.2 Load-pull Analysis ...................................................................... 57
- 4.6.3 Matching Network Design ......................................................... 58
- 4.6.4 Simulation Performance .............................................................. 59
5 Wideband Hybrids Design........................................................................................................61
  5.1 3-dB Quadrature Coupler Design........................................................................................61
    5.1.1 Offset Stripline Configuration.........................................................................................61
    5.1.2 Vertically Installed Planar Configuration......................................................................68
  5.2 Wilkinson Divider Design..................................................................................................68
  5.3 Conclusion .........................................................................................................................72

6 A 360 W 0.7-2.8 GHz Wideband GaN Instrumentation Amplifier ........................................74
  6.1 Circuit Design .....................................................................................................................74
  6.2 Simulated Performance ......................................................................................................77
  6.3 Measurements .....................................................................................................................87

7 Conclusion and Recommendations..........................................................................................88
  7.1 Conclusion ..........................................................................................................................88
  7.2 Recommendations .............................................................................................................90

A Even- and Odd-mode Analysis of Symmetrical Networks.....................................................92
  A.1 Even- and odd- mode analysis of symmetrical networks....................................................92
  A.2 Forward-wave and back-wave directional couplers............................................................95

B Analysis of a Two-section Tandem Coupler ......................................................................98

C Investigation on Adaptive Matching Using Duty-cycle Control in Class-E Power Amplifiers..........................................................................................................................100
  C.1 Introduction ....................................................................................................................... Error! Bookmark not defined.
  C.2 Class-E Load-Pull Simulation .............................................................................................. Error! Bookmark not defined.
  C.3 Simulation Results ............................................................................................................ Error! Bookmark not defined.

Bibliography ................................................................................................................................101
List of Figures

Figure 1.1 Simplified block diagrams of typical load-pull systems (a) Closed-loop active load-pull system (b) Open-loop active load pull system ................................................. 2
Figure 1.2 Equivalent schematic of an active load pull system .................................. 3
Figure 2.1 The generic schematic of a power amplifier............................................... 5
Figure 2.2 The reduced conduction angle current waveform........................................ 9
Figure 2.3 Normalized output power and efficiency as a function of conduction angle [10]. 11
Figure 2.4 Basic circuit of Class-E power amplifier.................................................. 12
Figure 2.5: The schematics of Class-F power amplifier and inverse Class-F power amplifier ........................................................ ........................................... 13
Figure 3.1 The symbol of a directional coupler .......................................................... 15
Figure 3.2 The schematics of the directional couplers............................................... 17
Figure 3.3 Coupling of single section, three symmetrical section and three asymmetrical section couplers ........................................................................................................ 19
Figure 3.4 Phase difference between the waves of through port and coupled port of single section, three symmetrical section and three asymmetrical section couplers........... 19
Figure 3.5 Several types of 3 dB quadrature coupler implementations (a) Lange coupler in microstrip technology (b) Edge-side microstrip coupler (c) Vertical installed planar coupler-line configuration (d) Offset coupled striplines configuration .................. 21
Figure 3.6 A 3 dB quadrature coupler with the tandem structure................................ 21
Figure 3.7 The schematic of the Wilkinson coupler.................................................. 22
Figure 3.8 Configuration of a balanced amplifier ..................................................... 23
Figure 3.9 Another kind of a balanced amplifier configuration .................................... 28
Figure 3.10 The schematic of the three sections Wilkinson coupler connected with a quarterwave transmission line ...................................................................................... 28
Figure 3.11 The amplitude and phase responses of the three sections Wilkinson coupler
Figure 3.13 The amplifier topology used in this project ........................................... 30
Figure 3.12 A topology of a high power amplifier [40] ............................................ 30
Figure 4.1 A power device with internal prematch [45] ........................................ 35
Figure 4.2 Bode-Fano network: RC series network ................................................. 35
Figure 4.3 Bode-Fano network: RC parallel network .............................................. 36
Figure 4.4 A single section LC matching network (Rs > RL) .................................. 38
Figure 4.5 Multi-section LC matching network (Rs > RL) ....................................... 38
Figure 4.6 A multi-section quarter-wave transformer .............................................. 39
Figure 4.7 Illustration of the flat gain design concept of reactive match approach ...... 40
Figure 4.8 Several kinds of Lossy matching networks at the input of device ............. 41
Figure 4.9 A circuit schematic of a power amplifier with the input R-L shunt network ... 42
Figure 4.10 The input part of a power amplifier with the R-L shunt network ............ 43
Figure 4.11 The equivalent circuit of input part of a power amplifier with the R-L shunt network .................................................................................................................. 43
Figure 4.12 The output part of a power amplifier with the R-L shunt network ............ 43
Figure 4.13 Several different kinds of feedback networks ........................................ 44
Figure 4.14 The transfer characteristic of Gen7_050mm_050um for 28V drain bias .... 45
Figure 4.15 The transfer characteristic of Gen7_TUD_050mm_050um for 28V drain bias... 46
Figure 4.16 Load-line of a device for a Class-A operation ....................................... 47
Figure 4.17 The load-lines of the LDMOS Models ..................................................... 48
Figure 4.18 The schematic for simulation of lossy match: R-L shunt network ........... 49
Figure 4.19 The simulation result of lossy match: R-L shunt network ..................... 50
Figure 4.20 The package implemented in HFSS ....................................................... 51
Figure 4.21 A circuit schematic of a power amplifier with the R shunt network ........... 51
Figure 4.22 The schematic for simulation of lossy match: R shunt network for LDMOS Model Gen7_050mm_050um (R=1.4 Ohm) ......................................................... 52
Figure 4.23 The simulation results of lossy match: R shunt network for LDMOS Model Gen7_050mm_050um (R=1.4 Ohm) ........................................................................ 53
Figure 4.24 The schematic for simulation of lossy match: R shunt network for the LDMOS Model Gen7_TUD_050mm_050um (R=3 Ohm) .......................................................... 54
Figure 4.25 The simulation results of lossy match: R shunt network for the LDMOS Model Gen7_TUD_050mm_050um (R=3 Ohm) .......................................................... 55
Figure 4.26 The total schematic of the proposed power amplifier ...................................... 56
Figure 4.27 The transfer characteristic of CGH40180PP for 28V drain bias .............................. 57
Figure 4.28 The Load-pull simulation setup ........................................................................ 57
Figure 4.29 The output matching network ........................................................................ 59
Figure 4.30 The input matching network ........................................................................... 59
Figure 4.31 The schematic simulation results of the designed power amplifier ....................... 60
Figure 5.1 The cross section of the offset stripline ............................................................... 62
Figure 5.2 The stripline configuration constructed by stacked microstips ............................... 62
Figure 5.3 The layout of a 8.34 dB coupler based on 50 Ohm reference impedance ................. 63
Figure 5.4 The layout of the designed 3 dB offset stripline coupler in momentum ................. 64
Figure 5.5 The momentum simulation results of the designed 3 dB offset stripline coupler
(a) S21 and S31 (b) S11 and S41 (c) Amplitude balance (d) Phase difference ...................... 65
Figure 5.6 The modified layout of the designed -3 dB offset stripline coupler in momentum 66
Figure 5.7 The structure of the designed -3 dB offset stripline coupler in HFSS ................. 66
Figure 5.8 The comparison of HFSS simulation results of the designed 3 dB offset stripline coupler without air (a) (c) and with air in the structure (b) (d) ................................. 67
Figure 5.9 The effect of process variations on performance of the designed coupler ............... 68
Figure 5.10 A typical directional coupler with the VIP structure Error! Bookmark not defined.
Figure 5.11 The cross sectional view of VIP structure Error! Bookmark not defined.
Figure 5.12 The electric field distribution for (a) even (AA’ is a magnetic wall) and (b) odd (AA’ is an electric wall) excitation Error! Bookmark not defined.
Figure 5.13 Representation of capacitances of the VIP topology coupler Error! Bookmark not defined.
Figure 5.14 A design example of VIP topology using 12.5 Ohm as the reference impedance Error! Bookmark not defined.
Figure 5.15 The setup to calculate the even- and odd-mode characteristic impedances of the separate central section of the VIP configuration coupler.  

Figure 5.16 The total structure of the three-section VIP topology coupler.  

Figure 5.17 The results simulated by HFSS of the designed VIP topology coupler.  

Figure 5.18 The modified VIP coupler.  

Figure 5.19 Schematic diagram of the compensated three section directional coupler.  

Figure 5.20 The structure of the designed coupler with compensation capacitances.  

Figure 5.21 The results simulated by HFSS of the modified VIP topology coupler.  

Figure 5.22 The schematic of the designed impedance transforming Wilkinson divider with ideal components.  

Figure 5.23 The schematic simulation of the impedance transforming Wilkinson divider using ideal components (a) S21 and S31 (b) S22, S33 and S32 (c) S11 (d) Phase difference.  

Figure 5.24 The structure of the designed impedance transforming Wilkinson divider in HFSS.  

Figure 5.25 The HFSS simulation results of the designed impedance transforming Wilkinson divider.  

Figure 6.1 The proposed topology of the desired amplifier.  

Figure 6.2 The layout of the designed amplifier (version I).  

Figure 6.3 The s layout of the designed amplifier (version II).  

Figure 6.4 The simulation results of the single-ended amplifiers using Momentum simulation data for the passive structures (a) S21 and S11 (b) Output power (c) Stability k factor (d) μ factor.  

Figure 6.5 The layout of impedance transformers.
Figure 6.6 The simulation results of the single-ended PA connected with wideband impedance transformers at the input and output (simulated using Momentum data for the passive structures) (a) S21 and S11 (b) Output power (c) Stability k factor (d) μ factor........79

Figure 6.7 The modified layout of the 3-dB quadrature coupler using the offset stripline configuration.........................................................79

Figure 6.8 The HFSS simulation results of the modified layout of the 3-dB quadrature coupler using the offset stripline configuration (a) S21 and S31 (b) S11 and S41 (c) Amplitude balance (d) Phase difference ..........................................80

Figure 6.9 The modified layout of the 3-dB quadrature coupler using VIP configuration .....81

Figure 6.10 The HFSS simulation results of the modified layout of the 3-dB quadrature coupler using the VIP configuration.........................................................81

Figure 6.11 The Momentum simulation results of the modified layout of the Wilkinson divider ................................................................................................................82

Figure 6.12 The simulation results of the balanced PA I (a) S21 and S11 (b) Output power (c) Stability k factor (d) μ factor.................................................................84

Figure 6.13 The simulation results of the balanced PA II (a) S21 and S11 (b) Output power (c) Stability k factor (d) μ factor.................................................................85

Figure 6.14 The simulation results of the total PA I (a) S21 and S11 (b) Output power (c) Stability k factor (d) μ factor.................................................................86

Figure 6.15 The simulation results of the total PA II (a) S21 and S11 (b) Output power (c) Stability k factor (d) μ factor.................................................................87

Figure A.1 A four-port symmetrical network.................................................................................................................................92

Figure A.2 A directional coupler.............................................................................................................................................96

Figure B.1 A two-section tandem coupler.................................................................................................................................98

Figure C.1 Class-E PA with varying duty cycle and load impedance

Figure C.2 The transfer characteristic of CGH60060D for 28V drain bias

Figure C.3 The drain-source capacitance versus the drain voltage
Figure C.4 The load pull simulation schematic for the Class-E PA.

Figure C.5 Simulation results for the efficiency, output power and peak drain voltage for a 50% of duty-cycle (standard Class-E operation).

Figure C.6 (a) The optimum efficiency contours (b) The corresponding output power contours when the efficiencies are optimum (c) The optimum output power contours (d) The corresponding efficiency contours when the output powers are optimum (Vpeak<100V) (Standard Class-E).

Figure C.7 (a) The optimum efficiency contours (b) The corresponding output power contours when the efficiencies are optimum (c) The optimum output power contours (d) The corresponding efficiency contours when the output powers are optimum (Vpeak<100V) (Subharmonic Class-E).

Figure C.8 (a) The optimum efficiency contours (b) The corresponding output power contours when the efficiencies are optimum (c) The optimum output power contours (d) The corresponding efficiency contours when the output powers are optimum (Vpeak<100V) (Parallel circuit Class-E).

Figure C.9 (a) The optimum efficiency contours (b) The corresponding output power contours when the efficiencies are optimum (c) The optimum output power contours (d) The corresponding efficiency contours when the output powers are optimum (Vpeak<100V) (Even harmonic Class-E).

Figure C.10 The load areas of the four different Class-E PAs (a) Standard Class-E (b) Subharmonic Class-E (c) Parallel circuit Class-E (d) Even harmonic Class-E (aiming for both high efficiency (>60%) and high output power (>45 dBm)).

Figure C.11 The schematic of load-pull simulation for the Class-B PA.

Figure C.12 The result of load-pull simulation for the Class-B PA.
List of Tables

Table 4.1 Material properties of Si and GaN................................................................. 34
Table 4.2 Extracted intrinsic parameters for Gen7_050mm_050um.............................. 36
Table 4.3 The theoretical maximum bandwidths versus different input and output reflection coefficients .................................................................................................................. 37
Table 4.4 The values of important components in the schematic of R-L shunt matching topology ............................................................................................................... 49
Table 4.5 The values of important components in the schematic of R shunt matching topology for LDMOS Model Gen7_050mm_050um ................................................................. 52
Table 4.6 The different gains of power amplifiers with different values of shunt resistors (LDMOS Model Gen7_050mm_050um) ................................................................................... 53
Table 4.7 The values of important components in the schematic of R shunt matching topology for LDMOS Model Gen7_TUD_050mm_050um ................................................................. 54
Table 4.8 The optimum source and load impedances versus frequencies ..................... 58
Table 5.1 The parameters for the offset stripline ................................................................ 62
Table 5.2 Design parameters and physical dimensions of the -8.34dB coupler ............. 63
Table 5.3 The normalized even- and odd-mode characteristic impedance values of each section for a wideband 3 dB coupled line based quadrature hybrid Error! Bookmark not defined.
Table 5.4 The even- and odd-mode impedance values of the central section versus different reference impedances ............................................................. Error! Bookmark not defined.
Table 5.5 The even- and odd-mode characteristic impedances of the VIP topology coupler Error! Bookmark not defined.
Table 5.6 The physical dimensions of the designed VIP topology coupler Error! Bookmark not defined.
Table 5.7 Values of capacitances used for compensation of the designed coupler Error! Bookmark not defined.
Introduction

1.1 Motivation

There is a huge demand for high power wideband amplifiers in many application areas. Broadband high power amplifiers are considered as key components in next generation software defined radio communication systems [1]. In principle, application of a linear, highly efficient wideband amplifier can replace several narrowband power amplifiers, yielding reduced costs and form factor.

Also, in the instrumentation field, broadband high power amplifiers are needed in order to create sufficient flexibility in the testing of active devices for the next generation of wireless applications. Typically, these power amplifiers are the most expensive components in microwave characterization systems. This is definitely the case in active load pull systems, which are used to evaluate the performance of active devices in large signal operation. Using these setups, the best circuit conditions for the active devices can be found that yield the highest efficiency, output power or linearity.

1.2 Active Load-Pull Systems

Generally, there are two major types of active load pull systems, namely the closed-loop and open-loop active systems. Simplified block diagrams of these active load-pull systems are shown in Figure 1.1. A desired reflection coefficient $\Gamma_{\text{load}}$, as illustrated in Equation (1.1), can be achieved by injecting signals from external sources (open-loop system) or reusing the wave generated by the device under test (DUT) (closed-loop systems). The equivalent schematic is shown in Figure 1.2.
1.3 The injection amplifier requirements

The required injection power in an active load-pull system not only depends on the output power of the DUT and the desired $\Gamma_{load}$, but also on the output impedance of the device. [3] Note that for high power devices, their optimum load impedances can be very small (typically <5 $\Omega$), which are much smaller than the typical system impedance of an active load pull system (50 $\Omega$). To get some indication on the power requirements in such a system, the following example: assuming that a 100 W device needs to be characterized and its optimum load is 1.2 Ohm, to achieve this value in the active load pull system (without pre-match), it needs to delivery almost 1000 W, which can be calculated by Equation (1.2) [4]. Hence, a very high power amplifier is required for active load pull systems. Additionally, in order to have sufficient flexibility in the operating frequency of the load-pull system, the injection amplifiers need to be wideband as well. The communication bands that people are interested in are 700-1000MHz, 1.5 GHz, 1.8-2.7 GHz, and 3.2-3.8 GHz. Hence, in order to cover all those communication bands, the bandwidth should be at least from 700 MHz to 3.8 GHz.
\[ \Gamma_{\text{load}} = \frac{b_1}{a_1} \]  
(1.1)

\[ P_{\text{LP}} = \frac{p_d |\Gamma_{\text{LP}}|^2}{1 - |\Gamma_{\text{LP}}|^2} \]  
(1.2)

Figure 1.2 Equivalent schematic of an active load pull system

1.4 Thesis Research Goal and Strategy

This project aims to build a high power wideband amplifier for instrumentation purpose. To obtain high power, large periphery devices are required, such as high power LDMOS and GaN transistors, which own high breakdown voltages and provide a high power density. However, large peripheries imply large input/output capacitances limiting the bandwidth. In addition, their optimal load impedances are quite low. Consequently, the required impedance transformation to the system reference impedance (usually 50 Ohm) further limits the maximum achievable bandwidth. Especially the input matching proves to be very difficult when aiming for a high bandwidth performance using LDMOS transistors. For identical power levels, GaN transistors have smaller parasitic capacitances, which makes the wideband matching easier compared to LDMOS FETs. However, to enable both LDMOS as well as GaN technology for true wideband operation, bandwidth extension methods are studied and developed within this thesis work.

Unfortunately, even with these advanced design techniques, single device operation usually does not provide us with the desired power levels. To overcome this limitation, the achievable
power levels can be significantly increased by combining a number of power devices. In view of this, the balanced amplifier topology is explored to improve the power levels as well as the input and output matching, something that is highly beneficial when cascading multiple amplifier stages. However, when using balanced amplifiers, 3dB quadrature hybrids are demanded, which for the wideband operation can require a complicated implementation. Within this thesis work, attention is also given on how to overcome the technology limitation for 3 dB wideband hybrids by making some clever choices.

1.5 Thesis Organization

This thesis is organized as follows. Chapter 2 gives the general background information on RF amplifier operation. Chapter 3 discusses the power combining topologies for high power wideband amplifiers, and introduces the theory of balanced amplifiers with their advantages and disadvantages. Chapter 4 covers the theory of the single stage wideband branch amplifier design. Several bandwidth extension design methods for these PA cells are discussed. The design of two different broadband power amplifiers (using different device technologies) is also presented. Chapter 5 presents the design of wideband hybrids as required when combining the power of several devices. Two kinds of 3-dB quadrature couplers, of which one is pretty novel and a Wilkinson divider are designed and implemented. Chapter 6 is devoted to the design and measurement of a 360 W 0.7-2.8 GHz wideband GaN instrumentation amplifier. Chapter 7 concludes the thesis and gives recommendations for the future work.
This chapter presents the main considerations and the classification of power amplifiers.

2.1 Power Amplifier Basics

Power amplifiers are key elements of most microwave systems. When designing a microwave system, the specifications of the power amplifier are generally of most importance. Figure 2.1 shows the generic schematic of a power amplifier. In the following, the major specifications and classifications of power amplifiers are discussed.

![Figure 2.1 The generic schematic of a power amplifier](image)

2.1.1 Power Amplifier Considerations

2.1.1.1 Output Power

The power delivered to the load is known as the output power, $P_{\text{out}}$. In most cases, people are only interested in the power at the fundamental frequency. Hence, $P_{\text{out}}$ is calculated by the
fundamental components of the load current \( i_{\text{out}} \) and load voltage \( v_{\text{out}} \) as shown in Figure 2.1.

\[
P_{\text{out}} = \frac{1}{2} \text{real}(v_{\text{out}} \cdot i_{\text{out}}^*)|_{f=f_0} \tag{2.1}
\]

The transistors used in power amplifier designs have typically some constraints represented by parameters, such as \( I_{\text{DSS}} \) (drain saturation current) and \( V_{\text{br}} \) (breakdown voltage). Typically these transistors are also the most costly components in the systems. So, it is desired to extract the maximum power from them.

### 2.1.1.2 Power Gain

The power gain of an amplifier is the ratio of the output power to its input power, and it can be defined in several ways. For power amplifiers, the most common definitions of power gains are transducer power gain \( (G_T) \) and operating power gain \( (G_P) \). Their definitions are given below: [5]

\[
G_T = \frac{\text{power delivered to the load}}{\text{power available from the source}} = \frac{P_{\text{out}}}{P_{\text{avs}}} \tag{2.2}
\]

\[
G_P = \frac{\text{power delivered to the load}}{\text{power delivered to the network}} = \frac{P_{\text{out}}}{P_{\text{in}}} \tag{2.3}
\]

### 2.1.1.3 Gain Flatness

Gain flatness is often specified as how much the gain varies over the specified frequency range. Since variations in the flatness of the power amplifier’s gain can cause signal distortion. So, most amplifiers need a flat gain response over the desired bandwidth.

### 2.1.1.4 Efficiency

Efficiency can be specified in several ways, most commonly as Drain Efficiency, and Power Added Efficiency. Drain efficiency, \( \eta \), is defined as the ratio of the RF output power \( (P_{\text{out}}) \) and the total DC consumption power \( (P_{\text{DC}}) \) in Equation (2.4).
\[ \eta = \frac{P_{\text{out}}}{P_{\text{DC}}} \] 

(2.4)

PAE takes the effect of the input power into account, defined as Equation (2.5).

\[ \text{PAE} = \frac{P_{\text{out}} - P_{\text{in}}}{P_{\text{DC}}} \] 

(2.5)

Since \( P_{\text{out}} = P_{\text{in}} G_p \),

\[ \text{PAE} = \frac{P_{\text{out}} - P_{\text{in}}}{P_{\text{DC}}} = \frac{P_{\text{out}}}{P_{\text{DC}}} \left(1 - \frac{1}{G_p}\right) = \eta \left(1 - \frac{1}{G_p}\right) \] 

(2.6)

It can be found that PAE also depends on the gain of the amplifier. If the gain becomes really small (e.g. smaller than 1), PAE could even be negative.

2.1.1.5 Linearity

Linearity is very important for broadband microwave systems. Large signal nonlinearity is typically most severe at large input powers, which causes output signals to exceed their maximum value, and results in clipping. The nonlinearity of an amplifier can be characterized by their AM-AM distortion and AM-PM distortion. There are various ways to evaluate the nonlinearity of an amplifier. The simplest method is the measurement of the 1-dB compression power \( (P_{1\text{dB}}) \) for a single-carrier system. Two-tone measurements can provide the information on the third-order intermodulation distortion, yielding the third order intercept point (IP3). For operation with complex modulated signal, the adjacent channel power ratio (ACPR) and error vector magnitude (EVM) measurements are commonly used [5].

Linearity is mostly achieved at the expense of efficiency. For instance, conventional power amplifiers that operate at class A, are very linear, but their efficiencies are low. Other classes like Class AB or B have poorer linearity but greater efficiency. In the other hand, the efficiencies of switch mode power amplifiers (such as Class-E PAs) can be very high, but basically they are nonlinear in their behavior. There are some advanced amplifier configurations that provide high efficiency while maintaining linearity, for example,
feed-forward, Doherty amplifier, envelope elimination and restoration, and LINC (linear amplification with nonlinear components) [6].

2.1.1.6 Stability

Stability is an absolute requirement in power amplifier designs, and can be analyzed from the S parameters, the matching networks with their terminations. Oscillations are possible when either the input or output port of a network presents a negative resistance. This occurs when $|\Gamma_{IN}| > 1$ or $|\Gamma_{OUT}| > 1$. [7] The stability factor $K$ is often used to evaluate these conditions and is given by:

$$
K = \frac{1 - |S_{11}|^2 - |S_{22}|^2 + |\Delta|^2}{2|S_{12}S_{21}|} \\
\Delta = |S_{11}S_{22} - S_{12}S_{21}|
$$

If $K > 1$ and $|\Delta| < 1$, the designed power amplifier is unconditional stable, while it is conditional stable if $K < 1$.

Oscillations in single-ended configurations have been discussed above. There are also some possibilities for odd mode oscillations when dealing with power amplifiers using two or more transistors in parallel. In an even-mode operation, the currents and voltages are in phase for all devices, whereas in the odd-mode case the internal device currents and voltages of an amplifier may have opposite signs. There are many reasons that can cause odd-mode oscillations. For instance, the matching networks of different transistors may be not exactly the same due to coupling between circuit elements (e.g. bondwires). This slight mismatch can create a condition for odd-mode oscillations due to different RF voltages at the transistor drain nodes. Odd-mode oscillation can typically be eliminated by adding resistors between the inputs of the transistors in the multi-device amplifier design. [8][9]

2.1.2 Power Amplifier Classification

There are two main categories of power amplifiers, namely transconductance type of power amplifiers and switch-mode power amplifiers. The first type of power amplifier operates the
transistor as a dependent-current source, while in the second kind of PA, the transistor works as a switch.

### 2.1.2.1 Transconductance PAs

The classification of the transconductance type power amplifiers is based on the conduction angle of the drain current. The conduction angle is defined as the fraction of a period during which the transistor is carrying current. This type of PAs includes the Classes A, B, AB, and C. The reduced conduction angle current waveform is shown in Figure 2.2 and $\alpha$ is the conduction angle.

![Figure 2.2 The reduced conduction angle current waveform](image)

The Class-A power amplifier is the simplest amplifier type in terms of design. Its quiescent point is biased at halfway between device pinch-off and saturation region. Hence, the transistor operates during the complete cycle and the conduction angle $\alpha$ is $360^0$. As a result, the Class-A power amplifier operation is generally considered to be the most linear, because it operates between cutoff and saturation. The disadvantage is that its efficiency is low, with a theoretical maximum of 50%, as shown in Figure 2.3. So the Class-A PA is mostly used in those microwave systems that require extremely high linearity and that can afford the low efficiency.
For Class-B PAs, the quiescent point is at the threshold voltage of the device. Its conduction angle $\alpha$ is $180^\circ$, and its theoretical maximum efficiency is 78.5%. The linearity degrades somewhat because Class-B power amplifiers only conduct half of the cycle, while in theory also for Class B excellent linearity can still be obtained, this is less trivial than for Class A. Class-B power amplifiers are often implemented using a push-pull configuration, which uses two transistors in parallel; each amplifying one half of the RF input signal. In push-pull amplifiers, all even harmonics of the load current are cancelled.

The conduction angle $\alpha$ of Class-AB PAs is between $180^\circ$ and $360^\circ$. So its quiescent point can be chosen to make the device behave more like a Class-A or Class-B amplifier. This class allows a trade-off between linearity and efficiency. Class-AB power amplifiers can also be implemented using push-pull configuration.

Class-C power amplifiers are biased below the threshold voltage of devices, and hence the conduction angle $\alpha$ is between $0^\circ$ and $180^\circ$. Their efficiency can be high but this compromises somewhat their maximum output power. They are quite nonlinear in nature, so, they can be only used in applications whose linearity requirement is not too high, or they can be used together with linearization techniques.

The related output power and efficiency trends over the conduction angle are shown in Figure 2.3, from which conclusions above can be verified. The output powers of a comparable Class A and Class B are the same. However, the output power of Class AB is slightly larger than those of Class A and Class B, as depicted in Figure 2.3. Note that a reduction in conduction angle yields higher efficiency. Therefore the efficiency of Class AB is between the efficiencies of Class A and Class B. Taking linearity into account, Class AB is a compromise between Class A and Class B. Class C owns very high efficiency, but its output power is sharply reduced as a function of a shorter conduction angle.
2.1.2.2 Switch Mode PAs

Switch mode PAs can provide larger efficiencies than the transconductance PAs. In switch mode PAs, the transistor is driven by a large input signal (i.e. into compression), such that the transistor operates as a switch rather than as a current source. The overlap of the non-zero drain current and non-zero drain voltage versus time is minimized, yielding higher efficiencies. In principle, the drain efficiency of switch mode PAs can reach 100% without degrading output power. In practice, various loss mechanisms degrade the efficiency of switch mode PAs. In order to improve/restore the linearity of switch mode amplifiers, several advanced amplifier systems have been proposed, like LINC (Linear amplification using Nonlinear Components) and EER (Envelope Elimination and Restoration).

One of the most straightforward switch mode amplifier implementations is Class E, which uses transistor operated as an on-to-off switch. The drain current and voltage waveforms do not overlap simultaneously, which minimizes the power loss and maximizes the efficiency. [11] A typical Class-E circuit is shown in Figure 2.4. The device output capacitance is included in the shunt capacitor C. A series resonator, a reactive component jX, and a load
$R_L$ are connected in series. The series resonator resonates at the fundamental frequency, which makes the output signal to be sinusoidal. The reactive component $jX$ adjusts the phase shift between the output voltage in the load and the drain voltage.

Figure 2.4 Basic circuit of Class-E power amplifier

For the so-called “optimum-mode” operation, the zero voltage switching and zero slope switch conditions must be satisfied simultaneously [11]:

\[
V_{ds}(T) = 0
\]

\[
\left.\frac{dV_{ds}(T)}{dt}\right|_{t=T} = 0
\]

The main advantages of Class-E power amplifiers are soft switching, something that reduces the switching losses and their simpler circuit topology compared to Class-F power amplifiers. However, the main disadvantage of Class-E power amplifiers is the high peak drain voltage due to charging of the large shunt capacitor $C$. There are two methods to reduce this problem. The so-called “sub-optimum switch mode” can be used to reduce the peak drain voltage at the expense of dropping a little efficiency [12]. Another way is to use the transistors with higher breakdown voltages.

In Class-F PAs, harmonic traps are used to make the even harmonics and odd harmonics to be short and open, respectively. This can shape the drain waveforms, yielding a square wave for the drain voltage and a half-sinusoidal wave for the drain current. High efficiency can be
achieved because of the minimized overlapping of the two waves. The inverse Class F, which is also known as Class $F^{-1}$, is similar as Class F, but now the even harmonics are open, while odd harmonics are short circuited. So, the drain voltage is a half-sinusoidal wave and the drain current is a square wave, which also leads to high efficiency. In practice, it is impossible to connect an infinite number of harmonic tank resonators. Quarter-wave transmission lines are often used in Class-F and Class-$F^{-1}$ design. [13][14] The quarter-wave transmission line is equivalent to an infinite number of series-resonate circuit. The schematics of Class F and Class $F^{-1}$ using a quarter-wave transmission line and a LC tank are shown in Figure 2.5.

The quarter-wave transmission line can also provide some impedance transformation. Compared to Class E, the advantage of Class F is the low peak voltage and current, while its disadvantage is a complex load network.

Figure 2.5: The schematics of Class-F power amplifier and inverse Class-F power amplifier
To summarize, switch-mode PAs have higher efficiencies than transconductance PAs. However, they are inherently more narrowband, because all of them need resonators at the output tuned to the fundamental frequency. Class A is suitable for broadband amplifier design. For the efficiency consideration, Class AB bias like conditions can also be used in wideband PA design. Here the self biasing properties of the device can push it to Class-A operation at higher drive levels. In truly wideband amplifier design (more than octave), the harmonic matching condition (e.g. shorted 2\textsuperscript{nd} harmonics) can no longer be established without additional measures.

### 2.2 Conclusion

This chapter mainly presented some background concepts important for the thesis. Basic properties and classes of power amplifiers were discussed. It was described that Class A and Class AB operations are suitable for wideband power amplifier design. For efficiency consideration, Class AB is superior to Class A.
Amplifiers which are capable of providing high output powers over large bandwidths are mostly based on summing the power from multiple active devices. In this chapter, it is discussed that balanced amplifiers are very suitable for this purpose. In view of this, the first section of this chapter introduces 3-dB quadrature couplers, which are important components in the realization of the balanced amplifiers. The next section describes Wilkinson power dividers. Thirdly, balanced amplifiers will be explained and discussed. This section will also estimate the effect of imperfect balances. Finally, the power combining topology used within this project will be presented.

### 3.1 3-dB Quadrature Couplers

A 3-dB quadrature coupler is well known and widely used in microwave circuits such as balanced amplifiers [15], balanced mixers [16], and power dividers [17]. Before discussing the 3-dB quadrature couplers in detail, it is better to first introduce the main considerations of directional couplers (Figure 3.1).

![Figure 3.1 The symbol of a directional coupler](image)

Directional couplers are important passive microwave elements used for power splitting and combining. Their performance is characterized by four main parameters: coupling, through,
directivity, and isolation [18]. Coupling shows the fraction of input power that is coupled to the output port, while through states the part of input power that is directly transmitted to the output. Directivity indicates the coupler’s ability to isolate forward and backward waves, as is the isolation. Directivity is not directly measurable, but is calculated from the difference of the isolation and coupling measurements.

1) Coupling,

\[ C = 10 \log \frac{P_1}{P_4} = -20 \log |S_{31}| \text{ dB} \]  \hspace{1cm} (3.1)

2) Through,

\[ T = 10 \log \frac{P_2}{P_1} = 20 \log |S_{21}| \text{ dB} \]  \hspace{1cm} (3.2)

3) Directivity,

\[ D = 10 \log \frac{P_3}{P_4} = 20 \log |S_{34}| \text{ dB} \]  \hspace{1cm} (3.3)

4) Isolation,

\[ I = 10 \log \frac{P_1}{P_4} = -20 \log |S_{41}| \text{ dB} \]  \hspace{1cm} (3.4)

Where \( P_1, P_2, P_3, \) and \( P_4 \) are powers at the input, through, coupled, and isolated ports, respectively.

Hybrids are basically a kind of directional couplers, which are symmetrical networks. Even- and odd- mode analysis of symmetrical networks is discussed in appendix A. Generally, there are two groups of directional couplers, which are forward- and backward-wave directional couplers, as shown in Figure 3.2. Microstrip or stripline couplers are backward-wave couplers. [19] The specific discussion about forward- and backward-wave directional couplers is also shown in appendix A.
From [20], it is known that $S_{21}$ (through) and $S_{31}$ (coupling) of the backward-wave directional coupler (Figure 3.2 (b)) are shown in Equation (3.5) and (3.6), respectively.

\[
S_{21} = \frac{\sqrt{1-k^2}}{\sqrt{1-k^2 \cos \theta + jsin \theta}} \tag{3.5}
\]

\[
S_{31} = \frac{jksin \theta}{\sqrt{1-k^2 \cos \theta + jsin \theta}} \tag{3.6}
\]

Where $k$ is the coupling coefficient of the coupler and $\theta$ is the electrical length of the coupled-line.

\[
k = \frac{Z_{0e} - Z_{0o}}{Z_{0e} + Z_{0o}} \tag{3.7}
\]

\[
\theta = \beta l \tag{3.8}
\]

where $Z_{0e}$ and $Z_{0o}$ are the even-mode and odd-mode characteristic impedances of the coupled lines, respectively, $\beta$ is the phase constant, $l$ is the physical length of the coupled-line.

The necessary condition to ensure that all ports of the directional coupler are matched for any length $l$ and perfect isolation is [20]

\[
Z_{0e}Z_{0o} = Z_0^2 \tag{3.9}
\]

where $Z_0$ is the characteristic impedance to which the coupled lines are terminated.

From (3.7) and (3.9), the even- and odd-mode characteristic impedances can also be expressed as a function of the coupling coefficient $k$: 
\[ Z_{oe} = Z_0 \sqrt{\frac{1+k}{1-k}} \]  \hspace{1cm} (3.10)

\[ Z_{oo} = Z_0 \sqrt{\frac{1-k}{1+k}} \]  \hspace{1cm} (3.11)

Dividing Equation (3.6) by (3.5) gives,

\[ \frac{V_2}{V_2} = j \frac{k}{\sqrt{1-k^2}} \sin \theta \]  \hspace{1cm} (3.12)

Equation (3.12) shows that the voltage at the coupled port leads the voltage at the direct port by 90 degrees at all frequencies.

In the specific case of 3 dB couplers, the input power is equally split at the central frequency, this is

\[ k = \frac{1}{\sqrt{2}} \]  \hspace{1cm} (3.13)

When \( \theta = 90^\circ \) (at the central frequency), \( S_{21} = -\frac{1}{\sqrt{2}} \), \( S_{41} = \frac{1}{\sqrt{2}} \)  \hspace{1cm} (3.14)

Normally, the bandwidth of a directional coupler with a single section is small. Hence, a number of sections are required to be cascaded in order to achieve a wider bandwidth. Directional couplers with multiple sections are generally divided into two groups, symmetrical and asymmetric couplers. Asymmetric couplers may have any number of sections, while symmetric couplers only can have odd number of sections. E.G. Cristal and Leo Young have constructed tables for the design of optimum symmetrical TEM-mode coupled-transmission-line directional couplers [21], while Ralph Levy has generated similar tables for the design of TEM-mode asymmetric multi-element coupled-transmission-line directional couplers [22]. According to those tables, a pair of even and odd mode impedances can be found, based on which, the dimensions of each section can be calculated by some equations or CAD software. Figure 3.3 and Figure 3.4 depict the coupling factor and phase difference of two outputs over frequencies of single section, three symmetric section and three asymmetric section couplers. It can be observed that indeed a single section is narrowband, and asymmetric section couplers can get greater bandwidth than symmetric couplers for the same number of sections and same coupling ripples. The phase difference between the waves of through port and coupled port of single section and symmetric couplers is 90 degrees at all frequencies, while asymmetric couplers do not exhibit the same phase property. An important
limitation of multi-section couplers is that the increased number of sections results in an increased coupling at the center section, which could be even larger than -3 dB, yielding a fabrication problem.

Figure 3.3 Coupling of single section, three symmetrical section and three asymmetrical section couplers

Figure 3.4 Phase difference between the waves of through port and coupled port of single section, three symmetrical section and three asymmetrical section couplers

There are several types of 3 dB quadrature coupler implementations, such as the Lange couplers [23], edge-side microstrip couplers [24]. Figures 3.5 (a) and 3.5 (b) show the implementations of both the Lange coupler and the edge-side microstrip coupler, respectively. 3 dB couplers have several fabrication constrains, as 3 dB is a tight level of coupling. Therefore when aiming for microstrip implementations of tight coupling, the limits of a simple practical realization are always reached or exceeded. So, other technology
implementations are introduced to solve these problems, such as the vertical installed planar coupler-line configuration [25][26][27] (sees Figure 3.5 (c)), offset coupled striplines [28][29] (sees Figure 3.5 (d)), or the tandem coupler structure.

The tandem coupler structure, utilizes loosely coupled lines to form a 3 dB coupler, relaxing the width and spacing restrictions. As an example of the relaxation of restriction of the tandem coupler structure, two 8.34-dB couplers can be used to construct a 3-dB coupler. (note that -8.34 dB=20log sin(π/8).) The reason that a 3-dB coupler can be constructed by two 8.34-dB couplers will be discussed in appendix B in detail. Jeong-Hoon Cho has derived design equations for an N-section tandem coupler in [30]. For the tandem structure, a crossover connection is necessary. Hence, microstrip is not suitable to implement the tandem structure. However, when combined with symmetrical multi-section couplers, the tandem structure (shown in Figure 3.6), seems to be suitable to implement the wideband 3-dB 90° coupler in this project.
Figure 3.5 Several types of 3 dB quadrature coupler implementations
(a) Lange coupler in microstrip technology (b) Edge-side microstrip coupler
(c) Vertical installed planar coupler-line configuration (d) Offset coupled striplines configuration

Figure 3.6 A 3 dB quadrature coupler with the tandem structure
### 3.2 Wilkinson Power Dividers

The Wilkinson power divider was invented around 1960 by Ernest Wilkinson [31]. The divider can be designed with arbitrary power division, although in this work only the equal power distribution case (3 dB) is considered. Figure 3.7 shows the schematic of the Wilkinson divider. It splits an input signal into two output signals with equal phase, or combines two equal-phase signals into one. Two ports are matched at the output and are isolated by a resistor. In the ideal case of having a symmetrical loading on port 2 and port 3, there will be no voltage drop across the resistor, so no current will flow through it.

![Figure 3.7 The schematic of the Wilkinson coupler](image)

The S-matrix of the Wilkinson divider can be written as [20]:

$$S_{\text{wilkinson}} = \frac{-1}{\sqrt{2}} \begin{bmatrix} 0 & j & j \\ j & 0 & 0 \\ j & 0 & 0 \end{bmatrix}$$  \hspace{1cm} (3.15)

The bandwidth of a single section Wilkinson divider is quite narrow. Hence, multi-section topologies are required to increase the bandwidth. [32][33][34]
3.3 Balanced Amplifiers

3.3.1 Background Theory

The balanced amplifier configuration introduced by Eisele, et al. [35], is often used in microwave amplifiers. The configuration of a balanced amplifier is shown in Figure 3.8. Two identical single-ended amplifiers (A, B) are combined in parallel by two 3-dB quadrature couplers (also known as 90° hybrid couplers), respectively. Note that the 3-dB quadrature couplers are operated as a power splitter at the input and as a power combiner at the output.

![Figure 3.8 Configuration of a balanced amplifier](image)

Besides their use as power splitters and combiners, 3-dB quadrature couplers have some additional properties that are extremely useful in wideband PA design, which will be discussed next. In Figure 3.8, one port of the 90° hybrid coupler is terminated with a resistor. The scattering parameters of this 90° hybrid coupler including resistors (this is, seen as a 3-port network) is

\[
S_{\text{hybrid coupler}} = \frac{1}{\sqrt{2}} \begin{bmatrix}
0 & 1 & -j \\
1 & 0 & 0 \\
-j & 0 & 0
\end{bmatrix}
\]  

(3.16)

If the S-parameters of balanced amplifier are assumed as follows:

\[
S_T = \begin{bmatrix}
S_{11T} & S_{12T} \\
S_{21T} & S_{22T}
\end{bmatrix}
\]

(3.17)

Then the input reflection coefficient of the balanced amplifier is
\[ S_{11T} = \frac{1}{\sqrt{2}} \times \frac{1}{\sqrt{2}} S_{11A} + \frac{1}{\sqrt{2}} \times (-j) \times \frac{1}{\sqrt{2}} \times (-j) \times S_{11B} \]  

Hence, \[ S_{11T} = \frac{1}{2} (S_{11A} - S_{11B}) \]  

The remaining three scattering parameters can be found with the same procedure.

\[ S_{12T} = -\frac{1}{2} j(S_{12A} + S_{12B}) \]  

\[ S_{21T} = -\frac{1}{2} j(S_{21A} + S_{21B}) \]  

\[ S_{22T} = \frac{1}{2} (S_{22A} - S_{22B}) \]  

At the isolation port of the hybrid coupler, the combined reflected signals are given by

\[ \frac{1}{\sqrt{2}} \times \frac{1}{\sqrt{2}} \times (-j) \times S_{11A} + \frac{1}{\sqrt{2}} \times (-j) \times \frac{1}{\sqrt{2}} \times S_{11B} = \frac{(-j)}{2} (S_{11A} + S_{11B}) \]  

\[ \frac{1}{\sqrt{2}} \times \frac{1}{\sqrt{2}} \times (-j) \times S_{22A} + \frac{1}{\sqrt{2}} \times (-j) \times \frac{1}{\sqrt{2}} \times S_{22B} = \frac{(-j)}{2} (S_{22A} + S_{22B}) \]

If the two individual amplifiers (A, B) are identical, the input and output reflection coefficients should be zero. All unwanted reflected power is absorbed by the resistors (equal to the reference impedance), while the gain of the balanced amplifier is identical to that of the branch amplifiers.

### 3.3.2 Advantages and Disadvantages

The balanced amplifier has many advantages. Firstly, there is the remarkable property that the input and output matching of the entire balanced structure does not depend on the individual amplifying cells (Equations 3.19 & 3.22) as long as both amplifying cells are identical. This makes the balanced amplifier particularly useful in designing low noise amplifiers [36], broadband amplifiers [37] and power amplifiers [38]. In LNAs design, the input of the amplifying cell can be matched for optimum noise performance, which is not conjugate matched. In broadband amplifiers, the input of a single amplifying cell can be mismatched to achieve a flat gain without compromising the overall input matching of the entire structure.
Also, the output of the individual PAs can be matched for maximum output power or maximum efficiency, without affecting the matching of the total balanced PA. In all these three cases, the balanced amplifier provides a perfect impedance matching. Because of this reason, the balanced amplifier is very suitable for the wideband amplifier of this project, where high power and very wideband operation are desired. Secondly, the balanced amplifier can be easily cascaded with other components while maintaining low interstage reflections. Thirdly, the stability is significantly improved due to the perfect match. Fourthly, the 1-dB compression output power and saturation output power is twice of those of the single-ended amplifier. Fifthly, the system will still work if one of the two single-ended amplifiers broken, although in that case the gain will be reduced by 6 dB (note that -6 dB=20 log ($\frac{1}{\sqrt{2}}$, $\frac{1}{\sqrt{2}}$)).

Another important advantage is that the linearity is improved [39]. If a two-tone test is performed by exciting a system with two sinusoidal signals, the input voltages of the power amplifiers (A, B) shown in Figure 3.8 are $V_{l1}$ and $V_{l2}$, given by Equations (3.25) and (3.26).

$$V_{l1}(t) = A \cos(\omega_1 t) + A \cos(\omega_2 t)$$ (3.25)

$$V_{l2}(t) = A \cos \left( \omega_1 t + \frac{\pi}{2} \right) + A \cos \left( \omega_2 t + \frac{\pi}{2} \right)$$ (3.26)

In general, the relation between an input signal $x(t)$ and the output signal $y(t)$ for a system can be expressed by a power series as follows:

$$y(t) = a_1 x(t) + a_2 x^2(t) + a_3 x^3(t) + \cdots$$ (3.27)

Substituting Equation (3.25) and (3.26) into (3.27), the output voltages of power amplifiers (A, B) $V_{o,1}(t)$ and $V_{o,2}(t)$ are obtained.

$$V_{o,1}(t) = a_2 A^2 + \left( a_1 A + \frac{9}{4} a_3 A^3 \right) (\cos \omega_1 t + \cos \omega_2 t) + \frac{1}{2} a_2 A^2 (\cos 2\omega_1 t + \cos 2\omega_2 t) + \frac{1}{4} a_3 A^3 (\cos 3\omega_1 t + \cos 3\omega_2 t) + a_2 A^2 (\cos (\omega_2 + \omega_1) t + \cos (\omega_2 - \omega_1) t) + \frac{3}{4} a_3 A^3 \cos (2\omega_1 - \omega_2) t + \frac{3}{4} a_3 A^3 \cos (2\omega_1 + \omega_2) t + \frac{3}{4} a_3 A^3 \cos (2\omega_2 - \omega_1) t + \frac{3}{4} a_3 A^3 \cos (2\omega_2 + \omega_1) t$$ (3.28)
\[ V_{o,2}(t) = a_2A^2 + \left( a_1A + \frac{3}{4}a_3A^3 \right) \left( \cos(\omega_1 t + \frac{\pi}{2}) + \cos(\omega_2 t + \frac{3\pi}{2}) \right) + \frac{1}{2}a_2A^2 \cos(2\omega_1 t + \pi) + \cos(2\omega_2 t + \pi) + \frac{3}{4}a_3A^3 \left( \cos(3\omega_1 t + \frac{3\pi}{2}) + \cos(3\omega_2 t + \frac{3\pi}{2}) \right) + a_2A^2 \cos(\omega_2 + \omega_1 + \pi)t + \cos(\omega_2 - \omega_1)t + \frac{3}{4}a_3A^3 \cos \left( 2\omega_1 - \omega_2 + \frac{\pi}{2} \right) t + \frac{3}{4}a_3A^3 \cos \left( 2\omega_2 + \omega_1 + \frac{3\pi}{2} \right) t \]  
(3.29)

The output voltage of the power amplifier \( A \), \( V_{o,1}(t) \), undergoes another 90-degree phase shift after the output coupler.

\[ V'_{o,1}(t) = a_2A^2 + \left( a_1A + \frac{3}{4}a_3A^3 \right) \left( \cos(\omega_1 t + \frac{\pi}{2}) + \cos(\omega_2 t + \frac{\pi}{2}) \right) + \frac{1}{2}a_2A^2 \cos(2\omega_1 t + \frac{\pi}{2}) + \cos(2\omega_2 t + \frac{\pi}{2}) + \frac{3}{4}a_3A^3 \cos(3\omega_1 t + \frac{\pi}{2}) + \cos(3\omega_2 t + \frac{\pi}{2}) + a_2A^2 \cos((2\omega_1 + \omega_2)t + \frac{\pi}{2}) + \cos((2\omega_2 - \omega_1)t + \frac{\pi}{2}) + \frac{3}{4}a_3A^3 \cos((2\omega_1 - \omega_2)t + \frac{\pi}{2}) + \frac{3}{4}a_3A^3 \cos((2\omega_2 + \omega_1)t + \frac{\pi}{2}) \]  
(3.30)

According to Equations (3.29) and (3.30), the second order harmonics and intermodulation distortion products like \( \omega_2 + \omega_1, \omega_2 - \omega_1, 2\omega_1, 2\omega_2 \) are phase shifted by 90 degrees, and attenuated by 3 dB after the output coupler. Third order intermodulation distortion products and third order harmonics like \( 2\omega_2 + \omega_1, 2\omega_1 + \omega_2, 3\omega_1, 3\omega_2 \) are canceled out after the output coupler due to a 180 degree phase shift. However, the other third order intermodulation distortion products like \( 2\omega_2 - \omega_1, 2\omega_1 - \omega_2 \), are not canceled. These linearity improvements are based on ideal case. In practice, they are dependent on the characteristics of the real coupler.

The balanced amplifier also has some disadvantages. Compared to a single-ended amplifier, it requires extra structures such as the input and output couplers. Also, it needs two active devices instead of a single one, yielding a double periphery. Generally, this implies a large total dimension, due to the two couplers (especially at low frequencies), so the cost will increase. Also, the losses of the couplers result in a slightly higher noise figure of the LNAs and a lower PAE and output power of the PAs.
3.3.3 Effect of Imperfect Balance

In the previous discussion, 3-dB 90\(^\circ\) couplers and single-end power amplifiers in the balanced amplifier are assumed ideal and identical. However, this assumption never happens in reality. For instance, Equation (3.12) shows that the amplitude balance of 3-dB 90\(^\circ\) couplers varies with \(\sin^2\left(\frac{n\theta}{2\theta_0}\right)\). Hence, it is necessary to estimate the effects of imperfection, such as phase, amplitude, and gain imperfections. [39] has introduced an equation to evaluate those effects as follows

\[
\frac{P_{o,u}}{P_{o,e}} = \frac{1}{4} \left[ 1 + 2\delta \cos(\alpha) + \delta^2 \right] \tag{3.31}
\]

Where \(P_{o,e}\) is the output power if the two voltage components \((V_{out,1} and V_{out,2})\) at the output of the output coupler had equal amplitude and their phase difference \(\alpha = 0\), \(P_{o,u}\) is the output power when they are unequal and \(\alpha \neq 0\), and assumes \(\delta = V_{out,2}/V_{out,1} < 1\).

From Equation (3.31), the gain and phase imbalances’ influence on the overall gain is obtained. If the gain and phase imbalances are 1 dB and 15 degrees, which can exist in practice, the overall gain of the circuit is reduced by 0.56 dB. Hence, it can be noticed that the gain, phase, and amplitude imbalance will not greatly influence the total performance of the balanced amplifier.

3.3.4 Alternative Configuration of the Balanced Amplifier

There is another kind of balanced amplifier configuration shown in Figure 3.9 [7], using Wilkinson couplers and 90 degrees phase shift transmission lines.
Assume input signal is $V_\angle 0$, the reflected signals from the two single-ended amplifiers (A, B) across the isolation resistor of the input Wilkinson coupler is

$$\frac{V_\angle(-270)}{\sqrt{2}} \times S_{11A} + \frac{V_\angle(-90)}{\sqrt{2}} \times S_{11B} = \frac{j}{\sqrt{2}}(S_{11A} - S_{11B}) \quad (3.35)$$

If the two amplifiers (A, B) are identical, the reflected signals will be cancelled at the isolation resistor. The same is for the output. Thus, this kind of balanced amplifier also provides perfect match for both input and output.

A three-section wideband Wilkinson coupler connected with a quarter-wave transmission line is simulated from 0.7 GHz to 2.8 GHz in ADS. The schematic is shown in Figure 3.10.
From the simulation result, shown in Figure 3.11, it is observed that the phase difference between coupled waves is 90 degree only at the central frequency, and the phase unbalance is quite large in the rest of the bandwidth. Hence, this balanced amplifier topology is not suitable for wideband design.

### 3.4 Power Amplifier Topology on This Work

A very high power amplifier consists of a number of branches with single-ended power amplifiers. Each PA cell is fed by the signal split by the input power dividers, while the amplified signals are combined at the output. Figure 3.12 shows a typical topology of a high power amplifier. In some designs, high gain is required, so there are driver stages at the input of the high power amplifier. The dividers and combiners are required to be complementary to each other, this in order to make the signals combine in phase at the output. [40] Power combining networks shown in Figure 3.12 are called corporate networks [41]. This network not only can combine power, but also provide redundancy, that means, if one of the branch amplifiers fails, the overall network based amplifier still works, though with lower output power. And the number of devices combined in this way is binary.
The target of this project is to design a wide band high power amplifier, with a bandwidth of 2.1 GHz (0.7 GHz ~ 2.8 GHz) and 360 W output power. For this purpose, two 180 W Cree package devices (CGH40180PP) are used, each of which contains two die transistors in its package. Since the implementation of Wilkinson dividers is much cheaper than that of 3-dB quadrature couplers, hence, in order to reduce the cost, two Wilkinson dividers are used instead of 3-dB quadrature couplers at the appropriate places. The specific topology used in this project is depicted in Figure 3.13. Chapter 5 describes in detail the specific design of the 3-dB quadrature couplers as well as Wilkinson dividers. The design of the entire PA is further described in Chapter 6.
3.5 Conclusion

It is difficult to design a high power high bandwidth amplifier directly using a single device. The reason for this is that the input impedance and load of high power device become very small at high power levels (due to the large die size that supports such power levels), and hence they are not easy to match over a large bandwidth. Fortunately, high power high bandwidth amplifiers can be implemented by several lower power amplifiers together with power dividers and power combiners. The total input power is first split into several amplifying cells and then all the amplified singles are combined at the output. This can be done by a balanced amplifier which has other remarkable properties useful for wideband designs.
Wideband Power Amplifier Design

This chapter mainly discusses the design of wideband power amplifiers. First, two RF power technologies are introduced in section 4.1, which are GaN HEMTs (gallium nitride high electron mobility transistors) and silicon LDMOS FETs (laterally diffused metal oxide semiconductor field effect transistors). Then, section 4.2 presents the Bode Fano criteria, which gives the inherent bandwidth limitation of power amplifier devices due to the input and output matching [42]. After that, the two most commonly used wideband matching networks are described in section 4.3, namely multi-section LC matching networks and multi-section quarter-wave transformers. Section 4.4 illustrates three of the most commonly bandwidth enhancement techniques, which are: reactive matching, lossy matching and feedback. Subsequently, the design of two different broadband power amplifiers (using different device technologies) is presented. The first design employs a NXP LDMOS die transistor and it is presented in section 4.5. The second design, given in section 4.6, uses a Cree GaN packaged transistor.

4.1 RF Power Transistor Technologies

Nowadays LDMOS is considered as the industry-standard technology for RF power applications. LDMOS performance is continuously pushed to its limits realizing superb power and efficiency levels at ever increasing frequencies. [43] However, for higher frequencies and emerging switch-mode PAs, a new technology is required which can provide superior performance. At this moment, GaN is the technology that seems more suitable. The material properties of Si and GaN are listed in Table 4.1[44].
Table 4.1 Material properties of Si and GaN

<table>
<thead>
<tr>
<th>Property</th>
<th>Si (eV)</th>
<th>GaN (eV)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Bandgap energy</td>
<td>1.1</td>
<td>3.4</td>
</tr>
<tr>
<td>Breakdown field (V/cm)</td>
<td>$7 \times 10^5$</td>
<td>$35 \times 10^5$</td>
</tr>
<tr>
<td>Saturation velocity (cm/s)</td>
<td>$1 \times 10^7$</td>
<td>$2.2 \times 10^7$</td>
</tr>
<tr>
<td>Saturation field (V/cm)</td>
<td>$8 \times 10^3$</td>
<td>$15 \times 10^3$</td>
</tr>
<tr>
<td>Thermal conductivity (W/cm · k)</td>
<td>1.5</td>
<td>1.7</td>
</tr>
<tr>
<td>Electron mobility (cm²/V · s)</td>
<td>1350</td>
<td>1000</td>
</tr>
<tr>
<td>Hole mobility (cm²/V · s)</td>
<td>450</td>
<td>300</td>
</tr>
<tr>
<td>Dielectric constant</td>
<td>11.9</td>
<td>9.5</td>
</tr>
</tbody>
</table>

GaN owns outstanding material properties and is regarded as the next generation RF power transistor technology. GaN’s large breakdown voltage enables the device to have greater power densities than Si LDMOS, resulting in smaller transistor dies for equal higher output powers. Hence, for identical power levels, GaN HEMTs have smaller parasitic capacitances than Si LDMOS which implies larger input and load impedances. These higher impedances, allow broader operating bandwidths and simpler matching networks. Also, smaller parasitic capacitances make GaN more suitable for switch-mode PA designs. However, GaN is still far from being competitive with LDMOS in terms of cost.

In this project, both LDMOS FETs and GaN HEMTs have been considered. For LDMOS, two die models have been used from NXP Semiconductors: Gen7_050mm_050um and Gen7_TUD_050mm_050um. For GaN, a packaged device from Cree Inc. was employed, namely CGH40180PP. The difference between the models of Gen7_050mm_050um and Gen7_TUD_050mm_050um is that the second one assumes a thicker gate oxide. The advantage of using “naked” die devices is that it is possible to add dedicated wideband pre-matching networks into the package, yielding compact implementations with the proper design impedances. An example of a power device with internal prematch is illustrated in Figure 4.1.
4.2 Bode-Fano Limitation on Matching

Before going into details of discussing wideband impedance matching networks, it is important to understand the theoretical limits that constrain the performance of the impedance matching. The Bode-Fano criterion [46], [47] represents the optimum wideband matching result that can be ideally obtained.

The Bode-Fano criterion states for the theoretical maximum bandwidth a minimum matching condition (given by a reflection coefficient) can be realized for a given network, such as series or parallel RC networks, using ideal lossless matching networks (with infinite number of stages). This criterion is explained by considering Figures 4.2 and 4.3 for the case of series and parallel RC networks, respectively. This is relevant because the input of a LDMOS transistor can be simplified as a series RC network composed of the channel resistance \( r_i \) and the gate-source capacitance \( C_{gs} \). Similarly, the output of a LDMOS transistor can be simplified as a parallel RC network composed of the optimum load impedance \( R_L \) and the drain-source capacitance \( C_{ds} \).

![Figure 4.2 Bode-Fano network: RC series network](image)
\[
\int_{0}^{\infty} \frac{1}{\omega^2} \ln \frac{1}{|\Gamma(\omega)|} \, d\omega = \int_{\omega_1}^{\omega_2} \frac{1}{\omega^2} \ln \frac{1}{|\Gamma(\omega)|} \, d\omega = \frac{\Delta \omega}{\omega_1 \omega_2} \ln \left( \frac{1}{|\Gamma_{\text{min}}|} \right) < \pi r_1 C_{gs}
\]  

(4.1)

Then Equation (4.1) becomes

\[
\Delta \omega < \frac{\pi r_1 C_{gs} \omega_1 \omega_2}{(-\ln(|\Gamma_{\text{min}}|))}
\]  

(4.2)

Where \( \Gamma(\omega) \) is the reflection coefficient seen looking into the lossless matching network, and \( \Gamma_{\text{min}} \) is the minimum reflection coefficient in the frequency band \( (f_1 \sim f_2) \).

In the case of parallel RC networks (refer to Figure 4.3), the Bode-Fano limit is given by Equation (4.3).

![Lossless matching network diagram](image)

\[
\int_{0}^{\infty} \ln \frac{1}{|\Gamma(\omega)|} \, d\omega = \int_{\omega_1}^{\omega_2} \ln \frac{1}{|\Gamma(\omega)|} \, d\omega = \Delta \omega \ln \left( \frac{1}{|\Gamma_{\text{min}}|} \right) < \frac{\pi}{R_L C_{ds}}
\]  

(4.3)

Then Equation (4.3) becomes

\[
\Delta \omega < \frac{\pi}{-\ln(|\Gamma_{\text{min}}|) R_L C_{ds}}
\]  

(4.4)

To illustrate an application of the Bode-Fano criterion, a NXP LDMOS FET die was used as an example, specifically the model for the Gen7_050mm_050um device. For this, the intrinsic transistor parameters for this device were extracted from its simulation model using the procedure indicated in [48], assuming a central frequency \( (\omega_0 = \sqrt{\omega_1 \omega_2}) \) of 1.8 GHz, and are given in Table 4.2.

<table>
<thead>
<tr>
<th>( C_{gs} )</th>
<th>( r_1 )</th>
<th>( C_{ds} )</th>
<th>( R_L^* )</th>
</tr>
</thead>
<tbody>
<tr>
<td>44 pF</td>
<td>0.386 Ohm</td>
<td>14 pF</td>
<td>3.9 Ohm</td>
</tr>
</tbody>
</table>

* The value of \( R_L \) will be explained in detail in section 4.5.
Using Equations (4.2) (4.4), the theoretical maximum bandwidths at different matching conditions (i.e. different input and output reflection coefficients) are shown in Table 4.3.

Table 4.3 The theoretical maximum bandwidths versus different input and output reflection coefficients

<table>
<thead>
<tr>
<th>( \Gamma_{\text{min}} ) (dB)</th>
<th>Input (GHz)</th>
<th>Output (GHz)</th>
</tr>
</thead>
<tbody>
<tr>
<td>-20</td>
<td>0.472</td>
<td>3.98</td>
</tr>
<tr>
<td>-14</td>
<td>0.675</td>
<td>5.69</td>
</tr>
<tr>
<td>-8</td>
<td>1.186</td>
<td>9.99</td>
</tr>
</tbody>
</table>

Since the targeted bandwidth in this project is larger than 2 GHz, from the discussion above, it is noticed that the input matching of the design using NXP Gen7_050mm_050um devices is a big challenge, while the output matching is easier to obtain.

4.3 Wideband Matching Networks

Two most commonly used wideband matching networks are introduced, namely multi-section LC matching networks and multi-section quarter-wave transformers.

4.3.1 Multi-section LC Matching Networks

Before the multi-section LC matching network is discussed, a single section LC matching network is introduced.

The Q-factor of any matching network is given by

\[ Q = \frac{f_0}{\Delta f} \]  \hspace{1cm} (4.5)

Where \( f_0 \) and \( \Delta f \) are the central frequency and frequency bandwidth, respectively. Then, according to Equation (4.5), the bandwidth of those networks is inversely proportional to their Q-factor value.
The Q-factor of the matching network topology of Figure 4.4, assuming \( R_s > R_L \), is:

\[
Q = \sqrt{\frac{R_s}{R_L} - 1} \quad (4.6)
\]

For given \( R_s \) and \( R_L \), the Q of the network is defined meaning a fixed bandwidth.

In order to increase the bandwidth, more LC networks must be cascaded with virtual resistances between each network as shown in Figure 4.5, assuming also \( R_s > R_L \). The virtual impedances can be decided by distributing the impedance transformation ratio equally among \( N \) sections.

\[
\frac{R_s}{R_1} = \frac{R_1}{R_2} = \frac{R_2}{R_3} = \cdots = \frac{R_{n-1}}{R_L} = \left( \frac{R_s}{R_L} \right)^{\frac{1}{N}} \quad (4.7)
\]

Then, the Q-factor of an N-section LC matching network is given by:

\[
Q = \sqrt{\left( \frac{R_s}{R_L} \right)^{\frac{1}{N}} - 1} \quad (4.8)
\]

From Equation (4.11), it can be observed that the Q–factor of the network is reduced for an increased number of sections, resulting in a wider bandwidth. The discussion above only dealt with the transformation of real impedances. For complex impedances, the reactance can be absorbed into the individual LC sections of the matching networks.

Figure 4.5 Multi-section LC matching network (\( R_s > R_L \))
4.3.2 Multi-section Quarter-wavelength Transformers

A multi-section quarter-wavelength transformer, shown in Figure 4.6, is usually used to match real impedances over wide bandwidths. Each section has a different characteristic impedance but the same electrical length, which is one quarter of a wavelength at the central frequency.

![Multi-section Quarter-wavelength Transformer](image)

Figure 4.6 A multi-section quarter-wave transformer

4.4 Bandwidth Enhancement Techniques

For a bilateral device, the operating power gain $G_p$ is given by [7]

$$G_p = \frac{1}{1-|\Gamma_{IN}|^2} |S_{21}|^2 \left( \frac{1-|\Gamma_{L}|^2}{1-|S_{22}|^2|\Gamma_{L}|^2} \right)$$  (4.9)

Where $\Gamma_{IN}$ and $\Gamma_{L}$ are input and load reflection coefficients, respectively. $S_{21}$ and $S_{22}$ are S-parameters of the device.

The device’s gain decreases with frequency (usually 20 dB /decade). According to Equation (4.9), in order to obtain a constant gain over a broad frequency range, the input matching network of the PAs is required to be designed properly, while the output is matched for maximum power or maximum efficiency. There are various techniques that can be used to achieve a wider bandwidth. In this section, the three most common bandwidth enhancement techniques are discussed: reactive matching, lossy matching and feedback.

4.4.1 Reactive Matching

The flat gain design concept of reactive match approach is illustrated by Figure 4.7. In order to obtain the flat gain over the whole bandwidth between $f_1$ and $f_2$, the gain at every
frequency in the bandwidth is increased or decreased by matching or mismatching at the input. So, the reflection loss is monotonically decreasing with frequency. Constant gain circles [7] are normally used for the design of matching conditions to accomplish this gain adjustment. This can be done with the aid of proper transistor models and simulation software such as Agilent ADS. However, it is important to estimate some rough values for the elements of the circuit before any optimization.

![Figure 4.7 Illustration of the flat gain design concept of reactive match approach](image)

The main disadvantage of this approach is that the voltage standing-wave ratio (VSWR) can be high, which is bad when cascading other components. This problem can be solved by the balanced structure (already discussed in Section 3.3), as both the input and output matching are improved as discussed. For the reactive matching technique, the matching networks can use lumped inductors and capacitors or transmission lines. This technique is used in one of the designs of this thesis, as discussed in section 4.5.

### 4.4.2 Lossy Matching

In the lossy match approach, resistors are used to absorb overhead in gain in order to achieve a flat gain over the whole frequency range. In addition, resistors also improve the amplifier stability. Normally, the lossy match amplifier exhibits a better impedance match at its input. Figure 4.8 shows some commonly used lossy matching network solutions.
The R-L shunt network, as depicted in Figure 4.8 (a), is the most typical lossy matching network solution. At low frequencies, the inductor’s impedance is very small, so the resistor reduces the gain. However, at high frequencies, the resistor has little effect on reducing the gain because the impedance of the inductor increases. Hence, the gain roll-off is compensated by the R-L shunt network due to its positive gain slope.

The theory how the R-L shunt network makes the gain flat has been qualitatively explained. Here, it will be analyzed in another way. A circuit schematic of a power amplifier with the R-L shunt network is shown in Figure 4.9. In this circuit, multi-section LC networks are used,
although, multi-section quarter-wave transmission lines or a combination of both of them can also be used. The input part of this amplifier and its equivalent circuit are shown in Figure 4.10 and Figure 4.11, respectively. The output part of this amplifier is depicted in Figure 4.12. Because $r_1$ is very small, it can be neglected in Figure 4.11. Then the equivalent circuit in Figure 4.11 is exactly a multi-section LC matching network that transforms the resistor $R$ to reference impedance $Z_0$. This indicates that lossy power amplifiers with the R-L shunt network can easily have a good input match over the desired bandwidth, as long as the values of $R$ and $L$ are chosen carefully. According to Section (4.3.1), the impedance at the gate node is equal to a virtual resistance ($R_{\text{virtual}}$) in Figure 4.11. In addition, the multi-section network is lossless, hence $v_g$ is constant over frequency based on Equation (4.10).

$$v_g = \sqrt{2R_{\text{virtual}}P_{\text{avs}}} \quad (4.10)$$

At the drain node, and for a linear PA class, the power at the drain node, is

$$P_{\text{drain}} = \frac{1}{2}\left(g_m v_g\right)^2 R_{\text{opt}} \quad (4.11)$$

Where $R_{\text{opt}}$ is the optimum load impedance for maximum output power.

The output matching network absorbs the drain-source capacitance ($C_{\text{ds}}$), and is also lossless. Therefore, the power at the output port is the same as the power at the drain node. Then, according to Equation (2.2), at these conditions the gain will be flat over the whole frequency range. For the purpose of this project, only the R-L shunt and R shunt networks are analyzed, however, other lossy matching networks can also be analyzed in a similar way.

![Figure 4.9 A circuit schematic of a power amplifier with the input R-L shunt network](image-url)
4.4.3 Feedback

Feedback is another method to achieve broad bandwidth. In addition, it can improve the input and output match, and stability by reducing gain at low frequencies. Figure 4.13 shows some kinds of feedback networks. Consider the transistor with series-shunt feedback resistors, as shown in Figure 4.13 (c). From [7], the expressions of $S_{21}$, $R_1$ and $R_2$ are obtained, as depicted in Equations (4.12), (4.13), and (4.14). Equation (4.12) indicates that $S_{21}$ only
depends on $R_1$. However, the feedback resistor consumes power, and so it should be able to dissipate the heat. For very high power designs, such as in this project, the feedback approach is not suitable.

\[
S_{21} = \frac{Z_{0} - R_1}{Z_{0}} \quad \text{(4.12)}
\]

\[
R_1 = Z_{0}(1 + |S_{21}|) \quad \text{(4.13)}
\]

\[
R_2 = \frac{Z^2_{0}}{R_1} - \frac{1}{g_m} \quad \text{(4.14)}
\]

Figure 4.13 Several different kinds of feedback networks

4.5 Design Version I Using NXP LDMOS Die Transistors

In this section, wideband single-ended amplifiers are designed using the two different transistor die models from NXP, namely LDMOS Model Gen7_050mm_050um and LDMOS Model Gen7_TUD_050mm_050um. The difference between them is that the Gen7_TUD_050mm_050um model assumes a thicker gate oxide, yielding a lower
gate-source capacitance. To study the effect of gate-source capacitances on matching, R shunt lossy matching networks are used in the design with the two different models. The gains of the designed power amplifiers with different values of shunt resistors are also investigated. To compare the performance of using R shunt and R-L shunt networks, they are used separately in the design with LDMOS Model Gen7_050mm_050um. Class-A operation is chosen in this design version, because the objective is to build broadband instrumentation amplifiers which require high linearity. This design version was not implemented; it was only simulated for research purpose. Hence, the input and output are matched to intermediate real impedances instead of 50 Ohm. For a real design, the conversion from those intermediate real impedances to 50 Ohm is still required. However, this is easy to realize by using multi-section transmission line or LC networks. The desired bandwidth for these designs is 2.4 GHz (0.6 ~ 3 GHz).

4.5.1 DC Characteristics

For LDMOS Model Gen7_050mm_050um:

The transfer characteristic of the LDMOS device Gen7_050mm_050um is shown in Figure 4.14. From the curve of \( I_D \sim V_G \) at the drain voltage \( V_D = 28V \), it can be seen that the gate voltage should be 3.5V for Class A mode operation.

![Figure 4.14 The transfer characteristic of Gen7_050mm_050um for 28V drain bias](image-url)
For LDMOS Model Gen7_TUD_050mm_050um:

The transfer characteristic of Gen7_TUD_050mm_050um is shown in Figure 4.15. The supply voltage is 28 V with a quiescent drain current of about 4.5 A which corresponds to a Class-A operation. The gate voltage should be 6.75V.

![Figure 4.15 The transfer characteristic of Gen7_TUD_050mm_050um for 28V drain bias](image)

4.5.2 Load-line Analysis

The load-line method [10], is an easy and effective method to design a power amplifier. However, the load line technique can be applied only to the intrinsic device but not to a packaged device, because the waveforms at the package terminals and those at the intrinsic device are greatly different [40]. Figure 4.16 illustrates the load line of a device for a class-A operation. To obtain the maximum power from the device, the load-line is chosen as the optimum line, as shown in Figure 4.16, so that the device operates between the maximum allowed drain to source voltage at one extreme and the maximum allowed drain current at the other extreme. By definition, the device in Class-A mode is biased at point Q (V_Q = V_DD, I_Q = I_max/2). Hence, the optimum load resistance is,

\[ R_{opt} = \frac{V_{DD} - V_{Knee}}{I_{max}/2} = \frac{8P_{max}}{I_{max}^2} \]  \hspace{1cm} (4.15)

Where \( V_{Knee} \) is the knee voltage, \( I_{max} \) is the maximum drain current, and \( P_{max} \) is the
maximum output power.

If the load impedance is smaller than optimum load impedance ($R_L < R_{opt}$), the power device will swing over the current up to $I_{max}$ which is typically limited by the device. The current is the same as that at the optimum load. However, due to the reduced voltage swing at the load, the output power and efficiency degrade accordingly. On the other hand, if the load impedance is larger than optimum load impedance ($R_L > R_{opt}$), the voltage swing is limited by the breakdown voltage of the device. The output power and efficiency also degrade because of reduced current swing at the load.

![Load-line of a device for a Class-A operation](image)

Figure 4.16 Load-line of a device for a Class-A operation

The load-lines of the LDMOS Models Gen7_050mm_050um and Gen7_TUD_050mm_050um are shown in Figure 4.17, and optimum load impedances for those devices are 3.9 Ohm and 4.8 Ohm, respectively.
4.5.3 Using a R-L Shunt Matching Network

The designed power amplifier with the LDMOS Model Gen7_050mm_050um uses an input matching based on the R-L shunt network. The circuit schematic of this design topology is shown in Figure 4.18. The input is matched for maximum power transfer, and the prematch network is used to convert the impedance of $C_{gs}$ and $R_i$ series network to an intermediate
real impedance, which is chosen as 4 Ohm. The output is the load line matched. As discussed in Section 4.5.2, the optimum load impedance was found as 3.9 Ohm for this design. Because of $C_{ds}$ and $L_5$, the optimum impedance is transformed to about 3.5 Ohm, seen at the output terminal of the package. Table 4.4 lists the values of all relevant components in this design. The simulation results are presented in Figure 4.19. The gain of the designed PA is $17.5 \pm 0.5$ dB in the operating bandwidth (0.6 to 3.0 GHz). The circuit is unconditionally stable as seen in Figure 4.19 (b). At 1.8 GHz (mid-band), the 1-dB compression output power is about 46 dBm.

Table 4.4 The values of important components in the schematic of R-L shunt matching topology

<table>
<thead>
<tr>
<th>Component</th>
<th>Value</th>
<th>Component</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>$L_1$</td>
<td>277 pH</td>
<td>$C_1$</td>
<td>1 pF</td>
</tr>
<tr>
<td>$L_2$</td>
<td>346 pH</td>
<td>$C_2$</td>
<td>25 pF</td>
</tr>
<tr>
<td>$L_3$</td>
<td>247 pH</td>
<td>$C_3$</td>
<td>25 pF</td>
</tr>
<tr>
<td>$L_4$</td>
<td>66 pH</td>
<td>$C_4$</td>
<td>2.75 nF</td>
</tr>
<tr>
<td>$L_5$</td>
<td>200 pH</td>
<td>$C_5$</td>
<td>1 pF</td>
</tr>
</tbody>
</table>

Figure 4.18 The schematic for simulation of lossy match: R-L shunt network
The prematching network can be made in the package to achieve a more compact design. Originally, the capacitor $C_1$ should be 11 pF, however, the lead capacitance is about 1 pF. Hence, two transmission lines (TL$_1$ and TL$_2$), whose characteristic impedances and electrical lengths at the central frequency are 11 Ohm and 31.5 degree respectively, are used to realize the extra 10 pF capacitance. The inductors are constructed by bondwires. HFSS is used to implement the package indicated in Figure 4.18, and a 3D view of such a package is shown in Figure 4.20. The total physical length of the package (L), not accounting for the leads, would be 5.5 mm.
4.5.4 Using a R Shunt Matching Network

Using R-L lossy matching strategy can provide a good return loss in a larger bandwidth. However, the disadvantage of this implementation is that there is coupling effect between inductors $L_3$ and $L_4$. The coupling effect degrades the input return loss of the designed circuit, and causes the stability issue. Hence, another lossy matching strategy, namely R shunt matching, can be used. To analyze the performance obtained with this R shunt matching, both the LDMOS Models Gen7_050mm_050um and Gen7_TUD_050mm_050um were used in the design. The circuit schematic of this new design is shown in Figure 4.21. Several different values of the resistor are chosen to compare the performance of the designed power amplifiers, especially with respect to the gain.
Design with the LDMOS Model Gen7_050mm_050um:

The schematic for the specific design is shown in Figure 4.22. The resistor R is chosen as 1.4 Ohm, which is the same as the resistor chosen in the R-L design topology. The output is also based on the load line method. Because of $C_{ds}$ and $L_4$, the optimum impedance is transformed to about 3.5 Ohm as well. The input is also matched to the same intermediate real impedance (4 Ohm) as in the former design. The values of the important components of the circuit shown in Figure 4.22 are listed in Table 4.5. The simulation results are shown in Figure 4.23. In the same operating bandwidth as the previous design, the gain is $17 \pm 1$ dB. This circuit is also unconditionally stable. At 1.8 GHz, the 1-dB compression output power is 46.15 dBm.

Table 4.5 The values of important components in the schematic of R shunt matching topology for LDMOS Model Gen7_050mm_050um

<table>
<thead>
<tr>
<th>Component</th>
<th>Value</th>
<th>Component</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>$L_1$</td>
<td>241 pH</td>
<td>$C_1$</td>
<td>21 pF</td>
</tr>
<tr>
<td>$L_2$</td>
<td>224 pH</td>
<td>$C_2$</td>
<td>41 pF</td>
</tr>
<tr>
<td>$L_3$</td>
<td>138 pF</td>
<td>$C_3$</td>
<td>49 pF</td>
</tr>
<tr>
<td>$L_4$</td>
<td>200 pH</td>
<td>$C_4$</td>
<td>2.75 nF</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$C_5$</td>
<td>1 pF</td>
</tr>
</tbody>
</table>

Figure 4.22 The schematic for simulation of lossy match: R shunt network for LDMOS Model Gen7_050mm_050um (R=1.4 Ohm)
In order to analyze the influence of the shunt resistor $R$ with the gain, other values were tested: $R=2$ and $3 \, \text{Ohm}$. The different gains of power amplifiers with different values of shunt resistors are shown in Table 4.6. It was observed in simulations that a stability issue can arise when the gain of the amplifier is increased by using a resistor larger than 2.

Table 4.6 The different gains of power amplifiers with different values of shunt resistors (LDMOS Model Gen7_050mm_050um)

<table>
<thead>
<tr>
<th>The value of shunt resistor (Ohm)</th>
<th>$S_{21}$ (dB)</th>
</tr>
</thead>
<tbody>
<tr>
<td>1.4</td>
<td>16.8</td>
</tr>
<tr>
<td>2.0</td>
<td>18.1</td>
</tr>
<tr>
<td>3.0</td>
<td>19.8</td>
</tr>
</tbody>
</table>
Design with the LDMOS model Gen7_TUD_050mm_050um:

The schematic for this design with the LDMOS model Gen7_TUD_050mm_050um is shown in Figure 4.24. In this case, the resistor R was chosen as 3 Ohm, which is also one of the values used for the design with the Gen7_050mm_050um model. The output is also based on the load line method. Because of C_{ds} and L_3, the optimum impedance is transformed to about 3.7 Ohm. The input is matched to 6 Ohm. Table 4.7 shows the values of the components in Figure 4.24. The simulation results are shown in Figure 4.25. For this design, a gain of only 10.8 ± 1 dB can be achieved in the desired bandwidth. Although this circuit is also unconditionally stable, its stability seems better than the design with LDMOS model Gen7_050mm_050um with the same shunt resistor value. At 1.8 GHz, the 1-dB compression output power is about 46.3 dBm.

Table 4.7 The values of important components in the schematic of

R shunt matching topology for LDMOS Model Gen7_TUD_050mm_050um

<table>
<thead>
<tr>
<th>Component</th>
<th>Value</th>
<th>Component</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>L_1</td>
<td>355 pH</td>
<td>C_1</td>
<td>13 pF</td>
</tr>
<tr>
<td>L_2</td>
<td>241 pH</td>
<td>C_2</td>
<td>28 pF</td>
</tr>
<tr>
<td>L_3</td>
<td>267 pH</td>
<td>C_3</td>
<td>2.75 nF</td>
</tr>
<tr>
<td></td>
<td></td>
<td>C_4</td>
<td>1 pF</td>
</tr>
</tbody>
</table>

Figure 4.24 The schematic for simulation of lossy match: R shunt network for the LDMOS Model Gen7_TUD_050mm_050um (R=3 Ohm)
4.5.5 Conclusion from previous designs

In this section, two lossy matching networks were investigated. In principle, with the R-L shunt matching technique is easier to achieve a good input return loss in the desired wide bandwidth. However, the coupling between the shunt inductor and other nearby inductors in a realistic matching network implementation degrades the input return loss and stability of the circuit. Additionally, the R-L shunt matching implementation is more complicated. Because of this, the R shunt matching is preferred. Also, a larger shunt resistor can be chosen to increase the gain, but if the value is too large, the stability will become a problem.

Comparing the simulation results between the two NXP transistor models, it was found that wideband matching is easier for the second model, Gen7_TUD_050mm_050um (R=3 Ohm).
design with the same second model is easier to stabilize than the design with the first model, Gen7_050mm_050um. However, the gain obtained with the Model Gen7_TUD_050mm_050um design is smaller than that of the Model Gen7_050mm_050um design.

Also, from the previous designs, a topology for a wideband amplifier design using the NXP devices is illustrated in Figure 4.26. In the same transistor package, the LDMOS device should be integrated with a shunt resistor and bias decoupling network as well as some input pre-match to intermediate real impedances.

Since as at the moment this work was carried out, NXP did not have any of the studied LDMOS devices ready, a packaged transistor was used instead. The wideband power amplifier design with this device is discussed in the next section.

![Figure 4.26 The total schematic of the proposed power amplifier](image)

**4.6 Design Version II Using Cree GaN Packaged Transistors**

For this PA design, the Cree GaN packaged transistor was employed, specifically CGH40180PP. In this case, a Class-AB operation was selected, as a workable compromise between linearity and efficiency. This design was finally implemented and measured, as later discussed in Chapter 6.
4.6.1 DC Characteristic

The DC transfer characteristic of the CGH40180PP device is shown in Figure 4.27. The supply voltage is 28 V with a quiescent drain current of 1A which corresponds to Class-AB operation. For these operation conditions, the gate-source voltage should be -2.85 V.

![Figure 4.27 The transfer characteristic of CGH40180PP for 28V drain bias](image)

4.6.2 Load-pull Analysis

Source- and load-pull simulations were carried for this GaN device, and Figure 4.28 shows the simulation setup in Agilent ADS. Similarly to the load-line technique, the source/load-pull technique is also an important tool for the design of matching networks. Table 4.8 shows the optimum load and source impedances found after repeating source/load-pull simulations at different frequencies.

![Figure 4.28 The Load-pull simulation setup](image)
Table 4.8 The optimum source and load impedances versus frequencies

<table>
<thead>
<tr>
<th>Freq [GHz]</th>
<th>$Z_S$ [Ohm]</th>
<th>$Z_L$ [Ohm]</th>
</tr>
</thead>
<tbody>
<tr>
<td>0.7</td>
<td>0.5+j4.8</td>
<td>1.96-j0.5</td>
</tr>
<tr>
<td>1.0</td>
<td>1.8+j4.1</td>
<td>2.56-j2.0</td>
</tr>
<tr>
<td>1.3</td>
<td>3.6+j2.6</td>
<td>3.06-j2.9</td>
</tr>
<tr>
<td>1.6</td>
<td>2.7+j0</td>
<td>2.78-j3.5</td>
</tr>
<tr>
<td>1.9</td>
<td>2.63-j3.9</td>
<td>2.21-j2.7</td>
</tr>
<tr>
<td>2.2</td>
<td>2.53-j3.6</td>
<td>2.31-j2.9</td>
</tr>
<tr>
<td>2.5</td>
<td>2.03-j3.8</td>
<td>2.41-j3.2</td>
</tr>
<tr>
<td>2.8</td>
<td>1.89-j5.3</td>
<td>3.26-j4.3</td>
</tr>
</tbody>
</table>

4.6.3 Matching Network Design

The actual input and output matching networks were implemented using microstrip lines, in a PCB whose substrate was Roger RO4003C with a thickness of 0.203 mm. A reference impedance ($Z_0$) of 25 Ohm was used, as required for 3 dB quadrature couplers, that are further explained in chapter 5. For the intended complete high power amplifier design, several single-ended power amplifiers will be cascaded with 3 dB quadrature couplers and these couplers are terminated at 25 Ohm. The output matching network is first designed and synthesized by ADS for maximum output power, and its circuit is shown in Figure 4.29. The input matching network is mismatched to achieve the flat gain, and its circuit is depicted in Figure 4.30. The stabilization network is also shown in Figure 4.30, which consists of a resistor ($R_2$), the feed inductor ($L_1$), and a capacitor ($C_1$). In addition, a small resistor ($R_1$) is added to further improve the stability, as well as the bandwidth. Microstrip curved bends are used to make the matching network compact considering the complete intended PA implementation (which include several PA cells).

By following the design procedure discussed previously, initial element values can be obtained, and then the final design parameters are found by an overall optimization of all amplifier design parameters by using ADS. For all SMD components implementing lump elements, comprehensible and substrate-dependent models were employed (provided by Modelithics), such as to include all parasitic effects.
4.6.4 Simulation Performance

The schematic simulation results of the designed power amplifier are shown in Figure 4.31. \( P_{avS} \) is chosen as 40 dBm for this simulation. It is observed that a gain of \( 13 \pm 1 \) dB can be achieved in the operating bandwidth. For the stand-alone PA cell, the input return loss is not
very good versus the overall bandwidth. However, this input return loss will be greatly improved for the overall amplifier which uses a balanced amplifier topology. Output saturation power is about $49.4 \pm 0.4$ dBm, and the designed power amplifier is unconditionally stable.

Figure 4.31 The schematic simulation results of the designed power amplifier
In chapter 3, 3-dB quadrature couplers and Wilkinson dividers were introduced. This chapter will focus on the design and implementation of these hybrids. First, the design of two topologies of 3-dB quadrature couplers is discussed in section 5.1. Section 5.2 presents the design of Wilkinson dividers. At last, the conclusion of this chapter is provided.

5.1 3-dB Quadrature Coupler Design

As discussed in chapter 3, a fabrication problem exists when designing couplers of tight coupling levels using conventional edge coupled microstrip lines. This problem can be overcome by using an offset coupled stripline configuration or a vertically installed planar (VIP) coupler-line configuration.

5.1.1 Offset Stripline Configuration

An offset stripline configuration is a structure to achieve tight value of coupling. The cross section of the offset stripline is shown in Figure 5.1. The stripline is much more difficult and expensive to fabricate compared to the microstrip line since multilayer PCBs will be required. In order to reduce the fabrication cost of the structures for this project, a multilayer substrate is created out of three individual simpler double layer substrates which are later stacked, as shown in Figure 5.2. The PCB material of all these three substrates is Rogers RO4003C. Both the thicknesses of substrates 1 and 3 are Sub1=Sub3=0.813mm, while the thickness of substrate 2 is Sub2=0.203mm. The parameters for the offset stripline are listed in Table 5.1.
As discussed previously, multi-section couplers are required for larger bandwidths. However, their disadvantage is that the coupling value of their center section becomes very tight, resulting in fabrication issues. As discussed in Chapter 3, a tandem coupler structure can be used to overcome this problem. In addition, the offset stripline configuration is very suitable for the tandem structure due to its crossover characteristic. As a result, in this design, two 8.34 dB couplers are cascaded to construct a 3 dB coupler. According to the tables listed in [21],

<table>
<thead>
<tr>
<th>Parameters</th>
<th>Values</th>
</tr>
</thead>
<tbody>
<tr>
<td>Relative dielectric constant, $\varepsilon_r$</td>
<td>3.55</td>
</tr>
<tr>
<td>Relative permeability, $\mu_r$</td>
<td>1</td>
</tr>
<tr>
<td>Ground plane spacing, $H$</td>
<td>1.969 mm</td>
</tr>
<tr>
<td>Inter-layer spacing, $S$</td>
<td>0.203 mm</td>
</tr>
<tr>
<td>Conductor thickness, $T$</td>
<td>70 um</td>
</tr>
<tr>
<td>Conductor conductivity, $\sigma$</td>
<td>5.8e7 S/m</td>
</tr>
<tr>
<td>Dielectric loss tangent, $\delta$</td>
<td>0.0021</td>
</tr>
</tbody>
</table>

Table 5.1 The parameters for the offset stripline
each coupler consists of three sections, all are designed with a quarter wavelength line at the central frequency of the desired bandwidth, and corresponding normalized even-mode characteristic impedances are shown below.

\[ Z_{e1,3} = 1.11, \quad Z_{e2} = 1.79 \]  

(5.1)

The values of conductor widths (W), offsets (W_o) and conductor lengths can be calculated using the ADS tool Linecalc. Normally, the reference impedance is 50 Ohm. However, if 50 Ohm is chosen, the conductor widths of the sections would be smaller than 0.8 mm for the chosen substrate thickness, and this would not be safe for high power designs (due to practical limits on the current handling capability of the PCB traces). Another more important problem is that the width offsets of both section 1 and 3 are relatively large, which causes the two yellow conductors and two brown conductors as shown in Figure 5.3 to disconnect from each other (C, D).

![Figure 5.3 The layout of a 8.34 dB coupler based on 50 Ohm reference impedance](image)

Therefore, in this project, 25 Ohm is chosen as the reference impedance. The corresponding even- and odd- mode impedances, and physical dimensions of each section of the -8.34 dB offset stripline coupler are shown in Table 5.2. Another advantage of choosing 25 Ohm as the reference impedance is that the input and output of the power amplifier part in the balanced amplifier can be matched to 25 Ohm, instead of 50 Ohm, which simplifies the high power amplifier design.

<table>
<thead>
<tr>
<th>Freq (GHz)</th>
<th>C (dB)</th>
<th>Ripple (dB)</th>
<th>Section</th>
<th>Z_{oe} (Ohm)</th>
<th>Z_{oo} (Ohm)</th>
<th>W (mm)</th>
<th>W_o (mm)</th>
<th>L (mm)</th>
</tr>
</thead>
<tbody>
<tr>
<td>0.7-2.8</td>
<td>8.34</td>
<td>+/- 0.4</td>
<td>I = 1,3</td>
<td>27.65</td>
<td>22.60</td>
<td>2.69</td>
<td>3.05</td>
<td>22.74</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>I = 2</td>
<td>44.84</td>
<td>13.94</td>
<td>1.83</td>
<td>1.18</td>
<td>22.74</td>
</tr>
</tbody>
</table>
The layout of the design 3 dB offset stripline coupler is shown in Figure 5.4. Because of practical considerations, four small extra pieces of conductors are added to join section 1 and 2, as illustrated in Figure 5.4. For the sake of cascading with other components, some vias are added to make the two connecting conductors of the stripline to be on the same plane.

![Figure 5.4 The layout of the designed 3 dB offset stripline coupler in momentum](image)

ADS momentum is used to do the EM simulation, which considers all discontinuity effects and other unwanted couplings between the two tandem -8.34 dB couplers. The momentum simulation result is shown in Figure 5.5. The return loss and isolation are both better than 16 dB. The amplitude balance is ±1 dB for a frequency range from 0.7 to 2.7 GHz, while it is -1.43 dB at 2.8 GHz. Phase balance is $90 \pm 3.7^\circ$ over the desired bandwidth (0.7-2.8 GHz).
Figure 5.5 The momentum simulation results of the designed 3 dB offset stripline coupler
(a) $S_{21}$ and $S_{31}$ (b) $S_{11}$ and $S_{41}$ (c) Amplitude balance (d) Phase difference

The three stacked dielectric substrates used to form the multilayer PCB of the coupler are firmly fixed by vertical screws. In addition, many vias are required between the bottom and top metal conductors of each PCB to enable ground to be present at the bottom-most and top-most layer of the entire structure. Also, shielding can be made with vias such as to eliminate unwanted coupling between two different sections of the coupler coupled regions. A more comprehensible layout is depicted in Figure 5.6, showing these grounding vias and screws. Due to the real implementation, the etched metal of the conducting layers will contain air instead of dielectric material. For this reason, 3D EM simulations were performed in Ansoft HFSS to evaluate the overall coupler performance, including air gaps (the air gap is much harder to simulate in ADS momentum). Also, in order to really analyze the effect of the air layer, the same structure was simulated without air (i.e. only the RO4003C substrate) in HFSS for comparison. However, due to practical simulation issues, HFSS simulations used
vertical metal sheets to represent the real grounding due to vias and screws, this in order to save simulation times. The structure that was simulated in HFSS is shown in Figure 5.7 where the grounding metal sheets can be observed in the middle of the ground plates.

![Figure 5.6 The modified layout of the designed -3 dB offset stripline coupler in momentum](image)

![Figure 5.7 The structure of the designed -3 dB offset stripline coupler in HFSS](image)

The HFSS simulation results of the designed 3 dB offset stripline coupler without air and with air in the structure are shown in Figure 5.8. Comparing the HFSS simulation result of the structure without air (sees Figure 5.8 (a) (c)) with momentum simulation result (sees Figure 5.5), the amplitudes of coupling and direct through become a little worse. The reason is that HFSS simulation is full wave simulation, which includes the radiation loss. The phase
difference also degrades, especially at the higher frequency. Comparing the results depicted in Figure 5.8, the present of air in the structure improves the electrical performance a bit.

Monte Carlo simulations are very useful to analyze the effect of process variations [49]. Some Monte Carlo simulations were performed for the coupler in this work using process variations on the components of the couplers. For the conducting PCB traces, the width was assumed to have a variation up to 25 um as stated by the PCB manufacturer. Among the three PCB substrates, the variation on thickness of the middle one (substrate 2) is more critical since it influence the coupling of each coupler section and it is the thinnest one. A variation of up to 1 mil is specified in substrate 2 by the substrate manufacturer. The combined effect of these two process variations was analyzed in the Monte Carlo simulation depicted in Figure 5.9. It is found that the amplitude balance is greatly dependent on these two parameters, while the phase difference is not so sensitive to them.

Figure 5.8 The comparison of HFSS simulation results of the designed 3 dB offset stripline coupler without air (a) (c) and with air in the structure (b) (d)
5.1.2 Vertically Installed Planar Configuration

This part will not be shown in this version of report.

5.2 Wilkinson Divider Design

As mentioned in Section 3.4, Wilkinson dividers are required for splitting and combining the input and output power, respectively, in the total amplifier topology. The design of a single-section Wilkinson power divider is well known [18]. However, its frequency bandwidth is limited. Also in this case, multiple sections are needed to design broader band Wilkinson couplers. The design theory for multi-section three port hybrids has been proposed by S. B. Cohn and design tables have been published. [54]

Although more sections result in a larger bandwidth, more losses will also be introduced. So, there is a trade-off between losses and bandwidth. Additionally, using more sections will
require a larger space. For the bandwidth requirements of this project (0.7-2.8 GHz), three section Wilkinson dividers were designed. In the overall design, the Wilkinson dividers are cascaded with the two 3-dB quadrature couplers discussed in the previous section, whose port reference impedance is 25 Ohm. Hence, the two output port reference impedances are chosen as 25 Ohm, while the input port reference impedance is chosen as 50 Ohm based on characterization considerations. Because of these different impedances, the design tables in [54] can’t be used directly, since they were proposed for the case of having the same reference impedances at all the ports. The main design algorithm for a multi-section three-port hybrid like the one of this project is based on optimum design of stepped transmission line transformer. [55] Computer aided design software (ADS) is utilized to assist the Wilkinson divider design. The three resistors used in the Wilkinson divider design are chosen as 120 Ohm. These resistors play a key role in the splitter performance in terms of output matching and isolation.

The schematic of the designed Wilkinson divider with ideal components is depicted in Figure 5.22. Figure 5.23 shows the simulation results. Note that $S_{21}$ and $S_{31}$ are the same, -3±0.25 dB, while both $S_{22}$ and $S_{33}$ are smaller than -18.4 dB. Isolation and return loss are better than 17.9 dB and 12 dB, respectively. The phase difference of the two outputs is almost zero degrees.
Figure 5.2 The schematic of the designed impedance transforming Wilkinson divider with ideal components

Figure 5.22 The schematic simulation of the impedance transforming Wilkinson divider using ideal components (a) $S_{21}$ and $S_{31}$ (b) $S_{22}$, $S_{33}$ and $S_{32}$ (c) $S_{11}$ (d) Phase difference
The design can be implemented using microstrip lines. The substrate is 0.813 mm-thick Roger RO4003C as used also in other components of the entire amplifier. The ADS tool Linecalc is used to obtain the physical dimensions of the lines. Bends and T-junctions are added to make the designed Wilkinson divider more compact. The layout of the designed impedance transforming Wilkinson divider in HFSS is shown in Figure 5.24.

![Figure 5.24 The structure of the designed impedance transforming Wilkinson divider in HFSS](image)

The HFSS simulation results of the designed Wilkinson divider are shown in Figure 5.25. $S_{21}$ and $S_{31}$ are almost the same, $-3 \pm 0.47$ dB. Both $S_{22}$ and $S_{33}$ are smaller than $-14.9$ dB. Isolation and return loss are better than $14.9$ dB and $10.6$ dB, respectively. Both amplitude and phase differences between the two outputs are very small.
Figure 5.25 The HFSS simulation results of the designed impedance transforming Wilkinson divider

5.3 Conclusion

This chapter discussed the design and implementation of two versions for a 3 dB quadrature coupler and an impedance transforming Wilkinson divider for the specified bandwidth (0.7-2.8 GHz).

For the 3 dB coupler, VIP topology has advantages over offset stripline configuration, such as low cost and ease of tuning. However, the conventional VIP coupler has two outputs located at different output sides of the structure, making it impractical for cascading other components in a system. Hence, a novel VIP coupler with a crossover is designed whose two outputs are at the same output side. Compensating capacitances are connected to the coupler lines to improve the overall performance of the designed coupler. Multiple sections and the tandem structure are used to achieve a wide bandwidth and tight coupling without fabrication problems. Monte Carlo simulations indicated that PCB parameter variations can affect the performance of the designed coupler, specially the amplitude balance.
For the Wilkinson power divider/combiner, multiple sections were also employed to obtain a larger bandwidth. Additionally, the reference impedance of the two outputs was selected as 25 Ohm due to the following 3 dB couplers.
A 360 W 0.7-2.8 GHz Wideband GaN Instrumentation Amplifier

High power amplifiers and wide band amplifiers have been introduced in Chapter 3 and 4, respectively. In this chapter, the design and implementation of a 360 W 0.7-2.8 GHz wideband instrumentation amplifier using GaN transistors is discussed. The simulation and measurement results are also presented.

6.1 Circuit Design

The topology of the designed amplifier is shown in Figure 6.1, as introduced in Chapter 3. It contains two Wilkinson dividers, four 3-dB quadrature couplers and four single-ended PAs. The design of those PAs has been presented in Chapter 4, and the design of the Wilkinson dividers and 3-dB quadrature couplers have been described in Chapter 5. Those components have been used, as represented in Figure 6.1, to form a wideband high power amplifier. The total layout of the designed amplifier, using an offset stripline 3-dB coupler, is shown in Figure 6.2. A second layout version of the designed amplifier with 3-dB couplers using the VIP configuration instead of offset stripline configuration, is shown in Figure 6.3.

Figure 6.1 The proposed topology of the desired amplifier
Figure 6.2 The layout of the designed amplifier (version I)
Figure 6.3 The s layout of the designed amplifier (version II)
6.2 Simulated Performance

The simulation results of the individual parts as well as the total amplifier are presented next. The operating bandwidth is 0.7 to 2.8 GHz.

I Single-ended PA:

The simulation results of the single-ended amplifiers using Momentum simulation data for the passive structures are shown in Figure 6.4. $P_{\text{avg}}$ is chosen as 40 dBm in this simulation. The designed power amplifier is unconditionally stable. It is observed that a flat gain of about $13 \pm 1$ dB can be achieved in the operating bandwidth. Output saturation power is $49.5 \pm 0.5$ dBm.

Figure 6.4 The simulation results of the single-ended amplifiers using Momentum simulation data for the passive structures (a) $S_{21}$ and $S_{11}$ (b) Output power (c) Stability k factor (d) $\mu$ factor
II Single-ended PA + Impedance Transformers:

As discussed in Chapter 4, the input and output port impedances of the designed single-ended PAs are 25 Ohm. Hence, if the single-ended PAs are required to be measured separately, wideband impedance transformers (transforming from 25 Ohm to 50 Ohm) are needed, their layout is shown in Figure 6.5. The PCB substrate is Rogers RO 4003C with the thickness of 0.813 mm.

![Figure 6.5 The layout of impedance transformers](image)

The simulation results of the single-ended PA connected to the wideband impedance transformers at the input and output are shown in Figure 6.6. $P_{\text{avg}}$ is chosen as 40 dBm for this simulation. The small signal gain is almost the same as that of the previous simulation. An unpredictably 1 dB drop for the output power appears at the 2 GHz compared with that of the previous simulation.

![Simulation Results](image)
III 3-dB Quadrature Couplers:

- **Offset stripline configuration**

It can be noticed from Figure 6.2 that the layout of the 3-dB quadrature coupler using offset stripline configuration has been modified compared with the layout shown in Figure 5.6. Figure 6.7 shows the simulated structure. The pink part of the layout is the microstrip line, which was added for connecting to the rest of the circuit. The isolation port (bottom right) is altered to make some space for the isolation resistors (two 50 Ohm resistors in parallel).
The HFSS simulation results of this coupler are depicted in Figure 6.8. The return loss and isolation are both better than 18.75 dB. Amplitude balance is ±1.38 dB in the desired frequency bandwidth. Phase balance is 90 ± 6.7° over the same bandwidth.

![Graphs of HFSS simulation results showing return loss and isolation](image)

**Figure 6.8** The HFSS simulation results of the modified layout of the 3-dB quadrature coupler using the offset stripline configuration

(a) $S_{21}$ and $S_{31}$ (b) $S_{11}$ and $S_{41}$ (c) Amplitude balance (d) Phase difference

- **Vertically Installed Planar Configuration**

A vertically installed planar 3-dB coupler was designed also in order to test its performance and compare it with the offset stripline coupler. In order to be able to replace the offset stripline 3-dB quadrature coupler with the 3-dB quadrature coupler using VIP configuration, both layouts must be “pin compatible”, therefore the layout of the VIP coupler is shown in Figure 6.9. Note that the actual required PCB area for the VIP coupler in reality is much smaller than the offset stripline coupler.
The HFSS simulation results of this structure are shown in Figure 6.10. The return loss and isolation are both better than 20 dB. Amplitude balance is $\pm 1$ dB in the frequency range of 0.7 to 2.7 GHz, while it is -2 dB at 2.8 GHz. Phase balance is $90 \pm 1.4^\circ$ over the same bandwidth. Both amplitude and phase balance are better than those of the previous coupler.
IV Wilkinson Dividers:

In the total amplifier, the outputs of the original layout of the Wilkinson divider (refer to Figure 5.24) need to be extended to connect the inputs of the 3 dB quadrature couplers, as shown in Figure 6.2 & Figure 6.3. The Momentum simulation results of the modified layout of the Wilkinson divider are shown in Figure 6.11. $S_{21}$ and $S_{31}$ are almost the same, $-3\pm 0.5$ dB. Both $S_{22}$ and $S_{33}$ are smaller than $-15.7$ dB. Isolation and return loss are better than 17.3 dB and 11 dB, respectively. Both amplitude and phase imbalances between the two outputs are almost zero.

![Figure 6.11 The Momentum simulation results of the modified layout of the Wilkinson divider](image)

(a) (b) (c) (d)
V Single-ended PAs + 3-dB Quadrature Couplers (Balanced Amplifier):

For the amplifier in this project, the GaN devices were chosen in the package (CGH40180PP). This package contains two GaN devices (with independent Gate and Drain leads). The reason for choosing this package was to make the total design more compact and with lower cost. However, actually this package is not very suitable for balanced amplifier designs. The two die transistors inside the CGH40180PP package are close enough such as to present some coupling between them, presumably this is due to the bondwires connecting the gate and drain leads of each device. This phenomenon degrades the performance of the designed PA in certain conditions. If the two devices are driven in phase or out-of-phase, this parasitic effect does not affect the performance. However, if those transistors are excited with signals in quadrature, the parasitic coupling affects the most. This coupling has been taken into account in the large signal model of CGH40180PP which was provided, however it was not expected. Some capacitors (3 pF) were added between the two gates of the transistors, and the same for the drains, to kill the apparently magnetic parasitic coupling in the desired bandwidth as much as possible.

(1) Balanced Amplifier I

The simulation results of the balanced amplifier are depicted in Figure 6.12. The 3-dB quadrature coupler is the one using the offset stripline configuration. $P_{\text{avg}}$ is chosen as 43 dBm for this simulation. It can be observed from Figure 6.12 that the saturation output power in the bandwidth (0.7~2.6 GHz) is $52.3\pm0.6$ dBm. However, the gain and output power are worse at higher frequencies. There may be three reasons for this: first, it is due to the coupling in the package (the effect described earlier); second, it is because of the loss of the 3-dB quadrature coupler; third, the imperfect balance also degrades somewhat the performance (as discussed in Chapter 3). The input return loss is improved, especially at lower frequencies, and the stability is also improved, compared with those of the single-ended amplifier.
Figure 6.12 The simulation results of the balanced PA I
(a) $S_{21}$ and $S_{11}$ (b) Output power (c) Stability k factor (d) $\mu$ factor

(2) Balanced Amplifier II

For this balance amplifier, the VIP 3-dB quadrature coupler is used instead of the offset stripline one. The simulation results of the balanced amplifier are depicted in Figure 6.13. In this case, $P_{\text{avg}}$ is chosen as 43 dBm for the simulation. Figure 6.13 shows the simulation results. The saturation output power in the bandwidth (0.7~2.6 GHz) is 52.6±0.7 dBm, and also degrades in the bandwidth from 2.6 GHz to 2.8 GHz. Both the input return loss and stability are also improved compared with those of the single-ended amplifier.
VI Wilkinson dividers + single-ended PA s+ 3-dB quadrature Couplers:

(1) Total Amplifier I

In this total amplifier, the 3-dB quadrature coupler is the one using the offset stripline configuration. $P_{av8}$ is chosen as 46 dBm for this simulation. The simulation results are shown in Figure 6.14. The saturation output power in the bandwidth (0.7~2.6 GHz) is $54.9 \pm 0.9$ dBm, facing some degradation from 2.6 GHz to 2.8 GHz. The loss of the Wilkinson dividers further degraded the output power. The designed total PA is unconditionally stable.
Figure 6.14 The simulation results of the total PA I
(a) $S_{21}$ and $S_{11}$ (b) Output power (c) Stability $k$ factor (d) $\mu$ factor

(2) Total Amplifier II

The 3-dB quadrature coupler in this total amplifier is the one using the VIP configuration. $P_{\text{av}}$ is chosen as 46 dBm for this simulation. Figure 6.15 depicts the simulation results. The output power in the bandwidth (0.7~2.6 GHz) is $54.9 \pm 1$ dBm. The designed total PA is unconditionally stable.
Figure 6.15 The simulation results of the total PA II
(a) $S_{21}$ and $S_{11}$ (b) Output power (c) Stability $k$ factor (d) $\mu$ factor

6.3 Measurements

Measurement is still carrying on, and the measurement results will be available soon.
7 Conclusion and Recommendations

7.1 Conclusion

The objective of this work was to build a high power wideband amplifier for instrumentation purpose. To reach the objective of high power, Chapter 3 explored the balanced amplifier, and a power combining topology for this thesis work was also presented.

Large periphery devices, such as high power LDMOS and GaN transistors, are demanded in this project. However, very large peripheries imply large input/output capacitances limiting the bandwidth. In addition, their optimal load impedances are quite low. It was investigated in Chapter 4 that the input matching of the design using LDMOS transistors is a big challenge. For identical power levels, GaN transistors have smaller parasitic capacitances, which makes the wideband matching easier compared to LDMOS FETs. However, the targeted bandwidth within this project is very large. In view of this, two bandwidth extension methods (lossy matching and reactive matching) were explored. Among the lossy matching networks, R-L shunt and R shunt networks were analyzed in this work. With these matching techniques, a quite flat gain in the bandwidth from 0.6 GHz to 3 GHz can be obtained for the designed amplifier (using NXP die LDMOS transistors). In principle, the R-L shunt matching technique is better for wideband matching than the R shunt matching technique. However, the coupling between the shunt inductor and other nearby inductors in a realistic matching network implementation will degrade the input return loss and stability of the circuit. Additionally, the R-L shunt matching implementation is more complicated. Because of this, R shunt matching is preferred.

Using this R shunt matching technique, two different transistor die models from NXP, namely
LDMOS Model Gen7_050mm_050um and LDMOS Model Gen7_TUD_050mm_050um, were employed in this design study. The second model assumes a thicker gate oxide, which means a lower gate-source capacitance. It was found that wideband matching is easier with the second model. In addition, it is also easier to stabilize. However, the gain obtained with the Model Gen7_TUD_050mm_050um design is smaller than that of the Model Gen7_050mm_050um design. A design topology for a wideband amplifier design using the NXP device was also proposed in Chapter 4.

Another bandwidth extension method (reactive matching) was studied for the amplifier design with a packaged device from Cree Inc. An acceptable flat gain and high power can be achieved in the bandwidth (0.7~2.8 GHz). The return loss of this designed amplifier is not very good versus the overall bandwidth. However, it can be greatly improved in the total amplifier design which uses a balanced amplifier topology. This is the design that was implemented in practice during this work.

Within this thesis work, attention was also given on the 3 dB wideband quadrature couplers, which are important components in the realization of the balanced amplifier. Two kinds of implementations of these couplers, namely offset stripline configuration and VIP configuration, were presented in Chapter 5. The conventional VIP configuration coupler is not suitable for this project because their two outputs are located at different sides of the structure, making it impractical for cascading other components in a system. In Chapter 5, a novel VIP coupler with a crossover was designed whose two outputs are at the same side. Compensating shunt capacitances were connected to the coupler lines to improve the overall performance of the designed coupler.

In the total topology, two Wilkinson dividers are used instead of the 3-dB quadrature couplers at the appropriate places in order to reduce cost and lower the complexity of the amplifier implementation. The input port impedances of these Wilkinson dividers are 50 Ohm, while their output port impedances are 25 Ohm, as required by the PA cells and the quadrature couplers. Hence, a wideband impedance transforming Wilkinson divider was designed and
implemented in Chapter 5.

In Chapter 6, the layouts of two versions of the high power wideband amplifier design were presented. Simulated and measured performances of the individual parts as well as the total amplifier were also presented.

7.2 Recommendations

The design presented in this thesis is only a first step toward realizing a true high power (1 kW) wideband compact instrumentation amplifier. Based on our experiences and new insights, there are several suggestions for future work:

1. Each transistor in the PA cell should be contained in a separate package in order to eliminate parasitic coupling through the bondwires (connecting devices to the package leads), which currently causes an important performance drop in quadrature operation. For example, two Cree packaged device CGH40120F should be used instead of one packaged device (CGH40180PP) that contains two transistors.

2. In Chapter 4, it was shown that the bandwidth of the designed amplifier (using NXP LDMOS die transistors) with lossy matching can be very high (more than 2.4 GHz). Additionally, according to the simulation with the Model Gen7_050mm_050um, high gain can be achieved (more than 17 dB). The most important however, is that LDMOS devices are much cheaper than GaN devices. In view of this, LDMOS transistors can be used in the design instead of GaN transistors.

3. The final version of the instrumentation amplifier requires high gain (more than 50 dB). For this purpose, multi-stage power amplifiers are needed to be designed, or some pre-amplifiers are need to be added into the design topology (refer to Figure 3.12).

4. The total design should be compact, to save the board space and relax the size requirement for the heatsink. In order to make the total design more compact,
high-dielectric constant PCB substrate can be employed for the PA sections of the design, which also lower the losses. Due to high $\varepsilon_r$ PCB substrate, together with individual packaged transistors, it is possible that the height of the PA PCB substrate can be the same as that of the couplers, which can reduce the interface complexity between the boards. In addition, wideband lumped-element quadrature 3-dB couplers can be investigated to reduce the dimensions of the coupler sections.

5. Also a modified topology of the design is proposed, as shown in Figure 7.1. In its corresponding layout, the length of the connections in the output combiner is minimized, which is good for reducing the loss, although that of the input divider is increased. It is still good for the design, since gain always comes cheaper than power.

Figure 7.1 Modified design topology with reduced output losses
Even- and Odd-mode Analysis of Symmetrical Networks

A.1 Even- and odd- mode analysis of symmetrical networks

A four-port symmetrical network is shown in Figure A.1. PP’ is a plane of symmetry. The relationship between incident and reflected voltage waves at different ports of the network as shown in Figure A.1 can be expressed as

\[
\begin{bmatrix}
V_1^- \\
V_2^- \\
V_3^- \\
V_4^-
\end{bmatrix} = [S] \begin{bmatrix}
V_1^+ \\
V_2^+ \\
V_3^+ \\
V_4^+
\end{bmatrix} 
\]  
(A.1)

where

\[
[S] = \begin{bmatrix}
S_{11} & S_{12} & S_{13} & S_{14} \\
S_{21} & S_{22} & S_{23} & S_{24} \\
S_{31} & S_{32} & S_{33} & S_{34} \\
S_{41} & S_{42} & S_{43} & S_{44}
\end{bmatrix} 
\]  
(A.2)

![Figure A.1 A four-port symmetrical network](image-url)

The network is symmetrical and reciprocal, so...
\[ S_{21} = S_{12}, \ S_{31} = S_{13}, \ S_{41} = S_{14}, \]
\[ S_{32} = S_{23}, \ S_{42} = S_{24}, \ S_{43} = S_{34}, \]
\[ S_{33} = S_{11}, \ S_{44} = S_{22}, \ S_{34} = S_{12}, \ S_{23} = S_{14} \]

The scattering matrix of the network can be therefore expressed as

\[
[S] = \begin{bmatrix}
S_{11} & S_{21} & S_{31} & S_{41} \\
S_{21} & S_{22} & S_{41} & S_{42} \\
S_{31} & S_{41} & S_{11} & S_{21} \\
S_{41} & S_{42} & S_{21} & S_{22}
\end{bmatrix}
\]

(A.3)

\[
[S] = \begin{bmatrix}[S_A] \\
[S_B]
\end{bmatrix}
\]

(A.4)

where

\[
[S_A] = \begin{bmatrix} S_{11} & S_{21} \\
S_{21} & S_{22} \end{bmatrix}
\]

(A.5)

\[
[S_B] = \begin{bmatrix} S_{31} & S_{41} \\
S_{41} & S_{42} \end{bmatrix}
\]

(A.6)

Equation (A.1) then becomes

\[
\begin{bmatrix}
V_1^- \\
V_2^- \\
V_3^- \\
V_4^-
\end{bmatrix} = \begin{bmatrix}[S_A] & [S_B] \end{bmatrix} \begin{bmatrix} V_1^+ \\
V_2^+ \\
V_3^+ \\
V_4^+
\end{bmatrix}
\]

(A.7)

If the symmetrical ports 1 and 3 are connected to equal magnitude and in-phase sources, the voltages not only at ports 1 and 3 but also at ports 2 and 4 will be equal in magnitude and in phase. This is called even-mode excitation. But if the symmetrical ports 1 and 3 are connected to equal magnitude and out-of-phase sources, the voltage at ports 1 and 3 will be equal in magnitude and out-of-phase. Similarly, the voltages at ports 2 and 4 will be equal in magnitude and out-of-phase. This is called odd-mode excitation.

For even-mode excitation:

\[ V_3^\pm = V_1^\pm = V_{1e}^\pm, \quad V_4^\pm = V_2^\pm = V_{2e}^\pm \]
\[
\begin{bmatrix}
V_{1e}^- \\
V_{2e}^- \\
V_{1e}^+ \\
V_{2e}^+
\end{bmatrix} =
\begin{bmatrix}
[S_A] & [S_B]
\end{bmatrix}
\begin{bmatrix}
V_{1e}^+ \\
V_{2e}^+
\end{bmatrix}
\] 

(A.8)

Hence,

\[
\begin{bmatrix}
V_{1e}^- \\
V_{2e}^-
\end{bmatrix} = [S_e]
\begin{bmatrix}
V_{1e}^+ \\
V_{2e}^+
\end{bmatrix} = ([S_A] + [S_B]) \begin{bmatrix}
V_{1e}^+ \\
V_{2e}^+
\end{bmatrix}
\] 

(A.9)

For odd-mode excitation:

\[
V_1^\pm = -V_3^\pm = V_{1o}^\pm, \quad V_2^\pm = -V_4^\pm = V_{2o}^\pm
\]

\[
\begin{bmatrix}
V_{1o}^- \\
V_{2o}^- \\
-V_{1o}^+ \\
-V_{2o}^+
\end{bmatrix} =
\begin{bmatrix}
[S_A] & [S_B]
\end{bmatrix}
\begin{bmatrix}
V_{1o}^+ \\
V_{2o}^+
\end{bmatrix}
\] 

(A.10)

Hence,

\[
\begin{bmatrix}
V_{1o}^- \\
V_{2o}^-
\end{bmatrix} = [S_o]
\begin{bmatrix}
V_{1o}^+ \\
V_{2o}^+
\end{bmatrix} = ([S_A] - [S_B]) \begin{bmatrix}
V_{1o}^+ \\
V_{2o}^+
\end{bmatrix}
\] 

(A.11)

From Equation (A.9) and (A.11),

\[
[S_A] = \frac{[S_e] + [S_o]}{2}
\] 

(A.12)

\[
[S_B] = \frac{[S_e] - [S_o]}{2}
\] 

(A.13)

Assumes

\[
[S_e] = \begin{bmatrix}
S_{11e} & S_{21e} \\
S_{21e} & S_{22e}
\end{bmatrix}
\] 

(A.14)

\[
[S_o] = \begin{bmatrix}
S_{11o} & S_{21o} \\
S_{21o} & S_{22o}
\end{bmatrix}
\] 

(A.15)

Equation (A.12) and (A.13) then can be written as

\[
[S_A] = \begin{bmatrix}
\frac{S_{11e} + S_{11o}}{2} & \frac{S_{21e} + S_{21o}}{2} \\
\frac{S_{21e} + S_{22o}}{2} & \frac{S_{22e} + S_{22o}}{2}
\end{bmatrix}
\] 

(A.16)
\[
[S_B] = \begin{bmatrix}
\frac{S_{11e} - S_{11o}}{2} & \frac{S_{21e} - S_{21o}}{2} \\
\frac{S_{21e} + S_{21o}}{2} & \frac{S_{22e} + S_{22o}}{2}
\end{bmatrix}
\] (A.17)

According to Equation (A.4), the scattering parameters are shown as follows:

\[S_{11} = \frac{S_{11e} + S_{11o}}{2}, \quad S_{12} = S_{21}, \quad S_{13} = S_{31}, \quad S_{14} = S_{41}\]

\[S_{21} = \frac{S_{21e} + S_{21o}}{2}, \quad S_{22} = \frac{S_{22e} + S_{22o}}{2}, \quad S_{23} = S_{41}\]

\[S_{24} = \frac{S_{22e} - S_{22o}}{2}, \quad S_{31} = \frac{S_{11e} - S_{11o}}{2}, \quad S_{32} = S_{41}\]

\[S_{33} = S_{11}, \quad S_{34} = S_{21}\]

\[S_{41} = \frac{S_{21e} - S_{21o}}{2}, \quad S_{42} = S_{24}, \quad S_{43} = S_{21}, \quad S_{44} = S_{22}\] (A.18)

### A.2 Forward-wave and back-wave directional couplers

A directional coupler is depicted in Figure A.2. If all ports of a four-port network are matched, a symmetrical four-port network can behave as a directional coupler. Because the network is symmetrical, matching of ports 1 and 2 automatically ensures that ports 3 and 4 are also matched. Therefore, the condition is

\[S_{11} = S_{22} = 0\] (A.19)

According to Equation (A.18), there are two possibilities to meet that condition.

**Case 1**

\[S_{11e} = S_{11o} = S_{22e} = S_{22o} = 0\] (A.20)

If Equation (A.20) is substituted into Equation (A.18),

\[S_{13} = S_{31} = S_{42} = S_{24} = 0\] (A.21)
Hence, there is no power that will be coupled to port 3. But power is coupled to port 4. This kind of couplers is called forward-wave directional couplers.

Case 2

If $S_{11e} = -S_{11o} \neq 0$, $S_{22e} = -S_{22o} \neq 0$, the condition ($S_{11} = S_{22} = 0$) can also be obtained. From Equation (A.19), it is found that $S_{31} \neq 0$ and $S_{42} \neq 0$. Hence, power is coupled to port 3. To ensure that no power is coupled to port 4, $S_{21e} = S_{21o}$ is required, which is easily satisfied if the coupler lines are of the TEM type. In this case, this type of couplers is called backward-wave directional couplers.
Analysis of a Two-section Tandem Coupler

A two-section tandem coupler is shown in Figure B.1. The up and bottom parallel-coupled lines are the same.

According to Appendix A, the relationship between incident and reflected voltage waves at different ports of the up coupled line can be expressed as

$$\begin{bmatrix} V_1^- \\ V_5^- \\ V_6^- \\ V_4^- \end{bmatrix} = \begin{bmatrix} S_{11} & S_{15} & S_{16} & S_{14} \\ S_{51} & S_{55} & S_{56} & S_{54} \\ S_{61} & S_{65} & S_{66} & S_{64} \\ S_{41} & S_{45} & S_{46} & S_{44} \end{bmatrix} \begin{bmatrix} V_1^+ \\ V_5^+ \\ V_6^+ \\ V_4^+ \end{bmatrix}$$

(B.1)

At the center frequency, (B.1) then can be written as

$$\begin{bmatrix} V_1^- \\ V_5^- \\ V_6^- \\ V_4^- \end{bmatrix} = \begin{bmatrix} 0 & S_{51} & S_{61} & 0 \\ S_{51} & 0 & 0 & S_{51} \\ S_{61} & 0 & 0 & S_{51} \\ 0 & S_{61} & S_{51} & 0 \end{bmatrix} \begin{bmatrix} V_1^+ \\ V_5^+ \\ V_6^+ \\ V_4^+ \end{bmatrix}$$

(B.2)

Similarly, the relationship between incident and reflected voltage waves at different ports of the down coupled line (@ center frequency) can be expressed as
\[
\begin{bmatrix}
V_2^- \\
V_7^- \\
V_8^- \\
V_3^-
\end{bmatrix} =
\begin{bmatrix}
0 & S_{72} & S_{82} & 0 \\
S_{72} & 0 & 0 & S_{82} \\
S_{82} & 0 & 0 & S_{72} \\
0 & S_{82} & S_{72} & 0
\end{bmatrix}
\begin{bmatrix}
V_2^+ \\
V_7^+ \\
V_8^+ \\
V_3^+
\end{bmatrix}
\]

(B.3)

\[S_{51} = S_{72}, \quad S_{61} = S_{82}\]  \hspace{1cm} (B.4)

\[V_6^- = V_8^+, \quad V_5^- = V_7^+\]  \hspace{1cm} (B.5)

From Equations (B.2) (B.3) (B.4) (B.5),

\[V_2^- = (S_{51}^2 + S_{61}^2)V_1^+ + 2S_{51}S_{61}V_4^+\]  \hspace{1cm} (B.6)

\[V_3^- = (S_{51}^2 + S_{61}^2)V_4^+ + 2S_{51}S_{61}V_1^+\]  \hspace{1cm} (B.7)

Hence, \(S_{21}\) and \(S_{31}\) at the center frequency are shown as follows:

\[S_{21} = (S_{51}^2 + S_{61}^2) = |S_{51}|^2 - |S_{61}|^2\]  \hspace{1cm} (B.8)

\[S_{31} = 2S_{51}S_{61} = 2|S_{51}||S_{61}|\]  \hspace{1cm} (B.9)

If the two-section tandem coupler is equal to a 3-dB coupler, \(S_{21}\) and \(S_{31}\) at the center frequency are \(\sqrt{2}\) and \(\sqrt{2}\). \(S_{61}\) is then given as 0.383, which is -8.34 dB. Hence, it can be concluded that a 3-dB coupler can be realized by two tandem 8.34 dB couplers.
Investigation on Adaptive Matching Using Duty-cycle Control in Class-E Power Amplifiers

This part will not be shown in this version of report.
101

Bibliography


[29] Paul Salem, Chen Wu, and Mustapha C.E. Yagoub, “Non-uniform tapered ultra wideband directional coupler design and modern ultra wideband balun integration”, Proceedings
of Asia-Pacific Microwave Conference 2006.


[33] Andreas Wentzel and Dariusz Pienkowski, “Broadband Wilkinson divider”.


[58] CGH60060D Data Sheet, Cree Inc., 2010.