

Capacitive Sensor Interface Using an Inverter-Based Period Modulator

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Capacitive Sensor Interface Using an Inverter-Based Period Modulator

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Abstract

This thesis discusses the basic principles, circuit implementation and measurements of an inverter-based capacitive-sensor interface based on period modulation.

The interface employs an inverter-based OTA and comparator to increase the current efficiency. And it applies a discrete-time feedback loop to eliminate the need for a large integration capacitor and thus reduce the die size. A dual-integration-capacitor scheme is used in order to reduce the front-end noise. Moreover, a sample and hold circuit is introduced to the integration current source to reduce the noise contribution of the bias circuit.

A prototype interface has been implemented in a $0.16 \mu\text{m}$ CMOS process to prove these concepts. The measurement results show that it can achieve more than 10 bit resolution consuming $14 \mu\text{A}$ from a 1 V supply. The die size and energy efficiency have improved by more than an order-of-magnitude compared to previous interfaces based on period modulation.

Keywords: Capacitive sensor, Period modulation, Energy-efficiency, Low-power

Tables of Contents

List of Figures	viii
List of Tables	x
Acknowledgement	xi
1. Introduction	1
1.1. Capacitive Sensors.....	1
1.2. Different Readout Approaches for Capacitive Sensors.....	3
1.3. Capacitive Sensor Interfaces Based on Period-Modulation.....	5
1.3.1. Introduction to Capacitive Sensor Interfaces Based on Period-Modulation.....	5
1.3.2. Objectives.....	7
1.4. Thesis Organization.....	9
2. Architecture-Level Study	12
2.1. Inverter-based OTA.....	12
2.1.1. Requirements of an OTA in Switched-Capacitor Circuits....	12
2.1.2. OTA Topologies.....	14
2.1.3. Inverter-based OTA in Switched-Capacitor Circuits.....	18
2.1.4. Inverter-Based PM Implementation.....	19
2.2. Auto-Calibration Technique.....	20
2.3. Dual-Integration-Capacitor Scheme.....	23
2.4. Discrete-time Feedback Loop.....	25
2.5. Final Architecture.....	31
3. Transistor-Level Design	33
3.1. Overview of Readout Circuitry.....	33
3.2. Inverter-based Integrator.....	37

3.3.	Integration Current Sources.....	39
3.4.	Multi-level Comparator.....	42
3.5.	Discrete-time Feedback Loop.....	43
3.5.1.	Switched Current Sources.....	43
3.5.2.	Comparators with Hysteresis.....	45
3.6.	Clock Booster.....	46
3.7.	Digital Block.....	47
3.8.	Design for Testability.....	50
3.9.	Layout.....	52
4.	Measurement Results.....	56
4.1.	Fabricated Chip.....	56
4.2.	Measurement Setup.....	57
4.2.1.	Equipment.....	57
4.2.2.	Test PCB.....	58
4.3.	Measurement Results.....	59
4.3.1.	Resolution.....	59
4.3.2.	Linearity.....	62
4.3.3.	Pressure Measurement.....	64
4.3.4.	Performance Summary.....	65
5.	Conclusions.....	69
5.1.	Thesis Contributions.....	69
5.2.	Future Work.....	71

List of Figures

Fig 1-1: Simple capacitive sensor model.....	2
Fig 1-2: Electrical model of practical capacitive sensor.....	3
Fig 1-3: Survey of energy consumption per measurement for various types of interfaces.....	4
Fig 1-4: Operation principle and timing diagram of capacitive sensor interfaces based on PM.....	6
Fig 2-1: (a) Circuit model of PM-based capacitive sensor interface (b) timing diagram and waveform of V_{int}	13
Fig 2-2: model of SC circuit in the settling phase.....	14
Fig 2-3: Folded-cascode OTA.....	15
Fig 2-4: Telescopic OTA.....	16
Fig 2-5: Inverter-based OTA.....	17
Fig 2-6: Current starved cascaded inverter.....	17
Fig 2-7: Characteristics of an inverter: A_0 and GB versus supply voltage.....	18
Fig 2-8: Inverter-based SC circuit.....	19
Fig 2-9: Inverter-based capacitive sensor interface based on PM.....	20
Fig 2-10: Auto-calibration technique.....	21
Fig 2-11: Proposed auto-calibration technique.....	22
Fig 2-12: Noise sources in the capacitive sensor interface based on PM.....	23
Fig 2-13: The effect of voltage noise at the comparator input on the jitter.....	24
Fig 2-14: Circuit and timing diagram of the use of two integration capacitor.....	25
Fig 2-15: Block diagram of the capacitive sensor interface based on period modulation with continuous-time negative feedback.....	27
Fig 2-16: simplified circuit diagram of the interface during phase ϕ_2	28
Fig 2-17: Circuit and timing diagrams of discrete-time feedback loop.....	29
Fig 2-18: Discrete-time feedback loop with hard-switches (a) circuit diagram (b) timing diagram.....	30

Fig 2-19: Final architecture of the inverter-based capacitive sensor interface based on period modulation.....	31
Fig 3-1: System-level diagram of the inverter-based capacitive sensor interface based on PM. (a) on-chip components (b) off-chip components.....	34
Fig 3-2: Simplified model of SC in the proposed interface.....	35
Fig 3-3: Schematic of the inverter-based integrator.....	38
Fig 3-4: Current source with resistive-degeneration.....	40
Fig 3-5: Implementation of sinking and sourcing integration current.....	40
Fig 3-6: Implementation of sinking and sourcing integration current with S&H circuit.....	41
Fig 3-7: Implementation of the multi-level comparator.....	42
Fig 3-8: Circuit model of discrete-time feedback loop.....	44
Fig 3-9: Implementation of switched current sources.....	45
Fig 3-10: Implementation of Schmitt-trigger logic gates (a) used in phase φ_1 (b) used in φ_2	46
Fig 3-11: Implementation of the clock booster.....	47
Fig 3-12: (a) Timing diagram (b) Implementation of dead-time generator.....	48
Fig 3-13: (a) Implementation of multi-level controller (b) Timing diagram.....	49
Fig 3-14: (a) Implementation of non-overlapping clock generator (b) Timing diagram.....	50
Fig 3-15: (a) Implementation of 6-bit shift register (b) Timing diagram.....	51
Fig 3-16: Implementation of PMOS source-follower.....	52
Fig 3-17: Layout of the capacitive sensor interface.....	53

List of Tables

Table 1-1: Design target of the PM-based capacitive sensor interface.....	8
Table 3-1: Simulated parameters of the inverter-based OTA.....	38
Table 3-2: Simulated parameters of integration current sources.....	42
Table 3-3: Simulated parameters of the multi-level comparator.....	43
Table 3-4: Simulated parameters of IDACs.....	45
Table 3-5: Simulated threshold levels of Schmitt-trigger logic gates.....	46
Table 3-6: Output of the 6-bit shift register.....	51
Table 3-7: I/O pin details.....	54
Table 4-1: Normal measurement conditions.....	59
Table 4-2: Characteristics of the MEMS pressure sensor.....	64
Table 4-3: Summary of the performance of the interface and comparison between different types of CDCs.....	67

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Chapter 1

Introduction

This chapter introduces capacitive sensors for energy-constrained applications and presents existing readout approaches for capacitive sensors. It discusses the advantages and disadvantages of these approaches, and, in more detail, the operating principles and features of interfaces based on period modulation (PM), which are compact and flexible, but lag behind in energy efficiency. Then, the objective of this thesis is introduced, which is to apply circuit techniques to improve the energy efficiency of PM-based interfaces. At the end of this chapter, the organization of this thesis is given.

1.1. Capacitive Sensors

Capacitive sensors nowadays are widely used, for instance, in consumer, medical, automotive, and industrial areas, because they don't consume static current, making them suitable in low-power and energy-constrained applications [1]. Comprising two electrical conductors separated by a dielectric, a simple capacitive sensor such as pressure sensor, humidity sensors, tactile sensors, biological sensors and so on can be implemented. With an overlapping area A , distance d and a dielectric permittivity ϵ , the capacitance between two plates in Fig 1-1 can be calculated:

$$C = \epsilon \frac{A}{d}. \quad (1-1)$$

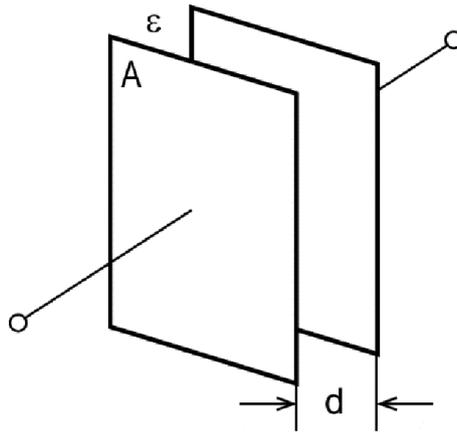


Fig 1-1: Simple capacitive sensor model

By changing one of these three elements while keeping the other two fixed, the capacitance changes correspondingly. For example, by changing the distance d and keeping the area A and dielectric permittivity ϵ fixed, displacement [4] and pressure sensors [10] can be implemented. By changing the area A and keeping the distance d and dielectric permittivity ϵ fixed, angular sensors [9] can be implemented. By changing dielectric permittivity ϵ and keeping the distance d and the area A fixed, humidity [3] and DNA sensors [11] can be implemented.

A challenge associated with capacitive sensors is the presence of parasitic elements. Finite parasitic resistance and capacitance inevitably exists. Fig 1-2 shows the practical electrical model of a capacitive sensor including these parasitics. Besides the sensor capacitor itself, a shunt resistor R_p , a shunt capacitor C_{p0} and two parasitic capacitors C_{p1} and C_{p2} at two terminals of the sensor capacitor are included. The parasitic capacitors play an important role for the energy efficiency of a capacitive sensor system since they get charged and discharged during the measurement.

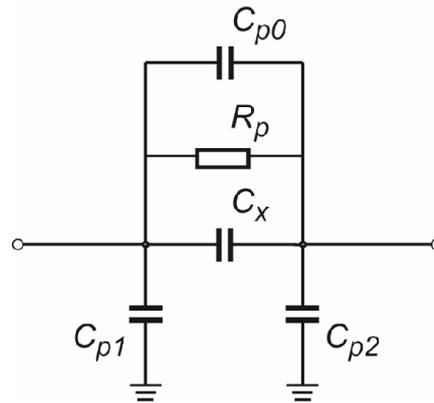


Fig 1-2: Electrical model of practical capacitive sensor

1.2. Different Readout Approaches for Capacitive Sensors

Since capacitive sensors don't consume static current, the energy consumption of a capacitive sensor system will be dominated by the readout circuit. Therefore, in recent years, different kinds of energy-efficient capacitance-to-digital converters (CDCs) have been presented, such as interfaces based on successive approximation (SAR), delta-sigma modulation (DSM), pulse-width modulation (PWM) and period modulation (PM).

For various types of CDCs, a survey of energy consumption per measurement versus ENOB has been reported in [1]. Since then, several new CDCs with lower figure of merit (FoM) have been published [14,15]. Fig 1-3 shows the energy consumption per measurement for these interfaces.

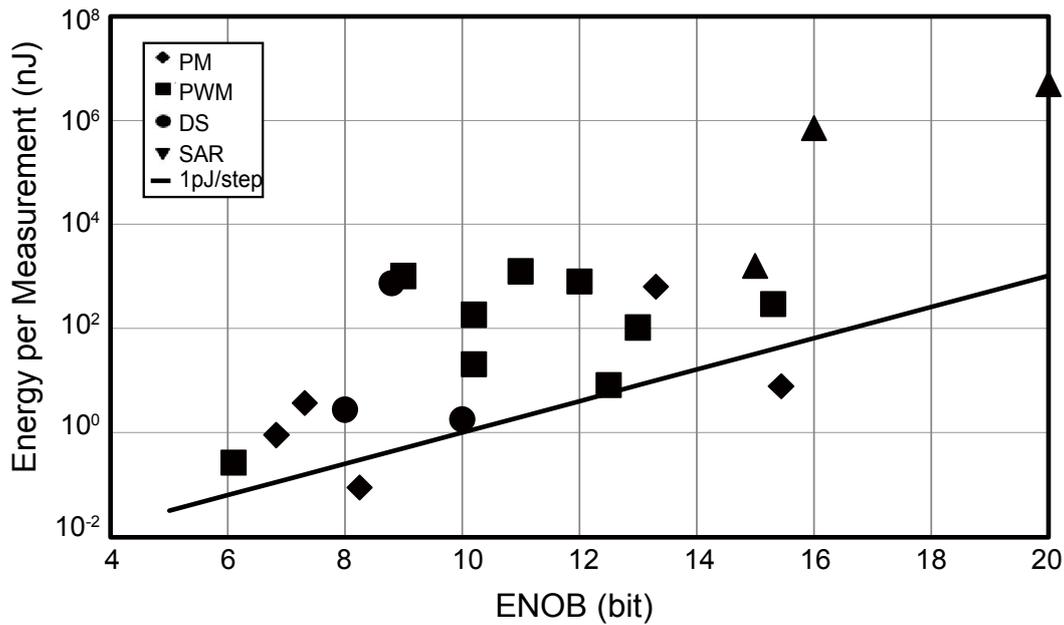


Fig 1-3: Survey of energy consumption per measurement for various types of interfaces according to [1]

Interfaces based on SAR employ a capacitor array, switches and a comparator. By applying charge redistribution, the sensor capacitor is compared with the capacitor array, step by step, whose value is approximating the value of sensor capacitance. Employing only one active element, this kind of CDC works with low power consumption. In [2], the sensor capacitor is connected to a capacitor DAC (CDAC) directly limiting the voltage swing of the comparator input. Therefore, most SAR CDCs have low ENOB.

Interfaces based on DSM [3,4] use charge balancing, by oversampling the sensor capacitor C_x and a reference capacitor C_{ref} , to generate a bit-stream whose bit-density is proportional to the ratio of C_x and C_{ref} . In order to extract this bit-density from the bit-stream, a decimation filter is needed. DSM CDCs can achieve high resolution with low power consumption by increasing the oversampling ratio (OSR). But higher-order modulators are typically needed in an energy-optimized implementation in order to balance quantization noise and thermal noise. Moreover, an oversampled clock is needed in the system. Both

increase the complexity of the system.

Interfaces based on PWM transduce the sensor capacitance into a current I_x which is proportional to C_x and then transform the modulated current into a pulse-width-modulated output, which is the ratio between I_x and a reference current I_{ref} [5]. Most interfaces based on PWM have a low effective number of bits (ENOB), because their input range is small even though the absolute resolution is comparable with those of other types of the interfaces

Interfaces based on PM use also charge balancing: to obtain a periodic output signal whose period is proportional to the sensor capacitance, they transfer charge from the sensor capacitor to an integration capacitor and balance this by charge transferred by an integration current source. PM-based interfaces don't require a clock because they operate asynchronously. Moreover, they can be designed to handle large input capacitance range with high resolution. Prior PM-based interfaces achieve high resolution, from 15 bits to 20 bits [6-8]. But compared with other types of capacitive interfaces, they are less energy-efficient.

1.3. Capacitive Sensor Interfaces Based on Period-Modulation

1.3.1. Introduction to Capacitive Sensor Interfaces Based on Period-Modulation

PM-based capacitive sensor interfaces are based on a relaxation oscillator whose output period is proportional to the sensor capacitance C_x . Figure 1-4 illustrates how the PM-based CDC reported in this thesis transforms the capacitance into a time period. The operating principle of earlier CDCs reported in [6-8] is similar. An initial state, in which the charge stored in the integration

capacitor C_{int} is cleared and the voltage on the drive side V_{drive} of the sensor capacitor C_x is connected to ground V_{ss} , is needed. After that, phase ϕ_1 starts and V_{drive} is connected to power supply V_{DD} . The output of the integrator V_{int} steps down, due to the amount of charge, $V_{DD} \cdot C_x$, transferred to C_{int} , and then rises smoothly since a sinking current $I_{int,n}$ discharges C_{int} . A comparator is needed to detect the moment when V_{int} returns to its initial value and to trigger the next phase ϕ_2 . During phase ϕ_2 , V_{drive} is pulled to V_{ss} and a sourcing current $I_{int,p}$ charges C_{int} similarly with an opposite polarity. Then a new phase ϕ_1 is triggered. This process will repeats N times and the time period of this process is:

$$T = \frac{2N \cdot V_{DD} \cdot C_x}{I_{int}} \tag{1-2}$$

By counting the number of clock cycles of a reference clock during this period, a digital representation of C_x is obtained.

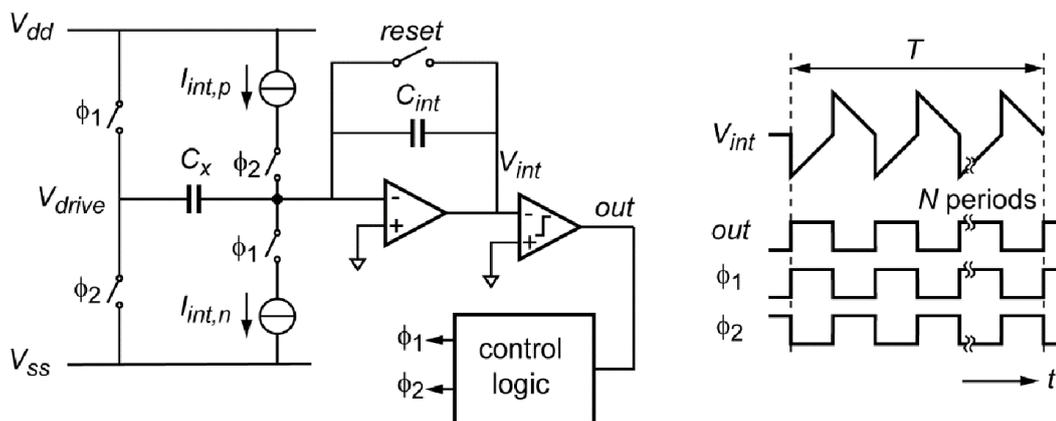


Fig 1-4: Operation principle and timing diagram of capacitive sensor interfaces based on PM

Compared with other types of capacitive sensor interfaces, PM-based capacitive sensor interfaces [6,7] have achieved relatively high resolution but

have high power consumption and long measurement time [1]. Therefore, these PM-based capacitive sensor interfaces have relatively low FoM even though they have high ENOB (see Fig. 1-3). The PM-based capacitive sensor interface in [8] consumes almost two orders of magnitude less energy than in [7,8] with the use of simple energy-efficient analog building blocks. However, a large gap between [8] and other capacitive sensor interfaces as such [2-5] in energy-efficiency still exists.

1.3.2. Objectives

Recently, inverter-based operational trans-conductance amplifiers (OTAs) have been employed instead of conventional OTAs to increase the current-efficiency in a humidity sensor [3], an implantable pacemaker, a CMOS image sensor, an audio codec [12] and a temperature sensor [13].

The aim of this thesis work is to implement an inverter-based capacitive sensor interface based on PM, in order to bridge the gap between PM-based capacitive sensor interfaces and DSM-based ones. In addition, some attractive schemes of PM-based capacitive sensor interfaces are proposed to improve the performances of this type of interfaces.

Table 1-1 lists the performance of previous designs [3,8] and the targeted specifications of the PM-based capacitive sensor interface. Even though the target of this project is to design a capacitive sensor interface which can handle a wide range of input capacitances, a limited range from 0 pF to 8 pF is chosen to determine the specifications of building blocks more clearly. A 1 V supply is chosen to ensure that the PMOS and NMOS in a simple inverter stay at the boundary between weak inversion and strong inversion. In order to bridge the gap between the energy consumption of PM-based capacitive sensor

interfaces and that of DSM-based ones, a current consumption less than 30 μA and a measurement time less than 4.5 ms are targeted, while maintaining an ENOB of 15 bit. Moreover, this capacitive sensor interface is designed to handle the parasitics more flexibly. The parasitic capacitor, which sits at the terminal of sensor capacitor connected to the drive side, is scalable while the other one is 15 pF.

Table 1-1: Design target of the PM-based capacitive sensor interface

Specification	[3]	[8]	Target
Type	DSM	PM	PM
Technology	0.16 μm CMOS	0.35 μm CMOS	0.16 μm CMOS
C_x Range (pF)	0.5 – 1	6.8	0 - 8
Parasitic Capacitor (pF)	-	$5 \cdot C_x$	C_{p1} : Scalable C_{p2} : 15
Supply Voltage (V)	1.2	3.3	1
Current Consumption (μA)	8.6	64	<30
Measurement Time (ms)	0.8	7.6 @ 6.8 pF	<4.5 @ 8 pF
Resolution (aF)	70	208	<229
ENOB (bit)	12.5	15	>15
FoM (pJ/step)	1.4	49 @ 6.8 pF	<3.5 @ 6.8 pF <1.4 @ 1 pF

1.4. Thesis Organization

This thesis presents the basic principles and circuit implementation of an inverter-based capacitive-sensor interface based on period modulation. Apart from this introductory chapter, the rest of this thesis is divided into five chapters.

Chapter 2 discusses the architecture of the interface. An auto-calibration technique is employed to maintain the accuracy of the system while using power-efficient analog building blocks. This chapter also introduces a new chopping scheme and discrete-time feedback loop.

Chapter 3 describes the transistor-level implementation of the sub-blocks of the interface one by one. The layout details are also given.

Chapter 4 briefly introduces the measurement methods and setup and presents in detail the measurement results.

Finally, Chapter 5 summarizes the contributions of this thesis and furthermore some potential works in future are highlighted.

References

- [1] M. A. P. Pertijs and Z. Tan, "Energy-Efficient Capacitive Sensor Interfaces," in *Analog Circuit Design*, A. Baschiroto, A. H. M. van Roermund and M. Steyaert, Eds. New York: Springer, pp. 129-147, 2012.
- [2] Tanaka K. et al., "A 0.026mm² Capacitance-to-Digital Converter for Biotelemetry Applications Using a Charge Redistribution Technique," *IEEE ASSCC'07*, pp. 244-247.
- [3] Z. Tan, Y. Chae, R. Daamen, A. Humbert, Yuri, V. Ponomarev, and M.A.P. Pertijs, "A 1.2V 8.3nJ Energy-Efficient CMOS Humidity Sensor for RFID Applications," *VLSI Circuits Dig. Tech. Papers*, pp. 24-25, 2012.
- [4] X. Sha, et al., "A Capacitance-to-Digital Converter for Displacement Sensing with 17b Resolution and 20 μ s Conversion Time," *ISSCC*, pp. 198-199, Feb. 2012
- [5] Meng-Lieh Sheu, et al., "A Capacitance-Ratio-Modulated Current Front-End Circuit with Pulsewidth Modulation Output for a Capacitive Sensor Interface." *IEEE Instrumentation and Measurement Society*, vol.61, no. 2, pp.447-455, 2011.
- [6] A. Heidary, S. Heidary Shalmany and G. Meijer "A Flexible Low-Power High-Resolution Integrated Interface for Capacitive Sensors", *Proc. IEEE Int. Symp. Industrial Electronics (ISIE)*, pp.3347 -3350, 2010
- [7] A. Heidary and G. C. M. Meijer "Features and Design Constraints for an Optimized SC Front-End Circuit for Capacitive Sensors with a Wide Dynamic Range", *IEEE J. Solid-State Circuits*, vol. 43, no. 7, pp.1609 -1616, 2008
- [8] Z. Tan, et al., "An Energy-Efficient 15-Bit Capacitive-Sensor Interface Based on Period Modulation," *JSSC*, vol. 47, no. 7, pp. 1703-1711, July 2012.
- [9] Li X, de Jong G W and Meijer G C M, "The Application of the Capacitor's Physics to Optimize Capacitive Angular-Position Sensors", *IEEE Trans. Instrum. Meas.*, Feb. 1997, Vol. 46, No. 1, pp. 8-14.
- [10] B. A. G. M. Shahiri-Tabarestani and R.Sabbaghi-Nadooshan, "Design and Simulation of High Sensitive Capacitive Pressure Sensor with Slotted Diaphragm", In *International Conference on Biomedical Engineering*, Penang, pages 484-489, 2012.

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- [11] C. Guiducci, et al., "Microelectrodes on a Silicon Chip for Label-Free Capacitive DNA Sensing," IEEE Sens. J., vol. 6, pp. 1084-1093, 2006.
- [12] Y. Chae and G. Han. "Low Voltage, Low Power, Inverter-Based Switched-Capacitor Delta-Sigma Modulator", J. Solid-State Circuits, vol. 44, no.2, pp. 485-472, 2009.
- [13] K. Souri, et al., "A CMOS Temperature Sensor With a Voltage-Calibrated Inaccuracy of 0.15°C (3) From-55°C to 125°C," J. Solid-State Circuits, vol. 48, is. 1, pp. 292-301, Jan. 2013.
- [14] S. Oh, et al., "15.4b Incremental Sigma-Delta Capacitance-to-Digital Converter with Zoom-in 9b Asynchronous SAR," VLSI Circ. Symp., June 2014.
- [15] H. Ha, et al., "A 160nW 69.3fJ/conversion-step Capacitance-to-Digital Converter for Ultra-Low-Power Wireless Sensor Nodes," ISSCC, pp. 220-221, Feb. 2014

Chapter 2

Architecture-Level Study

This chapter discusses techniques that can improve the performance of PM-based capacitive-sensor interfaces without increasing their energy consumption. It starts with an introduction to inverter-based OTAs, which improve current-efficiency compared to conventional OTAs. Then it describes an auto-calibration technique and a new dual-integration-capacitor scheme to improve the performance of the interface. To handle large input capacitance and parasitic capacitance, a discrete-time feedback loop is applied.

2.1. Inverter-based OTA

2.1.1. Requirements of an OTA in Switched-Capacitor Circuits

Fig 2-1 (a) shows the operation of the interface in the different phases φ_1 and φ_2 . Without the integration current sources $I_{int,p}$ and $I_{int,n}$, it can be regarded as a switched-capacitor (SC) circuit transferring the charge stored in C_x to C_{int} . This charge is balanced by the integration currents. In Fig 2-1 (b), a two-phase non-overlapping clock φ_1 and φ_2 is shown in order to ensure the correct timing for charge transfer. The solid line shows the waveform of V_{int} and the dashed line implies the waveform of V_{int} if the integration current sources are inactive. V_{int} cannot reach the ideal voltage corresponding to complete charge transfer, due to the limited DC loop gain (A_0) and bandwidth (BW) which cause static and dynamic errors in the SC circuit.

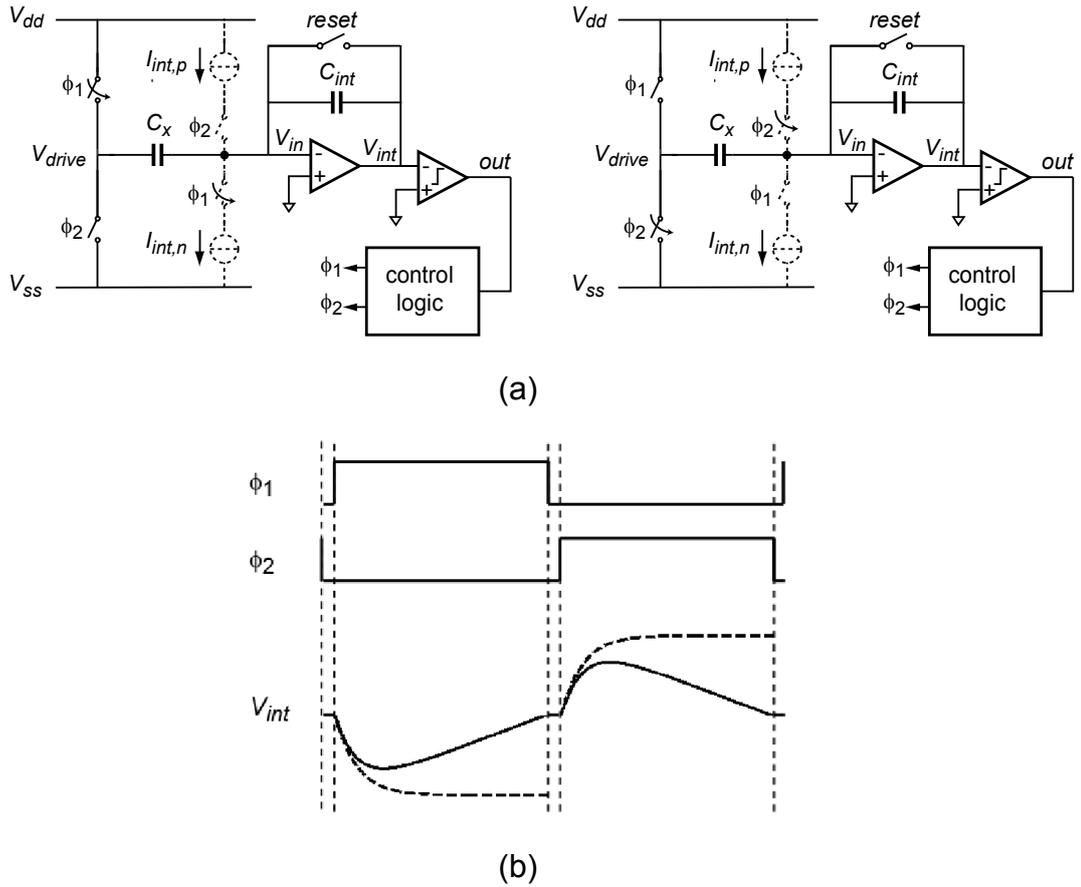


Fig 2-1: (a) Circuit model of PM-based capacitive sensor interface (b) timing diagram and waveform of V_{int}

If the time for charge transfer is infinitely long, the difference between the actual voltage of V_{int} and the ideal one is a static error associated with the finite DC loop gain. If the time is finite, the difference is a dynamic error, i.e. an error that depends on the time available for charge transfer.

To analyze these errors, a model of a SC circuit is shown in Fig 2-2. The reasons for the static error are due to the finite DC gain A_0 of the OTA:

$$V_{int} = -V_{in} \cdot \frac{C_x/C_{int}}{1+1/(A_0 \cdot F)}, \tag{2-1}$$

where F is feedback factor, $\frac{C_{int}}{C_{int}+C_x+C_i}$ and C_i is the combination of parasitic

capacitance of C_x and input capacitance of the inverter.

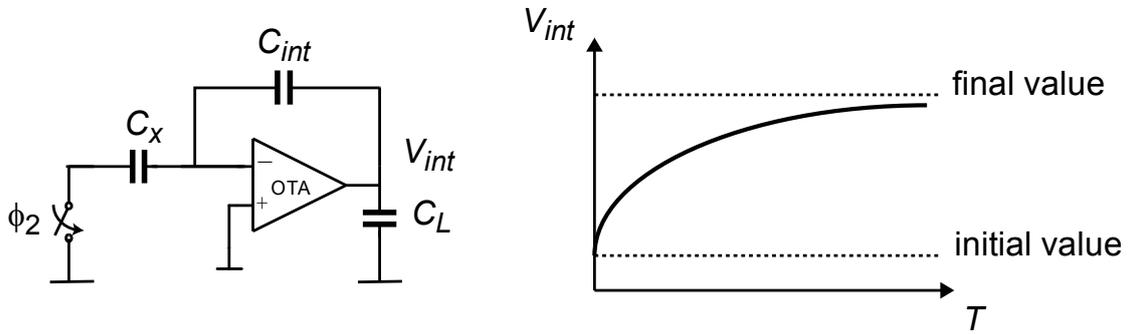


Fig 2-2: model of SC circuit in the settling phase

If the circuit is a one-pole system, V_{int} as a function of time can be expressed as:

$$V_{int}(t) = -V_{in} \cdot \frac{C_x/C_{int}}{1+1/(A_0 \cdot F)} \cdot (1 - e^{t/\tau}), \quad (2-2)$$

where the time constant τ is $\frac{C_L + (1-F)C_{int}}{Fg_m}$.

The requirements of the OTA used in the interface will be discussed in Session. 3.2 based on the targeted specifications of the interface.

2.1.2. OTA Topologies

Two OTA topologies are commonly used in SC circuit [9,10]. The first topology is the folded-cascode OTA, which is shown in Fig 2-3. It provides high A_0 , which is around $0.5 * (g_m r_o)^2$ (g_m is the transconductance of the input transistor and r_o is the output impedance of a single transistor), and reasonable output swing, which is around $V_{DD} - 4V_{dsat}$ (V_{dsat} is the drain-source voltage of a transistor in saturation). Assuming that the input transistors and the cascode transistors are biased at the same current I_d , the total current consumption is $4I_d$.

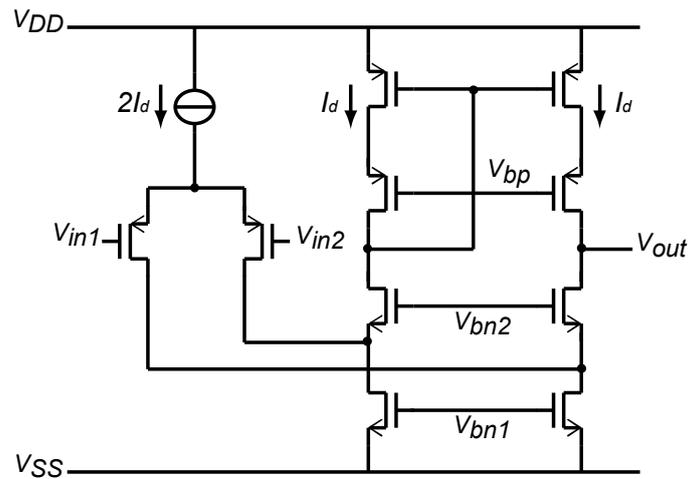


Fig 2-3: Folded-cascode OTA

In order to compare the current-efficiency easily, the current-efficiency factor γ of OTA is defined [8], which is:

$$\gamma = \frac{g_{m0}}{I_{tot}}, \quad (2-4)$$

where g_{m0} is the transconductance of OTA and I_{tot} is the total current consumption of the OTA.

Therefore, the current-efficiency factor of folded-cascode OTA γ_{folded} is:

$$\gamma_{folded} = \frac{g_{m0}}{4I_d}. \quad (2-5)$$

The second topology is the telescopic OTA. As is shown in Fig 2-4, a telescopic OTA consumes less current than a folded-cascode OTA since it has two branches instead of four. But it suffers from smaller output swing, $V_{dd} - 5V_{dsat}$, because of the tail current source.

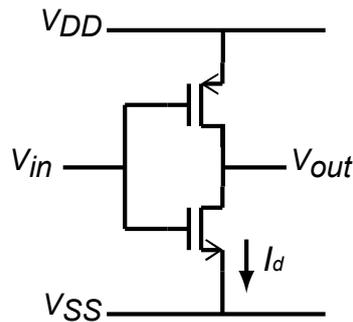


Fig 2-5: Inverter-based OTA

An additional advantage of inverter-based OTAs is their capability of operating at lower supply voltages, as required in scaled CMOS technologies. It is more difficult to employ telescopic or folded-cascode OTA at low supply voltages. It is not hard to imagine that the stack of four or five drain-source voltage (V_{DS}) of NMOS and PMOS, which is around 200 mV, increases the difficulty of the implementation of conventional OTAs in low supply voltage, such as 1.2 V and even 1 V. Inverter-based circuits have been employed these years [1-3]. Current starved cascaded inverter in Fig 2-6 [2] works in 1.2 V supply with 220 mV output swing. A simple inverter in Fig 2-5, which has a PMOS and a NMOS stack in one branch, can even work in 0.7 V.

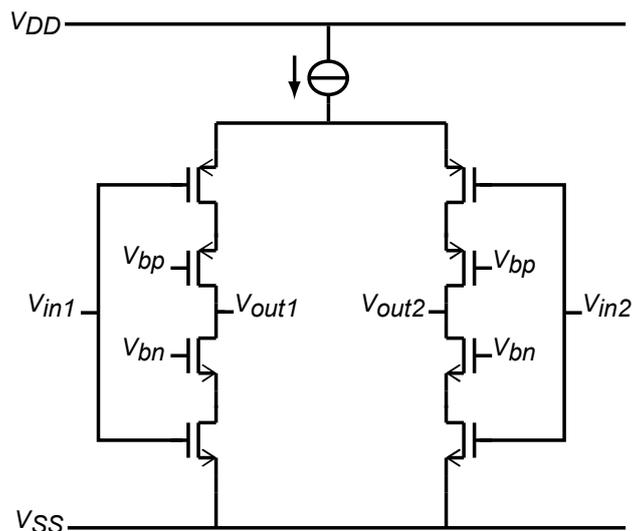


Fig 2-6: Current starved cascaded inverter [2]

Fig 2-7 [1] shows that an inverter has high A_0 in weak inversion while achieve wide gain-bandwidth product (GB) in strong inversion. Therefore, the inverter-based OTA should be biased at the boundary between weak and strong inversion regions, which is approximately the sum of the threshold voltage of NMOS $V_{th,n}$ and that of PMOS $V_{th,p}$. For example, the sum of $V_{th,n}$ and $V_{th,p}$ is around $0.9\text{ V} - 1\text{ V}$ in a $0.18\text{ }\mu\text{m}$ standard CMOS process.

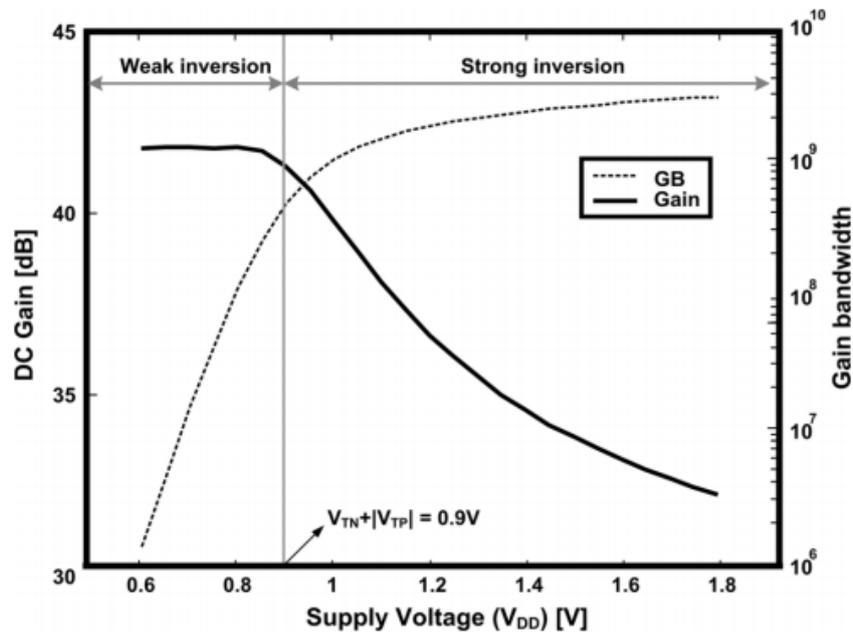


Fig 2-7: Characteristics of an inverter: A_0 and GB versus supply voltage [1]

2.1.3. Inverter-based OTA in Switched-Capacitor Circuits

SC circuits which employ inverter-based OTA operate in two phases φ_1 and φ_2 . Since an inverter is an inherently single-ended device, it cannot define a virtual ground voltage arbitrarily. Hence, auto-zeroing technique is applied to form a virtual ground [1], which is shown in Fig 2-8. In phase φ_1 , the inverter is switched to a unity-gain mode and the voltage V_i is sampled in C_{AZ} , which can be regarded as virtual ground of the OTA. At the same time, C_x is charged. In phase φ_2 , the charge is transferred from C_x to C_{int} and the output of the integrator V_{int} ideally equates:

$$V_{int} = V_{in} \cdot \frac{C_x}{C_{int}}. \quad (2-8)$$

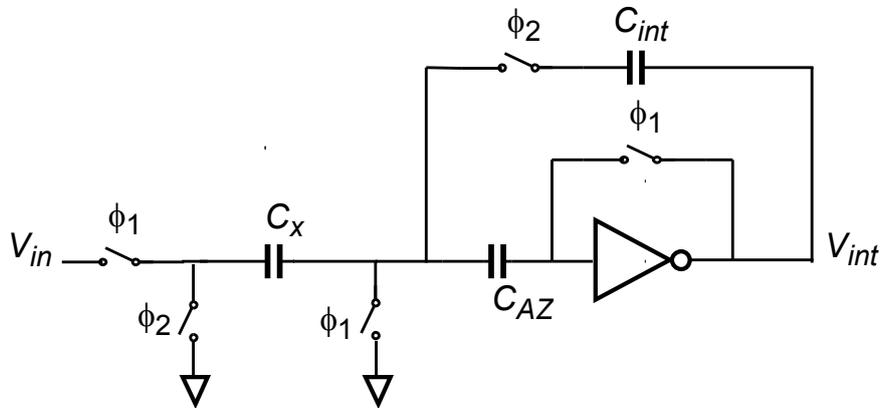


Fig 2-8: Inverter-based SC circuit

2.1.4. Inverter-Based PM Implementation

Fig 2-9 shows the operation of an inverter-based capacitive sensor interface based on PM. In Fig 2-9, no auto-zeroing is needed, because the input of the inverter can be readily biased at the unity-gain operating point that is defined during the reset phase and kept by the negative feedback during subsequent operation of the modulator. It is similar to Fig 2-1 while inverters are employed to implement the OTA and the comparator in order to increase the current-efficiency. Moreover, in order to improve the noise performance of the interface, multiple periods N are measured, corresponding to T .

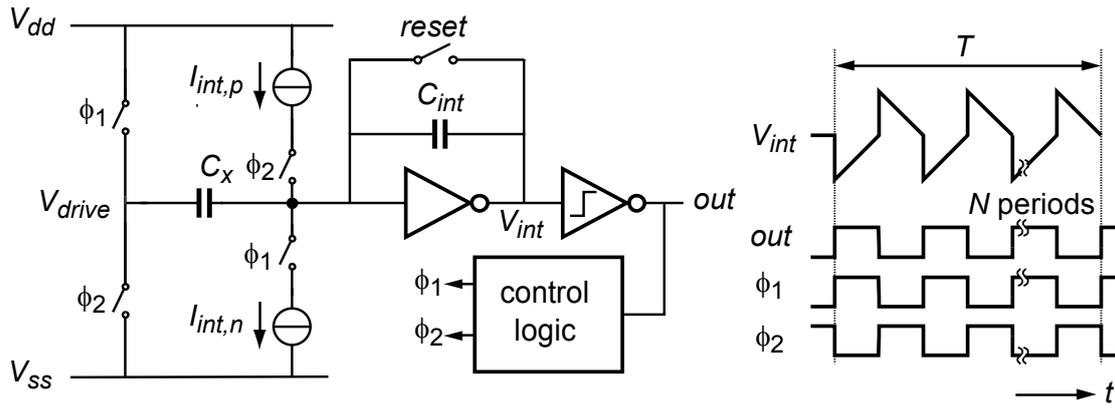


Fig 2-9: Inverter-based capacitive sensor interface based on PM

2.2. Auto-Calibration Technique

As discussed in Chapter 1 (Eq. 1-2), the output period T can be written as a linear function of the sensor capacitance C_x :

$$T = a \cdot C_x + b. \quad (2-9)$$

Unfortunately, in this expression, the gain coefficient $a \propto V_{dd}/I_{int}$ is poorly defined, and may drift, e.g. with time and temperature. Moreover, the offset coefficient b is not well-defined either, as it is affected by comparator delay t_{comp} and the charge injection of switches.

In order to eliminate the influence of coefficients a and b on T , auto-calibration is applied. As is shown in Fig 2-10, a multiplexer is added in this interface to have three subsequent measurement phases [4]. As in Fig 1-4, a reset phase is added to clear the charge stored in C_{int} and to initialize the control signal of the auto-calibration, so that ϕ_x and ϕ_{ref} are low. Then, an offset capacitor C_{off} , which is an on-chip capacitor, is measured. After an offset measurement phase, a reset phase occurs again, where ϕ_x is low and ϕ_{ref} is high. Then a combination of C_{off} and a reference capacitor C_{ref} is measured. Finally, a

combination of C_{off} and C_x is measured similarly.

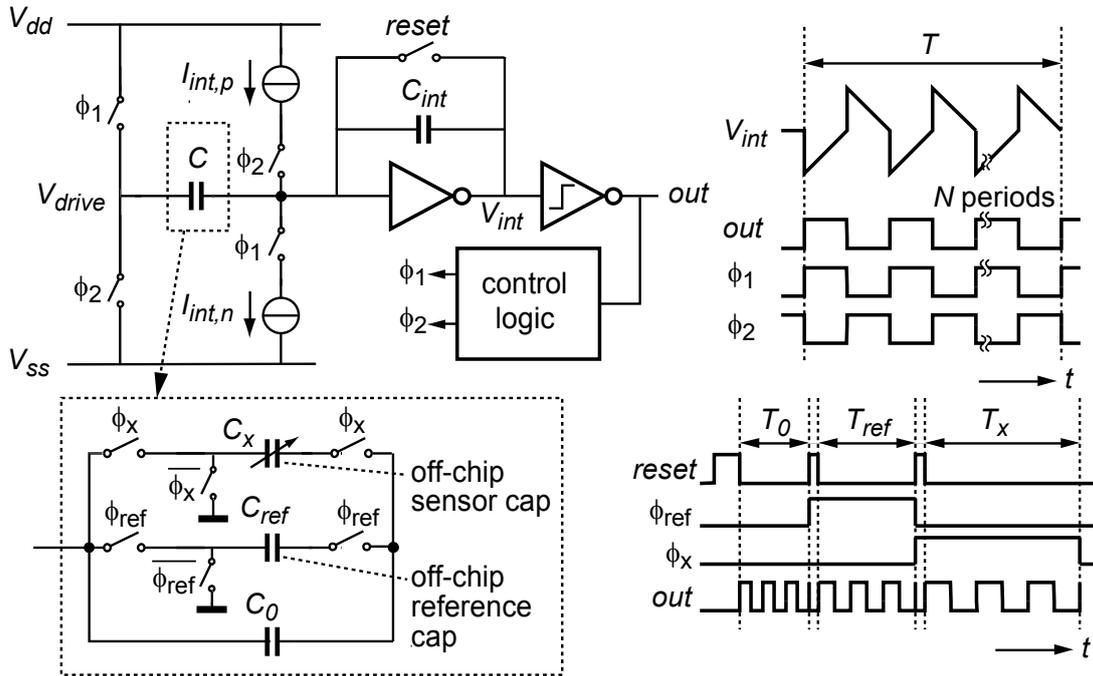


Fig 2-10: Auto-calibration technique

This leads to three time periods T_0 , T_{ref} and T_x , which are quantized by a counter:

$$T_0 = a \cdot C_{off} + b; \quad (2-10)$$

$$T_{ref} = a \cdot (C_{off} + C_{ref}) + b; \quad (2-11)$$

$$T_x = a \cdot (C_{off} + C_x) + b. \quad (2-12)$$

By digital post-processing, a final ratiometric output M can be calculated:

$$M = \frac{T_x - T_0}{T_{ref} - T_0}. \quad (2-13)$$

Therefore, the sensor capacitance can be extracted as:

$$C_x = M \cdot C_{ref}. \tag{2-14}$$

In Fig 2-10, the loading of the inverter-based OTA in the three measurement phases is different. For example, only C_{off} is connected to the inverter input during the offset measurement phase; C_{off} and C_{ref} are connected during the reference measurement phase; C_{off} and C_x are connected during the sensor measurement phase. Therefore, the feedback factor F in these measurement phases are different. In Eq. 2-2, different feedback factor F leads to different τ and, in consequence, a different dynamic error. Moreover, the static error is large because of the low A_o of the inverter-based OTA. Thus, the linearity of the interface is deteriorated.

In order to have the same feedback factor F in different measurement phases, C_{ref} and C_x can be connected to the inverter input even if they are not charged or discharged during the measurement phase, which is shown in Fig 2-11.

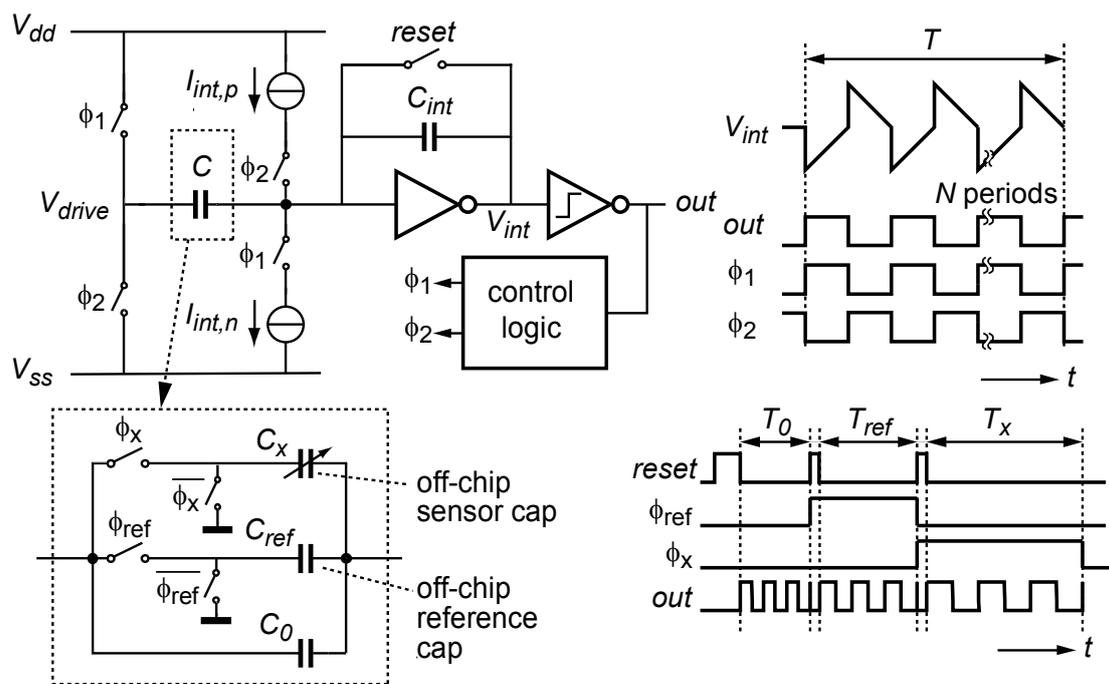


Fig 2-11: Auto-calibration technique

2.3. Dual-Integration-Capacitor Scheme

This capacitive sensor interface based on PM is an asynchronous SC circuit, whose clock period depends on the input capacitance. Therefore, it can be considered as a time-varying system. It is not hard to imagine that by introducing noise into the interface, the clock period of the interface is not fixed even if the same input capacitance value is measured. The time difference between the actual one and the ideal one is called jitter.

Fig 2-12 shows the noise sources in the interface. There are the input-referred voltage noise $V_{n,OTA}$ of the inverter-based OTA, the input-referred voltage noise $V_{n,comp}$ of the comparator, the thermal noise $V_{n,SW}$ of the switches, and the current noise of the integration current sources $I_{n,S}$. The noise of V_{dd} and V_{SS} are not considered here since they are decoupled by off-chip capacitors.

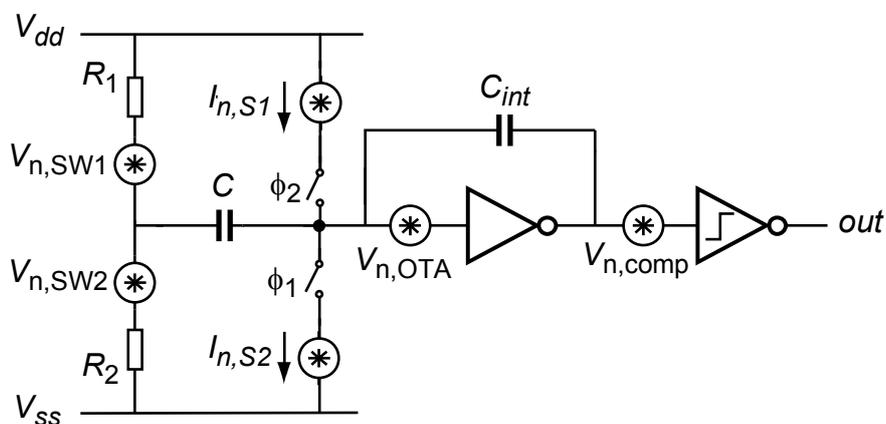


Fig 2-12: Noise sources in the capacitive sensor interface based on PM

As analyzed in [5], the noise sources $V_{n,SW}$ and $V_{n,OTA}$ have two mechanisms to contribute to the jitter. One of them is that the voltage noise is transferred to charge noise stored in C_{int} at the timing that zero crossing occurs. The other is that the voltage noise is transferred to voltage noise at the comparator input,

which has influence on the timing of the zero crossing in a similar way as $V_{n,comp}$. $I_{n,S}$ is transferred to voltage noise at the comparator input as other noise sources do. Moreover, the charge noise added to C_{int} by $I_{n,S}$ is equal to the charge added to the input node of the inverter-based OTA by $I_{n,S}$, because a negligible part of the charge noise is added to C [5].

The charge noise will be removed by I_{int} in the next phase contributing to the jitter and the voltage noise at the comparator input make the zero crossing occur earlier or later, contributing to the jitter as well. Calculation about how these noise sources are transferred to the jitter can be found in [5].

In Fig 2-13, the solid curves show the integrator output and the phases ϕ_1 and ϕ_2 as a function of time when the interface is noise free. The dashed curves show the waveforms with voltage noise at the comparator input, for the example case that the first rising edge of ϕ_2 occurs earlier because of the voltage noise causing the time period T to become shorter. This timing error is not repaired and thus causes jitter, as do similar errors on the other zero crossings.

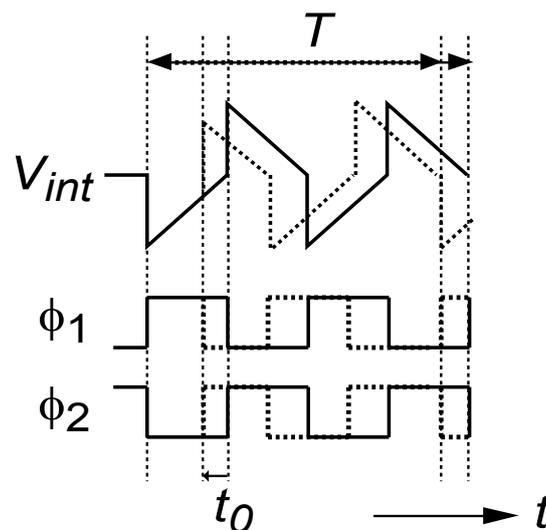


Fig 2-13: The effect of voltage noise at the comparator input on the jitter

Here, this problem is solved by employing two integration capacitors C_{int1} and C_{int2} for the two phases, as shown in Fig 2-14. The solid curves represent, as before, the noise-free waveforms, with the black one associated with C_{int2} and the gray one associated with C_{int1} , while the dashed curves represent the waveforms with noise. Considering a similar noise-induced timing error as before, the error charge associated with this error is now stored on C_{int1} . The time period of ϕ_2 , which follows the first ϕ_1 , is as long as the noise-free one, because no error charge is stored on C_{int2} . The next phase ϕ_1 becomes longer due to the error charge kept on C_{int1} and compensates for the timing error exactly. In this case, noise-induced timing errors on all transitions are thus cancelled, except for those on the last phases of T . Thus, the overall impact of the voltage noise transferred to the comparator input node is be strongly reduced. With this dual-integration-capacitor scheme, the current noise of the integration current sources becomes the dominant noise source, because this scheme cannot eliminate the noise of the integration current sources.

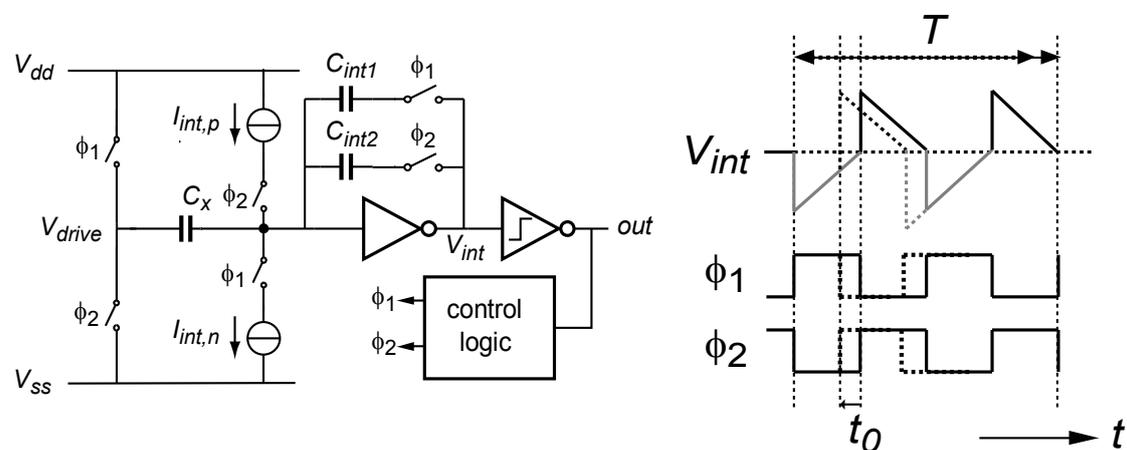


Fig 2-14: Circuit and timing diagram of the use of two integration capacitor

2.4. Discrete-time Feedback Loop

During the measurement, V_{drive} is pulled from V_{dd} to V_{ss} or from V_{ss} to V_{dd} causing the entire charge of C_x to be transferred to C_{int} at once. If the input

capacitance is large, the output of the integrator will saturate at V_{dd} or V_{SS} and thus the input of the integrator will be far away from the virtual ground voltage V_{th} . Therefore, I_{int} will vary and charge may be lost, making Eq 1-2 no longer valid. To reduce the output swing of the integrator for a given C_x , a larger C_{int} is needed. However, a larger C_{int} would slow down the OTA due to its larger parasitic capacitances, indicating a larger transconductance g_m of the OTA is required to maintain the accuracy of charge transfer. Furthermore, the die size of the chip becomes larger to handle a large sensor capacitance.

Another way to reduce the output swing of the integrator, is reducing the charge of C_x transferred to C_{int} , but simply reducing the charge transferred decreases the signal amplitude and thus the signal-to-noise ratio (SNR).

In [6,7], continuous-time negative feedback loops are introduced to reduce the output swing. The switches at V_{drive} are replaced by two feedback OTAs, which control the charge transfer speed. V_{drive} is pull to V_{dd} or V_{SS} by charging or discharging C_x by two feedback OTAs. In Fig 2-15, the current provided by the feedback OTA is initially larger than I_{int} , making V_{int} increase. When V_{int} reaches the control voltage V_b , the current provided by the feedback OTA equals to I_{int} , causing V_{int} to saturate at V_b . This situation remains until C_x is fully discharged. Then V_{int} ramps down due to I_{int} and reaches the threshold voltage V_{th} of the comparator.

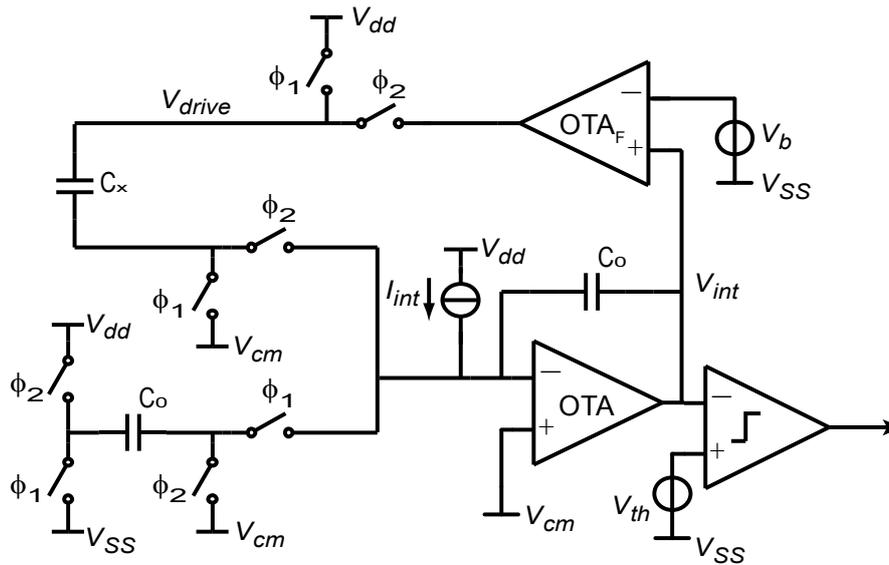


Fig 2-15: Block diagram of the capacitive sensor interface based on period modulation with continuous-time negative feedback

However, the negative feedback loops are conditionally stable. If the parasitic capacitors C_{p1} and C_{p2} in Fig 2-16 [7] are too large, the interface becomes unstable or stops oscillating. Fig 2-16 shows a simplified circuit diagram of the interface during phase φ_2 . C_{p2} absorbs part of the current provided by OTA_F at the beginning of phase φ_2 , $g_{mF} \cdot (V_b - V_{th})$ where g_{mF} is the transconductance of the OTA_F and V_b is the bias voltage of the OTA_F . The reset flows into C_x , whose fraction is $C_x / (C_x + C_{p2})$. It is possible that the part of current is smaller than I_{int} if C_{p2} is large leading to the insufficient capability of transferring the charge from C_x to C_{int} and therefore the interface stops oscillating. The loop has a pole at g_m / C_{p1} , indicating that the pole goes lower frequency with large C_{p1} and thus the instability probably occurs. To handle larger parasitics, higher g_m and g_{mF} are required with the cost of higher power consumption.

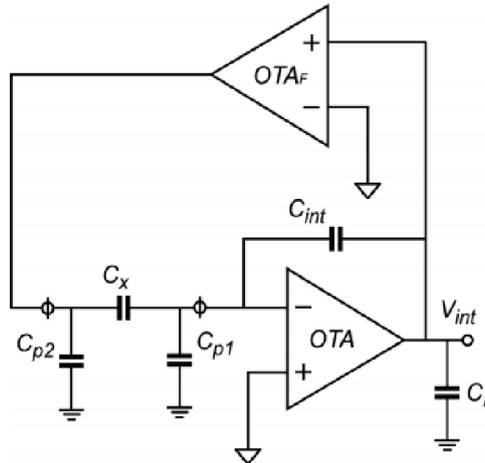


Fig 2-16: simplified circuit diagram of the interface during phase ϕ_2 [7]

In order to tackle large parasitics, a simpler solution, discrete-time feedback loop using switched current sources instead of feedback OTAs is proposed, as shown in Fig 2-17. The switched current sources $I_{drive,p}$ and $I_{drive,n}$ pull V_{drive} up and down between V_{dd} and V_{SS} , but can be temporarily switched off if V_{int} goes out of the range. This is detected by two comparators with hysteresis connected to V_{int} . As an example, the operation of this feedback loop in phase ϕ_2 is described. At the beginning of phase ϕ_2 , $I_{drive,n}$ is active to transfer the charge from C_x to C_{int2} making V_{int} ramp up. The signal $limit_H$ goes low when V_{int} reaches the upper threshold voltage of the hysteresis comparator $V_{th,H}$ and deactivates $I_{drive,n}$. Then V_{int} ramps down because of I_{int} until V_{int} reaches the lower threshold voltage $V_{th,L}$. This happens repeatedly, until the total charge stored in C_x initially is transferred to C_{int2} . The instability issue, due to C_{p1} , doesn't occur with discrete-time feedback loop and the switched current sources moreover is more flexible to handle C_{p2} than continuous-time feedback loops, because, given the parasitic capacitance of the sensor, the switched current sources can be easily designed to be sufficiently large.

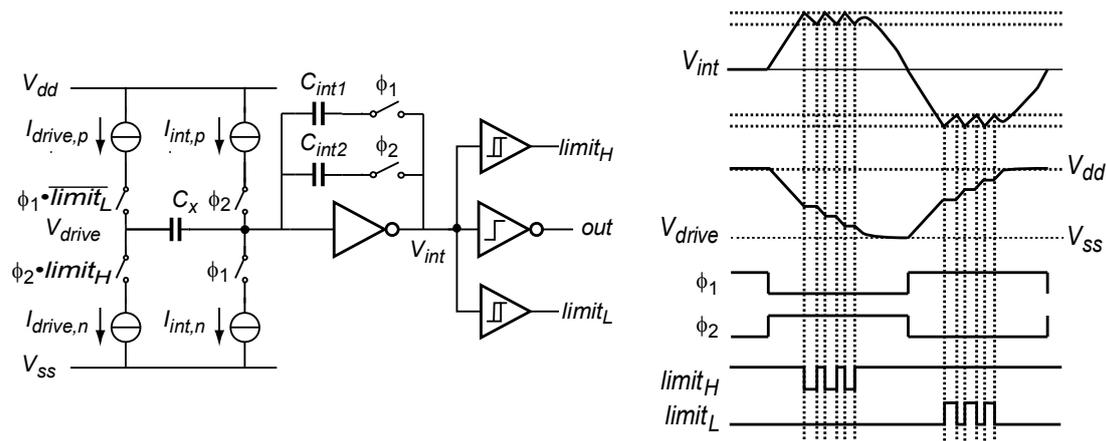
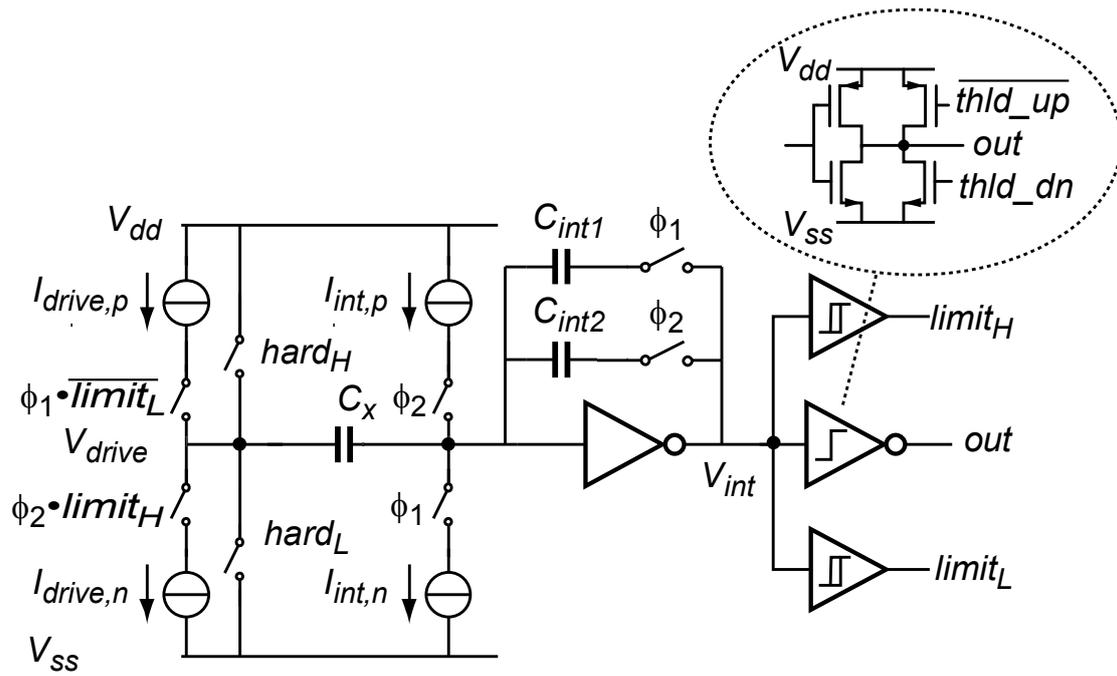
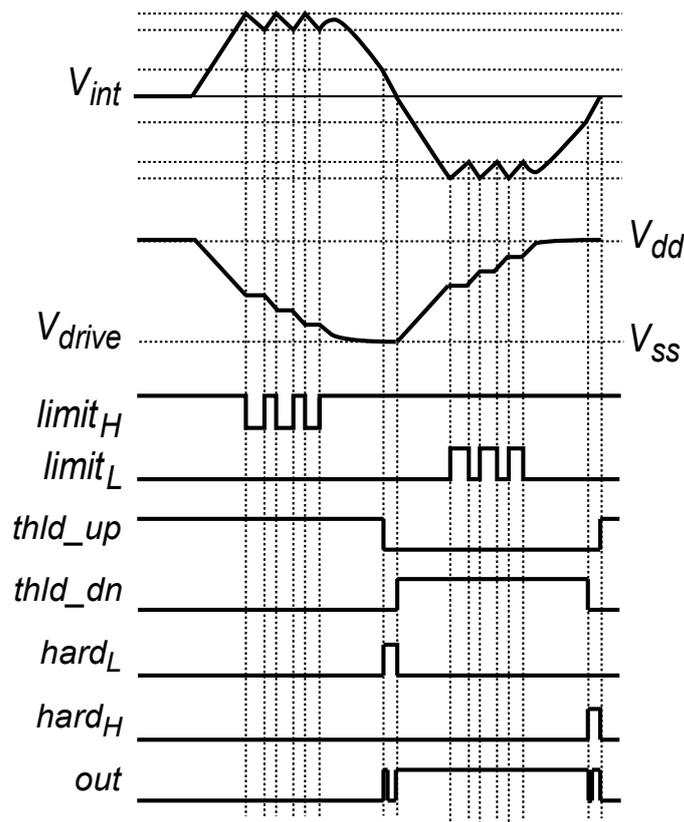


Fig 2-17: Circuit and timing diagrams of discrete-time feedback loop

However, V_{drive} cannot reach V_{dd} or V_{ss} at the end of the phase due to the limited output swing of the switched current sources. As a result, the accuracy of the charge transfer is degraded. To maintain accurate charge transfer, additional hard-switches are added in parallel to the switched current sources. At the end of the phase, the hard-switch turns on in order to ensure V_{drive} is pulled to V_{dd} or V_{ss} . Fig 2-18 shows how the hard-switches are employed. Before zeroing crossing occurs, V_{drive} is pulled to V_{dd} or V_{ss} by closing the switch ($hard_H$ or $hard_L$). The hard-switch is activated by the main comparator, whose threshold voltage is initially slightly shift up or down by activating an additional PMOS or NMOS using control signal $thld_dn$ and $thld_up$. After activating the hard-switch, the threshold voltage of the main comparator returns to its original value in order to detect the zero crossing.



(a)



(b)

Fig 2-18: Discrete-time feedback loop with hard-switches (a) circuit diagram
(b) timing diagram

2.5. Final Architecture

As discussed in this chapter, the interface based on PM employs an inverter-based OTA, an auto-calibration technique and a dual-integration-capacitor scheme to achieve an energy-efficient capacitive sensor interface. The final architecture is shown in Fig 2-19.

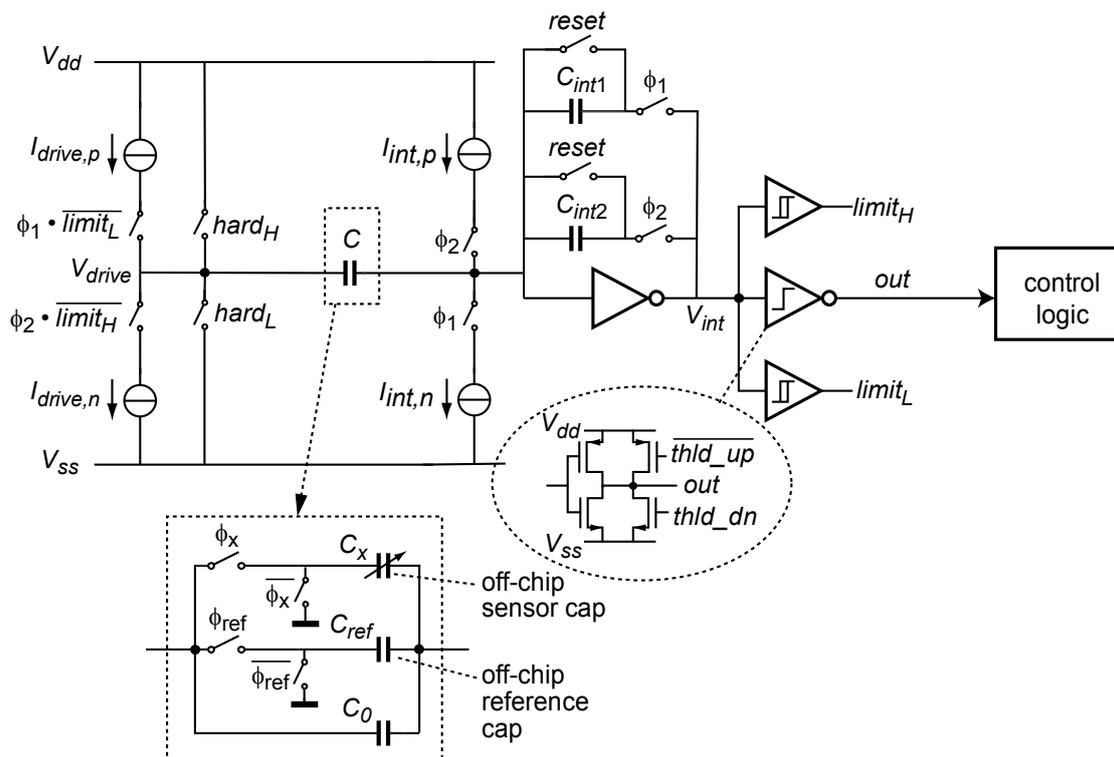


Fig 2-19: Final architecture of the inverter-based capacitive sensor interface based on period modulation

References

- [1] Y. Chae and G. Han. "Low Voltage, Low Power, Inverter-Based Switched-Capacitor Delta-Sigma Modulator", J. Solid-State Circuits, vol. 44, no.2, pp. 485-472, 2009.
- [2] Z. Tan, Y. Chae, R. Daamen, A. Humbert, Youri, V. Ponomarev, and M.A.P. Pertijs, "A 1.2V 8.3nJ Energy-Efficient CMOS Humidity Sensor for RFID Applications," VLSI Circuits Dig. Tech. Papers, pp. 24-25, 2012.
- [3] C. Chen, Z. Tan and M. Pertijs. "A 1V 14b Self-Timed Zero-Crossing-Based Incremental $\Delta\Sigma$ ADC", ISSCC, pp. 274-275, Feb. 2013
- [4] Frank ver der Geos, "Low-Cost Sensor Interfacing", Ph.D Thesis, Delft University of Technology, Delft, the Netherlands, 1996
- [5] S. Heidary Shalmany, et al., "Noise Analysis for Period-Modulation-Based Capacitive Sensor Interfaces", in process
- [6] A. Heidary and G. C. M. Meijer "Features and Design Constraints for an Optimized SC Front-End Circuit for Capacitive Sensors with a Wide Dynamic Range", IEEE J. Solid-State Circuits, vol. 43, no. 7, pp.1609 -1616, 2008
- [7] Z. Tan, et al., "An Energy-Efficient 15-Bit Capacitive-Sensor Interface Based on Period Modulation," JSSC, vol. 47, no. 7, pp. 1703-1711, July 2012.
- [8] Z. Tan, "Energy-Efficient Capacitive Sensor Interfaces", Ph.D Thesis, Delft University of Technology, Delft, the Netherlands, 2013
- [9] K. Bult and G. Geelen "A Fast-Settling CMOS Op Amp for SC Circuits with 90-dB DC Gain", IEEE Journal of Solid-State Circuits, vol. 25, no. 6, pp.1379 -1384, 1990
- [10] B. Razavi, Design of Analog CMOS Integrated Circuits. Boston: McGraw-Hill, 2001.

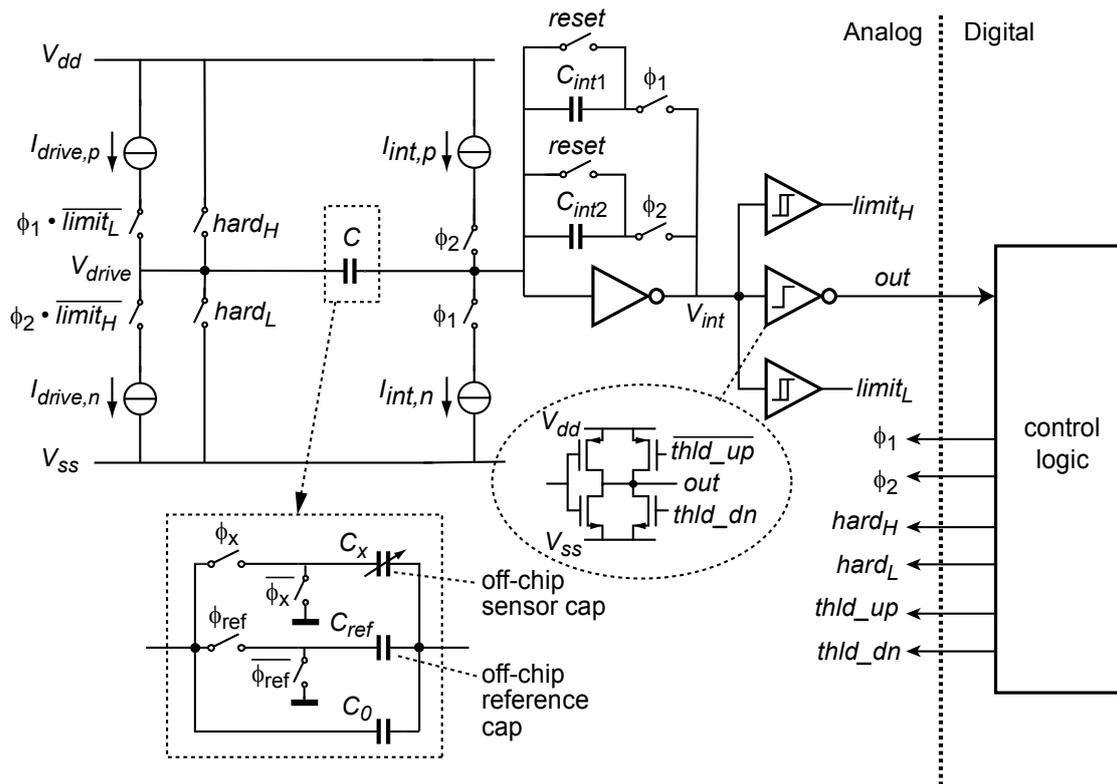
Chapter 3

Transistor-Level Design

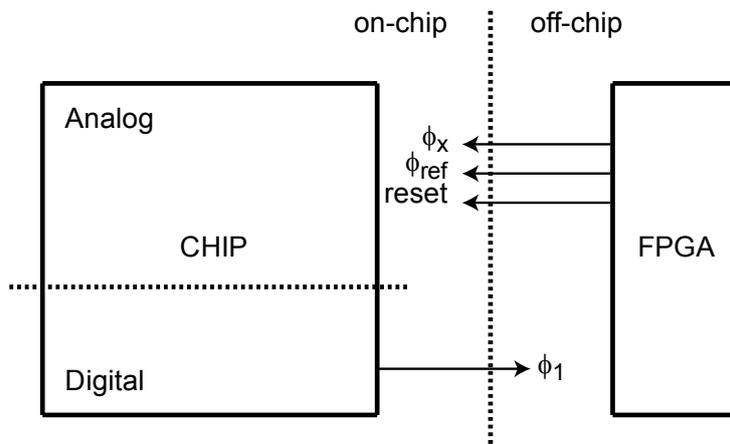
This chapter discusses the implementation details of the inverter-based capacitive sensor interface based on PM. It starts with an overview of the readout circuitry and then it derives the requirements of the sub-blocks based on the targeted specifications. After that, the implementation details of sub-blocks are discussed. At last, the layout is briefly discussed.

3.1. Overview of Readout Circuitry

The system-level diagram of the inverter-based capacitive sensor interface based on PM is shown in Fig 3-1 including an analog block, a digital block and some off-chip components. In Fig 3-1 (a), the analog block includes an inverter-based integrator, an inverter-based multi-level comparator, sinking and sourcing integration current sources for discharging and charging C_{int} , some switches, some capacitors as such C_{int} and C_{off} , and a discrete-time feedback loop, which contains two comparators with hysteresis and two switched current sources pulling V_{drive} to V_{dd} or V_{ss} . The digital block detects the output of the comparator and thus provides the analog block with control signals φ_1 , φ_2 , $hard_H$ and $hard_L$. In Fig 3-1 (b), C_{ref} and C_x are off-chip in order to maintain the flexibility of the interface and a Field-Programmable Gate Array (FPGA) is employed to control the number of measurement cycles by counting the rising edges of φ_1 and to send control signals $reset$, φ_x and φ_{ref} to the chip.



(a)



(b)

Fig 3-1: System-level diagram of the inverter-based capacitive sensor interface based on PM. (a) on-chip components (b) off-chip components

Accuracy requirements:

As is discuss in Section 2.1, the accuracy of the charge transfer depends on the g_m of the integrator, the loading of the integrator and the time period of the phase. Eq. 3-1 [1] indicates that the required g_m is highest in offset

measurement phase due to the smallest T_{clk} ,

$$g_m > 2 \ln 2 \frac{m+1}{T_{clk}} \left(C_{in} + C_L + \frac{C_{in} C_L}{C_{int}} \right), \quad (3-1)$$

where m is the target accuracy of the system in bits and T_{clk} is the time period for the charge transfer.

The simplified model of SC circuit in the proposed interface is shown in Fig 3-2 which is in phase ϕ_2 in offset measurement phase.

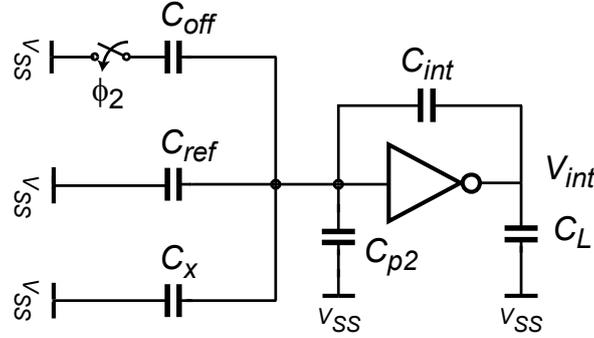


Fig 3-2: Simplified model of SC in the proposed interface

The required g_m calculation here is similar to that in [1] but the loading of the integrator is different due to the new auto-calibration scheme. The time constant τ is defined,

$$\tau = 2\pi C_0 / (\beta g_m), \quad (3-2)$$

where β is $\frac{C_{int}}{C_{int} + C_{off}}$ and C_0 is the loading of the integrator,

$$C_0 = \frac{C_{int} C_{tot}}{C_{int} + C_{tot}} + C_L, \quad (3-3)$$

where C_{tot} is the sum of C_{off} , C_{ref} , C_x and C_{p2} . To achieve enough accuracy, the time period has to satisfy the condition:

$$T_{clk} > (m + 1)\ln 2 \cdot \tau. \quad (3-4)$$

Given a specific V_{dd} , I_{int} and C_{off} , the time period is

$$T_{clk} = \frac{V_{dd}C_{off}}{I_{int}}. \quad (3-5)$$

From Eq. 3-2 to Eq. 3-5, the minimum transconductance of the integrator is

$$g_m > 2\pi\ln 2 \cdot \frac{(m+1)I_{int}}{V_{dd}C_{off}} \cdot \left(\frac{C_{int}C_{tot}}{C_{int}+C_{tot}} + C_L \right) \cdot \left(1 + \frac{C_{off}}{C_{int}} \right). \quad (3-6)$$

Measurement time requirements:

To get a ratiometric output M , three subsequent measurement of different capacitors are needed. In [2], the interface has better noise performance with higher number of measurement cycles N but it takes longer time to finish one measurement. Ignoring the time period of phase *reset*, the measurement time is approximately,

$$T_{meas} = 2N \cdot \frac{V_{dd}}{I_{int}} \cdot (3C_{off} + C_{ref} + C_x). \quad (3-7)$$

Resolution requirements:

In [2], a noise model has been derived. Moreover, it is found that the noise of the integration current sources are dominant, because the dual-integration-capacitor scheme cannot eliminate the noise of the integration current sources even though the low-frequency noise can be reduced by auto-calibration scheme, which means a low thermal-noise current source is needed. By tuning N , the targeted resolution can be achieved.

3.2. Inverter-based Integrator

The integrator in the interface is employed to transfer the charge stored in the input capacitor to C_{int} . It consists of an inverter-based OTA and an integration capacitor C_{int} . Before considering the g_m requirement of the OTA, C_{off} , C_{ref} , C_{int} and I_{int} need to be estimated. Even though a discrete-time feedback loop is employed to allow input capacitances larger than C_{int} , activating the feedback loop comes at the price of higher energy consumption. As a trade-off between energy consumption and the chip area, C_{int} is chosen to be 4 pF. C_{ref} is selected to be almost equal to the maximum value of input capacitance to minimize the non-linearity effect of auto-calibration scheme, 6.8 pF. Since C_{off} and I_{int} affect T_{clk} directly, a high g_m is required, consuming large current, if T_{clk} is short. Considering the current requirement of the chip, C_{off} is selected as 4 pF and I_{int} is 500 nA. Assuming C_{p2} is 15 pF and C_L is 1 pF, the minimum g_m of the inverter-based OTA is then 80 μ S. A larger value of g_m is chosen in order to accommodate larger parasitics.

Given the g_m of the inverter-based OTA, the power spectral density (PDS) of its input-referred voltage noise can be approximated by

$$S_{V_{n,OTA}}(f) = \frac{8}{3} \cdot \frac{kT}{g_m} (V^2/Hz), \quad (3-8)$$

where k is Boltzmann's constant, 1.38×10^{-23} (J/K), and T is the absolute temperature in Kelvin. Using the noise model derived in [2], the impact of this voltage noise on the measurement resolution can be derived. It meets the targeted resolution with the mentioned value of g_m , which is larger than $80 \mu\text{S}$.

To accommodate larger values of C_{p2} , the chip can be operated in two modes, high- g_m mode and low- g_m mode in Fig 3-3. Control signal EN enables an additional PMOS and NMOS in the OTA, whose size is the same as the original one, thus doubling the g_m at the expense of a doubling of the supply current.

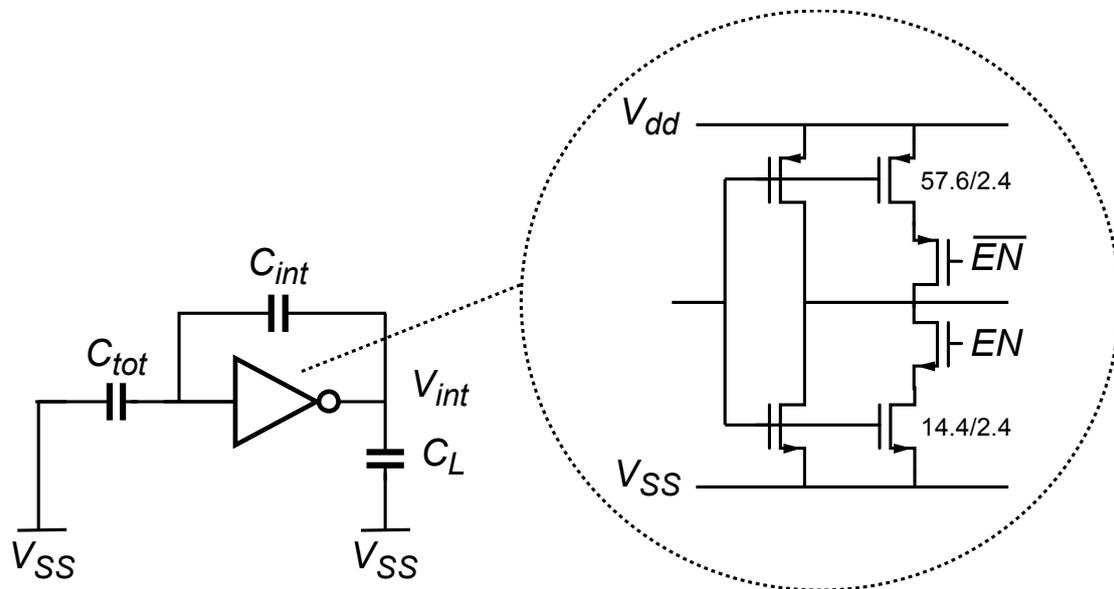


Fig 3-3: Schematic of the inverter-based integrator

Table 3-1 summarizes the parameters of the OTA.

Table 3-1: Simulated parameters of the inverter-based OTA

Parameters	Symbol	Low g_m mode	High g_m mode
Transconductance	g_m	$294 \mu\text{S}$	$580 \mu\text{S}$
Bias current	I_b	$11 \mu\text{A}$	$22 \mu\text{A}$
Nominal Votatge	V_n	471mV	472mV

3.3. Integration Current Sources

In Fig 3-1, two integration current sources are activated in two phases respectively. $I_{int,n}$ pulls charge from the input of the integrator during phase φ_1 while $I_{int,p}$ pumps charge into the input of the integrator during phase φ_2 . Given V_{dd} and the input capacitance, the measurement time period depends on $I_{int,n}$ and $I_{int,p}$.

As mentioned before, the noise of the integration current sources is the dominant noise source of the interface. The jitter caused by the other noise sources is strongly reduced by the dual-integration-capacitor scheme presented in Session 2.3. Only the jitters at the last two cycles remain, as so the impact of these noise sources reduces inversely proportional to the number of cycles N . While jitter caused by $I_{n,S}$ is not reduced by this scheme, its low-frequency components are reduced by the auto-calibration scheme. However, the auto-calibration scheme has effect on the noise at frequencies below $1/T_{meas}$, where T_{meas} can be calculated by Eq. 3-7.

Due to the finite output impedance of the current source, I_{int} changes according to the voltage at the input of the OTA. But this only affects the time period of T_o , T_{ref} , T_x but not the ratiometric output M , because the auto-calibration scheme attenuates the effect of I_{int} variation.

To sum up, the noise of current source plays an important role during the design. The resistively-degenerated current source structure shown in Fig. 3-4 is selected in the interface, because of the thermal noise of the degeneration resistor R_S is dominant if $1/g_m$ (g_m is the transconductance of the transistors) is much smaller than R_S , making it easier to design the current source in aspect

of noise.

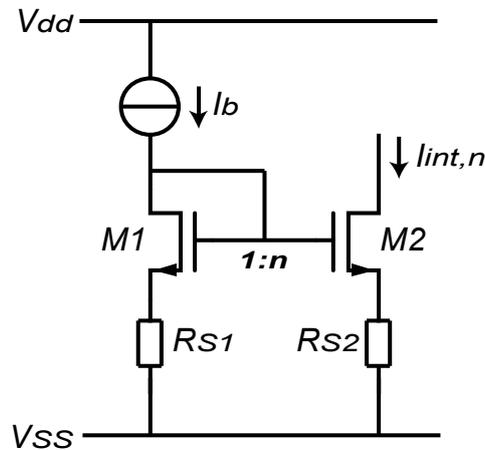


Fig 3-4: Current source with resistive-degeneration

Figure 3-5 shows the implementation of the sinking and sourcing integration current sources, $I_{int,n}$ and $I_{int,p}$, in aspect of matching. Both currents are derived from a single bias current I_b to reduce mismatch.

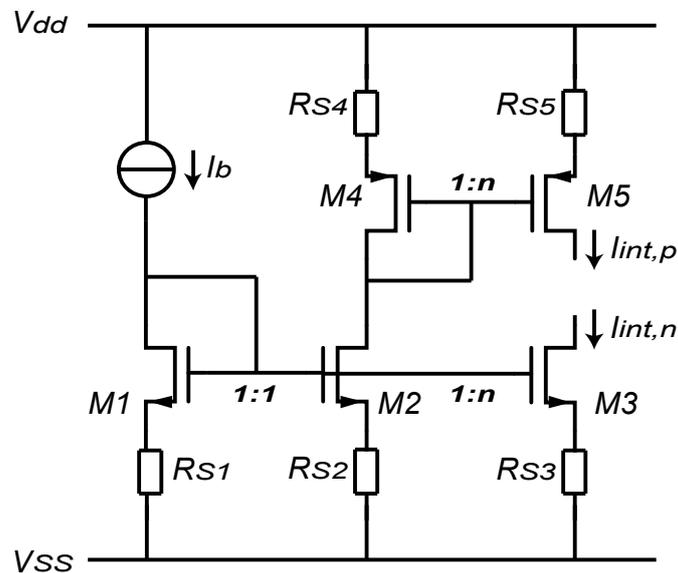


Fig 3-5: Implementation of sinking and sourcing integration current

In Fig 3-5, the noise of transistors $M1$, $M2$ and $M4$ is amplified by the current mirror ratio n making it the dominant noise in the structure. To ensure that the dominant noise is the thermal noise of R_{S3} and R_{S5} , a smaller ratio n , even

smaller than 1, is needed. However, this is not a power-efficient way since it consumes much power for bias circuit.

As shown in Fig 3-6, a sample-and-hold (S&H) circuit is added at the gates of $M3$ and $M5$ to circumvent this trade-off. At the beginning of the offset measurement phase, switches S are closed and sample capacitors C_S sample the gate voltage of $M3$ and $M5$. The switches S are open during the measurement, preventing the bias circuit from adding noise. The sampling causes the noise of bias circuit to be stored on C_S , but since it is constant during the measurement, it is compensated by the auto-calibration scheme. As a tradeoff of voltage headroom and matching between $I_{int,p}$ and $I_{int,n}$, the degeneration resistors R_{S3} and R_{S5} are selected as $300\text{ k}\Omega$ and the size of $M3$ and $M5$ are $12\text{ }\mu\text{m}/6\text{ }\mu\text{m}$ and $24\text{ }\mu\text{m}/6\text{ }\mu\text{m}$ respectively. As a tradeoff of the die size and the leakage of the sampling capacitors, the size of sampling capacitors is 26 pF .

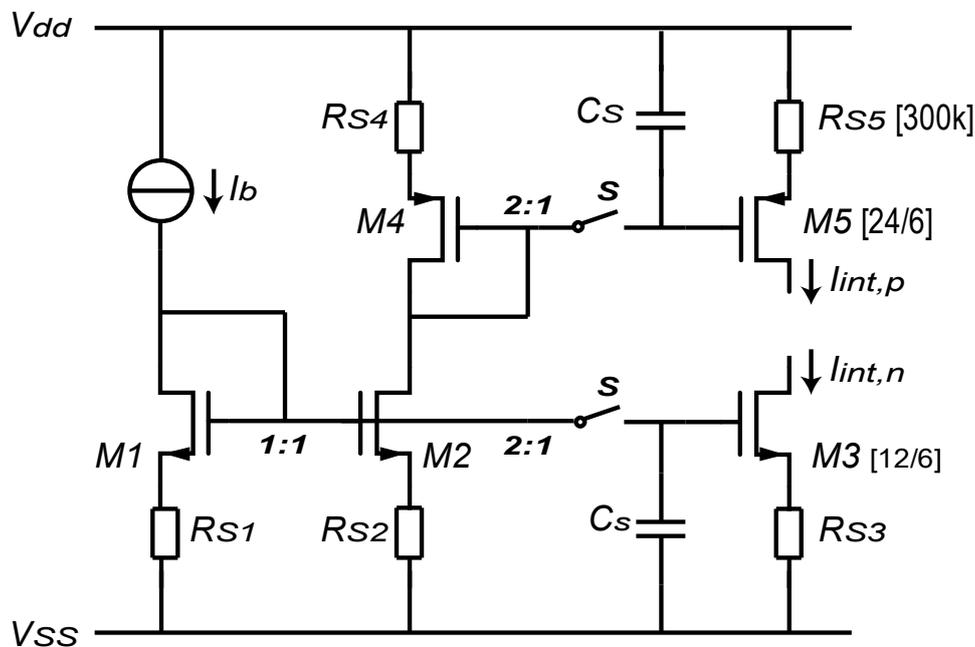


Fig 3-6: Implementation of sinking and sourcing integration current with S&H circuit

voltage to define the comparator's threshold is unnecessary. A single-ended inverter-based comparator can be employed. To increase the power-efficiency of the comparator, a slower comparator can be employed with smaller current consumption [4]. However, the speed of the comparator cannot be arbitrarily slow. With a slow comparator, the zero crossing and the trigger of switching the threshold to V_{th} cannot be detected due to short time difference between them. Therefore, the voltage difference between $V_{th,up}$, $V_{th,dn}$ and V_{th} cannot be too small.

Table 3-3 lists the simulated parameters of the multi-level comparator. .

Table 3-3: Simulated parameters of the multi-level comparator

Parameters	Symbol	Comparator
Transconductance	g_m	40 μS
Bias current	I_b	1.5 μA
Normal threshold	V_{th}	474 mV
Upper threshold	$V_{th,up}$	570 mV
Lower threshold	$V_{th,dn}$	439 mV

3.5. Discrete-time Feedback Loop

3.5.1. Switched Current Sources

The main concern about the design of the switched current sources is the current level I_{drive} , which has to be sufficient to handle the parasitics. However, the discrete-time feedback loop is activated at a high frequency if I_{drive} is too large, consuming energy. Based on the model shown in Fig 3-8, the following requirement for I_{drive} can be derived:

$$I_{drive} > \frac{C_{p1} + C_{in,min}}{C_{in,min}} \cdot I_{int,n}, \quad (3-9)$$

where $C_{in,min}$ is the minimum input capacitance, 4 pF.

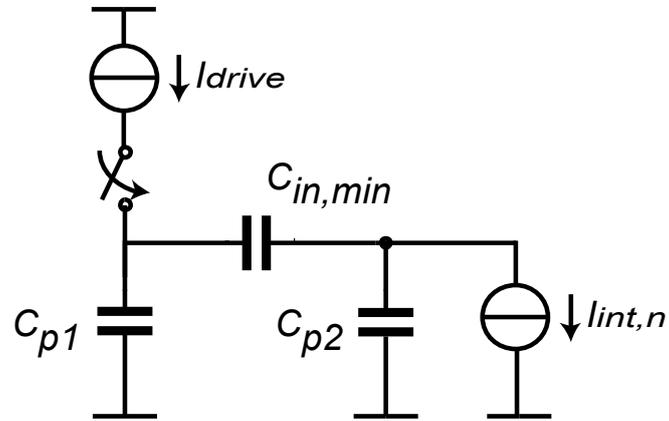


Fig 3-8: Circuit model of discrete-time feedback loop

In order to make the interface more flexible to handle different parasitics, I_{drive} is made programmable by employing a 3-bit current digital-to-analog converter (IDAC). Fig 3-9 shows the implementation of switched current sources. In Fig 3-9, $M0$, $M1$ and $M2$ are used to control the current value of IDAC and $limit_H$ and $limit_L$ are provided by the discrete-time feedback loop. And Table 3-4 lists the simulation results of the current values. According to Eq 3-13, the maximum value of C_{p1} that can be tolerated is 52 pF.

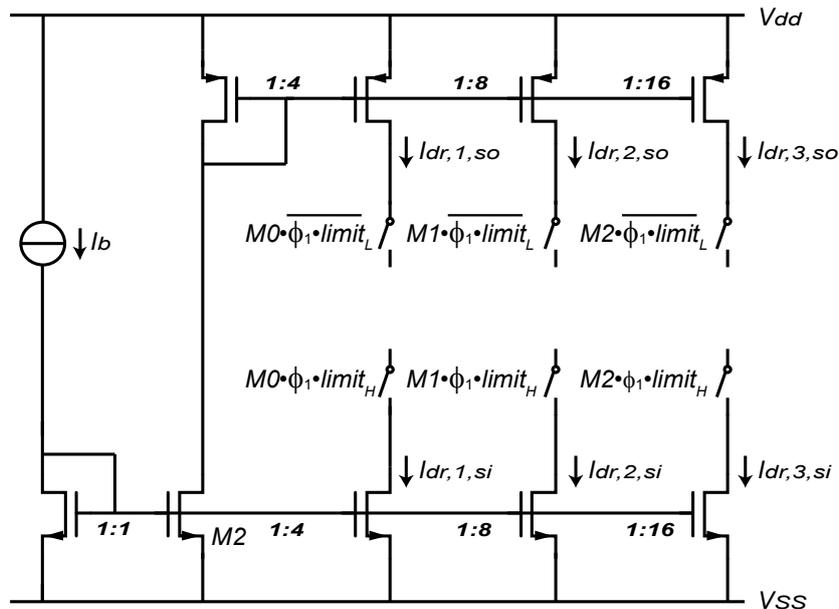


Fig 3-9: Implementation of switched current sources

Table 3-4: Simulated parameters of IDACs

Parameters	Symbol	Sourcing IDAC	Sinking IDAC
Current at 1 st bit	$I_{dr,1}$	1 μA	1.1 μA
Current at 2 nd bit	$I_{dr,2}$	2 μA	2.2 μA
Current at 3 rd bit	$I_{dr,3}$	4 μA	4.4 μA

3.5.2. Comparators with Hysteresis

The two comparators with hysteresis are employed in in phase ϕ_1 and phase ϕ_2 respectively to prevent the output of the integrator from going out of range. These comparators have been implemented using simple Schmitt-trigger logic gates [5], as shown in Fig 3-10. The transistors are sized to obtain appropriate threshold levels to enable the proper operation of the discrete-time feedback loop, which is shown in Table 3-5.

Table 3-5: Simulated threshold levels of Schmitt-trigger logic gates

Parameters	Symbol	Logic gate used in	Logic gate used in
		phase φ_1	phase φ_2
Upper threshold voltage	$V_{th,H}$	372 mV	724 mV
Lower threshold voltage	$V_{th,L}$	194 mV	586 mV

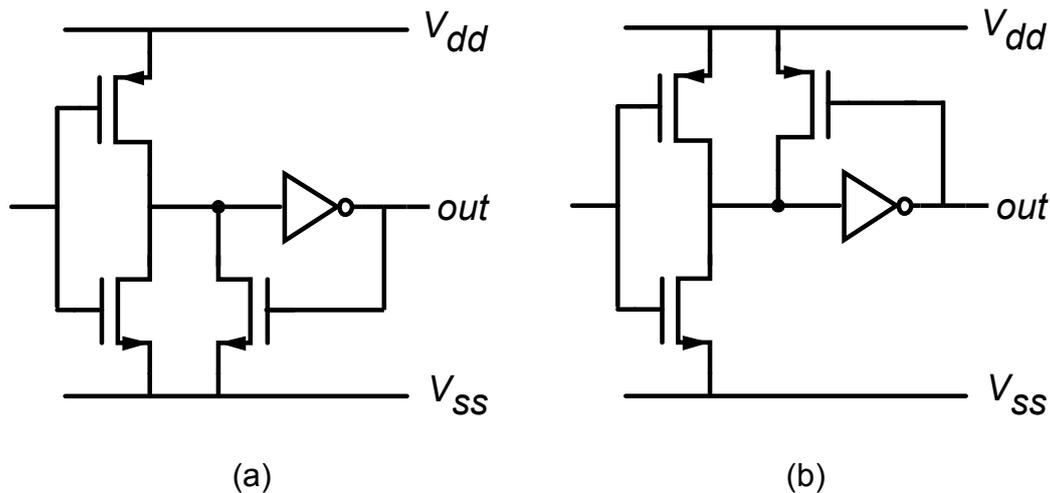


Fig 3-10: Implementation of Schmitt-trigger logic gates (a) used in phase φ_1
 (b) used in φ_2

3.6. Clock Booster

In standard CMOS technologies, the threshold voltage of transistors does not scale with the supply voltage. Most switches in the interface are implemented by transmission gate [6] to allow large voltage swing. But the switches, which control the selection of the dual integration capacitors, operate in mid supply voltage 0.5 V, which makes the switches have large on-resistance R_{on} . A clock booster technique is applied to ensure the proper operation of switches at low supply voltages [7-9].

In Fig 3-11, the clock booster driving a switch $M3$ includes a charge-pump circuit with cross-coupled NMOSs ($M1$ and $M2$) and a boosted clock signal generator.

undesired multiple transitions at the output of the comparator. These may arise due to noise at the comparator's input, as illustrated in Fig 3-12 (a). These pulses make the comparator send some wrong signals to the logic control to change the state of the interface. To remove these pulses, a dead-time generator [4] in Fig 3-12 (b) is employed. At the moment that V_{in} changes, the inputs of the XOR gate are the same and therefore the latch locks D_{in} . After 1 ns, due to the RC delay in the circuit, the inputs of the XOR are different and therefore the latch is transparent until V_{in} changes again.

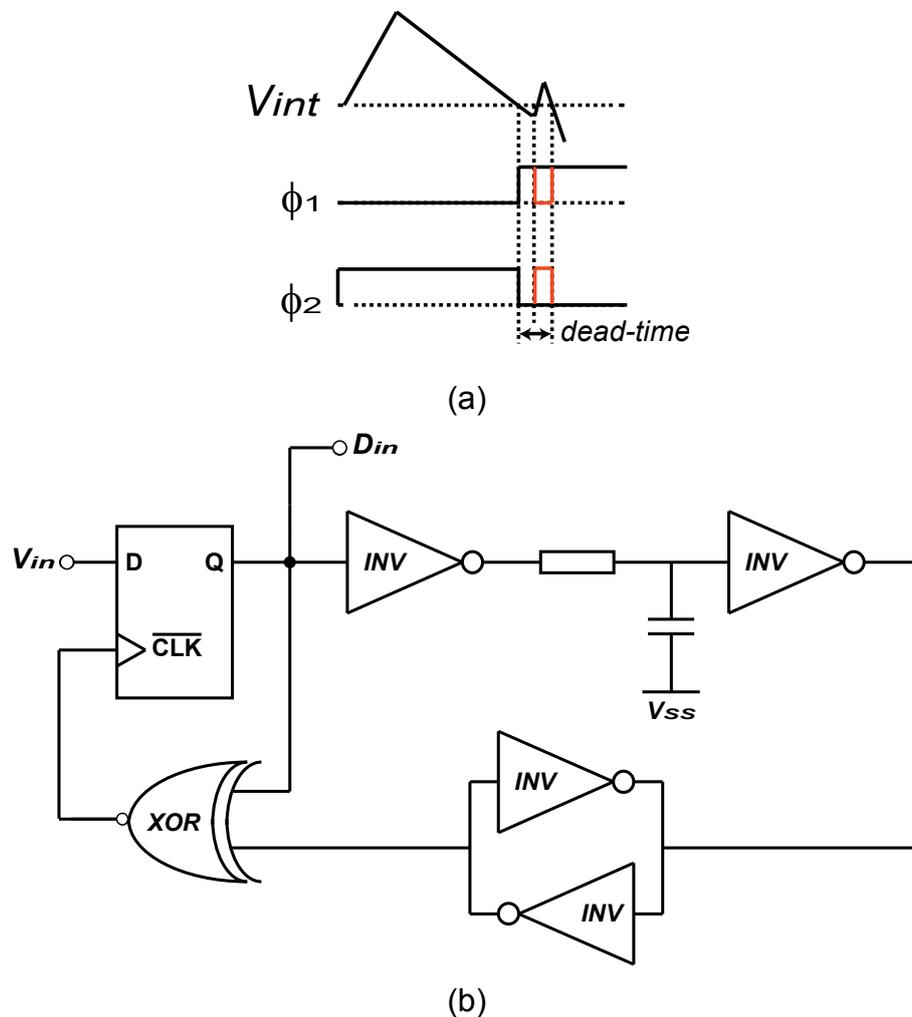
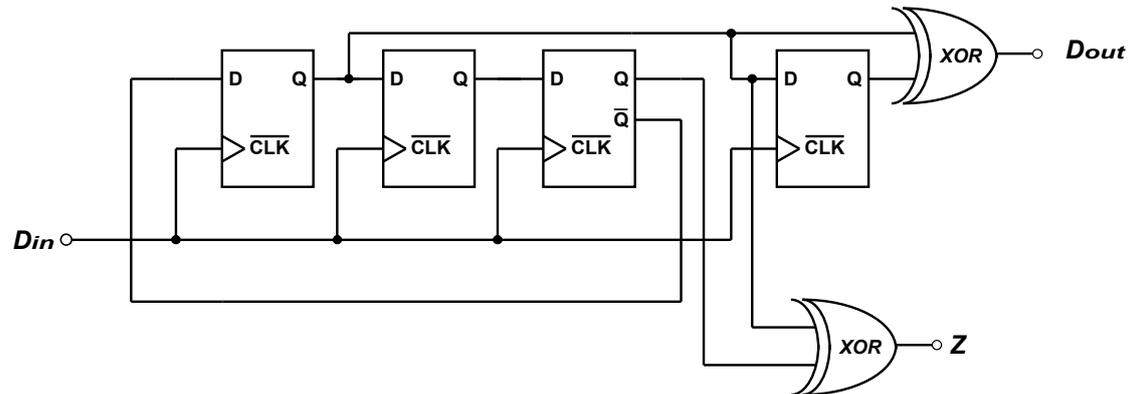


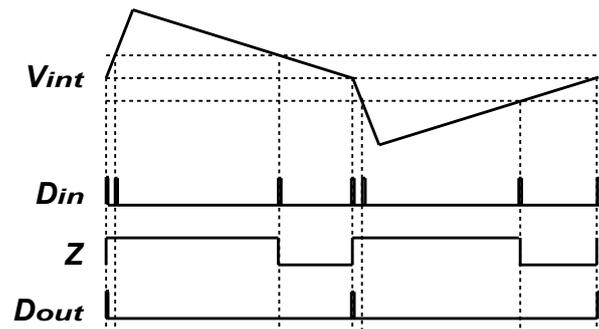
Fig 3-12: (a) Timing diagram (b) Implementation of dead-time generator

The implementation of the multi-level comparator controller is shown in Fig 3-13 (a). Every three transitions of digital input D_{in} , which has a rising-edge when

the output of the integrator goes across the threshold voltage of the comparator, the digital output D_{out} has a rising-edge, triggering the phase shifts. The signal Z controls the threshold of the comparator and the hard-switches for the discrete-time feedback loop. The timing diagram is shown in Fig 3-13 (b).



(a)



(b)

Fig 3-13: (a) Implementation of multi-level controller (b) Timing diagram

To ensure the proper operation of the interface, a non-overlapping clock generator is required, the implementation of which is shown in in Fig 3-14 [5].

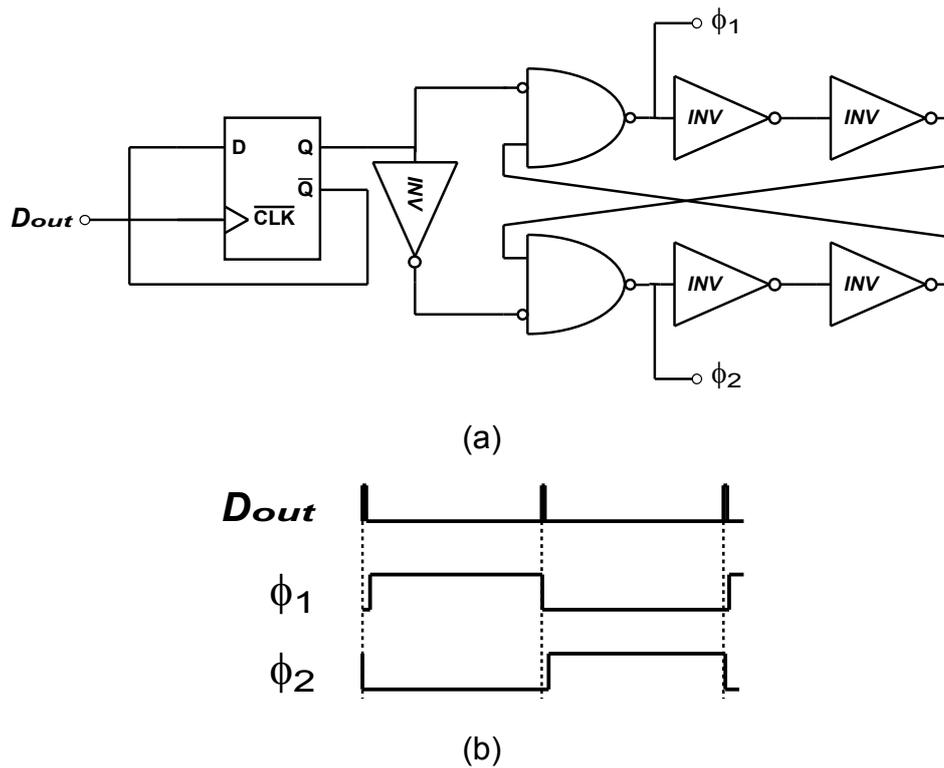


Fig 3-14: (a) Implementation of non-overlapping clock generator (b) Timing diagram

3.8. Design for Testability

To configure the operation of the interface, six control signals are needed: the control signal of IDAC (3 bits: $M0$, $M1$ and $M2$), the g_m mode of the OTA (1 bit: EN) and the auto-calibration phase (2 bits: ϕ_{ref} and ϕ_{ref}). These signals can be controlled by off-chip components via six I/O pins and, however, this approach would increase the number of I/O pins of the chip and its area, because the chip is pad-limited. A 6-bit serial-in, parallel-out shift register is employed to decrease the number of pins from six to three, serial input (IN), clock (CLK) and an enable trigger (EN_{sf}). Fig 3-15 (a) shows the implementation of the 6-bit shift register. Fig 3-15 (b) shows the timing diagram of the shift register. Table 3-6 lists the output of the 6-bit shift register.

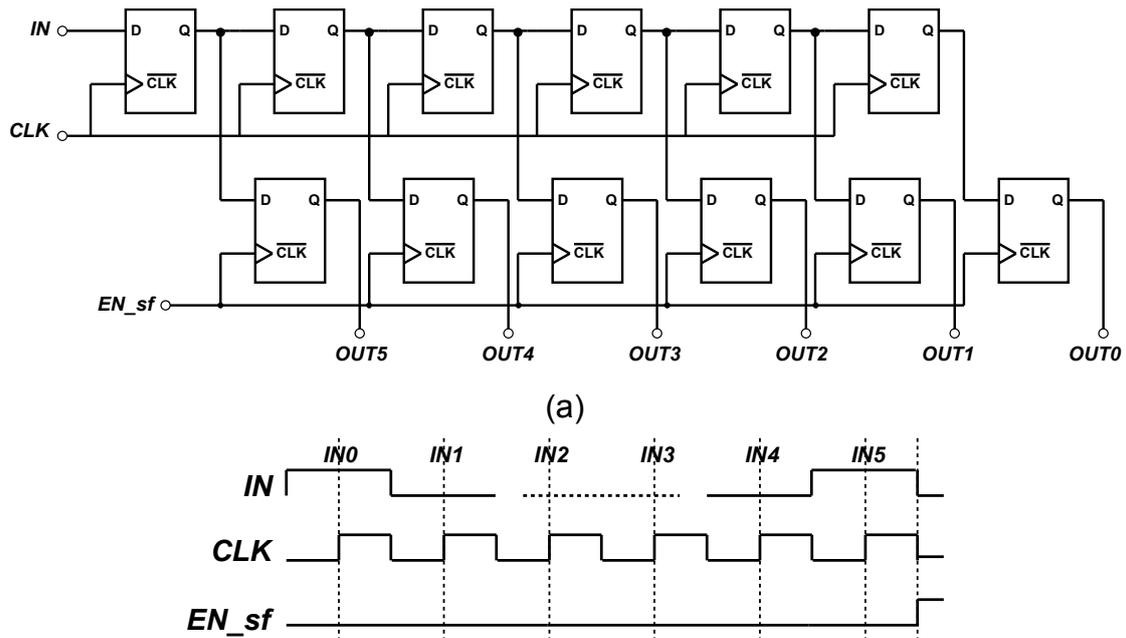


Fig 3-15: (a) Implementation of 6-bit shift register (b) Timing diagram

Table 3-6: Output of the 6-bit shift register

Parameters	Symbol	Corresponding control Signal
1 st bit	<i>OUT0</i>	φ_{ref}
2 nd bit	<i>OUT1</i>	φ_x
3 rd bit	<i>OUT2</i>	<i>EN</i>
4 th bit	<i>OUT3</i>	<i>M0</i>
5 th bit	<i>OUT4</i>	<i>M1</i>
6 th bit	<i>OUT5</i>	<i>M2</i>

In order to be able to observe the voltage waveform at the output of the integrator, an analog buffer is employed, which is a PMOS source-follower in Fig 3-16. The source of the PMOS is driven by a constant off-chip current source. By observing the output of the source-follower V_{SF} , the waveform of V_{int} can be estimated.

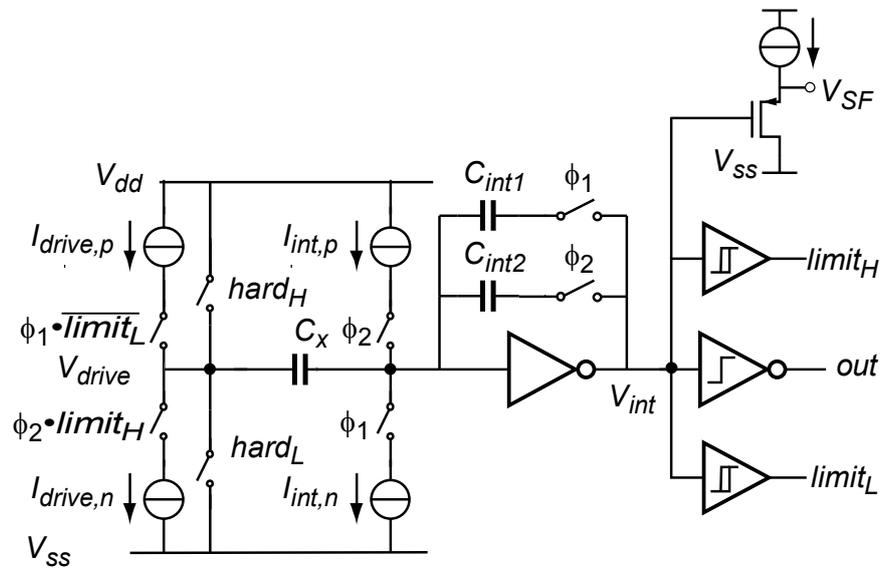


Fig 3-16: Implementation of PMOS source-follower

3.9. Layout

Fig 3-17 shows the layout diagram of the interface with critical sub-blocks. The active area is 0.05 mm^2 ($0.235 \text{ mm} \times 0.22 \text{ mm}$) and 22 pads are used, of which 11 are digital and 11 are analog. Table 3-7 describes the function of each pin.

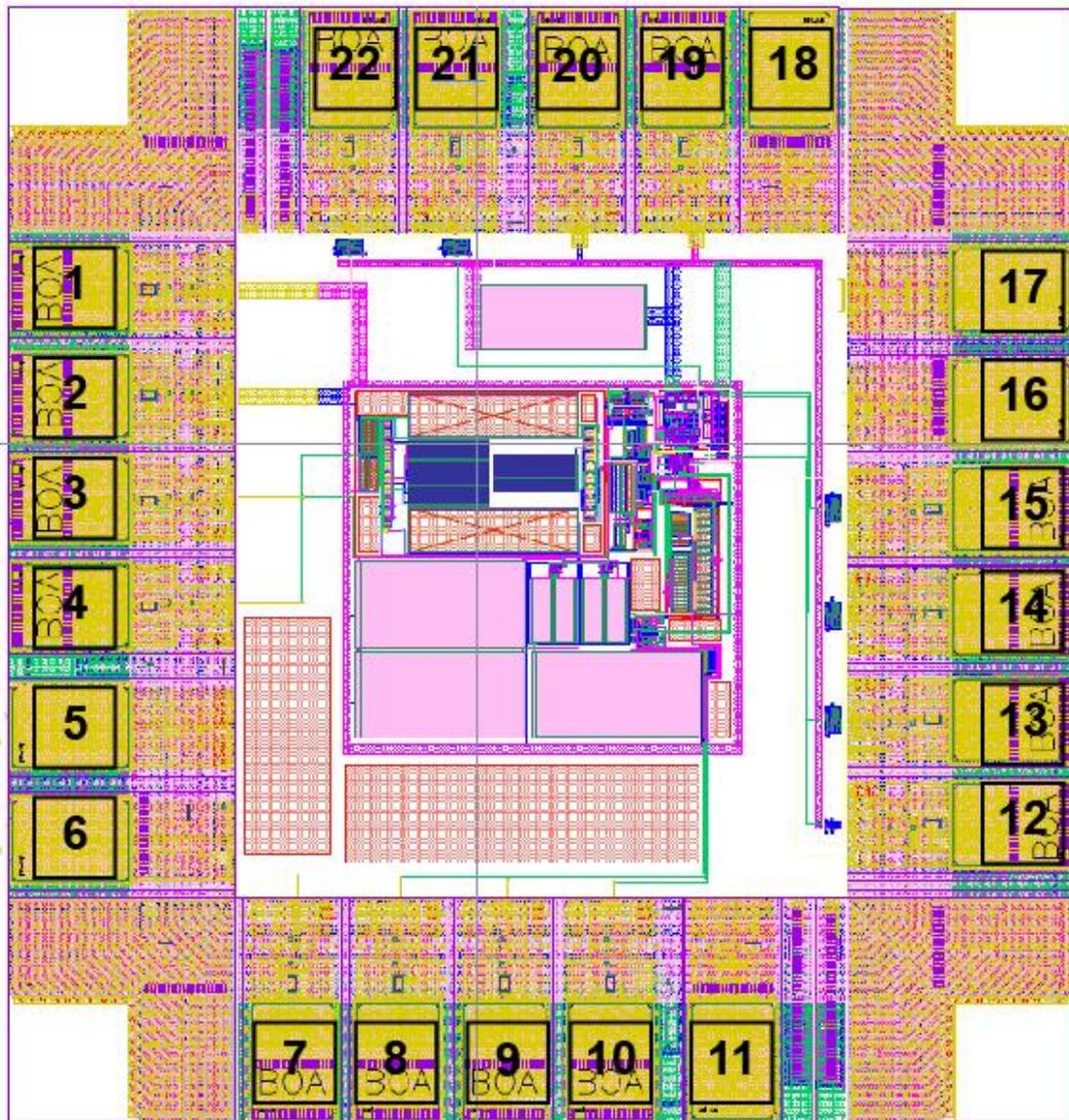


Fig 3-17: Layout of the capacitive sensor interface

Table 3-7: I/O pin details

Pin number	Name	Description
1,2	<i>AVDD, AGND</i>	1 V supply and ground for analog circuit
3	V_{in}	To connect C_{ref} and C_x to the input of the OTA
4	I_b	Bias current input for I_{int} (Fig. 3.5)
5,6	<i>AVDDCORE, AVSSCORE</i>	1 V supply and ground for analog pad ring
7	V_{SF}	PMOS source-follower output
8,9	V_{ref}, V_x	To connect drive side of C_{ref} and C_x
10	I_{b2}	Bias current input for IDAC (Fig. 3.9)
11	<i>AVDDE</i>	1 V supply for analog pad ring
12	<i>PH1OUT</i>	Output of phase ϕ_1
13	<i>EN_S</i>	S&H enable signal
14,15	<i>EN_sf, IN</i>	Enable trigger and serial input of shift register
16,17,18	<i>DVSSCORE, DVDDCORE, DVDDE</i>	1 V supply and ground for digital pad ring
19,20	<i>DVDD, DGND</i>	1 V supply and ground for digital circuit
21	<i>CLK</i>	Clock signal for shift register
22	<i>RESET</i>	Reset signal for reset phase

References

- [1] Z. Tan, "Energy-Efficient Capacitive Sensor Interfaces", Ph.D Thesis, Delft University of Technology, Delft, the Netherlands, 2013
- [2] S. Heidary Shalmany, et al., "Noise Analysis for Period-Modulation-Based Capacitive Sensor Interfaces", in process
- [3] A. Heidary, "A Low-Cost Universal Integrated Interface for Capacitive Sensors", Ph.D Thesis, Delft University of Technology, Delft, the Netherlands, 2010
- [4] Z. Tan, et al., "An Energy-Efficient 15-Bit Capacitive-Sensor Interface Based on Period Modulation," JSSC, vol. 47, no. 7, pp. 1703-1711, July 2012.
- [5] J. M. Rabaey, A. Chandrakasan, and B. Nikolic, "Digital Integrated Circuits - A Design Perspective (2nd Edition)", Prentice Hall, 2003.
- [6] W. M. C. Sansen, "Analog Design Essentials", Dordrecht, the Netherlands: Springer, 2006
- [7] T. Cho and P. Gray, "A 10 b, 20 Msample/s, 35 mW pipeline A/D converter", IEEE J. Solid-State Circuits, vol. 30, pp.166 -172, 1995
- [8] Y. Nakagome, et al., "An experimental 1.5-V 64-Mb DRAM", IEEE J. Solid-State Circuits, vol. 26, no. 4, pp.465 -472, 1991
- [9] C. Chen, Z. Tan and M. Pertijsse. "A 1V 14b Self-Timed Zero-Crossing-Based Incremental $\Delta\Sigma$ ADC", ISSCC, pp. 274-275, Feb. 2013

Chapter 4

Measurement Results

In this chapter, measurement results of the inverter-based capacitive sensor interface based on period modulation are presented. The fabricated chip is briefly introduced at first. Then the measurement setup is discussed in detail. At last, the measurement results are given.

4.1. Fabricated Chip

The interface has been implemented in a 0.16- μm CMOS process. Fig 4-1 shows the die microphotograph. The chip area is 0.56 mm^2 ($0.75 \text{ mm} \times 0.75 \text{ mm}$) and the active area is 0.05 mm^2 ($0.235 \text{ mm} \times 0.22 \text{ mm}$).

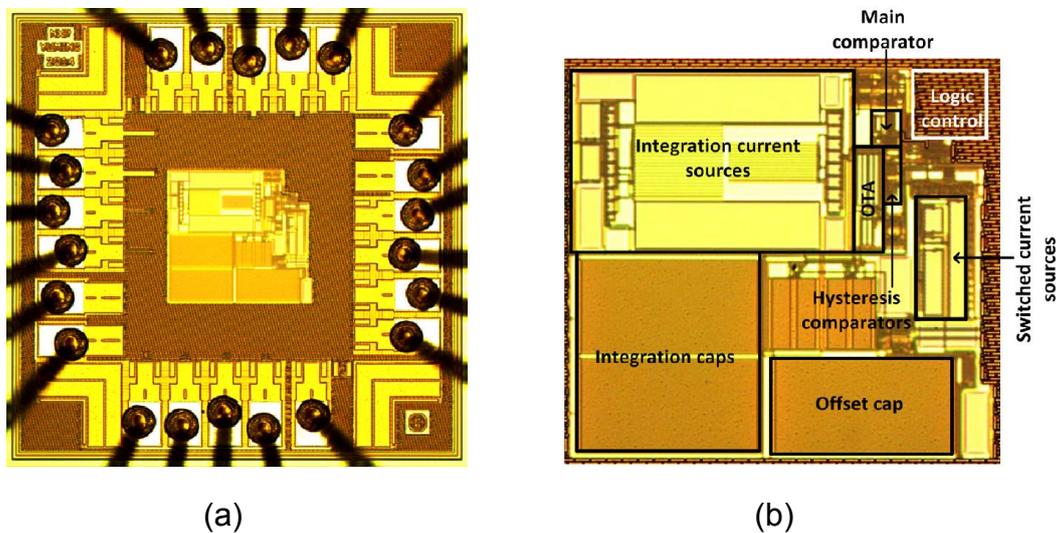


Fig 4-1: (a) Die microphotograph (b) Active area with identifications of key areas

4.2. Measurement Setup

4.2.1. Equipment

An overview of the measurement setup is depicted in Fig 4-2.

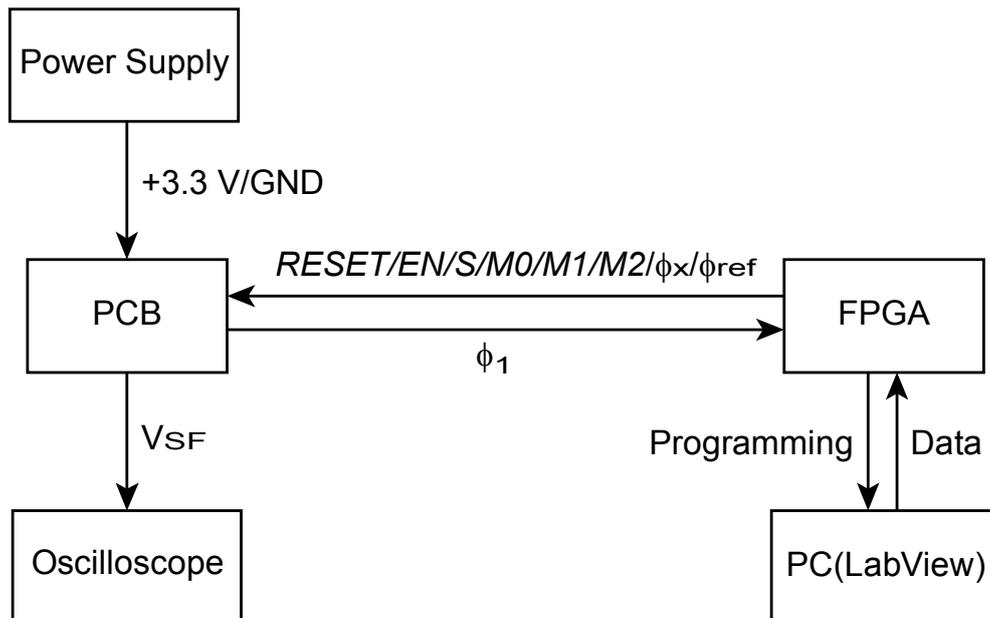


Fig 4-2: Overview of the measurement setup equipment

Several measurement equipment have been used:

a. Power supply

It provides positive supply voltage (+3.3 V) and ground (GND) for the test printed circuit board (PCB), which will discuss in next session.

b. Oscilloscope

The oscilloscope shows the output voltage of the source follower V_{SF} .

c. FPGA development board

The FPGA development board quantizes the measurement time, counts the number of measurement cycles and provides the control signals (*RESET*, *EN*, *EN_S*, *M0*, *M1*, *M2*, φ_x and φ_{ref}) for the test board.

d. PC

A LabView program running on a PC reads the data from the FPGA and processes it to get the final measurement value. Moreover, it is used for setting the parameters of the measurement, for example the number of measurement cycles.

4.2.2. Test PCB

The test board is used for providing a supply voltage to the analog and digital part of the fabricated chip and for providing bias currents to the chip. Moreover, off-chip capacitors C_x and C_{ref} are mounted on the board. Since the levels of the control signals of the chip and the FPGA are different, 1 V to 3.3 V level shifters are used. Fig 4-3 shows the layout of the test board and the components.

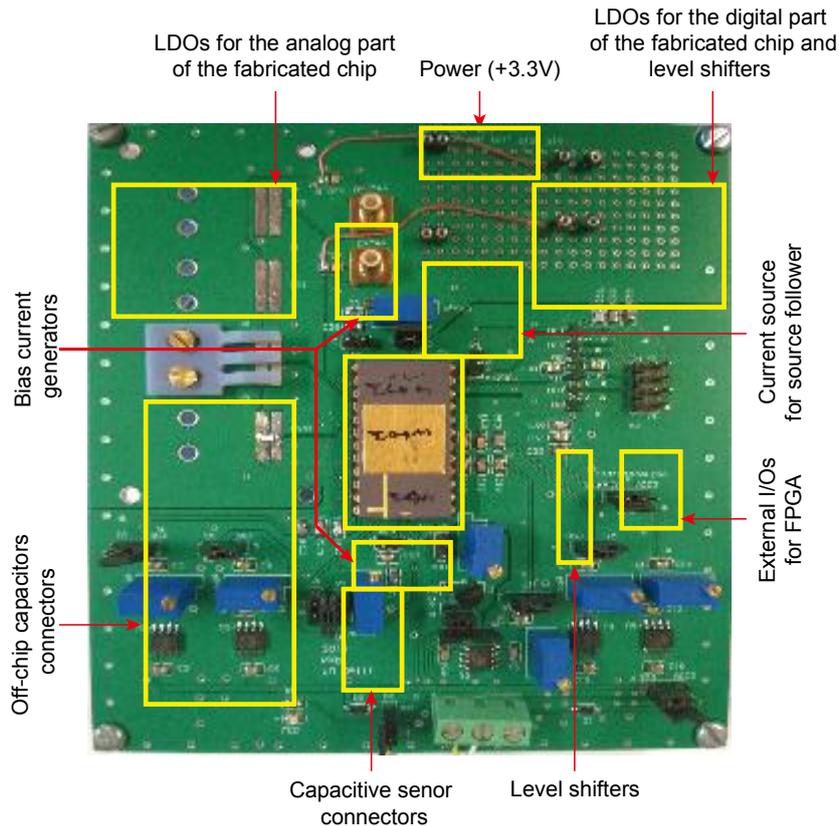


Fig 4-3: Layout of the test board and components

4.3. Measurement Results

Table 4-1 lists the conditions that have been used for the measurements, unless stated otherwise in the description below.

Table 4-1: Normal measurement conditions

Conditions	Symbol	Value
Measurement cycles	N	32
Reference capacitance	C_{ref}	6.8 pF
g_m -mode	N.A.	low
Drive current	I_{drive}	7 μA

4.3.1. Resolution

In order to analyze the noise performance of the interface, off-chip discrete capacitors are connected as C_x and an off-chip discrete reference capacitor is

connected as C_{ref} . To determine the resolution, 2000 samples are measured for the same C_x and the standard deviation of the measurement results $\sigma(M)$ is calculated. This is translated to an equivalent input-referred noise level $\sigma(C_x)$ by multiplying it with C_{ref} .

Fig 4-4 shows the resolution thus obtained for different C_x values with and without activating the S&H circuits in the integration current sources. Without activating the S&H circuits in the integration current sources, the resolution is degraded due to noise of the bias circuit. With the S&H enabled, a significant improvement is obtained.

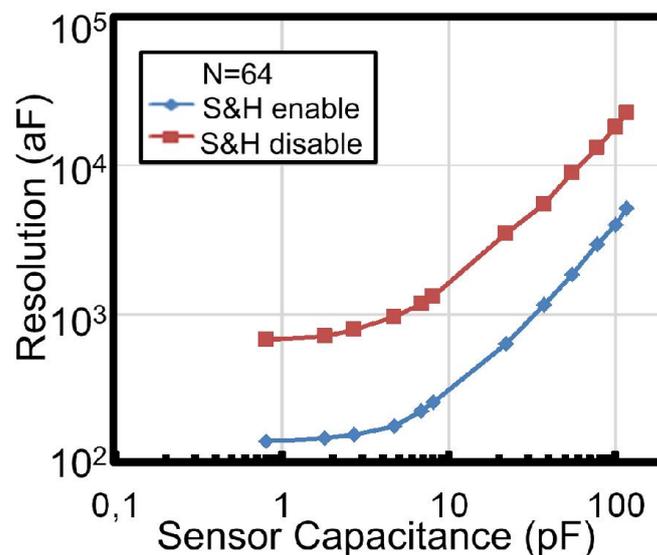
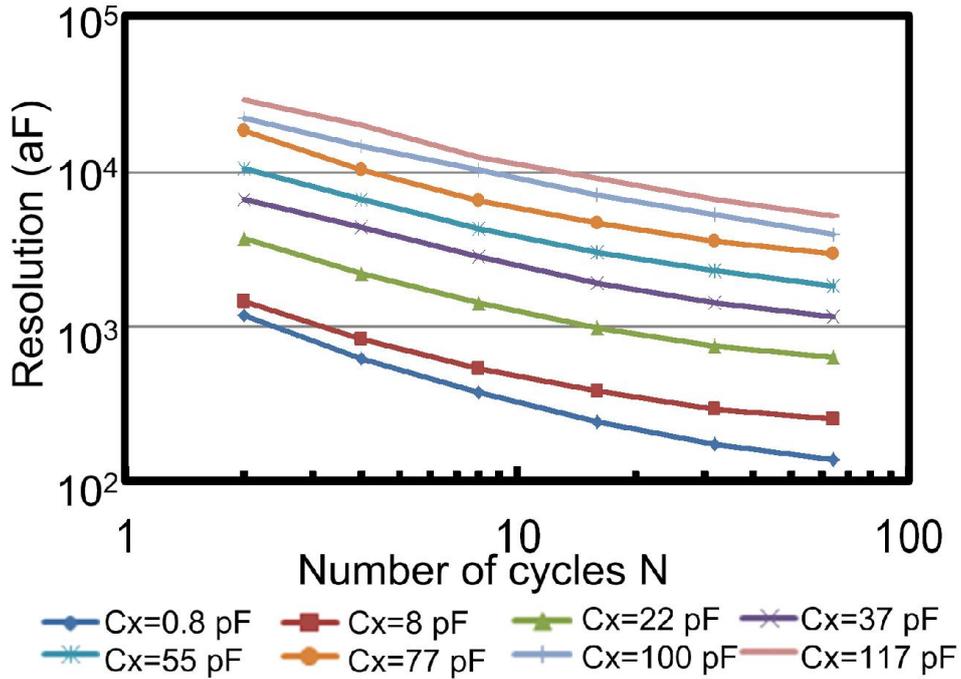


Fig 4-4: Resolution as a function of C_x

Fig 4-5 shows the resolution of the interface for different numbers of measurement cycles N . The results shown are for the low-gm mode; the high-gm mode provides comparable results. As is shown in Fig 4-5, the interface is capable of handling a wide range of capacitance values, far exceeding the reference capacitance and on-chip capacitance, making it suitable for interfacing with larger off-chip sensor capacitors.

Fig 4-5: Resolution as a function of N

The signal-to-noise ratio (SNR) and the effective number of bits (ENOB) of the interface in bits can be defined as follows:

$$SNR = 20 \cdot \log\left(\frac{C_{FS}/2\sqrt{2}}{\sigma(C_x)}\right), \quad (4-1)$$

where $\sigma(C_x)$ is the input-referred noise level described earlier, and C_{FS} is the input full-scale range of C_x .

$$ENOB = (SNR - 1.76)/6.02. \quad (4-2)$$

To meet the targeted specifications, N is chosen to be 32. Fig 4-6 shows the calculated resolution, which is based on [5], and measured resolution as a function of C_x across the targeted capacitance range.

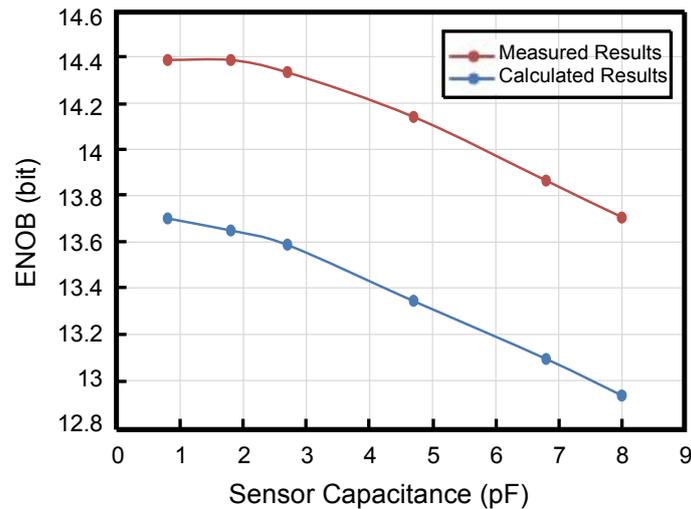


Fig 4-6: Simulated and measured resolution as a function of C_x

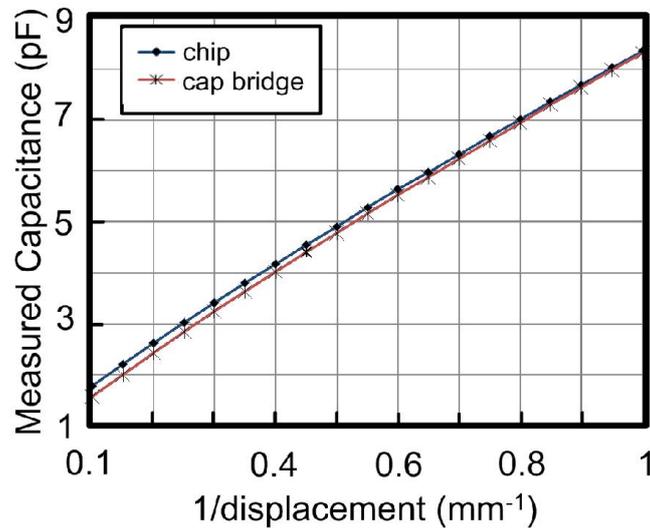
In Fig 4-6, it can be seen that the measured results show the same trend as the calculated results, but are around 0.7 bit lower than the calculation. The reason for this discrepancy is not yet clear at the time of this writing. Noise associated with the power supply could be a possible explanation, as this is not taken into account in the noise model [5]. The lowest ENOB is 12.9 bit when the input capacitance is 8 pF.

4.3.2. Linearity

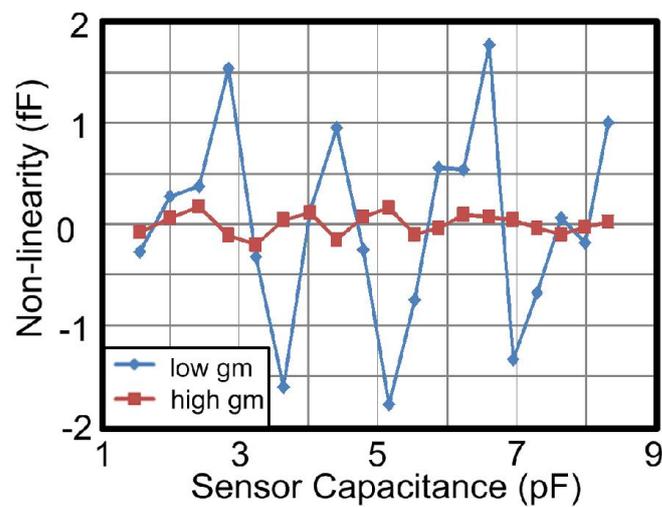
The linearity measurement was performed by comparing the capacitance measured using the interface with that measured by a precision capacitance bridge (Andeen-Hagerling AH 2700A). A parallel-plate capacitor mounted on a linear displacement stage is used as sensor capacitance to be able to sweep the capacitance across the range of interest.

Fig 4-7 (a) shows the output capacitance of the capacitive interface and the capacitive bridge as a function of $1/d$ (d is the distance between the parallel plates). The difference between the curves, which represents the measurement error of the interface, is largely is linear function of C_x , due the finite accuracy

of the reference capacitor on the test board. Fig 4-7 (b) shows the integral nonlinearity (INL), obtained by removing the linear component of the error, as a function of the sensor capacitance in high- g_m and low- g_m mode.



(a)



(b)

Fig 4-7: (a) Measured capacitance as a function of $1/d$ (b) INL as a function of sensor capacitance

In Fig 4-7(b), it can be seen that, in the low- g_m mode, the peak non-linearity is below ± 2 fF, while for the high- g_m mode it improves to less than ± 0.25 fF, which

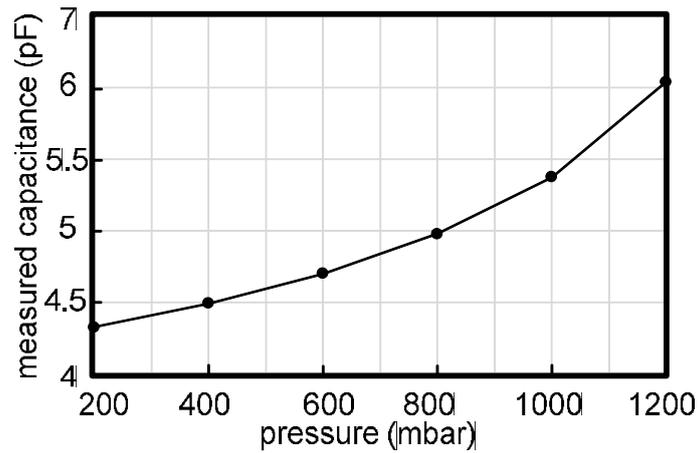
corresponds to 14 bits on the range of 8 pF. The INL is lower than what is expected during the design, because of the limited reproducibility of the linearity measurements. Specifically, the capacitive sensor is connected to the interface or the capacitive bridge using a relay. Our hypothesis is that unstable parasitic capacitance of the mechanical switches in the relay cause the limited reproducibility.

4.3.3. Pressure Measurement

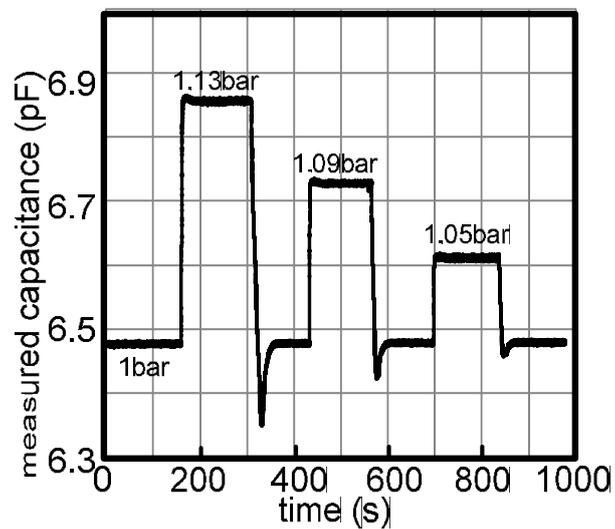
A pressure measurement was taken by connecting 4 MEMS pressure sensors, whose characteristics are listed in Table 4-2 [6], in parallel to the interface by a shielded cable, giving a nominal sensor capacitance C_x of about 4 pF and parasitic capacitances C_{p1} and C_{p2} of roughly 40 pF. A first measurement was performed by sweeping the pressure from 200 mbar to 1200 mbar and measuring the capacitance of the pressure sensor after the pressure becomes stable in a vacuum chamber. The results are shown in Fig 4-8 (a), which is similar to the characteristic curve of the sensor [6]. In Fig 4-8 (b), a second measurement was performed by measuring the capacitance of the pressure sensor as a function of time while the pressure in the chamber is changed in steps.

Table 4-2: Characteristics of the MEMS pressure sensor

Parameters	Value
Nominal capacitance	0.95 pF
Capacitance range (0.5 – 1.3 bar)	0.45 pF



(a)



(b)

Fig 4-8: (a) Measured capacitance as a function of pressure (b) Measured capacitance as a function of time

4.3.4. Performance Summary

In order to have a quantitative comparison between different interfaces, a figure of merit (FoM) that normalizes the energy consumption to the resolution, is defined as:

$$FoM = P \cdot T_{meas} / 2^{ENOB}, \quad (4-3)$$

where P is the power consumption of the interface and T_{meas} is the measurement time.

Table 4-3 summarizes the performance of the interface and compares it to prior CDCs with ENOB larger than 10 bit.

Table 4-3: Summary of the performance of the interface and comparison between different types of CDCs

	[1]	[2]	[3]	[4]	This work		
Technology	0.35 μ m CMOS	0.35 μ m CMOS	0.18 μ m CMOS	0.18 μ m CMOS	0.16 μ m CMOS		
Type	PM	DS	SAR	DS + SAR	PM		
Supply voltage	3.3 V	3.3 V	1.2 V (Analog) 0.9 V (Digital)	1.4 V	1 V		
Supply current	64 μ A	4.5 mA	N.A.	24 μ A	14 μ A		
Power	211 μ W	14.9 mW	160 nW	33.7 μ W	14 μ W		
Input range (pF)	0 – 6.8	8.4 – 11.6	2.5 – 75.3	0 – 24	0 – 8 ¹		
Meas. time	7.6 ms	20 ms	4 ms	230 ms	0.21 ms (N=2)	3.43 ms (N=32)	6.86 ms (N=64)
Resolution	208 aF _{rms}	65 aF _{rms}	6 fF _{rms}	156 aF _{rms}	1443 aF _{rms}	295 aF _{rms}	255 aF _{rms}
ENOB (bit)	13.5	13.80	11.8	15.44	10.6	12.9	13.1
FoM (pJ/step)	138.6	20.9	0.181	0.175	1.87	6.1	10.6
Area (mm ²)	0.51	2.6	0.49	0.456	0.05		

¹ Chosen as example; the CDC can handle larger capacitances (see Fig 4-5)

The effectiveness of the circuit topologies discussed in previous chapter has been tested and verified. Compared to prior capacitive sensor interface based on PM [1], the energy consumption and die size of the interface are more than an order-of-magnitude smaller. Compared with other designs with comparable resolution [2-4], it is 9 times smaller, making it an attractive candidate for area- and energy-constrained applications.

References

- [1] Z. Tan, et al., "An Energy-Efficient 15-Bit Capacitive-Sensor Interface Based on Period Modulation," JSSC, vol. 47, no. 7, pp. 1703-1711, July 2012.
- [2] X. Sha, et al., "A Capacitance-to-Digital Converter for Displacement Sensing with 17b Resolution and 20 μ s Conversion Time," ISSCC, pp. 198-199, Feb. 2012
- [3] H. Ha, et al., "A 160nW 69.3fJ/conversion-step Capacitance-to-Digital Converter for Ultra-Low-Power Wireless Sensor Nodes," ISSCC, pp. 220-221, Feb. 2014
- [4] S. Oh, et al., "15.4b Incremental Sigma-Delta Capacitance-to-Digital Converter with Zoom-in 9b Asynchronous SAR," VLSI Circ. Symp., June 2014.
- [5] S. Heidary Shalmany, et al., "Noise Analysis for Period-Modulation-Based Capacitive Sensor Interfaces", in process
- [6] L. Rajendran, "Design of an Energy-Efficient Interface Circuit for a MEMS-based Capacitive Pressure Sensor", Master Thesis, Delft University of Technology, Delft, the Netherlands, 2013

Chapter 5

Conclusions

5.1. Thesis Contributions

An inverter-based capacitive-sensor interface based on period modulation has been proposed in this thesis, which has been implemented in a $0.16 \mu\text{m}$ CMOS process and achieves the targeted performance. Using a discrete-time feedback loop that eliminates the need for a large integration capacitor, a dual-integration-capacitor scheme that reduces the front-end noise, and a sampled-biasing technique that reduces integration current noise, the interface is 9 times smaller than prior capacitive-sensor interfaces with larger than 10 bit resolution, and improves the energy efficiency by more than 10 times compared previous interfaces based on PM [1-3]. The energy consumption per measurement for various types of interfaces with this work is shown in Fig 5-1.

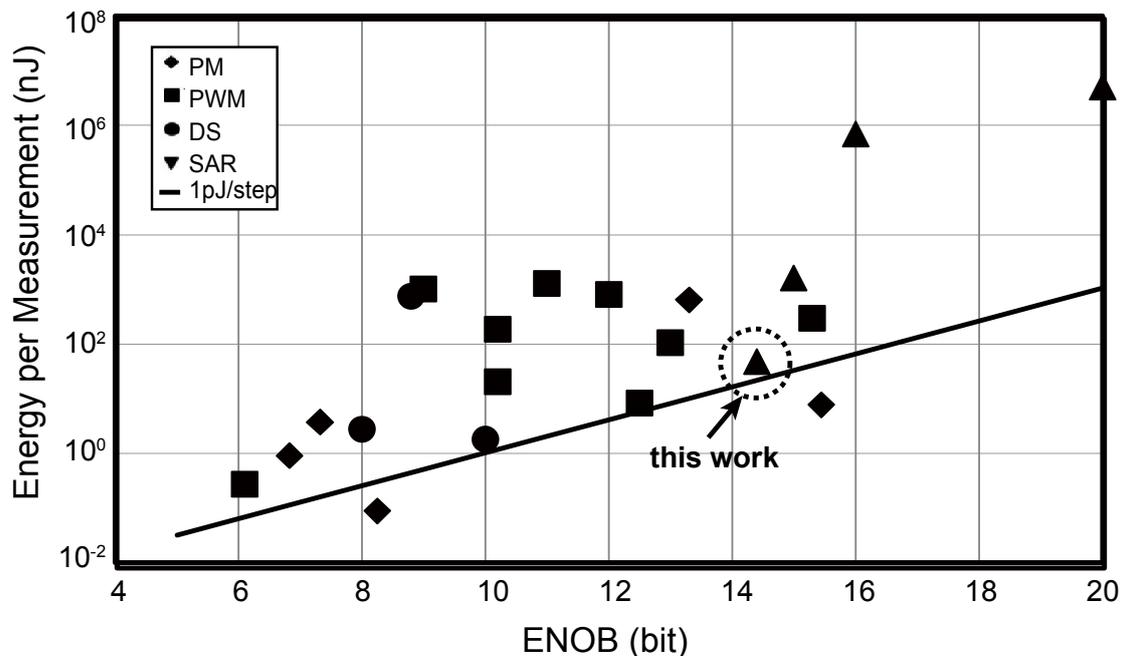


Fig 5-1: Survey of energy consumption per measurement for various types of

interfaces according to [1]

With this result, we successfully demonstrate that:

- **An inverter-based OTA and comparator are feasible for capacitive-sensor interfaces based on PM.**

The CMOS inverter is getting more and more used in analog circuits, due to its low-voltage operation and high current-efficiency. In this thesis, an inverter-based OTA and comparator are employed to improve the energy-efficiency, compared with the prior capacitive sensor interfaces based on PM [1-3].

- **The dual-integration-capacitor scheme is a valid method to improve the resolution of the interface.**

In this thesis, the dual-integration-capacitor scheme strongly reduces the noise of the OTA and comparator, improving the resolution of the interface. This scheme may be applicable to reduce noise in other relaxation oscillators.

- **The discrete-time feedback loop is feasible for handling sensor capacitances larger than the on-chip capacitors of the interface.**

The discrete-time feedback loop makes the interface capable of handling large sensor capacitance without increasing the die size. It avoids the stability issues associated with the continuous-time feedback loop applied in previous work [1,3] and is not limited by the parasitic capacitors associated with the sensor. Moreover, the Schmitt-trigger logic gates employed in the loop instead of feedback OTAs increase the energy-efficiency of the interface a step further.

- **The integration current source with S&H circuit is suitable for low-noise circuit.**

The current source with S&H circuit isolates the noise from the bias circuit.

In this thesis, the sampling causes the noise of bias circuit to be stored on *sampling* capacitors and thus held constant during the measurement, allowing it to be compensated by the auto-calibration scheme. A similar solution can be applied to other auto-calibrated interfaces based on a relaxation oscillator.

5.2. Future Work

The inverter-based capacitive interface based on PM can be further improved. A summary of several potential improvements is provided below.

- This thesis presents an inverter-based OTA and comparator, which are sensitive to the noise from power supply. In a practical application, an inverter-based OTA and comparator with better PSRR are needed.
- The integration current sources limit the lower supply voltage and the resolution of the interface. Therefore, a current source that is less noisy and applicable at lower supply voltages, can be studied in the future.
- A reproducibility problem was found during the linearity measurement, causing the reported results to be limited by instability of the setup rather than intrinsic non-linearity of the interface. A better measurement method can be studied in order to have a more reliable measurement setup for the linearity measurement.

References

- [1] Z. Tan, et al., "An Energy-Efficient 15-Bit Capacitive-Sensor Interface Based on Period Modulation," JSSC, vol. 47, no. 7, pp. 1703-1711, July 2012.
- [2] S. Heidary Shalmany, et al., "Noise Analysis for Period-Modulation-Based Capacitive Sensor Interfaces", in process
- [3] A. Heidary and G. C. M. Meijer "Features and Design Constraints for an Optimized SC Front-End Circuit for Capacitive Sensors with a Wide Dynamic Range", IEEE J. Solid-State Circuits, vol. 43, no. 7, pp.1609 -1616, 2008