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Tang, Zhong; Zamparette, Roger; Furuta, Yoshikazu ; Nezuka, Tomohiro; Makinwa, Kofi A.A.

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3.5 A ±25A Versatile Shunt-Based Current Sensor with 10kHz Bandwidth and ±0.25% Gain Error from −40°C to 85°C Using 2-Current Calibration

Zhong Tang[1], Roger Zamparette[1], Yoshikazu Furuta[2], Tomohiro Nezuka[2], Kofi A. A. Makinwa[1]

[1]Delft University of Technology, Delft, The Netherlands
[2]MIRISE Technologies, Aichi, Japan

Accurate current sensing is critical in many industrial applications, such as battery management and motor control. Precise shunt-based current sensors have been reported with gain errors of less than 1% over the industrial temperature range (–40°C to 85°C) [1-4]. However, since they are intended for coulomb counting, their bandwidth is limited to a few tens of Hz, making them unsuitable for battery impedance or motor-current sensing. This paper presents a current sensor with a wide (10kHz) bandwidth and a tunable temperature compensation scheme (TCS), which allows it to be flexibly used with different types of shunts while maintaining high accuracy. A low-cost room-temperature calibration scheme is proposed to optimize gain flatness over temperature by exploiting the shunt's self-heating at large currents. Over the industrial temperature range and a ±25A current range, it achieves state-of-the-art gain error (±0.25%) with both low-cost PCB and stable metal-alloy shunts.

A block diagram of the proposed current sensor is shown in Fig. 3.5.1. It digitizes the voltage V_S across a shunt connected between the load and ground. The shunt may be realized as a low-cost PCB trace, whose large temperature coefficient (TC, ~0.4%/K) must then be compensated to mitigate errors due to ambient temperature drift and self-heating. Higher accuracy can be achieved by using low-TC metal-alloy shunts, but this comes at the expense of cost. To be compatible with both types of shunts, the proposed sensor employs an ADC with a reference voltage V_{REF} whose TC can be tuned to match that of the shunt. As a result, the output of the ADC D_{OUT} is temperature-independent and does not require further processing [3]. V_{REF} is generated by combining a PTAT voltage V_{PTAT} with an attenuated CTAT voltage $V_{CTAT}/\alpha \pm V_{CTAT}/\lambda$, where λ (>80) is used for fine-tuning and α (=10) provides the attenuation needed to realize the reverse-bandgap voltage required by a low TC shunt. As in [3], an NPN-based reference generator is used to generate V_{PTAT} (ΔV_{BE}) and V_{CTAT} (V_{BE}).

Figure 3.5.2 shows a single-ended block diagram of the proposed readout circuit. Since V_S voltage is small ($|V_S| < 50mV$), it is boosted by a capacitively-coupled amplifier (CCA), which also serves as the summing node of a 1-bit 2nd-order switched-capacitor (SC) ΔΣ modulator. The CCA's gain (10×) suppresses the offset and kT/C noise of the modulator's 1st integrator, allowing the use of small sampling capacitors. To efficiently implement the large attenuation λ, the 1-bit feedback $\pm V_{REF}$ is applied via two feedback paths. Its PTAT component (ΔV_{BE}) is applied via the CCA, while its CTAT components (V_{BE}/α and V_{BE}/λ) are applied via the 1st integrator. Thus, both attenuations are realized by reasonable capacitor ratios: λ (= $C_{IN}/C_{FB}\times C_1/C_2$) and α (=$C_{IN}/C_{FB}\times C_1/C_3$), where $C_{IN} = 10C_{FB} = 500fF$, $C_1 = C_3 = 8C_2 = 400fF$. Since the capacitors are rather small, λ is trimmed in a ΔΣ fashion, rather than by using a multi-element DAC [2]. To avoid quantization noise folding, λ is implemented by two separate 1st-order ΔΣ modulators clocked in a bitstream-controlled (BSC) manner [6]. In this way, the CTAT component V_{BE}/λ can be trimmed with 8-bit resolution over a ±9mV range, corresponding to TC steps of ~1.6 and 10ppm/°C for the low-TC and PCB shunts, respectively.

To mitigate its offset and 1/f noise, the CCA is chopped at f_S (=2.56MHz), while the 1st integrator employs a correlated-double-sampling (CDS) scheme. Switched resistors are used to realize the large DC feedback resistances (>100MΩ) needed to ensure that the CCA's highpass cut-off frequency is well below f_S. The CDS scheme also demodulates the CCA's output, thus rejecting its offset without the need for the ripple-reduction loop used in [5]. Residual offset is suppressed by system-level chopping (CHL, f_{CHL} =20kHz). However, the resulting transients will disturb the state of the modulator, causing significant errors. In this work, rather than resetting the modulator during each CHL transition [1-3], the position of the integration capacitors is periodically swapped, thus preserving modulator state and enabling free-running operation [6]. To compensate for the loop filter's delay, the clock of the output chopper is delayed by one ΔΣ clock period.

The CCA is based on a 2-stage Miller-compensated amplifier, which consists of a folded-cascode input stage and a Class-AB output stage. Drawing ~180μA, it provides >100dB DC gain and rail-to-rail output swing. The SC integrators are based on current-reuse OTAs. For diagnostic purposes, an on-chip temperature sensor is implemented to monitor the self-heating of the shunt at large currents. This consists of a separate 1st-order SC ΔΣ modulator that balances $11\cdot\Delta V_{BE}$ against V_{BE} to generate a digital representation of temperature [6].

The sensor was implemented in a standard 0.18μm CMOS technology. Including the reference generator and current-sensing ADC, it occupies 0.36mm² (Fig. 3.5.7, right) and draws 265μA from a 1.8V supply. For flexibility, the sinc² decimation filter and BSC ΔΣ trimming logic are implemented off-chip. The sensor's performance was verified with 1.6mΩ PCB (36mm×5mm), and 2mΩ low-TC (75ppm/°C) shunts (Fig. 3.5.7, left). Good thermal coupling and galvanic isolation were achieved by directly bonding the chip to the shunt with non-conductive glue.

Figure 3.5.3 (top) shows the measured output spectra of the modulator. Trimming V_{REF} with a free-running digital ΔΣ modulator incurs significant noise folding, which is eliminated by the BSC scheme. The modulator then achieves a thermal-noise-limited resolution of 8.5μVrms in a 10kHz bandwidth. With CHL disabled, measurements on 20 samples show that the sensor's offset is less than 50μV. This drops below 6μV with CHL enabled. Figure 3.5.3 (bottom) shows the D_{OUT} variations of the sensor measured from -40°C to 85°C with a 15A input. The BSC ΔΣ trimming scheme allows D_{OUT} variation to be trimmed with high resolution, in steps of ~0.1% and ~0.03% for the PCB and low-TC shunts, respectively. With an optimal λ, D_{OUT} variations can be reduced to less than ±0.1% over the industrial temperature range for both shunts.

With a PCB shunt and a 0-to-5A step, the sensor's output settles to within 0.2% in 300μs (Fig. 3.5.4, left). However, a 0-to-25A step causes significant self-heating and slow settling; a temperature rise of ~10°C was observed over a 14s interval. Due to the initially non-homogenous temperature distribution in the shunt, a peak settling error of 0.7% can be seen, which drops to 0.2% within ~6s (Fig. 3.5.4, right).

By exploiting the shunt's self-heating at large currents, the optimal λ for minimum D_{OUT} variation over temperature can then be determined by a low-cost 2-current calibration at room temperature. For example, currents of 10A and 25A will result in a significant temperature difference, ~20°C for the PCB shunt, resulting in a significant error in the expected gain of 2.5 before λ optimization. Due to the residual high-order TC of both the shunt and V_{REF}, the optimal λ then corresponds to a non-zero gain error, which is obtained by batch calibration. After determining the optimal λ, the 10A current is then used to trim the gain error due to the spread of the shunt's nominal resistance. Ten sensors were characterized for each type of shunt in a current range of ±25A from -40°C to 85°C. With an optimized, but fixed, value of λ (~177 (PCB shunt) and ~683 (low-TC shunt)) and a single-current-gain trim [2], gain errors of ±0.4% (PCB shunt) and ±0.3% (low-TC shunt) were achieved. The proposed 2-current calibration scheme reduces them to ±0.25% (PCB shunt) and ±0.2% (low-TC shunt) without further processing (Fig. 3.5.5). The spread on the resulting values of λ, which reflects the combined spread in the TC of the shunt and V_{REF}, is limited to 10 and 20 LSBs for the PCB and low-TC shunts, respectively.

The performance of the sensor is summarized in Fig. 3.5.6 and compared with state-of-the-art PCB and low-TC shunt-based sensors. The proposed sensor achieves the highest bandwidth with competitive power efficiency. For both types of shunts, thanks to the low-cost 2-current calibration scheme, it achieves state-of-the-art gain accuracy (±0.25%) over a wide current (±25A) and temperature (-40°C to 85°C) range.

Acknowledgment:
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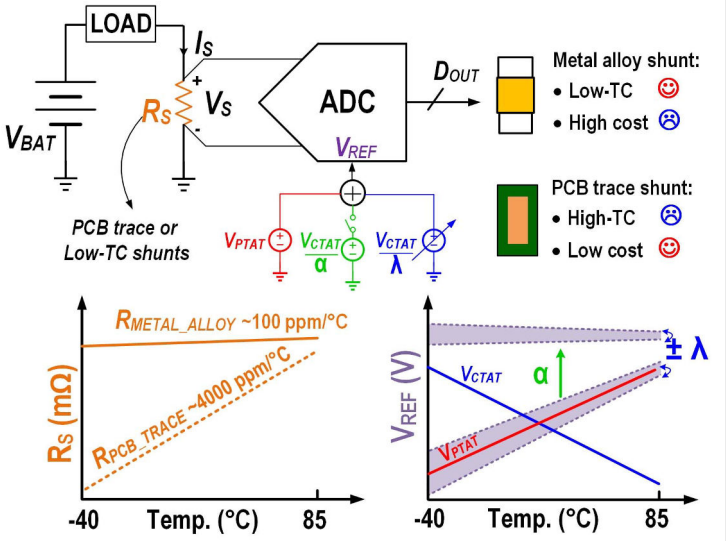

Figure 3.5.1: Block diagram of the proposed current sensor with Low-TC and PCB trace shunts.

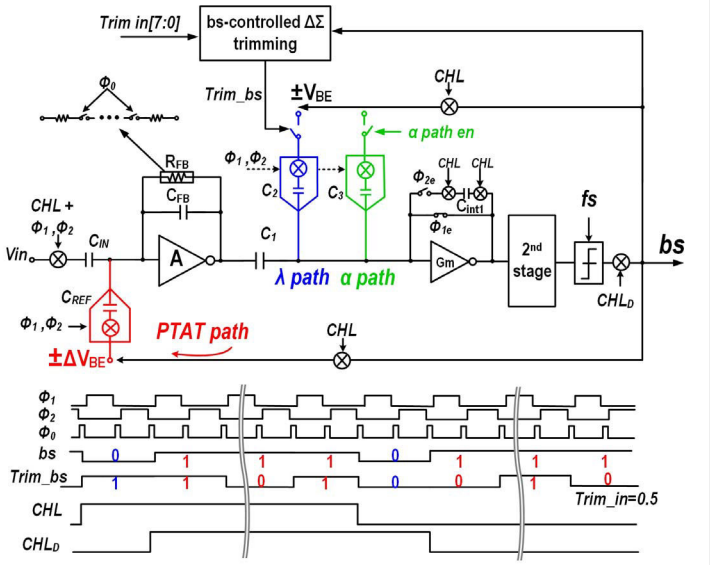

Figure 3.5.2: Simplified single-ended circuit diagram of the fully-differential current sensor and its timing diagram.

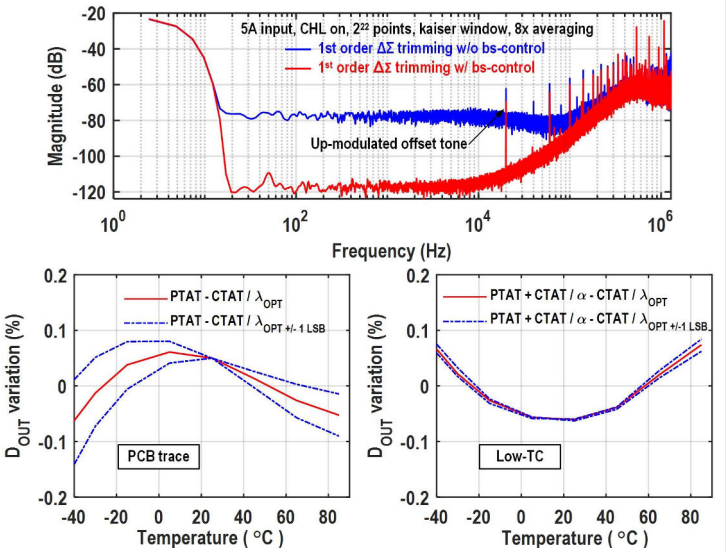

Figure 3.5.3: Measured output spectra w/ and w/o BSC ΔΣ trimming (top); measured D_{OUT} variations over temperature with a 15A current input (bottom).

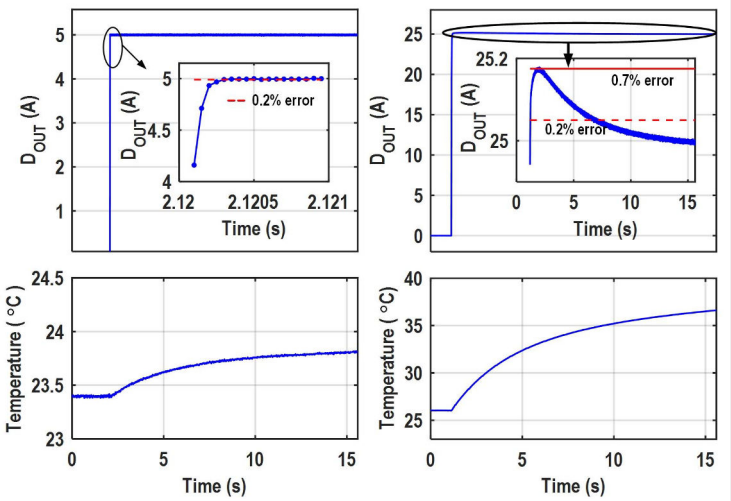

Figure 3.5.4: Transient measurements under 0 to 5A (left) and 0 to 25A (right, 16× averaging) current-step inputs with a PCB trace shunt.

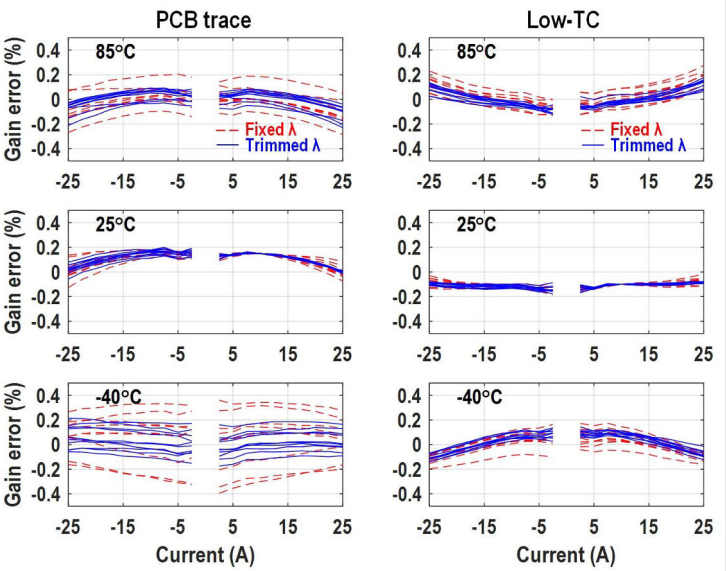

Figure 3.5.5: Measured gain errors at different ambient temperatures for PCB trace (left) and low-TC metal alloy shunt (right) w/ and w/o λ trimming.

	This work		Xu SSCL' 18 [1]	Zamparette VLSI' 21 [2]	Vroonhoven ISSCC' 20 [4]	INA 260
Tech. (μm)	0.18		0.18 BCD	0.18	0.18 BCD	/
Area (mm^2)	0.36		1.4	/	0.85	/
Shunt	1.6mΩ (PCB)	2mΩ (low-TC)	1mΩ (PCB)	3mΩ (PCB)	50mΩ (low-TC)	2mΩ (low-TC)
I Range	±25A	±25A	±12A	±15A	±1A	±15 A
Gain Error	±0.25%	±0.2%	±0.35%	±0.6%	±0.5%	±0.5%
Temp. Range	-40 to 85°C		-40 to 85°C	-40 to 85°C	-50 to 125°C	-40 to 85°C
ADC Offset	6μV		1μV	0.5μV	<5μV	10μV
Bandwidth	10kHz		40Hz	32Hz	<2.4Hz	<3.6kHz
ADC Resolution	8.5μV		1.1μV	5.4μV	/	/
Supply Voltage	1.8V		1.8V	1.8V	1.7-60V	2.7-5.5V
Supply Current	265μA		13.8μA	1.4μA	<5μA	310μA
Dynamic Range	73.5dB	75.4dB	80.7dB	78.4 dB	/	/
FoM*	147dB	149dB	143dB	149dB	/	/
Polynomial Calibration	No		Yes	Yes	No	/

* FoM=Dynamic Range +10log (Bandwidth/Power)

Figure 3.5.6: Performance summary and comparison table.

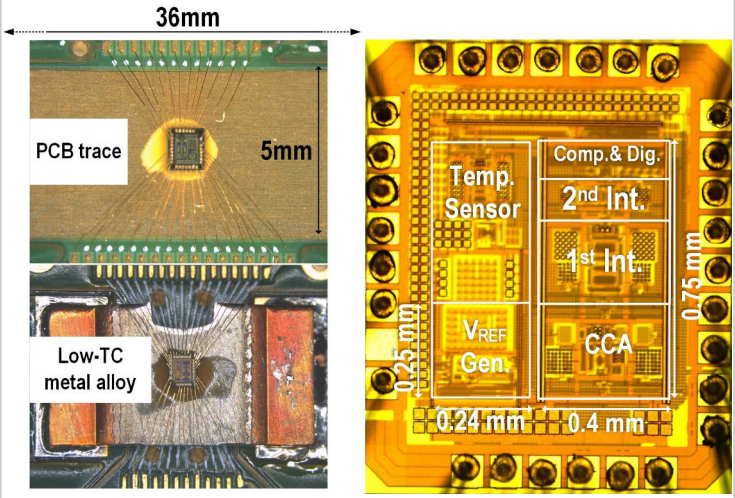

Figure 3.5.7: Chips on PCB and low-TC shunts; Die micrograph.

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