A Capacitive Fingerprint Sensor Front-End Circuit Design

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Challenge the future

A Capacitive Fingerprint Sensor Front-End Circuit Design

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ABSTRACT

This thesis describes the implementation of a capacitive fingerprint sensor readout circuit. Nowadays fingerprint sensors are becoming more and more popular as personal recognition device in smartphones and tablets. In order to be competitive on the market, an integrated fingerprint scanner should be as small and fast as possible.

In this thesis, the design of a new readout integrated circuit for a mutual capacitance fingerprint sensor is described. The proposed solution involves a Capacitive feedback Transimpedance Amplifier (CTIA), this stage aims to substitute an off-chip bandpass filter, while re-using the previous back end circuit. The circuit is designed in a standard 0.15 μm CMOS technology, the used supply voltage is 1.8 V. The readout architecture achieves an SNR of 25.2 dB in a measurement bandwidth of 50 kHz. The circuit can completely reject external common-mode interference as charger noise. This translates into a one-to-one comparison with the previous solution in terms of noise performances.

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1

INTRODUCTION

The advent of Smartphones and the advancement of technology makes it possible to store all of our Personal Identification Numbers (PIN's), mail messages and bank account credentials in a portable device. This allows us to access our contact information, and even transfer money, anywhere, anytime. The need for a reliable and personal recognition method integrated into cell phones is, therefore, a critical requirement for security and privacy issues. Biometrics or, in other words, the measure of the shape or composition of the human body [2], can solve this problem in a safe and efficient way. Fingerprint scanners, in particular, appear to be good solution as a person's fingerprints are unique and invariant during a lifetime [2].

Several touch sensing techniques are available in the literature [3], optical [4] , resistive [5], Surface Acoustic Wave (SAW) [6] and capacitive. The main parameters used to evaluate the quality of a touch sensor and to compare the different technologies are:

- The sensor's light transmittance, or, in other words, the transparency of the sensor. This directly influences the image of a display.
- The sensitivity of the sensor to external agents like water droplets, oil, dust or external light. In the case of a touch sensor, this is an undesired feature.
- The force required to detect a touch, i.e. how much the finger has to "push" on the sensor before a change is detected.
- The ability to detect more than one touch simultaneously (Multitouch)

When it comes to having an accurate, scalable, reliable and cheap solution that is also resistant to external contaminants, capacitive sensing gives the best results, as can be seen in Table 1.1.

Another emerging technology is ultrasonic sensing [7],which was introduced by Qualcomm in 2016 in a commercial fingerprint scanner for portable devices [8]. As the name suggests, this technique uses sound waves to penetrate the epidermis and create an image based on the reflected waves. The advantages of ultrasonic scanners come from the fact that no external chemical can influence the measurement making the system robust to spoofing attacks. Another advantage is the possibility of placing the sensor beneath the touched surface, since as the ultrasound can easily penetrate glass, plastic or aluminium, meaning that a dedicated area for the sensor is no longer needed. A possible disadvantage arises from the fact that the MEMS transducers have to be fabricated as a separate device, which must be subsequently bonded to a readout circuit.

In section 1.1, the operating principle of capacitive touch sensors will be explained. The basic characteristics of capacitive fingerprint readout circuits are presented in section 1.2. Finally, the objectives and thesis organization are presented in section 1.3 and 1.4, respectively.

Method	Linearity	Accuracy	Size Scalability	Optical Clarity	Damage Resistance	Force Required	Activated by	Multitouch
Infrared	*****	***	*****	*****	***	**	touch sun-light	yes (expensive)
Surface Acoustic Wave (S.A.W.)	****	****	**	***	*****	**	touch, water droplets dust	no
Surface Capacitance	**	**	**	*****	*****	**	finger	no
Resistive	****	****	****	**	*	****	any force	yes (expensive)
Projected Capacitance	*****	****	***	*****	*****	**	finger	yes

Table 1.1: Touch Sensing technique comparison [1]

1.1. CAPACITIVE TOUCH SENSORS

Capacitive touch sensors can be implemented in two different ways, by measuring surface capacitance changes, or by performing so-called projected capacitance measurements.

Surface capacitance devices consist of a uniform conductive layer coated with glass or plastic. The electrostatic field of the conductive layer is kept constant by applying a voltage at the four corners. When a touch occurs, an unbalance in the current flowing into the corners can be measured, this reveals the finger position. Figure 1.1 shows the operating principle of a surface capacitance sensor. However, the resolution of this type of sensor is not as good as that of projected capacitive sensors, due to its area the parasitic capacitance associated with the sensor makes it sensitive to external noise sources, and neither is it easily scalable since increasing the sensor's area increases its parasitic capacitance and makes it more sensitive to external interference. Therefore surface capacitance sensing is not a suitable technique for fingerprint sensors where many touch points are required in a very small area or in high-resolution touchscreen panels because of its noise performances.

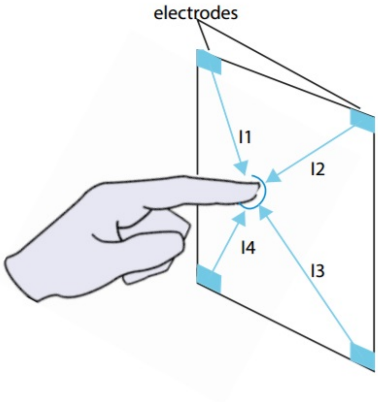

Figure 1.1: Surface Capacitance Sensing

As the name suggests, projected capacitive sensors measure changes in the projected electric field at an electrode. They represent the most common solution for touch screens and fingerprint sensors integrated into small portable devices such as tablets and smartphones. When a finger touch occurs, the reference capacitance of the sensor's changes as the finger "steals" some charges from it. Figure 1.2 illustrates this sensing technique.
Projected capacitive sensors can exploit self-capacitance sensing or mutual capacitance sensing. Some of the reasons why such a sensor technology is preferred are:

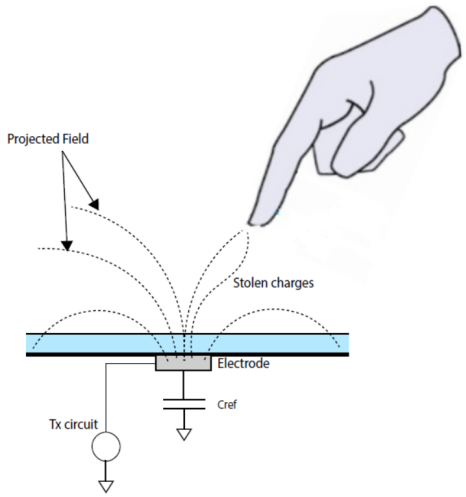

Figure 1.2: Projected Capacitance Sensing

- Cost: the sensor's electrodes can be made out of PCB traces.
- Plain glass or plastic covers can be used : the sensor gains in robustness and immunity towards chemicals.
- High accuracy.
- No moving part are involved.

An overview of the two different projected capacitance techniques follows in the next subsections.

1.1.1. SELF-CAPACITANCE SENSING

A self-capacitance sensor consists of separated electrodes built in a single layer of conductive material [9]. An electric field among the electrode and the grounds will develop if a voltage is applied. When touched, the fringing electric field above the sensor will be altered by the finger's presence, and this will increase the value of nearest electrode's capacitance. An example of such a sensor is shown in Figure 1.3

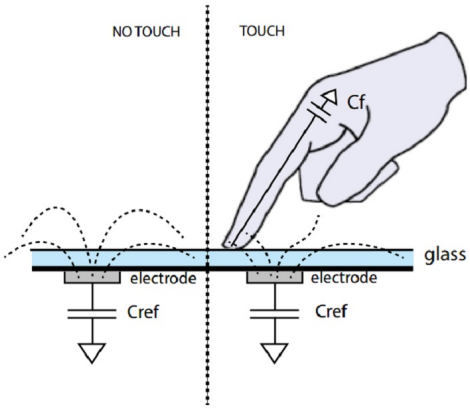

Figure 1.3: Self Capacitance Sensing

In self-capacitance sensors, every electrode is a touch point which can be connected to its own controller. The advantages of this sensing technique are a robust signal provided by a long-distance

field projection, and a simple readout circuit implementation. Disadvantages are a high area consumption, and a lower touch accuracy compared to mutual capacitance sensing [10].

1.1.2. MUTUAL CAPACITANCE SENSING

Mutual capacitance sensors are made of two separated conductive layers arranged as columns and rows (also called "Manhattan" fashion) or in a diamond pattern. If not disturbed, every intersection point between the two layers is able to hold charge [9]. When a finger touches the structure it absorbs some charges from the capacitor created at the intersection, thus decreasing the capacitance, this principle is illustrated in Figure 1.4.

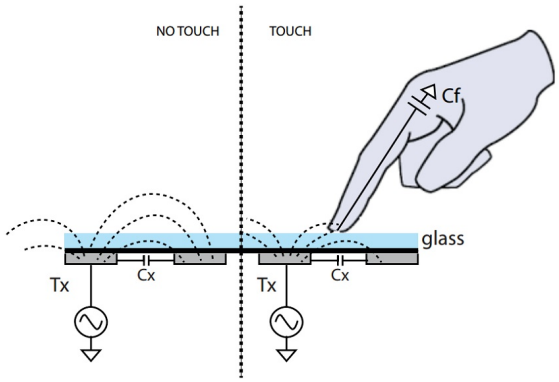

Figure 1.4: Mutual Capacitance Sensing

With respect to self-capacitance sensors, mutual capacitance sensing provide higher accuracy, and a better area efficiency at the cost of a more complex front-end circuit [10].

1.2. CAPACITIVE FINGERPRINT SCANNERS

A practical capacitive fingerprint scanner for portable devices application consist of a Capacitance-To-Digital Converter followed by a CPU or a microprocessor that is able to recreate the finger image. Such a device should, ideally, not occupy a large area, be as low power as possible, and give a clear picture of the finger in a few tens of milliseconds. Readout time, mainly driven by market, is critical. In many cases, the analog front-end circuit will need to scan all the sensor's electrodes in about 10mS.

The implementation of fingerprint sensor readout circuits presents some difficulties, a high resolution in terms of Dots Per Inch (DPI) must be achieved in order to be able to distinguish finger's ridges and valleys. In order to achieve this, a self or mutual capacitance sensor with at least a hundred of intersections in few mm^2 has to be used, resulting in a small reference capacitance value, and a tiny capacitive change to detect.

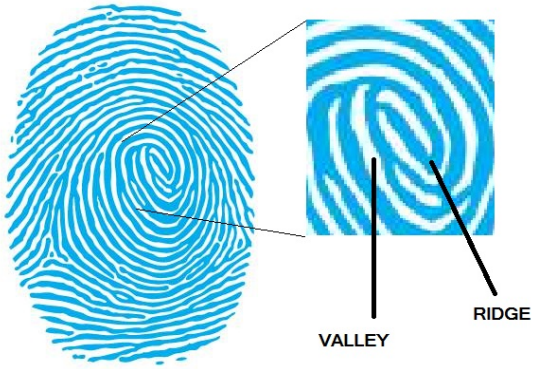

Figure 1.5: Ridges and Valleys

One of the biggest issues for fingerprint scanners is charger noise. Low-cost chargers lack proper noise suppression, therefore they create common-mode fluctuations in both the supply voltage and the ground reference. Since the disturbance is common-mode, i.e. the relative distance between the charger's supplies and the sensor stays constant, no noise is injected if no external touch occurs. When a finger makes contact with the phone, however, the touch sensor is connected to a capacitive path with a different reference ground. The finger touch will then inject noise exactly at the finger position[11]. Figure 1.6 gives an intuitive idea of the charger noise mechanism.

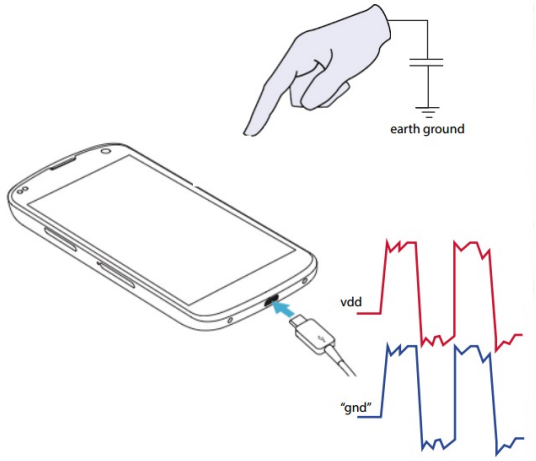

Figure 1.6: Charger Noise Principle

The voltage profile of this noise is characterized by very high magnitude peaks in a frequency range that goes from 1 kHz up to a few MHz. [12]

1.3. THESIS GOALS

In this thesis the development of an analog readout circuit for an existing mutual capacitance fingerprint sensor will be described. The starting point consists of a previously implemented lock-in amplifier preceded by an undesired off-chip passive band-pass filter. The new front-end should eliminate the need for the off-chip filter while re-using the previous back-end circuit, achieving similar performance. It should achieve at least 20 dB SNR for a minimum touch signal of 50aF in presence of a 2000x times larger parasitic capacitance at the input node. The challenges associated with this design comes from the need to detect a very small signal, which places stringent noise re-

quirements on the first stage. Lastly the proposed front-end circuit should be insensitive to external common-mode interference like charger noise.

1.4. THESIS ORGANIZATION

The thesis is organized in the following manner: chapter 2 introduces the sensor, the current implementation of its readout circuit, and the proposed changes. Chapter 3 describes the transistor level circuit implementation, while chapter 4 shows the relevant system level simulations and results. Finally, chapter 5 reports the conclusions and makes some recommendations for future work.

2

System Level Design

In the previous chapter, the background information, needed to understand capacitive touch sensing principles was given. The various sensing technique were then described, followed by a specification of the main requirements of capacitive fingerprint sensor.

This chapter starts, in in section 2.1, with a description of the capacitive fingerprint sensor used. This is followed in section 2.2, by a brief review of some possible fingerprint readout architectures. Next, an introduction to the current architecture, a comparison of possible new implementations, and the description of the proposed architecture will be presented in sections 2.3 and 2.4 respectively . Finally, system specifications will be calculated in section 2.7.

2.1. Sensor Description

The sensor used in this design consist of a 9x9 mm^2 mutual capacitance sensor, arranged in a Manhattan fashion, driven by a 9 MHz 5V peak to peak square wave. From the view point of the differen-

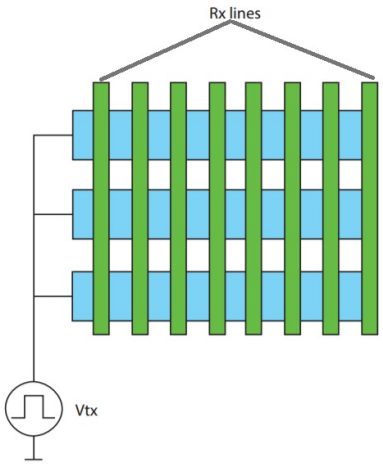

Figure 2.1: Manhattan fashion capacitive sensor

tial readout circuit, the equivalent model of the sensor is a capacitive wheatstone bridge, as shown in Figure 2.2. Here, Cref represent the reference capacitance, Csens the variable capacitance caused by the presence of a finger, and Cpar represents the sensor's parasitic capacitances. The presence of a ridge or a valley is sensed as a change in the mutual capacitance. The minimum change due to

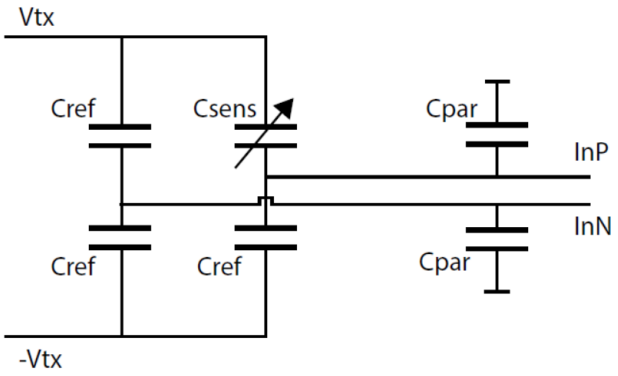

Figure 2.2: Sensor Equivalent Circuit

a finger touch is 50aF. The signal current associated with a capacitive change, considering a square wave with a finite rise time, can be expressed as :

$$\Delta I_{sensor} = \Delta C \frac{\partial V_{TX}}{\partial t} \tag{2.1}$$

where ΔC is the capacitance to sense, and V_{TX} is the sensor driving voltage. Assuming a 50aF capacitive change, a rise time of 10nS and a transmission voltage Vtx equal to 5, the resulting short-circuit current rms value is around 8nA.

All the sensor's electrodes are connected to a single receiver (Rx) via a multiplexer which selects the electrode to read in a round-robin fashion. The multiplexer's on-resistance is less than 150 Ohms. Every Rx line has its own ESD protection diode, arranged in such a way that the signal coming from the sensor is always within a diode drop of the ground voltage.

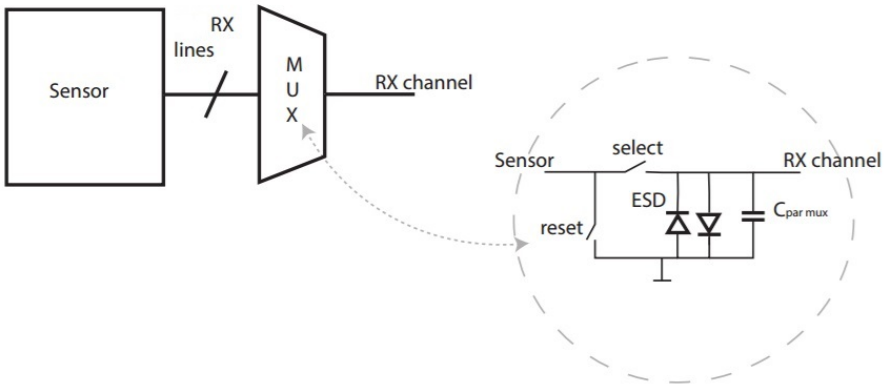

Figure 2.3: Multiplexer and ESD diodes electrical model

The multiplexer drastically reduces the silicon area required by the receiver channel; however, its use causes two serious problems. The first is associated with timing, since the electrodes are scanned sequentially, and the whole sensor must be scanned in less than 10ms, every node has to be scanned quickly. Secondly, the input node will be affected by a large parasitic capacitance due to the ESD protection diodes and the routing of the connections to all the electrodes. The total parasitic capacitance at the input node (including the sensor's parasitics) is in the order of 12pF,

which is 240000x larger than the minimum detectable capacitance change. Since this new design represents the first step towards a multi-channel solution i.e. a solution that involves more than one receiver channel, only 2.5 pF parasitic capacitance is considered.

2.2. LITERATURE REVIEW

Regarding the choice of the architecture to implement,there are two main possibilities:

1. implement a completely new architecture,
2. modify the current implementation.

In order to take a decision, a literature study is needed.

There are already many different readout architectures suitable for fingerprint sensing, in this section, 3 examples are described: an extremely compact multi-channel solution, an interesting combination of self and mutual capacitance sensing, and lastly a very high-resolution capacitance-to-digital converter, based on a lock-in amplifier will be introduced.

2.2.1. "A CMOS INTEGRATED CAPACITIVE FINGERPRINT SENSOR WITH 32B MICROCONTROLLER" [13]

The readout proposed in [13] consists of a 162x192 pixel array composed of a detection circuit and a 32-bit microcontroller. The front-end is used to boost the signal, convert it with a comparator and then send the data to a microcontroller for further processing. The pixel cell is showed in Figure 2.4 During pre-charge mode, the amplifier (SA) is in unity gain configuration and both the output node

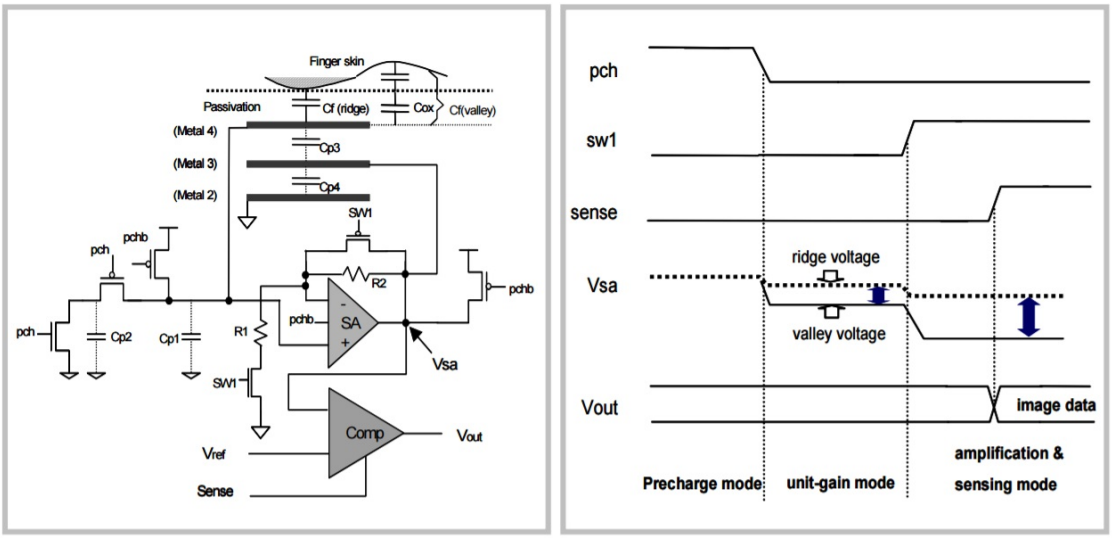

Figure 2.4: Pixel cell and timing diagram [13]

Vsa, and the positive input terminal of the amplifier are shorted to the reference voltage, while the parasitic metal capacitors Cp3 and Cp4 are charged to Vref. Since SA has unity gain configuration, the voltage drop across the parasitic capacitor Cp3 becomes approximately 0, thus its effect on the signal transfer function is drastically reduced. When signal Pch turns off, and a ridge or valley touch occurs, the input voltage of SA will decrease due to charge sharing at the input node, and will be

subsequently amplified when sw1 is opened. With this approach 423dpi (dot per inches) of resolution can be achieved in a $10x10mm^2$ sensor area. This kind of architecture gives a compact and fast solution, able to scan all the electrodes in 1.5mS, but lacks insensitivity to external interference, and the recognition algorithm requires 2 S to get a clear fingerprint image. On top of that, it involves a non-standard fabrication process because it exposes the grounded upper metal directly to the passivation layer.

2.2.2. "A 1 MM PITCH 80 × 80 CHANNEL 322 HZ FRAME-RATE MULTITOUCH DISTRIBUTION SENSOR WITH TWO-STEP DUAL-MODE CAPACITANCE SCAN" [14]

In this paper, a high-resolution touch screen is presented. As Figure 2.5 shows, the readout circuit uses a two-step dual mode capacitance scan to speed up the conversion time. Self-Capacitance sensing circuit, named "Self-Cs" in Figure 2.5, first scans all the sensor's electrodes and potential touch regions are detected. Mutual capacitance sensing of these regions then follows. As can be seen in picture 2.5, both the mutual-capacitance and the self-capacitance sensing are performed by exploiting a single slope ADC followed by a counter clocked at 100MHz. Mutual-Capacitance sensing shows performances close to the requirements of a fingerprint sensor readout. It consists of a capacitive feedback transimpedance amplifier that amplifies the tiny signal coming out of the sensor and an integrator to create a signal-dependent slope at the input of the comparator. The driving square wave frequency is 400 KHz. The system can detect 50 fF capacitive change, with 41dB SNR. The chopper around the integrator suppresses low frequency disturbances like flicker

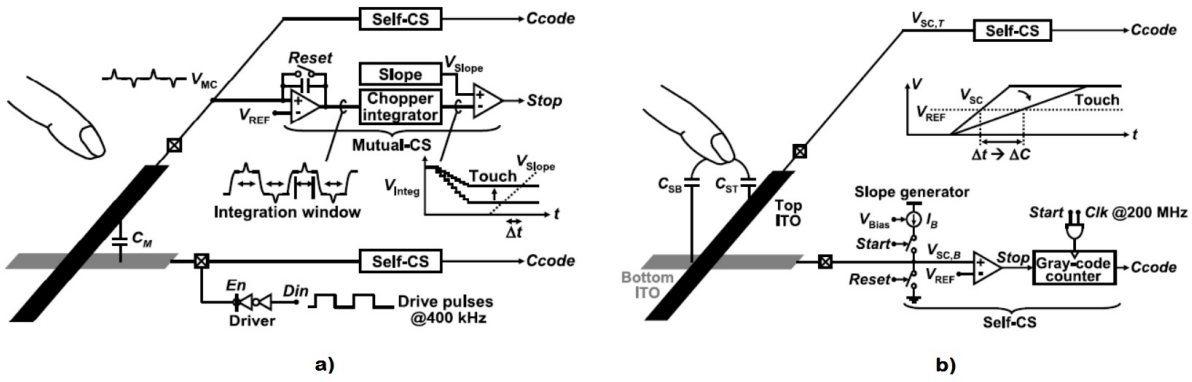

Figure 2.5: a)Mutual-capacitance sensing (Mutual-CS) and b) Self-capacitance sensing (Self-CS) pixels [14]

noise, offset and display noise up to 400kHz. The relatively low 400kHz driving frequency, combined with the single ended readout make this architecture susceptible to high frequency interference, like charger noise.

2.2.3. "MULTICHANNEL 65 ZF RMS RESOLUTION CMOS MONOLITHIC CAPACITIVE SENSOR FOR COUNTING SINGLE MICROMETER-SIZED AIRBORNE PARTICLES ON CHIP" [15]

In the presented paper [15], a sub aF resolution is achieved with a lock-in amplifier structure. The Rx channel consists of a capacitive divider driven by a square wave, amplified by low noise amplifier, modulated in baseband, and subsequently filtered. High-resolution is achieved by using a 40Hz readout bandwidth. However, the resulting long conversion time (20mS per channel), and thus the high energy consumption per conversion, exclude this architecture for use in portable applications.

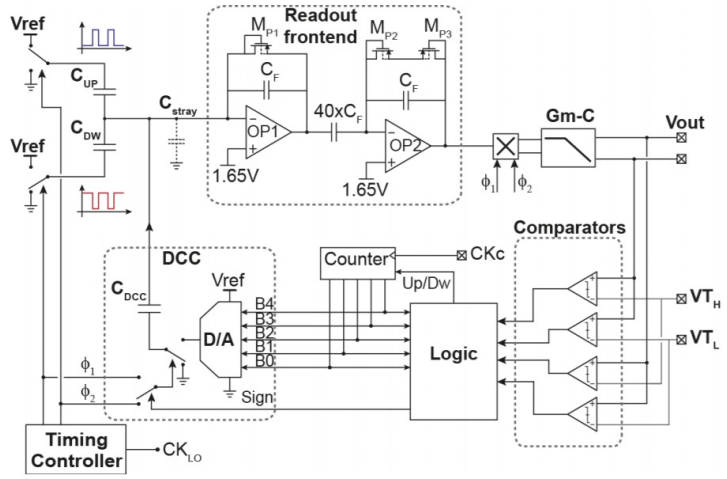

Figure 2.6: Implemented RX channel in [15]

2.3. PREVIOUS ARCHITECTURE

As mentioned in the previous chapter, an existing structure based on a lock-in amplifier has been already implemented. From the literature review, this approach can indeed achieve high resolution sensing [15] [17]. In view of this, this architecture has been chosen as a starting point.

The previous architecture consists of a fully differential AC coupled lock-in amplifier preceded by a passive bandpass filter. This solution achieves 26 dB SNR with a scan time of 25μs per electrode.

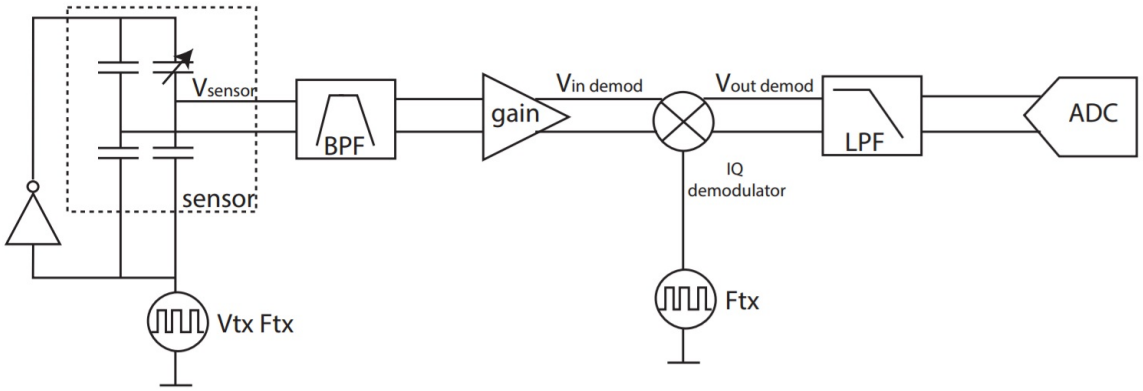

Figure 2.7: Block diagram old architecture

A fully differential structure is preferred because of its inherent rejection of common-mode interference. The signal is modulated with a 9 MHz square wave. The current coming out of the sensor is transformed into a voltage by the bandpass filter. The addition of the bandpass filter has the following benefits:

- It uses the 12pF parasitic capacitance at the input node as part of the filter.
- Because it's made by passive components, it has a very low noise figure.
- When it is followed by an open loop amplifier, it relaxes the noise requirements on the first stage with respect to a feedback configuration.

- It filters out charger noise and other low-frequency interferences.

On the other hand, a passive bandpass filter involves the use of rather big components such as inductors and capacitors. This makes it difficult to integrate such a circuit on-chip. Off-chip integration of these component has its own disadvantages:

- Off-chip components increase the overall height of the system.
- Inductance and capacitance changes with frequency, temperature, and process. To correct for these variations in the resonance frequency, the front-end requires more electronics and trimming.
- Off-chip components are expensive,their cost can contribute up to 10% the chip cost.

While a passive bandpass filter is desirable because of its energy efficiency and low noise figure, it requires expensive off-chip components. In this work, a new sensor front-end will be investigated, but still using the current lock-in amplifier as a back-end. A brief explanation of the architecture and its working principles is presented in the following subsection

2.3.1. LOCK-IN AMPLIFIER PRINCIPLES

As showed in Figure 2.8, a lock-in amplifier consists of an amplifier that increases the magnitude of a modulated signal, and a demodulator followed by a low pass filter. The combination of the latter two blocks is called a "coherent detector". A lock-in amplifier takes as input a narrow-band signal

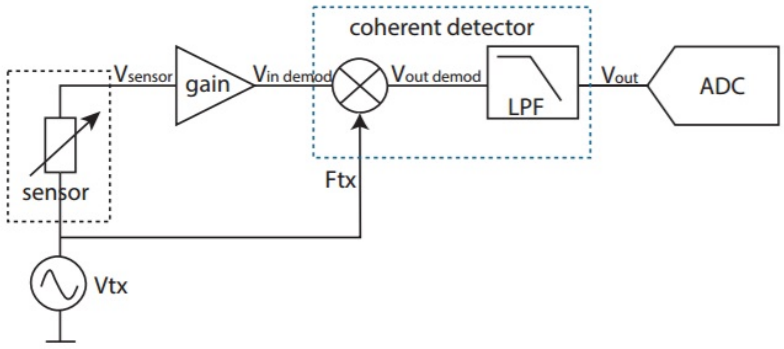

Figure 2.8: block diagram of a lock-in amplifier readout circuit

modulated with a known reference frequency carrier, and, after amplification, demodulates the signal back to baseband and filters it. This principle is shown, in the frequency domain, in Figure 2.9. The whole system performs like a bandpass filter centered at the modulation frequency. The enormous advantages are good rejection to low frequency interferences like offset, flicker noise, and, in touch sensing applications, charger noise, while at the same time having a narrow bandwidth measurement. On top of that, it has a better tolerance for mismatch and process variations than the use of high-Q resonators.

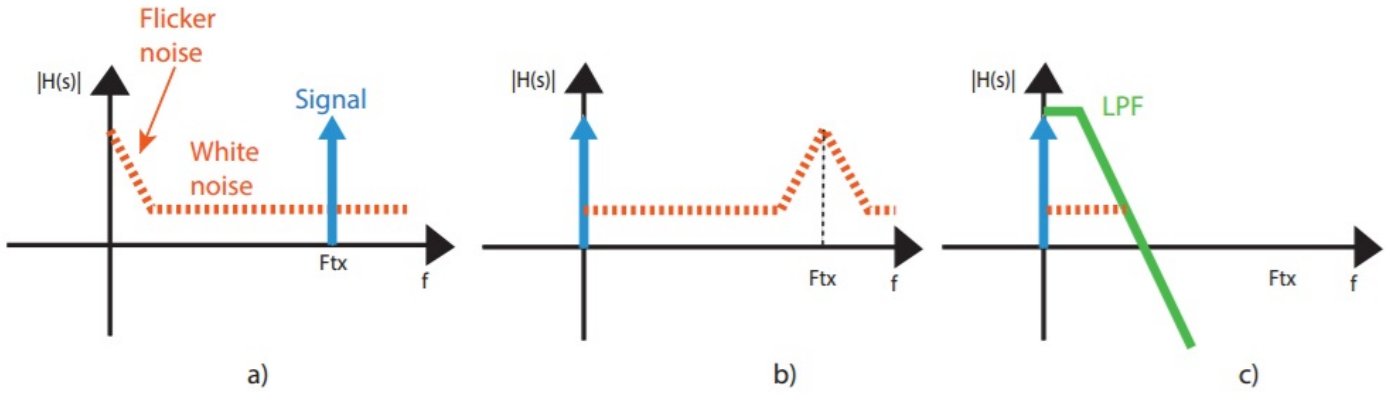

Figure 2.9: Synchronous demodulator principle, a) input of the coherent detector, b) output of the mixer, c) coherent detector's output

From a time domain perspective, the operation takes advantage of the orthogonality of two sinusoidal functions. The output signal can easily be expressed by basic goniometric relations for the case where modulation and demodulation are done with sine wave. We can express the signal at the output of the mixer as:

$$V_{outdemod} = V_{indemod}\cos(\omega t) * \cos(\omega t) = \frac{V_{indemod}}{2} * \cos(\omega t \pm \omega t) = \frac{V_{indemod}}{2} + \frac{\cos(2\omega t)}{2}, \quad (2.2)$$

where $V_{outdemod}$ is the output of the mixer, $V_{indemod}$ the voltage at the input of the mixer. The signal V_{out} at the coherent detector output can be approximated as:

$$V_{out} = \frac{V_{indemod}}{2}. \quad (2.3)$$

Since sine wave reference generators are not easy to implement, a square wave reference is often preferred. The Fourier series of square wave given by:

$$V_{square} = A_{in}\frac{4}{\pi}\left[\sum_{n=0}^{\infty}\frac{\cos((2n+1)\omega t)}{2n+1}\right], \quad (2.4)$$

hence, for the square wave we also have to take into account the higher order odd harmonics.
This has consequences on the noise modulation, in the worst-case, where we have to consider all the harmonics, the noise floor at the output of the coherent detector is increased by:

$$V_{nout}^2 = S_{nin}^2 * 2ENBW * \sum_{n=0}^{\infty}\left(\frac{1}{2n+1}\right)^2 = \frac{\pi^2}{8}S_{nin}^2 * 2ENBW, \quad (2.5)$$

where ENBW represents the equivalent noise bandwidth calculated in APPENDIX A, and S_{nin}^2 the noise power spectral density at the input of the coherent detector. The increase of noise is a factor $\frac{\pi^2}{8} = 0.9dB$ [18].

2.4. PROPOSED IMPLEMENTATION

By modeling the sensor as a voltage source in series with the capacitance to measure, it is clear that the output of such a sensor will be a current; therefore, an I-V conversion block has to be implemented. There are two different solutions as a replacement for the bandpass filter:

1. Open Loop Transimpedance Amplifier

2. Closed loop Capacitive Feedback Transimpedance Amplifier

The first proposal involves the linear amplification of the current coming from the sensor with a differential common-gate amplifier structure or a regulated cascode topology [16]. In order to suppress the input parasitic capacitance, the common-gate stage requires a big gm, thus a regulated cascode structure is preferred. Such a structure, however, has major drawbacks; it requires a fast common-gate stage in order to amplify the current pulses coming from the sensor. On top of that, there are no improvements in terms of SNR compared to the use of a feedback transimpedance amplifier, as the gm boosting amplifier connects directly to the input node and the resistors Rs and Rz contributes directly to the noise figure of the amplifier.

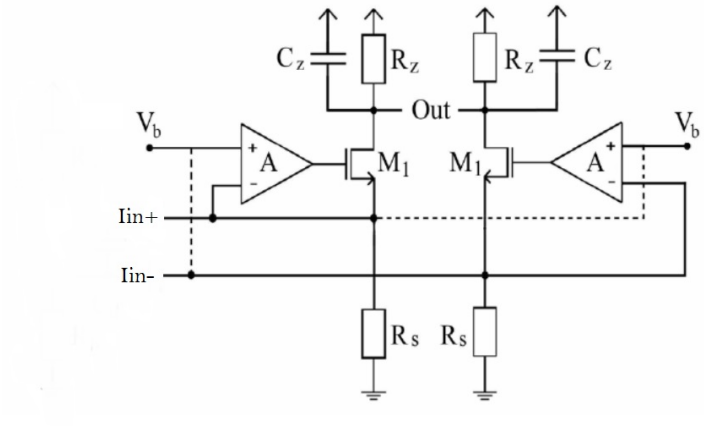

Figure 2.10: Differential Regulated Cascode [16]

The second proposal involves a capacitive feedback transimpedace amplifier (CTIA), see Figure 2.11). This configuration has all the benefit of feedback circuits: stable gain determined by the feedback, improved bandwidth, improved linearity and lastly, but not less important, it is a widely documented circuit that is easier to design. For these reasons, this topology has been chosen to replace the bandpass filter as front-end circuit for the sensor. Figure 2.12 points out the proposed

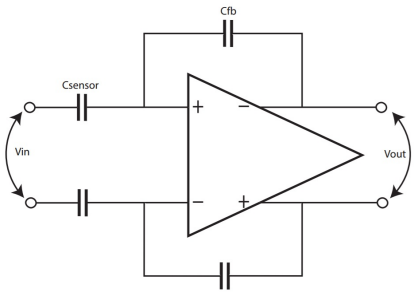

Figure 2.11: Capacitive feedback transimpedance amplifier

change for this design.

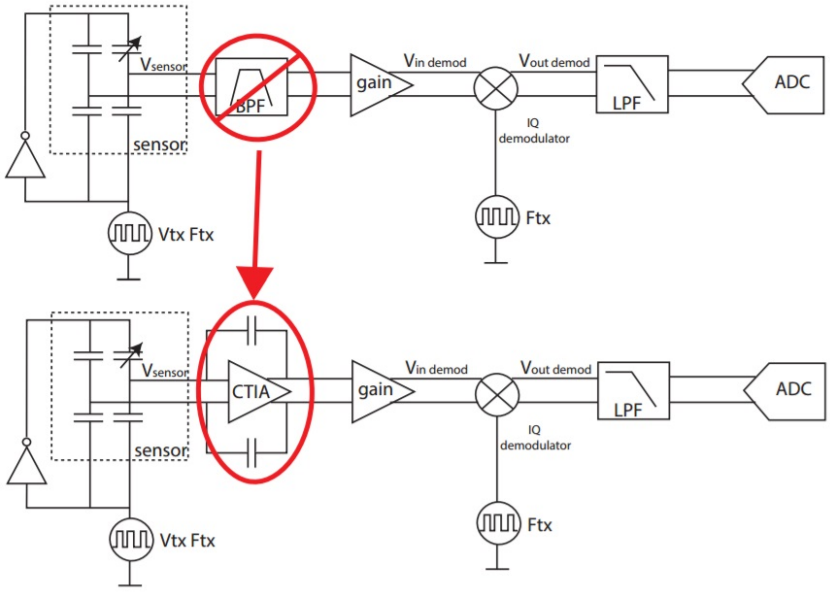

Figure 2.12: Difference between new proposal and previous architecture

2.5. SYSTEM LEVEL SPECIFICATIONS

As mentioned in chapter 1, the main goal of this project is to find an alternative for the input passive bandpass filter that is able to match the following main specifications :

- SNR > 20 dB,
- scan time of maximum 40 μS per electrode,
- output signal level equal or greater than 400 μV.

This specifications are derived from the actual implementation. Since the current solution has been already measured and tested, the back-end lock-in amplifier is fully characterized. The first step is to try to match the new proposal output to the back-end circuit, starting from the most important design goal: SNR.

2.5.1. SNR COMPARISON

For a 1-to-1 match between the previous architecture and the one proposed in this thesis, the ratio of the proposed architecture SNR over the previous architecture SNR is calculated. This ratio is evaluated at the input of the previous implementation amplification chain of the previous implementation. The characteristics to match are a signal level in the order of 400 μV, and the input referred noise coming from the second amplification stage, equal to 10 nV/$\sqrt{Hz}$, should not limit the noise figure.

As a first step, the system level of the previous architecture and the new proposal are calculated separately. The SNR achieved at the output of the bandpass filter is:

$$SNR_{existentarchitecture} = \frac{V_{tx}\Delta C \frac{4Q}{\pi C_{bpf}}}{V_{nbackend}\sqrt{2\frac{\pi^2}{8}ENBW_{current}}}, \tag{2.6}$$

where V_{tx} is the capacitive bridge driving voltage, ΔC the capacitive change to sense,C_{bpf} the filter capacitance, Q the quality factor of the bandpass filter,$V_{nbackend}$ the input referred noise of the backend circuitry, and ENBW the equivalent noise bandwidth determined by the coherent detector low pass filter cut-off frequency. The denominator of formula 2.7 represents the signal transfer function from Vtx to the input of the amplification stage, while the denominator is the calculated integrated noise. The performance of the actual front-end guarantees an SNR of 26 dB, which leaves 6 dB of margin with the respect of the design goal.

For the CTIA based front-end the simplified SNR formula is:

$$SNR_{newproposal} = \frac{\frac{V_{tx}\Delta C}{C_{fb}}}{\sqrt{(V^2_{nbackend} + V^2_{nCTIA}\left(\frac{C_p+C_{fb}}{C_{fb}}\right)^2)2\frac{\pi^2}{8}ENBW_{new}}}, \tag{2.7}$$

In this equation C_{fb} represents the CTIA's feedback capacitance,C_p the sum of all the parasitic

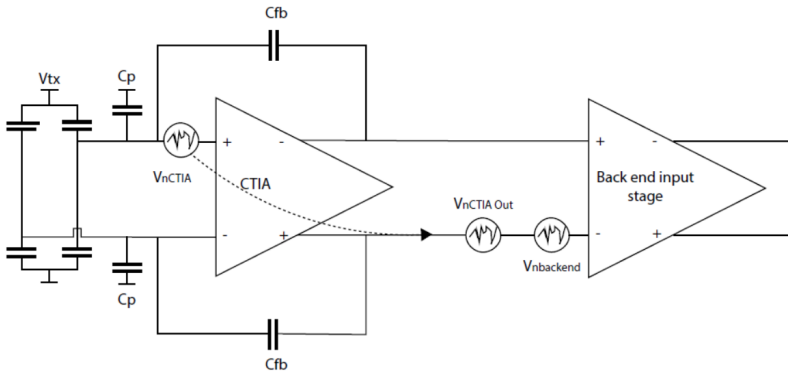

Figure 2.13: Noise Sources New Proposal, Noise is compared at the input of the back-end amplifier

capacitances at the CTIA's virtual ground plus 0.5pF of margin for the gate capacitance of the input pair, for a total of 3pF capacitance. V_{nCTIA} is the CTIA's OTA input referred noise. The sensor's reference capacitance is not included in this calculation as it is 1000x smaller than the parasitic capacitance
Combining equations 2.6 an 2.7 we get:

$$\frac{SNR_{newproposal}}{SNR_{currentarchitecture}} = \frac{C_{bpf}\pi}{4QC_{fb}} * \sqrt{\frac{ENBW_{current}}{ENBW_{new}}} * \frac{V_{nbackend}}{\sqrt{V^2_{nbackend} + V^2_{nCTIA}\left(\frac{C_p+C_{fb}}{C_{fb}}\right)^2}}, \tag{2.8}$$

This equation is divided into three fractions, the first fraction represents the ratio of the signal level between the existing architecture and the new one, the second represents the system bandwidth ratio, and the third the white noise level ratio. From this first calculation, it can be concluded that the main parameters to take into account are the CTIA's feedback capacitance, the system signal bandwidth, and the first gm stage input referred noise.

From equation 2.8, by keeping the required CTIA's input referred noise as an unknown, we note that the feedback capacitance value does not confer with an advantage in terms of SNR. The main benefit comes from the reduction of the coherent detector's low pass filter cut-off frequency, i.e., the system bandwidth. Decreasing the filter's cut-off frequency implies a longer scan time per electrode, but this is necessary to reduce the overall integrated noise, thus the requirement on the CTIA gm stage. To match timing requirements (a scan time lower than 40 μS per channel), the coherent detector cut-off frequency is chosen to be 50 kHz. The filter order is maintained to be 2, this will give us a linear factor 2.57 of improvement in the SNR.

2.5.2. FEEDBACK CAPACITANCE VALUE

Equation 2.8 shows that the feedback capacitance doesn't play a significant role in the SNR calculation, but it does for the signal amplification factor and the CTIA's gm stage bandwidth requirements. The simplified transfer function of the CTIA is derived:

$$V_{outCTIA} = V_{tx} \frac{\Delta C}{C_{fb} + \frac{C_p}{A_{OTA@Ftx}}}, \tag{2.9}$$

where $A_{OTA@Ftx}$ is the OTA's gain at the transmission frequency. This formula gives straightforward indication for the signal amplitude matching between the current architecture and the new proposal. The minimum signal level of $400\mu V$ is obtained with a feedback capacitance of 625fF, a smaller capacitance leads to a higher signal.

The feedback capacitance, together with the system-level bandwidth requirements defines the CTIA's gm stage bandwidth. Since the input signal is a square wave, some signal energy can be found at odd multiple harmonics with the respect of the transmission frequency. However, the signal decreases exponentially at these higher harmonics while the noise stays white. In order to estimate the suitable closed loop -3dB cut-off frequency, a simple Matlab simulation that takes into account the signal and noise transfer function of the CTIA, and the bandwidth of the second stage, has been performed.

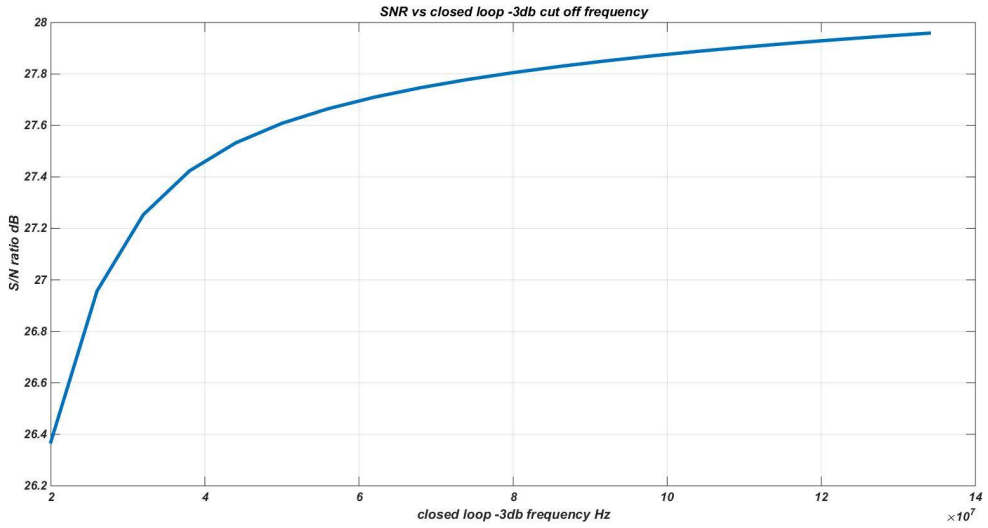

Figure 2.14: SNR as a function of closed loop -3db cut-off frequency

As can be seen from this graph, a higher bandwidth in the first stage will lead to a higher SNR, but the curve will saturate when the closed loop cut-off frequency is close to the seventh harmonic (63MHz). In this case, the following simplified equation to calculate the Gain-Bandwidth product (GBW) of the OTA holds:

$$GBW = f_{cl} \frac{C_p + C_{fb}}{C_{fb}}, \tag{2.10}$$

From this subsection, it can be concluded that a smaller feedback capacitance leads to a bigger, thus more robust, output signal, at the cost of increasing the bandwidth requirements for the first stage. The maximum value of capacitance that can be used is 650fF. However, in order to get a higher signal level, a feedback capacitance value of 500fF has been chosen, this results in a GBW requirement of 440 MHz and a $500\mu V_{pp}$ output square wave .

2.5.3. ELECTRONIC NOISE

The main noise contributor is the noise coming from the OTA. If the feedback capacitor value is set, we can obtain an estimation of the required input referred noise voltage of the OTA from equation 2.8. Imposing the SNR ratio equal to one and solving for V_{nCTIA} leads to:

$$V_{nCTIA} = \sqrt{\left(\frac{C_{bf}\pi}{4QC_{fb}}\right)^2 * \frac{ENBW_{existent}}{ENBW_{new}} - 1}\frac{C_p + C_{fb}}{C_{fb}} * V_{nbackend} = 3.24\frac{nV}{\sqrt{Hz}} \tag{2.11}$$

This value of input referred noise should give us a 1-to-1 comparison with the old system, which means at least 6 dB of margin in the SNR with the respect of the 20 dB SNR target.
The upper limit for the input referred noise can be calculated by solving equation 2.7 for V_{nCTIA} imposing an SNR of 20dB, in this case we have $V_{nCTIA} = 5.16\frac{nV}{\sqrt{Hz}}$

2.5.4. OTHER SPECIFICATIONS

Other useful information about the RX channel implementation are:

- The second amplification stage is AC coupled : no particular offset cancellation technique are needed.
- The supply voltage comes from a regulated reference: no stringent requirements on Power Supply Rejection Ratio.
- The sensor's outut signal is locked to ground: common-mode voltage of the input stage is required to be below 500mV.
- The output voltage swing of the CTIA ranges from 0.5mV to maximum 10 mV, for this reason, there are no requirements on slew rate on the first stage.
- An IQ demodulator is used in order to avoid phase shift problems; the output signal is calculated as $\sqrt{I^2_{channel} + Q^2_{channel}}$.
- The proposed new stage should draw less than 2mA of current.

2.6. SUMMARY

This chapter explains the necessary steps for deriving the system level specifications. First a detailed explanation of the used sensor and a brief overview of different possible implementations. A description of the actual front-end was given, followed by the new proposal and the derivation of the specifics.

The CTIA architecture is the best replacement for the off-chip bandpass filter as it adapts naturally to the sensor output, can guarantee good performances in terms of SNR, and does not involve drastic changes to the actual implementation. The main trade-off between the new architecture and the current one is the exchange of noise and power versus silicon area and cost.
In the next chapter, the circuit level design will be introduced.

3

ELECTRONICS DESIGN

In the previous chapter, the proposed architecture was explained, and the specifications for the input stage, a capacitive feedback transimpedance amplifier(CTIA) were derived. A summary of the calculated specifications for the CTIA is shown in Table 3.1.

Specification	***Value***
Input Referred Noise	$3.24\frac{nV}{\sqrt{Hz}} < V_{ninCTIA} < 5.16\frac{nV}{\sqrt{Hz}}$
GBW	>440 MHz
Offset	Not relevant, second stage AC coupled
Common mode input voltage	<0.5V
Output Swing	<10 mV
Slew Rate	Not relevant, small output swing
Technology	0.15μm triple well standard CMOS, 1.8V

Table 3.1: OTA specifications

In this chapter the transistor-level design of the CTIA will be discussed in detail. Figure 3.1 shows the top-level schematic of the CTIA, the implemented blocks are highlighted in the blue box. The design uses a 0.15 μm triple well CMOS technology, with a 1.8 V supply voltage.

The rest of this chapter will be organized as follows. Section 3.1 introduces the sensor on-chip replica, in section 3.2 the OTA core will be discussed, a self-biased μA block is presented in section 3.3, the Common-Mode Feedback circuit (CMFB), and the implementation of the feedback elements will follow in paragraphs 3.4 and 3.5 respectively. Section 3.6 will introduce the adopted reset scheme, while in section 3.7 the designed circuitry for testing the separate components of the circuit is reported. Section 3.8 will report the implemented layout.

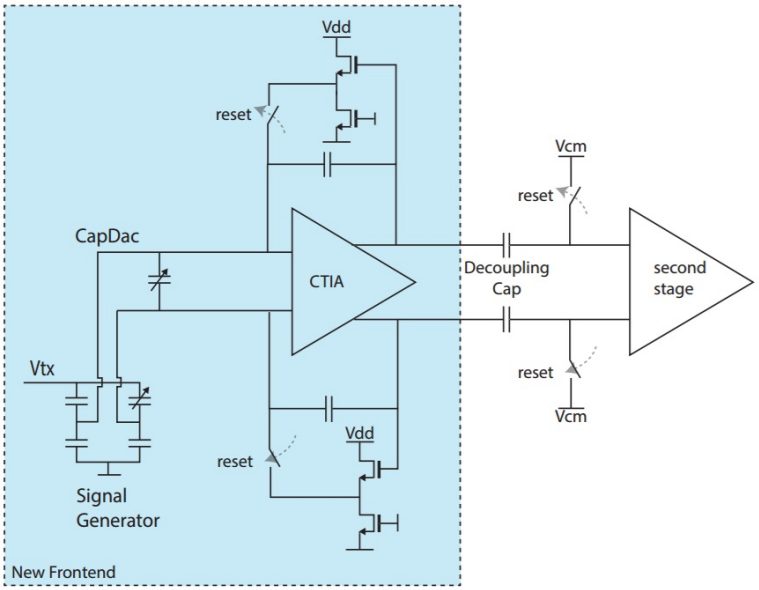

Figure 3.1: Input Stage Top Level Schematic

3.1. SENSOR ON-CHIP REPLICA

In the previous chapter, it was shown that the presence of parasitic capacitance at the input of the CTIA will degrade its noise performance. To minimize this, the sensor will be placed on top of the chip, and the two will be connected by bump bonding. This also results in a more compact solution. However, this is an expensive process, and so to test the functionality of the readout circuit, it was decided to create an on-chip sensor replica that emulates the expected capacitance changes and parasitics. The created solution consists of two blocks:

1. A programmable capacitive divider that acts as a signal generator Figure 3.2 shows the capacitive divider. This block recreates a 50aF signal by using 96fF unit capacitors. To avoid any mismatch in the parasitic between the two inputs, and to minimize the divider offset, a common centroid layout is used. This block can imitate a capacitive change ranging from approximately 60 aF up to 5fF, Vtx is a 9MHz 1.8V peak-to-peak square wave.

2. A 5-bit capdac that recreates the input parasitic capacitance associated with the sensor and the multiplexer. The capacitance range of the capdac goes from 128fF up to 4.7pF. The "nominal" value used is 2.5pF.

The Equivalent circuit for the combination of the capacitive divider with the capdac is showed in figure 3.4

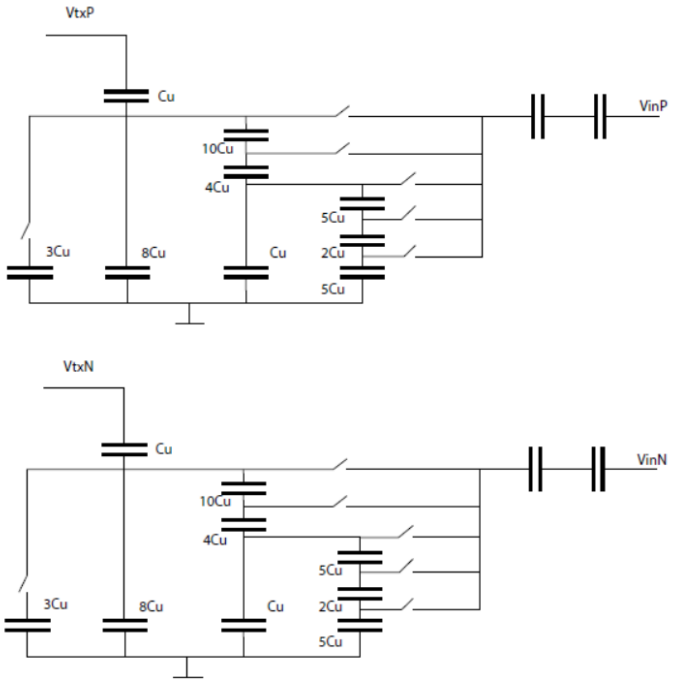

Figure 3.2: Capacitive divider

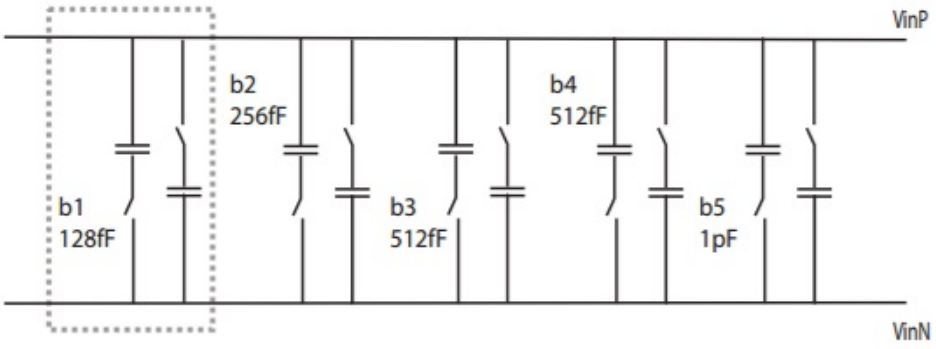

Figure 3.3: CapDac to recreate input parasitic capacitance

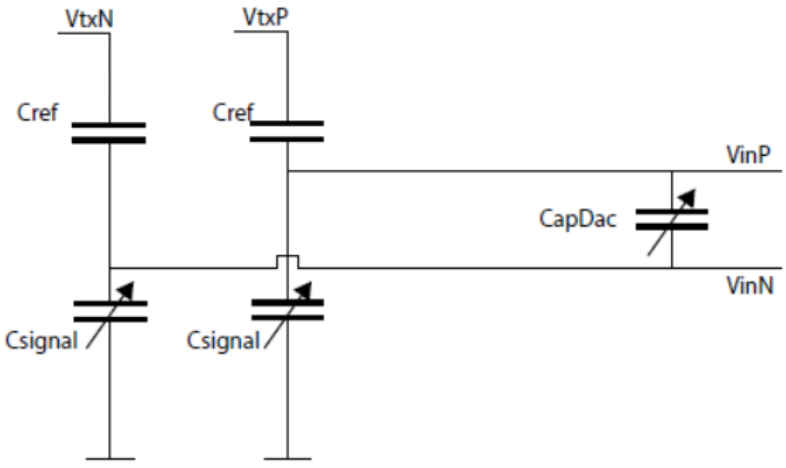

Figure 3.4: Equivalent Circuit for the Proposed Signal Generator and CapDac

3.2. OTA CORE

The designed transconductance amplifier consists of a Miller-compensated fully differential two-stage amplifier (figure 3.5). The choice of this topology is dictated by the need to minimize the noise contribution of the first amplification stage by using a resistive, rather than active, load. Single-stage amplifier topologies, like current re-use or telescopic cascode were considered. Despite their advantages in terms of bandwidth and the fact that they require no frequency compensation, their input common-mode voltage limitations, the high threshold voltages of the MOSFETs in the available technology (0.55V for low-vt pMOS devices)make such amplifiers complicated to design The

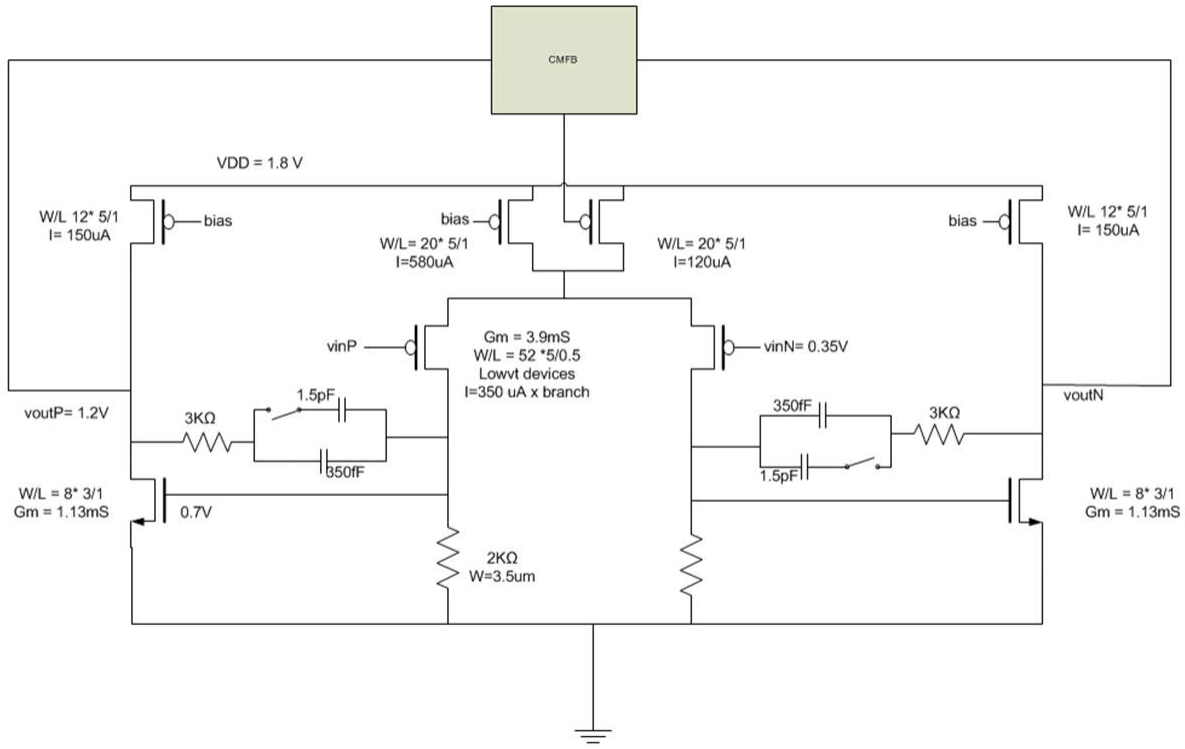

Figure 3.5: OTA schematic

first stage uses a resistive load, which means that its noise performance is set by the input pair. The input common-mode voltage is chosen to be the same as in the previous front-end amplifier, and thus is set to 0.35V. To support this input common-mode voltage and achieve a large gm, the input pair consists of low threshold pMOS devices. These were biased in a moderate inversion region to mitigate the size of their gate capacitance, which has a strong influence in the noise transfer function as it sums up with the parasitic capacitances at the input node. Compared to biasing in strong inversion, this results in better current efficiency. In order to achieve a matching of 1%, the load resistor's are quite wide: 3.5 μm. This value is supported by previous device characterization and measurements.

The second stage is a common-source nMOS input pair. This provides almost all the gain (36dB) and drives the feedback capacitance and the next stage. The output common-mode voltage is regulated by modifying 16% of the first stage's tail current. As the Miller capacitance is relatively small compared to the total CTIA area, Miller compensation is preferred over feed-forward compensation in order to save some power. Due to the wider bandwidth requirements during the scan phase, when

the amplifier doesn't need to be unity gain stable, the Miller compensation capacitor has different values for the reset and the scan phase. The Miller capacitor is chosen to be 350fF, which still gives an 80-degree phase margin over corners, as shown in Figure 3.6.

During the reset phase, however, the OTA is switched to a unity-gain configuration, where the Miller capacitor is increased to 1.85pF. Reset phase and stability concerns will be better explained in section 3.5. A nulling resistor larger than 1/gm2 is used to mitigate the amplifier's non-dominant pole.

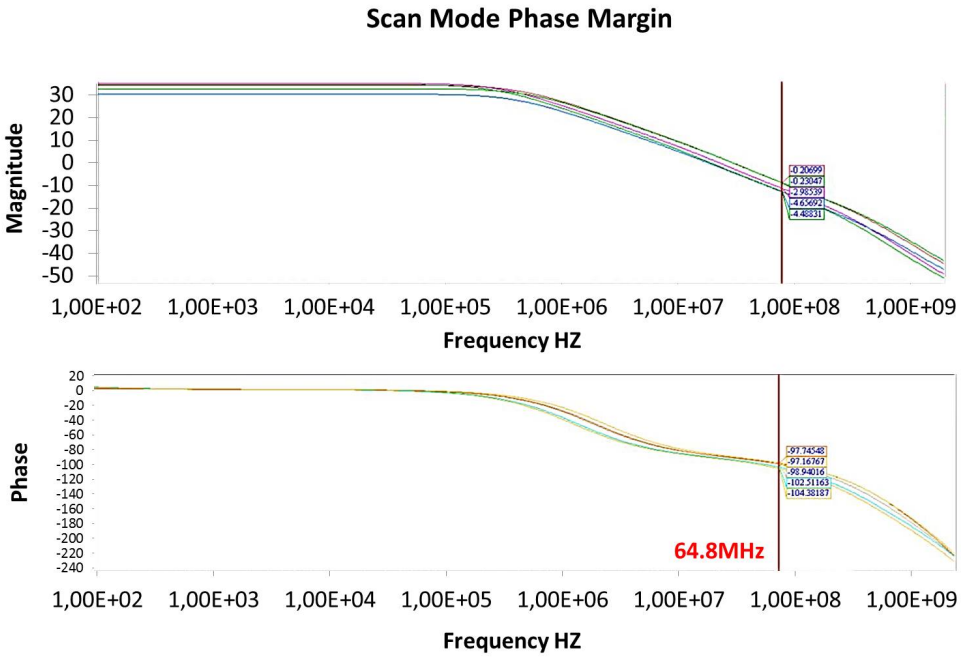

Figure 3.6: Phase Margin in Scan operating mode over corners

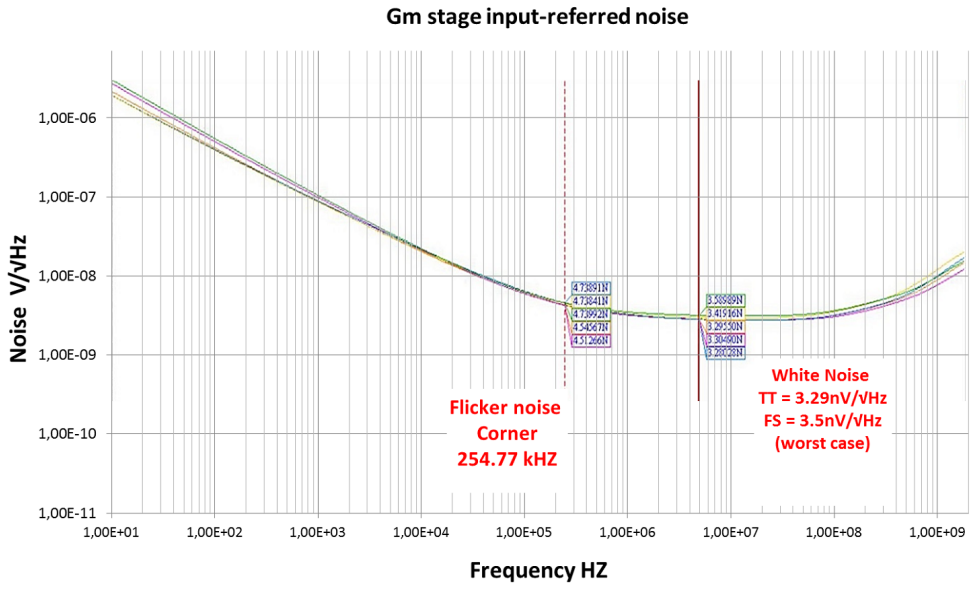

Figure 3.7: Input Referred Noise OTA

Simulations (Figure 3.7) shows an input-referred noise of 3.3 $\frac{nV}{\sqrt{Hz}}$ in the typical-typical corner

with a flicker noise knee frequency of 260 kHz.

3.3. BIASING CIRCUIT

The proposed bias circuit is a simple constant-gm current generator [19]. The reference current is inversely proportional to the bias resistor, and. is chosen to be 57 μA, which is 10x times less than the tail current of the first stage. The start-up circuit [20], essential to make sure that the bias generator

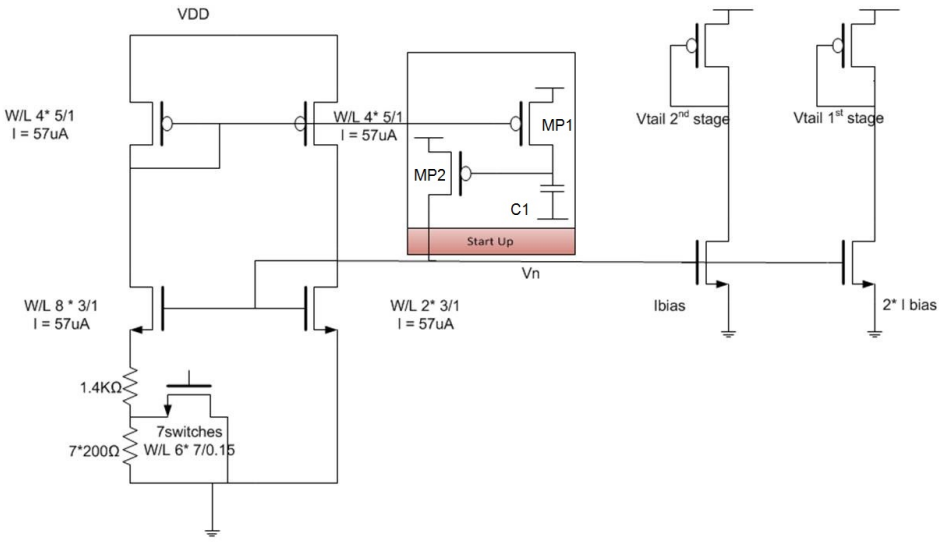

Figure 3.8: Self-Biased current generator

turns on at the right equilibrium point, consists of MOSFETs MP1,MP2 and capacitor C1. When the supply voltage turns on, the voltage drop across the capacitor is 0, as Vdd rises, MP1 starts slowly to charge C1. While the capacitor C1 is charging the MOSFET MP2 injects current into the bias circuit, this prevents the bias circuit from settling at an undesired equilibrium point. In order to be 100 % safe, an external start-up switch is added.
To add flexibility to the circuit, a tunable resistor is implemented, current in a range of 49 μA to 59μA is obtained by changing the resistor value. The tunable resistor selection switches are scaled in order to achieve an on resistance lower than 50Ω worst case.

3.4. COMMON-MODE FEEDBACK CIRCUIT

To maintain the output common-mode voltage at the designed value of 1.2V, a continuous time common-mode feedback circuit is used. A continuous time implementation has been chosen in order to avoid the clock circuitry required by a switched-capacitor implementation. If a differential input is given to the two input pairs, the signal current will be injected from a differential pair and absorbed totally by the other input pair. In this case no current will flow through the upper diode connected MOS, making the whole circuit transparent to such a stimulus. On the other hand, if a common-mode voltage change appears at the output, the two input pairs will provide currents with the same magnitude and polarity. These currents will flow in the diode connected MOS, and drive the regulating node, thus changing the amount of current flowing in the first stage. Stability of 67° degrees phase margin and DC gain of 32dB are achieved (figure 3.10)
Because of the lower loading of the main amplifier, this architecture is preferred to the common-sense resistor and error amplifier solution [21], or to the use of current sources operated in the

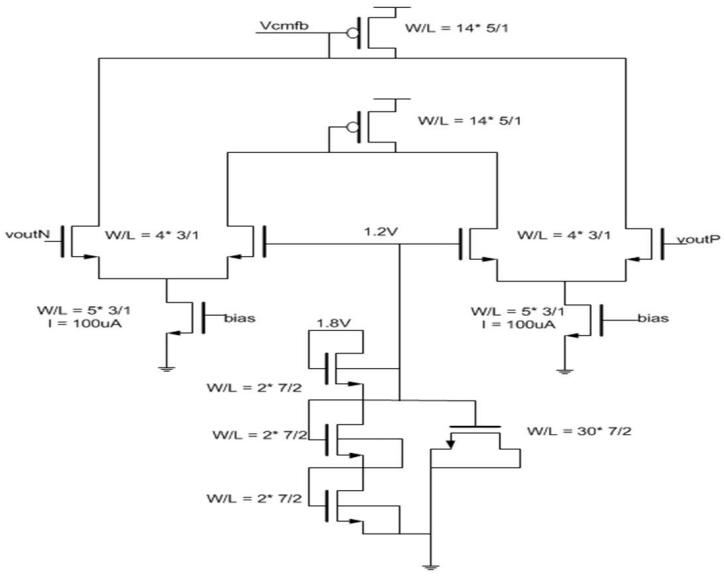

Figure 3.9: Common-Mode Feedback circuit

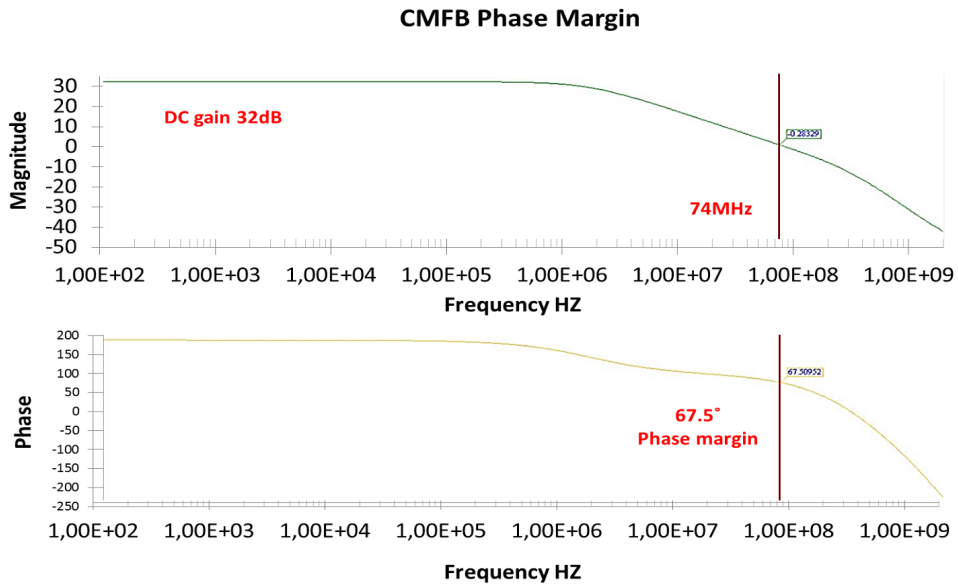

Figure 3.10: Common Mode Feedback circuit Loop Gain

linear region [20].

1.2 V reference is obtained by using a pMOS voltage divider, the source of these devices is tied to the bulk in order for a precise voltage division. The MOSFETs used in the divider have a low W/L ratio, few nA of current flows in these devices.

3.5. FEEDBACK CAPACITOR

To have more flexibility during the testing of the amplifier, a simple 2-bit programmable array of feedback capacitors has been designed. The unity cap C is 120fF; the switches are scaled in order

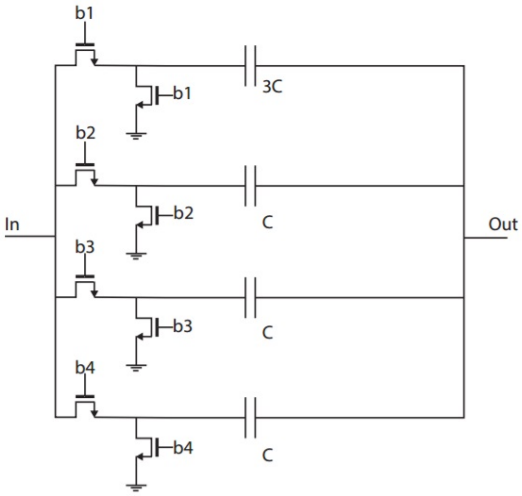

Figure 3.11: Feedback Capacitor Array

not to contribute to the noise performances of the system. The main disadvantage of this structure is the loading effect on the output when a capacitor is not selected. This will push the second OTA's pole towards the first amplifier pole, but, as shown in Figure 3.6 and Figure 3.14 this does not compromise the circuit stability.

3.6. RESET SCHEME

If no DC path is provided to a capacitive feedback amplifier, the presence of small DC offsets at the input can cause a significant drift of the OTA's output voltage and lead, eventually, to the failure of the stage.
Choosing the right reset strategy was one of the main concerns of this design. Several approaches were considered during the design of the CTIA.

- One approach is to create a permanent DC path by adding a resistor in parallel with the feedback capacitor (figure 3.12 a). If this solution is adopted, however, as the system level input-referred noise will be inversely proportional to the value of the feedback resistor, resistance in the order of 3 MΩ would be necessary, which implies a large chip area.
- An alternative to regular resistors can be the use of MOS pseudo-resistors [22] (figure 3.12 b), this structures can provide very high resistance in the order of GΩ. Unfortunately, their behavior, especially their leakage, is not well modeled in simulators, making this solution highly unreliable.
- Another option is shorting together both input and output to their respective common-mode voltages (figure 3.12 c). This solution, however, gives an undesired and uncontrollable offset amplification, as the input nodes of the OTA are shorted together.

As Figure 3.13 illustrates, the proposed solution involves the use of a source follower to recreate a "unity-gain" configuration. Such a circuit is needed because the input and the output common-mode voltages are not the same. During reset the source follower connects the OTA's output to its

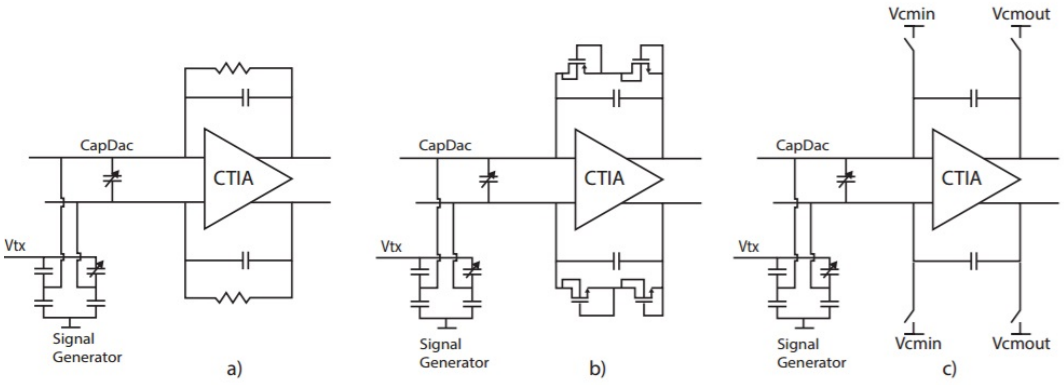

Figure 3.12: Reset schemes : a) resistor DC path b) Pseudo-resistors c)common-mode voltage shorts

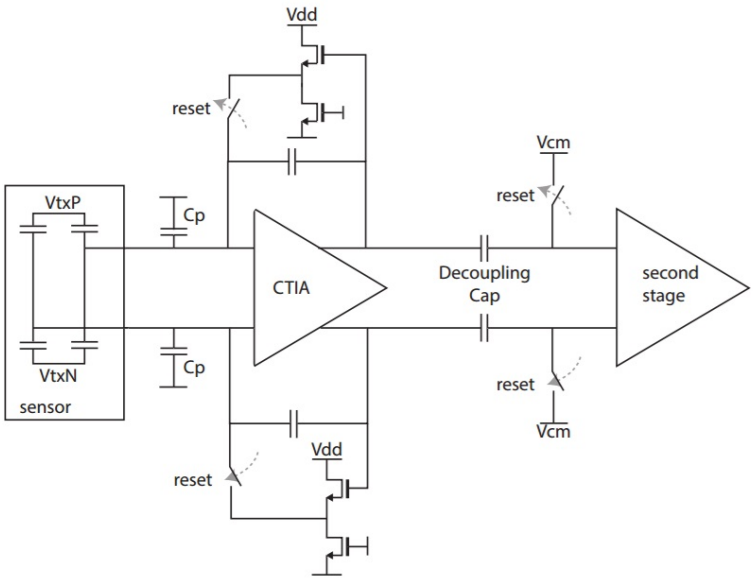

Figure 3.13: Front-end reset strategy

input, and, as already mentioned in section 3.1, the Miller capacitance of the OTA is increased to 1.85pF. As shown in picture 3.14, a 70° of phase margin during reset is achieved over corners. To avoid propagation of errors due to switching or settling during the reset phase, the following stage is kept in reset mode for a longer period compared to this one.

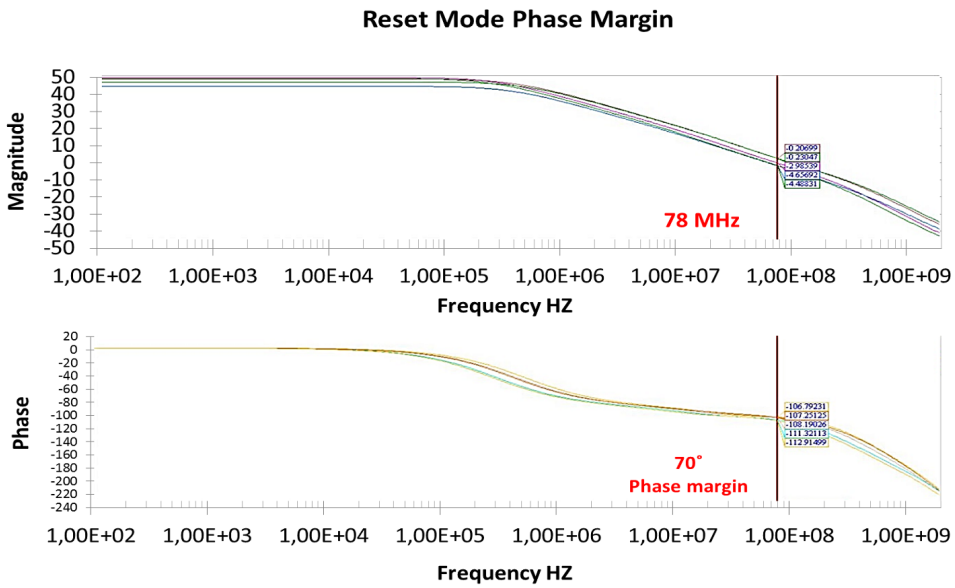

Figure 3.14: Reset Phase Loop Gain

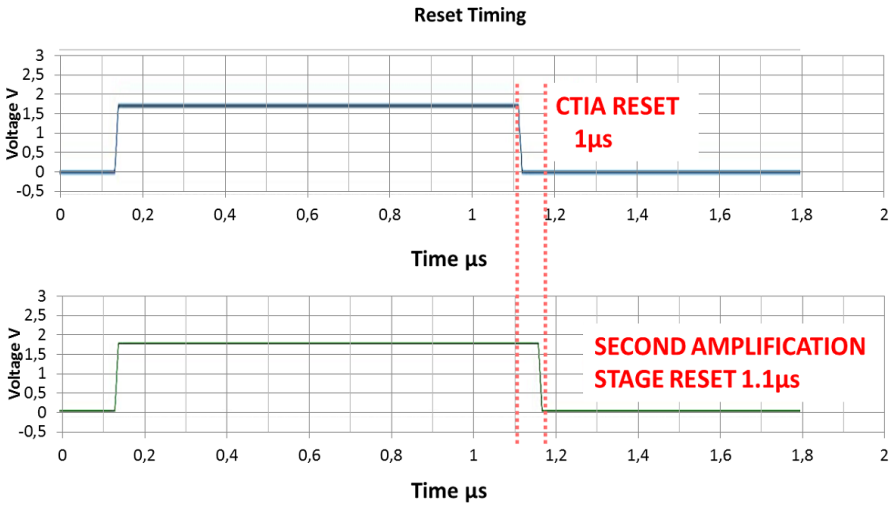

Figure 3.15: Reset Phase timing for input stages

3.7. TEST MODE

In Order to measure and debug possible errors in the circuit, a bypass structure has been implemented as shown in figure 3.16.
The bus structure can connect the output of the last amplification stage directly to the ADC input, whose output is connected to bond wires. It also allows the coherent detector to be bypassed, or for a signal to be injected directly into the mixer.

32 pads are also connected to the input node so as to be able to test the new structure with a real sensor. Two of these pad are bonded out and can be used for injecting a signal in the first stage.

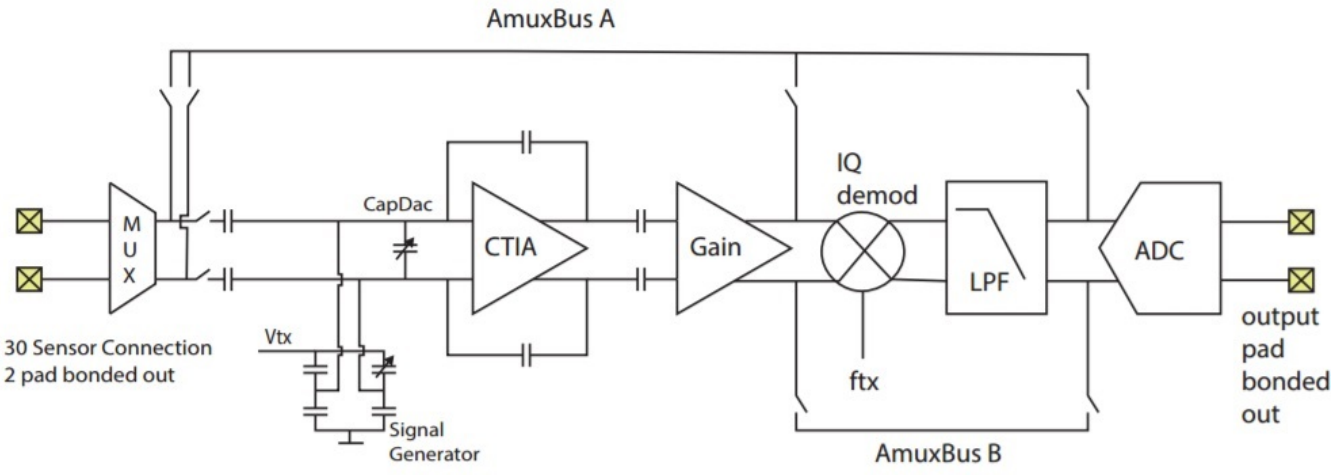

Figure 3.16: Bypass Amuxbus

3.8. LAYOUT

Figure 3.17 shows the layout of the proposed first stage; area is $303 \times 133 \mu m^2$. Correct isolation from substrate noise is required, for this reason, the block is placed in a deep N-well biased with a quiet substrate voltage, this avoids substrate noise. No particular common centroid structures are used in the amplifier in order to limit the parasitics. figure 3.18 shows the layout of the complete first stage including the cap-dac and the capacitive divider previously introduced in chapter 2.

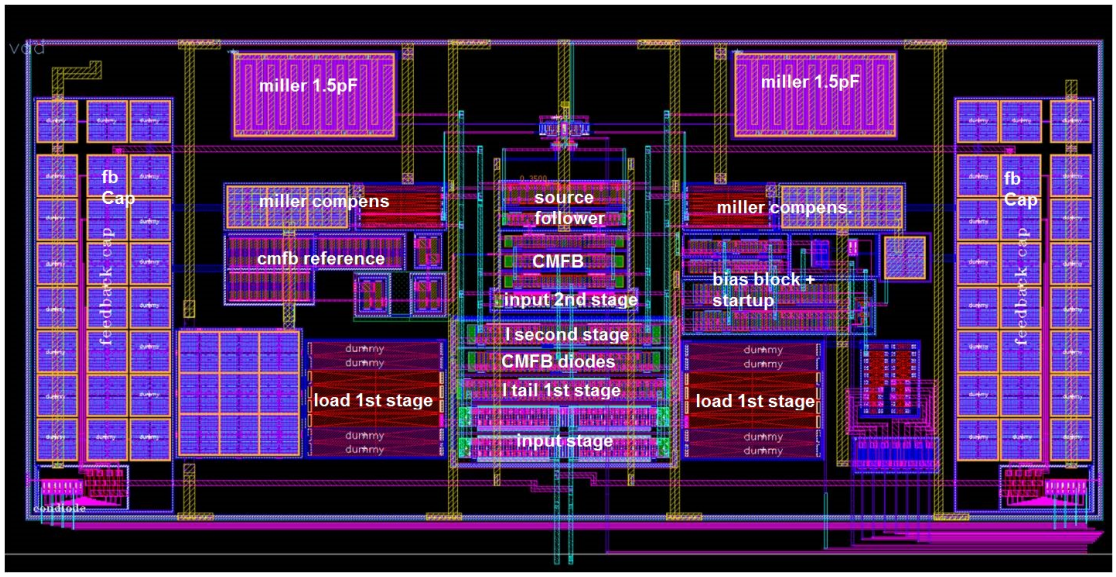

Figure 3.17: CTIA layout

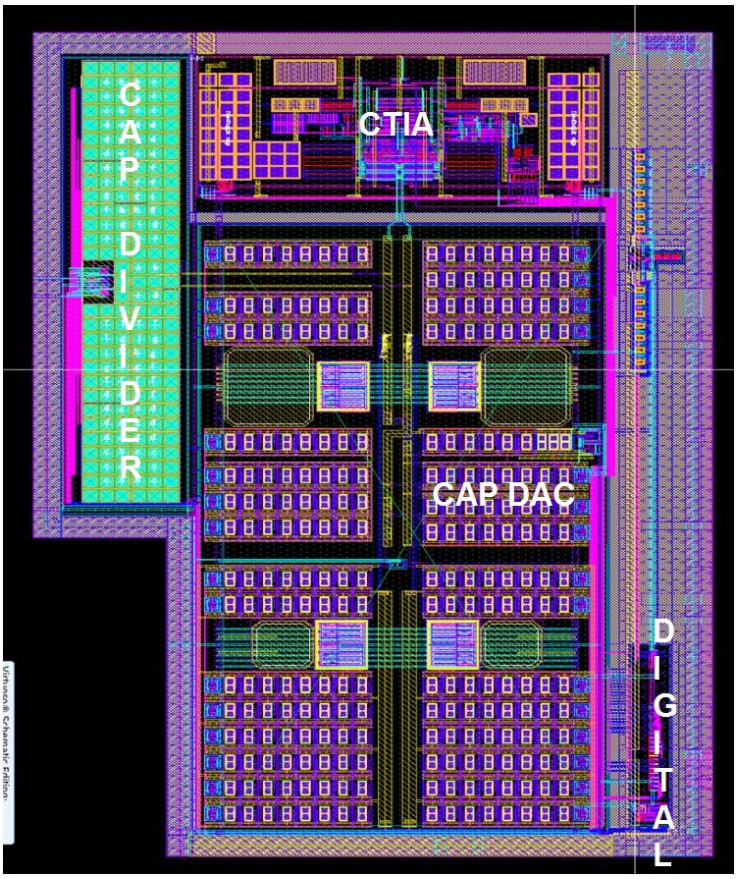

Figure 3.18: First stage layout

3.9. SUMMARY

This chapter described the transistor level design of the implemented first stage, pointing out the operating principles of the circuit and the challenges faced during the design. The implemented CTIA revolves around a very low-noise high-bandwidth amplifier. Lastly, the layout of the designed stage was showed. In the next chapter, the results of detailed system level simulations and post layout simulation will be discussed.

4

SIMULATIONS

The system level and circuit level design challenges were described in the previous chapters.

In this chapter, as a proof of concept, the most relevant simulations will be shown. The AC signal transfer of the implemented CTIA is found in section 1. In section 2 noise simulations are plotted. Particular attention is given to charger noise in section 3, and, in section 4, to Start-up simulations. Post-layout simulations are carried out in section 5. Power breakdown of the designed CTIA will be shown in section 6, and a summary of the achieved performances will finally be outlined in section 7.

4.1. SIGNAL TRANSFER

To check the transfer function, the AC simulation of the closed loop CTIA has been performed.The AC stimulus is in series with the input square wave. In Figure 4.1 the single ended output of the CTIA is plotted. The signal at the output is an attenuated version of the input square wave, the closed loop

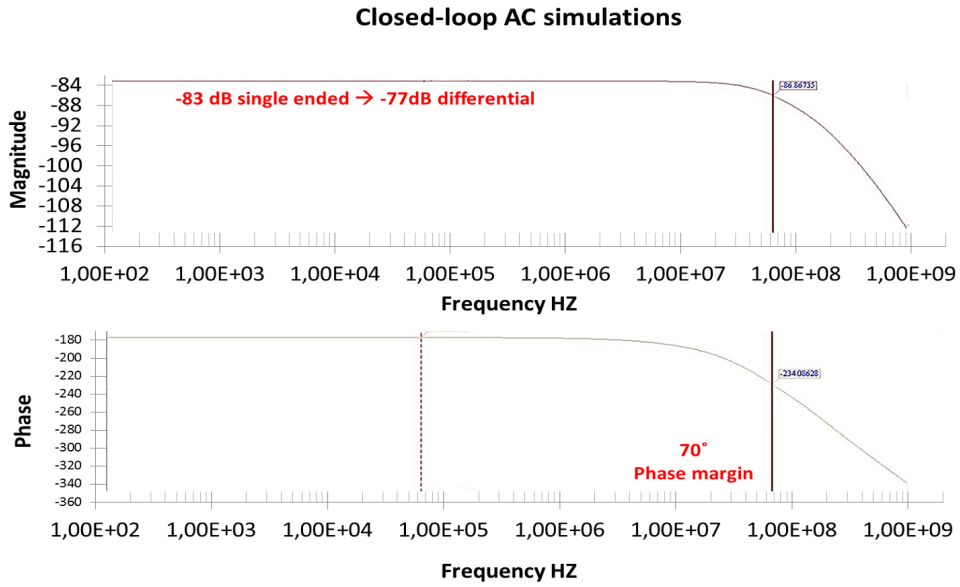

Figure 4.1: CTIA differential output AC transfer function

-3dB frequency is 66MHz, while the differential attenuation of the clock signal generator is -77.8dB.

4.2. NOISE SIMULATIONS

Noise is the primary concern of this design; gm stage input-referred noise target value is between $3.24\frac{nV}{\sqrt{Hz}}$ and $5.16\frac{nV}{\sqrt{Hz}}$, as derived in chapter 2. The lower limit is set in order to avoid an over-designed first stage, i.e. a higher power consumption. However, a value as close as possible to $3.24\frac{nV}{\sqrt{Hz}}$ guarantees a 1-to-1 match, in terms of SNR, with the respect of the actual implementation. The simulated input-referred noise of the OTA is $3.3\frac{nV}{\sqrt{Hz}}$, as shown in Figure 3.7 in chapter 3. Closed-loop noise simulation, including the noise contribution of the second amplification stage, gives a noise floor of $26.85\frac{nV}{\sqrt{Hz}}$ for the nominal run. According to formula 2.7, a theoretical maximum SNR of 27dB can be achieved. Figure 4.2 shows the noise profile at the output of the CTIA.

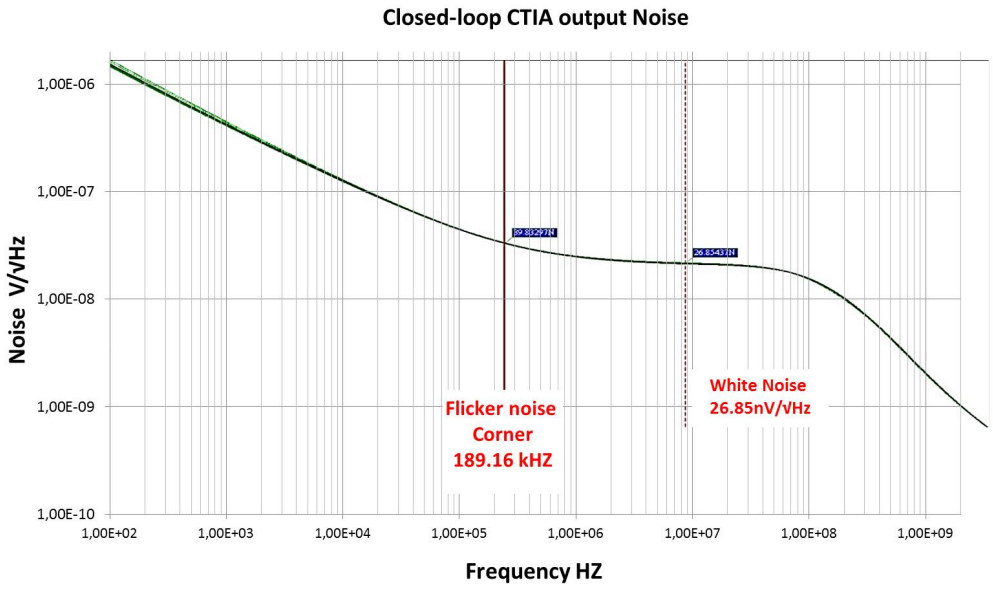

Figure 4.2: Simulated noise at the input of the second stage, 100 different runs

4.3. CHARGER NOISE

As explained in Chapter 1, charger noise capacitively couples directly at every touch point. As to simulate the effect of this disturbance on the circuit, a measured noise profile showed in Figure 4.4 was used. Charger noise coupling capacitors were measured to be approximately 7fF. A representation of the circuit utilized for this simulation is shown in Figure 4.3. As can be seen in Figure 4.5, when only charger noise is applied, the differential output of the CTIA is 100 times smaller with respect to signal amplitude. A second concern related with high voltage amplitude interferences is the overload, and subsequent clipping of the amplification stage. Figure 4.6 shows that the amplifier virtual ground and output are not shifting significantly from the applied common-mode bias voltage of 350mV and 1.2V respectively. In other words, the fully differential first stage rejects the charger noise.

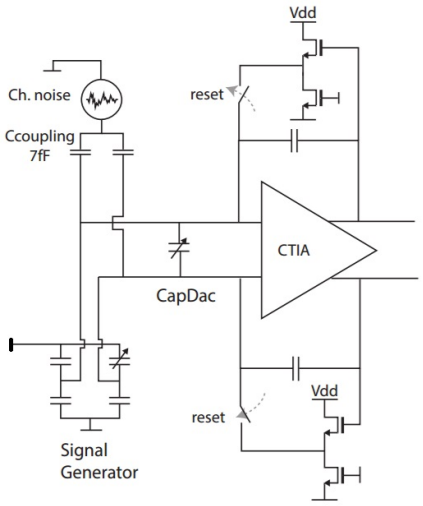

Figure 4.3: Simulation Schematic for Charger Noise

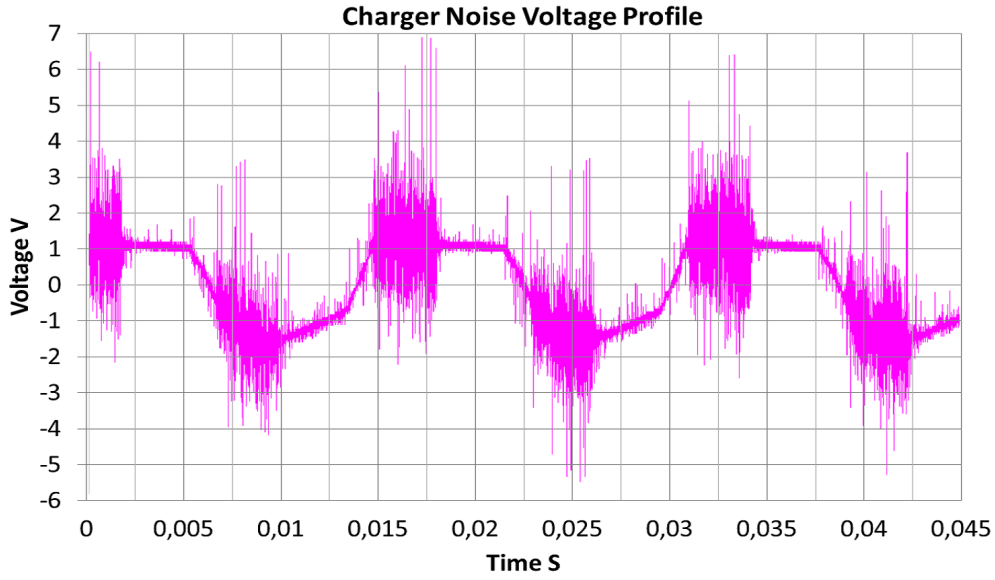

Figure 4.4: Charger Noise Profile

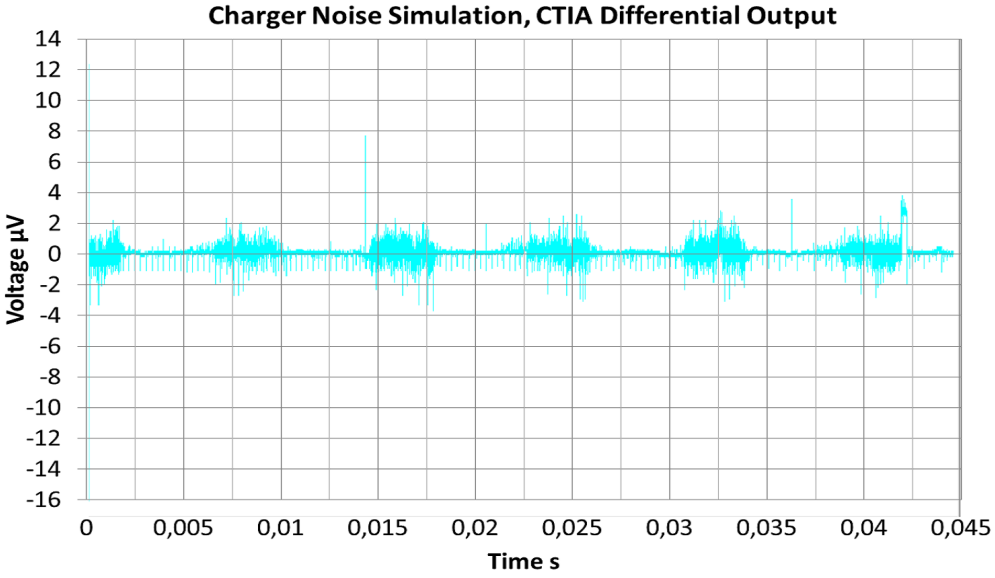

Figure 4.5: CTIA Differential Output Signal, Charger Noise Applied

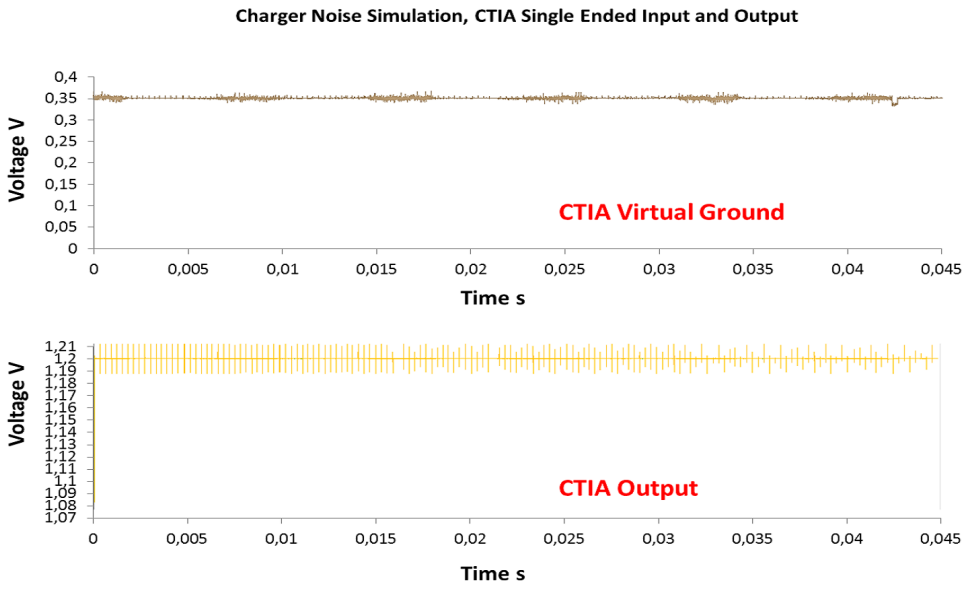

Figure 4.6: CTIA Single Ended Input and Output, the Negative and Positive Input(top figure)/ Output (bottom figure) are overlapping

4.4. START-UP

Start-up simulations are done by giving a finite rise time to the supply voltage. Such test pointed out a potential mechanism of failure of the circuit. Figure 4.7 shows the OTA core and the common-

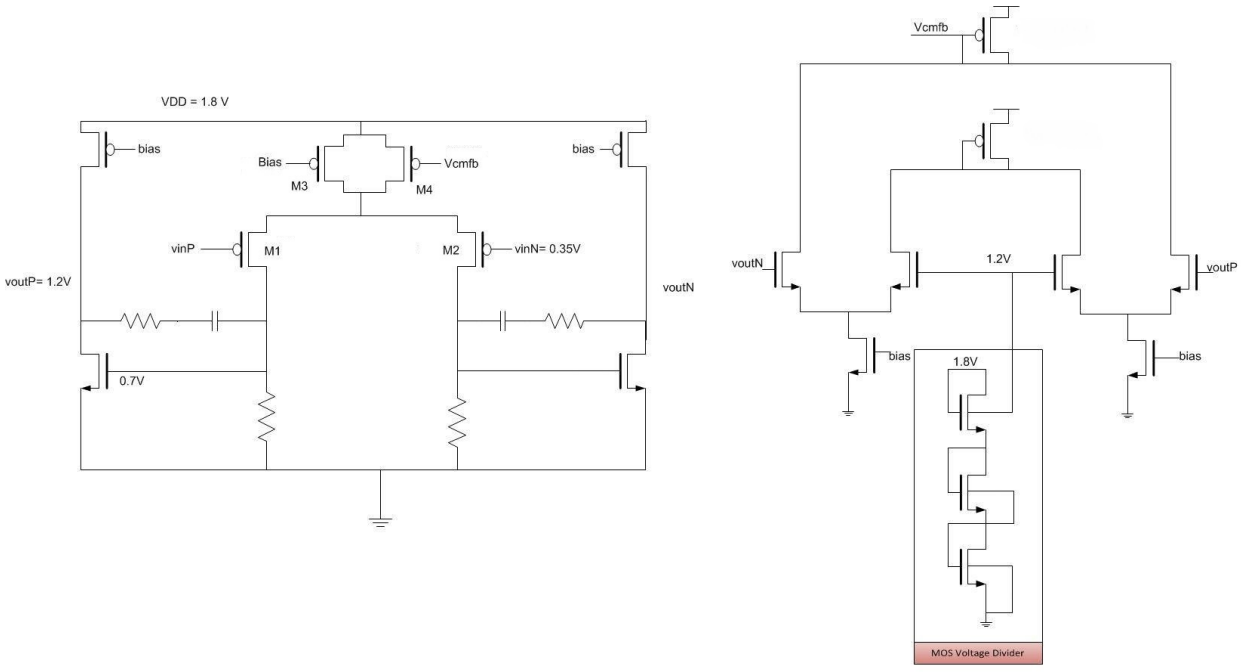

Figure 4.7: OTA core on the left, CMFB circuit on the right

mode feedback circuit introduced in chapter 3. When Vdd is increasing from 0 to the final value, the circuit activates. The start-up of the current bias generator introduced in chapter 3, is guaranteed by

the presence of a start-up circuit. In this phase the common-mode feedback is not entirely turned on because the 1.2V internal reference voltage is obtained with a Mos voltage divider. At the same time a low gain positive feedback for common-mode stimulus applies, so the source of the pMOS input pair M1 and M2 raise it's potential and starve the tail current sources M3 and M4. The effect on the OTA's input and output are shown in figure 4.8. When the output of the circuit saturates

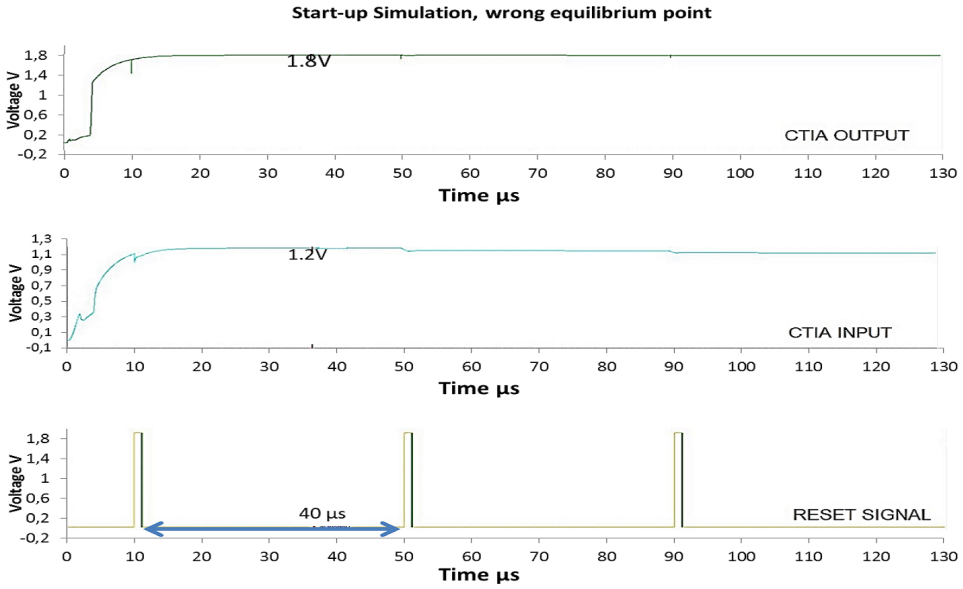

Figure 4.8: wrong equilibrium point found during startup

to Vdd, the source follower output is at 1.2 V, so out of the input common-mode range of the OTA that goes from 0V up to 0.9V. The source followers are not able to push down the input pair voltage enough to activate the common-mode feedback circuit.

In order to overcome this problem the source follower has been designed with a large Vgs, this permits the source follower output to be in the input common-mode range of the amplifier when the output is saturated. By doing this the common-mode feedback circuit activates and set the correct bias voltage. Figure 4.9 shows the effectiveness of the implementation.

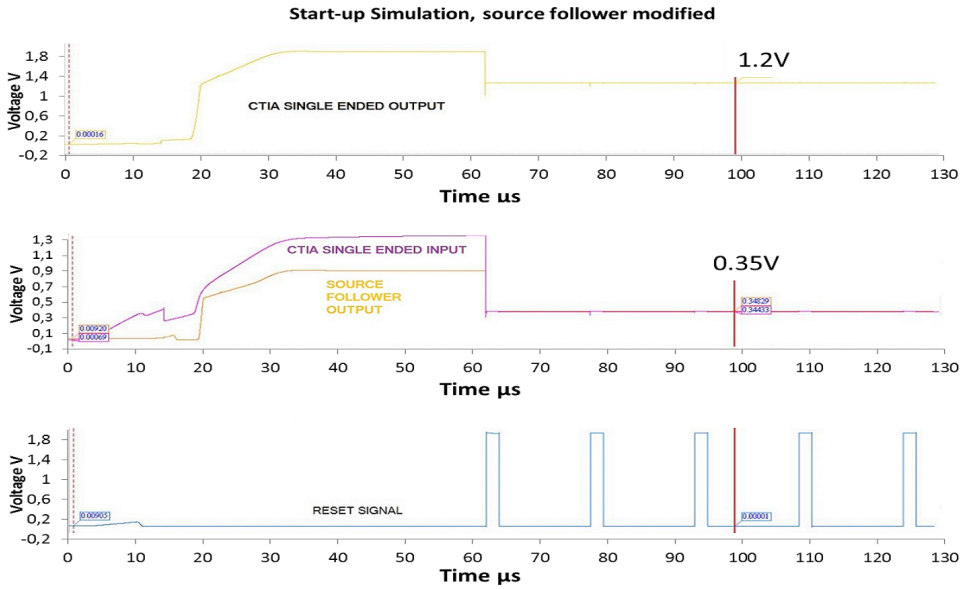

Figure 4.9: Reset Phase With Modified Source Follower

4.5. POST-LAYOUT SIMULATIONS

Post layout simulations were done to validate the overall system's performance, including the effect of parasitic capacitances, resistances, and diodes. Firstly the OTA's open-loop gain and input referred noise are simulated: As can be seen in Figure 4.10 the OTA's open-loop -3dB frequency de-

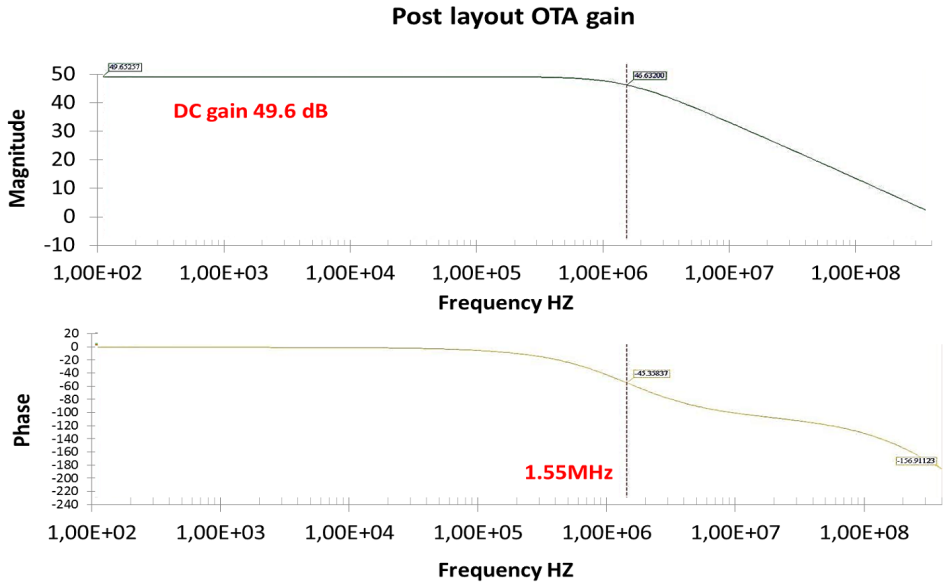

Figure 4.10: open loop gain

creases to 1.58 MHz. This result still guarantees a closed-loop -3db frequency of 60 MHz, which is slightly below the target of 63 MHz discussed in chapter 2. Due to the increase of the gate resistance, the OTA's input referred noise increases from 3.29$\frac{nV}{\sqrt{Hz}}$ to 3.5$\frac{nV}{\sqrt{Hz}}$, as shown in Figure 4.11.

The closed loop noise at the input of the second stage increases from 26$\frac{nV}{\sqrt{Hz}}$ up to 33$\frac{nV}{\sqrt{Hz}}$ because of

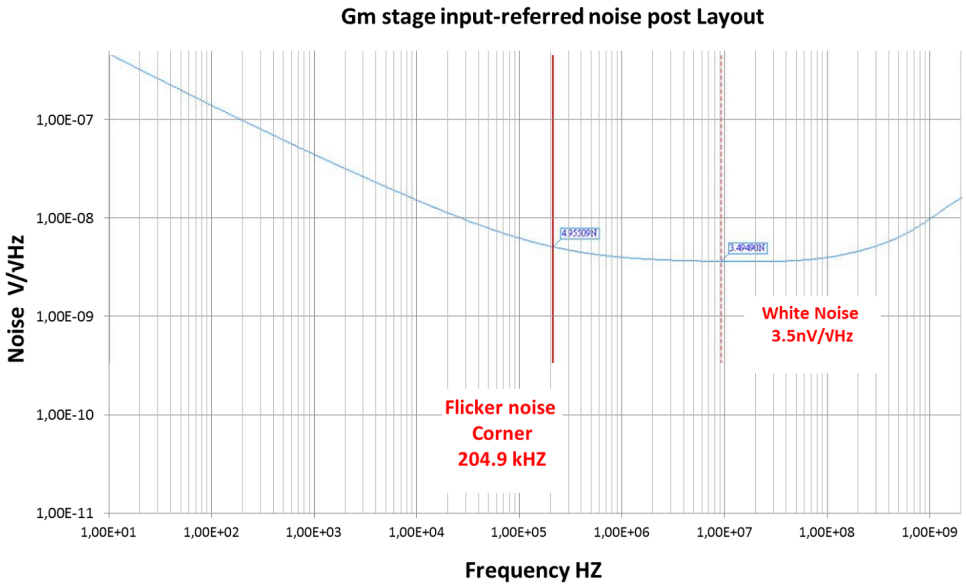

Figure 4.11: OTA input referred noise

the increase in the input referred noise of the OTA and the parasitic capacitance added at the input node. The calculated SNR is 25.2dB.

4.6. POWER

Power is not a critical specification for this design. The power budget for the first stage is 3.6mW, i.e. a quiescent current of 2mA in total. The power breakdown of the implemented stage is shown in Figure 4.12

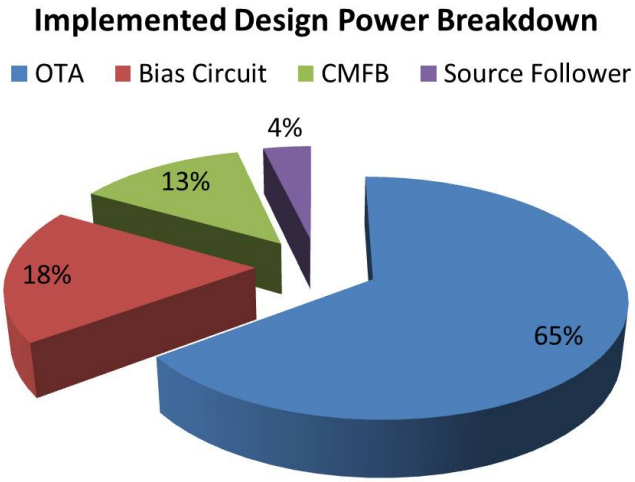

Figure 4.12: power breakdown

The OTA core consumes in total 1mA, the bias circuit plus the current mirror branches consume

in total 220μA, the common-mode feedback circuit is biased with 200 μA in total, and the source followers burn 57μA. The total quiescent current is 1.48mA, that translate in 2.67mW of power.

4.7. SUMMARY AND TABLE OF PERFORMANCES

The performance achieved by this circuit are summarized in Table 4.1: In this chapter the relevant

	Simulation Results	**Specifications**
OTA input referred noise (post layout)	$3.5\frac{nV}{\sqrt{Hz}}$	$3.27 < X < 5.16\frac{nV}{\sqrt{Hz}}$
OTA DC gain (post layout)	$49.4dB$	/
OTA GBW (post layout)	$470Mhz$	$\geq 440MHz$
SNR	$25.2dB$	$\geq 20dB$
CTIA area	$303 \times 133\mu m^2$	/
RX channel area	$1.5mm^2$	$2mm^2$
Power (Static, CTIA only)	$2.67mW$	$< 3.6mW$

Table 4.1: Table of performances

simulations and the results of post-layout simulations are shown in detail. In conclusion, a summary of the achieved performances is shown.

As can be seen in Table 4.1, the circuit meets the target specifications in terms of noise and bandwidth. The area of the proposed solution RX channel is 0.3x smaller with the respect to the actual RX channel. This results confirms the feasibility study and the effectiveness of the implemented design. Because of lack of time and resources, the circuit was not taped out, thus no measurements results are available. The next chapter will conclude this thesis report with some general conclusions and some suggestions for future improvements.

5

Conclusions and Future Work

5.1. Conclusions

This thesis discussed the design and implementation of a new first stage for a capacitive fingerprint sensor readout. The new front-end circuit aims to replace an off-chip bandpass filter with a Capacitive Feedback Transimpedance amplifier. The target of this project is to achieve a minimum SNR of 20 dB for a minimum capacitive change of 50aF. By eliminating the off-chip bandpass filter the cost of the chip is reduced, an overall thinner form factor solution is obtained, and a first step towards the implementation of a multi-channel receiver, thus a faster system, is made.

An SNR of 25.2 dB in a 50Khz bandwidth is simulated. The circuit can completely reject external common-mode interferences as charger noise. This translates into a one-to-one comparison with the solution involving the bandpass filter in terms of noise performances.

5.2. Future Work

Some further work can be done to improve some aspects of this design, such as input node parasitics and RX channel area. This may lead to more relaxed specifications for the first stage, and an easier step forward towards the implementation of a multi-channel structure

5.2.1. Multiplexer Architecture

The input parasitics mostly come from the capacitance associated with the ESD protection diodes present at every intersection.

The actual implementation of the multiplexer is shown in figure 5.1 When a line is selected, during scan mode, all the other lines are in high impedance mode to avoid a possible leakage path for the signal current. In this case, all the parasitic associated with the diodes are summed up, as they are in parallel, at the input node.

A possible solution involves the use of 1 more switch for every intersection in order to connect or disconnect completely the nodes. The trade-off to investigate is between parasitic capacitance, noise and area added by the extra switch placed.

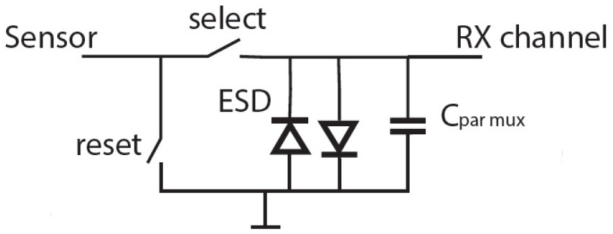

Figure 5.1: Multiplexer implemented

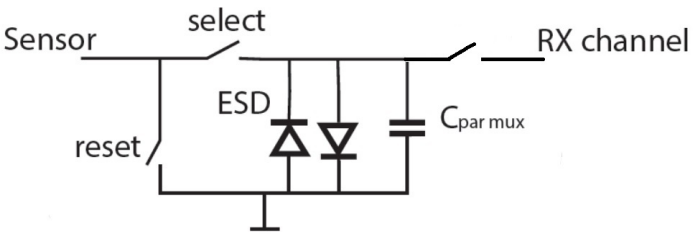

Figure 5.2: New Multiplexer Proposed

5.2.2. ΣΔ BANDPASS CONVERTER

The introduction of a continuous-time bandpass ΣΔ converter after the first two gain stages can replace the bulky coherent detector and ADC. Coherent detection can still be performed in the digital domain [23].

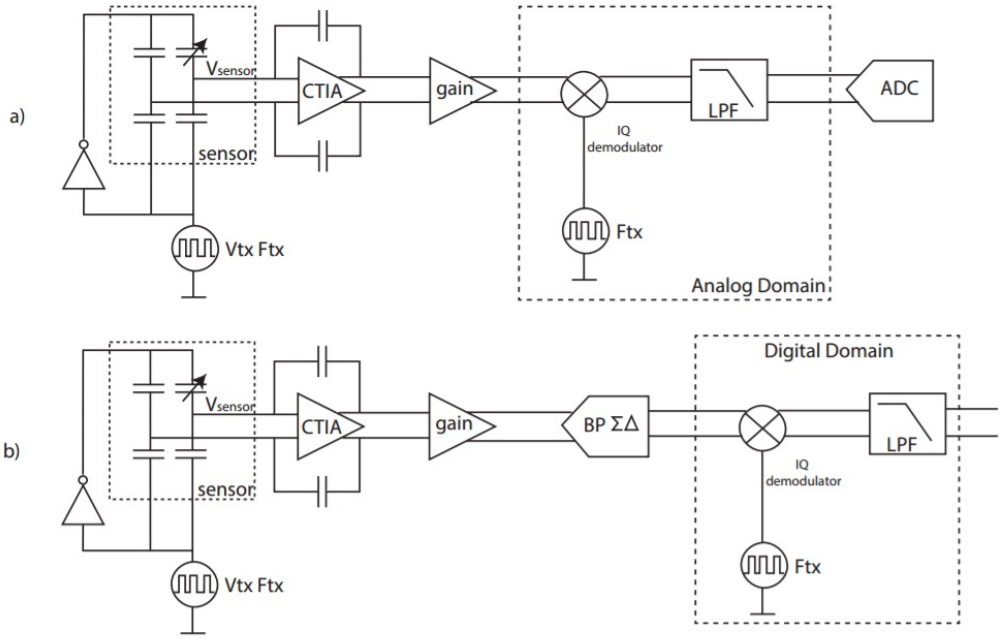

Figure 5.3: Difference between proposed architecture (a) and proposal for future work (b)

For this specific applications, since only 20dB SNR are required, a second order modulator is

sufficient for fulfilling the specifications. In other words, only a resonator, a 1-bit DAC and a comparator are needed. Continuous time implementation is preferred for its natural anti-alias filtering action

A simple MATLAB Simulink model of a continuous-time bandpass modulator has been implemented to prove the feasibility of this proposal. The model in Figure 5.4 doesn't take into account well-known problems related to the implementation of a continuous time ΣΔ such as loop delay or finite gain/bandwidth of the resonator. In this model the simulated signal and noise level at the output of

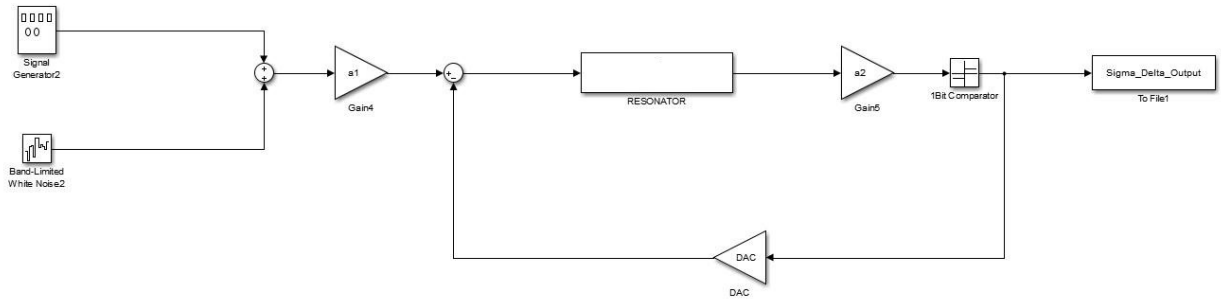

Figure 5.4: Matlab Modulator Model

the amplification chain are fed at the input of the modulator to recreate a realistic SNR estimation. Figure 5.5 shows the spectrum of the output bitstream when no thermal noise is applied, while figure 5.6 shows the FFT of the demodulator output in the presence of white noise, 26 dB SNR are obtained. The two proposed solution can lead to the integration of at least 4 channels in the same amount of area with a comparable power consumption.

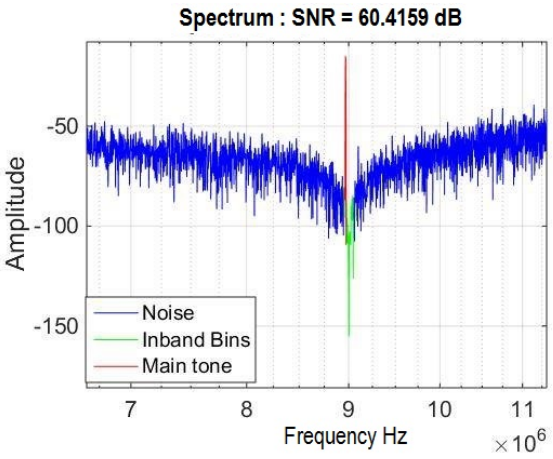

Figure 5.5: Bitstream Spectrum, No Thermal Noise

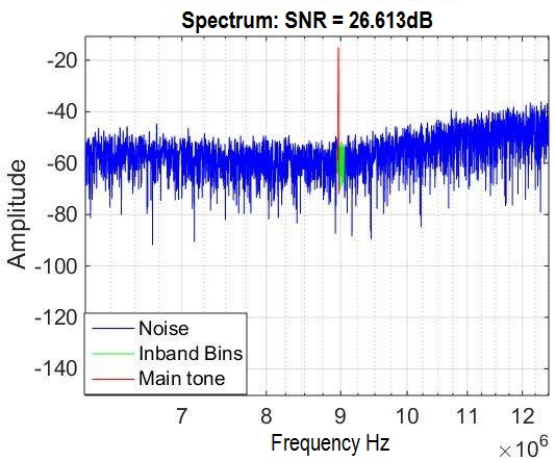

Figure 5.6: Bitstream Spectrum, Thermal Noise added

APPENDIX A
EQUIVALENT NOISE BANDWIDTH CALCULATION

The Equivalent Noise BandWidth (ENBW) is a mathematical concept introduced in order to have an easier calculation of the SNR in a noisy system. By using the ENBW while calculating the integrated noise, the system transfer function H(s) can be replaced by an equivalent "brickwall" filter that has the same total output noise power.

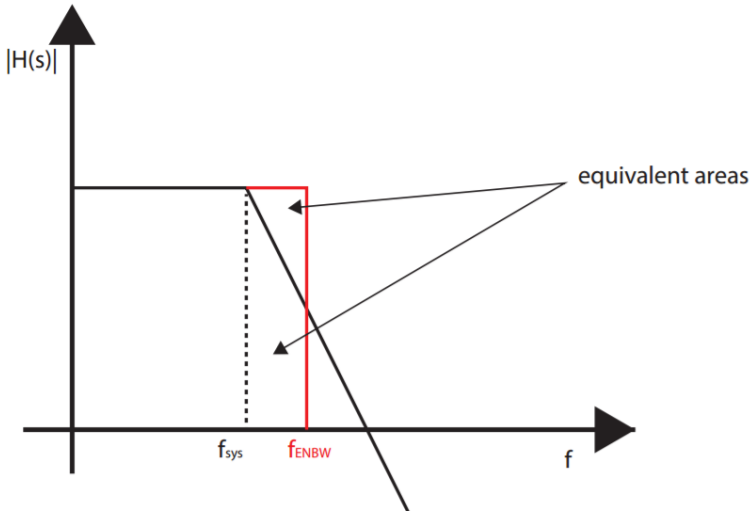

Figure 7: Equivalent Noise Bandwidth principle

The low-pass filter used in this design is a second order filter where the first stage corner frequency is at 50kHz and the second stage corner frequency at 440kHz. The ENBW is calculated as:

$$ENBW = \frac{1}{2\pi}\int_0^{\inf} \frac{|H(j\omega)_{first-filter}|^2}{H(0)^2_{first-filter}} \frac{|H(j\omega)_{second-filter}|^2}{H(0)^2_{second-filter}} d\omega = \frac{1}{2\pi}\int_0^{\inf} \left[\frac{1}{1+\left(\frac{\omega}{2\pi 50kHz}\right)^2} \frac{1}{1+\left(\frac{\omega}{2\pi 440kHz}\right)^2}\right] d\omega = 70kHz \quad (1)$$

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