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## A Novel Beam Switching Heatsink Antenna Array With CSRR Embedded Isolation Wall

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**DOI**
10.1109/LAWP.2023.3302572

**Publication date**
2023

**Document Version**
Final published version

**Published in**
IEEE Antennas and Wireless Propagation Letters

# From Cooling to Coupling and Back: A Novel Beam-Switching Heatsink Antenna Array With CSRR Embedded Isolation Wall

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***Abstract*—A novel electromagnetic-thermal codesign and optimization methodology is proposed for thermal management in active finned-heatsink antenna arrays. An innovative complementary split-ring resonator embedded dual-functional (i.e., heat-dissipating electromagnetic-isolation) wall is introduced. For concept demonstration, a two-element unit cell is designed at 26 GHz with the wall in between the antenna elements. It is shown via simulations that the proposed design decreases the junction temperature of the chip driving the elements by almost 40 °C and 15 °C as compared with the conventional and finned-heatsink antennas, respectively. Moreover, the port coupling level is reduced to below −25 dB near the operating frequency and a low-complexity beam-switching and nulling function is achieved.**

***Index Terms*—Antenna cooling, beam switching, complementary split-ring resonator (CSRR), heatsink antenna, mutual coupling, pattern nulling.**

## I. Introduction

5G AIMS to meet the ambitious data rate demands by increasing the operating frequencies to the millimeter-wave ranges (above 24 GHz) and introducing the active phased array technologies [1]. However, in the Ka-band (26–40 GHz), the efficiency of the low-cost silicon-based power amplifiers driving the antennas can reach only up to 30% [2]. This poor efficiency causes excess heat, which may lead to the failure of the electronics. Even in case of no failure, every 10 °C rise in the temperature halves the lifetime of the radio-frequency (RF) chip [3]. The maximum junction temperature of the chip must be kept under 125 °C for safe operation [4].

Conventionally, active arrays at the base stations use external heatsinks attached to the chips at the back of the board [5]. In such an approach, the cooling capability becomes limited by the effective height of the heatsink [6]. Dual-functional antennas that contribute to chip cooling while addressing the antenna pattern shape and port isolation requirements can improve the thermal management capacity and relax the requirements on the external heatsinks [7].

The intriguing concept of "antenna-as-a-heatsink" was introduced about a decade ago [8]. Since then, several forms of 3-D heatsink antenna elements based on extruded-fins [9], radial fins [10], and fractal topologies [11] have been proposed. However, the research was limited to single elements as the fins create a significant space-wave coupling problem in an array [12].

Various techniques to reduce mutual coupling include electromagnetic band-gap structures [13], defected ground planes [14], multilayer substrates [15], [16], complementary split-ring resonator (CSRR) [17], [18], and so on. However, they aim to suppress solely the surface-wave coupling. To deal with the space-wave coupling, a wall should be inserted vertically between the antenna elements, but using reradiating structures on the wall for coupling reduction can dramatically increase the back lobe and side lobes [19].

To allow usage of finned patches in arrays, support beam-switching, and simultaneously enhance cooling capabilities, we propose in this letter, a unique electromagnetic-thermal codesign and optimization methodology for a new dual-functional CSRR-embedded wall. For concept demonstration, we use the finned heatsink antenna element introduced in [10], and extend it to a two-element active unit cell for a 26 GHz base station antenna array. The letter novelty lies in the first-time development of 1) a heat-dissipating electromagnetic-isolation wall for finned antenna elements, and 2) a low-cost beam (and null) switching two-element subarray.

The rest of this letter is organized as follows. Section II describes the intended use case and performance requirements. Section III provides the electromagnetic-thermal analysis of a conventional array as the benchmark. Section IV revisits the heatsink antenna element and explains the design of the dual-functional walls. Section V discusses the simulation results. Finally, Section VI concludes this letter. Through our study, ANSYS ICEPAK and ANSYS HFSS are used for thermal and electromagnetic simulations, respectively.

## II. Use Case and Electro-Thermal Requirements

The array structure studied in this letter aims for multipattern operation in the elevation plane in the 26 GHz band with two antenna elements. Such two-element unit cells are combined horizontally to perform flexible beamforming in azimuth. As modern base stations are expected to communicate with satellites, ground users, and other base stations, with minimal interference levels and low analog and/or digital beamforming complexity [20], [21]. The following three different scenarios (patterns) are considered.

1) The array communicates with the satellite while avoiding interferences due to ground reflections and environmental scatterings.

Manuscript received 23 June 2023; revised 28 July 2023; accepted 29 July 2023. Date of publication 7 August 2023; date of current version 1 November 2023. This work was supported by the Microelectronics Department at the Delft University of Technology in the framework of the Synergy Grant. *(Corresponding author: Feza Turgay Celik.)*

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Digital Object Identifier 10.1109/LAWP.2023.3302572

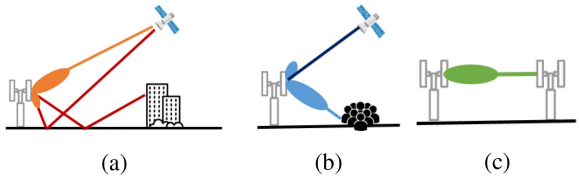


Fig. 1. Base station use case scenarios for communication with (a) satellites, (b) ground users, and (c) other base stations.

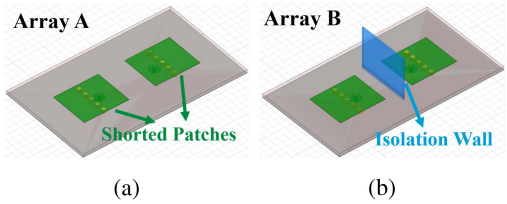


Fig. 2. Isometric view of the (a) conventional patch array (Array A) and (b) patch array with a cooling wall (Array B).

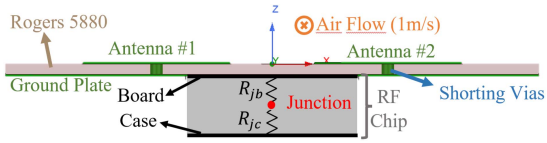


Fig. 3. ICEPAK simulation environment of the Array A.

2) The array communicates with the ground users while suppressing interference to the satellite.
3) The array communicates with another base station while suppressing interference to the satellite and ground users. Fig. 1 visualizes the three scenarios.

The objectives of the electromagnetic performance of the array are to reduce coupling between the two antenna elements below $-25$ dB at the resonance frequency while achieving 500 MHz bandwidth and beam switching to $+30°$, broadside, and $-30°$ directions in the elevation plane. The objective of the thermal performance of the array, on the other hand, is to keep the junction temperature ($T_j$) of a commercially inspired RF chip (required for power amplification and azimuthal beamforming) below 125 °C.

## III. Thermal Model of the Conventional Array

To highlight the cooling limitations of the conventional pin-fed patch antenna array, thermal simulations of the $2 \times 1$ unit cell are performed. To conduct the heat from the RF chip to the patch efficiently, the patch elements are shorted from their middle line with five copper vias having 0.2 mm diameter. Patch dimensions are selected as 3.6 mm $\times$ 3 mm to resonate at 26 GHz, which is printed on Rogers 5880 with a thickness of 0.254 mm. Such shorted-patch antenna is commonly used at all design iterations. The array formed with two shorted patches separated by 5.7 mm ($\sim \lambda_0/2$) will be denoted as "Array A" for simplicity [see Fig. 2(a)].

The simulation environment consists of a multilayered structure consisting of an RF chip, antenna ground, dielectric, and patches. The side view of the simulation environment can be seen in Fig. 3. The board of the chip makes thermal contact with the ground plate of the array through the junction to board resistance. Thermal energy is conducted between junction to antennas by using chips board, ground plate, and shorting vias as a heat conducting mechanism as seen in Fig. 3.

TABLE I
Thermal Properties of the Simulation Environment

| | | | |
|---|---|---|---|
| Rogers 5880 Conductivity | 0.2 W/m/K | Thermal Paste Conductivity | 8.9 W/mK |
| $R_{jb}$ | 14 K/W | $T_{\text{ambient}}$ | 20°C |
| $R_{jc}$ | 10 K/W | Junction Power | 1.35 W |
| Heat. Trans. Coef. | 10 $W/m^2K$ | Dielectric Size | 13×7.5 $mm^2$ |

Thermal simulations are realized under the assumption of 1 m/s airflow along the patches. Simulations are done by considering the worst-case scenario (i.e., when two antennas operate simultaneously). The junction temperature of the chip would be lower in single-port excitation scenarios. Two resistor network is used to model the thermal behavior of the chip, as suggested by the JEDEC standards [22], and validated experimentally with the temperature sensors [5]. This study implicitly considers an external heatsink cooler attached to the chip surface [5]. To reduce the complexity of the simulations, the heat power of the chip is reduced according to the maximal cooling capacity of the cooler, and the remaining heat is conducted to the antenna surface with the shorting vias. The RF chip thermal model parameters are retrieved from commercial communication chips [5]. The detailed information about thermal properties used in the simulations are given in Table I.

The junction temperature of Array A is simulated as 163.6 °C, which is unacceptable. The conventional design is not sufficient to reduce the junction temperature to an acceptable value. Therefore, a metallic wall is inserted, which results in the design of Array B [see Fig. 2(b)].

The wall in Array B is directly connected to the ground plate of the array. As this wall extends in the vertical axis, it introduces an additional surface for convection. To limit the input impedance and pattern distortions due to the excess reflections from the isolating wall, the wall size is arranged to be close to $\lambda_0/4$ (3 mm). In this case, the junction temperature is simulated as 147.3 °C by using the simulation environment illustrated in Fig. 3. Although the wall brings a 16.3 °C junction temperature drop, it still is not sufficient. Also, Array B suffers from an electromagnetic isolation problem. The conducting wall inserted between elements induces reradiated currents from elements, increasing the coupling between the ports ($|S_{21}|$ value) from $-16.92$ to $-13.3$ dB. In order to lower the junction temperature to 125 °C, we proposed to use finned antenna elements as additional cooling agents [10].

## IV. Design of Radiating and Isolating Elements

### A. Heatsink Antenna

To resolve the limited cooling capacity problem of conventional patch antennas, a copper fin array, which is connected to the patch by means of thermal glue [10], is used in this study. Even though the thermal glue is a poor electrical conductor, it does not affect the electromagnetic performance of the antenna as it is very thin compared with the wavelength (less than $\lambda_0/20$). The heatsink antenna has four essential parameters that have an impact on cooling capacity, impedance characteristics, and radiation pattern, namely, the height of the fin base ($h_b$), the distance between fins ($d$), fin height at the antenna center ($h_c$), and fin height at the edges of the antenna ($h_s$). As a

TABLE II
EFFECT OF INCREASE IN THE FIN PARAMETERS ON ELECTROMAGNETIC AND THERMAL PERFORMANCE MEASURES

| Variable name | Resonance frequency | Directivity | Polarization sense | Cooling capability |
|---|---|---|---|---|
| $h_b$ | Decreases | Increases | Deteriorates | Increases |
| $d$ | Decreases | Decreases | Deteriorates | Increases |
| $h_c$ | Not affected | Not affected | Not affected | Increases |
| $h_s$ | Decreases | Decreases | Deteriorates | Increases |

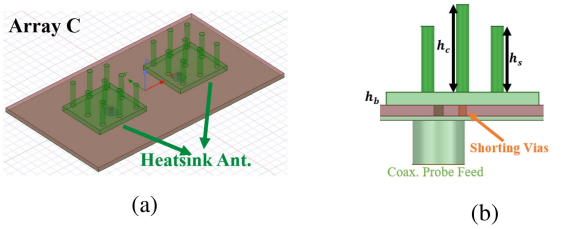


Fig. 4. Array C heatsink antenna view. (a) Isometric. (b) Element—side.

design guideline, the effect of the increase in the mentioned parameters on the thermal and electromagnetic parameters is given in Table II. Based on this, Array C is formed by using two heatsink antennas. Patch dimensions are selected as 3.5 mm × 3 mm, while using fin sizes $h_b = 0.3$ mm, $h_c = 2$ mm, $h_s = 1.5$ mm, and d = 0.8 mm to resonate at 26 GHz. The isometric view of the heatsink antenna array (Array C) and the side view of its elements can be seen in Fig. 4.

In Array C, the junction temperature of the chip is found to be 138.4 °C. Although the heatsink array yields better cooling as expected, more is needed. In addition, the vertical fins at the element edge in Array C result in stronger mutual coupling between the elements than in conventional patch arrays. The resulting $|S_{21}|$ value at the resonance frequency is −8.12 dB. Both the isolation and thermal problems of Array C motivate us to introduce a vertical wall between the elements that houses a CSRR structure to suppress the coupling, while bringing an extra heat dissipation surface.

### B. CSRR Isolation Wall

To deal with the shortcomings mentioned earlier, a dual-functional wall is placed between the two elements. A metallic shorting wall is embedded in the substrate to prevent the propagation of surface waves and to take the heat away from the chip. The space wave coupling is suppressed by vertical CSRR structures, which also create an additional surface for convective cooling. As compared with [19], the radiated fields are trapped in the cavity rather than being reradiated, thus, the pattern is not distorted. Besides, optimal cooling is achieved.

The SRR structures can be modeled as LC circuit that resonates at the characteristic frequency. Conventional SRR structures print the square-shaped metallic resonators on the dielectric structures. In this study, we use a dielectric that is coated with metal on both sides and remove the metal parts in a square resonator shape. Two structures are connected with Babinet's principle, therefore same analysis can be applied. The characteristic frequency of the SRR is given by [23]

$$f_0 = 1/(2\pi\sqrt{L_{\text{net}}C_{\text{net}}}) \quad (1)$$

where $L_{\text{net}}$ and $C_{\text{net}}$ are the total inductance and capacitance introduced by the resonator. These values can be modeled as a function of the resonator circumference, gap distance, and width [23]. On the other hand, the total capacitance is modeled as a function of the dielectric constant, resonator circumference, and characteristic impedance of the line.

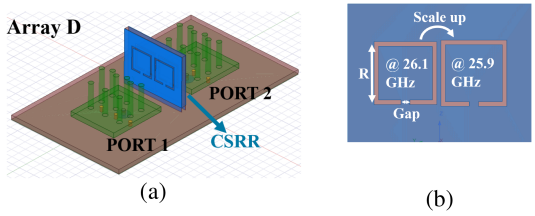


Fig. 5. Heatsink antenna array with CSRR embedded isolation wall (Array D). (a) Isometric view. (b) Side view of the CSRR.

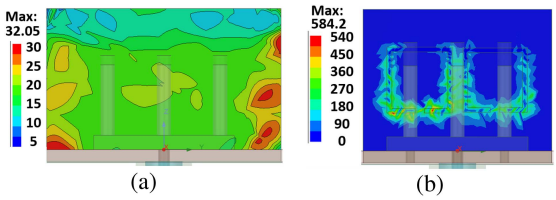


Fig. 6. Current distribution [A/m] on the heatsink antenna array with (a) flat and (b) CSRR-embedded isolation wall.

The resonators derived by using empirical formulas given in the references are tested in the simulation environment. In this test, the unit cell of the resonator is simulated in an infinite array topology, and a plane wave is applied from one side. The resonance point is determined by inspecting the frequency of the minimum signal received from the other side of the surface.

Although the CSRR structure illustrates great isolation between surfaces, it has a very narrow bandwidth. To resolve this problem, two resonators having slightly different sizes are used. The resonators are arranged with scaling to operate at 25.9 and 26.1 GHz to isolate two heatsink antennas resonating at 26 GHz. After designing an isolation wall with CSRR, Array D is formed. The isometric view of Array D and the front view of the CSRR can be seen in Fig. 5. Dimensions of the antennas in Array D are the same as the ones in Array C, while R = 1.37 mm, Gap = 0.2 mm, and a scale factor of 1.01 are selected for CSRR to operate at the 26 GHz.

## V. PERFORMANCE ANALYSIS OF THE PROPOSED ARRAY

The CSRR wall contributes to solving both the cooling and coupling problems. To resolve the electromagnetic-isolation problem, the CSRR structures create resonances that cannot be supported by a flat metallic wall [19]. The induced currents on the flat metallic wall and CSRR wall can be seen in Fig. 6. The CSRR wall induces 20 times more current on it compared with a flat wall. The resonances at the CSRR create a dramatic drop in the coupling between antennas. This can be seen in the reflection coefficient graph illustrated in Fig. 7. Moreover, the junction temperature of Array D configuration is simulated as 124.5 °C. This meets the thermal requirements of the RF electronics for safe operation. The temperature distributions on Arrays C and D surfaces under 1 m/s air inlet velocity condition can be seen in Fig. 8. Although the maximal surface temperature values of Arrays C and D are very close, the junction temperature is

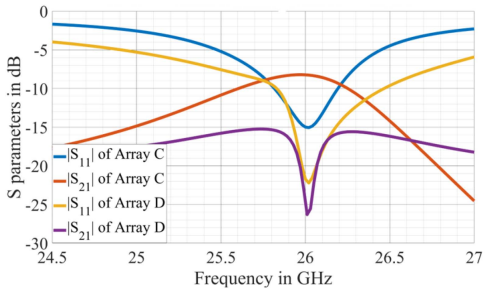


Fig. 7. $|S_{11}|$ and $|S_{21}|$ graphs of the Array C (without CSRR wall) and Array D (with CSRR wall).

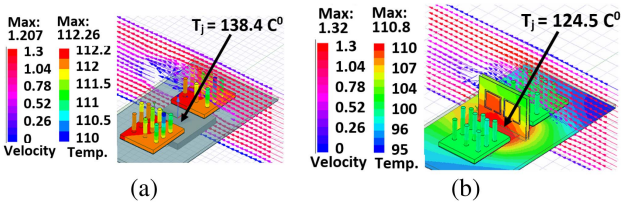


Fig. 8. Surface temperature distribution [°C] and a single cut of air velocity vectors [m/s] on (a) Array C and (b) Array D.

TABLE III
THERMAL-ELECTROMAGNETIC PERFORMANCE OF ARRAY A, B, C, AND D

| Array label | $T_j$ [C°] | BW [MHz] | $\lvert S_{21}\rvert$ [dB] | Active port | Max. realized gain [dB] | Beam scan angle [deg] |
|---|---|---|---|---|---|---|
| Array A | 163.6 | 637 | -16.92 | 1 | 6.56 | 26 |
| | | | | 2 | 6.59 | -26 |
| | | | | Both | 8.23 | 0 |
| Array B | 147.3 | 452 | -12 | 1 | 5.4 | 0 |
| | | | | 2 | 5.41 | 0 |
| | | | | Both | 8.41 | 0 |
| Array C | 138.4 | 451 | -8.12 | 1 | 8.51 | 29 |
| | | | | 2 | 8.18 | -29 |
| | | | | Both | 6.27 | 0 |
| Array D | 124.5 | 570 | -26.2 | 1 | 6.9 | 30 |
| | | | | 2 | 6.88 | -30 |
| | | | | Both | 7.96 | 0 |

reduced by 14 °C due to the low thermal resistance between the CSRR wall and chip.

In addition to the thermal improvement, Array D offers beam switching by altering the active element(s). The radiation pattern of the antenna can be switched to the $\theta = -30°$, $\theta = 0°$, and $\theta = 30°$ in the array plane ($\phi = 0°$ in this simulation). This brings an additional novelty (e.g., in comparison with [19]). Three beam modes corresponding to the use case in Fig. 1 are achieved by operating ports 1 and 2 either independently or simultaneously. Pattern and null switching or cocreation are done without applying any phase difference between elements. Copolarization and crosspolarization radiation patterns of different excitation schemes of Array D are shown in Fig. 9(a) and (b). Note that the cross-polarization patterns are given for the $\phi = 45°$ cut, as we observe the strongest lobe there.

The proposed array forms null at $\theta = -60°$ when Port 1 is active and $\theta = 60°$ when Port 2 is active without using any phase shift or gain control. The comparison between Arrays A–D * in the maximum realized gain, beam direction, $|S_{11}|$ bandwidth, $|S_{21}|$ value at 26 GHz, and junction temperature are given in Table III.

Finally, we studied infinite array simulations that consider the $2 \times 1$ arrays as unit cells and separate this unit cells by $\lambda_0/2$

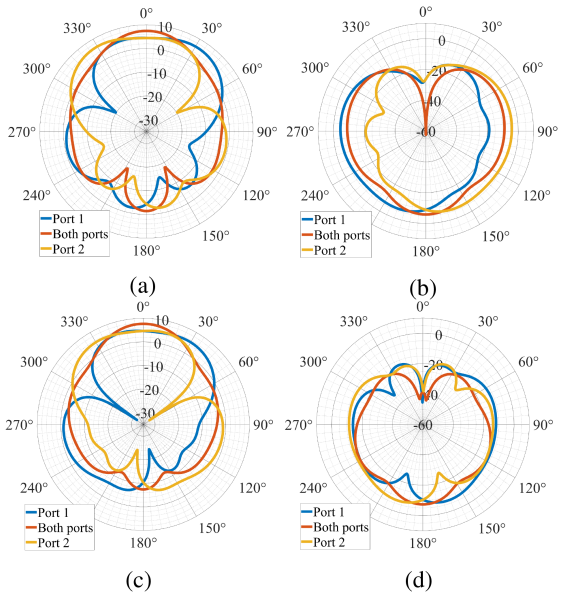


Fig. 9. Radiation pattern of the (a) Array D in $\phi = 0°$ cut under different excitation cases. (b) Cross-polarization patterns of the Array D in $\phi + 45°$ cut for different excitation. (c) Embedded radiation patterns of infinite array simulations for different excitation. (d) Embedded cross-polarization patterns of the infinite array in $\phi + 45°$ cut for different excitation.

on the horizontal axis. Since the port coupling remains below $-20$ dB among the unit cells, there is no need for an additional isolation wall in between the unit cells. The radiation behavior of the infinite array illustrates great resemblance with the unit element in both single port and double port excitations, as seen in Fig. 9(c) and (d). This proves that the unit element is suitable for large-scale base station arrays.

## VI. CONCLUSION

A novel concept on dual-functional CSRR-based electromagnetic-isolation and cooling wall is introduced. An active 26 GHz two-element finned-heatsink antenna unit cell, with the wall in between the elements, is used for demonstration. Through thermal simulations, it is shown that the proposed wall reduces the chip junction temperature by about 15 °C as compared with the no-wall case. As a result, safe chip operation below 125 °C and increased chip lifetime (of more than twice) are achieved. Moreover, the electromagnetic simulations show that the proposed CSRR-embedded wall reduces the port coupling within the unit cell from $-9$ to $-25$ dB around the center frequency. The proposed unit cell also provides simple beam (and null) switching for three operation modes: $-30°$ scan (with a null at 60°), broadside, and 30° scan (with a null at $-60°$) in elevation. With infinite array simulations, its potential for mm-wave base station use under the coexistence of satellites is demonstrated. The future work will focus on the additive manufacturing and experimental evaluation of the concepts.

## ACKNOWLEDGMENT

The authors would like to thank Dr. Kamil Karacuha from the Istanbul Technical University for supplying extensive computational power used in simulations.

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