Thin film encapsulated 1D thermoelectric detector in an IR microspectrometer

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ABSTRACT

A thermopile-based detector array for use in a miniaturized Infrared (IR) spectrometer has been designed and fabricated using CMOS compatible MEMS technology. The emphasis is on the optimal of the detector array at the system level, while considering the thermal design, the dimensional constraints of a design on a chip and the CMOS compatibility. The resolving power is maximized by spacing the Thermo-Electric (TE) elements at an as narrow as possible pitch, which is limited by processing constraints. The large aspect ratio of the TE elements implies a large cross-sectional area between adjacent elements within the array and results in a relatively large lateral heat exchange between micromachined elements by thermal diffusion. This thermal cross-talk is about 10% in case of a gap spacing of 10 μm between elements. Therefore, the detector array should be packaged (and operated) in vacuum in order to reduce the cross-talk due to the air conduction through the gap. Thin film packaging is a solution to achieve an operating air pressure at 1.3 mBar, which reduces the cross-talk to 0.4%. One of other advantages of having low operating pressure is the increased sensitivity of single TE element. An absorber based on an optical interference filter design is also designed and fabricated as an IC compatible post-process on top the detector array. The combination of the use of CMOS compatible materials and processing with high absorbance in 1.5 - 5 μm wavelength range makes a complete on-chip microspectrometer possible.

Keywords: Microspectrometer, Thermopile, IR detector array, Interference IR absorber, Surface micromachining

1. INTRODUCTION

Spectroscopy in the Infrared (IR) spectral range has applications in agriculture, the food industry, soil biology, remote sensing and the chemical industry. Optical microspectrometers based on IC-compatible MEMS technologies offer significant benefits due to: small sample volume, fast response, small dimensions, weight and integrated circuits for signal pre-processing[1]. The structure of the IR microspectrometer discussed in this paper comprises slit, planar imaging diffraction grating and TE detector array[2]. The dispersed IR spectrum is projected onto a 1-dimensional detector array. Therefore, the position of a spectral component within the IR spectrum is determined by the position of the element in the array. The response in terms of generated heat due to absorbed IR radiation at that particular element is a measure of the optical power within that part of the spectrum. The resulting localized increase in temperature is available as temperature difference relative to ambient temperature, which can conveniently be measured directly using a thermopile between the suspended absorber and the bulk silicon. The characteristic feature of a thermocouple of measuring temperature difference rather than temperature makes the integrated system insensitive to variations in the temperature of the bulk of the chip. Micromachining technologies are generally employed for the removal of the thermal shunt of any bulk silicon or oxide underneath the TE detector for maximum sensitivity. These techniques and their effect on the sensitivity of IR detectors have been extensively studied[3].

Micromachining technologies are mainly divided into two categories: bulk and surface micromachining. Wafers are subjected to a CMOS process and are subsequently etched from either front or backside of substrate to realize free-standing MEMS structure in bulk micromachining. The chemical etchant often utilized in the backside etching is KOH. The device has free spacing to the end of substrate in the vertical direction. This backside etching is an advantage for fabrication of thermally isolated on-chip devices. However, the long etching time is needed due to the thick substrate. Another issue is that a large footprint is unavoidable due to the anisotropic etching of KOH along a crystal plane. The disadvantage is avoided in surface micromachining. The shorter etching time makes this technique suitable for realizing inertial sensors (e.g. accelerometer or gyroscope) for the mass production application.

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Optical Sensing and Detection, edited by Francis Berghmans, Anna Grazia Mignani, Chris A. van Hoof,
Proc. of SPIE Vol. 7726, 772612 · © 2010 SPIE · CCC code: 0277-786X/10/$18 · doi: 10.1117/12.854182

However, the narrow gap between the MEMS structure and the substrate significantly decreases the performance of thermal sensor, because of the increased air conduction. The resulting heat loss greatly decreases sensor performance. As a result, most MEMS-based thermal sensors are realized using bulk micromachining.

This paper reports on an IR thermal detector array fabricated using a CMOS compatible MEMS process using surface micromachining with subsequent encapsulation by thin film technology. A technique for thin film encapsulation is applied to achieve low pressure inside the array cavity, which hugely reduces thermal diffusion cross the air gap to heat sink[4]. The advantages of surface micromachining as compared to bulk micromachining are amongst others: a reduced process complexity and reduces etching time, during which the already integrated microelectronic devices should be protected. The thermal cross-talk analysis is presented in section 2 and shows it is reduced to 0.4% due to the low pressure inside the cavity. Polysilicon (PolySi) is selected as the thermoelectric material for reasons of CMOS compatibility. Although neither PolySi nor Silicon Nitride (SiN), which is used as support structure, absorb IR in the 1.5 - 5 μm wavelength range, a thin-film PolySi/SiN based interference filter has been designed and fabricated to act as efficient IR absorber to improve the IR absorptance. This part of the detector is described in section 3. The simulation result shows that more than 80% of IR is absorbed.

2. CROSS-TALK REDUCTION BY THIN FILM ENCAPSULATION

2.1 Background

Conduction, convection and radiation are the three mechanisms of loss in thermal and IR thermal sensor. The thermal transfer due to these three mechanisms acting on the TE element is described in detail in literature[5]. An array of 26 TE elements, each on a bridge structure of 650×36 μm^2 is designed and fabricated. The volume around an element is small and the effect of gas pressure on the performance of detector has to be considered. The gas conductivity determines the residual thermal cross-talk and, consequently, the lower limit of what can actually be achieved by the optimised design of the support structure and the structural separation of the elements. For typical MEMS-based detectors the expression for thermal conductivity of air between two plates within an enclosed cavity as a function of pressure and temperature can be approximated as:

$$\kappa_{air} = \kappa_o \times \frac{1}{1 + \frac{7.6\times10^{-5}}{p \times \frac{D}{T_{avg}}}}. \qquad (1)$$

where κ_o, p, D, T_{avg} denote: the thermal conductivity of air at room pressure and temperature, the pressure, the distance between the plates and the average temperature of the plates respectively. When assuming a plate spacing of 10 μm, an average temperature of 300K and κ_o= 0.0284 Wm^{-1}K^{-1}, a pressure-dependent thermal conductivity of air results, which is about equal to κ_o at 1 Bar and becomes negligible for pressures below about 1 mBar.

Several layers are stacked during fabrication of the meander-shaped thermopile deposited on top of supporting membrane. This is a 2-dimensional problem with heat flux between several objects. Therefore, numerical methods are required. The commercially available Finite Element Method (FEM) software, COMSOL[6] has been used to solve the heat transfer equation. One element is given the constant heat flux in the middle position (the absorption area) of the bridge to create the temperature difference between the absorber to the bulk silicon where the temperature is constant. The temperature difference of the thermopile sensing area of the heated element is taken as the reference, while the temperature difference of two successive neighboring elements indicates the cross-talk. The simulation result of cross-talk as a function of pressure, while assuming a constant ambient temperature at 300K indicate an overall cross-talk at air pressure of 10%. In case the device is operated at 0.1 mBar pressure, the cross-talk is reduced to 0.4%. The thin film encapsulation technology is applied with PECVD technology, which has the process chamber pressure around 0.1 mBar.

2.2 Fabrication of encapsulated TE device

The fabrication was done in DIMES facility of TUDelft and the process sequence is shown simplified in Fig. 1. Wafer processing started with 4 μm PECVD TEOS as the sacrificial layer followed by 700 nm of low stress SiN film formation. Firstly, a 300 nm low-stress PolySi layer was grown by LPCVD. Secondly, Boron was implanted at 40 keV and 5×10^{15}/cm^2 to realize p-type PolySi. After cleaning procedure, n-type Poly-Si was formed by Phosphorous doping

(40 keV and $7.5\times10^{15}/cm^2$). Thirdly, Reactive Ion Etching was applied to remove PolySi from the backside and unwanted PolySi from the front side. In the next step, 100 nm low-stress SiN was deposited by LPCVD to make the isolation between metal contacts and Poly-Si. Aluminium was deposited and patterned on top to define connection of thermocouples. The following steps are dedicated for the thin film encapsulation. Another 4 µm TEOS is deposited and patterned as a second sacrificial layer followed by Silicon Carbide (SiC) layer deposition. The wafer is processed in high concentrated HF solution to release the structure. Finally, the wafer is sealed to form low pressure inside the small cavity.

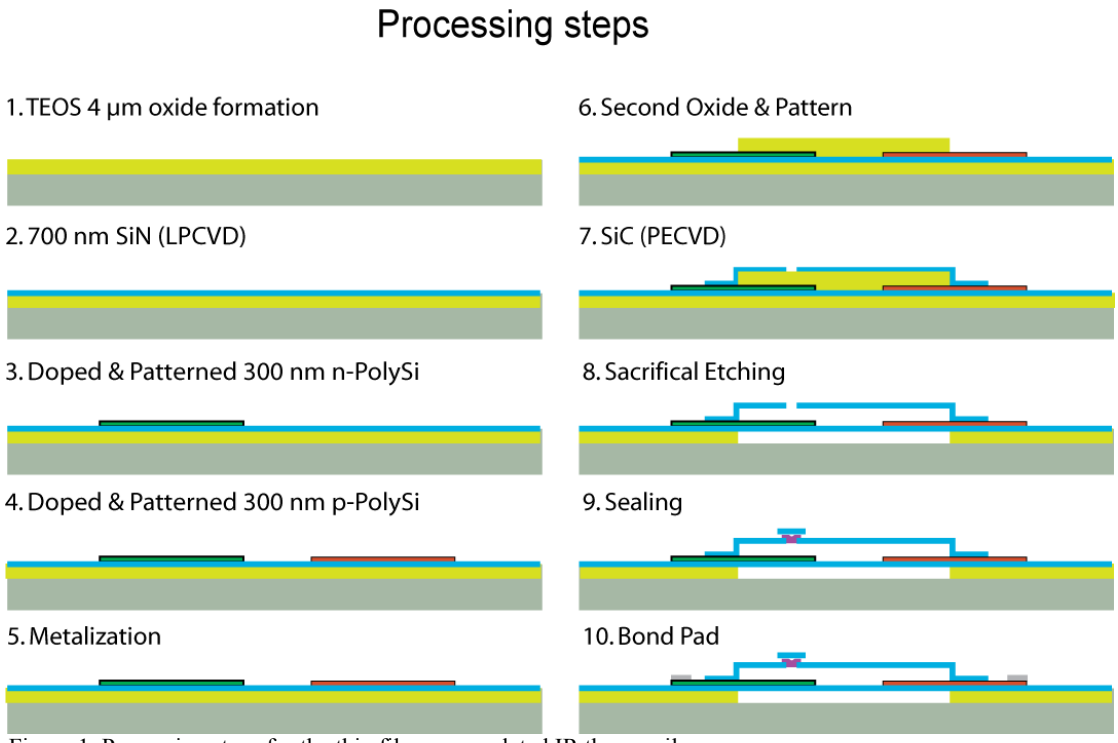

Figure 1. Processing steps for the thin film encapsulated IR thermopile array.

3. INTERFERENCE BASED IR ABSORBER

3.1 Introduction

The sensitivity of the thermal detector critically depends on the absorber, which determines the efficiency in which impinging IR radiant flux is converted into localised heat at the hot junction. Traditional IC-compatible materials, such as Si, SiO_2 and SiN, are not efficient absorbers in the near-IR spectral range. Therefore, alternative absorbing coatings with opportunities for IC-compatible deposition have been investigated. Thin-film metals and polymers are within this category. Consequently, black polymer absorbers or black (porous) gold[7] or silver layers have been used in thermopile detectors for absorption of IR radiation.

Black polymer materials introduce too much stress in the 36 µm wide bridges in the thermopile array. Black gold and silver are marginally IC-compatible materials, since these introduce significant process complications. The use of interference absorbers for IR have been theoretically proposed and practically verified in previous works[8-9]. However, the concept has not been implemented in a surface micromachined thermopile array. Figure 2 shows the processing steps for the fabrication of interference absorbers on TE elements. Interference absorbers include two Ti layers with a dielectric spacing. A SiC layer deposited on top of the metallic based absorber protects these layers in the subsequent sacrificial etching step.

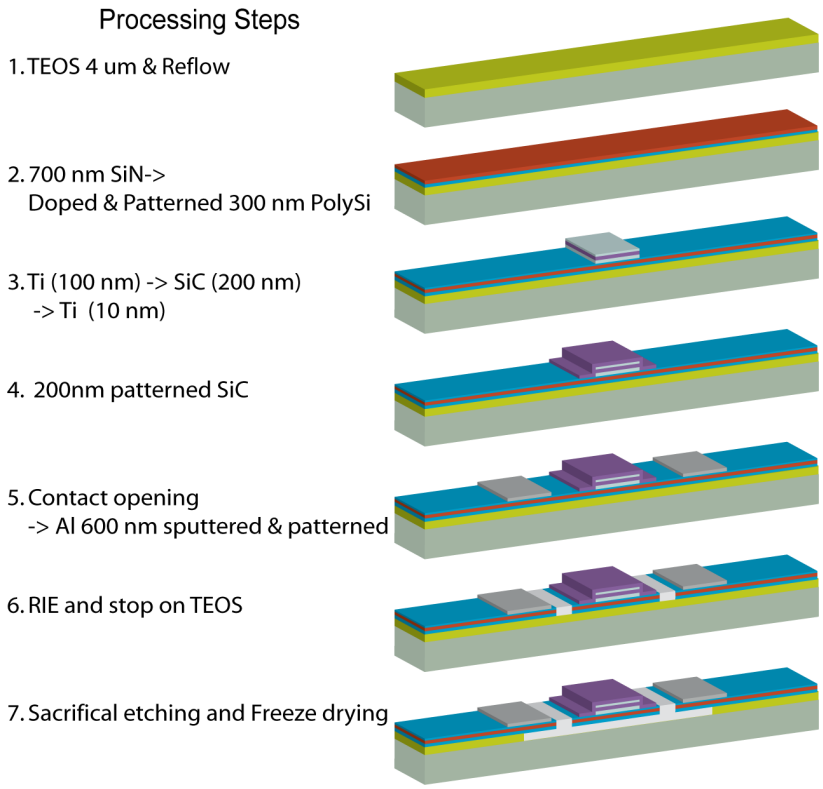

Figure 2. Processing steps for IR absorber on single TE element (thermopile is not illustrated).

The interference absorber consists of a thick Ti layer, a dielectric cavity layer and a thin Ti layer. Another dielectric layer is deposited on top of the 3-layered interference filter to protect the layers during the sacrificial etching step. SiC is preferred to SiN for this purpose, because of the good resistance during high concentration HF etching and acceptable optical properties in the IR. As it is shown at step 6 in Fig. 2, the protective layer is covering the area of absorber layers. In the mask, the protective layer is designed to overlap the absorber area 2 μm out of it. Al is sputtered to make contacts before the sacrificial etching. Since Al is unprotected, high concentration HF is used for sacrificial etching, which etches Al very slowly, rather than BHF[10-11]. RIE is used to separate the bridge structures as shown in step 8 followed by sacrificial etching. Freeze drying is performed to avoid stiction of the released structures.

3.2 Design of the absorber

The thin-film optical software package TFCalc 3.3 has been used to simulate and design the interference based absorbers. Ti is chosen as the metallic layer of the absorber. The optical properties of Ti are measured using ellipsometry on a test sample. Optical properties were measured up to 1.2 μm wavelength by ellipsometry. The absorber consists of one dielectric centre layer with thin-film Ti layers on either side. PECVD SiC has been used as the dielectric spacing layer. SiC is to be preferred because of the high resistance to HF etching. Another advantage of using SiC for the spacing layer is the decreased process complexity, since it is also used for the protective coating. Prior to the design, the optical properties of PECVD SiC have been measured by ellipsometry. Figure 3 shows the measured optical properties of PECVD SiC, which are in agreement with the values reported in literature[12].

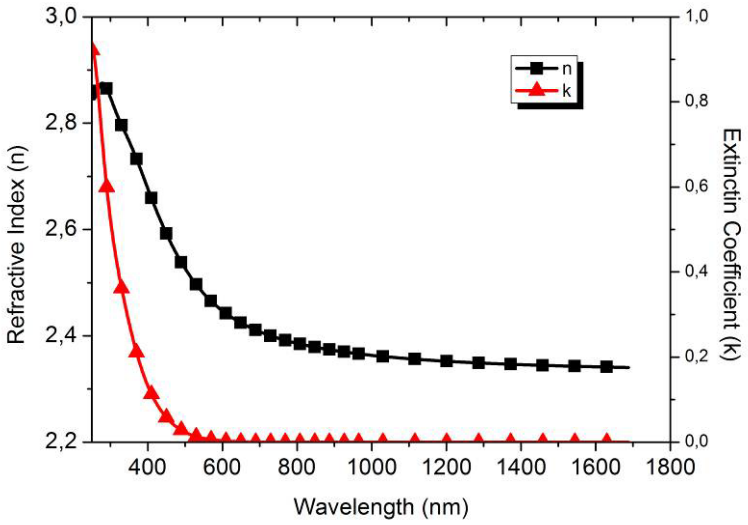

Figure 3. Measured optical properties of PECVD SiC.

The Ti (100 nm)/SiC (200 nm)/Ti (30 nm) three stacks interference absorber with additional SiC (200 nm) protective layer are purposed. It results a 4-layered Ti/SiC/Ti/SiC stack as the IR absorber. Optimal absorber design on the layer thickness is achieved in Fig. 4 by also taking the bridge layers into account. The relatively high absorptance covers from 1.5 μm to 5 μm wavelength range. This wide spectral range could be applied to some targets for gas spectroscopy application.

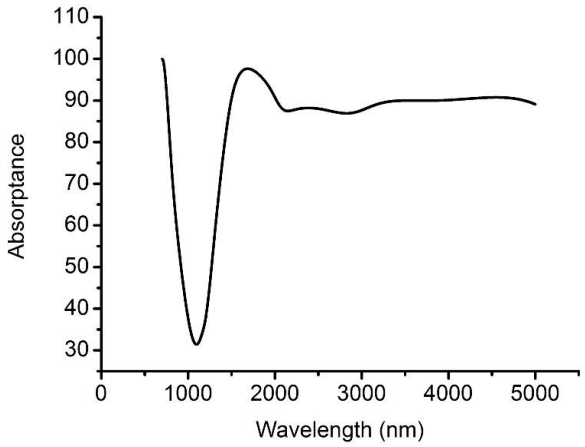

Figure 4. Simulation result of optimum design of IR absorber on Ti /SiC stacks.

3.3 Fabrication of the absorber

The fabrication of thermopile detector array starts with a 4 μm PECVD TEOS as the sacrificial layer. The process used for the fabrication of the uncoated TE elements has been described in detail in previous work[2]. This section is focused on the fabrication of absorber and realizing of bridge structure. The CMOS compatible bridge fabrication stops at the second SiN layer and is followed by deposition of the layer stack used for the absorber. The contact hole etching and metalization are completed prior to sacrificial etching. The process steps for the absorber are: The first 100 nm Ti is sputtered followed by the patterning step to define the thin film in the middle position of the bridge. SiC with 200 nm thickness is deposited with PECVD process. Next, the second 30 nm Ti is sputtered and patterned on top of SiC layer. Second 200 nm SiC is deposited on top of layers to form SiC/Ti/SiC/Ti four-layer stacks. Two SiC layered are etched and patterned, followed by contact hole and metallization process. Reactive ion etching is implemented in a final step to form the bridges in the detector array out of membrane. The fabricated device before sacrificial release is shown in Fig.

5(a). This zoom-in figure shows the absorber and part of the thermocouples. Excess under etch is found at the rim of absorber and is indicated by the color difference. The Scanning electron microscope (SEM) photo has been taken to show the cross section of absorber in Fig. 5(b). Two Ti layers together with a 200 nm SiC layer forms a sandwich structure. The thickness of the upper SiC layer is below the target design value and fails to act as protection layer. The insufficient coverage by the protection layer is examined at the sidewall. As a result underetching is observed at the rim of the absorber, due to partly removal of the thin Ti layer.

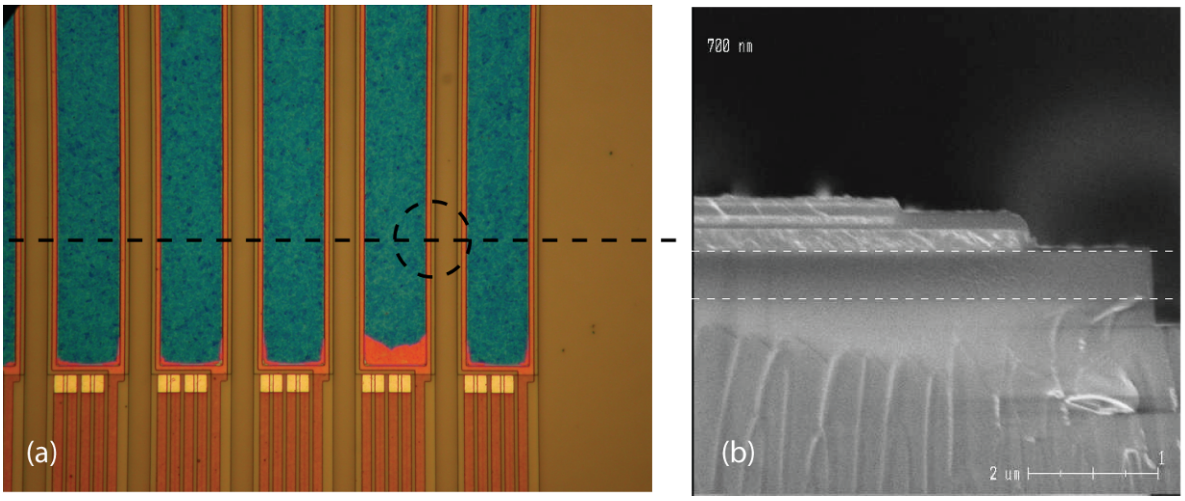

Figure 5. (a) Zoom-in photo of fabricated detector array with absorber stack. (b) SEM of cross-section of bridge before structural release.

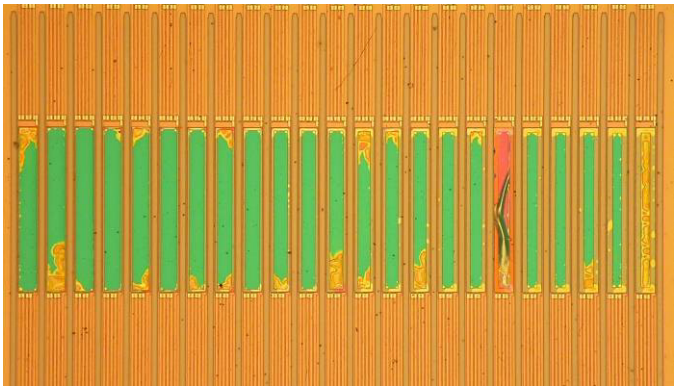

Figure 6. A photograph of the fabricated TE array.

Sacrificial etching is performed to realize structures with reduced thermal diffusion in the direction normal to the plane in which the TE elements are integrated (i.e. vertical). The width of a bridge is 36 μm with spacing of 10 μm. HF at 73% was used as the etchant due to the relatively slow etch rate of aluminium. The etch rate is determined by initial tests and was found to be 1740 nm per minute. The total etching time is set to 10 min and 30 sec by considering the etching rate and the width of the bridge. After that the die is rinsed in IPA for several times to remove HF. To prepare for freeze drying, the die is immersed in Cyclohexane solution for 10 minutes. Freeze drying is performed to avoid stiction of the released structures. Figure 6 shows a photograph of fabricated and free standing TE array. The photo clearly shows the color difference compared to the array before sacrificial etching. The device was analyzed and verified with SEM. The top SiC layer is floating, since the thin Ti layer underneath is removed during etching. Consequently, the absorber is incomplete after the sacrificial etching.

3.4 Measurements

The measurement of device from section 2 has not been achieved due to the side wall and pin holes problems. Instead, thin-film SiC(200 nm or 100 nm)/Ti (10 nm)/SiC (200nm)/Ti (100 nm) absorber layers have been deposited by

sputtering on two different silicon wafers. A LAMBDA 950 spectrophotometer has been used for the measurement. The reflectance from the wafers and transmission through the wafers have been measured. Transmission through the wafers is measured to be negligible for all the wafers and the absorptance can be easily calculated. Figure 7 shows the comparison between the simulation and reflectance measurements. These are in reasonable agreement, hence, the experiments validate the simulation results. Considering the non-zero throughput in the stack, absorptance is calculated and shown in Fig. 8.

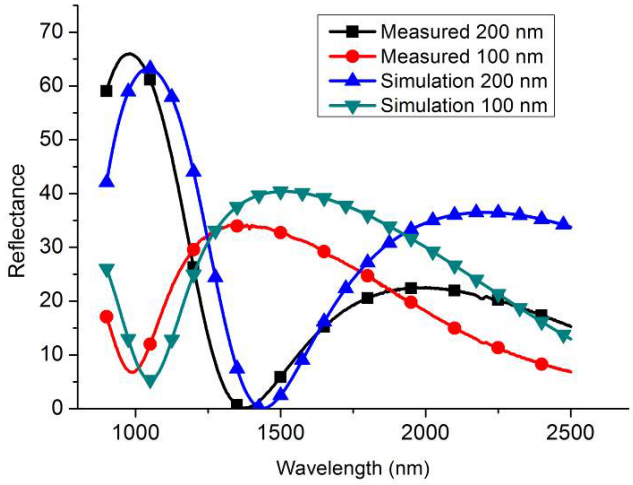

Figure 7. Comparison between the measured and simulated reflectance for SiC-based interference filters.

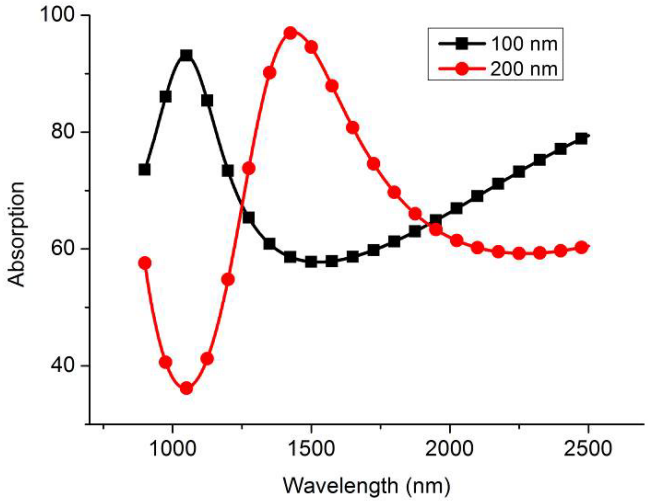

Figure 8. Measured absorptance of SiC-based interference absorbers.

4. CONCLUSIONS

A good solution to achieve high sensitivity MEMS-based thermopile detector array for use in a miniaturised IR microspectrometer is presented. The 1D dimension of the thermopile detector array is dictated by the optical properties of the imaging grating. As a result, the design and fabrication of TE device is implemented in terms of design constraints and technology aspect. Thin film encapsulation process and interference-based IR absorber are proposed to improve the performance of a CMOS compatible MEMS thermopile array. Thin film encapsulation technology is implemented to

reduce the pressure of cavity of device which results the minimum cross-talk between TE elements and to improve sensitivity. The cross-talk of array is estimated to be reduced from 10% to 0.4% due to the low pressure inside cavity (1m Bar). The second aspect is to design and fabricate the CMOS compatible interference filter based absorbers on single TE element of detector array. SiC has been used as the spacing layer in the interference absorbers stacks, together with Ti to form the sandwich structure. SiC is relatively resistant to HF etching compared to SiO_2. However, side wall and pin holes issues are addressed and needed to be taken into account during design phase. The experiments validate the simulations, which implies that the simulation tools and our material data can be used in future designs. Thin film encapsulation process and interference-based IR absorber can be combined and integrated into fabrication process since the requirements of CMOS compatibility are achieved.

ACKNOWLEDGEMENTS

This work has been supported in part by the Dutch technology foundation STW under grant DET.6667. Devices have been fabricated at the DIMES (Delft Institute of Microsystems and Nanoelectronics). The authors are indebted to W. van der Vlist and V. Rajaraman for their assistance in device fabrication, to J. Wingerden for acquiring the SEM image and to Prof. P. M. Sarro for helpful discussions on the processing.

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