A Subthreshold Source-Coupled Logic based Time-Domain Comparator for SAR ADC based Cardiac Front-Ends

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A Subthreshold Source-Coupled Logic based Time-Domain Comparator for SAR ADC based Cardiac Front-Ends

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***Abstract*—Low-voltage and low-power front-end design is required for the safe and long-term monitoring of cardiac signals. To address the low-voltage challenge, this paper presents a subthreshold source-coupled logic (STSCL) based time-domain comparator designed in 180 nm CMOS process technology. At a low supply voltage of 0.8 V, the STSCL time-domain comparator consumes 2.3 μW at 1 MHz. Using 4 stages, the input referred noise and the offset of the comparator are 32 μVrms and 1.8 mV, respectively.**

***Index Terms*—time-domain comparator, source-coupled logic, low-voltage, biosignal acquisition**

I. Introduction

For the early diagnosis of cardiac abnormalities and long-term monitoring of the heart [1], compact and portable cardiac analog front-ends which operate at a low voltage and consume little power are required. Fig 1 shows the system-level block diagram of a cardiac front-end which consists of a flexible electrode array and an electronic module for signal recording. For analog front-ends (AFE) that depend on an energy harvester for deriving power from ambient sources, both the supply voltage and the power consumption are required to be as low as possible.

A fundamental block in the AFE is the analog-to-digital converter (ADC) which converts analog signals to the digital domain for further processing. Successive approximation register (SAR) ADCs are a preferable choice for bio-signal acquisition for their low power consumption and resolution and consists of a sample and hold block, a comparator, a digital-to-analog converter and necessary logic as shown in Fig 1. The comparator, the main component of a SAR ADC, is designed to meet the speed, noise and energy efficiency requirements of the ADC.

Taking advantage of technology scaling, digital circuit design has achieved improvements in power, speed and cost, while analog and mixed-signal design has become a challenge due to the fact that threshold voltages of the devices have not scaled down at the same pace as the supply voltage. To be compatible with the rest of the circuitry, the design of a high-speed comparator for operation from a low supply voltage is a challenge. One of the approaches is to employ digitally-assisted analog/mixed-signal design, which tolerates less precision in the front-end and then recovers the accuracy

†S. Rout and S. Babayan-Mashhadi contributed equally to this work.

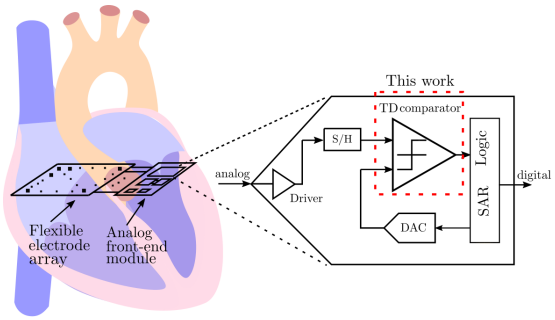


Fig. 1: System-level block diagram of a cardiac front-end

(and performance) in the digital domain. Despite the effectiveness of this approach, employing digital calibration methods often results in increased circuit complexity, die area of the chip and total power consumption. Conventionally, voltage-domain comparators have been used due to their high speed and energy efficiency [2]. However, at low supply voltages, the performance of voltage-domain comparators is degraded. While the supply voltage scales down, the circuit noise stays the same [3]. In order to maintain the performance of the circuit, complex calibration or correction methods may need to be employed.

As an alternative approach, time-domain can be used to represent and process the signals. Technology scaling and the focus on high-performance digital systems offers better time resolution by reducing the gate delay. Therefore, if we represent a signal as a period of time, rather than as a voltage, we can potentially reduce power consumption and die area [3]. Time domain comparators have been proposed [3]- [6] as an alternative to voltage domain comparators and they operate at lower supply voltages.

In this paper, we present a time-domain comparator based on subthreshold source-coupled logic (STSCL) which is designed to operate at 0.8 V at a speed of 1 MHz and consumes less than 2.3 μW power, making it a strong candidate for low voltage and low power bio-signal acquisition multi-channel front-ends.

The rest of the paper is organized as follows. Section II presents the proposed architecture of the STSCL based time-domain comparator. Section III describes the circuit implementation. Section IV presents the design considerations while the

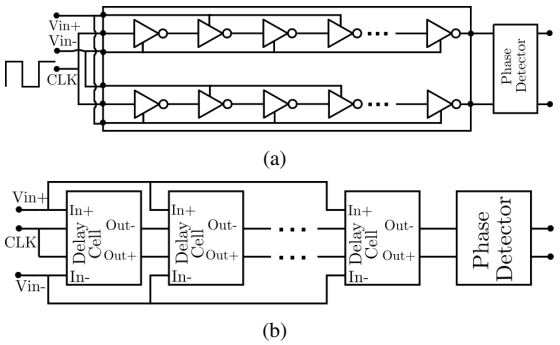


Fig. 2: (a) Conventional TD topology; (b) Proposed TD topology.

simulation results are presented in Section V. Finally, Section VI summarizes conclusions.

II. Time-domain comparators

Fig. 2 shows the concept of time-domain comparators. The delay lines convert the input voltages to pulses in the time domain. A phase detector compares the delay times and outputs the time difference. The following subsections describe the operation of a conventional voltage-controlled delay line (VCDL) and propose a subthreshold source-coupled logic (STSCL) based time-domain comparator.

A. VCDL-based time-domain comparators

In [3], [5], the voltage-to-time (V-T) conversion is performed by two separate V-T converters as shown in Fig 2(a), which controls the capacitor charging/discharging rate as a function of the input voltages $Vin+$ and $Vin-$, and the time difference is sensed by a delay flip-flop (DFF) based phase detector (PD). The multiple-stage VCDL [3] provides a high gain and thus reduces the effect of offset and noise. However, at low supply voltages, the comparator performance degrades in terms of speed. At low supply voltages, the comparator needs higher current to maintain the speed of operation, which leads to higher power consumption. A possible solution is to increase the size of transistors, which would lead to an increase in parasitic capacitances. In addition to this, the comparator operation is sensitive to the setup/hold uncertainties of the DFF based PD [3]. As the design uses conventional CMOS delay logic lines, the performance deteriorates at low supply voltages. To mitigate the design challenges in conventional CMOS logic, we propose a time-domain comparator which makes use of subthreshold source-coupled logic with very low bias currents resulting in a low-voltage time-domain comparator architecture with improved power efficiency.

B. Proposed STSCL based time-domain comparator

As opposed to conventional time-domain comparators that use two separate VCDL chains, in the STSCL-DL topology, the CLK signal propagates through a single STSCL-DL chain consisting of multiple delay cells. Figs. 2(b) and 3 show the schematic of the proposed comparator based on STSCL delay cell and a DFF based phase detector (PD). In the delay lines,

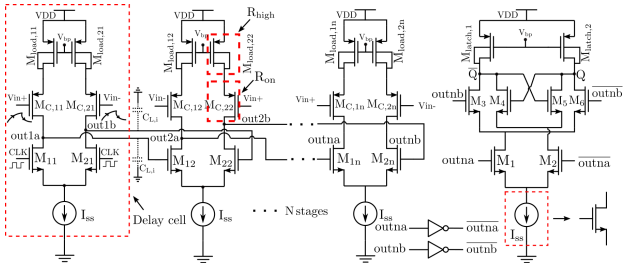


Fig. 3: Proposed STSCL time-domain comaparator

the rise-time and the fall-time of the propagating CLK signal are set alternatively by two analog input voltages $Vin+$ and $Vin-$. The latch compares the time delays that correspond to the input voltages. The number of cascaded stages denoted by N depends on the required voltage to time conversion gain to achieve the desired offset, noise and accuracy performance.

III. Circuit implementation

The STSCL time-domain comparator operates in two phases: the reset and the comparison phase. Fig. 3 shows the circuit schematic of the STSCL-DL comparator. During the reset phase, when $CLK = 0$, the delay cells reset the outputs of the first stage and the subsequent odd stages to V_{DD}. The second stage and the subsequent even stages are reset to ground. The DFF is also reset to clear the decision from the previous comparison. During the comparison phase, when $CLK = 1$, the CLK signal at the input of the NMOS transistors propagates through the chain from the two sets of branches, one through the left half of the delay cells, and the other through the right half of the delay cells. As a proof of concept, we have chosen $N = 4$, which meets the gain and the noise requirements of a SAR ADC designed for 8 bits. However, an optimization on the number of stages can be done to improve the efficiency of the comparator depending on the application.

In the first stage, NMOS-transisitors M_{11} and M_{12} are turned ON. Two currents corresponding to $Vin+$ and $Vin-$ respectively, flow through the branches and drive nodes out1a and out1b to ground potential. The discharging time constant for the output voltage is given by $C_{L,i}$, which refers to the parasitic capacitance at the i_{th} output and the total resistance (R_{high}+R_{on}), where R_{high} is implemented as described in [4]. In the second stage, the outputs are charged to V_{DD} where the charging time constants of the output voltage is determined by $Vin-$. The outputs of the last stage are charged to V_{DD} and are connected to the phase detector. The charging time constant of the last stage is different and the time difference Δt is detected by the phase detector, a DFF.

In the STSCL-DL time-domain comparator, the time delay $t_{delay,i}$ of the i^{th} delay cell can be approximated as:

$$t_{delay,i} = ln(2).C_{L,i}(R_{on,C1n} + R_{High}) \quad (1)$$

where, $R_{on,C1n}$ (or $R_{on,C2n}$) and R_{high} are the equivalent ON resistances of the control input transistors ($M_{C,1n}$ & $M_{C,2n}$) and the load transistors ($M_{load,1n}$ and $M_{load,2n}$).

Depending on the input voltage difference (ΔV_{in}), the time difference between two outputs in one delay cell, for an output swing of V_{DD}/2 , can be obtained from the following equation:

$$t_{d-diff} = ln(2).\Delta R_L C_{L,i} = ln2.\frac{V_{SW}}{\Delta I_L}.C_{L,i}$$
$$\cong \frac{2.ln(2).C_{L,i}V_{DD}g_{mC}}{I_{ss}^2}\Delta V_{in} \quad (2)$$

In 2, g_{mC} refers to the transconductance of the input control transistors and I_D is equal to $I_{ss}/2$. For N stages, the gain of a V-T converter is given by:

$$Gain_N = N.\frac{t_{d-diff}}{\Delta V_{in}} = N.\frac{2ln(2)C_{L,i}V_{DD}g_{mC}}{I_{ss}^2} \quad (3)$$

IV. Design Considerations

In this Section, the performance metrics, namely, offset and noise, are theoretically derived and discussed.

A. Offset voltage

In designing the STSCL time-domain comparator, there are some considerations that should be taken into account while determining the size of the transistors and the number of stages. Any mismatch in the differential pair of transistors in the delay cells will result in different current flowing through the branches with different charging/discharging times. Using simple calculations, we observe that the resulting timing error due to the offset ΔV_{os} for one stage can be obtained as follows,

$$\Delta t_{d,os} = \frac{2C_L\Delta V_{os}g_{mC}V_{DD}}{I_{ss}^2} \quad (4)$$

Since the final output is a result of the uncorrelated random offsets from every delay cell, the standard deviation of the offset due to the N stages, $\Delta t_{d,osN}$ can be written as, $\Delta t_{d,osN} = \sqrt{N}\Delta t_{d,os}$. The input-referred offset voltage, $\Delta V_{os,N}$ can be written as,

$$\Delta V_{N,os} = \frac{\Delta t_{d,osN}}{Gain_N} = \frac{1}{\sqrt{N}}\Delta V_{os} \quad (5)$$

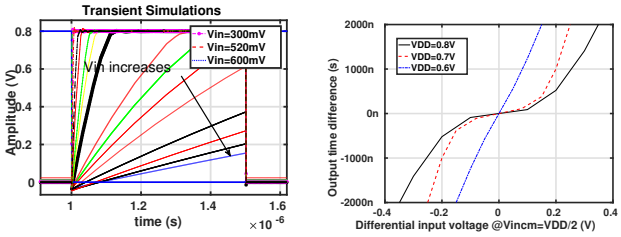
From 5, we can observe that the number of stages can be chosen based on the accuracy required for the ADC in which the TD comparator is employed. Besides, to achieve the least ΔV_{os}, transistor dimensions of input pairs should be carefully designed.

B. Noise

In the design of the proposed comparator, a clock drives the input transistors, which generates thermal noise due to switching, limiting the performance. Assuming a constant slew-rate in signal transitions, kT/C noise can be translated to a timing-error according to the following equation,

$$\overline{\Delta t_{d,noise}} = \frac{\overline{\Delta V_{out,noise}}}{SR} = \frac{ln(2)C_{L,i}}{I_{SS}}\overline{\Delta V_{out,noise}} \quad (6)$$

where $\Delta V_{out,noise}$ is the RMS output noise voltage and t_{delay} is the delay time, during which each output voltage changes about half of V_{DD} and is defined by the value of the delay cell



(a) (b)

Fig. 4: (a) Delay cell output with varying V_{in}; (b) Δt vs ΔV_{in}.

output parasitic capacitance ($C_{L,i}$) and the main current source (I_{SS}). In calculating the total input-referred noise voltage $\Delta V_{in,noise}$, since the effect of noise from every delay stage which is statistically independent of each other are considered, the standard deviation of the timing error due to N-stages given by $\Delta t_{dN,noise}$, and hence, $\Delta V_{in,noise}$ is given by,

$$\overline{\Delta V_{in,noise}} = \frac{\sqrt{N}\Delta t_{dN,noise}}{Gain_N} = \frac{ln(2)I_{ss,avg}\overline{\Delta V_{out,noise}}}{\sqrt{N}(V_{DD}/2)g_{mC}} \quad (7)$$

It can be seen that the number of stages play an important role in reducing the effect of kT/C noise. Also, the dimensions of the control transistors which directly affects the g_{mC}, $C_{L,i}$ and the average current should carefully be determined.

V. Simulation Results

The proposed comparator is designed and simulated in 0.18μm CMOS technology at a supply voltage of 0.8 V. First, the operation of each delay cell is verified. In the source-coupled delay cell, the input voltages influence both the charging and the discharging time constants of the output node voltages. Fig. 4(a) shows the transient simulation of one of the outputs (e.g out1a) for different input voltages. It is evident that during the time that clock (CLK) is zero, each output of the delay cell starts charging with a time constant depending on the sum of the ON resistances of load and control transistors (e.g., M_{load1} and M_{C1}) and the value of the output capacitor. For lower input voltages, the control transistors have larger gate-source voltages, resulting in lower ON resistances and consequently smaller time constants. So the outputs charges fast. However, as we increase the input voltage (for Vin = 600 mV), the time constant can become so large so that the signal cannot reach the desired value within the half clock period. This fact should be considered while determining the dimensions of the relevant PMOS transistors. As different inputs are applied to the delay cell (see Eq. 3), the output voltages charge/discharge with different time constants, resulting in a gain of V-to-T.

Fig. 4(b) demonstrates the time difference between two outputs of one delay cell (Δt), for different values of differential input voltages (ΔVin) for different supply voltages. The sensitivity of the TD comparator increases with increase in ΔVin. At V_{DD}=0.8 V, a differential input voltage of ΔVin = 10 mV results in Δt of 10 ns. Thus, depending on the required comparator gain (to achieve a certain accuracy), the number

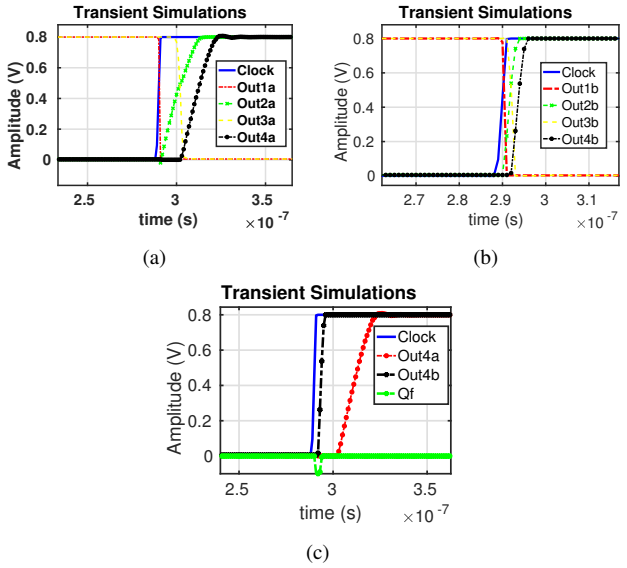


Fig. 5: Transient simulations for the proposed TD comparator for Vcmin=0.4 V and ΔVin=-100 mV, VDD=0.8 V.)

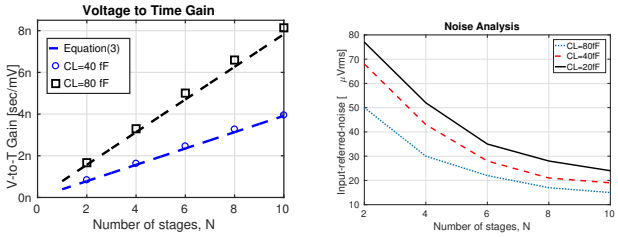


Fig. 6: (a) Simulated gain of V-to-T; (b) Comparator $V_{in,rms}$ vs. N

TABLE I: Performance summary of the STSCL TD comparator

Technology	180 nm
Supply	0.8 V
Energy/conv.	8.5 fJ @ fs=1 MHz
Δt @ ΔVin=1 mV	55 ns
V-T gain @ N=4	1.8 ns/mV
Offset σ @ N=4	1.85 mV
Noise $V_{in,rms}$	32 μV (BW=1 MHz)
Worst case Δt	42 ns @ SS, T=90°C

of cascading delay stages can be determined. For instance, in a SAR ADC with 8 bit resolution, for a sampling frequency of 100 KS/s and V_{DD}= 0.8 V, the least-significant bit is about 3 mV and each bit should be detected with 1 μs.

Figs. 5(a)-5(c) illustrate the transient simulations of the comparator for ΔVin=-100 mV. Clock signal is propagating through two parallel paths, the left-half and the right-half of the source-coupled delay cells, respectively. Input transistors control the time constants of the charging/discharging of the output nodes. Finally, the outputs of the last delay cell are applied to a PD to determine the comparator output. In this case, since $Vin+$ is less than $Vin-$, out4a goes high later than out4b which is applied to the clock of the DFF, so Qf is zero (see Fig 5(c)). Alternatively, for $Vin+$ larger than $Vin-$, out4a goes high earlier than out4b, so when DFF clock goes high, out4a is transferred to Qf which is V_{DD}.

Fig. 6(a) demonstrates the V-to-T gain for four-stage TD comparator. The simulation results are compared with the theoretical expression given by 3 for two different load capacitors. As expected, the cascaded stages provide gain for pre-amplification and improve the minimum resolvable voltage difference by simply increasing the number of stages or capacitance. To verify the noise performance, the proposed comparator is simulated for different load capacitors. Fig. 6(b) shows simulated input-referred noise voltage. As expected from the expressions 6 and 7, the effect of noise decreases as the number of stages or the load capacitance increases.

VI. Conclusions

A subthreshold source-coupled-logic based time-domain comparator for SAR ADC based low-voltage cardiac front-ends is presented. With a single multi-stage voltage-controlled delay line architecture, the proposed time-domain comparator eliminates the need for matching, as is done in differential VCDL CMOS-based architectures. To verify the functionality of the proposed design, an STSCL TD comparator is designed and simulated in 180 nm CMOS technology and analyzed in different process corners. The performance of the designed comparator is summarized in Table I. A power efficiency of 8.5 fJ per conversion (for 8-bit resolution) has been achieved at a frequency of 1 MHz for a supply voltage of 0.8 V. The performance of the proposed time-domain comparator guarantees proper operation under low supply voltage regime as an alternative to the voltage domain comparators.

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