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Read-disturb Detection Methodology for RRAM-based Computation-in-Memory Architecture

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***Abstract*—Resistive random access memory (RRAM) based computation-in-memory (CIM) architectures can meet the unprecedented energy efficiency requirements to execute AI algorithms directly on edge devices. However, the read-disturb problem associated with these architectures can lead to accumulated computational errors. To achieve the necessary level of computational accuracy, after a specific number of read cycles, these devices must undergo a reprogramming process which is a static approach and needs a large counter. This paper proposes a circuit-level RRAM read-disturb detection technique by monitoring real-time conductance drifts of RRAM devices, which initiate the reprogramming when actually it needs. Moreover, an analytic method is presented to determine the minimum conductance detection requirements, and our proposed read-disturb detection technique is tuned for the same to detect it dynamically. SPICE simulation result using TSMC 40 nm shows the correct functionality of our proposed detection technique.**

I. Introduction

Edge AI refers to algorithms and models implemented on devices such as smartphones, cameras, and sensors, rather than relying on cloud computing or remote servers. There have been many ASIC designs developed to implement deep neural networks (DNN) with a large number of multiply-and-accumulate (MAC) operations. By virtue of the massive data movement between computing and storage units, Von Neumann architecture approaches are energy-inefficient for real-time inference due to the significant power consumption and high latency [1]–[4]. The concept of computation-in-memory (CIM) involves performing computations directly within the memory, which can improve the energy efficiency as well as the performance of DNNs [5]–[7]. Resistive random access memory (RRAM) based CIM is promising due to its many advantageous features such as practically zero leakage, less access power consumption, high density, and massive parallelism [6], [7]. However, RRAM devices are subject to conductance drift over time during the read operations, leading to bit flips known as read-disturb. Any drifts in the conductance (or resistance) of the RRAM may result in computational errors due to the disruption of analog MAC values [8], [9].

Several approaches have been proposed to solve the read-disturb problem in RRAM-based CIM architecture. For instance, employing a low read voltage can reduce the impact of conductance drifts [10], [11]. Nevertheless, the voltage reduction can also increase the rate of incorrect computations, especially in the presence of process variation. Additionally, an architectural solution is proposed to improve the sensing margin that degrades the computational error due to the read-disturb [12]. However, these aforementioned solutions can just delay read-disturb occurrences and thus are not concrete solutions for the read-disturb. To address this problem, a periodic reprogram-based solution is proposed in which RRAM devices are rewritten after a certain number of read cycles [13]. Furthermore, a technique is proposed in which the read current directions can be periodically reversed to compensate for the drift effect [14], [15]. Both of these techniques use static approaches designed to consider the worst-case scenario for a correct computation, which makes the overall design too pessimistic. Additionally, a large counter is necessary to count the acceptable read cycles to reprogram periodically. Hence, there is a decisive need for a low-cost and process-independent read-disturb detection mechanism that can detect its occurrence dynamically in an efficient manner.

In this paper, we propose a methodology for RRAM read-disturb detection based on a real-time drift monitoring circuit. To introduce a realistic conductance drift scenario, the required resistance difference can be developed using a selector logic by activating/deactivating multiple RRAM devices, which can be compared using a sense amplifier. Our proposed detection methodology utilizes the same RRAM configuration as in a CIM array to detect drift effectively, considering variations in process, voltage, and temperature (PVT). Overall, the contributions to this paper are as follows:

- Develop a dynamic read-disturb detection methodology.
- Implement the circuit of the proposed read-disturb detection methodology.
- Present an analytic method to determine the minimum conductance states ratio to meet the accurate computation requirements.

SPICE simulation results using TSMC 40 nm verify the functionality of the proposed technique. Our proposed method has the capability to detect read-disturb with proximity to its occurrence, thus reducing the frequency of reprogramming cycles. The proposed technique results in a 2x improvement

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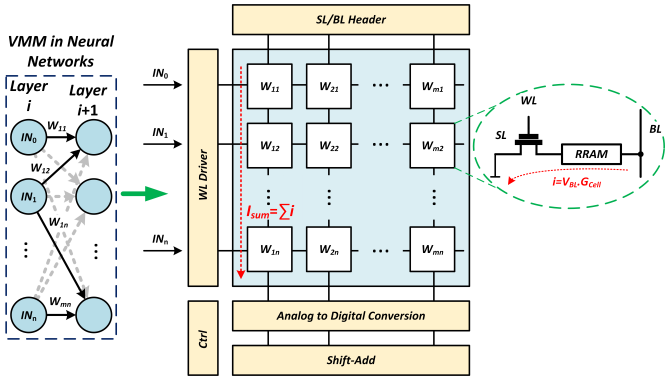


Fig. 1. A generic RRAM-based CIM architecture for neural networks.

in energy efficiency compared to the conventional periodic reprogramming approach.

The rest of the paper is organized as follows. A background on RRAM-based CIM and RRAM read-disturb is discussed in Section II. Section III presents proposed ideas, including the detection circuit and analysis. Section IV describes the simulation setups and results to verify the proposed circuit performance. The last section concludes the paper.

II. Background

A. RRAM-based CIM Architecture

Fig. 1 demonstrates a resistive random access memory (RRAM) crossbar array to implement vector-matrix multiplications (VMM) employing the computation-in-memory (CIM) paradigm. The weights of the DNN model are mapped as the resistance states of 1-transistor-1-resistor (1T1R) bitcells in the crossbar array. Multiple inputs are provided simultaneously to the bitcells in each row, where the current through bitcells perform multiplication of these inputs with the content of the bitcell (means weights). These current values are then summed up in a column to perform multiply-and-accumulate (MAC) operations. Such a MAC arrangement can result in high computation parallelism and improve energy efficiency [7].

B. Read-disturb Issue

DNN needs a large number of MAC operations [14], which means a significant of bitcell read operations are required. Due to such multiple read operations, the conductance state of the storage device can be drifted from its initial state, which can eventually switch its state, known as read-disturb [16]. Compared to standard memory, the RRAM-based CIM architectures can be more severely affected by this problem because it has to deal with small current/voltage margins during the MAC operations. Apart from the device-level parameters, the read disturb rate depends on the read voltage as well as the number of read operations [14]. Fig. 2 illustrates the impact of the aforementioned factors on the conductance state ratio of the RRAM, in which the read-disturb and conductance state ratio degradation are observed earlier as the read voltage increases. This deviation in conductance degrades computation accuracy significantly during the analog-to-digital conversion, which reduces the inference accuracy of DNNs [10], [13], [14].

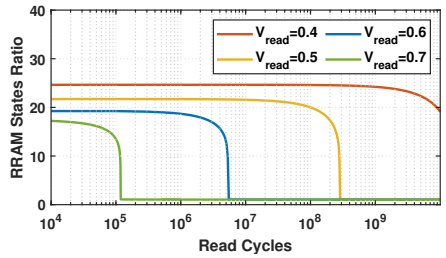
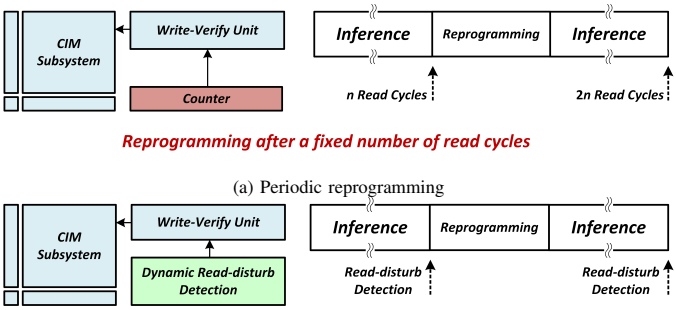


Fig. 2. SPICE simulation of RRAM conductance states ratio degradation



(a) Periodic reprogramming

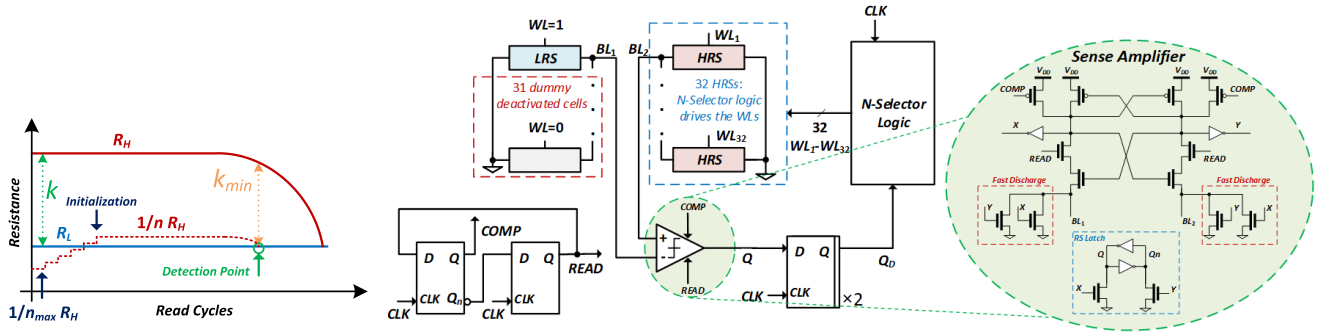
(b) Dynamic reprogramming

Fig. 3. Reprogramming approaches and their operation details.

III. Proposed Read-disturb Detection Approach

A. Overview

The most effective solution to address the read-disturb problem is to reprogram the RRAM devices after a certain number of read cycles. A static approach is proposed to program the RRAM devices after a fixed number of read cycles which is obtained considering the worst-case number of read operations on a set of test cells [13]. However, the number of read cycles for MAC values in a neural network follows a normal distribution [17], which means most of the bitcells experience it close to their mean value of read operations. As RRAMs in the CIM crossbar array do not face the same number of read operations, applying the worst iteration of read operations to test cells results in the definition of a pessimistic periodic reprogramming window. Although the majority of bitcells do not require reprogramming, it may be necessary to rewrite the entire array, even if a few conductance values are degraded for a few cells. This conservative approach ensures the long-term functionality of the RRAM-based CIM crossbar array at the cost of high energy consumption due to the higher write-verify iterations. According to our SPICE simulations, resetting a single-bit RRAM cell consumes 6x more energy than reading a 32x32 crossbar array of one-bit RRAM cells. Furthermore, defining a reprogramming period at design time cannot guarantee its accuracy in the presence of PVT variations of RRAMs at runtime. In this paper, we propose an on-chip read-disturb detection unit, as demonstrated in Fig. 3(b), which can be based on an input-profiled number of read operations on test RRAM bitcells. When the detection unit detects a read-disturb, it triggers the write-verify unit to reprogram the CIM array and test cells.



(a) (b)

Fig. 4. Proposed read-disturb detection methodology: (a) Conceptual diagram to describe the read-disturb detection mechanism (b) Circuit diagram.

B. Detection Methodology and Circuit

In our proposed read-disturb detection methodology, we arrange a set of RRAM devices with a high-resistance state (HRS) configuration in parallel so that its equivalent resistance can be compared with that of the RRAM device with a low-resistance state (LRS) configuration. For that, we employed two test columns of 32 RRAM devices, in which one column has a bitcell with LRS configuration, and the rest other are dummy cells. The other column has 32 bitcells, and all are configured in HRS. We consider the read-disturb of resistance states as illustrated in Fig. 4(a) to describe the proposed detection methodology. To detect RRAM read-disturb, two columns of RRAMs (Fig. 4(b)) are read by a read pulse with 25% duty-cycle to monitor the RRAM states ratio ($k = R_H/R_L$). Due to the large initial states ratio, n HRS bitcells (R_H) are connected in parallel to compare with one LRS bitcell (R_L) under the following condition:

$$R_H/n > R_L \tag{1}$$

The initial equivalent resistance of all parallel connected HRS bitcells in one column is adjusted to be lower than that of with LRS configuration:

$$\frac{R_{H0}}{n_{rows-max}} < R_{L0} \tag{2}$$

where R_{H0}, R_{L0}, and $n_{rows-max}$ are the initial high resistance value, the initial low resistance value, and the maximum number of activated rows in one column, respectively. In order to meet the condition described in (1), the active bit-cells with HRS configurations are turned off one by one during each cycle until the initialization point is reached. The resistance of n parallel-connected HRS bitcells equals one LRS bitcell when the read-disturb is detected at the detection point using a comparator to generate a detection signal. This means that the RRAM states ratio at the detection point is the number of active rows, n_{rows}. Also, the ratio at the detection point can be defined as the minimum required ratio, k_{min}.

Fig. 4(b) demonstrates the proposed detection circuit, which utilizes two columns of the crossbar array. The first column consists of one active LRS bitcell and 31 deactivated dummy cells, while all the wordlines of the second column, all programmed in HRS, are driven by a logic circuit called N-Selector logic. The N-Selector logic is utilized to initialize the number of active HRS bitcells. This block deactivates the last active wordline when the sense amplifier produces a high output. In other words, this block operates only if the condition described in (1) is not met. Therefore, it is employed to initialize the detection unit and remains inactive until the detection point.

A sense amplifier does the comparison between the current values of the two columns. We have employed a pseudo-differential StrongARM latch-based sense amplifier [18], as illustrated in Fig. 4(b). The sense amplifier was modified to apply a read voltage on the bitline using two overlapping $READ$ and $COMP$ pulses. Furthermore, a fast discharging path is considered to prevent post-comparison voltage on RRAMs and to rapidly reset the bitline voltages at the end of the comparison. High input offset is one of the issues of pseudo-differential sense amplifiers. To alleviate the input offset impact on initialization, the output of the sense amplifier has been delayed for two clock cycles. Consequently, the detection circuit initializes with two lower active wordlines than the first initialization point. This technique reduces the sensitivity of the circuit initialization to PVT variations.

C. Minimum RRAM Conductance States Ratio

As shown in Fig. 5, we considered the two low current states (I_0 and I_1) to have an equal relative error, e, which can be defined as $3\sigma/\mu$. In order to prevent the overlap of these current states, the following condition must be fulfilled:

$$I_0(1+e) < I_1(1-e) \tag{3}$$

Considering states ratio of $k(t)$ ($R_H = k(t)R_L$), condition described in (3) can be rewritten as:

$$\frac{n_{rows}V_{read}}{k(t)R_L}(1+e) < (\frac{(n_{rows}-1)V_{read}}{k(t)R_L} + \frac{V_{read}}{R_L})(1-e) \tag{4}$$

Therefore, the minimum states ratio (k_{min}) derives as:

$$k_{min} = \frac{2n_{rows}e - e + 1}{1-e} \tag{5}$$

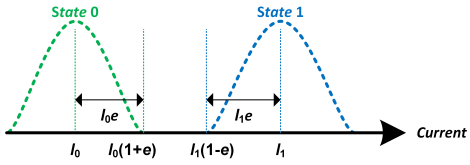


Fig. 5. Conceptual diagram of MAC current states.

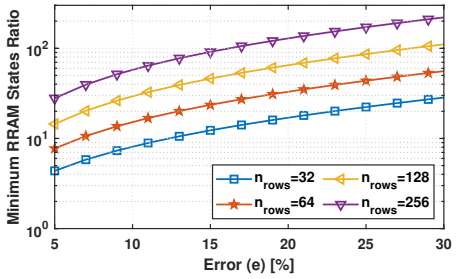


Fig. 6. Minimum required RRAM states ratio for the different numbers of rows and error values.

According to (5), the minimum required ratio is an ascending function of the number of rows, which indicates that it is essential to meet the conductance ratio criterion according to the memory size in design time. Please see Section IV-B for the simulation results for the minimum required ratio.

IV. Simulation Results

A. Setup

The proposed read-disturb detection unit has been designed using TSMC 40 nm CMOS technology with 0.9 V supply voltage and simulated using Cadence Virtuoso tools. Due to the inactive nature of N-Selector logic after initialization, it has been implemented using Verilog-A. Moreover, we have employed the JART VCM v1b RRAM model [19], [20]. To simulate the read behavior, a 200 MHz clock frequency is used in the proposed circuit, which applies a 460 mV voltage for a 5 ns period on bitlines followed by a 15 ns bitline reset according to the sense amplifier, augmented by the considered $READ$ and $COMP$ signals in the proposed circuit.

B. Analytic Results

The curves illustrated in Fig. 6 demonstrate the minimum required states ratio for the different numbers of rows and error values. Equation (5) states that in cases where the desired error is less than 20%, the minimum required ratio is less than the number of rows in the crossbar. This means that the monitoring circuit requires only one column of parallel-connected HRS bitcells, while multiple columns of parallel-connected HRS bitcells are essential for higher error values. However, the relative error value can be reduced significantly below 20% by employing the write-verify scheme during the design time [21].

C. Circuit-level Results

Simulation results demonstrate 75.9 μW power consumption, 1.6 fJ power-delay product (PDP), and less than 3.1×10^{-20} Js energy-delay product (EDP) for a 20 ns read-comparison operation in initialized condition. It is seen from

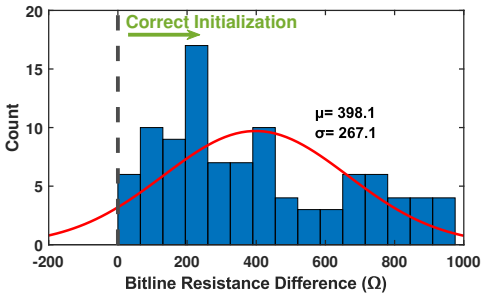


Fig. 7. Distribution of the resistance difference after initialization.

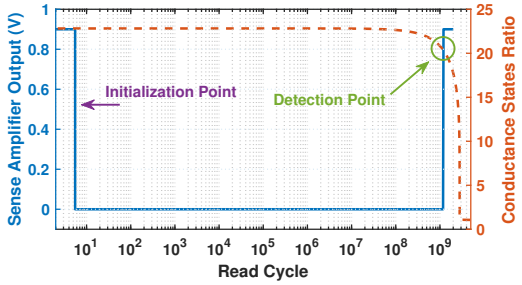


Fig. 8. Simulated transient response of the proposed circuit.

the Monte-Carlo simulation results of Fig. 7, that the detection circuit was initialized correctly in all of the 100 run points and satisfied the condition described in (1). The proposed detection unit was also evaluated in both the initialization and detection phases, as depicted in Fig. 8. It is seen that when the RRAM states ratio is degraded by 10% to its original value, the proposed circuit generates a detection signal.

Comparing the detected point in Fig. 8 with the ratio drop for a worst-case inputted RRAM cell, a reduction of 19% is indicated in the worst-case inputted RRAM cell. The worst-case input is rare [17] and its detection point occurs approximately 6×10^8 read cycles prior to the averaged input detection point. In other words, the proposed detection methodology triggers the write and verify unit around 50% less than the pessimistic reprogramming approach, which means $2\times$ write energy efficiency. Note that the acceptable conductance ratio reduction can be determined based on the calculated minimum required ratio and the desired error margin (e) for the actual crossbar in a specific application.

V. Conclusion

In this paper, an approach for detecting RRAM read-disturb in real-time by monitoring the RRAM states ratio was presented. Our proposed method facilitates dynamic reprogramming by providing superior energy efficiency and computation accuracy compared to the static method. Further, an analytical method was developed to determine the minimum required RRAM states ratio in a CIM architecture. According to SPICE simulation results using TSMC 40 nm CMOS Technology, the proposed methodology promises a 2x increase in the energy efficiency of the writing operation over conventional periodic reprogramming through the reduction of redundant write operations. The proposed approach is a potential solution for developing RRAM-based CIM architectures.

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