Flexible Interposer Based on Carbon Nanotubes and PDMS Composite

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by

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An electronic version of this thesis is available at http://repository.tudelft.nl/.
A new method of flexible interposer with vertically aligned carbon nanotube (CNT) embedded in polymer is proposed in this thesis. Interposer, working as electrical routing between different sockets or connections, is being used for spreading connections and rerouting in packaging technology nowadays. With the rapidly growing application of wearable electronics, flexible interposer plays a crucial role to meet the requirements of flexibility and high-density integration capability for interconnection. However, current flexible interposers, usually composed of metal and polyimide, have material physical limits, and heat resistance caused by pattern shrinkage etc. Vertically aligned CNT is an one dimensional conductive material with higher current density and longer electron free path than common used interconnection material, which could be used for interconnection. Polydimethylsiloxane (PDMS), as one of the most widely used elastomeric polymers in MEMS applications, has the advantages of low cost and easy fabrication. A flexible interposer combined the merits of CNT and PDMS was investigated in this work.

In Chapter 1, the relative knowledge of CNT and polymer are reviewed. Electrical simulation and design for the interposer structure are made in Chapter 2. Optimized CNT pillar and PDMS composite structure is chosen as the interposer architecture. Interposer with via size ranging from 20 um to 500 um were fabricated by utilizing CNT pillar bundles as interconnect via using its anisotropic electrical conductivity, and elastomeric material PDMS as thin flexible isolation layer. Processing details and techniques are shown in Chapter 3. Standard thin film process, including photolithography, metal evaporation, and spin coating are performed. Chapter 4 shows electrical and mechanical characterization of the fabricated device. I-V curve is obtained by a 4-probe measurement structure as well as calculation results. Chapter 5 presented the discussion about the future work. This study demonstrates a novel flexible interposer composed of vertically aligned CNT bundles and PDMS with wide application. The initial results promise the possibility for flexible interposer utilizing CNT as electrical interconnects and polymer as the supporting layer.

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Flexible interposer plays an important role in packaging technology. With physical limitation of commonly used metal vias in flexible electronics, PDMS/CNTs (polydimethylsiloxane and carbon nanotubes) could be good configuration for flexible interposer to meet increasing demands on flexible interposer. In this chapter, state of the art of flexible interposer is shown, and relative knowledge and boundedness of interposer are presented. The anisotropic conductivity of CNT is studied as well as widely used polymer which have potential as insulating and supporting material in the fabrication of interposer.

1.1. Flexible Interposer

Interposer works as electrical routing between different sockets or connections. It could be used for spreading connections to different ones and rerouting in packaging technology. By applying interposer in packaging, different chips could be connected together for combining operation and data transfer, and then connected to packaging board. Interposer with vias provide designers a possible way to achieve the benefits of chip-scale connected configuration without much design and production issues. It could be done by simply adding a die to an existing design in stacked chips design using interposer. The utilization of interposer meets the performance of bandwidth and power requirements simultaneously.

Figure 1.1: Typical interposer structure for connecting active chip to another. The interposer is composed of conductive vias, supporting material, and metal for connection with other chips.
As depicted in Figure 1.1, a typical interposer is composed of electrical conductive vias, substrate supporting material as substrates all around the vias, and conductive contacts between interposer and chips. The electrical conductivity of vias, contact metal, and contact resistance between vias and peripheral circuit determine the resistance of interposer, while the flexibility of interposer is mainly set by mechanical property of supporting material.

Interposer can be categorized as rigid and flexible interposers when it comes to substrate. One of the most popular rigid interposers is through silicon via (TSV). Interposer based on TSV overcomes the mismatch of the input/output (I/O) pitch between the integrated circuit (IC) and main printed circuit board (PCB) substrates. It is a common used technology in 2.5D/3D integrated circuit [1]. Flexible interposer, which could mitigate the stress between interposer tile and the substrate, usually takes polyimide as substrate, and metal as conductor for power and signal transmission [2] [3] [4].

Metal and polymer composite interposer combining the advantages of two materials, avoids the global interconnection delay and latency problem. Copper (Cu) is the most commonly used metal in flexible interposer configuration [5] [6]. However, copper is reaching its physical limits because of the shortage of electroplating fabrication method, and will not likely to be able to meet the desired aspect ratios requirement to create 3D IC with a high enough via density [5].

A novel flexible interposer based on CNT and polymer composite prototype was proposed in this project because of current interposer challenging issues. CNT, with its outstanding anisotropic electrical conductivity serves as interconnection material, and polymer, an elastomeric polymer works as flexible substrate and isolating material.

1.2. CARBON NANOTUBES (CNT) FOR INTERPOSER

1.2.1. GENERAL BACKGROUNDS OF CNT

CNT was first reported by Iijima in 1991 [7], and then soon drew widely attention from researchers because of its outstanding properties such as thermoelectricity, superconductivity, electroluminescence, and photoconductivity [8]. Outstanding electrical properties and high thermal conductivity make CNT a potential material for interconnection. CNT could be visualized as rolled up sheets of graphene while graphene is a layer of single carbon atoms. Single-walled carbon nanotube (SWCNT) is taken as one layer of cylinder graphene, and multi-walled carbon nanotubes (MWCNT) are rolling up of several layers of cylinder graphene sheets with conductivity. The structures of CNT and graphene are shown in Figure 1.2.

![Figure 1.2: Schematics of graphene (left), SWCNT (middle) and MWCNT (right) structure [9]](image)

Graphene, which is a single layer of sp² bonded carbon atoms could be rolled up to form nanotube. Car-
bon atoms in the cylinder have partial sp³ character that increases as the radius of curvature of the cylinder decrease. The way of graphene being rolled into tubes is described by a parameter, chirality. Chirality could be considered as the way of how graphene roll up compared with the unit vectors of the graphene unit cell. The map of chiral circumferential vectors \( \vec{C}_1 \), \( \vec{C}_2 \), and \( \vec{C}_3 \) and its indexed (n, m) are shown in Figure 1.3.

![Figure 1.3: CNT chiral vector [10]](image)

Where \( \vec{C} \) is the chiral vector. \( \vec{a} \) and \( \vec{b} \) are the unit vectors. A pair of integers n and m is the chiral vector indexes, which represents the number of steps along unit vectors of the lattice [11]. Solid dots in the figure locate on the tips of \( \vec{C}(n, m) \). With different n and m values, the orientations of the atoms around the nanotube circumference are classified as armchair (n=m), zigzag (n=0 or m=0), and chiral (others) [12]. Chirality represents the band structure of the CNT, and then causes an effect on its transport properties, especially on electrical properties. Armchair states would be metallic when n is equal to m. When n-m=3i, it presents as semi-metallic with a bandgap of a few meV, and the shell will be semi-conductive within other cases [13]. Rolling graphene along three vector resulted in three types of CNT, as shown in Figure 1.4 [14].

For MWCNT, having several shells of rolling up graphene layers, electrical property is the superposition of every single layer, which is hard to be predicted.

Many parameters of CNT are also important for CNT quality except chirality, such as grown temperature during synthesis, grown catalyst etc. Quality is the symbol of CNT crystallinity, which is difficult to be described with number. The quality of CNT could be investigated by expensive way of transmission electron microscope (TEM) or cheaper way of Raman spectroscopy.

1.2.2. Anisotropic Electrical Conductivity of CNT

CNT is employed to be a potential connection material thanks to its outstanding electrical properties. The current density of CNT via could reach \( 10^9 \) A/cm², even at high temperature [15] while Cu as the most widely used contact material has a current density of only \( 10^6 \) A/cm². The mean free path (also called ballistic length) of electrons in CNT could reach dozens of micrometers, longer than Cu, having a mean free path only a few micrometers. Longer mean free path means less scatter for CNT and better conductive performance. Further more, CNT is considered as a promising material for connection also because of its anisotropic electrical
1. Introduction

For vertically aligned SWCNT, out-of-plane conductivity (as shown in Figure 1.5) of a study about CNT films grew on quartz substrate being dip-coated in molybdenum and cobalt acetate solutions, taking Co-Mo as catalysts out-of-plane direction conductivity of CNT was measured to be about 0.56 Smm\(^{-1}\) independent of film thickness by CT. Lin et al. The in-plane conductivity was found to be more than an order of the height \[16\]. According to some other measurement results for vertically-aligned MWCNT, the out-of-plane electrical conductivity was about 0.50 Smm\(^{-1}\), while the in-plane electrical conductivity was about 0.05 Sm\(^{-1}\) \[17\], reported by Huang et al. These reported measurement results demonstrate that vertically aligned CNT bundles has a much better electrical conductivity in vertical direction than the one in horizontal direction, which is advantageous for conducting between different substrates of stacked layers.

Getting the orientation of CNT well controlled as vertically aligned could help with improving the electrical conductivity of CNT based conducting device, compared with previous nanopowder or nanofibre based conducting composite material.
1.2. Carbon Nanotubes (CNT) for Interposer

1.2.3. Equivalent Circuit Model of CNT

Resistance is a critical parameter for CNT serving as conducting material. It determines the electrical property of interposer to a large extent. Good understanding on CNT resistance helps with analysis in respect of interposer electrical performance. Because the electrical property of MWCNT is the superposition of every single layer's property, SWCNT equivalent resistance should be discussed at the beginning.

Equivalent resistance circuit of unit length SWCNT is presented in Figure 1.6. This model was developed by A. Naeemi et al. for one metallic SWCNT [18]. Resistance of CNT is composed of three parts. The constant quantum resistance, the length-dependent resistance because of electrons scattering, and the contact resistance at the ends of the unit length tube caused by conduction bands contact between CNT and other conductive material.

![Figure 1.6: equivalent resistance circuit of SWCNT [18]](image)

In this circuit, $R_C$ is the contact resistance, shared by two ends of the tube. $R_L$ is the resistance dependent on CNT length. $R_Q$ is the quantum resistance. $R_{bias}$ and $R_{shunt}$ are two components defined as bias voltage dependent resistance and shunt resistance, respectively. The influence from these two resistors could be ignored in interconnects as the voltage drop over an interconnect is small [18]. For SWCNT, there are 2 channels, of which are both spin-degenerate, then quantum resistance could be calculated easily [19]. Number of conductive channels are related to shell diameter, as Figure 1.7 illustrates the diameter dependency of the conduction channels at room temperature [18].

![Figure 1.7: number of conductive channels per wall versus diameter at room temperature [18]](image)
For MWCNT, several shells and larger diameter result in more conduction band. Small bandgap could be overtaken by charge carriers at temperature higher than room temperature. $R_Q$ is the sum of all quantum resistance of every conductive channel in parallel, as expressed in Equation 1.1

$$R_Q = \frac{1}{N_c N_t} \frac{h}{2e^2}$$

(1.1)

where $h$ is Planck’s constant, $e$ is the electron charge. $N_t$ is the number of tubes in the bundle, and $N_c$ is the total number of conductive shells for MWCNT, as expressed as Equation 1.2 [18]. $p$ is the number of shells in MWCNT, while $n$ is an integer which denotes the shell number, $Nos$ is the number of shells, and $Noc$ is the number of channels per shell.

$$N_c = \sum_{Nos} Noc$$

$$= \sum_{n=1}^{p} N_{C14}(d_n)$$

(1.2)

When the tube has a length longer than the mean free path (or ballistic length), there will be electrons scattering in the tube, resulting in resistance dependent with tube length, which could be described in Equation 1.3

$$R_L = R_Q \frac{1}{\lambda_{CNT}}$$

(1.3)

Then, with CNT bundles have a length of $l$, the total resistance of CNT bundles could be expressed by Equation 1.4

$$R_{CNT} = R_{CNT} = R_C + R_Q + R_L$$

$$= R_C + \frac{1}{N_c N_t} \frac{h}{2e^2} + \frac{1}{N_c N_t} \frac{h}{2e^2} \frac{l}{\lambda_{CNT}}$$

$$= R_C + \frac{1}{N_c N_t} \frac{h}{2e^2} (1 + \frac{l}{\lambda_{CNT}})$$

(1.4)

**1.2.4. CNT GROWTH METHOD**

CNT growth could be achieved mainly by three methods, arc-discharge, laser ablation, and chemical vapour deposition (CVD). Arc-discharge and laser ablation usually require high temperature up to 900 °C [20] [21], and need the condensation of hot gaseous carbon atoms generated from the evaporation of solid carbon, which is expensive. With CVD method, a gaseous carbon source will be decomposed, and the nanotube would be deposited around catalyst atom particles from the substrate. Besides, vertically aligned CNT could be synthesized easily, and the height, diameter of CNT could be more controllable within bottom-up CVD growth method [22].

Synthesis of CNT requires nanometer-size metal catalyst particles since CNT need to nucleate from a nanoparticle. Ni, Co, and Fe can serve as catalyst for CNT growth. The size of catalyst particles would dictate the diameter of the nanotube. MWCNT has diameter ranging from several nanometers to several hundred nanometers. During CVD process, these catalyst nano particles absorb the precursor and dissociate the hydrogen. Then carbon atoms diffuse by surface diffusion towards the CNT growth front, where it forms a CNT due to energy minimization. CNT growth direction is generally random, but is also steerable by interactions of the tubes with their surroundings. Due to Van der Waals interaction between tubes, vertically aligned CNT
could be obtained when the density of catalyst particles are sufficiently high [23].

To improve the catalyst density and quality, catalyst supporting layer should also be applied. It could prevent catalysts particles from diffusing too deep in the substrate. The same catalyst works differently with different supporting layer. Alumina, silica, silicon carbide are commonly used materials. Taking Al$_2$O$_3$ as an example, the thickness of Al$_2$O$_3$ has a large effect on CNT growth. According to some research, CNT growth results are related to thickness of Al$_2$O$_3$ coated on it when having a constant catalyst thickness of 0.5 nm Fe as catalyst, as illustrated in Figure 1.8 [24]. It is clear that when the alumina thickness increases, the height of CNT increases accordingly, while electrical conductance decreases until there is no current flow. At this time, ultra-thin layer of alumina allows tunnelling, and Fe catalysts diffuse into the substrate, and then eventually terminate CNT growth at an alumina thickness around 4 um [24].

CNT growth method is determined by catalyst and supporting material selection, or called catalyst-support interaction (CSI). With different catalyst and catalyst supporting layer combination, CNT growth mechanisms are classified as tip-growth and base-growth, illustrated in Figure 1.9. For example, with Fe-Al$_2$O$_3$, the interaction is quite strong, resulting in very low diffusion of catalyst. Nanoparticles couldn’t be raised up by the nanotube wall, then a base growth is yield. With metal-SiO$_2$, the metal particles were raised up during pre-treatment and growth, resulting in tip growth.

Other parameters, such as temperature, and time etc will also influence the synthesis of CNT. For example, generally, high temperature, from 900-1200°C usually yields SWCNT while low temperature 600-900°C is for MWCNT. Different temperature also has effect on CNT quality. CNT length is generally dependent on the growth time at the beginning. Temperature also matters with the CNT growth (results will be presented in
Chapter 3), while chirality is still not steerable for now [25]. For long growth time, catalyst particles might become inactive, caused by covering of catalyst particles, and finally results in growth rate reduction [26].

**1.2.5. Previous Work on CNT Based Composite**

Many researches about CNT and polymer composite for conduction have been done since CNT is considered as a promising material in connection usage with its outstanding electrical conductivity. Electrical properties of polymer composite containing carbon nanotubes depend on several aspects, such as synthetic process of producing nanotubes since quality of CNT determine its electrical performance; aspect ratio of the nanotubes in the composite (isolated, ropes, or bundles); nanotube orientation in the polymer matrix since etc. Diverse approaches of combining these factors will lead to different performance of CNT and polymer composite.

![Figure 1.10: Examples of CNT and polymer based composite (a). some of long nanotubes aligned, and some of them randomly oriented in 80-nm-thick film [27] (b). SEM image of nanotube on Al surface with 2.0 wt. % [28] (c). SEM image of shear-induced preferential alignment CNT film [29] (d). SEM image depicted randomly oriented CNT in Cu matrix [30]](image)

Nanocomposite using CNT as filler was first reported in 1994 by P. M. Ajayan et al [27]. Simple technique by cutting thin slices of a nanotube-polymer composite was utilized here. The composite was fabricated by randomly dispersed nanofibre in liquid epoxide-base resin. As shown in Figure 1.10 (a) some long, thin tubes were aligned in one direction, while the thicker, shorter tubes stayed randomly oriented.

Al-CNT reinforced metal matrix composite has been prepared by deformation routes by C. F. Deng et al [28]. Nanotubes could located in the composite homogeneously by being added to ethanol. Cold isostatic
pressing followed hot extrusion techniques were applied to be put into a pure Al package followed into a rubber bag. As illustrated in Figure 1.10 (b), CNT located out of order.

A shear-induced preferential alignment of CNT with polymer composite has been done by Leslie Joy Lanticse et al, which resulted in anisotropic electrical conductivity [29]. In this study, CNT have been induced by doctor blade to get CNT direction controlled for higher electrical performance. Aligned CNT SEM image is shown in Figure 1.10 (c), not very tidily.

Copper vertically aligned CNT samples prepared by electro-deposition is depicted in Figure (d), discussed by Lavanya Arysomayajula [30]. Randomly oriented CNT in copper matrix was formed for filling TSVs. With low cost and low technology handling issue, copper/CNT composite with dispersed CNT in the matrix helped a lot with the improvement on electrical resistivity reduce for 40 %.

Most of studies based on CNT and polymer composite utilized nano fibers or nano particles dispersed in polymer or metal matrix as filler. Sometimes induced alignment CNT also served as conduction material. These methods did make improvement on the electrical conductivity to different extent. However, none of these studies did take full advantage of anisotropic electrical conductivity of CNT.

1.3. POLYMER

Polymer, due to its simple process, high yield and low cost, is an important material in the fields of MEMS application and packaging technology. Some MEMS devices made with the most commonly used polymer have been reported, as shown in Figure 1.11.

Figure 1.11: MEMS device fabricated with commonly used polymer (a). CNT/PDMS based Fresnel optics [31] (b). Polyimide/Cu based interposer [5] (c). PDMS/glass hybrid structure [32] (d). Polyimide device of tactile sensor array on silicon wafer [33].

Figure (a) presents a tunable CNTs/PDMS based Fresnel optics for particles detecting, reported by X. Li et al [31]. In figure (b), a flexible interposer, which was composed of polyimide and copper is depicted [5]. Figure (c) presents a PDMS/glass based hybrid structure with integrated heating and sensing devices for biomedical application [32]. Figure (d) shows polyimide tactile sensor array [33]. These devices presented mechanically flexible performance because of the existence of elastic polymer materials in devices.
1.3.1. Polyimide

Polyimide, is considered one of the most important materials because of its excellent mechanical properties, and also its great stability even at elevated temperature. Polyimide based interposer research has been conducted for decades. It was reported very early in 1998 that the interposer was attached by pre-deposited adhesive at the active side the chip [2]. The fabrication of flexible interposer based on polyimide improved a lot during the last two decades. Electrolytic copper pattern plating based flexible polyimide interposer was published recently [6]. Some researches on nanocomposite based on polyimide have been reported. High-density micro thermal sensor was directly fabricated on Kapton polyimide film, and the film still remains its dimensional stability and electrical insulation, mechanical strength [34].

Normally, the operating temperature for polyimide could exceed 260 °C. It decomposes at temperature higher than 520 °C, showing a good stability at elevated temperature.

Dry etching method of polyimide uses Plasma Enhanced Chemical Vapour Deposition (PECVD). Silicon nitride works as mask, and oxygen plasma with some CF$_4$ as processing gas. Figure 1.12 (a) presents the surface of PI after plasma etching [35]. As shown in the figure, plasma etching of PI could lead to a relatively smooth surface. Another possible way of PI etching could be conducted as wet etching, using Tetramethylammonium hydroxide (TMAH) developer for unmasked polyimide. Photoresist would be developed at the same time by using this method. Wet etching of polyimide cannot realize gradually etching layer by layer. Then wet etching is not favorable during process.

Figure 1.12: Surface images of commonly used polymer in MEMS after plasma etching (a). Polyimide surface after plasma etching [35] (b). PDMS surface after plasma etching [36]

1.3.2. Polydimethyilsiloxane

PDMS, is another widely used structural material in microfluidics [37] to microelectronics [38] with its outstanding biocompatibility, optical transparency, and electrical insulation. It is cost-effective, and could be processed with standard silicon-based fabrication.

PDMS is directly formed in patterned mold, or spinned onto a substrate and then cured during fabrication, generally. After curing, PDMS could form a relatively rigid and durable device, and continue with some further selective removal procedure. Dry etching method of PDMS is the same with PI’s, using oxygen and CF$_4$ plasma. The etching rate could be controlled by changing the ratio of O$_2$ and CF$_4$. Wet etching of PDMS is also possible with some mixed solution.

As an elastometric material, PDMS has a tensile strength about 6.5 MPa, and working temperature is lower than 100 °C.
Technology of PDMS processing has been studied by DIMES [36] and other researchers [39] [40]. Dry etching method and wet etching method of PDMS resulted in different surface roughness, previous research results is shown in Figure 1.12 (b). Wet etching of PDMS brings up better surface smoothness compared with dry etching, still 0.7 um of peak-to-peak roughness was reported [41].

Principle behind this silicones is an alternative chain of silicon and oxygen atoms, with two free bonds on the silicon atom as shown in Figure 1.13. These bonds are both filled with methyl group in PDMS structure. Molecular configuration of PDMS shows that it is hydrophobic, which might cause some processing challenges during fabrication.

![Figure 1.13: PDMS formula](image)

PDMS was chosen in this project for prototype demonstration working as insulating material and supporting substrate because of ease of processibility, and also because of rich experience of technicians on PDMS processing. Another reason is that wet etching of PDMS could be achieved layer by layer while wet etching of polyimide is not possible to remove polymer gradually.

### 1.4. Flexible Interposer Based on CNT and PDMS Composite

A novel CNT and polymer composite flexible interposer has been proposed in this project. CNT, serves as conducting vias with its anisotropic electrical conductivity, and elastic polymer PDMS works as insulating and supporting material. The 3-D graphic of interposer is shown in Figure 1.14.

![Figure 1.14: interposer prototype based on CNT and PDMS](image)

Fabrication of this interposer device basically is composed of several critical procedures. Vertically aligned CNT bundles growth should be conducted on the substrate at the beginning, followed with PDMS infiltration on CNT samples through spinning and curing. Top ends of CNTs would be covered by PDMS because of the application of large amount of PDMS. Moderate wet etching of PDMS could expose CNT bundles in air without making CNT bundles much higher than the rest PDMS layer. Metal contacts pattern on CNT bundles made the CNT/PDMS composite as a complete interposer.
1.5. **Thesis Outline**

The purpose of this project was to propose and demonstrate a flexible composite polymer based on CNT and polymer interpose device, which could be used in flexible electronics packaging. The focus would be on the design, fabrication and characterization of flexible interposer device. CNT serves as electrical conducting material, PDMS works as isolation and supporting material, and metal works as the connection band between interposer device and other chips, so CNT growth, polymer processing and contact metal pattern were critical procedures need to be investigated. Characterization of fabricated device on the quality of CNT samples, the electrical performance of interposer device were also depicted. The realization of this work was determined in the way below:

- State of art of flexible interposer and potential material for new design (Chapter 1)
- Requirements on interposer parameters and materials, and simulations about interposer electrical performance (Chapter 2)
- Fabrication details of the interposer (Chapter 3)
- Electrical performance (Chapter 4)
- Discussion about future work (Chapter 5)
- Conclusion (Chapter 6)
In this chapter, current flexible interposer parameters are given as a reference for the new design. Requirements on CNT and PDMS for interposer are outlined. Simulation based on electrical performance are conducted. Simulation results of interposer model with diverse size and pitch are compared and well presented. Measurement methods of CNT bundles resistance and contact resistance are described. Based on simulation results, measurement method and fabrication rules in Else Kooi Lab, parameters such as interposer pitches and sizes are settled. Contact aligner masks are designed, and illustrated in this chapter.

2.1. **Requirements on Flexible Interposer**

Flexible Interposer as a key building block for flexible stacked system is becoming a primary enablers for completing electrical connection through shorter architecture. It is utilized in flexible electronics from flexible displays to flexible sensors widely. With great improvements in photolithography, process and devices etc., fine pitch with high performance is always required to meet the development of industry.

Flexible interposer based on polyimide for Chip size packaging (CSP) was reported in 1998 by V. Beyer el at. Solder pads with diameter of 220 um and pitch of 500 um were located at the interposer [2]. A flexible interposer with 40 um thick substrate and SnAg-solder bumps 50 um formed was reported by K. Hikasa el at in 2003[42]. In 2015, Y. Huang el at presented a ultra thin flexible interposer based on Cu and olyimide with a fine pitch of 12.5 um, and the size of the via was 20 um. The decrease on size and pitch reveals the development on processing and packaging technology. For the new CNT and PDMS based flexible interposer, with thickness of dozens of micrometers, and pitches also on micrometer level should be fabricated.

2.1.1. **Requirements on CNT**

As discussed in Chapter 1, CNT is a promising material in connection technology. Several requirements need to be met to realize the application of CNT in interposer, being compatible with current packaging technology.

1. CNT should be vertically aligned: only with vertically aligned CNT, can the anisotropic electric conductivity be made the most use;

2. High electrical performance: electrical performance should be high, at least being compatible with normal conductive metal. Electrical performance of CNT based on the quality of CNT, crystallinity is influential when chirality is not controllable;
3. Equivalent height with current packaging technology: thickness of interposer should be connectible with other dies and chips already exist.

### 2.1.2. Requirements on Polymer

Polymer works as supporting and insulation material in the novel flexible interposer. It isolates the current in horizontal direction and gets pressure relieved. Then the PDMS being used for this interposer device should be able to satisfy the following issues:

1. Polymer thickness should be accurately controlled: only with steerable thickness of polymer could it be guaranteed that CNT top end being exposed in the air for further metal contacts;

2. Polymer should has ease of processibility;

3. Material need to be compatible with clean room processing rules.

### 2.2. Simulation of Interposer Test Structure

Electrical simulations were conducted to better understand how CNT and polymer composite work as conductive device, and how CNT bundle size and pitches affect on the performance of interposer. COMSOL Multiphysics 4.4 is the simulation software being utilized to estimate the performance, and help with design.

Simulation was focus on the electrical performance since interposer is supposed to be an electrical connecting bloc. Based on the basic architecture of interposer, a simulation model was build. Figure 2.1 illustrates the vertical view of this structure, and cross section of line A-A' plane is shown in Figure 2.2. In this two figures, the square and circle array blocks are filled with vertically aligned CNT bundles, with a thickness of 100 um. The thin layer at the bottom and on top of CNT bundles are Aluminum metal layer, both with a thickness of 2 um. Metal layer are here serving as contacts. The rest light blue material is the isolation supporting layer, PDMS.

![Simulation model](image)

Figure 2.1: Vertical view of simulation model, circles and squares are CNT bundles top view

Fine pitch is one of important parameters of the target interposer. Smaller pitch is always the tendency for meeting scaling down packaging technology. However, keeping reducing the pitch is not always a solution since via might affect when pitch is small enough. It might affect the performance of interposer to some
extent. The first simulation was conducted to compare electrical potential distribution with diverse pitches. The diameter (or side length for square) was settled as 100 um, and then pitches differed as 20 um, 50 um, 100 um and 200 um. Applied with current density from the top metal layer. The bottom metal layer was settled as the ground, and a current 1 mA was applied. Then the potential distribution could be simulated, as presented in Figure 2.3. The potential on the surface was on milli volt level.

The potential decreases from top to bottom along the vias. There is potential distribution between two CNT bundles in PDMS isolation material even though PDMS is a dielectric material. As shown in Figure 2.3, with increasing pitch, the potential drop between two CNT bundles edge were becoming larger. With pitch larger than 100 um, potential difference was less critical since potential in the middle point between two vias presents a potential at the same level of potential far away from the current source input points.

The current density distribution was simulated, with results illustrated in Figure 2.4. It is obvious that current density is exactly the same along the vias from top to down, and all current were isolated in the vias strictly. There is no current leakage between vertical vias in all situations.

Small size of interposer via is a significant object for advanced packaging nowadays except for fine pitch. Based on the simulation results for pitch changing, pitch was fixed as 100 um, set diameter (or side length for
Figure 2.4: Simulation results of current density distribution on interposer with fixed size of 100 um and diverse pitch, pitch are (a). 20 um (b). 50 um (c). 100 (d). 200 um respectively

Figure 2.5: Simulation results of electrical potential distribution on interposer with fixed pitch of 100 um and diverse size, size are (a). 20 um (b). 50 um (c). 100 um (d). 200 um respectively
2.3. Electrical Measurement Method for CNT

The voltage potential simulation results show that the potential difference between smaller size vias are larger than the one between larger vias. The potential drop between 20 um vias has the biggest voltage drop. The voltage drop becomes smaller along the increasing vias size. Apply with 1 mA current on the input surface, the voltage on the surface are different since different size of CNT vias have different resistance. Vias with the smallest size has smallest cross section area, then the largest resistance, which resulted in the largest voltage with the same current applied.

Current density distribution results of interposer with fixed pitch of 100 um and diverse sizes are illustrated in Figure 2.6.

![Figure 2.6: Current density distribution simulation results of interposer with fixed pitch and diverse size, size were (a). 20 um (b). 50 um (c). 100 (d). 200 um respectively](image)

It is obvious that current density is exactly located only the vias from top to down. There is no current leakage between vertical vias in all situations. It should be noticed that in vias with circles as top view and vias with square top view have different current distribution. Current distribution in vias with circles top view is not homogeneous. This heterogeneity remains as a puzzle since they have the same potential distribution.

2.3. Electrical Measurement Method for CNT

To measure the resistance of CNT bundle, two ends of CNT bundle should be connected with measurement probes. The driven current could cause voltage drop between CNT bundle ends. Then the resistance of the CNT bundle could be calculated by dividing the voltage drop with the current flow the bundle. With this method, a 4-probe measurement structure was utilized [19]. In this method, the electrical measurements are done by placing probes on contact metal pads as illustrated in Figure 2.7.

Four contacts in this figure are defined as \( I_{out} \), \( I_{in} \), \( V_{in} \), and \( V_{out} \) respectively. The driven current goes in from the point \( I_{in} \), then goes down to the bottom of the to be measured CNT bundle. After spreading in the
bottom metal layer, it would pass through the conducting CNT bundle. Finally, the current would go out at point $I_{out}$. Since $I_{out}$ and $V_{out}$ are connected by the bottom metal layer, having the same potential, and the potential of point $I_{in}$ and the potential of point $V_{in}$ are also the same since they would be connected by top metal layer, the resistance of the CNT bundle could be easily calculated by Ohm's Law $R = \frac{V}{I}$.

Figure 2.8 illustrates the cross section of this measurement structure. Intrinsic resistance of metal is defined as $R_{metal-top}$ and $R_{metal-bottom}$ for metal on the surface, metal at the bottom, respectively. Contact resistance is the resistance between CNT and metal, $R_{con}$. $R_{CNT}$ is the resistance of CNT via to be measured. $R_{cnt}$ is the resistance of CNT bundle that served as connection. The equivalent circuit of this measurement is shown in Figure 2.9.

In this method, resistors are
then the total resistance measured could be expressed by

\[ R_{\text{total}01} = 4R_{\text{con}} + 2R_{\text{metal-top}} + R_{\text{metal-bottom}} + R_{\text{CNT}} + R_{\text{cnt}} \] (2.2)

Elimination of contact resistance need to be made since the resistance of metal layer and the contact resistance of metal and CNT bundle do matter more or less. A new method of obtaining the contact resistance is presented here. Put \( V_{\text{out}} \) probe on the same pad with \( I_{\text{out}} \). Then all relative resistances changed into

\[ R_1 = R_{\text{con}} \]
\[ R_2 = R_{\text{con}} + R_{\text{metal-top}} \]
\[ R_3 = R_{\text{con}} + R_{\text{metal-top}} \] (2.3)

the total resistance measured is expressed by

\[ R_{\text{total}02} = 3R_{\text{con}} + 2R_{\text{metal-top}} + R_{\text{CNT}} \] (2.4)

Total resistance \( R_{\text{total}01} \) and \( R_{\text{total}02} \) could be calculated by Ohm’s Law from I-V curves measured. \( R_{\text{metal-bottom}} \) and \( R_{\text{metal-top}} \) could be obtained by calculation with known resistivity and size of metal pads. With two unknown quantities \( R_{\text{CNT}} \) and \( R_{\text{con}} \) and two equations, the unknown quantities could be calculated. Details of calculation with measured data would be presented in Chapter 4.

2.4. DIAMETER AND PITCH OF CNT BUNDLES

Based on the measurement method requirements and all simulation results, CNT bundle size differed as 20 um, 50 um, 100 um, 200 um in the simulation. 40 um, 80 um, and 500 um were also designed during the mask design. As for the pitch, contact aligner exposure was taken into situation, then the smallest pitch was set as 100 um.

2.5. MASK DESIGN

For the fabrication of interposer, which is based on CNT growth and polymer spin coating and metal pattern, masks were designed. Interposer size, pitch have been discussed and simulated in sections above. With all these diverse parameters and Lab requirements, contact aligner was chosen as the exposure tool. Only in this way, can we obtained different sizes of interposer as much as possible. According to the design, two layers of masks for 4 inch silicon wafer were required, CNT bundle and contact metal layer respectively. Pattern layers are shown in Figure 2.10, and the full wafer screen shot is shown in Figure 2.11.

Metal pattern had a overlay more than 20 um on each side over the CNT bundles. The reason behind it is that CNT bundles grown on Fe nanoparticles, which could cause iron contamination. Then metal should
cover all CNT bundles with alignment mismatch being taken into consideration.

Pattern of different parameters are placed differently in this full wafer view since the processing might not be very conducted uniformly everywhere on the wafer, then discrete locations have higher chance to obtain desired device.
2.6. Conclusion
Flexible interposer as a connection block in flexible electronics requires mechanical flexibility and electrical conductivity. Requirements on interposer every components are well listed and discussed. Simulation results on electrical performance with diverse pitch or size are conducted and presented. Based on the simulation results and fabrication rules, masks were designed for CNT growth and metal pattern. Measurement method on CNT bundles is presented, with detailed explanation on inputs and output contacts, equivalent resistance circuit included.
In this chapter, details of fabrication of carbon nanotubes and PDMS based interposer device are presented. The process of CNT and PDMS based flexible interposer is finished with clean room fabrication compatibility. CNT growth and PDMS processing are critical processing procedures during process. PDMS wet etching process and metal pattern coverage are deliberated as main challenges. The fabrication devices are demonstrated, followed by discussion and realization about improvements on fabrication technology.

### 3.1. Flowchart Design

The fabrication of interposer device is based on standard thin-film process, including photolithography, metal evaporation and wet/plasma dry etching. Basic method of this flexible interposer fabrication is getting some vertically aligned CNT bundles grown on a silicon substrate, then applying PDMS by spinning for polymer infiltration into CNT bundles. PDMS wet etching to expose CNT top end for the following contact metal coverage. CNT growth would decide the quality of conducting vias, and PDMS wet etching would effect the connection between CNT bundles and metal. CNT growth, PDMS wet etching, and metal pattern are regarded as critical procedures.

Detailed process of flexible interposer are listed schematically in Figure 3.1, and main procedures are described below, while full fabrication flow chart is attached in appendix.

1. The fabrication of flexible interposer film required double side polished 4 inch p type silicon wafers with alignment markers on both sides as substrates. Alignment markers on the front side and back side were mirrored.

2. Catalyst pattern was made with negative photoresist exposure method, followed with Fe evaporation and lift off.

3. CNT grew by LPCVD method. PDMS curing was conducted on hotplate after PDMS infiltration on CNT forests.

4. Contact metal pattern was manipulated using Al/Si. Metal sputtering and etching were handled with temperature well controlled.
Figure 3.1: Schematic of processing flow for CNT and PDMS based interposer
3.2. **DOUBLE SIDES ALIGNMENT MARKER PROCESS**

Fabrication of interposer requires two layers of masks as discussed in chapter 2. One is used for catalyst pattern, and the other one is used for contact metal layer pattern. Corresponding steps of two mask involves steps in Figure 3.1 were (2) and (10), respectively. Alignment at the first time is normal lithography of alignment makers on the mask and the one on the front side of wafer. At the second time, the lithography of metal layer pattern need to align alignment makers on the mask and substrate wafer when there is PDMS film on the front side of wafers. The refraction index of PDMS would cause displacement of exposure if alignment is conducted on the front side. Then the alignment should be conducted between mask and alignment markers on the backside. Details of this back side alignment are expressed in appendix.

3.3. **CNT GROWTH**

CNT bundle was taken as electrical conductive vias made CNT growth a critical processing step since results of CNT growth could determine the electrical property of CNT bundles. CNT growth was conducted by wafer with catalysts and supporting layers on it processed in AIXTRON BlackMagic Carbon Nanotube Evaporator on wafer with catalysts and supporting layers on it. Some SEM images of CNT bundles are shown if Figure 3.2. Figure (a) and Figure (b) presented the test structures with CNT bundles in different sizes and different pitch. Figure (c) and Figure (d) showed the bottom and top view of CNT bundles, respectively.

![SEM images of CNT bundles grown at 650 C\(^\circ\) using LPCVD method (a), measurement structure for 50 um CNT bundle (b), measurement structure for 20 um CNT bundle (c), close up image of bottom vertically aligned CNT bundles at the bottom (d), close up image of vertically aligned CNT bundles on top](image_url)

Fe was chosen as the catalyst and Al\(_2\)O\(_3\) as supporting layer in this process. Utilizing supporting layer of alumina allows long and dense vertically aligned growth. The maximum CNT length could reach a height higher than 400 um. With elevated temperature, iron particles start to interact with the substrates, and then
diffuse into the substrates. Heated catalyst particles meet the hydrocarbon vapor, then the vapor disintegrate into hydrogen and carbon. Carbon atoms would diffuse into the catalyst particles, and hydrogen gas would flow away. With the carbon atom dissolved until overstep the solubility surface limit, the carbon atoms start to compose a crystallized cylinder due to van der Waals force, without dangling bonds. Fe-Al$_2$O$_3$ made nanoparticles diffused into the substrate deeper than it was in the tip-growth method. It would not be possible for tubes to push the metal particles up in tip-growth model. Then tubes grew at the bottom. The combination of Fe and Al$_2$O$_3$ fitted the base-growth model.

Supporting layer and catalyst layer are not formed in the same operation procedure. 10 nm Al$_2$O$_3$ layer was first produced by pure Al and oxygen gas flow, followed by catalyst area pattern. Evaporation of Fe generated a layer of iron nanoparticles on the surface of exposed wafer area and remained photoresist area where has negative photoresist as a protective layer. Lithography in this step might cause thin layer of Al$_2$O$_3$ loss because of effect from developer solution Al$_2$O$_3$. Then lift off was conducted using N-methyl-2-pyrrolidone (NMP) at 70°C, a stirring at 250 rpm to remove the rest photoresist as well as iron particles evaporated on it. Whether the pattern Fe layer could be observed with microscope or not depended on the thickness of catalyst. A layer of 5 nm Fe could be observed under optical microscope while 1.5 nm layer of Fe could not be inspected.

Growth time decides the length of CNT bundles to a great extent before CNT growth reach saturation, when other parameters such as temperature, catalyst, supporting layers are fixed. The curves in Figure 3.3 illustrates the relationship between growth time and the final length. There is an obvious boundary between two different growth rate. At the beginning, CNT bundle grew quickly with a growth rate higher than 1.2 um per second. With growth time longer time than 2 minutes, CNT growth rate was slacken, decreasing to only 0.9 um per second.

![Figure 3.3: CNT growth time versus final height](image)

High precision pattern of CNT bundles demands accurate catalyst pattern because of the synthesis mechanism. CNT grows strictly only on catalyst area according to CNT synthesis mechanism, which was clarified by experiment results. In figure 3.4 (a), it was clearly shown that the patterns on mask were designed as circles in black line, and the exported data for mask fabrication utilizing a octagon approximation in blue line. Figure (b) demonstrated the corresponding octagonal prism shaped CNT bundles. This discrepancy was caused by poor approximation with low resolution during mask data exporting. Most of circles-shaped pattern in the
3.3. CNT GROWTH

design are conducted with approximation into polygon, especially pattern with a size smaller than 100 um. The smaller size the pattern is, the worse approximation is made. The worst case happens with the smallest pattern with a size of 20 um. It is shown as a square with SEM inspection on corresponding CNT bundle grown on it. Rough resemblance makes CNT bundles lose the original shape, and then affect the CNT bundle resistance measurement because of area loss.

Figure 3.4: Polygon shaped mask approximation and CNT comparison (a). original design and approximation of circle pattern (b). octagonal prism 50 um CNT bundle corresponding to mask pattern with rough approximation

Defects of catalyst layer bring out corresponding defects on CNT forests grown. SEM images of CNT grew at 600 °C are presented in Figure 3.5. Figure (a) exhibits the deficiency of nanotubes. This hiatus of catalyst is caused by photoresist residuals. Catalyst particles were evaporated on the residuals, and then got removed during lift off processing, causing catalyst lost. In Figure (b), curly nanotubes are presented. Actually, with pure Fe as catalyst and alumina as supporting layer, CVD method produces only vertically aligned CNT. The curly CNT might be due to the catalyst quality. Substrate with catalyst for (b) sample had been preserved longer time than (a) sample. This assumption has not been settled yet. Catalyst oxidation remains as a hypothesis.

Figure 3.5: SEM images of CNT bundles with defects (a). loss of CNT bundles because of particles on mask (b). curly CNT presents as well as well align CNT bundles

Temperature during the process is a momentous parameter. SEM images of CNT grown at different temperature are presented in Figure 3.6. All these samples take 5 nm thick of Fe as catalyst layer, and 10 nm of alumina as catalyst supporting layer. Growing time is fixed at 60 seconds. CNT length are labeled in the images. At 500 °C, CNT height is only about 726 nm, and at 550 °C, CNT height is about 8.4 um. At higher temperature 600 °C, CNT height reaches 38.4 um. CNT length have a length up to 113 um at 650 °C. With these
SEM images and measurement data, temperature effect on CNT growth is revealed. Owing to the effect of temperature, CNT height on the same wafer also alters a bit. In the CNT CVD machine chamber, temperature is not uniformly located, which causes the non-uniformity of CNT grown. The difference on CNT height makes following steps much harder.

Figure 3.6: CNT forests grown for 60 seconds at different temperature using the same catalyst and same supporting layer (a) 500°C (b) 550°C (c) 600°C (d) 650°C

3.4. PDMS INFILTRATION

PDMS infiltration is a step right after CNT growth to add isolation material around CNT bundles. Mixing Sylgard 184 prepolymer and curing agent, in a weight ratio of 1:10 was necessary before starting the PDMS infiltration on CNT bundles. Several minutes of waiting was necessary for complete interaction of these two constituents. The interaction between two constituents is done until there is no more bubbles coming out. Degassing in conditioning mixer machine is conducted for better mixture, and reduce of bubbles under the function of centrifugal force. Pour mixtures slowly at the centre of the wafer with CNT bundles on it, and let PDMS spread gradually to the edge of the wafer. Bubbles should be avoided during pouring, and the wafer should be placed in a flat container. Wafer, together with the container should be preserved in a vacuum oven for at least 15 minutes. This vacuum step would remove the bubbles coming out of CNT bundles since there are lots of air inside the porous nanotubes. Air bubbles in CNT bundle would be pumped out in a vacuum oven. Wafer with PDMS could be took out when there are no bubbles coming out from CNT/PDMS composite surface.

Final thickness of PDMS layer mainly depended on spin speed and spinning duration when use spin coating as the approach to spread PDMS on CNT forests for a fine uniformity. Figure 3.7 presented the PDMS layer thickness as a function of spinning speed with experiments results comparison. If ratio of curing agent
and PDMS has been changed, then the trace would change. The ratio of PDMS and curing agent will affect the final thickness [43] [44].

![Figure 3.7: Sylgard-184 PDMS spin coating thickness as a function of spinning speed](image)

The line in the figure was the literature thickness value while the dots were experiments data obtained in MEMS Lab. The full spinning program is composed of three steps. At first, relative low speed (for example, 200 rpm) for 2 seconds is utilized for spreading out the PDMS. Then the dominate spinning speed for 30 seconds decide the thickness of PDMS layer. Finally, a 5 seconds spinning (usually 500 rpm) could help with get rid of residuals on the edge. The spinning speed in the Figure 3.7 is the dominate speed in the second step. Generally principle of spinning is that the product of final thickness and square root of spinning speed is a constant, as illustrated in blue line in the figure. For experiments results, a 1000 rpm for 30 seconds bring about 90 um of PDMS after curing, which fits the line perfectly. However, there is a ring of thicker PDMS on the edge with a width about 2 mm. The PDMS thickness in middle are quite uniform.

![Figure 3.8: PDMS infiltration in CNT bundles (a). top view of whole CNT bundle with PDMS surrounded (b). closed up image of a layer of PDMS composite (c). close up image of certain nanotube with obvious PDMS](image)

The sample is then cured in the oven for 60 minutes. An alternative method is baked on a hotplate for 15 minutes at 90 °C. After PDMS get cured, penetration of PDMS into CNT is shown in Figure 3.8. Samples are taken from CNT and PDMS composite tearing from the substrate. These SEM images proves that PDMS
did exist between nanotubes. Figure (a) shows a CNT/PDMS composite surrounded by PDMS. Figure (b) presents that CNT are well aligned vertically. Figure (c) illustrates that CNT stays in PDMS, not dissociative. PDMS infiltration might fail because of poor vacuum before curing.

3.5. PDMS Wet Etching

PDMS etching is the most challenging processing step during fabrication. CNT bundles top end need to be exposed to connect with the contact metal. Then PDMS layer need to be etched until its thickness is smaller than CNT height to get CNT bundle top end be exposed in air. There are two methods of PDMS etching, dry etching and wet etching. The dry etching method of PDMS works is that Garra et al. found that a 1:3 mixture of O$_2$ and CF$_4$ resulted in an optimum etch rate of 0.33 $\mu$m/min [45]. The other way of PDMS etching is using a solution of N-methyl pyrrolidinone (NMP) and tetra-butyl ammonium fluoride (TBAF) in a ratio of 3:1, respectively [41]. Wet etching was the way utilized here since dry etching machine might be contaminated by Fe, which was not allowed in cleanroom. A fine PDMS wet etching result should be as presented in Figure 3.9. CNT bundles top end surface was totally visible and without obvious PDMS residuals.

PDMS surface after wet etching is illustrated in Figure 3.10. The SEM image in figure (a) presents that the surface of PDMS is relatively flat except for some holes. The optical microscope image in figure (b) shows also little holes more clear than SEM image.

PDMS residue on the top surface of CNT bundle is possible because of the CNT non-uniformity caused by
the temperature difference in the chamber as shown in Figure 3.11. SEM images presents in figure (a) showed a thin layer of PDMS residuals still remained, covering most area of this CNT bundle. PDMS residuals exists at the center, and also on the edge, which indicates the non-uniformity of etching. This discrepancy might be caused by stirring of etching solution. To ensure a constant etch rate, stirring is utilized for refreshing the solution near the PDMS surface. Continuous stirring could cause height difference of solution liquid, and then result in etching discrepancy. Figure (b) presents also the residue of PDMS on the edge of a CNT bundle. It is obvious that PDMS was etched away layer by layer.

Some cracks could be found in Figure 3.11. Close up figures of cracks are shown in Figure ?? (a) presents that on the top of CNT bundles, small quantity of PDMS still remain on single tubes, and PDMS in the gap is all etched away. The close up images in Figure (b) on the right exhibits this phenomenon more clearly. These cracks are caused by etching solution bath. When CNT bundle get rid of PDMS, it get in contact with liquid. The immersion lead to cracks. Then the etching solution could reach the deeper place in the gap. PDMS in the gap is etched away. Existence of cracks in CNT bundle makes the surface become rough, which would cause some problem in following metal pattern (will be discussed later). Not every CNT bundles have cracks. CNT bundles with a size smaller than 100 um hardly have this problem.

Iron cleaning is manipulated since bare CNT bundles top surface are uncovered along with iron particles which served as catalyst. Iron cleaning was carried out in HF and NH₄F mixing solution. Silicon oxide on the backside of wafer would be removed at a rate 1.3 ± 0.2 nm/s at 20 °C. Etching time could be set as 5 minutes. Iron particles interacts with the solution, and become iron ions, which would be rinsed away during 10 minutes deionized water rinsing. This step should be handled very carefully since the PDMS layer might be stripped as shown in Figure 3.12 (b). Figure (a) illustrates a fine etched and cleaned wafer with CNT/PDMS
on it.

Figure 3.12: Composite film after PDMS wet etching and iron cleaning (a). Complete CNT and PDMS composite film on silicon substrate (b). CNT and PDMS composite film stripped off from silicon substrate resulted in film crimp

Long time wet etching and cleaning of PDMS composite film in liquid solution would result in absorption of water since PDMS is porous material with holes (indicated in Figure 3.10). Water vapor would escape from the film at elevated temperature, such as during metal sputtering. A 30 minutes of heating at 80°C should be conducted to prevent degassing in the next processing steps, especially those procedure need to be conducted in vacuum condition.

3.6. Metal Pattern

Contacts are important for interposer since good contact promises good connection for CNT vias and peripheral circuits. Metal Al with 1% silicon (Al/Si) was chosen as the contacts material. Usually, for CNT as connecting material, 100 nm thin layer of Ti with 2 um Al/Si was generally the way of contacts [19]. However, with the existence of polymer, high tense metal Ti resulted in cracks. Sputtering of Ti and Al/Si on PDMS layer was not very satisfying, as shown in Figure 3.13. Figure (a) presented the photo of PDMS layer with thin Ti layer and Al/Si layer while figure (b) showed the result with only Al/Si. It was clear that cracks were caused by Ti. The absence of Ti particles would make the contacts between CNT and metal layer worse than the one with Ti since Ti particles could get into tubes. Sputtering temperature during process was well controlled at room temperature by special recipe, which was composed of repeated steps combined by 0.5 um metal sputtering and cooling down each time. Otherwise, the PDMS layer would be burnt.

Figure 3.13: Sputtering of metal on PDMS layer (a). Ti and Al/Si layer resulted in lots of cracks (b). Al/Si only resulted in smooth surface
3.6. Metal Pattern

Cracks made by CNT immersion in PDMS wet etching solution bring out metal sputtering defects. Optical microscope images of CNT bundles after contact metal sputtering are shown in Figure 3.14. Figure (a) is a cross section of the cracks, and also demonstrated two focus planes for close up images. Figure (b) is the top view of a CNT bundle with a diameter of 500 um, which is the largest bundle in this project with the most cracks. Close up images of cracks were shown in figure (c) and (d), focusing on different planes as illustrated in figure (a). Shining particles are Al/Si. The surface and bottom of cracks are covered by metal while the cracks slope are not. Height difference between top and bottom of cracks indicates that metal layer is not continuous, which could result in error in resistance measurements.

![Figure 3.14: Al/Si sputtering on CNT bundle with cracks (a). bundle top view (b). cross section of gaps (c). close up image of gap focusing on the first focus plane (d). close up image of gap focusing on the second focus plane](image)

Perfect coverage of CNT bundles by metal layer couldn’t be guaranteed even though sputtering has a good step-coverage because of the resistance of cracks. Then the possibility of CNT exposing in air during metal etching exists. When the idea of covering gap with metal failed, some efforts on photoresist coverage had been done to solve this problem. A 12 um thick layer of photoresist method was employed (the normal procedure usually requires only 4 um for photoresist thickness), which didn’t work well. Then a coating recipe with thick photoresist and topology changing when released the photoresist. The movement of releasing tube would spread photoresist more evenly. Exposure time increased with the increasing photoresist thickness.

Al/Si plasma etching at 50 °C is conducted in Kavli Lab, using Oxford Instrument Plasmalab System 100. The etching recipe started up with temporization, then followed with breakthrough for alumina at the surface. 18 minutes of etching is required for 2 um Al/Si based on many experiments. Cl₂, BCl₃ are mixed as the gas utilized for Al etching in a ratio of 1:6. N₂ gas flow is essential for the last step pump out. 30 seconds of rinsing in water could prevent the residual processing gas from keeping etching after being taken out from the etching machine. In the first 15 minutes of etching, no obvious visible abatement of Al layer was observed. Only in the last three to four minutes, Al layer was etched away at a eyeable rate.

Figure 3.15 presents the SEM microscope images of test structure after Al/Si etching. Figure (a) shows the test structure of interposer device while all CNT bundles are covered only Al/Si layer could be inspected.
Close up image is shown in figure (b). Nice metal layer with clear edge is observed. Sputtering metal had a very nice step coverage on pattern. PDMS substrate is also illustrated in the figure.

![SEM images of test structure after Al/Si etching (a). top view of several test structures (b). close up image of a corner illustrated fine boundary between Al/Si and PDMS](image)

3.7. CONCLUSION

Fabrication of interposer device based on CNT and polymer is presented in this chapter. Lithography, metal pattern and thin film processing are critical procedures. Backside alignment is demonstrated because of the existence of polymer on front side of wafer. Large quantities of CNT grew at diverse conditions are obtained and investigated. Diverse results obtained from different processing methods are compared. Interposer device based on CNT and PDMS is fabricated through a combination method of each procedure. The final interposer have a thickness of about 100 um, and vias diameter differed from 20 um to 500 um. Only structure with a diameter from 50 um to 100 um should be measured since there are bending and cracks on other size CNT bundles, and cannot provide with reliable results.
In this chapter, measurement results of interposer device are presented. Crystallinity of CNT bundles are inspected by Raman spectroscopy. CNT samples grew at diverse temperatures are measured for CNT quality inspection. Raman spectroscopy results of a CNT sample after PDMS wet etching are compared with the results before PDMS infiltration. Electrical measurements are conducted on Cascade probe station. I-V curve and resistance of the device are demonstrated. The resistance deviation along with film stretching are also exhibited.

4.1. Raman Spectroscopy of CNT
Raman spectroscopy is a commonly used method for CNT quality inspection. The quality of CNT is usually defined as low or high, hardly to be discussed by accurate numbers, and it has large effect on electrical property as discussed in Chapter 1. The results of Raman Spectroscopy would be presented with numbers and figures, which would be a quantitative outcome, rather than qualitative result get from TEM. Raman spectroscopy is a method relied on inelastic scattering of monochromatic light. Incident lights interact with molecular vibrations, photons or other excitation in samples. Absorption and release of energy results in different scattering rays, which could be detected by a spectrum detector. Raman spectroscopy only need small size sample, and no direct contact required, which means no destruction on sample. For MWCNT samples grown in this project, green laser with a wave length of 514 nm is utilized for crystallinity check. Intensity ratio of D-band (around 1350 cm\(^{-1}\), defects) \(I_D\) and G-band (around 1582 cm\(^{-1}\), Raman active mode of graphitic materials) \(I_G\) are important parameter related to crystal quality determination.

Raman spectra of MWCNT bundles with different locations on the same wafer is conducted. Results are shown in Figure 4.1. Figure (a) displays four locations of measured CNT bundles, along the line vertical to the primary flat of P type wafer, figure (b) presents the ratio change along the distance from the first flat. Smaller ratio of \(I_D/I_G\) means better crystallinity. As illustrated in the figure that the ratio of \(I_D/I_G\) increases along the distance, which means that the crystallinity quality decreases. CNT bundles near the thermometer in LPCVD chamber have the best quality.

Raman spectra of MWCNT samples grew at different temperatures are presented in Figure 4.2. All figure data points are mean data from three times measurements. Temperatures ranges from 500 °C to 700 °C, with 50 °C step. All samples grew for 60 seconds using 10 nm of Al\(_2\)O\(_3\) as supporting layer and 5 nm Fe as catalyst. Obviously, in the first order region two strong bands D-band and G-band are observed, at 1350 cm\(^{-1}\) and
Characterization of Interposer

1582 cm$^{-1}$. The ratio of $I_D/I_G$ for CNT samples grew at 500 C°, 550 C°, 600 C° and 650 C° are 1.53, 1.47, 1.38 and 1.23, respectively. Raman results of samples at different temperature presents that CNT bundles grown at higher temperature have better quality than those grown at lower temperature.

Raman spectra of the same wafer after CNT growth and PDMS etching procedures are conducted to check the PDMS etching process effect on CNT quality. Results of this comparison are shown in Figure 4.3. Figure (a) displays that CNT quality right after CNT growth is quite high, the ratio of $I_D/I_G$ is 0.94, while Figure (b) is the result of CNT after PDMS wet etching, with a $I_D/I_G$ ratio of 1.24. In Figure (c), CNT in the gap (specified in Figure 3.11) shows a high quality with $I_D/I_G$ ratio only 0.49. The high quality CNT is from the middle part of CNT bundles. The reason behind it might be that CNT middle part grown at a stable situation, without the temporization time at the beginning or fading time at the end.

A special intensity peak at around 2875 cm$^{-1}$ is found (in blue circle). This peak is identified as PDMS structure Raman shift since figure (4) is the measurement results for PDMS only presented the same peak around 2875 cm$^{-1}$. High quality CNT and PDMS presents in figure (c) at the same time demonstrated that
there is PDMS residua even on high quality nanotubes. These residual might cause higher resistance than that with only nanotubes.

![Graph showing Raman shifts of CNT bundles before and after PDMS processing.](image)

**Figure 4.3:** Raman shifts of CNT bundles before and after PDMS processing (a). CNT bundle before PDMS infiltration has a $I_D/I_G$ ratio of 0.94 (b). CNT bundle after PDMS wet etching has a $I_D/I_G$ of 1.24, much worse than before (c). Cracks on CNT bundle after PDMS wet etching has a $I_D/I_G$ of 0.49, along with other peak around 2875 cm$^{-1}$ (d). Raman shifts on PDMS only with a Raman peak around 2875 cm$^{-1}$

### 4.2. ELECTRICAL CHARACTERIZATION

Electrical measurements performed on test vias through probe station for different size and different length CNT bundles are conducted in this section. Calculation on resistance of diver size of tested bundles are presented, and compared. Contact resistance of 100 um bundle is calculated roughly.

The probe station for measurement is configured with six probes, and each probe could provide with input current or voltage source and output results sense at the same time. This advanced function made it possible of using two probes rather than 4 probes for 4-probe measurement method. Accuracy of a probe providing with source and sensing the signal has been checked through comparison between input probe sensing result and another probe sensing result at the output. Two results turned out to be exactly the same, which meant the sensing result obtained from input probe was reliable.

#### 4.2.1. I-V CURVE

I-V Curve is measured for two connected bundle using two probes. As illustrated in Figure 4.4.

![Diagram showing I-V curve measurement setup.](image)

**Figure 4.4:** Bundles connected method during electrical measurements

The resistance measured in this method is equal to the one expressed in Equation 2.4.
Typical I-V characteristics for diverse size of two connected CNT bundles grew at 650 C° are presented in Figure 4.5. CNT bundle size are 100 um, 80 um, and 50 um, respectively. All I-V curves in Figure 4.5 display good linearity. Resistance obtained from this curve are two connected CNT bundles having the same size, having a resistance about 300 Ω.

\[ R_{total2} = 3R_{con} + 2R_{metal-top} + R_{CNT} \]  
(4.1)

Figure 4.5: I-V characteristics obtained from CNT bundles grown at 650 C° with a size of 100 um, 80 um, and 50 um

CNT bundles with a diameter of 20 um, 200 um and 500 um are not measured since the contact metal on these CNT bundles failed to make a perfect coverage. Measurement results on these bundles are not reliable since driven current couldn't pass through the whole CNT bundle.

IV curves obtained from CNT bundles with vertically applied force on contact metal pad is presented in Figure 4.6, comparing with normal contact I-V result. A normal contact for CNT/PDMS composite is defined as probe scratch on the Al/Si pattern without obvious deformation could be observed by naked eye. A contact with vertically applied force on contact metal pad is defined as probe contact causing a visible deformation going down for about 4 um.

It is obvious that the resistance of CNT bundles with vertically applied force had larger resistance than the one with normal contact. The normal contact CNT bundles had a resistance about 297.35 Ω while CNT bundles with vertical applied force had a resistance around 923.1 Ω. A reasonable solution for this resistance difference is given: For normal silicon substrate wafer measurement with probes, probes need to scratch on the contact metal to guarantee well contact, sometimes for pads made of Al, even brake through the Al₂O₃ layer to realize contact between probe and Al is required. For flexible interposer device on PDMS substrate,
the probe would bring force on the elastic substrate causing deformation, as illustrated in Figure 4.7.

Figure 4.7 (a) illustrates that the light blue PDMS material is deformed by the probe force. It transforms into the orange dashed line. Then the curly nanotubes are as illustrated in Figure 4.7 (b). On the left is the CNT before the applied force, then nanotubes get contact with other CNTs after the force applied. Nanotubes get contact with each other, even with themselves at different parts. These contact resistance between nanotubes bring out resistance increasing.

### 4.2.2. Resistance Calculation

As explained in Chapter 2, method to calculate the resistance could be realized by two times measurement. The first measurement is the one for I-V curves, as discussed before. The second time measurement is illustrated in Figure 4.8.
The resistance measured in this is expressed as 2.2.

\[ R_{\text{total}1} = 4R_{\text{con}} + 2R_{\text{metal-top}} + R_{\text{metal-bottom}} + R_{\text{CNT}} + R_{\text{cnt}} \]  
(4.2)

Applied addition and subtraction with these equations 2.2 and 2.4, the resulted formula were:

\[ R_{\text{total}1} + R_{\text{total}2} = 7R_{\text{con}} + R_{\text{metal-bottom}} + R_{\text{metal-up}} + 3R_{\text{CNT}} \]  
(4.3)

\[ R_{\text{total}1} - R_{\text{total}2} = R_{\text{con}} + R_{\text{metal-bottom}} + R_{\text{CNT}} \]  
(4.4)

Values of \( R_{\text{metal-top}} \), \( R_{\text{metal-bottom}} \) could be calculated with metal pattern resistivity, thickness and area.

\[ R = \rho \frac{l}{S} \]  
(4.5)

where \( \rho \) is the electrical resistivity of metal, \( l \) is the length of metal pads, and \( S \) is the cross section area of contact metal. For top metal layer Al, with a length of 2 \( \mu \)m, a cross section area of 10000 \( \mu \)m\(^2\), and a electrical resistivity of 2.83E-08 \( \Omega \)m. The bottom Au layer has a electrical resistivity about 2.40E-08 \( \Omega \)m. Resistance of top and bottom metal are calculated as 0.0566 \( \Omega \), and 0.06 \( \Omega \), respectively. These two resistance of metal are on 10\(^{-2}\) level, which could be ignored, compared with hundreds of Ohms of CNT bundle resistance.

Measurements conducted using the first method for 100 um CNT bundles is around 297 \( \Omega \). The resistance result using the second method for 100 um CNT bundles is about 168 \( \Omega \). Contact resistance and CNT bundle resistance could be calculated when

\[ R_{\text{cnt}} = R_{\text{CNT}} \]  
(4.6)

This equation is feasible since the to be measured CNT bundle and the bundle serves as conducting vias have the same size and length, which result in the same resistance theoretically.

The contact resistance between metal and 100 um CNT bundle is calculated around 11 \( \Omega \), and the resistance of CNT bundles is calculated about 128 \( \Omega \). The resistivity of CNT bundle are not presented here since the area of CNT bundles is not well defined because of the rough approximation on pattern during mask fabrication, and resistivity calculation is strongly related to bundle area.
4.2.3. **Conclusion**

Raman Spectroscopy of CNT samples grown at different temperatures presented an increase in quality with higher processing temperature. The quality comparison on the very same sample before PDMS infiltration and after PDMS wet etching is compared. Due to the cracks on CNT samples, the middle part CNT is found with very good quality, and the PDMS infiltration and wet etching processing did cause some negative effect on the quality of CNT bundles. Electrical measurements are conducted on probe station. Linear I-V curve of CNT bundles are obtained, with which CNT bundles resistance could be calculated on hundreds Ohm level.
In this chapter, some possible improvements on processing are listed without taking lab conditions into consideration. Some future work field about CNT/Polymer composite interposer are discussed.

5.1. DISCUSSION ABOUT PROCESSING OF FABRICATED FLEXIBLE INTERPOSER

Some unknown, or unpredictable factors might effect the reliability of interposer during fabrication of CNT/PDMS flexible interposer. There are some possible solutions to these problem, which are not realized during processing because of processing machine absence or prohibition because of instruments contamination rules.

5.1.1. CNT BUNDLE GROWTH

As discussed that CNT bundles with a size as small as 20 um or even smaller size will bend after CNT growth. Measurements on CNT bundles with size is not conducted since CNT height is relatively large, and not well vertically aligned, as illustrated in Figure 5.1.

![Figure 5.1: CNT bundle bend of a pattern with 20 um diameter (a). CNT bundle with a size of 20 um, and height about 290 um bend seriously (b). CNT bundle with a size of 20 um, and height about 82 um bend slightly](image)

It is obvious that with CNT bundles having a diameter of 20 um with a higher height of 290 um has more
serious bending phenomenon than the one with a shorter height of 82 um. Actually, CNT bundle having a
diameter could also grow on the substrate well vertically aligned with a height less than 60 um (summarized
based on my experiments results). The relative high height, is compares with its diameter. Bending of a
bundle with the same height of its diameter hasn’t been observed during all SEM inspection. Actually, the
final height was settle as 90 um since a relatively high height has better processibility. If there is a requirement
on shorter interposer, the fabrication of interposer could be achieved by less height CNT growth on silicon
substrate, which could be realized easily by reducing growth time without decreasing CNT quality.

Smaller height of CNT makes it possible to make CNT/PDMS composite interposer with size smaller than
20 um since CNT bundles could remain vertically aligned.

5.1.2. ALTERNATIVE METHODS FOR PDMS WET ETCHING
PDMS infiltration on CNT bundles made all CNT bundles are covered by PDMS. Wet etching conducted for
removing the top PDMS layer, and let CNT top ends exposed. However, the top ends of CNT bundles after
PDMS wet etching still remains some difference with CNT bundles without PDMS processing, as illustrated
in Figure 5.2. PDMS wet etching in Figure 5.2 (b) has been conducted with PDMS wet etching for a long time.
PDMS in cracks are all removed away, with only nanotubes remained. However, there is still PDMS residue
on the top ends of PDMS. It is possible that PDMS get into the tube successfully, which is hard to be removed.

An alternative method of solving this problem is applying Chemical Mechanical Polishing (CMP), as shown
in Figure 5.3. Removing the top ends of CNT along with PDMS layer above them would expose the cross sec-
tion of CNT bundles. This CMP step would also remove the twisted CNT ends (illustrated in Figure 5.2 (a))
5.2. **DISCUSSION ABOUT IMPROVEMENTS OF FLEXIBLE INTERPOSER**

5.2.1. **DISCUSSION ON CNT BUNDLES**

Chirality of CNT is still not controllable even though with some change of chirality has been observed. No clear explanation is proposed yet [46] [47] [25]. MWCNT has complex and unpredictable chirality because the chirality of MWCNT is a superposition of several (number of shells) SWCNT chirality. Some study on the electrical conductivity in PDMS composite was reported by E. Liu et al [48]. A 3D model of MWCNT in PDMS was build, the results are as illustrated in Figure 5.4. Electrical conductivity changes as the alignment angle changes, which is illustrated in Figure 5.4. The worst case happens when CNTs are horizontally aligned. The simulation result supports that there is a right angle for CNT/PDMS flexible interposer well aligned to achieve the best electrical conductivity. Vertically aligned is the reasonable way to realize it for now.

![Figure 5.4: Relationship between alignment and electrical conductivity](image)

For realizing excellent properties in real application, array-spun MWCNT yarns is studied by M B. Jakubinek at al [49]. As illustrated in Figure 5.5, CNT yarns (also known as CNT fibers) fabricated by spinning from the sides of vertically-aligned CNT arrays for nice electrical conductivity. This twisted yarn is a possible way to improve CNT properties since many great properties of CNT need to be translated to macroscopic materials in real application.

![Figure 5.5: CNT yarns (a). Spinning is utilized for fabrication of CNT yarns from array (b). SEM image of CNT yarn with a diameter of 34 μm. Twist is about 1.2E4 m⁻¹, and the outer twist is about 30 degrees](image)

Applied force on CNT/PDMS composite brings out electrical performance change as presented in Chap-
It is also discussed that the resistance change is caused by extra contacts between nanotube walls with other nanotube walls or themselves. A study about applied force on CNT pillars was reported by Rene H. Poelama et al [50].

The compressive failure images of uncoated CNT bundles is shown in Figure 5.6.

The compressive failure images of CNT bundles with a 5.6 nm thick of Si-C coating is shown in Figure 5.7.

Comparison between CNT bundles with and without coating presents a possibility for future CNT based vias. It is possible to have appropriate coating on CNT bundles for better aligned vertical cracks rather than twisted with each other when vertically aligned CNT vias encounter vertical force from out-of-plane direction.

5.2.2. IMPROVEMENT ON POLYMER
High degree of thermal stability of polyimide makes it a commonly used polymer in MEMS packaging technology. It has a coefficient of thermal expansion close to copper, making it be compatible with copper, and withstand processing and working at elevated temperature. CNT/Polyimide composite flexible interposer
should be studied in the future for further application. Some experiments about CNT/Polyimide has been conducted (Figure 5.8), with potential results.

**Figure 5.8: CNT/polyimide composite**

### 5.3. **Conclusion**

In this Chapter, some discussion about improvements in processing and further research has been presented. Different methods about CNT growth, polymer processing, and the way of how could nanotube fibers exist in polymer would provide with new idea about future work.
Flexible interposer is a key electrical conducting block in flexible electronics industry, which requires mechanical flexibility and electrical conductivity. State of the art on flexible interposer is generally based on polyimide and metal composite, or metal alloy. However, with physical limitation of metal and electroplating processing on metal, potential material CNT was proposed as electrical conductive vias in configuration of interposer. PDMS with its ease of processibility, constituting a flexible interposer demonstration with CNT. A demonstration of CNT and PDMS provides with the possibility of combination of nanotubes with polymer (such as polyimide, a polymer with better thermal performance than PDMS) could be possible. The proposed interposer device was achieved by cleanroom processing with different size and pitch combination.

A novel flexible interposer based on carbon nanotube and PDMS was proposed and fabricated for a new method of combination of CNT, a material with outstanding electrical property and polymer with good mechanical flexibility as conducting block in 2.5D/3D flexible packaging. Backgrounds on the anisotropic electrical conductivity of CNT and polymer processing were well studied. COMSOL simulation with size and pitch selection provided a reliable support on the electrical performance. With simulation results and fabrication flow chart discussion, masks on contact aligner were designed, protection for preventing machine from iron contamination was taken into consideration. Processing in clean room was conducted on 4-inch p type test wafer. Some efforts about PDMS spin coating, PDMS etching method and metal pattern were made. Finally, a thin flexible film which is composed of CNT and PDMS was made, and performed as conducting block well, being measured through probe station.

**Backgrounds on CNT and PDMS**

Study on backgrounds of CNT and PDMS provides a better understanding with the electrical or mechanical properties, and combination method of these two material could be better proposed. The research on CNT growth mechanism helped with many controllable parameters on CNT quality. A CNT bundle based with PDMS surrounded interposer model was proposed.

**COMSOL simulation on electrical performance**

COMSOL simulation results presented the effect from pitch size, diameter size. With fixed size, pitch had effect on the potential distribution when the pitch was samller than the vias size. With increasing pitch larger than the size of vias, pitch didn't affect potential distribution that much. With fixed pitch, high aspect ratio
vias had better electrical performance. Current density was isolated in CNT bundles only since the isolation of PDMS material.

**Fabrication of Interposer**

Fabrication of a novel flexible interposer based on CNT and PDMS was a challenging since there was no experience could be taken as reference. Lithography, metal pattern, and metal evaporation, sputtering were common used processing during cleanroom fabrication. PDMS infiltration on cNT forest turned out to be a challenging since CNT might bend during spin coating. Wet etching, instead of more steerable plasma etching of PDMS due to contamination rules was a critical processing procedure. This liquid immerse on CNT bundles brought up negative effect on its shape and stability. Cracks caused by the liquid bath of CNT resulted in following possibility of CNT coming out during metal pattern. Lots of experiments on metal pattern have been done. Finally, flexible thin film with interposer measurement structures were fabricated.

**Characterization**

Characterization of CNT and interpose device were conducted. Raman Spectroscopy on the quality of CNT bundles grown under different situation, and the quality of CNT samples processed with different procedures were all checked. The quality of CNT bundles were influenced by many parameter, such as catalyst particles, LPCVD temperature, and liquid bath etc. Electrical property of the fabricated flexible interposer was presented after electrical performance measurement on probe station. I-V curves of CNT bundles were obtained, and resistance were calculated. The contact resistance between metal and 100 um CNT bundle is calculated around $11 \, \Omega$, and the resistance of CNT bundles is calculated about $128 \, \Omega$.

**Discussion about future work**

Several possible methods about the way of CNT fibers in polymer, and alternative choice on polymer are discussed for further research.
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ALIGNMENT MARKER PROCESS

As set forth in the flow chart, after PDMS infiltration and curing, metal layer on top of PDMS substrate layer need to be patterned. Patterning requires lithography, which means alignment markers are requisite. However, with polymer on top of the entire wafer, even though PDMS is transparent, index of PDMS will result in displacement of alignment markers during the alignment exposure. Thus, special alignment was conducted in this project. The normal way of front side alignment and special backside alignment on contact aligner were both presented in Figure A.1.

In this concept figure, light source illuminated uniformly on the wafer through the mask. Photoresist was a relatively thin layer, usually thinner than 4 um, while PDMS was turned out to be thicker than 50 um, the refractive index of this isolation supporting polymer material could not be ignored, just like the same we did on photoresist. Index of refraction could result in displacement of alignment makers when the rays of light pass through PDMS layer. The normal front side alignment method was based on the alignment of alignment markers on the mask and the alignment markers on the front side of to be exposed wafer. Digital cameras were installed above the mask, through the computer connected with the camera, and then images of alignment markers on the mask could be found, and be aligned with alignment markers on the wafer. Alignment and exposure were conducted on the front side of the wafer. For the back side alignment, mirrored alignment markers should be made on the backside of the wafer. Digital cameras were underneath the mask, capturing
the alignment markers on the mask, and storing it on the computer. After the capturing of mask images, wafer should be loaded, and then the cameras under the wafer would search the alignment markers images on the backside of the wafer, then align the back side alignment markers with images captured before. With this rare side alignment, the index of PDMS would result in less displacement of alignment makers, thus lead to higher accuracy.
1. Always follow the "Security and Behavior" rules when working in the Dimes cleanrooms.

2. Always handle wafers with care during processing. Use cleanroom gloves and work as clean as possible.

3. Always check equipment and process conditions before starting a process.

   Directly notify the responsible person and other users when there are problems with equipment operation or contamination. Do not try to repair or clean unknown equipment yourself, and never try to refresh a contaminated etch or cleaning bath!

4. Always clean wafers after several hours of storage before performing a coating, furnace, epitaxy or deposition step.

   Wafers do not have to be cleaned after a furnace or epitaxy step if the next process step is carried out immediately.

   Use the correct cleaning procedure:
   - Acetone or Tepla stripper for photoresist removal
   - HNO3 100% for wafers which do not need a HNO3 65% step
   - HNO3 100% metal for wafers which are or have been in contact with a metal
   - HNO3 100% and HNO3 65% for all other wafers

5. Wafers that are covered with a resist or a metal layer may never be processed in a furnace. Only alloying is allowed for wafers with an Aluminum layer.

6. It is allowed to use the Leitz MPV-SP or Woollam measurement system for layer thickness measurements on the wafers of a process batch. These measurements are non-destructive and without contact to the wafer surface. If these methods cannot be used on your wafer, or when sheet resistance and/or junction depth measurements must be performed, an extra wafer has to be processed for measuring.

7. All substrates, layers and chemicals which are not standard being used in the Dimes 01/02/03/04 or Dimes 01 production processes are considered to be "non-standard" materials, and can be possibly contaminating.

   The use of those materials for processing in the class 100 cleanroom and SAL must always be evaluated and approved by the PAC committee. It is strictly forbidden to use "non-standard" materials without permission.

   Check the PAC "Rules & Instructions" - available on the internet - for more details.

8. Wafers that are contaminated may never be processed in any of the equipment without permission of the PAC committee. Special precautions may have to be taken, like the use of a special substrate holder or container.

9. Always perform all the measurements and inspection steps, and write down the results in your journal and in the result tables in the cleanroom !! The results can be used to check the condition of processes and/or equipment.
STARTING MATERIAL

Wafers taken out of an already opened box must be cleaned before processing, according to the standard procedure.
Wafers taken out of an unopened wafer box do not have to be cleaned before processing.

Notes:
- Fe and carbon nanotubes are potentially contaminating materials. Hence:
  - special precautions are necessary in handling them.
  - the flow chart needs to be approved by the PAC.
- Fe is passivated in pure HNO$_3$ but etches in diluted HNO$_3$
- Fe will remain on the bottom of the holes during carbon nanotube (CNT) growth (base growth)
- CNTs can be damaged by oxygen containing plasma, but are resilient against most etching solutions like HNO$_3$ and HF.
Use double sides polished p type wafer.

**Zero Layer** (On front side)

Have zero layer on the front side (with wafer number), all other process on the backside (without wafer number).

Alignment Marks (Zero Layer on both sides) @ Cleanroom 100

1. **Coating and Baking**

Use the EVG 120 Coater/Developer to coat the wafers with resist, and follow the instructions specified for this equipment. The process consists of a treatment with HMDS (Hexamethyldisilazane) vapour with nitrogen as a carrier gas, spin coating with Shipley SPR3012 positive photoresist, and a soft bake at 95 °C for 1.5 minute.

Always check the temperature of the hotplate and the relative humidity (48 ± 2 %) in the room first.

Use coating **1-Co-3012-zero layer** (resist thickness: **1.4 µm**). Look at the list for the correct program.

2. **Alignment and Exposure**

Processing will be performed on the ASML PAS5500/80 wafer stepper. Follow the operating instructions from the manual when using this machine.

Exposure masks **COMURK**, with job “**litho-Zefwam**”, the correct exposure energy 150mJ.

Batch size: wafer number

This results in alignment markers for the stepper and contact aligner for wafers.

3. **Development**

Use the EVG 120 Coater/developer to develop the wafers, and follow the instructions specified for this equipment. The process consists of a post-exposure bake at 115 °C for 1.5 minute, followed by a development step using Shipley MF322 developer (single puddle process), and a hard bake at 100 °C for 1.5 minute. Always check the temperature of the hotplates first.

Use development program: **1-Dev – SP**.

4. **Photoresist Inspection**

Visually inspect the wafers through a microscope. No resist residues are allowed in exposed parts.

5. **Numbering Wafer**

Write number process run and wafer number with glass pen in the resist, if there is number on the wafer, then skip this step. Write wafer numbers on notebook.

6. **Plasma Etching of Alignment Marks**

Use the Trikon Omega plasma etcher. Follow the operating instructions from the manual when using this machine. **Check the temperature before processing.**
It is not allowed to change the process conditions and times from the etch recipe!

Use sequence **URK_NPD** *(with a platen temperature of 20 °C)* to etch 120 nm deep ASM URK's into the Si.

### Process conditions from chamber recipe URK_ETCH:

<table>
<thead>
<tr>
<th>Step</th>
<th>Gasses &amp; flows</th>
<th>Pressure</th>
<th>Platen RF</th>
<th>ICP RF</th>
<th>Platen temp.</th>
<th>Etch time</th>
</tr>
</thead>
<tbody>
<tr>
<td>1. breakthrough</td>
<td>CF₄/O₂ = 40/20 sccm</td>
<td>5 mTorr</td>
<td>60 W</td>
<td>500 W</td>
<td>20 °C</td>
<td>0'10&quot;</td>
</tr>
<tr>
<td>2. bulk etch</td>
<td>Cl₂/HBr = 80/40 sccm</td>
<td>60 mTorr</td>
<td>20 W</td>
<td>500 W</td>
<td>20 °C</td>
<td>0'40&quot;</td>
</tr>
</tbody>
</table>

7. **Cleaning Procedure : Templa +HNO₃ 100% and 65%**

- **Plasma strip**
  - Use the Tepla plasma system to remove the photoresist in an oxygen plasma.
  - Follow the instructions specified for the Tepla stripper, and use the quartz carrier.
  - Use **program 1**: 1000 watts power and automatic endpoint + 2 minutes overetching.

- **Cleaning**
  - Use wet bench "HNO₃ (100%)" and the carrier with the red dot. 10 minutes in fuming nitric acid (Merck: HNO₃ 100% selectipur) at ambient temperature.

- **QDR**
  - Rinse in the QDR with the standard program until the resistivity is 5 MΩ.

- **Cleaning**
  - Use wet bench "HNO₃ (65%)" and the carrier with the red dot for 10 minutes.

- **QDR**
  - Rinse in the QDR with the standard program until the resistivity is 5 MΩ.

- **Drying**
  - Use the Semitool "rinser/dryer" with the standard program, and the white carrier.

8. **Thermal SiO₂ (2 um)**

- **Equipment : Furnace C1**
  - **Recipe**: Wet thermal silicon oxide 2um (8hrs 16min)
  - Thermal SiO2 on both sides of wafers for further processing.

9. **Measurement of Oxide Thickness**

Use the Leitz MPV-SP measurement system to measure the oxide thickness of a **dummy wafer**.  
Program: Th. SiO₂ on Si, >50 nm auto5pts.

10. **CNT Growth** *(On back side)*

- **Aluminium oxide Sputtering 10nm @ Cleanroom 100**

  Use the TRIKON SIGMA sputter tool for the deposition of the Aluminium oxide layer on the process wafers. Follow the operating instructions from the manual when using this machine. **Check the frequency settings before processing.**

  The target must exist of 100% Al. (Pure Al in Dep C. Ask technician for target change.)

  Use recipe Al₂O₃_10nm_100°C to sputter a 10nm thick layer of Al₂O₃.

  Add dummy wafers in-between as required. Temperature = 100 °C, use target clean recipe for dummy wafer. *(Al_in_between at 100°C, at the same temperature.)*
11. Coating and Baking @ Cleanroom 100

Always check the temperature of the hotplate and the relative humidity (48 ± 2 %) in the room first.

Use the EVG 120 Coater/Developer wafer track to coat the wafers with resist, and follow the instructions specified for this equipment.

Programme: Co_Az Niof2000_1500nm no EBR (otherwise there will be CNT on the edge)

Thickness: 1.5 um

The process consists of a treatment with HMDS (Hexamethyldisilazane) vapor with nitrogen as a carrier gas, spin coating with Co_Az Niof2000_1500nm negative photoresist.

12. Alignment and Exposure @ Cleanroom 100

!!!Align on front side, expose on back side

Processing will be performed on the ASML PAS 5000/50 automatic wafer stepper. Follow the operating instructions from the manual when using this machine.

Use Mask SU EX, exposure energy: 55mJ
Job: Special/ RenePoelma/P3241/incl edge
Reticle name: SU EX

13. Development @ Cleanroom 100

The process consists of x-link bake at 115 degC for 90 seconds with manual contact lanz, followed by a development step using Shipley MF322 developer (single puddle process), and a hard bake at 100 degC for 90 seconds.

Always check the temperature of the hotplates first. Use the EVG 120 Coater/ Developer to develop the wafers, and follow the instructions specified for this equipment.

Use development program Dev_DP2_no EBR puddle.

14. Inspection: Line Width and Overlay @ Cleanroom 100

Visually inspect the wafers through a microscope, and check line width and overlay. No resist residues are allowed.

15. Catalyst and Deposition @ Cleanroom 10000

Use the CHA Solution metal evaporator to deposit 1.5 nm Fe directly on the Al2O3 surface.
Recipe: 1.5nm@0.2 Å/s
Remark: After this step use dedicated contaminated box!

16. Lift-off  (Bottle NMP for Fe lift-off) @ SAL

Perform lift-off procedure with NMP solvent in beaker on hotplate with stirrer at 65 °C and 250 rpm. Time: 4 min in solvent. Temperature: max 70°C
REMARK: Use dedicated beaker for Cu contaminated wafers.

17. Rinse and Dry @ SAL

Rinse the wafer in DI for 4 min and dry using manual dryer with special Cu chuck

18. Inspection

Visually inspect the wafers through a microscope, check if catalyst layer remained on surface. Put paper under wafer and throw away paper after use.

19. CNT Growth @ Cleanroom 10000

Use the AIXTRON BlackMagic Carbon Nanotube Evaporator to grow CNTs using LPCVD at temperatures between 500-750°C for Fe catalyst layers.

Recipe includes an activation step (3 min) in H2 environment at ~600 °C, followed by CNT growth using 700/50 sccm H2/C2H2 at 80 mbar for 5 minutes at 650 °C.

Expected CNT heights: 90-200 um

20. SEM of CNT height @ Clean room 100 Red room

Use clean dummy wafer under processing wafer for inspection.

**Polymer Processing**

21. PDMS Preparation
a. Mix Sylgard 184 Base and Sylgard 184 Curing agent (located in chemical storage cupboard 17 ORG) in a 10:1 ratio by weight in a plastic bottle.
b. Degas in dedicated vacuum chamber next to vacuum oven SALVIS at RT for 10 min.

22. Spinner Preparation @ MEMS Lab

Machine: Manual Coater
a. Cover the manual spinner with aluminium foil all around the spinning area.
b. Place the clean room tissues on top of the aluminium foil that will absorb PDMS.
d. Dispose the tissues in a dustbin with an extraction on top in the MEMS Lab.

23. PDMS Coating @ MEMS Lab

a. Use the Special Cu chuck. Dispense PDMS on wafer (5 ml).
b. Use spin program ‘10’ (500 rpm - 2 s + 1000 rpm – 30 s + 5000 rpm – 2 s)
d. Check the chuck after each wafer and, if necessary, clean it with acetone followed by IPA.
e. Dispose the tissues in a dustbin with an extraction on top in the MEMS Lab.
f. Label the bottle containing left over PDMS and place in chemical storage room at correct waste location.
g. Degas in vacuum oven for 10min at room temperature.

24. PDMS Curing @ MEMS Lab

Bake at 70°C for 15 min in Oven or 10 minutes on hot plate at 90°C.

25. Inspection @ MEMS Lab

Measure the thickness of PDMS with a dummy wafer.

26. PDMS Etching @ SAL Black Bench

Wet etching:
Solution of N-methyl-2-pyrroldinone (NMP) and tetra-butyl ammonium fluoride (TBAF) in a ratio of 3:1, respectively.
Etch rate of 1.5 um/min, isotropic etching.
The etch bath has to be refreshed every 10-15 minutes to ensure a constant etch rate.

27. Cleaning @ SAL Black Bench

Iron Cleaning Use wet bench "HNO₃ (70%): H₂O" with a ratio of 1:7 at 50C, and the carrier with the red dot for 5 minutes at ambient temperature.
Dry
Use manual dryer with Cu chuck

Backside Oxide Cleaning
Use BHF 1:7 Clean the backside silicon oxide for 5min (about 500nm SiO2)
The etch rate of thermally grown oxide is 1.3 ± 0.2 nm/s at 20 °C.
Long rinse time (10min).

Rinse and Dry

Put wafers in clean box.

28. Bake and Degasing @ MEMS Lab

Put wafers in the oven to bake and vacuum. 80 C for 30min.
This step could reduce the degasing in sputter machine.

**Line Deposition**

29. Aluminum Deposition

Use SIGMA sputter tool to have 100nm TiN and 2 um pure aluminum deposition on the wafer at room temperature.

Leak Test before deposition.

30. SEM Inspection

Use SEM to check if all CNTs are covered by Aluminum.

31. Step height inspection

Check the height of steps with dummy wafer. The step height would decide the thickness of photoresist in step 33.

32. Manual Coating

Manually coat the wafers with positive photoresist. Then bake at 80C for 4min.

33. Alignment @ Class 100 Align on front side, expose on back side

Processing will be performed on the EVG 420 contact aligner.
Follow the operating instructions from the manual when using this machine.

Mask Metal1 BOX 457, exposure time 8 sec.
34. Develop @SAL Lab

35. Inspection

Have microscope inspection to check if there is any residuals.

36. Aluminum Etching

Use Omega etching machine to etch

37. Peel Off @ SAL

Peel CNT and polymer composite off from the substrate mechanically.

38. Deposition of Aluminum on the backside

Use contaminated carrier wafer of Fe to have 100nm TiN and 2um Aluminum deposition on the backside of the CNT and polymer composite.