A partition method
for the determination of multiple
DC operating points

van Arturo Sarmiento Reyes
1. In spite of the doubtless remarkable advances that have been made in relation to the techniques of circuit simulation, the current circuit simulation programs still provide little *comprehension of circuits.*

   This thesis, chapter 1.

2. In the process of setting up the equilibrium equations of electronic circuits, the topological information is mixed with all branch-relationships and thus hidden in the system of equations $f(x) = 0$. This leads to a *fuzziness of information*, which becomes particularly important if we consider multistable circuits.

   This thesis, chapter 3

3. In a good circuit simulation program, the solution of the DC problem must address the following issues: the uniqueness of the DC solution, the upper bound on the number of DC solutions and the determination of the DC solutions

4. The reestablishing of diplomatic relations between the Mexican Government and the Vatican represents a step backwards in the history of Mexico and constitutes a danger for the separation church-state and for the existence of other churches.

5. The celibacy of the catholic priests will lead soon or later to the extinction of the species.

6. The idea that moral principles have to be linked to religious fundamentals is a mistake; atheists possess solid moral principles, the obvious difference is that they do not proclaim their religious opinions as an aid to obtain the public approval.
7. A long stay in a foreign country allows one to evaluate more exactly one's own culture. One appreciates its good sides and recognizes its bad sides.

8. The impulse given to the modality of high speed chess by chess authorities and even by the players, was driven by the belief that it will bring the attention of the TV into chess in order to popularize the game. Given the current level of quality of TV programming, it is fortunate that this idea has not been successful.

9. The recent events (1st January 1994) in the southern Mexican state of Chiapas demonstrate that in Mexico still coexist two distinct countries: one in the first world with the NAFTA agreement, with neoliberal reforms in the economical aspects and the best known as touristic attraction; and the second one in the third world, in which the indigenous population is discriminated and exploited.

10. The term illegal worker cannot be conceived without the term illegal employer. The use of only the first one in the discussions concerning the unemployment crisis represents a dangerous fascist temptation and it is a cheap argumentum ad populum.

11. One of the best examples of pluralism in the society was given in Spain during the Caliphate of Cordoba, in which Moslems, Jews and Christians lived in harmony. Not only did The Reconquista mark the starting point of the history of the Spanish Empire but it also represented the beginning of religious intolerance.

12. The so called North-South conflict is generated from the aspiration of the poor countries to accede to a better quality of life. The consideration that this aspiration represents a danger for the rich countries involves a short-minded position and does not constitute a positive contribution to solve the problem.
A partition method for the determination of multiple DC operating points
A partition method for the determination of multiple DC operating points

Een partitie methode ter bepalen van meervoudige DC instelpunten

PROEFSCHRIFT

ter verkrijging van de graad van doctor aan de Technische Universiteit Delft, op gezag van de Rector Magnificus Prof.ir. K.F. Wakker, in het openbaar te verdedigen ten overstaan van een commissie door het College van Dekanen aangewezen, op maandag 2 mei 1994, te 10:30 uur

door:

Librado Arturo SARMIENTO REYES

geboren te Veracruz, México, master of sciences in electronics.
Published and distributed by:
Delft University Press
Stevinweg 1,
2628 CN Delft
The Netherlands
Telephone +31 15 783254
Fax +31 15 781661

CIP-DATA KONINKLIJKE BIBLIOTHEEK, DEN HAAG
Sarmiento Reyes, Librado Arturo
A partition method for the determination of multiple DC
operating points / Arturo Sarmiento Reyes.
Delft: Delft University Press. - I11.
Ph.D. Thesis Technische Universiteit Delft. - With ref. - With
summary in Dutch.

ISBN 90-6275-974-2
Subject headings: DC operating points / network topology
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be reproduced or utilized in any form or by any means, electronic mechanical,
including photocopying, recording or by any information storage and retrieval
system, without permission from the publisher: Delft University Press, Stev-
inweg 1, 2628 CN Delft, The Netherlands.

Printed in The Netherlands
Hagamos un trato

Compañera
usted sabe
que puede contar conmigo
... y cuando digo esto
quiero decir contar
aunque sea hasta dos
aunque sea hasta cinco
no ya para que acuda
presurosa en mi auxilio
sino para saber
a ciencia cierta
que usted sabe que puede
contar conmigo.

Mario Benedetti.

to Guadalupe
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CHAPTER 1

Introduction

1-1 Circuits with multiple DC solutions

Circuits with multiple equilibrium points do occur in electronics, but in most cases, they are caused by the special circumstances in which the circuit works. Those circumstances are related to the values of the circuit parameters, which determine the quantitative values of electrical variables constituting the solution of the circuit, and consequently the qualitative characteristics of the solution. Thus the designer will be confronted with the fact that a normal circuit, assumed to have only one equilibrium point, exhibits more than one. The problem is more serious than it seems to be, since a design can "look" correct, but be worthless, in that it is actually unstable and thus unobservable in practice. Circuits with multiple bias points are called multi-stable circuits.

One common characteristic of many of the classical studies on general nonlinear network analysis, and of the few dedicated to nonlinear networks having multiple equilibrium points, is that they usually start with a mathematical representation of the circuit, a set of equations, and then proceed (either analytically or numerically) to relate in a quantitative manner certain attributes of the system's behavior to the values of the system's variables. As a result of this approach, the ultimate purpose
of those studies was to solve the problem of multi-equilibrium points by attempting to solve the equations resulting from the circuit. Clearly this way of focusing on the problem is of a purely mathematical nature and has as disadvantage that valuable information about the electrical behavior of the circuit is not used to its full extent.

At this point, it is useful to remember what the problem of finding the equilibrium states of nonlinear networks is for the case of multiple bias points: to try to obtain the quantitative values of the electrical variables of the circuit (a solution) and determine how many equilibrium states the circuit can possess.

The current methods employed to achieve the analysis of circuits with multiple bias points are able to solve only the first part of the problem, and, even in most cases, only partially. This is because the mathematical approaches have outlined the problem as the problem of solving the set of nonlinear equations derived from circuit analysis:

\[ f(x) = 0 \]

where \( x \) represents the electrical variables of the circuit.

Because the current approaches are oriented only to solve this set of equations, they do not pay attention to the \textit{circumstances} which cause a circuit with one intended bias point to possess more. This is the reason why the current methods are not able to solve the second part of the problem (the number of solutions).

Moreover, the set of nonlinear equations related to a multi-equilibrium circuit is usually ill-conditioned, causing that the commonly used methods to solve systems of nonlinear equations fail. The currently used methods try to overcome this obstacle by using alternative approaches; but in all cases, the aim stays the same: finding the solution of \( f(x) = 0 \).

Later in this chapter, we will come back to the present methods. First, a brief overview on circuit simulation is presented in order to situate the analysis of nonlinear networks in a simulation environment.

1-2 A glance at circuit simulation

The complexity of current electronic circuits has reached such remarkable heights that analyzing and testing them by \textit{old-fashioned} methods is out
of question. Historically, the analysis of electronic circuits has been done in different ways and from different points of view, but whatever the case, the aim has been the same: to obtain the quantitative values of the electrical variables of the circuit. Formerly, electronic circuits were constituted of discrete components, with the result that the final analysis — or in other word: testing — was done on the breadboarded circuit in which internal nodes were accessible for the measurement of the electrical variables, and, if the circuit did not satisfy the design specifications, it could be modified.

However, in spite of the advances in the field of electronic instrumentation, these methods cannot be applied to integrated circuits. Internal nodes are inaccessible and if a chip shows a fault, there is essentially no way to repair it. In addition to this intrinsic difference, there are others. For example, in the problem of tolerance analysis (worst-case analysis), the breadboarding approach fails because it becomes almost impossible to vary the parameters in the required amounts. This example reveals another disadvantage of the breadboarding approach: the designer is not allowed to make changes in the circuit in order to examine in detail properties of the circuit depending on those changes; i. e. there is no flexibility in the process of analysis.

In the middle of the 60s, and because of the impact of the computers, the modus operandi of the circuit designers began to change. Several works from that time permit us to see how dramatic this change [1–3]. Designers started to look for analytical tools which could be implemented on digital computers with the main aim of improving circuit analysis. With the aid of computer programs, the circuit designer was able not only to analyze the circuit but also to carry out "numerical experiments", often faster and cheaper than was possible with the breadboarded version. Such a computer program is called a circuit simulator. This represented the start of a new discipline in electronics: Computer Aided Design, of which simulation is an important part. Nowadays, CAD plays an important role in designing electronic circuits.

In this section a brief glimpse of the general structure of a computer simulation program is given [4–6], with a remark on the DC analysis stage.
1-2-1 General structure of a simulator

Most circuit analysis problems can be solved in two steps. The first one consists of formulating the circuit equations in a suitable form by using the two Kirchhoff laws and the relationships of the elements involving their own electrical variables. The second step consists of solving these equations by appropriate analytical or numerical methods.

Unfortunately, analytical approaches to the second step impose severe limitations on the type of circuits that can be analyzed. Before the appearance of Computer Aided Design & Simulation, some analytical methods were used, but they were applied under simplified assumptions for the functions involving the electrical variables of the elements. Furthermore, this fact also imposed limitations to the size of the circuit that could be analyzed. With the advent of CAD, numerical methods are used to solve the equations resulting from the first step.

Figure 1.1: Schematic description of a circuit simulation program.

Thus, a circuit simulation program must analyze a circuit by (i) translating the circuit given by the user into a suitable mathematical representation, (ii) choosing and developing the analysis to be performed and (iii) giving the resulting output data.

This description is the basic structure of a simulation program as shown in fig. 1.1.
1-2. A GLANCE AT CIRCUIT SIMULATION

- The input stage performs the *translation* of the circuit to be analyzed in order to set up the basic data structures needed to achieve the analysis in the second stage. This first stage requires a considerable knowledge of computer programming techniques in order to obtain an input stage that is not only able to process the input data given by the designer, but also to provide flexibility and several *user-oriented* features that make the program easy to use. Some people tend to regard most of these features as means of saving code size at this stage, but the price that users must pay is a loss of flexibility to handle the input data. Some desirable features of this stage are: friendly input format and error detection facilities.

- The analysis stage is the most important one, because it is the core of any simulator. In this stage, the analyses required by the designer are performed by setting up the equations that model the performance of the circuit, and by applying some suitable numerical methods to solve the equations.

The various types of analysis that a simulator can perform are:

- DC analysis
- Linear AC analysis
- Nonlinear AC analysis
- Linear time-domain analysis
- Nonlinear time-domain analysis

This stage indeed solves the problem of circuit analysis, which implies that reliable solutions to an arbitrary network problem can be expected if the numerical methods used are also reliable. However, there is an exception when the problem involves *pathological* numerical difficulties.

This exception occurs either if the resulting equations modeling the performance of the circuit present *pathological* conditions, or if the numerical method used to carry out the analysis *runs* in such a way that the solution becomes meaningless.
• The output stage is the last but not the least important in a circuit simulation program, it performs the meaningful representation of the output data, or a first approach to any post-processing that can be done by other appropriate tools of the CAD environment. In this last context, the modern design of simulation tools is intended to provide simulators that can be placed as modules inside a more sophisticated CAD environment.

1-2-2 DC analysis

This thesis has to do with an analysis stage able to perform the DC analysis. This analysis determines the equilibrium points (DC points) of the circuit. By equilibrium points is meant that no dependence on $t$ occurs, so that those elements with relationships involving time-derivatives of their electrical variables ($\frac{\partial}{\partial t}$) must be considered zero, i.e. it is assumed that capacitors and inductors play no role in the DC performance of the circuit. One can see the DC analysis as the task of finding the solutions for a resistive network model which is obtained by shorting all inductors and opening all capacitors in the original network.

As result of the previous condition, the equation to be solved by any DC analysis stage has the following form:

$$ f(x) = 0 $$  \hspace{1cm} (1.1)

The equation formulation is obtained by applying some suitable network analysis method to the given circuit. Here $x$ represents those electrical variables of the circuit considered to be unknowns. Once the formulation is done, the next step is to obtain the solution of equation (1.1) which represents the equilibrium values for those electrical variables and is usually denoted as $x^*$. In practice, most circuits present nonlinear relationships between their electrical variables and this is the reason why the equation above has also a nonlinear nature. Thus a method for solving nonlinear equations must be applied as a numerical tool in order to find the solution of the circuit. In this case, one refers to equation (1.1) as a system of nonlinear equations. There is an important difference between nonlinear circuits and linear circuits, it is the number of solutions that the system
may have. Thus, nonlinear networks differ from linear networks in that
they may have no solution, an infinite number of solutions, a unique
solution or several solutions.

1-3 Multiple solutions in DC analysis

As pointed out in the preceding sections, the DC analysis of nonlinear
networks must find the operating point of the circuit by solving the non-
linear algebraic equation in (1.1). Several techniques have been developed
for solving this kind of equation, but relatively little has been done in
locating multiple solutions.

Currently circuit simulators are able to find only one DC operating
point — which has a location that depends on the given starting values
of $x$ —, but none is able to determine if the circuit has multiple solutions,
and if so, how many. It was mentioned previously that the reliability of
the answer to the problem of circuit analysis was commensurate with that
of the numerical method used to solve the equations of the circuit. In
the case of circuits with multiple bias points being analyzed by common
circuit simulators, it involves pathological numerical difficulties coming
from the inability of the numerical methods used to solve 1.1 for the
several solutions. Most of the circuit simulators use Newton-Raphson or
its variants as the numerical algorithm to find the solution, however, this
method is not suitable for analyzing circuits with multiple solutions. We
will return to this point in the following chapters.

1-3-1 Current methods to find multiple solutions

The most often used method to solve the nonlinear set of equations (1.1)
is the Newton-Raphson algorithm, which can be expressed as:

$$x^{(j+1)} = x^{(j)} - \left[J(x^{(j)})\right]^{-1} f(x^{(j)}) \quad (1.2)$$

where

$$\left[J(x^{(j)})\right]^{-1} = \left[\frac{df(x)}{dx} \right]_{x=x^{(j)}}^{-1} \quad (1.3)$$
CHAPTER 1. INTRODUCTION

This method converges to a solution, provided that the initial values of \( \mathbf{x} \) (\( \mathbf{x}_0 \)) are close enough to the solution \( \mathbf{x}^* \). However, the Newton-Raphson method fails when one tries to find more than one solution.

Alternative methods have been reported. All of them try to overcome the ill condition of (1.3) caused when \( \mathbf{J} \) becomes singular. This condition occurs when \( \det \mathbf{J} = 0 \).

The methods consist of numerically integrating some associated system of ordinary nonlinear differential equations related through a path of solutions. These kinds of methods are called Homotopy Methods. They allow the solving of \( \mathbf{f}(\mathbf{x}) = \mathbf{o} \) by adding an extra parameter and forming thus a modified system of equations.

A form to obtain an augmented version of (1.1) is by using the following system:

\[
\hat{\mathbf{f}}(\mathbf{x}, \mu) = \mathbf{o}
\]  

(1.4)

where \( \mathbf{x}_0 \) is any initial guess.

The equation above has the following properties:

1. At some initial value \( \mu = \mu_o \), a solution \( \mathbf{x}_o \) of equation (1.4) is known, \textit{a priori}:

\[
\hat{\mathbf{f}}(\mathbf{x}_o, \mu_o) = \mathbf{o}
\]  

(1.5)

2. At some value \( \mu^* \neq \mu_o \), equation (1.4) reduces identically to equation (1.1); namely,

\[
\hat{\mathbf{f}}(\mathbf{x}, \mu^*) = \mathbf{f}(\mathbf{x}) = \mathbf{o}
\]  

(1.6)

which has an obvious solution corresponding to the solution of the original system \( \mathbf{f}(\mathbf{x}) = \mathbf{o} \).

These methods have a purely mathematical application, among them the works in [7–11] can be mentioned. Applications of these methods to solve circuit equations are found for instance in [12–16].

Although these methods avoid the ill condition of the determinant, they have the following general disadvantages:

- In practice, they cannot be considered \textit{self-starting}. They need a starting algorithm in order to find a useful initial value \( \mathbf{x}_0 \).
• They determine a particular path, depending on the value of $x_0$.

• They cannot guarantee that all solutions are found, because they cannot determine if all the solutions lie on the same path.

• Because they are based on the application of an integration method along a path of solutions, it can occur that either the path returns to a solution already found, or the path stays searching for another solution. In the first case the solutions lie on closed paths, so that the algorithm stays running along the path. In the second case the solutions lie in open paths, so that the algorithm stays moving away. In a word, they lack reliable stop criteria.

However, a common characteristic of these methods is that they solve the problem of multiple-stable circuits by just solving $f(x) = 0$. In the following chapters, we present a more detailed discussion of the most commonly used methods of this type.

1-3-2 Nature of the solutions

The resistive model of a multi-stable circuit has more than one solution, depending on the characteristics of $f(x) = 0$. These solutions are divided into stable and nonstable solutions or equilibrium points. The stability of the equilibrium states is, of course, dependent on the energy storage components of the network, which means that the concept of stability is related to the time domain performance of the network.

Unstable solutions are undesirable for two reasons: the operating point is unobservable in terms of physical conditions, and even if the numerical solution "looks" correct, it represents values of the electrical variables of the network which are not in accordance with what was expected from the circuit. Until now, the designer has resorted to his/her experience to decide whether the solution represents a stable equilibrium state.

In addition to the stable equilibrium states, a multistable circuit can possess unstable equilibrium states.

The problem of nonlinear multivalued circuits must completely be described as:
1. Finding reliably the set of solutions.

2. Determining the stability of each solution and

3. Determining how many solutions the circuit under analysis has.

Applications of the concept of multiple solutions of nonlinear equations play an important role in the area of nonlinear circuit analysis, being relevant not only in order to determine the DC operating points, but also for other related tasks like input-output characteristics and sensitivity analysis of the equilibrium points.

Figure 1.2 shows an elementary example of such a circuit. Here a circuit with more than one bias point is sketched. It is well known that the operating points marked as A and B are stable, and the middle point C is unstable.

1.4 Scope of this work

A large number of circuits appears in electronics, which makes necessary that a classification must be made if we wish to focus on the DC problem in a proper way. Classification helps to define the problem by the use of a suitable description and the determination of the conditions under which the solution of the problem remains valid.

This classification is shown in figure 1.3. Firstly, the circuits\(^1\) can be divided in two classes:

- Linear circuits
- Nonlinear circuits

\(^1\)Because only the DC problem is involved, the circuits to be classified are purely resistive circuits, i.e. circuits containing elements associating the electrical variables \(i\) and \(v\).
In the first class, circuits containing positive linear resistors and any kind of voltage or current sources are considered. In the literature there are several works [17, 18] related to this class of linear circuits, mainly directed to determining the existence and uniqueness of the DC solution. They conclude that the DC solution for this kind of circuit exists, and that only one\textsuperscript{2} exists.

The second class involves circuits containing any type of voltage or current sources and resistors that may be expressed by nonlinear i-v relationships. This type of circuit may be further divided into two groups by taking into account the type of nonlinear functions associated with the elements. In this class there are two subgroups: circuits containing \textit{strictly monotone increasing nonlinearities} and circuits containing \textit{nonmonotone

\textsuperscript{2}This is true for the case that the circuit is not \textit{ill} posed, i.e. there is no loop (resp. no cut set) formed exclusively by independent voltage sources (resp. current sources).
**CHAPTER 1. INTRODUCTION**

*increasing nonlinearities.* In the first subgroup, circuits containing elements described by strictly monotone increasing \( i-v \) relationships and any kind of source are considered. The second subgroup involves circuits containing nonlinear elements described by tunnel diode-like \( i-v \) relationships.

A further subdivision can be applied to the first subgroup, depending on the presence of controlled sources. The most interesting group part encompasses circuits containing elements with strictly monotone increasing nonlinearities and controlled sources. Circuits with BJT s and IGFETs fall into this category, which represents actually a very large class of electronic circuits.

The present thesis is focussed on solving the DC problem of circuits with bipolar transistors, as shown in figure 1.3. This class includes circuits which have a very large area of application in electronics.

### 1.5 Conclusions

In spite of the doubtless remarkable advances that have been made in relation to the techniques of circuit simulation, the current circuit simulation programs still provide very little *comprehension of circuits*.

This hindrance becomes more obvious in the case of the analysis of nonlinear circuits with more than one bias point. The analysis has to date been done by using a completely mathematical approach; i.e. trying to solve the set of nonlinear equations \( f(x) = 0 \).

Besides the problems appearing in the process of solution, because that equation can become highly ill-conditioned, the designer loses contact with the electrical behavior of the network. It is necessary to develop a new method in order to solve properly the problem of multi-stable circuits. This new method must use the information on the electrical behavior of the circuit to its full extent. The method has to be founded on an approach that is much more oriented towards electrical behavior.

In addition to the above, the electrical approach pays attention to the conditions —behavior of the electrical variables— that cause a circuit to possess multiple solutions.
Bibliography


CHAPTER 2

Circuit Analysis Methods

2-1 Introduction

In order to analyze a network, its components and structure must be provided to the computer. Then one must set up the network equations in such a form that they are well-suited for a computer-aided analysis. A wide variety of formulation methods to perform this task already exist and they constitutes the subject of this chapter, in which we trace the outline of several of the most often used. However, it is not our aim to develop here a complete description of all the existing methods. Many treatises [1–4] on this subject are available, and most of them emphasize the usefulness of a particular method. This chapter is intended to handle the most basic definitions used in those methods.

For the purpose of restricting the analysis, the network under consideration is assumed to be a lumped electrical network. A lumped network can be described in terms of the branch characteristics and the manner in which those branches are interconnected. This process can be done inside any circuit simulator program by converting the information concerning the circuit into a suitable set of numerical equations. The information on the circuit is been given by the user through an ad hoc interface. The
resulting set of equations must be tailored such that it permits efficient manipulation in order to obtain the solution to the network problem by applying an appropriate numerical algorithm.

![Diagram of electrical network](image)

**Figure 2.1:** Schematic description of electrical network.

Because matrix notation is considered to be the tool *par excellence* for describing the electrical network problem in a form suitable for programming, all methods of circuit analysis result in a matrix representation of the circuit.

From a physical point of view, the network simulation problem is related to predicting the behavior of a set of interconnected elements in terms of the element characteristics and the manner in which the interconnected elements appear to constitute the network. With this idea as a basis, an electrical network $\mathcal{N}$ can be depicted as a set $\mathcal{C}$ of elements called *components* and the interconnection pattern $\mathcal{P}$.

Fig. 2.1 serves to show this definition. Here, each *component* is defined by an oval with its corresponding name $C_i$. Each $C_i$ is defined by a mathematical relationship between electrical variables. This relationship is given by the following basic expression:

$$v_{\text{dep}_i} = F_i(v_{\text{ind}_i}, v_{\text{ind}_j}, \cdots) \quad (2.1)$$
2-1. INTRODUCTION

where \( v_{\text{dep}_i} \) represents the dependent electrical variable of the \( i \)-th component, \( F_i \) constitutes its relationship with a set of independent electrical variables \( v_{\text{ind}_i} \).

These variables are related to the nature of the components and they represent physical quantities: voltages, currents, charges and fluxes.

For DC analysis, voltages and currents are the most important variables. Charges (resp. fluxes) may be part of the equations, but they must be given as functions of voltages (resp. currents). Because DC analysis assumes that time dependence is not considered, dynamic elements (those containing \( \partial / \partial t \) in their relationships) are not taken into account for analysis. This is the reason why inductors (resp. capacitors) are considered short circuits (resp. open circuits) when \( v_L = L \frac{\partial i_L}{\partial t} = 0 \) (resp. \( i_C = C \frac{\partial v_C}{\partial t} = 0 \)).

In the formula above, it can be noted that \( F_i \) represents a function of several electrical independent variables. The branch relationship given in equation (2.1) may take the form of a:

- relationship between electrical variables of the same element. In this case, the electrical variable \( v_{\text{dep}_i} \) is dependent on the variable \( v_{\text{ind}_i} \), of the same component. \( F_i \) can thus be expressed by the mapping between both electrical variables and can be plotted by means of a \( v_{\text{dep}_i} - v_{\text{ind}_i} \) curve.

- relationship between electrical variables of different elements. Here, the electrical variable \( v_{\text{dep}_i} \) is dependent on the electrical variable of another component. In this case we refer to a component used to provide the coupling between two electrical variables of the circuit. This circumstance allows the representation of components with more than two terminals, by modeling them as a set of two-terminal elements, some of which describe coupled relationships.
Both cases are described schematically in fig. 2.2 (a) and (b) respectively.

If the manner in which the components are interconnected is temporarily not considered, and only the components per se are taken into account, then apart from $C$, a set containing all functions $F_i$ is also present. This set of functions will be denoted as $\mathcal{F}$. The set of components $C$ is sketched in fig. 2.3.

![Diagram of network](image)

For each element $C_i$

$$v_{dep} = F_i(v_{ind_1}, v_{ind_2}, \cdots)$$

Figure 2.3: Set $C$ of components of the network $\mathcal{N}$.

However, if we represent the network $\mathcal{N}$ with each component substituted by a line, we obtain the interconnection pattern $\mathcal{P}$ of the network. This pattern is constituted only by lines (branches) and union points (nodes). Fig. 2.4 shows the corresponding interconnection pattern of the network $\mathcal{N}$, where $b_i$ represents the branches and $n_k$ denotes the nodes. In this context, each line or branch represents a component and each node represents the connection point between at least two components. In addition, we define the number of nodes as $n$ and the number of branches as $b$. 
In summary, the topological structure of the network $\mathcal{N}$ can be described by the interconnection pattern $\mathcal{P}$. The act of interconnecting the components introduces certain constraints, which can be interpreted as constraints on the electrical variables of the circuit. Or, put in another way: if the same components were interconnected by using another pattern, the constraints will change and also the values of the electrical variables. These constraints are related to the laws governing the energy distribution in the interconnected network. Since we are considering lumped networks, they must obey two constraints stated as the Kirchhoff voltage law (KVL) and the Kirchhoff current law (KCL), in addition to the element's characteristics (branch relationships).

2-2 The ABCDs of network topology

From a mathematical point of view, the network problem is essentially concerned with the solution of the circuit as finding a set of values of the electrical variables, such that it fulfills both the topological constraints and the set of relationships $\mathcal{F}$.

The process of solution can be greatly systematized by keeping in mind that the interconnection pattern gives information about how the
electrical variables are correlated. This can be achieved by using topological methods.

In fig. 2.4, the interconnection pattern $P$ of the network $N$ is shown. If we assign directions to each branch, then a directed graph $G$ can be obtained, as depicted in fig. 2.5. This graph is used in this section to determine the most important matrices related to circuit topology.

2-2-1 Node-branch incidence matrix

The first important matrix derived from the graph of the network is the node-branch incidence matrix ($A_a$). In order to form the matrix, the nodes of the graph must be associated to the rows and the branches to the columns. The node-branch incidence is denoted by a $+1$ if the edge goes away from the node, $-1$ if the edge goes into the node, and 0 if the branch does not touch the node at all. Thus each column contains a pair $(+1, -1)$ in the rows corresponding to the nodes where the branch is situated.
For the directed graph shown in fig. 2.5, the corresponding \( A_a \) is expressed as:

\[
A_a = \begin{bmatrix}
  n_1 & b_1 & b_2 & b_3 & b_4 & b_5 & b_6 & b_7 & b_8 \\
  n_2 & +1 & +1 & +1 & 0 & 0 & 0 & 0 & 0 \\
  n_2 & -1 & 0 & 0 & +1 & 0 & 0 & 0 & 0 \\
  n_3 & 0 & -1 & 0 & 0 & +1 & +1 & +1 & 0 \\
  n_4 & 0 & 0 & -1 & 0 & 0 & -1 & -1 & +1 \\
  n_0 & 0 & 0 & 0 & -1 & -1 & 0 & 0 & -1
\end{bmatrix}
\]

Now, if a node (in our case \( n_0 \)) is assumed to represent the reference node, \( A_a \) can be reduced by one row, yielding the following matrix, denoted as the \( A \) matrix and known as the reduced node-branch incidence matrix:

\[
A = \begin{bmatrix}
  n_1 & b_1 & b_2 & b_3 & b_4 & b_5 & b_6 & b_7 & b_8 \\
  n_1 & +1 & +1 & +1 & 0 & 0 & 0 & 0 & 0 \\
  n_2 & -1 & 0 & 0 & +1 & 0 & 0 & 0 & 0 \\
  n_3 & 0 & -1 & 0 & 0 & +1 & +1 & +1 & 0 \\
  n_4 & 0 & 0 & -1 & 0 & 0 & -1 & -1 & +1
\end{bmatrix}
\] (2.2)

This matrix can be used to relate the electrical variables of the circuit, yielding:

\[ A i_b = 0 \] (2.3)

and

\[ A^t v_n = v_b \] (2.4)

where \( i_b, v_b \) and \( v_n \) denote the vectors of branch currents, branch voltages and node voltages. Equation (2.3) represents Kirchhoff's Current Law and equation (2.4) Kirchhoff's Voltage Law.

### 2-2-2 Node-to-reference-node matrix

Another important matrix is called the node-to-reference-node matrix, which describes the path (set of branches) connecting a particular node to
the reference node. This matrix is the $B$ matrix and can be constructed in a systematic way with the aid of a tree. A tree is a subgraph $G_s$ from an original graph $G$ which contains all nodes of $G$; in addition $G_s$ has no loops. Thus a tree consists of a set of branches connecting all nodes of $G$ without forming a loop. In fig. 2.6 our graph is shown with a selected tree $T = \{b_1, b_2, b_5, b_7\}$ — represented by full lines — and the cotree $T_c = \{b_3, b_4, b_6, b_8\}$ — represented by dashed lines.

Figure 2.6: Directed graph with tree and cotree.

$B$ associates each node (represented as the columns) with the branches of the tree (represented as rows) conducing it to the reference node. The corresponding $B$ matrix is given by:

\[
\begin{bmatrix}
  b_1 & b_2 & b_3 & b_4 \\
  0 & -1 & 0 & 0 \\
  +1 & +1 & 0 & 0 \\
  +1 & +1 & +1 & +1 \\
  0 & 0 & 0 & -1 \\
\end{bmatrix}
= B \quad (2.5)
\]
So that an element $b_{ij}$ can be expressed as:

$$b_{ij} = \begin{cases} 
+1 & \text{if branch } j \text{ is included in the path from node } i \\
-1 & \text{if branch } j \text{ is included in the path from node } i \\
0 & \text{if branch } j \text{ is not included in the path from node } i 
\end{cases}$$

- to the reference node and \textit{goes to} to the reference node
- the reference node and \textit{goes away from}

However, the definition of $T$ permits us to express $A$ as a partitioned matrix:

$$A = [A_T | A_L] \quad (2.6)$$

where $A_T$ and $A_L$ are the sections corresponding to the tree branches and to the cotree branches. It can be demonstrated [3] that:

$$A_T^{-1} = B^t \quad (2.7)$$

### 2-2-3 Branch-loop incidence matrix

In order to express KVL equations from the directed graph of the circuit, a new matrix can be constructed with information about the incidence between branches and loops. This matrix is denoted as the $C_a$ matrix and to construct it, the branches are associated to its columns and the loops to the rows, so that an element $c_{ij}$ can be expressed as:

$$c_{ij} = \begin{cases} 
+1 & \text{if branch } j \text{ is in loop } i \text{ and their directions agree} \\
-1 & \text{if branch } j \text{ is in loop } i \text{ and their directions oppose} \\
0 & \text{if branch } j \text{ is not in loop } i 
\end{cases}$$

Fig. 2.7 shows our directed graph with a set of oriented loops numbered as \{l_1-l_6\}. 
According to the rule above, the $C_a$ matrix can be expressed as:

$$
\begin{bmatrix}
    b_1 & b_2 & b_3 & b_4 & b_5 & b_6 & b_7 & b_8 \\
    l_1 & | & -1 & 0 & +1 & -1 & 0 & 0 & +1 \\
    l_2 & | & -1 & +1 & 0 & -1 & +1 & 0 & 0 \\
    l_3 & | & 0 & 0 & 0 & 0 & -1 & 0 & +1 & +1 \\
    l_4 & | & -1 & +1 & 0 & -1 & 0 & 0 & +1 & +1 \\
    l_5 & | & 0 & 0 & 0 & -1 & +1 & 0 & 0 \\
    l_6 & | & 0 & -1 & +1 & 0 & 0 & -1 & 0 & 0
\end{bmatrix}
$$

Matrix $C_a$ is useful, because it permits us to express the KVL as:

$$C_a v_b = 0 \quad (2.8)$$

This equation represents a set of $l$ equations; where $l$ is the number of loops considered in the graph. However, if all existing loops are taken into account, the set of (2.8) contains redundant equations. In network analysis, a maximum set of independent equations is sufficient. This maximum is equal to $b - n + 1$, where $b$ is the number of branches and $n$ represents the number of nodes.

The $C_a$ matrix formed in this case is denoted as the basic $C_a$ matrix and is usually expressed as $C$ matrix. In order to form this new matrix, we apply the concept of tree previously introduced. The tree previously selected is used here as an example.

Each branch of the cotree (a link) forms a loop with some of the branches of the tree; the resulting loop is called a basic loop. In plain words: a basic loop is formed by one element of the cotree and one or more elements
2-2. THE ABCDS OF NETWORK TOPOLOGY

Figure 2.8: Directed graph with basic loops for a selected tree.

of the tree. The orientation of the loop is arbitrarily chosen to coincide with that of the link. The clear result is that \( b - n + 1 \) basic loops exist. For our graph, the several basic loops and the selected tree are shown in fig. 2.8. By properly ordering the branches — taking first those of the tree — the \( C \) matrix can be expressed as:

\[
\begin{bmatrix}
  b_1 & b_2 & b_3 & b_4 & b_5 & b_6 & b_7 & b_8 \\
  l_1 & l_2 & l_3 & l_4 & l_5 & l_6 & l_7 & l_8
\end{bmatrix}
\]

\[
= C \quad (2.9)
\]

Thus \( C \) can be partitioned as:

\[
C = [C_T | C_L] = [C_T | I] \quad (2.10)
\]

where \( C_T \) and \( C_L \) represent the sections corresponding to the tree branches and to the cotree branches.
Circuit Analysis Methods

C is useful because it permits us to express the KVL as:

\[ Cv_b = 0 \]  \hspace{1cm} (2.11)

and the branch currents as a linear combination of the basic loop currents as:

\[ C^t \mathbf{i}_l = \mathbf{i}_b \]  \hspace{1cm} (2.12)

which represents another form of the KCL.

![Directed graph with basic cutset](image)

Figure 2.9: Directed graph with basic cutset.

2-2-4 Branch-to-cutset incidence matrix

The final topological matrix is the cutset matrix \( \mathbf{D} \). Just as each link together with certain branches of the tree defines a basic loop, each tree branch with certain branches of the cotree (links) defines a basic cutset. This is shown in fig. 2.9 for our graph. The direction of the cutset is arbitrarily chosen to coincide with that of the tree branch. In order to form \( \mathbf{D} \), the cutsets are associated with the rows, and the branches with
the columns. This matrix is given by:

\[
\begin{bmatrix}
  b_1 & b_2 & b_5 & b_7 & b_3 & b_4 & b_6 & b_8 \\
  c_1 & 0 & 0 & 0 & 0 & -1 & 0 & 0 \\
  c_2 & 0 & +1 & 0 & 0 & +1 & +1 & 0 & 0 \\
  c_3 & 0 & 0 & +1 & 0 & 0 & +1 & 0 & +1 \\
  c_4 & 0 & 0 & 0 & +1 & +1 & 0 & +1 & -1 \\
\end{bmatrix}
\]

\[= D \quad (2.13)\]

By properly ordering the branches — taking first those of the tree — and because each basic cutset contains one and only one tree branch, \( D \) can be partitioned as:

\[D = [D_T | D_L] = [I | D_L] \quad (2.14)\]

where \( D_T \) and \( D_L \) are the sections corresponding to the tree branches and to the cotree branches.

The KCL can be expressed as:

\[D_i = 0 \quad (2.15)\]

and the KVL expresses the branch voltages as a linear relationship of the tree branch voltages:

\[D^t v_t = v_b \quad (2.16)\]

### 2-3 A glimpse of network analysis methods

As shown in the previous sections, network topology yields several matrices containing the information about the interconnection pattern of the circuit. Those matrices constitute the basis on which various circuit analysis methods are developed. In this section, a brief description of the most important methods of analysis is given.

#### 2-3-1 Loop analysis

This method is rarely used in circuit simulation programs, because its implementation on a digital computer is not easy to carry out. The reasons are more of historical nature, in fact, the only step that makes the
loop analysis less suitable in comparison with the nodal analysis is the selection of a tree. The primary independent variables are represented by the loop currents. This method makes use of the $C$ matrix which expresses the KVL as in equation (2.11). The branch voltages are given as:

$$v_b = Ri_b + e$$

where $R \in \mathbb{R}^{b \times b}$ represents linear or linearized voltage-current relations, $i_b \in \mathbb{R}^b$ represents branch currents and $e \in \mathbb{R}^b$ represents independent voltage sources. Substituting this equation in 2.11, yields:

$$C(Ri_b + e) = 0$$

Finally, by substituting 2.12 in the previous equation:

$$CRC'^t i_l = -Ce$$

(2.17)

This equation represents a system of $l$ equations, where $l$ is the number of basic loops and $i_l$ is the the vector of loop currents.

- Modified Loop Analysis\(^1\) (MLA) [6].

The loop analysis has as its main disadvantage that it cannot admit zero valued conductances, which occurs when current sources are involved — because ideal current sources by definition have associated infinite internal impedance connected in parallel. In order to overcome this problem, an augmented system is used instead of that of equation 2.17. The $C$ matrix is partitioned as:

$$C = [\hat{C}|C_j]$$

where $C_j$ is the portion of $C$ corresponding to those branches that are constituted by current sources and $\hat{C}$ is the part containing linear (or linearized) resistors and voltage sources.

\(^1\)For planar networks, the loop analysis method has received the name of mesh analysis method. The term Modified Mesh Analysis was introduced by Kleihorst in [5] as a dual denomination with respect to the well-known Modified Nodal Analysis.
The augmented system is formed by adding to the primary variables (the loop currents $i_i$) the voltages of the current sources ($v_j$). Thus we can obtain:

$$
\begin{bmatrix}
\hat{C} R \hat{C}^t & C_j \\
-C_j^t & 0
\end{bmatrix}
\begin{bmatrix}
i_i \\
v_j
\end{bmatrix}
= 
\begin{bmatrix}
-\hat{C} e \\
-j
\end{bmatrix}
$$

(2.18)

This equation represents a system of $l + j$ equations, where $l$ is the number of basic loops and $j$ the number of current sources. The representation above is not complete, since not all non-LA-compatible elements have been included.

2-3-2 Nodal analysis

This method is the most commonly used in circuit simulation programs because of the simple manner used to stamp the elements in the matrix. The primary independent variables are represented by the nodal voltages. This method makes use of the $A$ matrix which expresses the KCL as in equation (2.3), which is here repeated:

$$
Ai_b = 0
$$

The branch currents are given as:

$$
i_b = Gv_b + j
$$

where $G \in \mathbb{R}^{b \times b}$ represents linear or linearized current-voltage relations, $v_b \in \mathbb{R}^b$ represents branch voltages and $j \in \mathbb{R}^b$ represents independent current sources. Substituting this equation in 2.3, yields:

$$
A(Gv_b + j) = 0
$$

Finally, by substituting 2.4 in the previous equation:

$$
AGA^t v_n = -Aj
$$

(2.19)

This equation represents a system of $n$ equations, where $n$ is the number of nodes excluding the reference node and $v_n$ is the vector of nodal voltages.
• Modified Nodal Analysis (MNA) \([6,7]\).

The main disadvantage of nodal analysis is that it cannot admit zero valued resistors, which occurs when voltage sources are used — because ideal voltage sources have associated a zero valued internal impedance connected in series. This problem has been solved by using an augmented system instead of that of equation 2.19. The \(A\) matrix is partitioned as:

\[
A = [\hat{A} | A_e]
\]

where \(A_e\) is the portion of \(A\) corresponding to the branches containing voltage sources and \(\hat{A}\) is the part of linear (or linearized) conductances and current sources.

The augmented system is formed by adding to the primary variables (the nodal voltages \(v_n\)) the currents of the voltage sources \((i_e)\). Thus we can obtain:

\[
\begin{bmatrix}
\hat{A}G\hat{A}^t & A_e \\
-A_e^t & 0
\end{bmatrix}
\begin{bmatrix}
v_n \\
i_e
\end{bmatrix}
= \begin{bmatrix}
-\hat{A}j \\
-e
\end{bmatrix}
\quad (2.20)
\]

This equation represents a system of \(n + e\) equations, where \(n\) is the number of nodes without datum and \(e\) the number of voltage sources. The representation above is not complete, since not all non-NA-compatible elements can be included.

### 2-3-3 Cutset analysis

The last fundamental method is based on the cutset matrix \(D\), which expresses the KCL as in equation (2.15). The branch currents are given — as in the previous method — as:

\[
i_b = Gv_b + j
\]

Substituting this equation in 2.15, yields:

\[
D(Gv_b + j) = 0
\]

Finally, by substituting 2.16 in the previous equation:

\[
DGD^tv_t = -Dj
\quad (2.21)
\]
This equation represents a system of \( t \) equations, where \( t \) is the number of tree branches and \( \mathbf{v}_t \) is the vector of tree voltages.

- Modified Cutset Analysis (MCA).

The cutset analysis has the same disadvantage as the nodal analysis method. This problem can be solved in the same manner. The \( \mathbf{D} \) matrix is partitioned as:

\[
\mathbf{D} = [\hat{\mathbf{D}} \mid \mathbf{D}_e]
\]

where \( \mathbf{D}_e \) is the portion of \( \mathbf{D} \) corresponding to the branches connected to voltage sources and \( \hat{\mathbf{D}} \) is the part of linear (or linearized) conductances and current sources.

The augmented system is formed by adding to the primary variables (the tree branch voltages \( \mathbf{v}_t \)) the currents of the voltage sources \( \mathbf{i}_e \). In this way, it can be obtained:

\[
\begin{bmatrix}
\hat{\mathbf{D}} \mathbf{G} \hat{\mathbf{D}}^t & \mathbf{D}_e \\
\mathbf{-D}_e^t & \mathbf{0}
\end{bmatrix}
\begin{bmatrix}
\mathbf{v}_t \\
\mathbf{i}_e
\end{bmatrix}
= 
\begin{bmatrix}
\mathbf{-Dj} \\
\mathbf{-e}
\end{bmatrix}
\]

(2.22)

This equation represents a system of \( t + e \) equations, where \( t \) is the number of tree branches and \( e \) the number of voltage sources.

For each one of the methods previously presented, there exist a generalization recast in the so-called Tableau Method [2, 3, 8, 9]. The Tableau Method has the property that no special restrictions are imposed to the type of circuit elements and therefore all kind of non-linear relations of the elements are permitted. This results in a more extended set of primary variables and a more sparsed matrix, which constitutes an advantage during the process of solution.

**2-4 Topology and multivalued circuits**

In summary, any circuit analysis method makes use of two matrices in order to set up the equilibrium equations of the circuit. The first matrix contains the topological information of the circuit in the form of 1s,
Each solution means:

\[
\begin{align*}
    s_1 & : (v_i^{(1)}, i_i^{(1)}) \\
    s_2 & : (v_i^{(2)}, i_i^{(2)}) \\
    s_3 & : (v_i^{(3)}, i_i^{(3)})
\end{align*}
\]

For each element \( C_i \):

\[
\begin{align*}
    i_i &= f_i(v_i, v_j, \cdots) \\
    or \\
    v_i &= g_i(i_i, i_j, \cdots)
\end{align*}
\]

Figure 2.10: Multiple solutions in resistive circuits.

-1s and 0s. The second matrix contributes with the linear or linearized branch relationships. Because we are dealing with DC analysis, we refer to these relationships as \( i-v \) or \( v-i \) branch functions.

For circuits with multiple solutions, the set of values of branch variables (dependent and independent) is not unique even if the branch relationships are denoted by strictly monotone increasing functions\(^1\) (SMIFs). In Figure 2.10, the network \( \mathcal{N} \) is assumed to possess three DC solutions \((S_1 - S_3)\). Hence three different values of branch currents and branch voltages will be associated to each DC solution. Besides, the topological structure of the circuit remains the same. Thus the occurrence of multiple solutions can be found in the combined effects of the topology and the nonlinear nature of the branch functions.

The analysis will be restricted to branch relationships given in the form of SMIFs. In presenting a first statement, we will assume that a nodal analysis method is used (see eqn. 2.19). Two matrices serve to stipulate the equilibrium equation: the topology matrix \( A \) and the matrix with the linear or linearized branch relationships \( G \). Here, the matrix \( G \in \mathbb{R}^{b \times b} \) denotes the branch functions in the form of linearized

\(^1\)a function \( g \) is strictly monotone increasing if \( g(x_1) < g(x_2) \) for all \( x_1 < x_2 \)
expressions. If these expressions relate electrical variables of the same branch, then $G = \text{diag}[g_1, g_2, \cdots, g_b]$. Hence equation 2.19 establishes a linear combination of SMIFs.

In general, any circuit analysis method uses a topology matrix ($T$) and a branch relationships matrix ($\mathcal{W}$). If we assume that those branch relationships are SMIFs and they relate only electrical variables of the same branch, then the next statement can be given:

**Statement 2.1** If the branch relationships given (in linearized form) by the matrix $\mathcal{W}$ are SMIFs and they relate electrical variables of the same branch, then the resulting set of equilibrium equations cannot have more than one solution.

In plain words, the stipulated condition means that the circuit is constituted by elements with $i-v$ or $v-i$ characteristics which are SMIFs and there are no coupled elements [10,11].

The statement above is not sufficient to guarantee that the circuit has a solution. For functions exhibiting saturation, the solution may not always exist [8].

Another case arises when SMIFs or MIFs constitute the relationships of the nonlinear elements and the circuit contains coupled elements (controlled sources). In this case, the circuit may possess more than one DC solution depending on the combined effects of topology and the nonlinearities, i.e. in both $T$ and $\mathcal{W}$.

### 2-4-1 Non-SMIFs branch characteristics

If at least one branch relationship is given by a non-SMIF, then not only is the cause of multiple solutions found in the topology, but also in the non-SMIF itself. In this case, the topology may become the less dominant cause of multiple DC operating points.

**Statement 2.2** If at least one branch relationship is non-SMIF, then the resulting equilibrium equation may have more than one solution. Even if the circuit does not contain coupled elements.

Strictly speaking, non-SMIFs characteristics can also exhibit saturation, which cause that the existence of the solution cannot be guaranteed.
An example of the above case is the tunnel diode. It is well known that circuits in which this device appears may possess multiple solutions. However, this type of device is not often encountered in electronic circuits, whereas coupled elements with SMIF or MIF characteristics are quite common. For this reason, in this thesis, the focus is on analyzing circuits containing elements defined by continuous strictly monotone increasing functions and coupled elements. This class of element is of major importance in modeling more sophisticated electronic devices, e.g. the well-known Ebbers-Moll bipolar transistor model (in one basic version) is formed by two diodes (i.e. two SMIF's branch relationships) and two current-controlled current sources (i.e. two coupled elements).

Bibliography


CHAPTER 3

Nonlinear DC Analysis

A brief overview on network topology and a short description of commonly used network analysis methods were given in Chapter 2. The ultimate aim of those methods is to formulate the nonlinear equilibrium equations. The next step in order to complete the analysis is to solve them by using appropriate numerical techniques. In this chapter the focus of attention is on currently used methods for analyzing nonlinear circuits.

In fact, all electronic circuits can be considered as nonlinear; i.e. the functions used to define the relationship between the electrical variables (for DC analysis: usually voltages and currents) are not linear. Some electronic components are considered to be linear elements in a certain range or operating region. There are many applications that make use of this approximation; among others, filters and amplifier circuits. However, in other applications, the nonlinear characteristics are precisely required for the intended purposes. One important group of nonlinear circuits is constituted by circuits containing transistors. Many multistable circuits belong to this group.

We start this chapter with a brief discussion on the process of setting up the equilibrium equations that result from the circuit analysis. Because of the nonlinear nature of these equations, iterative procedures
have to be used to solve them. The Newton-Raphson method is the most commonly used one. In this chapter, this method will be described with emphasis on shortcomings in the case of equations with multiple solutions. Finally, we give a review of the most successful methods used to solve the problem of multiple solutions.

3-1 Formulation of the equilibrium equations

The set of equilibrium equations of a network is obtained by using some topological information on the network and the relationships of the components. This procedure yields a set of equations with as unknowns some electrical variables of the circuit. The variables contained in this set ($x$) are determined by the selected circuit analysis method. For example, nodal voltages for the nodal analysis method or loop currents for loop analysis. The set of equilibrium equations has the following form:

$$f(x) = 0$$  \hspace{1cm} (3.1)

Each component $C_i$ of the set of elements of the circuit ($C$) is defined by a relationship $F_i$. Then the equation above can be established as$^1$:

$$f(x) = f(F(V)) = 0$$  \hspace{1cm} (3.2)

If we assume that nodal analysis is applied, the resulting equilibrium equation — actually a form of the KCL — can be expressed as:

$$A_i - A_j =$$

$$Ag(A^tv_n) - A_j = 0$$  \hspace{1cm} (3.3)

where $A$ is the node-branch incidence matrix, $i$ the vector of currents, $v_n$ the vector of nodal voltages (the unknowns) and $j$ the vector of current sources. Further, the function $g(o)$ represents a $b \times 1$ vector of current

$^1$In order to be congruent with most of the authors in the field, $f$ is used to denote the set of equilibrium equations of the circuit resulting from some class of analysis. $x$ is used to denote any set of unknowns. Here, $F_i$ represents the relationship of the $i$-th electrical component and $V$ represents the set of electrical variables of the circuit.
functions in terms of \( v_n \), i.e. conductance functions. This equation can be recast in the following general form:

\[
f(v_n, j) = 0
\]  
(3.4)

These few manipulations stipulate that a certain amount of topological information has vanished by expressing the set of equilibrium equations in the closed form 3.4. Note that the topological information given through the incidence matrix \( A \) appears in 3.3 and seems to have disappeared in the final equation. The next table shows the same form of equilibrium equations for several circuit analysis methods:

<table>
<thead>
<tr>
<th>Method</th>
<th>Original form</th>
<th>Developed form</th>
</tr>
</thead>
<tbody>
<tr>
<td>Loop</td>
<td>( Cv_b - Ce = 0 )</td>
<td>( Cr \left( C^t_i \right) - Ce = 0 )</td>
</tr>
<tr>
<td>Cutset</td>
<td>( Di_b - Dj = 0 )</td>
<td>( Dg \left( D^t v_n \right) - Dj = 0 )</td>
</tr>
<tr>
<td>Nodal</td>
<td>( Ai_b - Aj = 0 )</td>
<td>( Ag \left( A^t v_n \right) - Aj = 0 )</td>
</tr>
</tbody>
</table>

where \( A, C \) and \( D \) are respectively the node-branch, loop-branch and cutset-branch incidence matrices, \( j \) and \( e \) the vectors of independent current and voltage sources, \( v_n, i_e \) and \( v_e \) are respectively the nodal voltages, loop currents and the voltages of the tree branches, i.e. the unknowns for respectively nodal analysis, mesh analysis and cutset analysis. The functions \( r(\phi) \) and \( g(\phi) \) are resistance and conductance functions in terms of the unknowns.

In general, it can be established that the equilibrium equations from any circuit analysis method result in the following long form:

\[
M \phi \left( \vartheta_{(M)}, \zeta_{(M)} \right) - M \zeta_{(M)} = 0
\]  
(3.5)

where \( M \) refers to the incidence matrix used by the network analysis method, \( \vartheta_{(M)} \) represents the electrical variables considered as unknowns by the method, \( \zeta_{(M)} \) are the natural independent sources in the method (e.g. current sources in Modified Nodal Analysis) and \( \zeta_{(M)} \) represent the non-natural independent sources (voltage sources in Modified Nodal Analysis) and \( \phi \) is the set of relationships of the components.
The closed form can thus be expressed as:

\[ f(\vartheta_n, e, j) = 0 \]  

(3.6)

The results is, evidently, that in the process of setting up the equilibrium equations, the topological information is mixed with all branch relationships and thus is hidden in the system of equation 3.6. This process, graphically depicted in fig. 3.1, leads to a fuzziness of information which becomes specially important if we consider multistable circuits. For this case, the function expressed in closed form in 3.6 has more than one solution.

All existing methods try to solve the DC problem by simply solving this set of equations. The topological information on the network is used only partially.

### 3-2 Newton-Raphson method

The most commonly used algorithm for solving (3.1) is the well-known Newton-Raphson method. It is an iterative procedure which approximates an initial set of values of the unknowns (\(x^0\)) to a final value. This final value can be considered as the solution (\(x^*\)) for a certain given tolerance. The method is frequently recast in the following recursive formula:

\[ x^{(j+1)} = x^{(j)} - [J(x^{(j)})]^{-1} f(x^{(j)}) \]  

(3.7)

where

\[ [J(x^{(j)})]^{-1} = \left[ \frac{df(x)}{dx} \right]_{x=x^{(j)}}^{-1} \]  

(3.8)
We will not extend the discussion beyond the perspectives of this thesis — the solution of nonlinear systems — and for this reason the theoretical considerations about convergence and rate of convergence will not be analyzed. In the literature, a group of dedicated works [1–4] offers extended and rigorous analysis of this and other related subjects. We mention here only the most important properties.

- **Convergence rate**

  The method converges to a solution \((x^*)\) provided that it *starts* from an initial guess \((x^0)\) *sufficiently close* to the solution. The rate of approach from the initial value to the solution is given by:

  \[
  \frac{|f(x^{(j+1)})|}{|f(x^{(j)})|} \rightarrow \text{constant}
  \]

- **Error rate**

  As a consequence of the quadratic rate of convergence, the error defined as \(\epsilon^{(j)} = |f(x^{(j+1)}) - f(x^{(j)})|\) also decreases quadratically; i.e.,

  \[
  \epsilon^{(j+1)} \leq k [\epsilon^{(j)}]^2
  \]

- **Behavior of \(J(x)\)**

  The method is able to converge to a solution \((x^*)\) iff \(J(x^*) \neq 0\).

Several Newton-like methods have appeared in the literature with the aim of improving the performance of the original method. Among these methods, perhaps the modified Newton-Raphson variant is the most commonly studied:

\[
x^{(j+1)} = x^{(j)} - H^{(j)} [J(x^{(j)})]^{-1} f(x^{(j)}) = x^{(j)} - H^{(j)} [\epsilon^{(j)}]. \tag{3.9}
\]

where the newly introduced \(H^{(j)}\) represents a diagonal matrix containing the step size used in each iteration to *scale* the error vector. This method is intended to be used to avoid the possible(s) singularity(ies) of \(J\), which occur at the turning points of \(f(x) = 0\). There are several variants to select optimal or quasi-optimal values of the elements of \(H^{(j)}\).
Figure 3.2 represents the geometrical interpretation of the Newton-Raphson method for the one-dimensional case. The iterative procedure is schematically shown in fig. 3.2-(a). In the same figure, the nonconvergence problem is illustrated. Firstly, in fig. 3.2-(b), an initial guess at point $b_1$ will cause the iterative process to oscillate around $b_1$ and $b_2$. In a similar form, an initial guess point $c_1$ will conduce the process to nonconvergence by diverging toward infinity. In addition, an initial guess at point $a_1$ will eventually converge to the solution at $x_a$; however, the solution at $x_d$ cannot be reached from the initial guess in (a). Other kind of behavior (namely chaotic behavior) can also occur, which occurs when extraneous saddle point(s) appears.

![Graph](image_url)

(a) (b) (c)

Figure 3.2: Geometrical interpretation of the Newton-Raphson method.

Because of its quadratic rate of convergence, the Newton-Raphson method is the most frequently used numerical tool for solving the set of equations resulting from nonlinear circuits. In order to improve its behavior (essentially to assure convergency), several schemes are used, among them can be mentioned:

- Limiting schemes

They limit the span of the permitted maximum (possibly also the minimum) value of the branch electrical variables in order to avoid overflow and to make the method converge.
3-2. NEWTON-RAPHSON METHOD

- Alternating bases algorithms

They are used specially for the exponential diode functions. They iterate over the normal function or over the inverse function, depending on the direction in which the current varies during the iterative process.

- Source-stepping schemes

They start the search for DC solutions by setting all sources to values lower than in the given circuit. Eventually a solution is found and the sources are increased in value, so that the previous solution is used as a set of starting values for the next search. This process is repeated until the sources reach the given values.

However, the Newton-Raphson method (and its variants) still have many shortcomings that become really problematic when one carries out the analysis of circuits possessing multiple solutions. Besides, those methods are able to find just only one DC operating point. In the case that 3.1 has more than one solution, it may occur that for some iteration \((j)\) the matrix \(J\) becomes singular. In this case the method cannot converge to any solution.

3-2-1 Circuit interpretation of the Newton-Raphson algorithm: the linearized branch concept

The problem of solving a circuit for DC analysis yields to the problem of solving the system of equations \(f(x) = 0\), where \(x\) represents the unknowns of the circuit. However, analyzing a circuit by constructing first \(f(x)\) and then attempting to solve this equation by applying the recursive formula of the Newton-Raphson method is not computationally efficient; instead, a linearization of the nonlinear elements is achieved in order to obtain a system of linear equations. This process can be better clarified if the recursive formula is written in a slightly different form:

\[
J(x^{(j)})x^{(j+1)} = -f(x^{(j)}) + J(x^{(j)})x^{(j)} \tag{3.10}
\]

in other words, the Newton-Raphson algorithm linearizes the nonlinear system \(f(x) = 0\) into a linear system of the form \(Ay = b\).
Figure 3.3: Linearized voltage-controlled branch.

Suppose that the $i$-th nonlinear element is defined by a voltage-controlled characteristic $i_i = g_i(v)$. By expanding this function in Taylor's series, we obtain:

$$i^{(j+1)} = \frac{\partial g(v)}{\partial v} \bigg|_{v=v(j)} v^{(j+1)} + g(v(j)) - \frac{\partial g(v)}{\partial v} \bigg|_{v=v(j)} v^{(j)}$$  \hspace{1cm} (3.11)

where:

$$\frac{\partial g(v)}{\partial v} \bigg|_{v=v(j)} = \left[ \frac{\partial g(v)}{\partial v_1} \bigg|_{v=v(j)}, \frac{\partial g(v)}{\partial v_2} \bigg|_{v=v(j)}, \ldots, \frac{\partial g(v)}{\partial v_n} \bigg|_{v=v(j)} \right]$$

If the branch relationship is only concerned with variables of the same branch, then the Newton-Raphson algorithm linearizes the nonlinear branch relationship and converts the branch into a composite branch (this equivalent circuit is also known [5] as the companion model of the nonlinear element). The equation above can be recast as:

$$i^{(j+1)} = I_{off}^{(j)} + G_{eq}^{(j)}v^{(j+1)}$$  \hspace{1cm} (3.12)

where

$$I_{off}^{(j)} = g(v(j)) - G_{eq}^{(j)}v^{(j)} = i(v(j)) - G_{eq}^{(j)}v(j)$$

and

$$G_{eq}^{(j)} = \left. \frac{df(v)}{dv} \right|_{v=v(j)}$$

The circuit shown in figure 3.3 represents the equivalent circuit of the linearized branch and fig. 3.4 the geometrical equivalence.

We note that the concept of linearization of the nonlinear branch preserves the topological information given through the incidence matrix;
Figure 3.4: Geometrical interpretation of the linearized branch.

however, in order to solve properly the problem of multiple DC operating points, the information from a dedicated topology must be obtained. This means that another formulation of the equilibrium equations must be established in order to make use of the circuit topology on its full extent.

3-3 Methods used to find more than one solution

As we have seen, Newton-like techniques have been used for solving the equations originated from nonlinear circuits, but they are able to find only one DC solution, depending on the given starting values for $x$. The problem remains in solving the algebraic nonlinear equation

$$f(x) = 0 \quad (3.13)$$

Other types of methods have been applied to solve the problem to finding more solutions to the system of nonlinear equations. They are often called continuous deformation methods, variable dimension methods or homotopy methods. They are based on the fact that all (in order to be realistic, it must be read as some) solutions can be connected by a curve.
This curve is called the *path of solutions*. This path constitutes, in fact, a seeking trajectory, which passes through the solutions. In order to construct this trajectory, these methods make use of a *continuation parameter*, which is embedded in the original equation. The resulting equation is sometimes called the *augmented equation*. When the continuation parameter is set to an initial value, then the augmented system is reduced to a system whose equations present a trivial, or easy to find, solution.

![Figure 3.5: Paths of solutions of continuation method.](image)

This solution is then considered the starting point of the trajectory or *continuation path*. From this starting point, the augmented equation is then continuously deformed. This process leads to a certain value of the continuation parameter. At this value the augmented equation has a solution equal to that of the original system \( f(x) = 0 \). All continuation methods convert the problem of trying to solve a set of nonlinear equations into a problem of integrating a set of differential equations.

Fig. 3.5 shows schematically the concept of the continuation trajectory. In this figure, the trajectory \( t_1 \) connects the solutions \( (x_1, x_2, x_3) \) and the trajectory \( t_2 \) connects \( (x_4, x_5, x_6) \). A variety of methods [6–8] have been developed in order to find more and more solutions of the equilibrium equations from nonlinear circuits. We limit our scope here to three classical works about continuation algorithms: Branin [9], Khao's method [10] and Chua's method [11]. The first method was the first attempt to solve the nonlinear equations pertaining to electrical circuits when these have more than one solution. Its simplicity is remarkable. The Khao's and Chua's methods are based on the introduction of an extra parameter.
3-3. METHODS USED TO FIND MORE THAN ONE SOLUTION

3-3-1 Branin’s method

This method is not precisely a continuation method in the sense that an embedded parameter appears in the numerical process of solution. However, it uses the *continuation philosophy* by allowing the path of solutions to be continued. The process of continuation is carried out by changing the sign of the determinant after a solution is found. This method is based on the integration of a related system of differential equations [9] which is obtained by adding to (3.1) an artificial parameter derivative:

\[
\frac{df}{dp} + f(x) = 0
\]

(3.14)

The basis of the method can be seen in the analytical solution of (3.14):

\[
f[x(p)] = f[x(0)] e^{-p}
\]

where it is obvious that eqn. (3.1) will be satisfied when \( p \to \infty \).

Since \( f(x) \) is not an explicit function of \( p \), it follows by using the chain-rule that:

\[
\frac{df}{dp} = \left( \frac{\partial f}{\partial x} \right) \frac{dx}{dp}.
\]

So that eqn. 3.14 can be recast in the form:

\[
\frac{dx}{dp} = - \left( \frac{\partial f}{\partial x} \right)^{-1} f(x) = -J^{-1} f(x)
\]

(3.15)

This equation proves to be effective as long as the Jacobian matrix \( J \) is nonsingular. The impasse point present at the Jacobian singularity is avoided by allowing a change of sign in (3.14):

\[
\frac{df}{dp} \pm f(x) = 0
\]

(3.16)

\( f[x(p)] = f[x(0)] e^{\mp p} \) being the solution.

Thus when \( \det J \) changes sign or when a solution of \( f(x) \) is obtained, the sign in (3.16) is changed and the integration may be continued.

Thus equation (3.15) becomes:

\[
\frac{dx}{dp} = \mp \left( \frac{\partial f}{\partial x} \right)^{-1} f(x) = \mp J^{-1} f(x)
\]

(3.17)
The iterative forward Euler method is applied to solve eqn. (3.17):

$$x_{k+1} = x_k + h_k \mathbf{J}_k^{-1} f(x_k) \quad (3.18)$$

Branin in his work made use of the adjoint matrix of \( \mathbf{J} \) in order to evaluate the inverse of \( \mathbf{J} \), besides accomplishing a normalization on the correction vector \( \mathbf{J} f(x) \) in order to avoid the explicit use of \( \text{det} \mathbf{J} \).

$$x_{k+1} = x_k + h_k \frac{\text{adj} \mathbf{J} f(x_k)}{\| \text{adj} \mathbf{J} f(x_k) \|} \quad (3.19)$$

This makes Branin’s method rather inefficient because each \( p \)-step requires the computation of the determinants which form \( \text{adj} \mathbf{J} \). Moreover, extraneous singular points may appear even when \( f(x) = 0 \) at \( \text{adj} \mathbf{J} f(x) = 0 \), which implies that \( \text{det} \mathbf{J} = 0 \). This method has the advantage of not requiring any prior initial guess so that it is self-starting.

### 3.3.2 Khao’s Method

This method is another implementation [10] of the idea given by Branin. It is intended to overcome the difficulties due to extraneous singularities by selecting an initial point which lies in a curve passing through all the solutions, provided that this curve is a single curve, i.e. a continuously differentiable curve which does not intersect itself and consists of only a single branch.

Instead of eqn (3.14), this method uses:

$$\frac{df_i[x(p)]}{dp} + f_i[x(p)] = 0 \quad f_i[x(0)] = 0 \quad i = 1, 2, \ldots, n - 1 \quad (3.20)$$

and the \( n \)-th equation is given as:

$$\frac{df_n[x(p)]}{dp} \pm f_n[x(p)] = 0, \quad f_n[x(0)] = f_{n0} \quad (3.21)$$
Both equations can be recast as:

\[
\frac{df}{dp}(x(p)) + \begin{bmatrix}
  f_1 [x(p)] \\
  f_2 [x(p)] \\
  \vdots \\
  f_{n-1} [x(p)] \\
  \pm f_n [x(p)]
\end{bmatrix} = 0
\]

The initial point \(x(0)\) is found by solving \(f_i(x) = 0, i = 1, 2, \ldots, n - 1\). This initial point lies in a curve \(\ell\). The derivative of \(f\) with respect to the parameter \(p\) can be calculated by using the chain rule:

\[
\frac{df}{dp} = \frac{df}{dx} \frac{dx}{dp} \equiv J \dot{x}
\]

By using this equation in combination with 3.20 and 3.21, we obtain:

\[
\dot{x} = J^{-1} \begin{bmatrix}
  -f_1 \ [x(p)] \\
  -f_2 \ [x(p)] \\
  \vdots \\
  -f_{n-1} \ [x(p)] \\
  \pm f_n \ [x(p)]
\end{bmatrix}
\]

Again, the forward Euler formula is used to solve the equation above:

\[
x_{k+1} = x_k - h_k J_{k}^{-1}(x_k) [f_1(x_k), f_2(x_k), \ldots, f_{n-1}(x_k), \pm f_n(x_k)]^t
\]

where \(x_0 \in \ell, \quad k = 0, 1, 2, \ldots \quad (3.22)\)

As previously performed in Brinian's method, the change of the sign of \(f_n\) must occur at the points where the Jacobian changes sign and at the solution points. In the first case, the change of sign prevents the curve \(\ell\) from moving away from the path of solutions; so that the non-convergence state caused by \(\det J = 0\) is also avoided. In the second case, the transition in sign should occur in order to allow the algorithm to search further for a next solution.

Khao's method is thus able to find a particular trajectory of solutions which coincides with the intersection of the \((n - 1)\) surfaces defined by
\( f_i = 0, i = 1, 2, \ldots, n - 1 \). The method has two major disadvantages: first, it is not a self-starting method because an initial point must be found, which could be rather time consuming and, second, this starting procedure can determine only one trajectory and it may occur that solutions lie in other trajectories; thus only those solutions related to one particular trajectory can be found.

3-3-3 Chua’s Method

This method [11] introduces a parameter \( \mu \) in the original system defined by eqn. (3.1); it yields an augmented system of \( n \) equations:

\[
\dot{f}(x, \mu) = 0
\]  
(3.23)

in \( (n + 1) \) unknowns \([x, \mu]\). This system has two properties:

1. At some initial value \( \mu = \mu_0 \) a solution \( x_0 \) is known, a priori:

\[
\dot{f}(x_0, \mu_0) = 0
\]
(3.24)

2. At some value \( \mu^* \neq \mu_0 \), eqn. (3.23) reduces to eqn. (3.1); i.e.,

\[
\dot{f}(x, \mu^*) = f(x) = 0
\]
(3.25)

A way to obtain an augmented version of (3.1) is by using the following system:

\[
\dot{f}(x, \mu) = f(x) + (\mu - 1)f(x_0) = 0
\]
(3.26)

where \( x_0 \) is any initial guess. The equation above satisfies (3.24) and (3.25) at \( \mu_0 = 0 \) and \( \mu^* = 1 \). Firstly, at \( \mu_0 = 0, \dot{f}(x, 0) = f(x) - f(x_0) \) has an obvious solution at \( x = x_0 \) and, secondly, \( \dot{f}(x, 1) = f(x) \).

The system in eqn. (3.26) has one more unknown than equations, thus there are many possible solutions for it, but if \( \mu \) is fixed, then the solutions of the augmented system can be geometrically interpreted as a set of space curves in the \((x_1, x_2, \ldots, x_n, \mu)\)-space, where the initial value \( x_0 \) lies on the hyperplane \( \mu = \mu_0 \) and the solution \( x^* \) lies on the hyperplane \( \mu = \mu^* \).
3.3. METHODS USED TO FIND MORE THAN ONE SOLUTION

In his work, Chua formed a slightly changed version of eqn. (3.14):

\[ \frac{d \hat{f}(x, \mu)}{dp} + c \hat{f}(x, \mu) = 0 \]  \hspace{1cm} (3.27)

where \( c \) is an arbitrary positive constant which serves as a damping factor, as we see in the analytical solution given by:

\[ \hat{f}[x(p), \mu(p)] = \hat{f}[x(0), \mu(0)] e^{-cp} = \hat{f}[x_0, \mu_0] e^{-cp} \]

Equation (3.27) can be rewritten as:

\[ \frac{d \hat{f}(x, \mu)}{dp} = \begin{bmatrix} \frac{\partial \hat{f}(x, \mu)}{\partial x} & \frac{\partial \hat{f}(x, \mu)}{\partial \mu} \end{bmatrix} \begin{bmatrix} \frac{dx}{dp} \\ \frac{d\mu}{dp} \end{bmatrix} = -c \hat{f}(x, \mu) \] \hspace{1cm} (3.28)

However, the equation above represents a system of \( n \) equations in \((n+1)\) unknowns. The lacking equation is given by:

\[ \text{sgn}(\frac{dx_k}{dp}) \frac{dx_k}{dp} = 1 \] \hspace{1cm} (3.29)

and is intended to allow the continuation procedure.

Equations (3.28) and (3.29) can be expanded as follows:

\[ \begin{bmatrix} \frac{\partial \hat{f}_1}{\partial x_1} & \frac{\partial \hat{f}_1}{\partial x_2} & \cdots & \frac{\partial \hat{f}_1}{\partial x_k} & \cdots & \frac{\partial \hat{f}_1}{\partial x_n} & \frac{\partial \hat{f}_1}{\partial \mu} \\ \frac{\partial \hat{f}_2}{\partial x_1} & \frac{\partial \hat{f}_2}{\partial x_2} & \cdots & \frac{\partial \hat{f}_2}{\partial x_k} & \cdots & \frac{\partial \hat{f}_2}{\partial x_n} & \frac{\partial \hat{f}_2}{\partial \mu} \\ \vdots & \vdots & \cdots & \vdots & \cdots & \vdots & \vdots \\ \frac{\partial \hat{f}_n}{\partial x_1} & \frac{\partial \hat{f}_n}{\partial x_2} & \cdots & \frac{\partial \hat{f}_n}{\partial x_k} & \cdots & \frac{\partial \hat{f}_n}{\partial x_n} & \frac{\partial \hat{f}_n}{\partial \mu} \\ 0 & 0 & \cdots & \text{sgn}(\frac{dx_k}{dp}) & \cdots & 0 & 0 \end{bmatrix} \begin{bmatrix} \frac{dx_1}{dp} \\ \frac{dx_2}{dp} \\ \vdots \\ \frac{dx_n}{dp} \\ \frac{d\mu}{dp} \end{bmatrix} = \begin{bmatrix} -c \hat{f}_1(x, \mu) \\ -c \hat{f}_2(x, \mu) \\ \vdots \\ -c \hat{f}_n(x, \mu) \\ 1 \end{bmatrix} \] \hspace{1cm} (3.30)

The iterative forward Euler method is applied to solve eqn. (3.30):

\[ x_{i+1} = x_i + \mathbf{J}_i^{-1}(x_i) \begin{bmatrix} \hat{f}_1, \hat{f}_2, \cdots, \hat{f}_n, \mu \end{bmatrix}^T \] \hspace{1cm} (3.31)

where \( \mathbf{J} \) is the square matrix \([\cdot]\) in eqn. (3.30).

As with Khao’s method, Chua’s algorithm cannot reach those solutions lying in a trajectory different than that being traced.
3-3-4 Properties

In summary, the previously discussed methods are able to find more than one solution to the system of nonlinear equations of a nonlinear resistive circuit. However, they have several shortcomings, which will be briefly explained hereunder.

In general, continuation methods incorporate an extra parameter into the original equation in order to form the augmented equation with the form:

$$\mathcal{H}(\mathbf{f}(\mathbf{x}), \mu) = 0 \tag{3.32}$$

This expression is called a homotopy relationship or, for short, homotopy. Several forms of homotopy (i.e. the manner in which $\mu$ and $\mathbf{f}(\mathbf{x}) = \mathbf{0}$ are related in order to form 3.32) have been developed. Unfortunately, those forms are able to compute all the solutions for only specific cases. For instance, in [12] a homotopy form is given. This particular method is able to deal with polynomials and to find all the solutions to them. This means that a specific form of homotopy behaves correctly (i.e. finds all solutions) for certain reduced types of nonlinearities.

Another characteristic of continuation methods is related to the number of paths that can be found. Figure 3.5 shows a space of solutions with two paths. This problem is closely related to the determination of the initial point $p_o$. It leads to the conclusion that the homotopy at some initial guess $\mu_o$ does not always have a unique solution. The existence of more than one path means that one is not completely sure if all solutions have been found.

The possibility that more than one path exists reveals another aspect of the homotopy methods: the paths of solutions can be open or closed paths. In the first case, the method starts at some initial point and searches for solutions. During this process, a curve passing through several (resp. all) solutions is found. However after the last (resp. $n$-th) solution is found, the method continues seeking for more possible solutions, until it diverges. Thus, there is not a reliable stop criterion in order to decide when the search can be stopped. In the second case, the solutions lie on a closed path. By starting at some initial point $p_o$, the method draws a curve passing along several solutions; but because of the fact that they lie in a closed path, eventually the method will come back
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to the initial solution. Here the essential problem is that one cannot assert that the set of solutions lying in the path constitutes the whole set of solutions of the system.

A very important aspect from the point of view of a circuit designer is the nature of the solution. Unfortunately, these methods do not give any information about the stability of the found solution.

The above aspects clearly show that homotopy methods are able to find more than one solution, but they have major disadvantages which can be summarized as follows:

- **Uniqueness of the trajectory**
  They cannot guarantee that all the solutions of the system lie on a certain found trajectory. This disadvantage is closely related to the process of finding an initial point $p_0(x_o, \mu_o)$.

- **Repeated solutions**
  It may occur that the set of solutions includes repeated solutions, in this case the trajectory constitutes a closed path.

- **Stop criteria**
  For open trajectories, the found solutions correspond to the solutions lying on one side of the trajectory, depending on the starting point. After this is achieved, the integration method continues searching for more solutions.

  For closed trajectories, the method returns to previously found solutions and stays oscillating.

- **Number of solutions**
  One cannot assert that all solutions have been found.

- **Extraneous singularities**
  Other limitations are related to the extraneous singularities of the differential equation. Of course, they are unique for each $f(x) = 0$.

- **Nature of the solutions**
  There is no information about the qualitative characteristics of any found solution.
In view of the above, we see that it is necessary to employ other methods that can cope with these disadvantages, which, combined with the potential of numerical tools, give a reliable solution of the problem.

Bibliography


CHAPTER 4

Topological approach

4-1 Introduction

In order to formulate the problem of nonlinear circuits having multiple solutions from a point of view which takes into account the topology of the circuit, it is reasonable to develop the analysis within certain bounds or definitions, which in turn helps us to contend with the problem. In this chapter, the analysis is restricted to circuits containing bipolar transistors as nonlinear components.

As has been said, our objective is determining the multiple solutions of circuits in DC, but we limit the scope of our analysis to circuits containing strictly monotone increasing functions. Under these constraints, multiple equilibrium points may appear as a result of the manner in which the elements are interconnected and of the values of the parameters (values of the linear components and the coupled constants, among which are the α’s from the transistors).

Various works have been focused on the solution of this problem for circuits containing nonmonotone functions, which represents indeed a more general class of nonlinear branch relationships, but from a more practical point of view it appears that they comprise a very small class of electronic circuits, such as tunnel diode circuits. Besides, in these cases
the possibility of multiple solutions resides not only in the topology, but primordially in the type of non-monotonicity.

Several approaches have been proposed to the analysis of nonlinear circuits which have the possibility to possess more than one equilibrium point. Among these approaches, we can mention, for instance, the methods based on the testing of the \(v-i\) characteristic on a certain predefined port of the circuit. These methods are based on the concept of negative resistance devices. Several works appear in the literature [1–3] on methods for coping with such a class of device. These works make use of a property of any circuit with multiple solutions: circuits with multiple solutions present \(v-i\) (or \(i-v\)) characteristics with a region of negative conductance (or resistance).

Other methods cope with the problem of the stability of the multiple solutions. They conclude that the stability cannot be rigorously assessed on the basis of the analysis of the resistive circuit alone, [4,5].

In order to tailor this class of method to nonlinear resistive networks, it becomes necessary to add dynamic elements to the original resistive network. This process is denoted in figure 4.1(a). The idea behind this approach is that every nonlinear dynamic circuit has a DC operating point which constitutes indeed the solution of an equivalent resistive circuit, when the dynamic elements are not taken into account. In this form, the DC solution permits the obtaining of a linearized equivalent circuit, which in combination with the dynamic elements determines the time domain behavior and the location of the poles.

When the time-domain response is used, the excitation is set to an \(ad hoc\) input (e.g. a ramp function) and the analysis is achieved until the circuit reaches the steady state response. This method is known as pseudo-transient analysis. Clearly these methods are able to determine the stability of only one operating point. However, the stability of the resulting dynamic circuit is often dependent on the values of the chosen dynamic elements (in the figure capacitors). This means that it may occur that an originally stable bias point becomes unstable due to the choice of values for the dynamic elements.

The root locus of the circuit can also be used as a criterion for determining the stability of the DC operating point: if the resulting linearized circuit at the DC operating point has positive natural real poles or
Figure 4.1: Stability of dynamic linearized circuit.
complex conjugate natural poles with a positive real part, then the dynamic circuit is unstable and the DC operating point at which the circuit has been linearized is said to be also unstable. In other words, if a certain positive-valued dynamic element has been added, then the original DC circuit presents a negative valued resistance at the port where the dynamic element is connected. This method tests the resistive circuit for the occurrence of a negative slope in the $i$-$v$ characteristic of any two nodes of circuit. Figure 4.1(b) shows schematically this concept.

Although these methods deal with DC analysis of nonlinear resistive circuits, they are not able to find all possible solutions and they do not solve the problem of finding an upper bound on the number of possible solutions. The work done in this area can be reclassified according to several categories, which actually represent the state of the art in the field of nonlinear resistive circuits.

4-1-1 The work of Nielsen, Wilson et al

The contribution made by this group of works [6–12] is mainly concerned with the existence and uniqueness of the solution of circuits containing positive linear resistors, transistors, diodes and independent current and voltage sources. The major result of these works has been presented in the form of a theorem, which states that a circuit possesses one and only one solution if it cannot be reduced to a certain structure containing two transistors in the configuration shown in fig. 4.2. This structure is obtained by reducing some of the branches in the original circuit to short or open circuits (the branches corresponding to the independent sources and the linear resistors) and all the transistors (except two) to a combination of short and/or open circuits.

An important result derived from the previous works was presented in [13], which is focussed to predict an upper bound on the number of solutions for circuits containing two transistors. It shows that no more than three solutions are possible for this class of circuit. However, its scope of applications is very limited, since it deals with two-transistor circuits only. However, this is the only work focussed to determine the possible upper bound on the number of DC operating points.
Finally, an extension of the work of Nielsen was presented by Trajković and Nielsen for circuits containing Darlington-like structures [14] and a more general analysis of the existence and uniqueness of the solution of transistor circuits is done in [15] when the transistors have variable current gains for circuits containing two transistors.

4-1-2 The work of Nishi and Chua

Both authors directed their efforts [16–19] towards developing a graphical approach to determine the existence and uniqueness of the solution for circuits containing positive linear resistors, independent sources, the four types of transactors (controlled sources) and nonlinear resistors with strictly monotone increasing $i$-$v$ or $v$-$i$ relationships. Their result led to a topological equivalent of the result given by Nielsen & Wilson. Their method is based on the manipulation of the original graph of the circuit to obtain a reduced graph which is called a cactus graph (see fig. 4.3). This graph is obtained by applying to the original graph a series of graph operations in a way similar to the way in which Nielsen’s method operates with the branches of the circuit.

4-1-3 The work of Hasler and Fosséprez

Both authors made a contribution to determining the existence and uniqueness of the solution of nonlinear resistive circuits [4, 5]. In [20] the later author established a theory which connects the behavior of the
circuit with its topology. Their study is focussed on circuits represented by theoretical equivalent elements such as nullators and norators; which allows them to apply this method to circuits containing operational amplifiers. Their method can be considered as a continuation of Nishi and Chua’s work, but with more emphasis on the set of parameter values of the circuit.

In summary, it can be said that the all previously cited works represent very important contributions to the theory of nonlinear circuits in general, but they do not cope with the problem of finding an upper bound on the number of possible solutions, or the location of all of them. They just partially solve the DC problem, because they are focussed on coping with the problem of the existence and uniqueness of the DC solution. They are certainly more topologically oriented than the continuation methods discussed in the previous chapter, but still they have severe limitations in the implementation. This is caused by the exponential nature of the problem, which implies that the time required for calculation strongly increases with the number of transistors. In particular, Nielsen’s method deals with the calculation of $2^q$ determinants, $q$ being the number of transistors. However, the methods of the other authors carry out a graph-oriented analysis, in which $2^n$ ($n$ being the number of branches defined by nonlinear relationships) possible graph permutations have to be tested.
It is necessary to find a method that can solve these deficiencies, but that still has insight into the topology of the circuit and not only into the equations coming from the analysis of the circuit.

4-1-4 General nonlinear resistive-circuits

In order to establish the class of circuits this work is devoted to, a brief classification of the elements that these circuits may contain must be done. The branches of any nonlinear resistive circuit can be classified as:

- Constant $i$ or $v$ branches.
- Linear $i-v$ or $v-i$ defined branches.
- Nonlinear $i-v$ or $v-i$ defined branches.
- Dependent (linear and nonlinear) defined branches.

![Diagram of a general nonlinear network](image)

Figure 4.4: General nonlinear network.

The linearly defined branches represent positive linear resistors or positive linear conductances. The nonlinear branches actually are constituted by elements with strictly monotone increasing $i-v$ or $v-i$ functions,
which implies a restriction in the number of circuits that can be analyzed but, however, it offers the possibility to analyze a large class of electrical circuits, which can be described by means of strictly monotone increasing branch relationships.

Figure 4.4 shows this in a schematic representation. The most external circle represents the nonlinearities of the circuit and contains as well the branches defined by nonlinear relationships as the branches which couple variables of one branch to another branch. The internal circle represents the set of linear branches and constants of the circuit (e.g. DC sources).

Several methods can be developed based on the type of nonlinear branches the circuit contains. In this work attention is given to circuits containing bipolar transistors.

With this representation we make a separation between the linear portion and the nonlinear portion of the circuit. In this form, the possible DC solutions are generated as the result of the interaction between both parts of the circuit.

### 4-2 General BJT–circuits

There are many useful circuits with a relevant role in electronics which contain bipolar transistors. Most of them are designed to possess a single DC operating point, others, contrarily, must be designed to have more than one DC point in order to function properly and, a third group of them may have more than one DC solution even when they are intended to have a single one. In this section, analysis of circuits with BJTs is done in a systematic form with the aim of formulating a basic theory which will be used to predict the conditions which cause a circuit to have more than one solution in DC.

#### 4-2-1 Transistor modeling

In order to implement the analysis of circuits containing transistors, it is necessary to use a mathematical model for the transistor. This model is used to describe the device as a set of branches (or set of two terminal components). A model that is in widespread use has been proposed
by Ebers and Moll [21]. This model is drawn in fig. 4.5. This is the simplest model for a bipolar transistor, it does not describe all possible effects due to the physical mechanisms acting in BJTs; however, it is able to cope with the first-order effects and, because of its simplicity is the most frequently used model in the current simulators. For the purpose of the initial setting of the formulation, this model is adequate to express the basic equations involved in coping with the problem of multistable points. The functions $f_1(v_1)$ and $f_2(v_2)$ represent continuous and strictly monotone increasing functions. Usually, one regards both functions as typical diode exponential functions. We will use this basic model in our analysis.

### 4-2-2 Representation of transistor circuits

A canonical representation for circuits containing bipolar transistors has been used [6] to determine the existence and uniqueness of the solution of transistor circuits. It is based on the idea given in fig. 4.4. This representation is shown in fig. 4.6. The linear portion of the circuit and the independent sources are included in the $2n$-port, where $n$ is the number of transistors. Each pair of ports is connected to a transistor. This $2n$-port can be characterized by an equation of the form:

$$ Bv = Qi + c $$

(4.1)
where $B$ and $Q \in \mathbb{R}^{2n \times 2n}$, $i$ and $v \in \mathbb{R}^{2n}$ are the currents and voltages of the $2n$-port, and $c \in \mathbb{R}^{2n}$ is the vector related to the independent sources.

In this representation, each transistor has associated a pair of currents of the port. These are given as functions of the nonlinear relationships and the coupling constants, i.e.:

$$i = \left[ \begin{array}{c} i_1 \\ i_2 \end{array} \right] = -\left[ \begin{array}{cc} 1 & -\alpha_r^{(1)} \\ -\alpha_f^{(1)} & 1 \end{array} \right] \left[ \begin{array}{c} f_1(v_1) \\ f_2(v_2) \end{array} \right]$$  \hspace{1cm} (4.2)
For the whole set of transistors, the current vector is given by:

\[
\begin{bmatrix}
i_1 \\
i_2 \\
i_3 \\
i_4 \\
\vdots \\
i_{2n-1} \\
i_{2n}
\end{bmatrix}
= -\begin{bmatrix}
1 & -\alpha_r^{(1)} \\
-\alpha_f^{(1)} & 1 \\
1 & -\alpha_r^{(2)} \\
-\alpha_f^{(2)} & 1 \\
\vdots & \vdots \\
1 & -\alpha_r^{(n)} \\
-\alpha_f^{(n)} & 1
\end{bmatrix}
\begin{bmatrix}
f_1 \\
f_2 \\
f_3 \\
f_4 \\
\vdots \\
f_{2n-1} \\
f_{2n}
\end{bmatrix}
\]  

(4.3)

The block diagonal matrix in the equation above is denoted as the matrix \( T \). It contains \( n \) 2 \times 2 diagonal blocks of the form given in (4.2). By substituting \( i = -Tf(v) \), we obtain:

\[
Af(v) + Bv - c = 0
\]  

(4.4)

where \( A = QT \) and \( f(v) \) represents the diode functions of the transistor model.

This equation represents the general description of the circuit and constitutes a system of \( 2n \) nonlinear equations. The linear resistors and the network topology determine both \( A \) and \( B \); these matrices are not affected by changes in the values of the independent sources. Equation (4.4) is indeed the equilibrium equation of the circuit, but in contrast with the more general equation \( f(x) = 0 \), it separates both linear and nonlinear portions of the circuit, which are in close relation with the topology. The derivative of this function with respect to \( v \) constitutes the Jacobian and it is given by:

\[
J(v) = \frac{\partial[Af(v) + Bv - c]}{\partial v} = A \frac{\partial f(v)}{\partial v} + B
\]

Because \( f(v) \) represents the nonlinear relationships of the diodes of the transistor model which are modeled by strictly monotone increasing
functions, we can obtain:

\[ J = AD + B \]

where \( D = \text{diag}(d_1, d_2, \cdots, d_n) \), with \( d_i = \frac{df_i(x_i)}{dx_i} > 0 \), for \( i = 1, 2, \cdots, n \).

So that:

\[ \det J = \det [AD + B] \quad (4.5) \]

This determinant is closely related to the behavior of the circuit in DC. This fact can be exposed in two different manners:

- The behavior of the determinant inside an iterative process.
  During the process of solution of the system of nonlinear algebraic equations the value of \( \det J \) varies. If it changes sign along this process, then the circuit under analysis may possess more than one DC operating point.

- The behavior of the determinant as a function of a sweeping parameter.
  More often, it is required to find the operating point for several values of a certain circuit parameter (mostly a voltage source). In this case, a DC solution corresponds to each value of the sweeping parameter. Also \( \det J \) possesses a value at the found solution. The determinant changes of value as the sweeping parameter varies. If it varies sign, then the circuit has more than one solution or DC operating points. In this case the curve \( \det J \) vs. sweeping parameter does not actually constitute a monotone increasing function.

It is necessary to emphasize the importance of this determinant. It has the same interpretation as the determinant that was derived when the Newton-Raphson method was used to solve the system of nonlinear equations derived from the analysis of the circuit. In that case the Jacobian matrix is given as \( J = \frac{\partial f(x)}{\partial x} \). The determinant is given in such a form that it is difficult to get information about the behavior of the circuit in DC analysis.

At this stage, we are capable of expressing the determinant in terms of the matrices of the circuit under the general representation here employed. This determinant is used to determine the conditions on the
parameter values which cause more than one solution. It is based on the fact that in order to have more than one DC point, the determinant must change sign, i.e. it becomes zero for some set of parameter values.

4-3 \( \det [AD + B] \)

In this section we set up the expression for \( \det J \) in terms of the matrices \( A, D \) and \( B \). In order to achieve this, in the next subsection some useful definitions are given. We use these definitions in order to obtain a closed form of equation (4.5). A more detailed analysis of the juxtaposing sets and the derivation of the formulas are given in appendix A.

4-3-1 Juxtaposed set of matrices

Here an introduction to \( C \) sets (or juxtaposed sets) is presented.

**Definition 4.1** Given a pair of real \( n \times n \) matrices \((X, Y)\), the set of matrices \( C(X, Y) \) consists of all \( n \times n \) matrices that can be constructed by juxtaposing columns taken either from \( X \) or \( Y \) while maintaining the original relative ordering of the columns. This set contains obviously \( 2^n \) matrices.

The most basic \( C \) set is formed when the involved matrices are the identity matrix \( I \) and the null matrix \( \phi \). We denote this set as \( \Delta \) and its \( k \)-th component as \( \Delta_k \). Then:

\[
\Delta = C(I, \phi)
\]

**Definition 4.2** Given two matrices

\[
\Delta_a = \text{diag}[d_a^{(a)}] \quad \Delta_b = \text{diag}[d_b^{(b)}]
\]

\( \in C(I, \phi) \). They form a complementary pair if \( \forall k = l \)

\[
\begin{align*}
d_i^{(a)} + d_k^{(b)} &= 1 \\
d_i^{(a)}d_k^{(b)} &= 0 \\
a + b &= 2^n - 1
\end{align*}
\]
CHAPTER 4. TOPOLOGICAL APPROACH

Obviously:

\[ \Delta_i + \Delta_{2^n-1-i} = I \]
\[ \Delta_i \Delta_{2^n-1-i} = \Delta_{2^n-1-i} \Delta_i = \phi \]

In order to illustrate this definition, assume that 6 \times 6 matrices are involved. So that for \( i = 10 \), the elements \( \Delta_{53} \) and \( \Delta_{10} \) are given by:

\[ \Delta_{10} = \begin{bmatrix}
0 & 0 & 0 & 0 & 0 & 0 \\
0 & 0 & 0 & 0 & 0 & 0 \\
0 & 0 & 1 & 0 & 0 & 0 \\
0 & 0 & 0 & 0 & 0 & 0 \\
0 & 0 & 0 & 0 & 0 & 1 \\
0 & 0 & 0 & 0 & 0 & 0 \\
\end{bmatrix} \quad \Delta_{53} = \begin{bmatrix}
1 & 0 & 0 & 0 & 0 & 0 \\
0 & 1 & 0 & 0 & 0 & 0 \\
0 & 0 & 0 & 0 & 0 & 0 \\
0 & 0 & 0 & 1 & 0 & 0 \\
0 & 0 & 0 & 0 & 0 & 0 \\
0 & 0 & 0 & 0 & 0 & 1 \\
\end{bmatrix} \]

i.e. \( \Delta_{10} = \text{diag}[0, 0, 1, 0, 1, 0] \) and \( \Delta_{53} = \text{diag}[1, 1, 0, 1, 0, 1] \)

4-3-2 Closed form of \( \det [AD + B] \)

By making use of the definitions above, we are able to express \( \det [AD + B] \) in terms of the matrices taking part in the definition of the circuit. A more exhaustive analysis and the proof of the theorem can be found in Appendix A.

The first important theorem is given as follows:

\textbf{Theorem 4.1} \( \det J = \det [AD + B] \) can be expanded in the form:

\[
\begin{bmatrix}
\det [AD + B] = \sum_{i=0}^{(2^n-1)} \det [AD \Delta_{2^n-1-i} + B \Delta_i] \\
\end{bmatrix}
\]

(4.6)

By using the definitions of the preceding sections, which take into account the parity of all matrices here involved, we can obtain the equation above in terms of complementary pairs:

\[
\begin{bmatrix}
\det [AD + B] = \\
\sum_{i=0}^{(2^n-1)} \det [AD \Delta_{2^n-1-i} + B \Delta_i] + \det [AD \Delta_i + B \Delta_{2^n-1-i}] \\
\end{bmatrix}
\]

(4.7)
\[ \det [AD + B] = \sum_{i=0}^{2^n-1} \det [AD \Delta_{2^n-1-i} + B \Delta_i] \]

Figure 4.7: Interpretation of \( \det [AD + B] \).

Equations (4.6) and (4.7) express the determinant as a combination of the matrices involved in the circuit: \( A \) determining the nonlinear portion, \( B \) determining the linear portion and \( D \) containing the derivatives of the nonlinear functions. The conditions which cause the determinant to become zero can then be deduced from each separated term in the summation. By taking the first and the last elements of equation (4.6) or the first element of (4.7) we can express:

\[
\det [AD + B] = \frac{\det [AD]}{\det [B]} + \sum_{i=1}^{2^n-2} \det [AD \Delta_{2^n-1-i} + B \Delta_i] + \det [B] \tag{4.8}
\]

This equation remains with a binary structure, which is due to the fact that the same structure occurs for the pair formed by \( (\Delta_i, \Delta_{2^n-1-i}) \).
The summation has in its extremes the elements $\Delta_0 = \phi$ and $\Delta_{2^n-1} = I$, while in the middle part a combination of terms occurs. It means that each term in the summation has a particular well-defined structure. In plain words, we can regard the equation above as a complete set of cross-referenced information between both portions of the circuit. Firstly, this set contains information about both pure portions of the circuit (linear and nonlinear part) —0-th term in equation (4.7) and 0-th and $(2^n - 1)$-th term in (4.6). Secondly, this equation contains also a combination of information from both portions of the circuit, which is given through the matrices $\Delta_i$. This structure is schematically denoted in fig. 4.7.

Finally, equation (4.6) can be also expressed as:

$$\det [AD + B] = \sum_{i=0}^{2^n-1} \det C_i \det \theta_i$$  \hspace{1cm} (4.9)

where $C_i \in \mathcal{C}(A, B)$ and $\theta_i \in \mathcal{C}(D, I)$.

It can be assumed without loss of generality that $A = T$. In this case, $B$ represents an admittance matrix for the linear portion of the circuit. Because of the fact that this linear portion contains only positive resistors and independent sources, $B$ is symmetric and positive. In this form, the equation (4.6) can be given as:

$$\det [TD + B] = \det [TD] + \sum_{i=1}^{2^n-2} \det [TD\Delta_{2^n-1-i} + B\Delta_i] + \det [B]$$

and equation (4.9) is given as:

$$\det [AD + B] = \det [TD + B] = \sum_{i=0}^{2^n-1} \det \tau_i \det \theta_i$$  \hspace{1cm} (4.10)

where $\tau_i \in \mathcal{C}(T, B)$ and $\theta_i \in \mathcal{C}(D, I)$.

The sign of the determinant $\det [AD + B]$ is an indicator for possible multiple-solution conditions. All equations above denote this determinant as a polynomial in the $d_i$ components of $D$. The development of
4-4. TOPOLOGICAL IMPLICATIONS OF $C(T, B)$

Equation (4.9) shows more clearly this characteristic:

$$\det [AD + B] = \det C_0 \det \theta_0 + \det C_1 \det \theta_1 + \det C_2 \det \theta_2 + \cdots$$

$$\det C_{2n-2} \det \theta_{2n-2} + \det C_{2n-1} \det \theta_{2n-1} =$$

$$\det[a_1, a_2, \ldots, a_{n-1}, a_n]d_1d_2 \cdots d_{n-1}d_n + \det[a_1, a_2, \ldots, a_{n-1}, b_n]d_1d_2 \cdots d_{n-1} + \cdots$$

$$\det[b_1, b_2, \ldots, a_{n-1}, a_n]d_{n-1}d_n + \det[b_1, b_2, \ldots, b_{n-1}, a_n]d_{n-1} + \det[b_1, b_2, \ldots, b_{n-1}, a_n]d_n + \det[b_1, b_2, \ldots, b_{n-1}, b_n] =$$

$$c_1^{12 \cdots n-1, n}d_1d_2 \cdots d_{n-1}d_n + c_1^{12 \cdots n-1, n}d_1d_2 \cdots d_{n-1} + \cdots$$

$$c^{n-1,n}d_{n-1}d_n + c^{n-1}d_{n-1} + c^n d_n + c^0$$

Where $c^k$ is the determinant associated with a matrix from the set $C(A, B)$.

Each term has associated a set of $\alpha$'s according to the columns of $A$ contained in $C_i$. For instance, if we consider a circuit with two transistors ($n = 4$), then the term denoted in the summation by 6 (in binary 0110) involves the term $A\Delta_6 + B\Delta_9 = [b_1, a_2, a_3, b_4]$ which has associated the set $\alpha_r^{(1)}, \alpha_f^{(2)}$.

4-4 Topological implications of $C(T, B)$

In the equation above, three matrices play a main part in the description of the transistor network:

<table>
<thead>
<tr>
<th>$T$</th>
<th>Transistor relationships: Coupling factors</th>
</tr>
</thead>
<tbody>
<tr>
<td>$D$</td>
<td>Diode function derivatives</td>
</tr>
<tr>
<td>$B$</td>
<td>Linear elements</td>
</tr>
</tbody>
</table>
The vector $\mathbf{D}$ represents the derivatives of the exponential diode functions from the transistor model. Because of the fact that they are strictly monotone increasing functions, $\mathbf{D}$ contains elements with value greater than or equal to zero. If the analyzed circuit results to have a certain solution, then $\mathbf{D}$ is the vector with the linearized conductances at the obtained operating point. It clearly results that for another DC solution the set of values of $\mathbf{D}$ must be different, i.e. $\mathbf{D}$ is merely a consequence of the resulting DC operating point, and it does not play any role in the number of solutions nor in the location of them. Figure 4.8 shows schematically this fact. The sphere is the space of possible solutions; $S_1$, $S_2$ and $S_3$ represent three DC solutions. For each $S_i$ there is a different vector $\mathbf{D}$, here denoted as $\mathbf{D}^{(i)}$.

Henceforth, this means that the possibility of multiple solutions must be found in the structure of both the linear and nonlinear parts of the circuit; i.e. in both matrices $\mathbf{T}$ and $\mathbf{B}$. This makes the set $\mathcal{C}(\mathbf{T}, \mathbf{B})$ of special importance in the process of predicting the number of possible solutions.

![Figure 4.8: Multiple solutions and matrices involved.](image-url)
4-4-1 Classification of the terms in the set \( C(T, B) \)

As has been shown in the preceding section, each \( C_i \in C(T, B) \) is a matrix formed by taking columns of \( T \) and \( B \). Every time that a column from the transistor matrix is taken, \( C_i \) contains a column of the form:

\[
\begin{bmatrix}
: \\
0 \\
1 \\
-\alpha_i^{(q)} \\
0 \\
: \\
\end{bmatrix}
\quad \text{or} \quad
\begin{bmatrix}
: \\
0 \\
-\alpha_i^{(q)} \\
1 \\
0 \\
: \\
\end{bmatrix}
\]

where \( q = j/2 \) when the \( j \)-th column corresponds to an even-numbered column in \( T \) and \( q = (j + 1)/2 \) otherwise. This fact permits us to state the following:

**Statement 4.1** For each \( C_i \in C(T, B) \), there is associated a set \( \alpha \) containing those \( \alpha \)'s that correspond to the columns of \( C_i \) taken from \( T \).

Because each \( \alpha \) corresponds to the gain factor of a current source from any \( be \) or \( bc \) junction, the previous statement can also be expressed as:

**Statement 4.2** For each \( C_i \in C(T, B) \), there is associated a set of junctions corresponding to the columns of \( C_i \) taken from \( T \).

This statement leads to the following:

**Statement 4.3** Each \( C_i \) has associated an equivalent subcircuit, which is the circuit resulting from connecting the original linear circuit to those \( be \) and/or \( bc \) junctions corresponding to the columns of \( C_i \) taken from \( T \).

Each \( C_i \) can be expressed as:

\[
C_i = T \Delta_{2n-1-i} + B \Delta_i
\]  \hspace{1cm} (4.11)
where $\Delta_i, \Delta_{2^n-1-i} \in C(I, \phi)$, $I$ is the unit matrix and $\phi$ the null matrix. If we consider a circuit containing four transistors, the matrices involved are $(8 \times 8)$ matrices and for instance the element $C_6$ is given by $C_6 = T\Delta_{249} + B\Delta_6$; where $\Delta_6 = \text{diag}[00\ 00\ 01\ 10]$ and $\Delta_{249} = \text{diag}[11\ 11\ 10\ 01]$.

The structure of the matrix $\Delta_i$ and its complement $\Delta_{2^n-1-i}$ allows us to introduce a binary index as help in order to recognize each of the elements in the set as well as the corresponding equivalent subcircuit. This index is defined by the elements in the diagonal matrix $\Delta_i$, as follows:

- **zero** If a column of $T$ is being taken
- **one** If a column of $B$ is being taken

This binary index can also be used to obtain a classification of the elements $C_i$, so that the set $C(T, B)$ can be subdivided in several subsets. In order to illustrate these subsets, their indices and their equivalent subcircuits, all examples will refer to a four transistor circuit.

The subsets of $C(T, B)$ are given in the following classification:

1. **Subset $E^0$ : elements containing only one zero**
   In these cases one column of $T$ and $2n - 1$ columns of $B$ are taken, e.g. $[11\ 11\ 01\ 11]$. This corresponds with a subcircuit formed by a resistive circuit and a single diode from some transistor junction, as shown in fig. 4.9(a).

2. **Subset $E^1$ : elements containing only one one**
   In these cases one column of $B$ and $2n - 1$ columns of $T$ are taken, e.g. $[00\ 00\ 00\ 01]$. These cases involve those subcircuits formed by taking all diode junctions except one, as shown in fig. 4.9(b).

3. **Subset $E^P$ : elements containing only pairs**
   In these cases one or more column-pairs from either $T$ or $B$ are taken, e.g. $[00\ 11\ 11\ 00]$. The term *column-pair* refers to two adjacent columns labeled as $k$ and $k + 1$, while $k$ is odd. These cases involve those subcircuits that are formed by taking one or more
complete transistors, as shown in fig. 4.10(a). The term complete transistor is used to indicate that a transistor is fully connected to or disconnected from the linear circuit.

4. Subset $\mathcal{E}^{P-1}$: elements containing only pairs except one

As in the previous case, with the exception of only one pair, e.g. [11 00 11 01], i.e. those subcircuits that are formed by taking one or more complete transistors and a single diode from some transistor, as shown in fig. 4.10(b). For circuits with two transistors, this subset is actually given by the subsets $\mathcal{E}^0$ and $\mathcal{E}^1$.

5. Elements containing at least one pair but not all

This subset exists only if $n > 2$, and it can be subdivided as:

(a) Subset $\mathcal{E}^{P+\text{odd}}$: elements containing at least one pair and only odd-numbered columns of $T$

In these cases at least one column-pair from either $T$ or $B$ is taken and also odd-numbered columns of $T$, e.g. [00 11 01 01]. Those subcircuits formed by at least a complete transistor and at least two base-emitter junctions, as shown in fig. 4.11(a).
Figure 4.10: \( \mathcal{E}^P \) and \( \mathcal{E}^{P-1} \) elements.

(b) Subset \( \mathcal{E}^{P+\text{even}} \) : elements containing at least one pair and only even-numbered columns of \( T \)
In these cases at least one column-pair from either \( T \) or \( B \) is taken and also even-numbered columns of \( T \), e.g. [00 11 10 10]. Those subcircuits formed by at least a complete transistor and at least two base-collector junctions, as shown in fig. 4.11(b).

(c) Subset \( \mathcal{E}^{P+\text{mix}} \) : elements containing at least one pair and mixed-numbered columns of \( T \)
In these cases at least one column-pair from either \( T \) or \( B \) is taken and also mixed-numbered columns of \( T \), for example [00 11 10 01]. Those subcircuits formed by at least a complete transistor and at least one base-collector and one base-emitter junction, as shown in fig. 4.11(c).

6. Elements containing no pairs at all
This group can be subdivided as:

(a) Subset \( \mathcal{O}^{be} \) : one element containing only odd-numbered columns of \( T \)
e.g. [01 01 01 01]. The subcircuit formed by taking only base-emitter junctions (see fig. 4.12(a)).
Figure 4.11: $\mathcal{E}^{P+odd}$, $\mathcal{E}^{P+even}$ and $\mathcal{E}^{P+mix}$ elements.

(b) Subset $\mathcal{O}^{mix}$: elements containing only mixed-numbered columns of $T$

Elements like [01 10 10 01]. Those subcircuits formed by different base-collector and base-emitter junctions, as shown in fig. 4.12(b).

(c) Subset $\mathcal{O}^{bc}$: one element containing only even-numbered columns of $T$

e.g. [10 10 10 10]. The subcircuit formed by taking only base-collector junctions (see fig. 4.12(c)).
Figure 4.12: $O^{be}$, $O^{mix}$ and $O^{bc}$ elements.

The idea behind this classification is to consider that for all $C_i$ in a subset $\in C(G,T)$ exist similar equivalent subcircuits. The various types of elements actually denote various types of subcircuits with particular properties. The next table shows a summary of the given classification,
### 4-5. SAVINGS IN THE NUMBER OF ELEMENTS TO EVALUATE

<table>
<thead>
<tr>
<th>Subset</th>
<th>Components</th>
<th>Index example</th>
</tr>
</thead>
<tbody>
<tr>
<td>$E^0$</td>
<td>Only one diode</td>
<td>11 11 10 11</td>
</tr>
<tr>
<td>$E^1$</td>
<td>$n - 1$ transistors + one diode</td>
<td>00 00 00 10</td>
</tr>
<tr>
<td>$E^P$</td>
<td>$n$ complete transistors</td>
<td>00 11 11 00</td>
</tr>
<tr>
<td>$E^{P-1}$</td>
<td>$n - 1$ complete transistors + one diode</td>
<td>00 11 01 00</td>
</tr>
<tr>
<td>$E^{P+odd}$</td>
<td>complete transistors + diodes be</td>
<td>01 00 11 01</td>
</tr>
<tr>
<td>$E^{P+even}$</td>
<td>complete transistors + diodes bc</td>
<td>10 00 11 10</td>
</tr>
<tr>
<td>$E^{P+mix}$</td>
<td>complete transistors + diodes be + diodes bc</td>
<td>10 00 11 01</td>
</tr>
<tr>
<td>$O^{be}$</td>
<td>Only diodes be</td>
<td>01 01 01 01</td>
</tr>
<tr>
<td>$O^{mix}$</td>
<td>Diodes be + Diodes bc</td>
<td>01 10 10 01</td>
</tr>
<tr>
<td>$O^{bc}$</td>
<td>Only diodes bc</td>
<td>10 10 10 10</td>
</tr>
</tbody>
</table>

where a transistor junction is here denoted as a "diode", the term "complete transistor" denotes a fully connected or disconnected transistor and the column of "Index example" shows just an example for the case of four transistors.

### 4-5 Savings in the number of elements to evaluate

The preceding classification allows us to introduce some savings in the number of elements that must be taken into account in the process of evaluation, while keeping the topological information in the binary index. It is done by observing the particular structure of the matrices $T$ (positive block diagonal matrix) and $B$, (symmetric matrix representing the admittance matrix related to the linear circuit), as well as the structure of the resulting $C_i$ matrix according to the type of element in the classification.

The terms which do not need to be evaluated are those corresponding to matrices that cannot become negative. These terms are found by applying the following theorem:

**Theorem 4.2** Given the matrices $T$ and $B$, which represent respectively the transistor relationships and the linear part of the circuit, then the
following subsets only contain positive-semidefinite matrices:

\[
\begin{align*}
\mathcal{E}^0 & \in \mathcal{C}(T, B) \\
\mathcal{E}^1 & \in \mathcal{C}(T, B) \\
\mathcal{E}^P & \in \mathcal{C}(T, B) \\
\mathcal{E}^{P-1} & \in \mathcal{C}(T, B)
\end{align*}
\]

The proof of this theorem as well as the analysis for each of the types is given in Appendix B. The above-mentioned subsets count a total of \(2^{\frac{n}{2}}(1 + \frac{n}{2})\) elements, which are distributed as follows:

<table>
<thead>
<tr>
<th>Subset</th>
<th>Elements in</th>
</tr>
</thead>
<tbody>
<tr>
<td>(\mathcal{E}^0)</td>
<td>n</td>
</tr>
<tr>
<td>(\mathcal{E}^1)</td>
<td>n</td>
</tr>
<tr>
<td>(\mathcal{E}^P)</td>
<td>(2^{\frac{n}{2}})</td>
</tr>
<tr>
<td>(\mathcal{E}^{P-1})</td>
<td>(n(2^{\frac{n}{2}}-1 - 2))</td>
</tr>
</tbody>
</table>

where \(n\) represents the order of the involved matrices, \(n = 2q\), i.e. twice the number of transistors. In this form, the elements which need to be evaluated are:

- **Elements containing at least one pair but not all**
  - Subset \(\mathcal{E}^{P+\text{odd}}\)
    
    Elements containing at least one pair and only odd-numbered columns of \(T\).
  - Subset \(\mathcal{E}^{P+\text{even}}\)
    
    Elements containing at least one pair and only even-numbered columns of \(T\).
  - Subset \(\mathcal{E}^{P+\text{mix}}\)
    
    Elements containing at least one pair and mixed-numbered columns of \(T\).

- **Elements containing no pairs at all**
  - Subset \(\mathcal{O}^{bc}\)
    
    An element containing only odd-numbered columns of \(T\).
- Subset $O^{miz}$
  Elements containing only mixed-numbered columns of $T$.
- Subset $O^{bc}$
  An element containing only even-numbered columns of $T$.

Let us consider, for instance, a circuit containing two transistors, then the terms that need to be evaluated are given by:

\[
O^{bc} = C_5 \\
O^{miz} = \begin{cases} 
  C_6 \\
  C_9 \\
O^{bc} = C_{10}
\end{cases}
\]

4-6 Most basic case: two-transistor circuits

The first case in order of complexity is related to circuits containing only two transistors. Such circuits are important from a theoretical point of view because they possess the minimum number of transistors which can allow the circuit to have multiple solutions. From a more practical point of view, they are important because a great number of useful circuits are built up with only two transistors. Besides, several large-sized circuits are usually constructed by using various one-transistor and two-transistor stages. In these cases, the cause of multiple DC operating points may be found in the occurrence of latch-up or multi-stable condition from only one two-transistor sub-circuit. This fact will become clearer in the following chapter, when the analysis of the original circuit is carried out by applying a partitioning procedure to the matrices involved, which actually means a partitioning of the circuit.

The case of two-transistor circuits has been studied in several works [2, 10–13, 22] concluding that circuits with two transistors may possess a maximum of three DC operating points. Here, this case is analyzed in order to answer several important points:

- What is the cause of multiple solutions?
- What is the relation between this cause and the elements of the set $C(T, B)$ (or $O(T, B)$)?
4-6-1 Remaining terms of $C$

Because two transistors are contained in the circuit, the matrices involved are matrices of order $n = 4$ and they are given by:

$$
T = \begin{bmatrix}
1 & -\alpha_r^{(1)} & 0 & 0 \\
-\alpha_f^{(1)} & 1 & 0 & 0 \\
0 & 0 & 1 & -\alpha_r^{(2)} \\
0 & 0 & -\alpha_f^{(2)} & 1
\end{bmatrix}
\quad B = \begin{bmatrix}
b_{11} & b_{12} & b_{13} & b_{14} \\
b_{21} & b_{22} & b_{23} & b_{24} \\
b_{31} & b_{32} & b_{33} & b_{34} \\
b_{41} & b_{42} & b_{43} & b_{44}
\end{bmatrix}
$$

The set $C(T, B)$ contains 16 elements, from which only some must be evaluated. The expansion of this set as well as the analysis of its elements are accomplished in Appendix C. Directly from this analysis, it follows that the only elements to be evaluated are:

$$
\begin{align*}
C_5 &= \begin{bmatrix}
1 & b_{12} & 0 & b_{14} \\
-\alpha_f^{(1)} & b_{22} & 0 & b_{24} \\
0 & b_{32} & 1 & b_{34} \\
0 & b_{42} & -\alpha_f^{(2)} & b_{44}
\end{bmatrix}_{0101} = \mathcal{O}^{be} \\
C_6 &= \begin{bmatrix}
1 & b_{12} & b_{13} & 0 \\
-\alpha_f^{(1)} & b_{22} & b_{23} & 0 \\
0 & b_{32} & b_{33} & -\alpha_r^{(2)} \\
0 & b_{42} & b_{43} & 1
\end{bmatrix}_{0110} \in \mathcal{O}^{mix} \\
C_9 &= \begin{bmatrix}
b_{11} & -\alpha_r^{(1)} & 0 & b_{14} \\
b_{21} & 1 & 0 & b_{24} \\
b_{31} & 0 & 1 & b_{34} \\
b_{41} & 0 & -\alpha_f^{(1)} & b_{44}
\end{bmatrix}_{1001} \in \mathcal{O}^{mix} \\
C_{10} &= \begin{bmatrix}
b_{11} & -\alpha_f^{(1)} & b_{13} & 0 \\
b_{21} & 1 & b_{23} & 0 \\
b_{31} & 0 & b_{33} & -\alpha_r^{(2)} \\
b_{41} & 0 & b_{43} & 1
\end{bmatrix}_{1010} = \mathcal{O}^{bc}
\end{align*}
$$

i.e. only those matrices formed by taking a column from a column pair of $T$ and a column from the other column pair of $B$ have to be evaluated. This fact is here illustrated by keeping the corresponding binary index for each matrix.
4-6. MOST BASIC CASE: TWO-TRANSISTOR CIRCUITS

Figure 4.13: Schematic equivalent $\mathcal{O}$ subcircuits for a two transistor circuit.

Because an equivalent subcircuit has been assigned to each $C_k \in C(T, B)$, the elements to be evaluated have the associated equivalent subcircuits shown in figure 4.13. Note that the resulting subcircuits correspond to circuits formed by taking two junctions from different transistors.

4-6-2 On the expansion of the determinants of $\mathcal{O}$

It has been demonstrated for the case of circuits containing two transistors [13] that from the terms in (4.12), only the element $\mathcal{O}^{be}$ may result in a negative determinant, provided that $\alpha_f^{(i)} > \alpha_r^{(i)}$ for $i = 1, 2$, which is a realistic assumption for most of the practical cases. It leads to the conclusion that only the equivalent subcircuit for the index 01 01 contains such a structure that causes the possibility of multiple solutions. This circuit is shown in fig. 4.14.
Additionally, [12] establishes that the uniqueness of the DC solutions cannot be guaranteed if a feedback structure is found embedded in the circuit (see figure 4.15). This structure can be found by applying some operations on the branches containing the linear elements. These operations are a combination of short circuits and/or open circuits.

![Figure 4.14: Schematic equivalent 01 01 subcircuit.](image1)

Two important results have already been established for this class of circuit:

- The result given in [13]
  
  It guarantees that only one of terms $\in C$ may become negative.

- The structure provided by [10]
4-7. CONCLUSIONS

It causes the uniqueness of the solution not to be guaranteed.

Based on the previous classification of the elements $C_i \in C(T, B)$, the previous results may be also expressed by the following:

**Statement 4.4** A circuit composed of positive linear resistors, independent sources and two transistors possesses three solutions iff $\det \mathcal{O}^{be}$ is negative, i.e. iff $\det C_{0101}$ is negative.

4-7 Conclusions

In order to solve the DC problem of circuits having multiple operating points, a formulation has been established which takes into account the topological information of the circuit. A model which separates the linear part from the nonlinear part has been used. This results in a canonical representation of the circuit in the form of a $2q$-port, where $q$ is the number of transistors. This port contains only the linear part of the circuit constituted by linear positive resistors and independent sources.

Since one of the involved matrices (actually, the derivatives matrix $D$) is a result in the DC problem, the model can be fully described by setting up two matrices, the first one related to the linear part of the circuit and a second matrix related to the part containing the transistors. From this pair of matrices a juxtaposed set is formed and the topological implications of each of the matrices in the set have been derived.

Bibliography


CHAPTER 5

Multiple solutions

5-1 Introduction

The amount of savings reported in the previous chapter means there has already been some advance in the reduction of the number of operations required in the process of solution, however the number of elements to evaluate in the \( \mathcal{O} \) subset is still \( 2^q \). This fact indicates that the evaluation of its terms will represent a formidable task even for small circuits with only a few transistors, i.e. the problem remains an NP problem.

In order to deal with this problem, an additional saving procedure will be pursued with the purpose of reducing the size of the matrices involved and thus the size of the generated subsets. This will be done by looking at the properties of the matrices involved in the current representation of the transistor circuit.

This study will lead to the determination of a particular pattern on the entries of the matrix \( G^{-1} \), which allows the implementation of a partitioning process with the will of decreasing the amount of calculations by postponing the evaluation of the concerned determinants until it becomes necessary to do.

In fact, the method described hereunder takes into account the topology of the circuit in the process of solving the problem of circuits with
multiple DC operating points. This problem involves in the first place
the determination of an upper bound on the number of possible DC so-
lutions and in second place finding out all of them. In this process, the
solution to the problem of assessing the uniqueness of the DC operating
point will also be obtained.

5-2 Similar sets

In the previous chapter, the matrices $T$ and $B$ have been used to de-
termine the topological implications of the set of juxtaposed matrices
$C(T, B)$ by associating an equivalent subcircuit to each element in the
set. The circuit is described by the equation (4.4), which is expressed
here in a slightly modified form:

$$ Tf(v) + Gv - c = 0 $$

(5.1)

where $T$ is the block diagonal matrix with the transistor current gain fac-
tors ($\alpha$'s) and $G$ is the symmetrical matrix representing the admittance
matrix from the linear part of the circuit. In addition, several equivalent
forms of this equation can be given.

Firstly, if the equation above is premultiplied by $T^{-1}$, we can obtain:

$$ I f(v) + T^{-1} Gv - \bar{c} = 0 $$

(5.2)

where $I$ represents the unitary matrix of order $2q$.

The equation (5.1) can be premultiplied by $G^{-1}$ in order to obtain:

$$ G^{-1} T f(v) + I v - \bar{c} = 0 $$

(5.3)

For each equation above, similar $C$ sets and $O$ subsets can be formed:

\begin{align*}
\text{for (5.1) } & \sim C(T, G) \text{ and } O(T, G) \\
\text{for (5.2) } & \sim C(I, T^{-1} G) \text{ and } O(I, T^{-1} G) \\
\text{for (5.3) } & \sim C(G^{-1} T, I) \text{ and } O(G^{-1} T, I)
\end{align*}

(5.4)

The savings in the number of elements to evaluate in the set formed
with the matrices $T$ and $G$ are similar for the sets indicated in the last
equation. In the following sections, it will be assumed that the sets $\mathcal{C}$ and $\mathcal{O}$ correspond to those formed by $T$ and $G$.

Additionally, the new sets have the advantage that they use the unitary matrix to generate the matrices $C_i$ and $O_i$, which results in more sparseness of the matrices in the set and thus in the possibility to carry out some extra reductions in the order of the matrices to be evaluated. In fact, the appearance of the unitary matrix means that the determinants of the matrices $C_i$ and $O_i$ are the principal minors of the other involved matrix. The next table gives a summary of these possible subsets:

<table>
<thead>
<tr>
<th>Equation</th>
<th>Set $\mathcal{C}$ or $\mathcal{O}$</th>
<th>Properties</th>
</tr>
</thead>
</table>
| $Tf(v) + Gv - \tilde{c} = 0$ | $(T, G)$ | $\circ$ Linear and nonlinear parts stay clearly separated  
$\circ$ Elements in $\mathcal{C}$ or $\mathcal{O}$ sets must be fully evaluated  
$\circ$ $T$ is a block diagonal matrix  
$\circ$ $G$ is a symmetrical matrix which actually represents an admittance matrix  
$\circ$ Besides $G$ may be partitioned into $2 \times 2$ submatrices |
| $If(v) + T^{-1}Gv - \tilde{c} = 0$ | $(I, T^{-1}G)$ | $\circ$ Linear and non-linear parts are mixed  
$\circ$ Elements in $\mathcal{C}$ or $\mathcal{O}$ sets do not need to be fully evaluated |
| $G^{-1}Tf(v) + Iv - \tilde{c} = 0$ | $(G^{-1}T, I)$ | $\circ$ Linear and non-linear parts are mixed  
$\circ$ Elements in $\mathcal{C}$ or $\mathcal{O}$ sets do not need to be fully evaluated  
$\circ$ $G^{-1}$ is a block symmetrical matrix related with the inverse of the MNA linear matrix |

The matrices $G$ and $G^{-1}$ are the most important, because they actually contain all the information about the topology in the circuit and together with the $T$ matrix will determine the possibility for a given circuit to have multiple DC operating points.
5-3 Matrix relationships

The matrix $G^{-1}$ is directly related to the MNA matrix of the linear part of the circuit. In figure 5.1 a generically connected transistor is shown. The equation describing just this part of the circuit is given by:

$$
\begin{bmatrix}
  g_{ee} & -g_{be} & -g_{ce} \\
  -g_{be} & g_{bb} & -g_{bc} \\
  -g_{ce} & -g_{bc} & g_{cc}
\end{bmatrix}
\begin{bmatrix}
  V_e \\
  V_b \\
  V_c
\end{bmatrix}
+ \begin{bmatrix}
  i_1 \\
  -i_1 - i_2 \\
  i_2
\end{bmatrix} = 0
$$

where each $g_{xx}$ represents the sum of all admittances connected to the transistor terminal labeled as $x$ and $V_x$ represents the corresponding nodal voltages.

This expression can be also given as:

$$
Y_{MNA_{lin}} V_{MNA} + \begin{bmatrix}
1 & 0 \\
-1 & -1 \\
0 & 1
\end{bmatrix} i = 0
$$

where $Y_{MNA_{lin}}$ denotes the MNA matrix of the linear part of the circuit, $V_{MNA}$ is the vector of nodal voltages and $i$ is the vector of transistor currents (emitter and collector currents). The expression above can be given as:

$$
v + \begin{bmatrix}
-1 & 0 \\
0 & 1
\end{bmatrix} Y_{MNA_{lin}}^{-1} \begin{bmatrix}
-1 \\
0 \\
1
\end{bmatrix} i = 0
$$

This final expression can be modified and given as:

$$
v + K^T Y_{MNA_{lin}}^{-1} K i = 0 \quad (5.5)
$$

where $v$ is the vector of transistor voltages (base-emitter and base-collector voltages), $K$ constitutes a $k \times l$ transformation matrix between the MNA representation and the representation actually being used, $k$ is the number of nodes and $l$ twice the number of transistors.
For the transistor in this example, $K$ is given by:

$$
K = \begin{bmatrix}
1 & 2 \\
1 & 0 \\
-1 & -1 \\
0 & 1 \\
\end{bmatrix}
\begin{bmatrix}
n_e \\
n_b \\
n_c \\
\end{bmatrix}
$$

In the expression above, the transistor terminals are denoted by the nodes $n_e$, $n_b$, and $n_c$, while the transistor junctions are denoted as branches 1 and 2. Thus, the rows and columns of the matrix $K$ are respectively associated to some nodes (terminals of the transistors) and to some branches (junctions of the transistors), i.e. the ports in the $2n$-representation. This means that $K$ constitutes a submatrix of the node-branch incidence matrix $A$ related to the topology of the circuit$^1$.

The equation just obtained has the same structure as the equation (5.2), so that:

$$
G^{-1} = K^T Y_{MNA_{in}}^{-1} K
$$

This matrix can be seen as an impedance matrix of the representation here used.

In addition, the matrix $K$ can easily be found, because it relates both voltage vectors from the MNA and the current representations:

$$
v = K^T V_{MNA}
$$

In general, all elements of the transformation matrix are $+1$, $-1$, or 0. It has also a column-pair-like structure. Each column pair has a $-1$ at the row corresponding to the base of the transistor related to that column-pair, while the first column of the column-pair has a $+1$ at the row corresponding to the emitter and the second column has a $+1$ at the row corresponding to the collector. $K$ is thus an unimodular matrix.

In summary, several matrices are involved, beginning by the nodal analysis matrix from the linear part of the circuit and finally the impedance

$^1$This matrix $A$ must not be confused with the matrix $A$ in equation 4.4. Here it denotes the node-branch incidence matrix from the ABCDs of network topology. Hereafter, in order to refer to this last matrix, the complete term "node-branch incidence $A$ matrix" or $A_i$ will be used.
matrix of the $2n$-representation. Several properties of these matrices are presented in the following.

The matrix of the linear part of the circuit: $Y_{MNA_{lin}}$

The linear part of the MNA matrix represents the admittance matrix of a purely passive circuit and is given also as the following triple product:

$$Y_{MNA_{lin}} = A_i Y A_i^t$$

where $Y \in \mathbb{R}^{b \times b}$ represents a diagonal matrix from the linear components, $b$ being the number of branches. Because of the fact that the linear part of the circuit contains positive linear resistors and independent current and voltage sources, this matrix possesses only non-negative elements.

The entries of the matrix $Y_{MNA_{lin}}$ are denoted as $y_{ij}$ and they represent:

$$y_{ij} = \begin{cases} \sum & \text{all admittances connected} \\
& \text{to node } i \text{ when } j = i \\
& \sum & \text{all admittances connected} \\
& & \text{between nodes } i \text{ and } j \text{ when } j \neq i \\
\end{cases}$$

This concept is graphically depicted in figure 5.2

The $Y_{MNA_{lin}}$ matrix is a special class of the paramount matrix [1]. An $n$th-order real symmetrical matrix is defined as a paramount matrix if each principal minor of order $r$ is not less than the absolute value of any $r$th-order minor built from the same rows (or columns), where $r = 1, 2, \cdots, n - 1$. Because $Y_{MNA_{lin}}$ describes only the linear part of the circuit, it may occur that some entries at the main diagonal are zero (i.e. nodes at which no linear element is connected), however, the rest of entries in the corresponding row (and column) also have a zero value, so that $Y_{MNA_{lin}}$ remains paramount. In this way, the matrix $Y_{MNA_{lin}}$ is at least positive semidefinite.
The inverse of $Y_{MNA_{lin}}$.

The second matrix involved is the inverse of the matrix of the linear part of the circuit, denoted as $Y_{MNA_{lin}}^{-1}$. Because $Y_{MNA_{lin}}$ is related to a passive circuit, the entries of $Y_{MNA_{lin}}^{-1}$ represent resistive elements and are denoted as $z_{ij}$. The elements lying on the main diagonal can be seen as the following equivalent resistor:

$$z_{ii} = \text{Equivalent resistance connected from node } i \text{ to datum}$$

The resistance $z_{ii}$ can be decomposed as a sum of terms, which means that the resistance related to the node $i$ can be modeled by a series of resistors connected from node $i$ to datum. Because this representation constitutes only a model for the element $z_{ii}$, the interconnection points between the resistors in the model do not represent nodes in the original circuit. Thus, according to this model, the elements $z_{ii}, z_{jj}$ and $z_{ij}$ are given by:

$$z_{ii} = \text{Series equivalent of resistances connected from node } i \text{ to datum}$$

$$z_{jj} = \text{Series equivalent of resistances connected from node } j \text{ to datum}$$

$$z_{ij} = \sum \text{common series resistances } \in z_{ii} \text{ and } z_{jj} = z_{ji}$$
In figure 5.3(a), the element $z_{ii}$ (resp. $z_{jj}$) is represented by a single resistor connected from node $i$ (resp. node $j$) to datum. The element $z_{ij}$ is represented in this figure as the intersection between $z_{ii}$ and $z_{jj}$. The models used to represent these resistor elements are given in figure 5.3(b), where the model of the element $z_{ii}$ (resp. $z_{jj}$) is given by the series equivalent resistor from node $i$ (resp. node $j$) to datum. The element $z_{ij}$ (identical to $z_{ji}$) is given by the intersection of both series equivalents.

**Example 1:**

In order to illustrate these concepts, a first example is presented in figure 5.4, where a combination of series resistors is connected from both nodes $i$ and $j$ to datum. Besides, the paths from both nodes to datum are formed by single trajectories passing through a common set of series resistors; i.e. actually the set of series resistors in $z_{jj}$ is a subset of $z_{ii}$. Obviously, this example illustrates the simplest case.

**Example 2:**

A second example is presented in figure 5.5(a), where a combination of series-parallel resistors is connected from both nodes $i$ and $j$ to datum. The paths from both nodes to datum are formed by trajectories consisting of more than one branch and they have a common branch (in this case given for the resistor $R_2$). The corresponding common resistance must be found with the aid of the series-resistance equivalent model as shown in figure 5.5(b), where the terms $z_{ii}$ and $z_{jj}$ are represented by series equivalents and the resulting $z_{ij}$ is the common set.
5-4. $G^{-1}$: THE KEY OF PARTITIONING

![Diagram](a) and (b)

Figure 5.5: Example 2 of $(z_{ii}, z_{ij}, z_{jj})$.

Because the series equivalent common to a pair of nodes cannot be greater than the equivalent series from any of the nodes, it clearly results:

$$0 \leq z_{lk} \leq \max (z_{ll}, z_{kk})$$

so that the matrix $Y^{-1}_{MNA_{in}}$ remains paramount and thus at least positive semidefinite.

5-4. $G^{-1}$: the key of partitioning

Equation (5.6) represents a congruency transformation on the symmetrical matrix $Y^{-1}_{MNA_{in}}$. This transformation involves not only both matrices but also the variables from both representations (the MNA representation and the representation here being used). Because of this congruency relationship, two important properties for the matrix $G^{-1}$ can be assessed:

- the non-zero valued eigenvalues of $Y^{-1}_{MNA_{in}}$ and $G^{-1}$ are the same

- $G^{-1}$ and $G$ are also paramount

Because of the fact that $K$ is an unimodular matrix, the congruency transformation expressed in equation (5.6) yields:

$$r_{ij} = \sum_{l=1}^{n} k_{jl} \left( \sum_{m=1}^{n} k_{im} z_{ml} \right) \quad i, j = 1, 2, \cdots, 2q.$$
where: $q$ is the number of transistors, $r_{ij} \in G^{-1}$, $z_{ml} \in Y_{MN_A_{in}}^{-1}$ and $k_{ij}$ and $k_{ml} \in K$ may be $+1$, $-1$, or $0$.

In addition, the matrix $G^{-1}$ possesses also a block symmetrical structure, with $2 \times 2$ blocks on the main diagonal denoted by $r_{qq}$ corresponding to the $q$th transistor and $2 \times 2$ blocks outside the main diagonal denoted by $r_{st}$. 
5-4. $G^{-1}$: THE KEY OF PARTITIONING

5-4-1 Blocks in the main diagonal

Each $r_{qq}$ is related to one transistor and thus with a triad of nodes (for a given transistor $Q_q$, namely the terminals: $e_q$, $b_q$ and $c_q$). Figure 5.6 shows a transistor and the corresponding elements of the matrix $Y_{MNA_{tin}}^{-1}$ associated to each transistor node. Each block matrix in the main diagonal of $G^{-1}$ constitutes a submatrix generated by a triple product of the form:

$$
\begin{bmatrix}
1 & -1 & 0 & \cdots \\
0 & -1 & 1 & \cdots \\
\vdots & \vdots & \vdots & \ddots \\
\end{bmatrix}
\begin{bmatrix}
z_{e_q,e_q} & z_{e_q,b_q} & z_{e_q,c_q} \\
z_{b_q,e_q} & z_{b_q,b_q} & z_{b_q,c_q} \\
z_{c_q,e_q} & z_{c_q,b_q} & z_{c_q,c_q} \\
\end{bmatrix}
\begin{bmatrix}
1 & 0 & \cdots \\
-1 & -1 & \cdots \\
0 & 1 & \cdots \\
\vdots & \vdots & \ddots \\
\end{bmatrix}
$$

Thus, a block in the main diagonal is given by:

$$
r_{qq} = \begin{bmatrix}
(z_{b_q,b_q} - z_{b_q,e_q} - z_{b_q,c_q} + z_{e_q,e_q}) & (z_{b_q,b_q} - z_{b_q,e_q} - z_{b_q,c_q} + z_{e_q,e_q}) \\
(z_{b_q,b_q} - z_{b_q,e_q} - z_{b_q,c_q} + z_{c_q,e_q}) & (z_{b_q,b_q} - z_{b_q,e_q} - z_{b_q,c_q} + z_{c_q,c_q})
\end{bmatrix}
$$

where $z_{e_q,e_q}$, $z_{b_q,b_q}$ and $z_{c_q,c_q}$ are the equivalent resistances seen from the terminals of the transistor to datum and, $z_{x_q,y_q}$ represents the common terms between the equivalent resistances $z_{x_q,x_q}$ and $z_{y_q,y_q}$.

The elements on the main diagonal of the matrix above are actually the resistors in the loops formed by the corresponding junctions and the paths from the transistor terminals to datum. In the figure 5.6, these loops are labeled as the ellipses $l_{beq}$ and $l_{bce}$. The elements outside the diagonal (elements $r_{qq(12)}$ and $r_{qq(21)}$) are the common resistance to both loops.

This permits to establish a first result about the properties of the matrix $R$.

**Theorem 5.1** The $2 \times 2$ blocks located on the main diagonal of the matrix $R = G^{-1}$ are at least positive definite matrices and can be denoted by:

$$
r_{qq} = \begin{bmatrix}
z_{l_{beq}} & z_{l_{beq}} \\
z_{l_{beq}} & z_{l_{beq}} \\
\end{bmatrix}
$$
where the term $z_{t_{beq}}$ (resp. $z_{t_{bcq}}$) represents a set with the equivalent series resistors in the loop BE (resp. BC) and the symbol $\cap$ is used to denote the intersection of a pair of sets.

This concept is graphically depicted in figure 5.7, where each transistor junction has assigned a circle representing the set of resistors in the corresponding loop.

By letting $\mathcal{Z}_{beq} = z_{t_{beq}}$, $\mathcal{Z}_{bcq} = z_{t_{bcq}}$ and $\mathcal{Z}_{beq}^{bcq} = \mathcal{Z}_{bcq}^{beq} = z_{t_{beq}} \cap z_{t_{bcq}}$; it is possible to express this matrix as:

$$\tau_{qq} = \begin{bmatrix} \mathcal{Z}_{beq} & \mathcal{Z}_{bcq}^{beq} \\ \mathcal{Z}_{beq}^{bcq} & \mathcal{Z}_{bcq} \end{bmatrix}$$

(5.8)

5-4-2 Blocks off the main diagonal

In addition to what has been found in the previous part, it must be noted that each block $\tau_{st}$ is related to two transistors denoted as $Q_s$ and $Q_t$ and obviously also related to two triads of terminals. Thus, this matrix
Figure 5.8: Elements of a $2 \times 2$ block associating transistors $Q_s$ and $Q_t$.

is given by:

$$
\mathbf{r}_{st} = \begin{bmatrix}
\left( z_{bs,b_t} - z_{bs,e_s} - z_{bs,e_t} + z_{e_s,e_t} \right) & \left( z_{bs,b_t} - z_{bs,e_s} - z_{bs,c_t} + z_{c_t,e_s} \right) \\
\left( z_{bs,b_t} - z_{bs,e_t} - z_{bs,c_t} + z_{c_t,e_t} \right) & \left( z_{bs,b_t} - z_{bs,c_t} - z_{bs,c_t} + z_{c_t,c_t} \right)
\end{bmatrix}
$$

Now two transistors are involved, so that $z_{x_s,y_t}$ stands for "the element in $Y_{MNA}^{-1}$ at the entry $(x_s, y_t)$ corresponding to the $x$ terminal of transistor $s$ and $y$ terminal of transistor $t" which indicates that the element $z_{x_s,y_t}$ is the intersection of two sets containing the series resistors used to model the resistance seen between datum and the terminals $x_s$ and $y_t$. Because every transistor has associated a pair of loops, one expects that each $2 \times 2$ block outside the main diagonal has now associated four loops. This fact provides a main result for these blocks:

**Theorem 5.2** The $2 \times 2$ blocks located outside the main diagonal of the matrix $\mathbf{R} = G^{-1}$ are denoted by:
where the terms $z_{bc[e][c]}$ \textit{(resp.} $z_{be[e][c]}$ \textit{)} represent a set with the equivalent series resistors in the loop \textit{BE (resp.} \textit{BC) from the transistor s (or t), i.e. the blocks out off the diagonal represent indeed the degree of "connectivity" between transistors $Q_s$ and $Q_t$.

This matrix is expressed as:

\[
\mathbf{r}_{st} = \begin{bmatrix}
    z_{be[e]} & z_{be[c]} \\
    z_{bc[e]} & z_{bc[c]}
\end{bmatrix}
\]

However, the definiteness of this submatrix cannot be predicted and the signs of the elements in it are determined by means of the orientation of the loop currents in the common terms. For instance if the current of the BE loop of transistor $Q_s$ has the same direction as the BE loop of transistor $Q_t$ in the common resistance between both loops, then the element $r_{st(11)}$ in the matrix above has positive sign. The same criteria is used for determining the sign of all other elements of $\mathbf{r}_{st}$. Figure 5.8 shows schematically this fact; the circles represent the set of resistors related to each transistor junction loop, while the shadowed sectors are the intersections between them.

In summary, the $q$-th column-pair of the matrix $\mathbf{G}^{-1}$ (i.e. the pair
related to the $q$th transistor) has the following structure:

$$q\text{-th column-pair of } G^{-1} = $$

$$
\begin{bmatrix}
(z_{b_1,b_q} - z_{b_q,c_1} - z_{b_1,e_q} + z_{c_1,e_q}) & (z_{b_1,b_q} - z_{b_q,c_1} - z_{b_1,c_q} + z_{c_q,e_1}) \\
(z_{b_1,b_q} - z_{b_1,e_q} - z_{b_q,c_1} + z_{c_1,e_q}) & (z_{b_1,b_q} - z_{b_q,c_1} - z_{b_1,c_q} + z_{c_1,c_q}) \\
\vdots & \vdots \\
(z_{b_q,b_q} - z_{b_q,e_q} - z_{b_q,c_q} + z_{c_q,e_q}) & (z_{b_q,b_q} - z_{b_q,e_q} - z_{b_q,c_q} + z_{c_q,c_q}) \\
(z_{b_q,b_q} - z_{b_q,c_q} - z_{b_q,c_q} + z_{c_q,e_q}) & (z_{b_q,b_q} - z_{b_q,c_q} - z_{b_q,c_q} + z_{c_q,c_q}) \\
\vdots & \vdots \\
(z_{b_t,b_q} - z_{b_q,e_t} - z_{b_t,e_q} + z_{e_t,e_q}) & (z_{b_t,b_q} - z_{b_q,e_t} - z_{b_t,c_q} + z_{c_q,e_t}) \\
(z_{b_t,b_q} - z_{b_t,e_q} - z_{b_q,c_t} + z_{c_t,e_q}) & (z_{b_t,b_q} - z_{b_q,c_t} - z_{b_t,e_q} + z_{c_t,c_q}) \\
\vdots & \vdots
\end{bmatrix}
$$

By using the loops $be$ and $bc$, the column-pair above may be expressed also as:

$$q\text{-th column-pair} = $$

$$
\begin{bmatrix}
[z_{b_{be_1}} \nabla z_{b_{beq}}] & [z_{b_{be_1}} \nabla z_{b_{becq}}] \\
[z_{b_{bc_1}} \nabla z_{b_{beq}}] & [z_{b_{bc_1}} \nabla z_{b_{becq}}] \\
\vdots & \vdots \\
[z_{b_{beq}} \nabla z_{b_{beq}}] & [z_{b_{beq}} \nabla z_{b_{becq}}] \\
[z_{b_{becq}} \nabla z_{b_{beq}}] & [z_{b_{becq}} \nabla z_{b_{becq}}] \\
\vdots & \vdots
\end{bmatrix} =
\begin{bmatrix}
Z_{b_{beq}} & Z_{b_{beq}} \\
Z_{b_{beq}} & Z_{b_{beq}} \\
\vdots & \vdots \\
Z_{b_{beq}} & Z_{b_{beq}} \\
Z_{b_{beq}} & Z_{b_{beq}} \\
\vdots & \vdots
\end{bmatrix}
$$
In this way, a general $G^{-1}$ matrix may be given as:

$$G^{-1} = \begin{bmatrix}
Z_{be1} & Z_{be1} & Z_{be2} & Z_{be2} & Z_{be3} & Z_{be3} & \cdots \\
Z_{be1} & Z_{be1} & Z_{be2} & Z_{be2} & Z_{be3} & Z_{be3} & \cdots \\
Z_{be2} & Z_{be2} & Z_{be2} & Z_{be2} & Z_{be3} & Z_{be3} & \cdots \\
Z_{be3} & Z_{be3} & Z_{be3} & Z_{be3} & Z_{be3} & Z_{be3} & \cdots \\
\cdots & \cdots & \cdots & \cdots & \cdots & \cdots & \cdots
\end{bmatrix} \quad (5.10)$$

Figure 5.9 shows the construction of the $G^{-1}$ matrix for the case of three transistors. In this figure each transistor has associated two loops (one for each junction), they are labeled with subscripts of the form $ii$. There is an intersected loop area for each pair of loops from a certain transistor denoted by subscripts $i, i+1$ and $i+1, i$; they represent actually the common impedance in the loops BE and BC of the transistor. These terms are the elements of each $2 \times 2$ block $r_{ii}$. This structure has the property that the block elements out off the main diagonal are transpose, i.e. $r_{ij} = r_{ji}^T$, which leads to $\det r_{ij} = \det r_{ji}$. The blocks outside the main diagonal are here denoted by the shadowed ellipses representing the intersection of the two loops incident to it.

Figure 5.9: Matrix structure for a three transistors case.
5-5 Partitioning process

The matrices $r_{st}$ reveal important characteristics, because the elements in these matrices are impedance elements common to the loops in two transistors. In other words stated: the blocks outside the main diagonal are related with the interconnection of the transistors. From this point of view, an important case occurs when at least one junction is disconnected between both transistors. Several possibilities arise:

$$r_{st} = \begin{cases} 
\begin{bmatrix} 0 & 0 \\ x & x \end{bmatrix} & \ell_{be_t} \text{ is disconnected from transistor } t \\
\begin{bmatrix} x & x \\ 0 & 0 \end{bmatrix} & \ell_{bc_t} \text{ is disconnected from transistor } t \\
\begin{bmatrix} 0 & x \\ 0 & x \end{bmatrix} & \ell_{be_s} \text{ is disconnected from transistor } s \\
\begin{bmatrix} x & 0 \\ x & 0 \end{bmatrix} & \ell_{bc_s} \text{ is disconnected from transistor } s \\
\begin{bmatrix} 0 & 0 \\ 0 & 0 \end{bmatrix} & \text{There is no connection between both transistors}
\end{cases}$$

where "x" denotes a non-zero entry.

Any of the cases above implies that there is not a full connection between the loops of two transistors, which means that no feedback structure may be formed by these transistors. A block of this type is called a disconnection block. Figure 5.10(a–e) schematically shows each one of these cases. Because of the property that $r_{st} = r_{ts}^T$, the same conclusions may be obtained by considering $r_{ts}$.

The existence of the disconnection blocks allows to carry out a partitioning procedure based on the fact that a disconnection block $r_{st}$ implies the non-existence of a feedback structure between both transistors $Q_s$ and $Q_t$. 
Figure 5.10: Disconnection blocks.

Some of the $2 \times 2$ blocks in certain column-pair (row-pair$^2$) may constitute disconnection blocks. If all blocks $r_{st}$ for a certain column-pair (or row-pair) $s$ and for $t \neq s$ constitute disconnection blocks, then the $s$th transistor may be considered as not taking part of any feedback structure and, thus, it can be separated from the rest of the circuit.

$^2$The term row-pair is here used to denote a pair of rows corresponding to a particular transistor, it clearly results that each row-pair is a $1 \times q$ composed vector in which the elements are $2 \times 2$ matrices.
In this case the $s$-th column of $G^{-1}$ has the form:

$$\begin{bmatrix}
\tilde{r}_{1,s} \\
\tilde{r}_{2,s} \\
\vdots \\
r_{h,s} \\
\vdots \\
r_{ss} \\
\vdots \\
r_{q,s}
\end{bmatrix}$$

where each $\tilde{r}_{s,t}$ represents a disconnection block.

For a set of column-pairs, some of those blocks may be common, i.e. the whole matrix has a portion defined by a row-pair and the set of column-pairs, which delimits a partitioning on the original matrix. In this case a reordering of the matrix may be carried out in order to obtain the following general structure:

$$G^{-1} \triangleq \begin{bmatrix}
R_{aa} & \tilde{R}_{ab} \\
\tilde{R}_{ba} & R_{bb}
\end{bmatrix}$$

where $\tilde{R}_{ab} = \tilde{R}_{ba}^T$ represents the disconnected block between two sets of transistors. It means that partitioning may be applied and two new submatrices of smaller order are generated, namely $R_{aa}$ ($a \times a$ order) and $R_{bb}$ ($b \times b$ order) with $a + b = 2q$. The partitioning process can be now applied to each of the subsequent matrices.

The same process can be applied to the matrix $T$, which is straightforward, since $T$ has a block diagonal structure. In this way, two submatrices can be formed, namely $T_{aa}$ and $T_{bb}$:

$$T \triangleq \begin{bmatrix}
T_{aa} & 0 \\
0 & T_{bb}
\end{bmatrix}$$

In a posterior step, the main aim is to form juxtaposed sets of matrices with lower order, for instance:

$$C\left(T_{aa}, R_{aa}^{-1}\right) \quad C\left(T_{bb}, R_{bb}^{-1}\right)$$
A special structure:

A very common structure occurs when two (or more) transistors are connected in parallel (fig. 5.11(a)). It becomes obvious that the impedance loops related to all transistors are identical. In figure 5.11(b) the blocks denoted by (ss,tt,uu) correspond to the $2 \times 2$ blocks for the transistors connected in parallel. The blocks outside the diagonal (st,su,tu and their corresponding transposes) are related to the $2 \times 2$ interconnection blocks between those transistors. Because of the fact that they are connected to the same impedance loops, the following statement can be obtained:

**Statement 5.1** If a set of transistors $(Q_i, Q_j, \ldots, Q_k)$ are connected in parallel, then all $2 \times 2$ sub-blocks $r_{mn}$ are identical for $m$ and $n$ equal to $i, j, \ldots, k$.

The blocks denoting the interconnection between any of the transistors in parallel with another transistor in the circuit are also identical, which allows to conclude that the set $(Q_i, Q_j, \ldots, Q_k)$ can be represented by a single transistor, for instance $Q_i$; i.e. the column-pairs and row-pairs of the other transistors in the parallel structure can be deleted, thus reducing the order of the matrices involved.

This method used here does not actually constitute a partitioning procedure, but it also serves to reduce the order of the matrices and thus
it makes sense to us it when constructing smaller subsets. Finally, when a feedback structure is found and it contains one of the transistors in parallel, then all transistors in parallel are considered to be included in the feedback structure.

5-5-1 Savings obtained by partitioning.

In the previous chapter, it was found that the number of elements to be evaluated in the $O$ subset is still $2^q$. This fact makes desirable to find a procedure in order to achieve possible additional savings in the number of calculations.

A partitioning process will be pursued with the purpose of reducing the size of the matrices involved and thus the size of the generated subsets. This means that the number of subsets will be increased, but the matrices in each subset will be of smaller sizes. In this way, instead of evaluating $2^q$ elements from $O(T, G)$, two new subsets will be formed for the submatrices obtained after partitioning. These subsets will be denoted as $O_a(T_{aa}, G_{aa})$ and $O_b(T_{bb}, G_{bb})$. If it is assumed that a subset involves $k$ column-pairs ($k$ transistors), then the second subset involves $q - k$ columns-pairs. In consequence, the number of elements to be evaluated is given by:

$$2^k + 2^{q-k} = 2^{\frac{q}{2}} \left[ 2^{\frac{q}{2} - k} + \frac{1}{2^{\frac{q}{2} - k}} \right]$$

for $1 \leq k \leq q - 1$

which leads to a smaller number of calculations than for the original subset.

This partitioning procedure produces an important number of savings, even in the case when only one column-pair has been separated, because at this point the number of evaluations is $2^{q-1} + 2$. However, because the only column-pair involves a $2 \times 2$ matrix, the number of evaluations is actually $2^{q-1}$, which represents a saving of 50% in the number of elements to be evaluated from the original $O$ subset.

The largest saving takes place when exactly each partition contains half of the columns-pairs (for $q$ even). In this case, the number of

---

3For $q$ odd, the maximum saving occurs when a partition results in a submatrix containing $\frac{2q+1}{2}$ columns-pairs and the other \frac{2q-1}{2}
evaluations is \(2 \times 2^{q/2}\), which already represents a formidable amount of savings in the number of elements to evaluate and in addition, the order of the matrices to be evaluated is halved.

For \(q\) odd, the number of evaluations is given by \(3 \times 2^{(q-1)/2}\).

The purpose is to attempt to apply this partitioning process for each subsequently generated pair of submatrices. If this is successful, then more savings in the number of calculations are achieved. Figure 5.12 shows schematically this process.

In summary, the partitioning procedure is closely related to the structure of the matrices involved in the circuit description, namely \(T\) and \(R\). This means that the procedure is strongly related to the topology of the circuit, which allows us to establish the generation of subcircuits associated to each of the achieved partitionings.

Figure 5.13 represents an example of partitioning for a case with 10 transistors, the dashed submatrices represent actually the submatrices formed by disconnection blocks appearing at each level of partitioning. The number of evaluations after the third level is reduced from \(2^{10}\) to 22. This number (for this example) is actually 20, because one of the matrices obtained during the process of partitioning results in a matrix of order \(2 \times 2\), which never can contain negative elements.

The figure 5.14 shows the number of evaluations for each level of partitioning. The aim is to carry out the partitioning procedure until the dimension of the generated matrices is \(4 \times 4\), because such a matrix represents the smallest structure (with two transistors) with possibly multiple DC operating points.
5-5. PARTITIONING PROCESS

Figure 5.13: Example of partitioning process for a case with 10 transistors

Total of evaluations = $2^2 + 2^3 + 2^4 + 2^5 + 2^6 = 22$
5-6 Solving the DC problem

In order to solve the general DC problem, the following three points must be determined:

- The uniqueness of the DC solution.
- If the uniqueness is not guaranteed, then determine the upper bound on the number of multiple solutions.
- Find the set of DC solutions.

The first point has been theoretically solved by the works cited in the previous chapters. However, the implementation of the methods there described involves a large number of calculations.

By using the partitioning procedure, it is possible to search for the existence of negative elements in the juxtaposed set of (sub)matrices. The uniqueness of the DC operating point is thus assessed by the following:

**Theorem 5.3** A circuit containing transistors, positive linear resistors and independent sources is defined by a pair of matrices $T$ and $R$. Then it possesses more than one operating point iff at least one of the elements in the juxtaposed set of matrices $O_{aa}$ or $O_{bb}$ is negative. The juxtaposed sets may correspond to any of the sets in

$$
\begin{align*}
O(T, R^{-1}) \\
O(I, T^{-1}R^{-1}) \\
O(RT, I)
\end{align*}
$$

(5.11)

<table>
<thead>
<tr>
<th>Level</th>
<th>number of evaluations</th>
</tr>
</thead>
<tbody>
<tr>
<td>0 (original size)</td>
<td>$2^{10} = 1024$</td>
</tr>
<tr>
<td>1</td>
<td>$2^6 + 2^4 = 80$</td>
</tr>
<tr>
<td>2</td>
<td>$2^5 + 2^1 + 2^2 + 2^2 = 42 \sim 40$</td>
</tr>
<tr>
<td>3</td>
<td>$2^3 + 2^2 + 2^1 + 2^2 + 2^2 = 22 \sim 20$</td>
</tr>
</tbody>
</table>

Figure 5.14: Number of evaluations vs level
The problem of the number of solutions and the finding of the solutions will be discussed in the following sections.

5-7 On the number of solutions

The maximum number of solutions is determined after the partitioning process has been tried. Several cases occur depending firstly on whether the partitioning process has been successful and secondly on the number of transistors involved in the generated submatrices of lower order.

5-7-1 CASE 1: After applying partitioning process

Each time the partitioning process is carried out, a pair of matrices is obtained. After the last level of the partitioning procedure has been applied, a total of \( p \) submatrices of the type \( R_{aa} \) or \( R_{bb} \) can be separated in order to accomplish the analysis of the respective juxtaposed set \( \mathcal{O}(T, G) \).

In a second phase of the process, the occurrence of negative terms in these sets must be investigated, in order to find the matrices involved in feedback structures and to assess the uniqueness of the DC operating point by applying the previous theorem. Besides, this step also allows us to identify the transistors taking part in each one of the subcircuits constituting feedback structures. The number of matrices with negative terms is denoted by \( f \). Figure 5.15 shows schematically this procedure.

After the negative submatrices have been obtained, the number of solutions must be determined, firstly for each negative submatrix (i.e. for each subcircuit) and secondly for the whole circuit. For each negative submatrix a number of solutions \( n_i \) is assessed, then the number of solutions \( N_{sol} \) of the whole circuit is given by:

\[
N_{sol} = \prod_{i=1}^{f} n_i \quad (5.12)
\]

Several cases arise according to the order of the involved matrices.
CASE 1a: Feedback structures formed by two transistors

Here the matrices involved in the subset $O$ are of dimension $4 \times 4$ and some of them are negative. This fact indicates that two transistors are involved in the feedback structure.

In this case a subset has negative $O^{be}$ terms and the number of DC operating points is less than or equal to 3.

In fact, the occurrence of a negative $O^{be}$ indicates the existence of three solutions, because just two transistors are involved. A truth table can be introduced in order to assign different binary states to each solution:

<table>
<thead>
<tr>
<th>Solution</th>
<th>Binary state</th>
<th>stability</th>
</tr>
</thead>
<tbody>
<tr>
<td>$S_1$</td>
<td>0 1</td>
<td>stable</td>
</tr>
<tr>
<td>$S_2$</td>
<td>1 0</td>
<td>stable</td>
</tr>
<tr>
<td>$S_3$</td>
<td>1 1</td>
<td>unstable</td>
</tr>
</tbody>
</table>

For such a feedback structure, two stable and one unstable solutions occur. For a particular case, for instance a flip-flop circuit, solution
number 1 corresponds to the situation when the transistor placed on the right "wins" over the transistor placed on the left. The second solution corresponds to the inverse case. The third solution occurs when both transistors are in balance. The table above is indeed in accordance with the truth table of an SR flip-flop.

The following statement can be made:

**Statement 5.2** If the order of all negative submatrices is $4 \times 4$, then each subset has negative $O^b_e$ terms and the number of DC operating points is less than or equal to $3^f$, $f$ being the number of subsets having negative terms.

**CASE 1b: Feedback structures formed by more than two transistors**

The aim of the partitioning process is to achieve additional savings in the number of elements to be evaluated by reducing the original size of the matrices involved. The application of the partitioning procedure has optimal results when the obtained submatrices are of dimension $4 \times 4$ — which leads us to consider the previous case. However, there are other cases where the matrices with negative terms are of dimensions $> 4$, which means that more than two transistors are involved in the feedback structure.

**Structures with three transistors:**

The first case in order of importance is, of course, when three transistors are involved. The following classification gives a brief overview of this case:

1. It may be that at least one of the transistors in the structure is a *composed transistor*, like:
   - Transistors in parallel.
   - Transistors in Darlington structure.

2. Nontypical structures.
In the first case, because each composed transistor behaves as a normal transistor, the number of solutions is given by the same way as in the previous case; i.e. $3^f$. The binary states are given in a similar form.

The second case occurs when each transistor can get any of the binary states independently of the rest, which means that all possible combinations of binary states may occur. In this case, a complete analysis of this subset $O_i$ must be done. This case is actually similar to case 2, but is here applied to a subcircuit.

### 5-7-2 CASE 2: Partitioning process fails

There is a last case, when the partitioning process is not able to reduce the order of the matrices. In this case a complete analysis of the juxtaposed subset, must be carried out in order to search the binary states of the solutions.

### 5-8 On the stability of the solutions

Each time that a feedback structure has been recognized, the existence of a maximum of three solutions can be assessed. The solutions have a typical flip-flop-like logical behavior. Then a logical state can be assigned to each solution according to the following considerations:

- Two stable solutions are present, having respectively the binary states $0 \ 1$ and $1 \ 0$

- One unstable solution occurs and has the binary state $1 \ 1$

- The stability can be determined by using the following table:

<table>
<thead>
<tr>
<th>Solution</th>
<th>Binary state</th>
<th>Stability state</th>
</tr>
</thead>
<tbody>
<tr>
<td>$S_1$</td>
<td>0 1</td>
<td>0 \cdot 1 = 1</td>
</tr>
<tr>
<td>$S_2$</td>
<td>1 0</td>
<td>1 \cdot 0 = 1</td>
</tr>
<tr>
<td>$S_3$</td>
<td>1 1</td>
<td>1 \cdot 1 = 0</td>
</tr>
</tbody>
</table>
When two or more feedback structures are involved, the stability state of a particular solution can be given in terms of the stability states of the solutions from each feedback structure:

<table>
<thead>
<tr>
<th>Stability state for solution ( S_1 )</th>
<th>Stability state for solution ( S_2 )</th>
<th>Stability states for solution ( S_{12} )</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>1</td>
</tr>
</tbody>
</table>

5-8-1 Stability criterion

In order to determine the stability of a found solution, the eigenvalues of the matrix \( RT_q D + I \) must be found, and if any of them is not negative, then the solution is stable. This is more exact than just calculating the \( \det [RT_q D + I] \), because if two eigenvalues result to be negative, still their product stays positive, which leads to the erroneous conclusion that an unstable solution is stable.

Example:

In order to illustrate the occurrence of solutions due to more than one feedback structure and the stability states for all of the solutions, this example assumes that two feedback structures have been found. They are denoted as \( F_1 \) and \( F_2 \). For each structure three solutions may appear, and thus three different binary states can be assigned in accordance with the table above.

For the total circuit, the number of solutions is given by the combination of solutions from both independent feedback structures. In this case, two feedback structures are assumed, so that one by one the solutions in \( F_1 \) must be combined with each solution in \( F_2 \), which provides a total of nine possible solutions. Figure 5.16 shows two planes containing the solutions corresponding to \( F_1 \) and \( F_2 \). These two planes of solutions may be considered independent of each other, because not only do they possess independent variables but they also involve independent parts of the circuit. Another plane may be conceptualized having the solutions of the whole circuit as a combination of the two sets of solutions from each structure. On this plane the solutions of the whole circuit lie as a
Figure 5.16: Two feedback solutions
set of nine points. The binary states of the solutions are thus a result of
the combination of the binary states of the solutions in $\mathcal{F}_1$ and $\mathcal{F}_2$. The
following table shows the equivalent truth table for this example where
the solutions are expressed as $S_{ij}$.

<table>
<thead>
<tr>
<th>Solution</th>
<th>Binary state</th>
<th>stability</th>
</tr>
</thead>
<tbody>
<tr>
<td>$S_{11}$</td>
<td>0 1 0 1</td>
<td>stable</td>
</tr>
<tr>
<td>$S_{12}$</td>
<td>0 1 1 0</td>
<td>stable</td>
</tr>
<tr>
<td>$S_{13}$</td>
<td>0 1 1 1</td>
<td>unstable</td>
</tr>
<tr>
<td>$S_{21}$</td>
<td>1 0 0 1</td>
<td>stable</td>
</tr>
<tr>
<td>$S_{22}$</td>
<td>1 0 1 0</td>
<td>stable</td>
</tr>
<tr>
<td>$S_{23}$</td>
<td>1 0 1 1</td>
<td>unstable</td>
</tr>
<tr>
<td>$S_{31}$</td>
<td>1 1 0 1</td>
<td>unstable</td>
</tr>
<tr>
<td>$S_{32}$</td>
<td>1 1 1 0</td>
<td>unstable</td>
</tr>
<tr>
<td>$S_{33}$</td>
<td>1 1 1 1</td>
<td>unstable</td>
</tr>
</tbody>
</table>

Bibliography

CHAPTER 6

Examples

6-1 Introduction

In this chapter several examples are presented in order to show the functioning of the algorithm as well as the several particular problems arising during the formulation of the equations for some of the examples under discussion. The examples to be described are:

1. Schmitt-trigger circuit
2. Flip-flop circuit
3. Reflected flip-flop circuit
4. Nine solutions circuit
5. Current source

In the first example, a complete analysis is done. In particular the structure of the matrix $G^{-1}$ is completely described by means of figures showing the topological implications for each element. In addition, all elements in the set $\mathcal{C}(T_q, G)$ are symbolically determined, and an expression is found for the element $C_5$ which leads to the condition for the circuit to possess several DC solutions. The involved matrices as
well as the numerical results from the evaluation of the juxtaposed set \( \mathcal{O}(\mathbf{T}_q, \mathbf{G}) \) are presented. In the last step, the DC operating points are found and the multivalued transfer functions are plotted.

In the second example, the structure of the matrix \( \mathbf{G}^{-1} \) is also fully described, but no symbolical analysis of the juxtaposed set has been done. In an ulterior step, the involved matrices and the results of the analysis of \( \mathcal{O}(\mathbf{T}_q, \mathbf{G}) \) are presented. Finally all solutions are obtained.

The third example involves a circuit formed by the mirroring of the flip-flop circuit from the previous example. For this reflected flip-flop circuit, only the numerical results concerning the involved matrices and the juxtaposed set are presented. In a second step, the solutions of the circuit are found.

The circuit used for the fourth example is a bench-mark circuit used by several authors. Last, an example involving a current source is analyzed.

### 6-2 Schmitt-trigger circuit

In this section the circuit shown in figure 6.1 [1, 2] is presented.

The currents \( i_1, i_2, i_3 \) and \( i_4 \), which are defined in the figure, are determined as:

\[
\begin{bmatrix}
  i_1 \\
  i_2 \\
  i_3 \\
  i_4
\end{bmatrix} = \begin{bmatrix}
  G_e & 0 & 0 & 0 \\
  -G_1 & (G_{c1} + G_1) & G_1 & 0 \\
  -(G_1 + G_2) & G_2 & (G_1 + G_2) & 0 \\
  G_{c2} & 0 & -G_{c2} & G_{c2}
\end{bmatrix} \begin{bmatrix}
  v_1 \\
  v_2 \\
  v_3 \\
  v_4
\end{bmatrix} + \begin{bmatrix}
  G_e V_{bb} \\
  G_{c1}(V_{bb} - V_{cc}) \\
  -G_2 V_{bb} \\
  G_{c2}(V_{bb} - V_{cc})
\end{bmatrix}
\]

where \( G_x = 1/R_x \).

This equation is easily solved for \( i_1, i_2, i_3 \) and \( i_4 \), as functions of \( v_1, v_2, v_3 \) and \( V_{bb} \) and \( V_{cc} \), in order to obtain the 2q-port representation given in figure 4.6. Then, we can write:

\[ i = Gv + c \]
where \( i = col(i_1, i_2, i_3, i_4) \), \( v = col(v_1, v_2, v_3, v_4) \),

\[
G = \begin{bmatrix}
(G_1 + G_2 + G_e + G_{c_2}) & -G_1 & -(G_1 + G_2 + G_{c_2}) & G_{c_2} \\
-G_1 & (G_{c_1} + G_1) & G_1 & 0 \\
-(G_1 + G_2 + G_{c_2}) & G_1 & (G_1 + G_2 + G_{c_2}) & -G_{c_2} \\
G_{c_2} & 0 & -G_{c_2} & G_{c_2}
\end{bmatrix}
\]

and

\[
c = \begin{bmatrix}
(G_2 + G_e + G_{c_2})V_{bb} - G_{c_2}V_{cc} \\
G_{c_1}(V_{bb} - V_{cc}) \\
-(G_2 + G_{c_2})V_{bb} + G_{c_2}V_{cc} \\
G_{c_2}(V_{bb} - V_{cc})
\end{bmatrix}
\]

### 6-2-1 \( G^{-1} \) matrix

The matrix \( G^{-1} \) can be obtained directly by inverting \( G \); however, in this section the elements of the matrix \( G^{-1} \) are obtained by analyzing the impedance loops related to the transistor junctions according to the concepts explained in section 5-3.

In order to determine the elements of this matrix, it is assumed that the voltage sources are reduced to a short circuit (i.e. \( V_{bb} = 0 \) and...
$V_{cc} = 0$), and then we proceed to analyse all the loops formed at each of the BE and BC junctions.

The matrix $G^{-1}$ has the following structure:

$$G^{-1} = \begin{bmatrix} r_{11} & r_{12} \\ r_{21} & r_{22} \end{bmatrix}$$

where each $r_{ij}$ represents a $2 \times 2$ matrix.

Firstly, those blocks that are related to each particular transistor are determined; i.e. the blocks $r_{11}$ and $r_{22}$. Then the interconnection block ($r_{12}$ is determined $^1$).

- Blocks in the main diagonal:

  - For transistor $Q_1$:

    $\text{block } r_{11} = \begin{bmatrix} z_{11} & z_{12} \\ z_{21} & z_{22} \end{bmatrix}$

    - $z_{11} = R_e$
    - $z_{22} = R_{c1} \parallel (R_1 + R_2)$
    - $z_{12} = z_{21} = z_{11} \cap z_{22} = 0$

  - For transistor $Q_2$:

    $\text{block } r_{22} = \begin{bmatrix} z_{33} & z_{34} \\ z_{43} & z_{44} \end{bmatrix}$

    - $z_{33} = R_e + R_2 \parallel (R_1 + R_{c1})$
    - $z_{44} = R_{c2} + R_2 \parallel (R_1 + R_{c1})$
    - $z_{34} = z_{43} = z_{33} \cap z_{44} = R_2 \parallel (R_1 + R_{c1})$

$^1$The element $r_{21}$ is simply the transpose of $r_{12}$.
- Block outside the main diagonal: \[ r_{12} = \begin{bmatrix} z_{13} & z_{14} \\ z_{23} & z_{24} \end{bmatrix} \]

(a) Loops on the BE junction of Q1 and the BE junction of Q2
\[ z_{13} = z_{11} \cap z_{33} = R_e \]

(b) Loops on the BE junction of Q1 and the BC junction of Q2
\[ z_{14} = z_{11} \cap z_{44} = 0 \]

(c) Loops on the BC junction of Q1 and the BE junction of Q2
\[ z_{23} = z_{22} \cap z_{33} = -\frac{R_2}{R_1 + R_2} \left[ R_{c1} \parallel (R_1 + R_2) \right] \]

(d) Loops on the BC junction of Q1 and the BC junction of Q2
\[ z_{24} = z_{22} \cap z_{44} = -\frac{R_2}{R_1 + R_{c1}} \left[ R_2 \parallel (R_1 + R_{c1}) \right] = z_{23} \]
Hence, the $G^{-1}$ matrix is given by:

$$G^{-1} = \begin{bmatrix}
R_e & 0 & 0 & R_e \\
0 & R_c & 0 & -k[R_c][(R_1 + R_2)] \\
0 & -k[R_c][(R_1 + R_2)] & R_c & 0 \\
\end{bmatrix}$$

where $k = \frac{R_2}{R_1 + R_2}$.

6-2-2 Elements of the juxtaposed set $C(T, G)$

The matrices $T$ and $G$ will be used to form the juxtaposed set. The matrix $T$ is the block diagonal matrix representing the transistor model and is given by:

$$T = \begin{bmatrix}
1 & -\alpha_f^{(1)} & 0 & 0 \\
-\alpha_f^{(1)} & 1 & 0 & 0 \\
0 & 0 & 1 & -\alpha_r^{(2)} \\
0 & 0 & -\alpha_f^{(2)} & 1 \\
\end{bmatrix}$$

(6.3)

The set $C(T, G)$ contains $2^4$ matrices, here denoted as $C_i$. The matrices $\in C(T, G)$ are:

$$C_0 = T$$

$$\det C_0 = \det T = (1 - \alpha_f^{(1)} \alpha_r^{(1)}) (1 - \alpha_r^{(2)} \alpha_f^{(2)})$$

$$C_1 = \begin{bmatrix}
1 & -\alpha_r^{(1)} & 0 & G_{c2} \\
-\alpha_f^{(1)} & 1 & 0 & 0 \\
0 & 0 & 1 & -G_{c2} \\
0 & 0 & -\alpha_f^{(2)} & G_{c2} \\
\end{bmatrix}$$

$$\det C_1 = G_{c2} (1 - \alpha_f^{(2)}) (1 - \alpha_f^{(1)} \alpha_r^{(1)})$$
\[ C_2 = \begin{bmatrix} 1 & -\alpha_r^{(1)} & -G_1 - G_2 - G_{c_2} & 0 \\ -\alpha_f^{(1)} & 1 & G_1 & 0 \\ 0 & 0 & G_1 + G_2 + G_{c_2} & -\alpha_r^{(2)} \\ 0 & 0 & -G_{c_2} & 1 \end{bmatrix} \]

\[ \det C_2 = (1 - \alpha_f^{(1)} \alpha_r^{(1)}) \left( G_1 + G_2 + G_{c_2} - \alpha_r^{(2)} G_{c_2} \right) \]

\[ C_3 = \begin{bmatrix} 1 & -\alpha_r^{(1)} & -G_1 - G_2 - G_{c_2} & G_{c_2} \\ -\alpha_f^{(1)} & 1 & G_1 & 0 \\ 0 & 0 & G_1 + G_2 + G_{c_2} & -G_{c_2} \\ 0 & 0 & -G_{c_2} & G_{c_2} \end{bmatrix} \]

\[ \det C_3 = (G_1 + G_2) G_{c_2} \left( 1 - \alpha_f^{(1)} \alpha_r^{(1)} \right) \]

\[ C_4 = \begin{bmatrix} 1 & -G_1 & 0 & 0 \\ -\alpha_f^{(1)} & G_{c_1} + G_1 & 0 & 0 \\ 0 & G_1 & 1 & -\alpha_r^{(2)} \\ 0 & 0 & -\alpha_f^{(2)} & 1 \end{bmatrix} \]

\[ \det C_4 = (G_{c_1} + G_1 - \alpha_f^{(1)} G_1) \left( 1 - \alpha_r^{(2)} \alpha_f^{(2)} \right) \]

\[ C_5 = \begin{bmatrix} 1 & -G_1 & 0 & G_{c_2} \\ -\alpha_f^{(1)} & G_{c_1} + G_1 & 0 & 0 \\ 0 & G_1 & 1 & -G_{c_2} \\ 0 & 0 & -\alpha_f^{(2)} & G_{c_2} \end{bmatrix} \]

\[ \det C_5 = G_{c_2} \left[ G_{c_1} \left( 1 - \alpha_f^{(2)} \right) + G_1 \left( 1 - \alpha_f^{(1)} - \alpha_f^{(2)} \right) \right] \]
\[ C_6 = \begin{bmatrix}
1 & -G_1 & -G_1 - G_2 - G_{c2} & 0 \\
-G_1 & G_{c1} + G_1 & G_1 & 0 \\
0 & G_1 & G_1 + G_2 + G_{c2} & -\alpha_r^{(2)} \\
0 & 0 & -G_{c2} & 1
\end{bmatrix} \]

\[ \det C_6 = G_{c1} G_1 + G_{c1} G_2 + G_{c1} G_{c2} \left( 1 - \alpha_r^{(2)} \right) + G_1 G_2 + G_1 G_{c2} \left( 1 - \alpha_r^{(2)} + \alpha_f^{(1)} \alpha_r^{(2)} \right) \]

\[ C_7 = \begin{bmatrix}
1 & -G_1 & -G_1 - G_2 - G_{c2} & G_{c2} \\
-G_1 & G_{c1} + G_1 & G_1 & 0 \\
0 & G_1 & G_1 + G_2 + G_{c2} & -G_{c2} \\
0 & 0 & -G_{c2} & G_{c2}
\end{bmatrix} \]

\[ \det C_7 = G_{c2} \left( G_{c1} G_1 + G_{c1} G_2 + G_1 G_2 \right) \]

\[ C_8 = \begin{bmatrix}
G_1 + G_2 + G_e + G_{c2} & -\alpha_r^{(1)} & 0 & 0 \\
-G_1 & 1 & 0 & 0 \\
-G_1 - G_2 - G_{c2} & 0 & 1 & -\alpha_r^{(2)} \\
G_{c2} & 0 & -\alpha_f^{(2)} & 1
\end{bmatrix} \]

\[ \det C_8 = \left( G_1 + G_2 + G_e + G_{c2} - G_1 \alpha_r^{(1)} \right) \left( 1 - \alpha_r^{(2)} \alpha_f^{(2)} \right) \]

\[ C_9 = \begin{bmatrix}
G_1 + G_2 + G_e + G_{c2} & -\alpha_r^{(1)} & 0 & G_{c2} \\
-G_1 & 1 & 0 & 0 \\
-G_1 - G_2 - G_{c2} & 0 & 1 & -G_{c2} \\
G_{c2} & 0 & -\alpha_f^{(2)} & G_{c2}
\end{bmatrix} \]

\[ \det C_9 = G_{c2} \left[ G_1 \left( 1 - \alpha_r^{(1)} + \alpha_r^{(1)} \alpha_f^{(2)} \right) + G_2 + G_e \left( 1 - \alpha_f^{(2)} \right) \right] \]
\[ C_{10} = \begin{bmatrix} G_1 + G_2 + G_e + G_{c2} & -\alpha_r^{(1)} & -G_1 - G_2 - G_{c2} & 0 \\ -G_1 & 1 & G_1 & 0 \\ -G_1 - G_2 - G_{c2} & 0 & G_1 + G_2 + G_{c2} & -\alpha_r^{(2)} \\ G_{c2} & 0 & -G_{c2} & 1 \end{bmatrix} \]

\[ \det C_{10} = G_e \left[ G_1 + G_2 + G_{c2} \left( 1 - \alpha_r^{(2)} \right) \right] \]

\[ C_{11} = \begin{bmatrix} G_1 + G_2 + G_e + G_{c2} & -\alpha_r^{(1)} & -G_1 - G_2 - G_{c2} & G_{c2} \\ -G_1 & 1 & G_1 & 0 \\ -G_1 - G_2 - G_{c2} & 0 & G_1 + G_2 + G_{c2} & -G_{c2} \\ G_{c2} & 0 & -G_{c2} & G_{c2} \end{bmatrix} \]

\[ \det C_{11} = G_e G_{c2} \left( G_1 + G_2 \right) \]

\[ C_{12} = \begin{bmatrix} G_1 + G_2 + G_e + G_{c2} & -G_1 & 0 & 0 \\ -G_1 & G_e + G_{c1} + G_1 & 0 & 0 \\ -G_1 - G_2 - G_{c2} & G_1 & 1 & -\alpha_f^{(2)} \\ G_{c2} & 0 & -\alpha_f^{(2)} & 1 \end{bmatrix} \]

\[ \det C_{12} = \frac{\left( G_{c1} G_1 + G_{c1} G_2 + G_1 G_2 + G_e G_e G_{c1} + G_e G_1 + G_{c1} G_{c2} + G_1 G_{c2} \right)}{\left( 1 - \alpha_r^{(2)} \alpha_f^{(2)} \right)} \]

\[ C_{13} = \begin{bmatrix} G_1 + G_2 + G_e + G_{c2} & -G_1 & 0 & G_{c2} \\ -G_1 & G_e + G_{c1} + G_1 & 0 & 0 \\ -G_1 - G_2 - G_{c2} & G_1 & 1 & -G_{c2} \\ G_{c2} & 0 & -\alpha_f^{(2)} & G_{c2} \end{bmatrix} \]

\[ \det C_{13} = G_{c2} \left( \frac{G_{c1} G_2 + G_1 G_2 + G_{c1} G_1 + G_e G_{c1} \left( 1 - \alpha_f^{(2)} \right) + G_e G_1 \left( 1 - \alpha_f^{(2)} \right)}{G_{c2}} \right) \]
\[ C_{14} = \begin{bmatrix} G_1 + G_2 + G_e + G_{e2} & -G_1 & -G_1 - G_2 - G_{e2} & 0 \\ -G_1 & G_{c1} + G_1 & G_1 & 0 \\ -G_1 - G_2 - G_{e2} & G_1 & G_1 + G_2 + G_{e2} & -\alpha_r^{(2)} \\ G_{e2} & 0 & -G_{c2} & 1 \end{bmatrix} \]

\[
\det C_{14} = G_e \left( \frac{G_{c1} G_1 + G_{c1} G_{e2} +}{G_{c1} G_{c2} \left( 1 - \alpha_r^{(2)} \right) +} \frac{G_{c1} G_{c2} \left( 1 - \alpha_r^{(2)} \right)}{G_1 G_2 + G_1 G_{c2} \left( 1 - \alpha_r^{(2)} \right)} \right)
\]

\[ C_{15} = G = \begin{bmatrix} G_1 + G_2 + G_e + G_{e2} & -G_1 & -(G_1 + G_2 + G_{e2}) & G_{c2} \\ -G_1 & G_{c1} + G_1 & G_1 & 0 \\ -(G_1 + G_2 + G_{e2}) & G_1 & G_1 + G_2 + G_{e2} & -G_{c2} \\ G_{c2} & 0 & -G_{c2} & G_{c2} \end{bmatrix} \]

\[
\det C_{15} = \det G = G_e G_{c2} \left( G_{c1} G_1 + G_{c1} G_2 + G_1 G_2 \right)
\]

It is not necessary to accomplish the analysis above in such a complete form. It is here so done, merely in order to illustrate the procedure of forming the various elements in the set \( C \) and their respective determinants. In practice this is not done, instead, only the element \( \mathcal{O}^{be} \) is numerically analyzed because of the fact that for a circuit containing two transistors, this element represents the only possibility for the circuit to have multiple solutions. Besides, a symbolical analysis like this is very time consuming since \( 2^n \) determinants must be evaluated; which is not practical for matrices of size \( > 2 \).

Only the expressions in the "boxes" corresponding to \( C_5 \) (i.e. \( \mathcal{O}^{be} \)) and its determinant may become negative, which occurs if:

\[
\left[ G_{c1} \left( 1 - \alpha_f^{(2)} \right) + G_1 \left( 1 - \alpha_f^{(1)} - \alpha_f^{(2)} \right) \right] < 0
\]

This inequality constitutes the condition for the circuit to have the possibility to present multiple DC operating points, which ensures that the circuit will function with the well-known hysteresis behavior.
6-2-3 Other involved matrices

In this section, other involved matrices are shown. The matrix of the 2\(q\)-representation \((G^{-1})\) is obtained from the congruency transformation of the initial MNA representation.

- Symbolical MNA matrix of the linear part of the circuit

\[
Y_{MNA_{lin}} = 
\begin{bmatrix}
G_{c1} + G_{c2} & -G_{c1} & -G_{c2} & 0 & 0 & 0 & 1 & 0 \\
-G_{c1} & G_{c1} + G_1 & 0 & -G_1 & 0 & 0 & 0 & 0 \\
-G_{c2} & 0 & G_{c2} & 0 & 0 & 0 & 0 & 0 \\
0 & -G_1 & 0 & G_1 + G_2 & 0 & 0 & 0 & 0 \\
0 & 0 & 0 & 0 & G_e & 0 & 0 & 0 \\
0 & 0 & 0 & 0 & 0 & r_0 & 1 & 0 \\
1 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\
0 & 0 & 0 & 0 & 0 & 0 & 1 & 0 \\
\end{bmatrix}
\]

The part of the matrix under the dashed columns represents the entries of the nodes as given in figure 6.1. The remaining columns correspond to the currents through the voltage sources in the circuit. A resistor \(r_0\) has been added, in order to avoid the ill-condition of the matrix during the LU decomposition procedure. Without this resistor, the linear part of the circuit would constitute a non-connected network. The inverse is thus calculated and evaluated by making \(r_0 \rightarrow \infty\).

- Inverse of the MNA matrix of the linear part of the circuit

\[
Y^{-1}_{MNA_{lin}} = 
\begin{bmatrix}
0 & 0 & 0 & 0 & 0 & 0 & 1 & 0 \\
0 & \frac{G_1 + G_2}{\delta} & 0 & \frac{G_1}{\delta} & 0 & 0 & 0 & 0 \\
0 & 0 & 1/G_{c2} & 0 & 0 & 0 & 0 & 0 \\
0 & \frac{G_1}{\delta} & 0 & \frac{G_{c1} + G_1}{\delta} & 0 & 0 & 0 & 0 \\
0 & 0 & 0 & 0 & 1/G_e & 0 & 0 & 0 \\
0 & 0 & 0 & 0 & 0 & 0 & 0 & 1 \\
\frac{1}{G_{c1} (G_1 + G_2)} & \frac{G_{c1} G_1}{\delta} & 0 & 0 & 0 & 0 & 0 & 1/\delta \\
0 & 0 & 0 & 0 & 0 & 0 & 1 & 0 \\
\end{bmatrix}
\]

where: \(\delta = G_{c1} G_1 + G_{c1} G_2 + G_1 G_2\).
The transformation matrix.

\[ K = \begin{bmatrix}
0 & 0 & 0 & 0 \\
0 & 1 & 0 & 0 \\
0 & 0 & 0 & 1 \\
0 & 0 & -1 & -1 \\
1 & 0 & 1 & 0 \\
-1 & -1 & 0 & 0 \\
0 & 0 & 0 & 0 \\
0 & 0 & 0 & 0
\end{bmatrix} \]

where the columns are associated to the ports (the transistor junctions) and the rows to the nodes.

Numerical congruency transformation matrix:

\[ G^{-1} = \begin{bmatrix}
1000 & 0 & 1000 & 0 \\
0 & 950 & -400 & -400 \\
1000 & -400 & 5800 & 4800 \\
0 & -400 & 4800 & 5800
\end{bmatrix} \]

where the numerical entries come from the components values given in the table on the figure 6.1.

The numerical matrix corresponding to the transistors model.

\[ T = \begin{bmatrix}
1 & -0.33 & 0 & 0 \\
-0.99 & 1 & 0 & 0 \\
0 & 0 & 1 & -0.33 \\
0 & 0 & -0.99 & 1
\end{bmatrix} \]

Numerical \( R' \) matrix.

\[ R' = G^{-1}T = \begin{bmatrix}
1000 & -333 & 1000 & -333 \\
-940.5 & 950 & -4 & -266.8 \\
1396 & -733 & 1048 & 2868.6 \\
396 & -400 & -942 & 4201.6
\end{bmatrix} \]
6-2-4  Numerical results from analysis of juxtaposed set

The juxtaposed set \( \mathcal{O}(R' = G^{-1} T, I) \) will be formed, where the matrices involved are:

\[
R' = G^{-1} T = \begin{bmatrix}
1000 & -333 & 1000 & -333 \\
-940.5 & 950 & -4 & -266.8 \\
1396 & -733 & 1048 & 2608.8 \\
396 & -400 & -942 & 4201.6
\end{bmatrix}
\]

\[
I = \begin{bmatrix}
1 & 0 & 0 & 0 \\
0 & 1 & 0 & 0 \\
0 & 0 & 1 & 0 \\
0 & 0 & 0 & 1
\end{bmatrix}
\]

The following table presents the results from the analysis of the elements \( \in \mathcal{O} \).

<table>
<thead>
<tr>
<th>N</th>
<th>det</th>
<th>Type</th>
<th>Sign</th>
<th>Index</th>
<th>Binary index</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>-3.4800000e+05</td>
<td>( \mathcal{O}^{be} )</td>
<td>NEG!</td>
<td>5</td>
<td>[0,1,0,1]</td>
</tr>
<tr>
<td>1</td>
<td>4.333468e+06</td>
<td>( \mathcal{O}^{mix} )</td>
<td>_POS</td>
<td>6</td>
<td>[0,1,1,0]</td>
</tr>
<tr>
<td>2</td>
<td>9.926680e+05</td>
<td>( \mathcal{O}^{mix} )</td>
<td>_POS</td>
<td>9</td>
<td>[1,0,0,1]</td>
</tr>
<tr>
<td>3</td>
<td>3.884800e+06</td>
<td>( \mathcal{O}^{bc} )</td>
<td>_POS</td>
<td>10</td>
<td>[1,0,1,0]</td>
</tr>
</tbody>
</table>

6-2-5  Finding the solutions

From the results above, it follows that a maximum of three solutions may appear because the element \( \mathcal{O}^{be} \) is negative. The solutions have the following binary index:

<table>
<thead>
<tr>
<th>Solution</th>
<th>Binary state</th>
<th>stability</th>
</tr>
</thead>
<tbody>
<tr>
<td>( S_1 )</td>
<td>0 1</td>
<td>stable</td>
</tr>
<tr>
<td>( S_2 )</td>
<td>1 0</td>
<td>stable</td>
</tr>
<tr>
<td>( S_3 )</td>
<td>1 1</td>
<td>unstable</td>
</tr>
</tbody>
</table>

The stability is determined by calculating the eigenvalues, which are given in the form of a \( 2Q \times 2 \) matrix. Each row indicates an eigenvalue. Each one is denoted by \( \text{Re}\ e \) and \( \text{Im}\ m \) parts.

For the circuit values given in figure 6.1 the solutions are given by:

- 1st solution,

\[
v = \begin{bmatrix}
-0.31516 \\
3.32985 \\
0.210593 \\
7.19675
\end{bmatrix}
\]

\[
i = \begin{bmatrix}
0.00301476 \\
-0.00298463 \\
-9.8792e-11 \\
-2.00322e-08
\end{bmatrix}
\]
Checking stability for the 1st solution.

\[
\begin{align*}
\text{eigenvalues of } [RTd + I] &= \begin{bmatrix} 1 & 0 \\ 1 & 0 \\ 0 & 0 \\ 0 & 0 \\ 121.59 & 0 \end{bmatrix} \\
\det [RTd + I] &= 121.59
\end{align*}
\]

\(\rightarrow\) Stable

2nd solution.

\[
\begin{align*}
v &= \begin{bmatrix} 0.230434 \\ 6.1601 \\ -0.219439 \\ 2.58459 \end{bmatrix} \\
\hat{v} &= \begin{bmatrix} -1.00007e-10 \\ -2.0031e-08 \\ 0.00357751 \\ -0.00354175 \end{bmatrix}
\end{align*}
\]

Checking stability for the 2nd solution.

\[
\begin{align*}
\text{eigenvalues of } [RTd + I] &= \begin{bmatrix} 1 & 0 \\ 1 & 0 \\ 150.969 & 0 \\ 1 & 0 \end{bmatrix} \\
\det [RTd + I] &= 150.969
\end{align*}
\]

\(\rightarrow\) Stable

3rd solution.

\[
\begin{align*}
v &= \begin{bmatrix} -0.297894 \\ 4.7471 \\ -0.236208 \\ 5.15024 \end{bmatrix} \\
\hat{v} &= \begin{bmatrix} 0.001541118 \\ 0.00154027 \\ 0.00154027 \\ -0.001541499 \end{bmatrix}
\end{align*}
\]

Checking stability for the 3rd solution.

\[
\begin{align*}
\text{eigenvalues of } [RTd + I] &= \begin{bmatrix} 1 & 0 \\ 1 & 0 \\ 135.191 & 0 \\ -8.5953 & 0 \end{bmatrix} \\
\det [RTd + I] &= -1162.01
\end{align*}
\]

There is 1 negative eigenvalue; \(\rightarrow\) Unstable

6-2-6 Multivalued transfer functions

The results above (for \(V_{bb} = 3.33\)) are easily checked if the variables \((v_1, v_2, v_3, v_4)\) and \((i_1, i_2, i_3, i_4)\) are determined for different values of \(V_{bb}\). Figures 6.2 and 6.3 show the typical behavior of the circuit.
Figure 6.2: Voltages from the transistor junctions.
(a) $i_1$ vs $V_{bb}$  
(b) $i_2$ vs $V_{bb}$  
(c) $i_3$ vs $V_{bb}$  
(d) $i_4$ vs $V_{bb}$

Figure 6.3: Currents from the transistor junctions.
6-3 Flip-flop circuit

In this section the circuit reported in [3] (fig. 6.4) is presented. The analysis is carried out in a shorter form with respect to the previous example.

![Flip-flop circuit diagram]

<table>
<thead>
<tr>
<th>Components</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>$R_{c1} = R_{c2}$</td>
<td>2K</td>
</tr>
<tr>
<td>$R_{b1} = R_{b2}$</td>
<td>61K</td>
</tr>
<tr>
<td>$V_{cc}$</td>
<td>-12</td>
</tr>
</tbody>
</table>

Figure 6.4: Flip-flop circuit.

6-3-1 Matrix $G^{-1}$

In this section the elements of the matrix $G^{-1}$ are obtained by analyzing the impedance loops.

The matrix $G^{-1}$ again has the following structure:

$$G^{-1} = \begin{bmatrix} r_{11} & r_{12} \\ r_{21} & r_{22} \end{bmatrix}$$
The elements are given by:

- Blocks in the main diagonal:

  For transistor \( Q_1 \):

  \[
  \text{block } r_{11} = \begin{bmatrix} z_{11} & z_{12} \\ z_{21} & z_{22} \end{bmatrix}
  \]

  \[
  z_{11} = R_{b1} + R_{c2} \\
  z_{22} = R_{b1} + R_{c2} + R_{c1} \\
  z_{12} = z_{21} = z_{11} \cap z_{22} = R_{b1} + R_{c2}
  \]

  For transistor \( Q_2 \):

  \[
  \text{block } r_{22} = \begin{bmatrix} z_{33} & z_{34} \\ z_{43} & z_{44} \end{bmatrix}
  \]

  \[
  z_{33} = R_{b2} + R_{c1} \\
  z_{44} = R_{b2} + R_{c2} + R_{c1} \\
  z_{34} = R_{b2} \cap z_{44} = R_{b2} + R_{c1}
  \]

- Block outside the main diagonal: \( r_{12} = \begin{bmatrix} z_{13} & z_{14} \\ z_{23} & z_{24} \end{bmatrix} \).
6-3. FLIP-FLOP CIRCUIT

- (a) Loops on the BE junction of Q₁ and the BE junction of Q₂
  \[ z_{13} = z_{11} \cap z_{33} = 0 \]
- (b) Loops on the BE junction of Q₁ and the BC junction of Q₂
  \[ z_{14} = z_{11} \cap z_{44} = -R_{c2} \]
- (c) Loops on the BC junction of Q₁ and the BE junction of Q₂
  \[ z_{23} = z_{22} \cap z_{33} = -R_{c1} \]
- (d) Loops on the BC junction of Q₁ and the BC junction of Q₂
  \[ z_{24} = z_{22} \cap z_{44} = -(R_{c1} + R_{c2}) \]

In this way, the \( G^{-1} \) matrix is given by:

\[
G^{-1} = \begin{bmatrix}
R_{b1} + R_{c2} & R_{b1} + R_{c2} & 0 & -R_{c2} \\
R_{b1} + R_{c2} & R_{b1} + R_{c2} + R_{c1} & -R_{c1} & -(R_{c1} + R_{c2}) \\
0 & -R_{c1} & R_{b2} + R_{c1} & R_{b2} + R_{c2} + R_{c1} \\
-R_{c2} & -(R_{c1} + R_{c2}) & R_{b2} + R_{c1} & R_{b2} + R_{c1} + R_{c2}
\end{bmatrix}
\]  \hspace{1cm} (6.4)

6-3-2 Other involved matrices

In this part, several matrices are shown. The numerical matrices are obtained from the components values given in figure 6.4.
\( Y_{MNA_{\text{lin}}} = \begin{bmatrix}
G_{c_1} + G_{c_2} & 0 & -G_{c_1} & 0 & -G_{c_2} & 1 \\
0 & G_{b_1} & 0 & 0 & -G_{b_1} & 0 \\
-G_{c_1} & 0 & G_{c_1} + G_{b_2} & -G_{b_2} & 0 & 0 \\
0 & 0 & -G_{b_2} & G_{b_2} & 0 & 0 \\
-G_{c_2} & -G_{b_1} & 0 & 0 & G_{c_2} + G_{b_1} & 0 \\
1 & 0 & 0 & 0 & 0 & 0 
\end{bmatrix} \)

where \( G_z = R_z \). The column numbers correspond to the node numbers of the circuit according to figure 6.4.

- Inverse MNA matrix of the linear part of the circuit:

\( Y^{-1}_{MNA_{\text{lin}}} = \begin{bmatrix}
0 & 0 & 0 & 0 & 0 & 1 \\
0 & R_{b_1} + R_{c_2} & 0 & 0 & R_{c_2} & 1 \\
0 & 0 & R_{c_1} & R_{c_1} & 0 & 1 \\
0 & 0 & R_{c_1} & R_{c_1} + R_{b_2} & 0 & 1 \\
0 & R_{c_2} & 0 & 0 & R_{c_2} & 1 \\
1 & 1 & 1 & 1 & 1 & 0 
\end{bmatrix} \)

- The transformation matrix.

\( K = \begin{bmatrix}
0 & 0 & 0 & 0 & 1 \\
-1 & -1 & 0 & 0 \\
0 & 1 & 0 & 0 \\
0 & 0 & -1 & -1 \\
0 & 0 & 0 & 1 \\
0 & 0 & 0 & 0 
\end{bmatrix} \)

- Inverse of the congruency matrix:

\[
G = \begin{bmatrix}
G_{c_1} + G_{b_2} + G_{b_1} & -(G_{c_1} + G_{b_2}) & -(G_{b_2} + G_{b_1}) & G_{b_1} \\
-(G_{c_1} + G_{b_2}) & G_{c_1} + G_{b_2} & G_{b_2} & 0 \\
-(G_{b_2} + G_{b_1}) & G_{b_2} & G_{c_2} + G_{b_2} + G_{b_1} & -(G_{c_2} + G_{b_1}) \\
G_{b_1} & 0 & -(G_{c_2} + G_{b_1}) & G_{c_2} + G_{b_1} 
\end{bmatrix}
\]
6.3. FLIP-FLOP CIRCUIT

- The matrix corresponding to the transistor model.

\[
T = \begin{bmatrix}
1 & -\alpha_t^{(q1)} & 0 & 0 \\
-\alpha_f^{(q1)} & 1 & 0 & 0 \\
0 & 0 & 1 & -\alpha_t^{(q2)} \\
0 & 0 & -\alpha_f^{(q2)} & 1
\end{bmatrix}
= \begin{bmatrix}
1 & -0.33 & 0 & 0 \\
-0.99 & 1 & 0 & 0 \\
0 & 0 & 1 & -0.33 \\
0 & 0 & -0.99 & 1
\end{bmatrix}
\]

- Numerical \(G^{-1}\) matrix.

\[
G^{-1} = \begin{bmatrix}
63K & 63K & 0 & -2K \\
63K & 65K & -2K & -4K \\
0 & -2K & 63K & 63K \\
-2K & -4K & 63K & 65K
\end{bmatrix}
\]

- Numerical \(R'\) matrix.

\[
R' = G^{-1}T = \begin{bmatrix}
630 & 42210 & 1980 & -2000 \\
-1350 & 44210 & 1960 & -3340 \\
1980 & -2000 & 630 & 42210 \\
1960 & -3340 & -1350 & 44210
\end{bmatrix}
\]

6-3-3 Numerical results from analysis of juxtaposed sets

The following matrices will be used to form the juxtaposed set \(\mathcal{O}(R' = G^{-1}T, I)\):

\[
R' = \begin{bmatrix}
630 & 42210 & 1980 & -2000 \\
-1350 & 44210 & 1960 & -3340 \\
1980 & -2000 & 630 & 42210 \\
1960 & -3340 & -1350 & 44210
\end{bmatrix}
\]

\[
I = \begin{bmatrix}
1 & 0 & 0 & 0 \\
0 & 1 & 0 & 0 \\
0 & 0 & 1 & 0 \\
0 & 0 & 0 & 1
\end{bmatrix}
\]

The next table shows the results of analyzing the elements in the juxtaposed \(\mathcal{O}\) set.
### 6-3-4 Finding the solutions

Because $O^{be}$ is negative, the circuit may possess a maximum of three solutions, which are given by:

- **1st solution.**

\[
\begin{bmatrix}
0.765999 \\
0.644632 \\
0.121367 \\
-11.522
\end{bmatrix}
\quad i =
\begin{bmatrix}
-0.00611763 \\
0.00593932 \\
-1.05416e-13 \\
1.06362e-13
\end{bmatrix}
\]

◇ Checking stability for the 1st solution.

\[
\text{eigenvalues of } [RTd + I] =
\begin{bmatrix}
1 & 0 \\
223.73 & 291.92 \\
223.73 & -291.92 \\
1 & 0
\end{bmatrix}
\]

$\sim$ Stable

- **2nd solution.**

\[
\begin{bmatrix}
0.121367 \\
-11.522 \\
0.765999 \\
0.644632
\end{bmatrix}
\quad i =
\begin{bmatrix}
-1.05416e-13 \\
1.06362e-13 \\
-0.00611763 \\
0.00593932
\end{bmatrix}
\]

◇ Checking stability for the 2nd solution.

\[
\text{eigenvalues of } [RTd + I] =
\begin{bmatrix}
1 & 0 \\
1 & 0 \\
223.73 & 291.92 \\
223.73 & -291.92
\end{bmatrix}
\]

$\sim$ Stable
6-4. REFLECTED FLIP-FLOP CIRCUIT

- 3rd solution.

\[ v = \begin{bmatrix} 0.756636 \\ -2.62776 \\ 0.756636 \\ -2.62776 \end{bmatrix}, \quad i = \begin{bmatrix} -0.0043078 \\ 0.00426472 \\ -0.0043078 \\ 0.00426472 \end{bmatrix} \]

Checking stability for the 3rd solution.

The eigenvalues of \( RTd + I \) are:

\[ \begin{bmatrix} 1 & 0 \\ 1 & 0 \\ 433.437 & 0 \\ -222.674 & 0 \end{bmatrix} \]

\[ \det [RTd + I] = -96515.3 \]

There is 1 negative eigenvalue: \( \to \) Unstable

6-4 Reflected flip-flop circuit

In this section, another example is presented; which is a very trivial application of the partitioning procedure. The circuit consists of the flip-flop — the same as in the previous section — but here it is reflected along the voltage source (fig. 6.5), which is of course a very simple form of a circuit with the partitioning characteristic, but it is here presented with the aim of exemplifying the partitioning procedure.

The partitioning procedure may become more obvious if the circuit is redrawn by making \( V_{cc} = 0 \). In this form two independent subcircuits can be formed (see fig. 6.6).

Involved matrices

In this part, some matrices are shown, for the numerical ones, the values of the components from the previous example are used.
• The MNA matrix of the linear part of the circuit:

\[
Y_{\text{MNA}_{\text{lin}}} =
\begin{bmatrix}
G_{c_1} + G_{c_2} & 0 & -G_{c_1} & 0 & -G_{c_2} & 0 & -G_{c_3} & 0 & -G_{c_4} & 1 \\
0 & G_{b_1} + G_{c_3} + G_{c_4} & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\
-G_{c_1} & 0 & G_{c_1} + G_{b_2} & 0 & -G_{b_1} & 0 & 0 & 0 & 0 & 0 \\
0 & 0 & -G_{b_2} & G_{b_2} & 0 & 0 & 0 & 0 & 0 & 0 \\
-G_{c_2} & -G_{b_1} & 0 & 0 & G_{c_2} + G_{b_1} & 0 & 0 & 0 & 0 & 0 \\
0 & 0 & 0 & 0 & 0 & G_{b_3} & 0 & 0 & 0 & 0 \\
-G_{c_3} & 0 & 0 & 0 & 0 & 0 & G_{c_3} + G_{b_4} & 0 & -G_{b_4} & 0 \\
0 & 0 & 0 & 0 & 0 & 0 & 0 & G_{b_4} & 0 & 0 \\
-G_{c_4} & 0 & 0 & 0 & 0 & 0 & 0 & 0 & G_{c_4} + G_{b_3} & 0 \\
1 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0
\end{bmatrix}
\]

• Inverse MNA matrix of the linear part of the circuit:

\[
Y_{\text{MNA}_{\text{lin}}}^{-1} =
\begin{bmatrix}
0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\
0 & 0 & R_{b_1} + R_{c_2} & 0 & 0 & 0 & 0 & 0 & 0 & 1 \\
0 & 0 & 0 & R_{c_1} & 0 & 0 & 0 & 0 & 0 & 0 \\
0 & 0 & 0 & 0 & R_{c_1} + R_{b_2} & 0 & 0 & 0 & 0 & 0 \\
0 & 0 & R_{c_2} & 0 & 0 & R_{c_2} & 0 & 0 & 0 & 0 \\
0 & 0 & 0 & 0 & 0 & R_{b_3} + R_{c_4} & 0 & 0 & R_{c_4} & 0 \\
0 & 0 & 0 & 0 & 0 & 0 & R_{c_3} & R_{c_3} & 0 & 0 \\
0 & 0 & 0 & 0 & 0 & 0 & 0 & R_{c_3} & R_{c_3} + R_{b_4} & 0 \\
0 & 0 & 0 & 0 & 0 & R_{c_4} & 0 & 0 & 0 & R_{c_4} \\
1 & 1 & 1 & 1 & 1 & 1 & 1 & 1 & 1 & 0
\end{bmatrix}
\]
- Numerical $Y^{-1}_{MNA_{lin}}$ matrix:

$$
Y^{-1}_{MNA_{lin}} = \begin{bmatrix}
0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 1 \\
0 & 63K & 0 & 0 & 2K & 0 & 0 & 0 & 1 \\
0 & 0 & 2K & 2K & 0 & 0 & 0 & 0 & 1 \\
0 & 0 & 2K & 63K & 0 & 0 & 0 & 0 & 1 \\
0 & 2K & 0 & 0 & 2K & 0 & 0 & 0 & 1 \\
0 & 0 & 0 & 0 & 63K & 0 & 0 & 2K & 1 \\
0 & 0 & 0 & 0 & 0 & 0 & 2K & 2K & 0 & 1 \\
0 & 0 & 0 & 0 & 0 & 2K & 63K & 0 & 0 & 1 \\
0 & 0 & 0 & 0 & 0 & 2K & 0 & 0 & 1 & 1 \\
1 & 1 & 1 & 1 & 1 & 1 & 1 & 1 & 1 & 1 \\
0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0
\end{bmatrix}
$$

- The transformation matrix:

$$
K = \begin{bmatrix}
0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\
-1 & -1 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\
0 & 1 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\
0 & 0 & -1 & -1 & 0 & 0 & 0 & 0 & 0 \\
0 & 0 & 0 & -1 & 1 & 0 & 0 & 0 & 0 \\
0 & 0 & 0 & 0 & 0 & 0 & 0 & 1 & 0 \\
0 & 0 & 0 & 0 & 0 & 0 & 0 & -1 & -1 \\
0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 1 \\
0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0
\end{bmatrix}
$$

- The transistor matrix:

$$
T_q = \begin{bmatrix}
1 & -\alpha_r^{(q1)} & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\
-\alpha_f^{(q1)} & 1 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\
0 & 0 & 1 & -\alpha_r^{(q2)} & 0 & 0 & 0 & 0 & 0 \\
0 & 0 & -\alpha_f^{(q2)} & 1 & 0 & 0 & 0 & 0 & 0 \\
0 & 0 & 0 & 0 & 0 & 1 & -\alpha_r^{(q3)} & 0 & 0 \\
0 & 0 & 0 & 0 & -\alpha_f^{(q3)} & 1 & 0 & 0 & 0 \\
0 & 0 & 0 & 0 & 0 & 0 & 1 & -\alpha_r^{(q4)} & 0 \\
0 & 0 & 0 & 0 & 0 & 0 & -\alpha_f^{(q4)} & 1 & 0 \\
0 & 0 & 0 & 0 & 0 & 0 & 0 & -\alpha_f^{(q4)} & 1
\end{bmatrix}
$$
• The congruency matrix:

\[ G^{-1} = \begin{bmatrix}
  R_{b1} + R_{c2} & R_{b1} + R_{c2} & 0 & -R_{c2} & 0 & 0 & 0 & 0 \\
  R_{b1} + R_{c2} & R_{b1} + R_{c2} + R_{c1} & -R_{c1} & -(R_{c1} + R_{c2}) & 0 & 0 & 0 & 0 \\
  0 & -R_{c1} & R_{b2} + R_{c1} & R_{b2} + R_{c1} + R_{c1} & 0 & 0 & 0 & 0 \\
  -R_{c2} & -(R_{c1} + R_{c2}) & R_{b2} + R_{c1} & R_{b2} + R_{c1} + R_{c1} & 0 & 0 & 0 & 0 \\
  0 & 0 & 0 & 0 & R_{b3} + R_{c4} & R_{b3} + R_{c4} & 0 & -R_{c4} \\
  0 & 0 & 0 & 0 & R_{b3} + R_{c4} & R_{b3} + R_{c4} + R_{c3} & -R_{c3} & -(R_{c3} + R_{c4}) \\
  0 & 0 & 0 & 0 & -R_{c3} & -(R_{c3} + R_{c4}) & R_{b4} + R_{c3} & R_{b4} + R_{c3} + R_{c3} \\
  0 & 0 & 0 & 0 & -R_{c4} & -(R_{c3} + R_{c4}) & R_{b4} + R_{c3} & R_{b4} + R_{c3} + R_{c3}
\end{bmatrix} \]

• By using the values of the previous example, the numerical \( G^{-1} \) is:

\[ G^{-1} = \begin{bmatrix}
  63K & 63K & 0 & -2K & 0 & 0 & 0 & 0 \\
  63K & 65K & -2K & -4K & 0 & 0 & 0 & 0 \\
  0 & -2K & 63K & 63K & 0 & 0 & 0 & 0 \\
  -2K & -4K & 63K & 65K & 0 & 0 & 0 & 0 \\
  0 & 0 & 0 & 0 & 63K & 63K & 0 & -2K \\
  0 & 0 & 0 & 0 & 63K & 65K & -2K & -4K \\
  0 & 0 & 0 & 0 & 0 & -2K & 63K & 63K \\
  0 & 0 & 0 & 0 & -2K & -4K & 63K & 65K
\end{bmatrix} \]
6-4. REFLECTED FLIP-FLOP CIRCUIT

• Numerical $G$ matrix:

$$ G = \begin{bmatrix} G_{11} & 0 \\ 0 & G_{22} \end{bmatrix} $$

where:

$$ G_{11} = G_{22} = \begin{bmatrix} 532.787 \mu & -516.393 \mu & -32.7869 \mu & 16.3934 \mu \\ -516.393 \mu & 516.393 \mu & 16.3934 \mu & 0 \\ -32.7869 \mu & 16.3934 \mu & 532.787 \mu & -516.393 \mu \\ 16.3934 \mu & 0 & -516.393 \mu & 516.393 \mu \end{bmatrix} $$

$$ R = G^{-1} T_q = \begin{bmatrix} 630 & 42210 & 1980 & -2000 & 0 & 0 & 0 & 0 \\ -1350 & 44210 & 1960 & -3340 & 0 & 0 & 0 & 0 \\ 1980 & -2000 & 630 & 42210 & 0 & 0 & 0 & 0 \\ 1960 & -3340 & -1350 & 44210 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 630 & 42210 & 1980 & -2000 \\ 0 & 0 & 0 & 0 & -1350 & 44210 & 1960 & -3340 \\ 0 & 0 & 0 & 0 & 1980 & -2000 & 630 & 42210 \\ 0 & 0 & 0 & 0 & 1960 & -3340 & -1350 & 44210 \end{bmatrix} $$

6-4-1 Analysis of the juxtaposed sets

The first step consists in forming the juxtaposed set of the following matrices:

$$ R' = G^{-1} T_q = \begin{bmatrix} 630 & 42210 & 1980 & -2000 & 0 & 0 & 0 & 0 \\ -1350 & 44210 & 1960 & -3340 & 0 & 0 & 0 & 0 \\ 1980 & -2000 & 630 & 42210 & 0 & 0 & 0 & 0 \\ 1960 & -3340 & -1350 & 44210 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 630 & 42210 & 1980 & -2000 \\ 0 & 0 & 0 & 0 & -1350 & 44210 & 1960 & -3340 \\ 0 & 0 & 0 & 0 & 1980 & -2000 & 630 & 42210 \\ 0 & 0 & 0 & 0 & 1960 & -3340 & -1350 & 44210 \end{bmatrix} $$

$$ I = \begin{bmatrix} 1 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 1 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 1 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 1 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 1 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 1 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 1 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & 1 \end{bmatrix} $$

The structure of the matrices allows to apply the partitioning process, hence two smaller juxtaposed subsets will be analyzed.
Figure 6.5: Reflected flip-flop circuit.

Figure 6.6: Circuit after $V_{cc} = 0$. 
6-4. REFLECTED FLIP-FLOP CIRCUIT

- 1. A first subset is generated, namely \( O_1(R'_{11}, I^{(4)}) \), which corresponds to the subcircuit containing transistors Q₃ and Q₄:

\[
R'_{11} = \begin{bmatrix}
630 & 42210 & 1980 & -2000 \\
-1350 & 44210 & 1960 & -3340 \\
1980 & -2000 & 630 & 42210 \\
1960 & -3340 & -1350 & 44210 \\
\end{bmatrix}
\]

\[
I^{(4)} = \begin{bmatrix}
1 & 0 & 0 & 0 \\
0 & 1 & 0 & 0 \\
0 & 0 & 1 & 0 \\
0 & 0 & 0 & 1 \\
\end{bmatrix}
\]

The following table shows the results for the \( O_1 \) set.

<table>
<thead>
<tr>
<th>N</th>
<th>Det</th>
<th>TYPE</th>
<th>SIGN</th>
<th>Index</th>
<th>Binary index</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>-3.523500e+06</td>
<td>( O^{bc} )</td>
<td>NEG!</td>
<td>5</td>
<td>[0,1,0,1]</td>
</tr>
<tr>
<td>1</td>
<td>3.17723e+07</td>
<td>( O^{mix} )</td>
<td>...POS</td>
<td>6</td>
<td>[0,1,1,0]</td>
</tr>
<tr>
<td>2</td>
<td>3.17723e+07</td>
<td>( O^{mix} )</td>
<td>...POS</td>
<td>9</td>
<td>[1,0,0,1]</td>
</tr>
<tr>
<td>3</td>
<td>1.943368e+09</td>
<td>( O^{bc} )</td>
<td>...POS</td>
<td>10</td>
<td>[1,0,1,0]</td>
</tr>
</tbody>
</table>

These results can be summarized as:

\[
\begin{array}{|c||c|c|c|c|}
\hline
\text{Total} & \text{O items} \\
\hline
\text{nega} & \text{bc} & \text{mix} & \text{bc} \\
\hline
1 & 0 & 0 & 1 \\
3 & 1 & 2 & 0 \\
\hline
\end{array}
\]

- 2. The second juxtaposed set to be formed is \( O_2(R_{22}, I^{(4)}) \), corresponding to the subcircuit containing transistors Q₁ and Q₄:

\[
R_{22} = \begin{bmatrix}
630 & 42210 & 1980 & -2000 \\
-1350 & 44210 & 1960 & -3340 \\
1980 & -2000 & 630 & 42210 \\
1960 & -3340 & -1350 & 44210 \\
\end{bmatrix}
\]

\[
I^{(4)} = \begin{bmatrix}
1 & 0 & 0 & 0 \\
0 & 1 & 0 & 0 \\
0 & 0 & 1 & 0 \\
0 & 0 & 0 & 1 \\
\end{bmatrix}
\]

Analysis of this subset yields:

<table>
<thead>
<tr>
<th>N</th>
<th>Det</th>
<th>TYPE</th>
<th>SIGN</th>
<th>Index</th>
<th>Binary index</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>-3.523500e+06</td>
<td>( O^{bc} )</td>
<td>NEG!</td>
<td>5</td>
<td>[0,1,0,1]</td>
</tr>
<tr>
<td>1</td>
<td>3.177230e+07</td>
<td>( O^{mix} )</td>
<td>...POS</td>
<td>6</td>
<td>[0,1,1,0]</td>
</tr>
<tr>
<td>2</td>
<td>3.177230e+07</td>
<td>( O^{mix} )</td>
<td>...POS</td>
<td>9</td>
<td>[1,0,0,1]</td>
</tr>
<tr>
<td>3</td>
<td>1.943368e+09</td>
<td>( O^{bc} )</td>
<td>...POS</td>
<td>10</td>
<td>[1,0,1,0]</td>
</tr>
</tbody>
</table>
These results can be summarized as:

<table>
<thead>
<tr>
<th>negs</th>
<th>0 bc</th>
<th>0 mix</th>
<th>0 be</th>
</tr>
</thead>
<tbody>
<tr>
<td>pos</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>3</td>
<td>1</td>
<td>2</td>
<td>0</td>
</tr>
</tbody>
</table>

Once the analysis of each separated subset has been done, a summary of both results can be set in the next table:

<table>
<thead>
<tr>
<th>negs</th>
<th>0 bc</th>
<th>0 mix</th>
<th>0 be</th>
</tr>
</thead>
<tbody>
<tr>
<td>pos</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>2</td>
<td>0</td>
<td>0</td>
<td>2</td>
</tr>
<tr>
<td>6</td>
<td>2</td>
<td>4</td>
<td>0</td>
</tr>
</tbody>
</table>

From the results above, it can be concluded that two separated feedback structures arise, which causes that three possible solutions may appear for each one. This leads to the fact that a total of nine possible solutions for the whole circuit may appear. The figure 6.7 shows schematically the nine solutions as a combination of the three solutions obtained for each subcircuit.

\[\text{2The unit matrix here is also partitioned and with dimensions } 4 \times 4\]
### 6-4. REFLECTED FLIP-FLOP CIRCUIT

#### 6-4-2 Finding the solutions

<table>
<thead>
<tr>
<th>Solution #</th>
<th>( s )</th>
<th>( i )</th>
<th>eigenvalues of ( RT_d + I )</th>
<th>( \det (RT_d + I) )</th>
</tr>
</thead>
<tbody>
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<td>1</td>
<td>0.765999</td>
<td>-0.00611763</td>
<td>1 0</td>
<td>1.82986\times10</td>
</tr>
<tr>
<td></td>
<td>0.644632</td>
<td>0.00593932</td>
<td>223.73 291.92</td>
<td></td>
</tr>
<tr>
<td></td>
<td>0.121367</td>
<td>-1.05416e-13</td>
<td>223.73 -291.92</td>
<td></td>
</tr>
<tr>
<td></td>
<td>-11.522</td>
<td>1.06362e-13</td>
<td>223.73 291.92</td>
<td></td>
</tr>
<tr>
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<td>-0.00611763</td>
<td>223.73 -291.92</td>
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</tr>
<tr>
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<td>0.00593932</td>
<td>223.73 291.92</td>
<td></td>
</tr>
<tr>
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<td>-1.05416e-13</td>
<td>223.73 -291.92</td>
<td></td>
</tr>
<tr>
<td></td>
<td>-11.522</td>
<td>1.06362e-13</td>
<td>223.73 291.92</td>
<td></td>
</tr>
<tr>
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<td>0.121367</td>
<td>-1.05416e-13</td>
<td>1 0</td>
<td>1.82986\times10</td>
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<tr>
<td></td>
<td>-11.522</td>
<td>1.06362e-13</td>
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</tr>
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<td>223.73 -291.92</td>
<td></td>
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<tr>
<td></td>
<td>-11.522</td>
<td>1.06362e-13</td>
<td>223.73 291.92</td>
<td></td>
</tr>
<tr>
<td>3_{(unstable)}</td>
<td>0.756636</td>
<td>-0.0043078</td>
<td>1 0</td>
<td>-1.30558\times10</td>
</tr>
<tr>
<td></td>
<td>-2.62776</td>
<td>0.00426472</td>
<td>1 0</td>
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<td>0.765999</td>
<td>-0.0043078</td>
<td>-222.074 0</td>
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<tr>
<td></td>
<td>-2.62776</td>
<td>0.00426472</td>
<td>433.437 0</td>
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<tr>
<td></td>
<td>-2.62776</td>
<td>0.00426472</td>
<td>-222.074 0</td>
<td></td>
</tr>
</tbody>
</table>
6-5 Nine solutions circuit

In this section the circuit reported in [1] is presented. Figure 6.8 shows the circuit, which is actually composed of two Schmitt trigger circuits connected back-to-back. The first circuit involves the upper part of the figure with the transistors Q₁ and Q₂, and the resistors \( R_{c1}, R_{c2}, R_{11}, R_{12}, R_{e1} \) and \( 2 \times R_{bb} \). The first step is to obtain the elements of the matrix \( G^{-1} \), which are related to the loops formed according to section 4-6. Because of the symmetry of this matrix, only the description of the elements on the upper triangular part of \( G^{-1} \) is given.

![Figure 6.8: Nine solutions circuit.](image-url)
In order to form the elements of this matrix, it is assumed that each voltage source is reduced to a short circuit (i.e. $E = 0$), and then we proceed to analyse all the loops formed at each of the BE and BC junctions. Firstly, the elements corresponding to the $2 \times 2$ blocks located on the main diagonal of $G^{-1}$ are to be found, which are related to a particular transistor. Because of the symmetrical structure of the circuit, the analysis is carried out for the upper part of the circuit (for the transistors $Q_1, Q_2$). The analysis of the lower part (for the transistors $Q_3, Q_4$) is done in a similar way:

- Block $R_{11(33)}$

  - Loop on the BE junction of $Q_{1(3)}$

    \[
    z_{11} = \frac{R_{e1} + R_{bb}[R_{nn} + (R_{s1} + R_{c2})][(R_{s2} + R_{c4})]}{
    R_{bb}[R_{nn} + (R_{s1} + R_{c2})][(R_{s2} + R_{c4})]}
    \]

    \[
    z_{55} = \frac{R_{e3} + R_{bb}[R_{nn} + (R_{s1} + R_{c2})][(R_{s2} + R_{c4})]}{
    R_{bb}[R_{nn} + (R_{s1} + R_{c2})][(R_{s2} + R_{c4})]}
    \]

  - Loop on the BC junction of $Q_{1(3)}$

    \[
    z_{22} = \frac{R_{e1}[R_{11} + R_{12}] + R_{bb}[R_{nn} + (R_{s1} + R_{c2})][(R_{s2} + R_{c4})]}{
    R_{bb}[R_{nn} + (R_{s1} + R_{c2})][(R_{s2} + R_{c4})]}
    \]

    \[
    z_{66} = \frac{R_{e3}[R_{21} + R_{22}] + R_{bb}[R_{nn} + (R_{s1} + R_{c2})][(R_{s2} + R_{c4})]}{
    R_{bb}[R_{nn} + (R_{s1} + R_{c2})][(R_{s2} + R_{c4})]}
    \]

It yields:

\[
    z_{12} = z_{21} = z_{11} \cap z_{22} = R_{bb}[R_{nn} + (R_{s1} + R_{c2})][(R_{s2} + R_{c4})]
    \]

\[
    z_{56} = z_{65} = z_{55} \cap z_{66} = R_{bb}[R_{nn} + (R_{s1} + R_{c2})][(R_{s2} + R_{c4})]
    \]
- Loop on the BE junction of $Q_{2(4)}$

\[ z_{33} = R_{e1} + [R_{12}|| (R_{11} + R_{c1})] \]
\[ z_{77} = R_{e3} + [R_{22}|| (R_{21} + R_{c3})] \]

- Loop on the BC junction of $Q_{2(4)}$

\[ z_{44} = R_{12}||(R_{11} + R_{c1}) + R_{e2}||(R_{e2} + R_{c3})||(R_{nn} + R_{bb}) \]
\[ z_{88} = R_{22}||(R_{21} + R_{c3}) + R_{e4}||(R_{e2} + (R_{e1} + R_{c2})||(R_{nn} + R_{bb}) \]

It yields:

\[ z_{34} = z_{43} = z_{33} \cap z_{44} = R_{12}||(R_{11} + R_{c1}) \]
\[ z_{78} = z_{87} = z_{77} \cap z_{88} = R_{22}||(R_{21} + R_{c3}) \]

Now the analysis of the crossed elements will be carried out; i.e. those blocks outside the main diagonal which actually represent the possible interconnection between two transistors.
Block $\mathbf{R}_{12} = \begin{bmatrix} z_{13} & z_{14} \\ z_{23} & z_{24} \end{bmatrix}$:

- Loops on the BE junction of $Q_1$ and the BE junction of $Q_2$
  $z_{13} = z_{11} \cap z_{33} = R_{e1}$

- Loops on the BE junction of $Q_1$ and the BC junction of $Q_2$
  $z_{14} = z_{11} \cap z_{44} = \frac{R_{c2} R_{bb} [(R_{s1} + R_{c2})((R_{s2} + R_{c4})]}{R_{s1} + R_{c2} R_{bb} + (R_{s1} + R_{c2})((R_{s2} + R_{c4})} + R_{nn}$

- Loops on the BC junction of $Q_1$ and the BE junction of $Q_2$
  $z_{23} = z_{22} \cap z_{33} = \frac{R_{12} R_{c1}}{R_{11} + R_{12} + R_{c1}}$

- Loops on the BC junction of $Q_1$ and the BC junction of $Q_2$
  $z_{24} = z_{22} \cap z_{44} = \frac{R_{12} R_{c1}}{R_{11} + R_{12} + R_{c1}} + \frac{R_{c2} R_{bb} [(R_{s1} + R_{c2})((R_{s2} + R_{c4})]}{R_{s1} + R_{c2} R_{bb} + (R_{s1} + R_{c2})((R_{s2} + R_{c4})} + R_{nn}$
Block $R_{13} = \begin{bmatrix} z_{15} & z_{16} \\ z_{25} & z_{26} \end{bmatrix}$:

- Loops on the BE junction of $Q_1$ and the BE junction of $Q_3$
  $z_{15} = z_{11} \cap z_{55} = R_{bb} || [R_{nn} + (R_{s1} + R_{c2})] || (R_{s2} + R_{c4})$

- Loops on the BE junction of $Q_1$ and the BC junction of $Q_3$
  $z_{16} = z_{11} \cap z_{66} = R_{bb} || [R_{nn} + (R_{s1} + R_{c2})] || (R_{s2} + R_{c4})$

- Loops on the BC junction of $Q_1$ and the BE junction of $Q_3$
  $z_{25} = z_{22} \cap z_{55} = R_{bb} || [R_{nn} + (R_{s1} + R_{c2})] || (R_{s2} + R_{c4})$

- Loops on the BC junction of $Q_1$ and the BC junction of $Q_3$
  $z_{26} = z_{22} \cap z_{66} = R_{bb} || [R_{nn} + (R_{s1} + R_{c2})] || (R_{s2} + R_{c4})$
Block $R_{14} = \begin{bmatrix} z_{17} & z_{18} \\ z_{27} & z_{28} \end{bmatrix}$:

- Loops on the BE junction of $Q_1$ and the BE junction of $Q_4$
  $z_{17} = z_{11} \cap z_{77} = 0$

- Loops on the BE junction of $Q_1$ and the BC junction of $Q_4$
  $z_{18} = z_{11} \cap z_{88} = \frac{R_{c4}}{R_{s2}+R_{c4}} \frac{R_{bb}((R_{s1}+R_{c2})||(R_{s2}+R_{c4}))}{R_{bb}+(R_{s1}+R_{c2})||(R_{s2}+R_{c4})} + R_{nn}$

- Loops on the BC junction of $Q_1$ and the BE junction of $Q_4$
  $z_{27} = z_{22} \cap z_{77} = 0$

- Loops on the BC junction of $Q_1$ and the BC junction of $Q_4$
  $z_{28} = z_{22} \cap z_{88} = \frac{R_{c4}}{R_{s2}+R_{c4}} \frac{R_{bb}((R_{s1}+R_{c2})||(R_{s2}+R_{c4}))}{R_{bb}+(R_{s1}+R_{c2})||(R_{s2}+R_{c4})} + R_{nn}$
Block $R_{23} = \begin{bmatrix} z_{35} & z_{36} \\ z_{45} & z_{46} \end{bmatrix}$:

- Loops on the BE junction of $Q_2$ and the BE junction of $Q_3$
  $z_{35} = z_{33} \cap z_{55} = 0$

- Loops on the BE junction of $Q_2$ and the BC junction of $Q_3$
  $z_{36} = z_{33} \cap z_{66} = 0$

- Loops on the BC junction of $Q_2$ and the BE junction of $Q_3$
  $z_{45} = z_{44} \cap z_{55} = R_{bb} || [R_{nn} + (R_{s1} + R_{c2})][(R_{s2} + R_{c4})]$

- Loops on the BC junction of $Q_2$ and the BC junction of $Q_3$
  $z_{46} = z_{44} \cap z_{66} = R_{bb} || [R_{nn} + (R_{s1} + R_{c2})][(R_{s2} + R_{c4})]$
Block $R_{24} = \begin{bmatrix} z_{37} & z_{38} \\ z_{47} & z_{48} \end{bmatrix}$.

- Loops on the BE junction of $Q_2$ and the BE junction of $Q_4$
  $z_{37} = z_{33} \cap z_{77} = 0$

- Loops on the BE junction of $Q_2$ and the BC junction of $Q_4$
  $z_{38} = z_{33} \cap z_{88} = 0$

- Loops on the BC junction of $Q_2$ and the BE junction of $Q_4$
  $z_{45} = z_{44} \cap z_{77} = 0$

- Loops on the BC junction of $Q_2$ and the BC junction of $Q_4$
  $z_{48} = z_{44} \cap z_{88} = \frac{R_{c2}R_{c4}(R_{nn}+R_{bb})}{[(R_{s1}+R_{e2})+(R_{s2}+R_{e4})](R_{nn}+R_{bb})+(R_{s1}+R_{e2})(R_{s2}+R_{e4})}$
Block \( R_{34} = \begin{bmatrix} z_{67} & z_{68} \\ z_{67} & z_{68} \end{bmatrix} \):

- Loops on the BE junction of \( Q_3 \) and the BE junction of \( Q_4 \)
  \( z_{57} = z_{55} \cap z_{77} = R_{e3} \)

- Loops on the BE junction of \( Q_3 \) and the BC junction of \( Q_4 \)
  \( z_{58} = z_{55} \cap z_{88} = \frac{R_{c4}}{R_{e2} + R_{c4}} \cdot \frac{R_{bb}((R_{s1} + R_{c2})||((R_{e2} + R_{c4}) \cap R_{nn}))}{R_{bb} + ((R_{s1} + R_{c2})||((R_{e2} + R_{c4}) \cap R_{nn}))} \)

- Loops on the BC junction of \( Q_3 \) and the BE junction of \( Q_4 \)
  \( z_{65} = z_{66} \cap z_{77} = \frac{R_{e1} R_{c1}}{R_{e1} + R_{e2} + R_{e3}} \)

- Loops on the BC junction of \( Q_3 \) and the BC junction of \( Q_4 \)
  \( z_{68} = z_{66} \cap z_{88} = \frac{R_{e3} R_{c3}}{R_{e2} + R_{e2} + R_{c3}} + \frac{R_{c4}}{R_{e2} + R_{c4}} \cdot \frac{R_{bb}((R_{s1} + R_{c2})||((R_{e2} + R_{c4}) \cap R_{nn}))}{R_{bb} + ((R_{s1} + R_{c2})||((R_{e2} + R_{c4}) \cap R_{nn}))} \)
The following are some of the involved matrices of the circuit:

- The transformation matrix:

\[
K = \begin{bmatrix}
0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\
0 & 1 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\
0 & 0 & 0 & 1 & 0 & 0 & 0 & 0 & 0 \\
0 & 0 & -1 & -1 & 0 & 0 & 0 & 0 & 0 \\
1 & 0 & 1 & 0 & 0 & 0 & 0 & 0 & 0 \\
-1 & -1 & 0 & 0 & -1 & -1 & 0 & 0 & 0 \\
0 & 0 & 0 & 0 & 1 & 0 & 1 & 0 & 0 \\
0 & 0 & 0 & 0 & 0 & 1 & 0 & 0 & 0 \\
0 & 0 & 0 & 0 & 0 & 0 & -1 & -1 & 0 \\
0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\
0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 1 \\
0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\
0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\
0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\
0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\
0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0
\end{bmatrix}
\]

- The transistor matrix:

\[
T = \begin{bmatrix}
1 & -\alpha_1^{(q_1)} & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\
-\alpha_f^{(q_1)} & 1 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\
0 & 0 & 1 & -\alpha_r^{(q_2)} & 0 & 0 & 0 & 0 & 0 \\
0 & 0 & -\alpha_f^{(q_2)} & 1 & 0 & 0 & 0 & 0 & 0 \\
0 & 0 & 0 & 0 & 1 & -\alpha_r^{(q_3)} & 0 & 0 & 0 \\
0 & 0 & 0 & 0 & 0 & -\alpha_f^{(q_3)} & 1 & 0 & 0 \\
0 & 0 & 0 & 0 & 0 & 0 & 0 & 1 & -\alpha_r^{(q_4)} \\
0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & -\alpha_f^{(q_4)}
\end{bmatrix}
\]

- Numerical $G^{-1}$ matrix:

\[
G^{-1} = KY^{-1}MNA_{tin}K^T = 
\begin{bmatrix}
4718.75 & 4218.75 & 500 & -312.5 & 4218.75 & 4218.75 & 0 & -312.5 \\
4218.75 & 7855.94 & -916.1 & -1228.6 & 4218.75 & 4218.75 & 0 & -312.5 \\
500 & -916.1 & 8286.85 & 7786.85 & 0 & 0 & 0 & 0 \\
-312.5 & -1228.6 & 7786.85 & 11426.6 & -312.5 & -312.5 & 0 & 110.294 \\
4218.75 & 4218.75 & 0 & -312.5 & 4718.75 & 4218.75 & 500 & -312.5 \\
4218.75 & 4218.75 & 0 & -312.5 & 4218.75 & 7855.94 & -916.1 & -1228.6 \\
0 & 0 & 0 & 0 & 500 & -916.1 & 8286.85 & 7786.85 \\
-312.5 & -312.5 & 0 & 110.294 & -312.5 & -1228.6 & 7786.85 & 11426.6
\end{bmatrix}
\]
- Numerical $R'$ matrix:

$$R' = G^{-1}T = \begin{bmatrix}
584.375 & 2661.56 & 806.25 & -477.5 & 84.375 & 2826.56 & 306.25 & -312.5 \\
-3480.07 & 6463.75 & 287.928 & -926.287 & 84.375 & 2826.56 & 306.25 & -312.5 \\
1397.78 & -1081.1 & 655.737 & 5052.19 & 0 & 0 & 0 & 0 \\
891.528 & -1125.47 & -3411.17 & 8856.89 & -6.25 & -209.375 & -108.088 & 110.294 \\
84.375 & 2826.56 & 306.25 & -312.5 & 584.375 & 2661.56 & 806.25 & -477.5 \\
84.375 & 2826.56 & 306.25 & -312.5 & -3480.07 & 6463.75 & 287.928 & -926.287 \\
0 & 0 & 0 & 0 & 1397.78 & -1081.1 & 655.737 & 5052.19 \\
-6.25 & -209.375 & -108.088 & 110.294 & 891.528 & -1125.47 & -3411.17 & 8856.89
\end{bmatrix}$$

Analysis of juxtaposed set $O(R' = G^{-1}T, I)$:

The structure of the matrix $R'$ shows that the last two column-pairs (i.e., those corresponding to transistors $Q_3$ and $Q_4$) have identical disconnection blocks, which allows to make a first partitioning.

- For the 1st pair: Analysis of juxtaposed set $O(R'_a, I_a)$

List of transistors: $Q_3, Q_4$

$$R'_a = \begin{bmatrix}
584.375 & 2661.56 & 806.25 & -477.5 \\
-3480.07 & 6463.75 & 287.928 & -926.287 \\
1397.78 & -1081.1 & 655.737 & 5052.19 \\
891.528 & -1125.47 & -3411.17 & 8856.89
\end{bmatrix}$$

$$I_a = \begin{bmatrix}
1 & 0 & 0 & 0 \\
0 & 1 & 0 & 0 \\
0 & 0 & 1 & 0 \\
0 & 0 & 0 & 1
\end{bmatrix}$$

Table with analysis of elements $\in O_a$ set:

<table>
<thead>
<tr>
<th>N</th>
<th>Det</th>
<th>TYPE</th>
<th>SIGN</th>
<th>Index</th>
<th>Binary index</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>-7.437620e+05</td>
<td>$O^b$</td>
<td>NEG!</td>
<td>5</td>
<td>[0,1,0,1]</td>
</tr>
<tr>
<td>1</td>
<td>5.601452e+06</td>
<td>$O^{mix}$</td>
<td>_POS</td>
<td>6</td>
<td>[0,1,1,0]</td>
</tr>
<tr>
<td>2</td>
<td>4.549799e+06</td>
<td>$O^{mix}$</td>
<td>_POS</td>
<td>9</td>
<td>[1,0,0,1]</td>
</tr>
<tr>
<td>3</td>
<td>5.620624e+07</td>
<td>$O^b$</td>
<td>_POS</td>
<td>10</td>
<td>[1,0,1,0]</td>
</tr>
</tbody>
</table>

O Summary table for the partition $a$

<table>
<thead>
<tr>
<th>Total</th>
<th>$O^b$</th>
<th>$O^{mix}$</th>
<th>$O^b$</th>
</tr>
</thead>
<tbody>
<tr>
<td>neg</td>
<td>1</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>pos</td>
<td>3</td>
<td>1</td>
<td>2</td>
</tr>
</tbody>
</table>
For the 2nd pair: Analysis of juxtaposed set $O(R'_b, I_b)$

List of transistors: $Q_1, Q_2$

$$R'_b = \begin{bmatrix}
584.375 & 2661.66 & 806.25 & -477.5 \\
-3480.07 & 6463.75 & 287.928 & -926.287 \\
1397.78 & -1081.1 & 655.737 & 5052.19 \\
891.528 & -1126.47 & -3411.17 & 8856.89
\end{bmatrix}$$

$$I_b = \begin{bmatrix}
1 & 0 & 0 & 0 \\
0 & 1 & 0 & 0 \\
0 & 0 & 1 & 0 \\
0 & 0 & 0 & 1
\end{bmatrix}$$

Table with analysis of elements $\in O_b$ set.

<table>
<thead>
<tr>
<th>N</th>
<th>Det</th>
<th>TYPE</th>
<th>SIGN</th>
<th>Index</th>
<th>Binary index</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>-7.437620e+05</td>
<td>$O^{bc}$</td>
<td>NEG!</td>
<td>5</td>
<td>[0,1,0,1]</td>
</tr>
<tr>
<td>1</td>
<td>5.601452e+06</td>
<td>$O^{mix}$</td>
<td>_POS</td>
<td>6</td>
<td>[0,1,1,0]</td>
</tr>
<tr>
<td>2</td>
<td>4.549799e+06</td>
<td>$O^{mix}$</td>
<td>_POS</td>
<td>9</td>
<td>[1,0,0,1]</td>
</tr>
<tr>
<td>3</td>
<td>5.620624e+07</td>
<td>$O^{bc}$</td>
<td>_POS</td>
<td>10</td>
<td>[1,0,1,0]</td>
</tr>
</tbody>
</table>

**O Summary table for the partition $b$**

<table>
<thead>
<tr>
<th>neg pos</th>
<th>$O^{bc}$</th>
<th>$O^{mix}$</th>
<th>$O^{bc}$</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>0</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>3</td>
<td>1</td>
<td>2</td>
<td>0</td>
</tr>
</tbody>
</table>

A table with the combined results from both partitioning stages is shown as follows:

**O Summary table**

<table>
<thead>
<tr>
<th>Total</th>
<th>$O_-$ items</th>
</tr>
</thead>
<tbody>
<tr>
<td>neg pos</td>
<td>$O^{bc}$</td>
</tr>
<tr>
<td>2</td>
<td>0</td>
</tr>
<tr>
<td>6</td>
<td>2</td>
</tr>
</tbody>
</table>

In this form two independent feedback structures have been found which means that three independent solutions for each subcircuit occur. In this form an upper bound in the number of possible solutions can be given, the maximum number is thus 9 operating points.
<table>
<thead>
<tr>
<th>Solution #</th>
<th>[ \begin{pmatrix} 2.195e-3 &amp; -0.3611 \ 8.391e-3 &amp; -0.3611 \ 3.970e-3 &amp; -0.3655 \ 8.419e-3 &amp; -0.3625 \end{pmatrix} ]</th>
<th>[ \begin{pmatrix} 38.876 &amp; 0 \ 126.150 &amp; 0 \ -264.524 &amp; \pm j214.431 \ -179.466 &amp; \pm j192.387 \ 191.793 &amp; \pm j185.157 \end{pmatrix} ]</th>
<th>[ \begin{pmatrix} 10.084 &amp; 0 \ 131.261 &amp; 0 \ 232.213 &amp; \pm j120.062 \ 192.813 &amp; \pm j610.863 \end{pmatrix} ]</th>
<th>[ \begin{pmatrix} 2.1879e18 \end{pmatrix} ]</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>[ \begin{pmatrix} -0.3366 \ 4.178e-3 \ -0.3615 \ 4.737e-3 \ 3.5251 \ 8.419 \end{pmatrix} ]</td>
<td>[ \begin{pmatrix} 47.041 &amp; 0 \ 246.431 &amp; 0 \ 204.733 &amp; \pm j261.064 \ 212.431 &amp; \pm j310.672 \end{pmatrix} ]</td>
<td>[ \begin{pmatrix} 1 \end{pmatrix} ]</td>
<td>[ \begin{pmatrix} 12.783e12 \end{pmatrix} ]</td>
</tr>
<tr>
<td>2</td>
<td>[ \begin{pmatrix} -0.3245 \ 2.876e-3 \ -0.3711 \ 7.302e-3 \ 1.1037 \ 3.9760 \ -0.3775 \ 7.518e-3 \end{pmatrix} ]</td>
<td>[ \begin{pmatrix} 181.774e12 \end{pmatrix} ]</td>
<td>[ \begin{pmatrix} 1 \end{pmatrix} ]</td>
<td>[ \begin{pmatrix} 0 \end{pmatrix} ]</td>
</tr>
<tr>
<td>3</td>
<td>[ \begin{pmatrix} -0.3859 \ 2.201e-3 \ 4.3110 \ 3.9329 \ -0.3483 \ 3.970e-3 \ -0.3577 \ 5.415e-3 \end{pmatrix} ]</td>
<td>[ \begin{pmatrix} 46.050e12 \end{pmatrix} ]</td>
<td>[ \begin{pmatrix} 1 \end{pmatrix} ]</td>
<td>[ \begin{pmatrix} 1 \end{pmatrix} ]</td>
</tr>
<tr>
<td>4</td>
<td>[ \begin{pmatrix} -0.3384 \ 2.047e-3 \ 3.7922 \ 8.4939 \ -0.3808 \ 3.887e-3 \ -0.3577 \ 8.385 \end{pmatrix} ]</td>
<td>[ \begin{pmatrix} 180.708 &amp; \pm j392.037 \end{pmatrix} ]</td>
<td>[ \begin{pmatrix} 1 \end{pmatrix} ]</td>
<td>[ \begin{pmatrix} 1 \end{pmatrix} ]</td>
</tr>
<tr>
<td>5</td>
<td>[ \begin{pmatrix} -0.3879 \ 2.076e-3 \ 4.92 \ 8.760 \ 1.520 \end{pmatrix} ]</td>
<td>[ \begin{pmatrix} -2.597e9 \end{pmatrix} ]</td>
<td>[ \begin{pmatrix} 1 \end{pmatrix} ]</td>
<td>[ \begin{pmatrix} 1 \end{pmatrix} ]</td>
</tr>
<tr>
<td>6</td>
<td>[ \begin{pmatrix} 0.7119 \ 2.185e-1 \ -0.3775 \ 8.304e-3 \ -0.3557 \end{pmatrix} ]</td>
<td>[ \begin{pmatrix} 0 \end{pmatrix} ]</td>
<td>[ \begin{pmatrix} 1 \end{pmatrix} ]</td>
<td>[ \begin{pmatrix} 1 \end{pmatrix} ]</td>
</tr>
<tr>
<td>7</td>
<td>[ \begin{pmatrix} 0.5166 \ 3.058e-1 \ -0.3775 \ 8.41e-3 \end{pmatrix} ]</td>
<td>[ \begin{pmatrix} 1 \end{pmatrix} ]</td>
<td>[ \begin{pmatrix} 1 \end{pmatrix} ]</td>
<td>[ \begin{pmatrix} 1 \end{pmatrix} ]</td>
</tr>
<tr>
<td>8</td>
<td>[ \begin{pmatrix} 0.3974 \ 7.803e-3 \end{pmatrix} ]</td>
<td>[ \begin{pmatrix} -209.585 &amp; \pm j355.760 \end{pmatrix} ]</td>
<td>[ \begin{pmatrix} 1 \end{pmatrix} ]</td>
<td>[ \begin{pmatrix} 1 \end{pmatrix} ]</td>
</tr>
<tr>
<td>9</td>
<td>[ \begin{pmatrix} 0 \end{pmatrix} ]</td>
<td>[ \begin{pmatrix} -196.623 &amp; \pm j224.92 \end{pmatrix} ]</td>
<td>[ \begin{pmatrix} 1 \end{pmatrix} ]</td>
<td>[ \begin{pmatrix} 1 \end{pmatrix} ]</td>
</tr>
</tbody>
</table>

The unstable solutions are those in which the real part of the eigenvalues of \[ [RTd + I] \] is negative.

### 6-6 Current source

Reference circuits constitute one of the most frequently used kind of circuit in electronics, with several applications such as use in stabilized
power supplies and instrumentation circuits. In this section, a current source is presented [4]. The circuit is depicted on fig. 6.9. The dashed part can be seen as a composed resistor. This resistor exhibits the behavior of a negative resistor device.

Matrices from $2Q$–representation

The circuit is depicted in another form on fig. 6.10, in order to show the $2Q$–representation.

From this representation, several involved matrices can be given:
Figure 6.10: Current source: $2Q$ - representation.
• The MNA matrix of the linear part of the circuit:

\[
Y_{\text{MNA}_{\text{lin}}} = \begin{bmatrix}
\frac{1}{r_{ee}} & -\frac{1}{r_{ee}} & 0 & 0 & 0 & 0 & 0 & 1 & 0 \\
-\frac{1}{r_{ee}} & \frac{1}{r_{ee}} & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\
0 & 0 & \frac{1}{r_{\infty}} & 0 & 0 & 0 & 0 & 1 & 0 \\
0 & 0 & 0 & \frac{1}{r_{\infty}} & 0 & 0 & 0 & 0 & 0 \\
0 & 0 & 0 & 0 & \frac{1}{r_{p}} & 0 & 0 & 0 & 0 \\
0 & 0 & 0 & 0 & 0 & \frac{1}{r_{p}} & 0 & 0 & 0 \\
1 & 0 & 0 & 0 & 0 & 0 & \frac{1}{r_{p}} & 0 & 0 \\
0 & 0 & 0 & 1 & 0 & 0 & -1 & 0 & \frac{1}{r_{\infty}}
\end{bmatrix}
\]

• Numerical \(Y_{\text{MNA}_{\text{lin}}}^{-1}\) matrix:

\[
Y_{\text{MNA}_{\text{lin}}}^{-1} = \begin{bmatrix}
0 & 0 & 0 & 0 & 0 & 0 & 0 & 1 & 0 \\
0 & \frac{1}{r_{ee}} & 0 & 0 & 0 & 0 & 0 & 1 & 0 \\
0 & 0 & \frac{1}{r_{\infty}} & 0 & 0 & 0 & 0 & 0 & 0 \\
0 & 0 & 0 & \frac{1}{r_{\infty}} & 0 & 0 & 0 & 0 & 0 \\
0 & 0 & 0 & 0 & \frac{1}{r_{\infty}} & 0 & 0 & 0 & 0 \\
0 & 0 & 0 & \frac{1}{r_{p}} & 0 & 0 & 0 & 0 & 0 \\
0 & 0 & 0 & \frac{1}{r_{p}} & 0 & 0 & 0 & 0 & 0 \\
1 & 1 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\
0 & 0 & 0 & 0.5 & 0 & 0 & -0.5 & 0 & -5e-13
\end{bmatrix}
\]

• The transformation matrix:

\[
K = \begin{bmatrix}
0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\
1 & 0 & 1 & 0 & 0 & 0 & 0 & 0 & 0 \\
-1 & -1 & -1 & -1 & 0 & 0 & 0 & 0 & 1 \\
0 & 1 & 0 & 0 & 0 & 1 & 0 & 0 & 0 \\
0 & 0 & 0 & 1 & 0 & 0 & 0 & 1 & -1 \\
0 & 0 & 0 & 0 & 1 & 0 & 0 & 0 & 0 \\
0 & 0 & 0 & 0 & -1 & -1 & -1 & -1 & 0 \\
0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\
0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0
\end{bmatrix}
\]
• The transistor matrix:

\[
T = \begin{bmatrix}
1 & -\alpha_r^{(1)} & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\
-\alpha_f^{(1)} & 1 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\
0 & 0 & 1 & -\alpha_r^{(2)} & 0 & 0 & 0 & 0 & 0 \\
0 & 0 & -\alpha_f^{(2)} & 1 & 0 & 0 & 0 & 0 & 0 \\
0 & 0 & 0 & 0 & 1 & -\alpha_r^{(3)} & 0 & 0 & 0 \\
0 & 0 & 0 & 0 & -\alpha_f^{(3)} & 1 & 0 & 0 & 0 \\
0 & 0 & 0 & 0 & 0 & 0 & 1 & -\alpha_r^{(4)} & 0 \\
0 & 0 & 0 & 0 & 0 & 0 & -\alpha_f^{(4)} & 1 & 0 \\
0^* & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 1 \\
0 & 0 & 0 & 0 & 0 & 0 & 0 & -\alpha_f^{(5)} & 1
\end{bmatrix}
\]

\[
R' = G^{-1} T = \begin{bmatrix} R_a & R_b \\ R_c & R_d \end{bmatrix}
\]

where:

\[
R_a = \begin{bmatrix}
1.2346e+10 & 7.693e+10 & 1.2346e+10 & 7.693e+10 & 1.2346e+10 & 7.693e+10 & 0 \\
-4.81481e+11 & 5.7693e+11 & 1.2346e+10 & 7.693e+10 & 1.2346e+10 & 7.693e+10 & -5e+11 \\
1.2346e+10 & 7.693e+10 & 1.2346e+10 & 7.693e+10 & 1.2346e+10 & 7.693e+10 & 0 \\
1.2346e+10 & 7.693e+10 & -9.75308e+11 & 1.07693e+12 & 0 & 0 & 5e+11 \\
4.93827e+11 & -5e+11 & 0 & 0 & 0 & 0 & 0
\end{bmatrix}
\]

\[
R_b = \begin{bmatrix}
0 & 0 & 0 & 9.9e+11 & -1e+12 \\
1.665e+11 & -5e+09 & -3.335e+11 & 9.9e+11 & -1e+12 \\
0 & 0 & 0 & 9.9e+11 & -1e+12 \\
0 & -9.9e+11 & 1e+12 & 9.8e+11 & -1.667e+12 \\
-1.665e+11 & 5e+09 & 3.335e+11 & 0 & 0
\end{bmatrix}
\]

\[
R_c = \begin{bmatrix}
0 & 0 & 0 & 0 & 0 & 0 & 0 \\
4.93827e+11 & -5e+11 & 0 & 0 & 0 & 0 & 0 \\
4.93827e+11 & -5e+11 & -9.87654e+11 & 1e+12 & 0 & 0 & 0 \\
0 & 0 & 0 & 0 & 0 & 0 & 0 \\
-1.2346e+10 & -7.693e+10 & 9.75308e+11 & -1.07693e+12 & 0 & 0
\end{bmatrix}
\]

\[
R_d = \begin{bmatrix}
0 & 0 & 0 & 0 & 0 \\
-1.665e+11 & 5e+09 & 3.335e+11 & 0 & 0 \\
-1.665e+11 & -9.85e+11 & 1.3335e+12 & -1e+10 & -6.67e+11 \\
0 & 9.9e+11 & -1e+12 & 1e+10 & 0 & 0 & 0 \\
0 & 9.9e+11 & -1e+12 & -9.8e+11 & 1.667e+12 & 0
\end{bmatrix}
\]
6-6. CURRENT SOURCE

6-6-1 Analysis of the juxtaposed sets

The first step consists in forming the juxtaposed set of the following matrices: \( \mathcal{O} \left( R' = G^{-1} T, I \right) \).

The structure of the matrices allows us to apply the partitioning process, hence two smaller juxtaposed subsets is analyzed.

- 1. Forming \( \mathcal{O}_1(R_{11}, I^{(4)}) \), corresponding to the subcircuit containing transistors \( Q_2 \) and \( Q_5 \):

\[
R_{11} = \begin{bmatrix}
1.2346e+10 & 7.693e+10 & 9.9e+11 & -1e+12 \\
-9.75308e+11 & 1.07693e+12 & 9.8e+11 & -1.667e+12 \\
9.87654e+11 & -1e+12 & 1e+10 & 6.67e+11 \\
9.75308e+11 & -1.07693e+12 & -9.8e+11 & 1.667e+12 \\
\end{bmatrix}
\]

\[
I^{(4)} = \begin{bmatrix}
1 & 0 & 0 & 0 \\
0 & 1 & 0 & 0 \\
0 & 0 & 1 & 0 \\
0 & 0 & 0 & 1 \\
\end{bmatrix}
\]

The following table shows the results from analyzing the elements in the subset \( \mathcal{O}_1 \).

<table>
<thead>
<tr>
<th>N</th>
<th>Det</th>
<th>TYPE</th>
<th>SIGN</th>
<th>Index</th>
<th>Binary index</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>-9.776540e+23</td>
<td>( \mathcal{O}_{be} )</td>
<td>NEG!</td>
<td>5</td>
<td>[0,1,0,1]</td>
</tr>
<tr>
<td>1</td>
<td>9.958888e+23</td>
<td>( \mathcal{O}_{mix} )</td>
<td>_POS</td>
<td>6</td>
<td>[0,1,1,0]</td>
</tr>
<tr>
<td>2</td>
<td>9.907693e+23</td>
<td>( \mathcal{O}_{mix} )</td>
<td>_POS</td>
<td>9</td>
<td>[1,0,0,1]</td>
</tr>
<tr>
<td>3</td>
<td>0.000000e+00</td>
<td>( \mathcal{O}_{bc} )</td>
<td>_</td>
<td>10</td>
<td>[1,0,1,0]</td>
</tr>
</tbody>
</table>

Summary of the analysis of the first subset:

<table>
<thead>
<tr>
<th>negs</th>
<th>( \mathcal{O}_{bc} )</th>
<th>( \mathcal{O}_{mix} )</th>
<th>( \mathcal{O}_{be} )</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>0</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>3</td>
<td>1</td>
<td>2</td>
<td>0</td>
</tr>
</tbody>
</table>

It clearly results that the element \( \mathcal{O}_{be} \) is negative, consequently a negative feedback structure is constituted by transistors \( Q_2 \) and \( Q_5 \).
2. Forming $O_2(R_{22}, I^{(4)})$, corresponding to the subcircuit containing transistors $Q_1$ and $Q_4$:

$$R_{22} = \begin{bmatrix}
1.2346e + 10 & 7.693e + 10 & 0 & 0 \\
-4.81481e + 11 & 5.7693e + 11 & -5e + 09 & -3.335e + 11 \\
4.93827e + 11 & -5e + 11 & 5e + 09 & 3.335e + 11 \\
4.93827e + 11 & -5e + 11 & -9.85e + 11 & 1.3335e + 12
\end{bmatrix}$$

$$I^{(4)} = \begin{bmatrix}
1 & 0 & 0 & 0 \\
0 & 1 & 0 & 0 \\
0 & 0 & 1 & 0 \\
0 & 0 & 0 & 1
\end{bmatrix}$$

Table with analysis of elements $\in O_2$ set.

<table>
<thead>
<tr>
<th>N</th>
<th>Det</th>
<th>TYPE</th>
<th>SIGN</th>
<th>Index</th>
<th>Binary index</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>6.173003e+19</td>
<td>$O^{bc}$</td>
<td>_POS</td>
<td>5</td>
<td>[0,1,0,1]</td>
</tr>
<tr>
<td>1</td>
<td>1.646340e+22</td>
<td>$O^{mix}$</td>
<td>_POS</td>
<td>6</td>
<td>[0,1,1,0]</td>
</tr>
<tr>
<td>2</td>
<td>3.846500e+20</td>
<td>$O^{mix}$</td>
<td>_POS</td>
<td>9</td>
<td>[1,0,0,1]</td>
</tr>
<tr>
<td>3</td>
<td>6.025862e+23</td>
<td>$O^{bc}$</td>
<td>_POS</td>
<td>10</td>
<td>[1,0,1,0]</td>
</tr>
</tbody>
</table>

Summary of the second subset:

<table>
<thead>
<tr>
<th>Total</th>
<th>$O$ items</th>
</tr>
</thead>
<tbody>
<tr>
<td>$neg_1$ $pos$</td>
<td>$O^{bc}$</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>4</td>
<td>1</td>
</tr>
</tbody>
</table>

This table shows that the subcircuit formed by $Q_1$ and $Q_4$ does not possess a feedback structure, which leads to conclude that it cannot contribute to generate multiple solutions.

The following table shows a summary of the analysis from both juxtaposed subsets.

<table>
<thead>
<tr>
<th>Total</th>
<th>$O$ items</th>
</tr>
</thead>
<tbody>
<tr>
<td>$neg_1$ $pos$</td>
<td>$O^{bc}$</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>7</td>
<td>2</td>
</tr>
</tbody>
</table>
Hence, it is possible to conclude that a maximum of three solutions may be present.

6-6-2 Finding the solutions

The following table shows two solutions for the circuit, corresponding to the normal and latch-up operating points.

<table>
<thead>
<tr>
<th>Solution #</th>
<th>1</th>
<th>1</th>
<th>2</th>
<th>2</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>1.09218</td>
<td>1.07199e-07</td>
<td>1.05875e-07</td>
<td>1.07199e-07</td>
</tr>
<tr>
<td></td>
<td>-13.4284</td>
<td>-1.07199e-07</td>
<td>1.05875e-07</td>
<td>1.07199e-07</td>
</tr>
<tr>
<td></td>
<td>-13.9223</td>
<td>1.05875e-07</td>
<td>1.05875e-07</td>
<td>1.05875e-07</td>
</tr>
<tr>
<td></td>
<td>-0.493655</td>
<td>-8.21666e-08</td>
<td>-8.13351e-09</td>
<td>-8.21666e-08</td>
</tr>
<tr>
<td></td>
<td>0</td>
<td>2.73550e-08</td>
<td>2.73550e-08</td>
<td>2.73550e-08</td>
</tr>
<tr>
<td></td>
<td>-0.479365</td>
<td>-2.167e-08</td>
<td>-2.167e-08</td>
<td>-2.167e-08</td>
</tr>
<tr>
<td></td>
<td>-0.30381</td>
<td>2.15966e-15</td>
<td>2.15966e-15</td>
<td>2.15966e-15</td>
</tr>
<tr>
<td></td>
<td>13.8223</td>
<td>1.07199e-07</td>
<td>1.07199e-07</td>
<td>1.07199e-07</td>
</tr>
<tr>
<td></td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td></td>
<td>154312 ± j164350</td>
<td>50905.1</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td></td>
<td>2.54102e + 15</td>
<td>1.00021</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td></td>
<td>1.81836e + 18</td>
<td>1.00201</td>
<td>1</td>
<td>0</td>
</tr>
</tbody>
</table>

Bibliography


CHAPTER 7

Conclusions

This chapter is devoted to point out the main results of this work and to present a brief outline of possible further research on the subject.

7-1 Conclusions

In this thesis, the solution of the DC problem has been achieved by using an approach which makes use of the topology of the circuit to its full extent. A complete solution of the DC problem was stated, which covers the following aspects:

1. the uniqueness of the DC operating points
2. the upper bound on the number of DC operating points
3. the determination of all DC operating points and their stability

The aim of the work presented in this thesis has been to solve this problem for a large class of electronic circuits, namely circuits containing electronic devices like bipolar transistors. By representing the circuit through a model which separates the linear part from the nonlinear part, a partitioning-based method has been devised in order to solve the DC
problem. In this way, a systematical method of analysis based on a
topological criterion has been implemented to partition the circuit. In
addition, the use of the partitioning method permits us to reduce con-
siderably the number of calculations involved.

The description of the circuit is given by means of a pair of matrices:
the impedance matrix $R$ for the linear part of the circuit and the matrix
$T_q$ for the nonlinear part, i.e. the portion of the circuit containing the
transistors. The particular properties of both matrices (positive definite
and quasi block diagonal structure) serve to carry out the partitioning of
the circuit by partitioning the matrices. Because these matrices involve
information on the topology of the circuit, this partitioning is actually
carried out in a topology-based form.

Firstly, a result concerning the uniqueness of the DC operating point
has been obtained. This is done by testing if at least one element in
the juxtaposed (sub)set of matrices has negative value, which means
that the uniqueness is not guaranteed and the circuit possesses multiple
solutions. In executing the partitioning procedure, the testing is car-
rried out on matrices of steadily decreasing orders. This constitutes an
important achievement with respect to all previously developed meth-
ods in which a large number of calculations must be carried out in the
matrix-oriented methods ($2^{2q}$ determinants, $q$ being the number of tran-
sistors), or a large number of combinations of graphs must be tested in
the purely topologically oriented methods ($2^n$, $n$ being the number of
branches with nonmonotone increasing $i$-$v$ relationships). In the present
method, a significant reduction in the number of involved calculations
has been obtained, as a result of the implementation of the partitioning
procedure.

Secondly, this work is also focussed on solving the question of find-
ing the upper bound on the number of DC solutions. This bound is
determined after negative elements have been found in the juxtaposed
subsets. This step permits the identification of the portions of the circuit
containing negative feedback structures. As a consequence, a second re-
sult has been established, which permits the assessment of a maximum
of $3^f$ DC solutions for the whole circuit, where $f$ is the number of neg-
avative feedback structures found embedded in the circuit. Although the
method is able to deal only with a certain class of transistor circuits, this
work constitutes the first attempt — the first based on the combination of both topological and mathematical analysis — to solve the problem of determining an upper bound on the number of DC operating points for circuits with more than two transistors. For classes of transistor circuits that are not suited to the application of the partitioning procedure, the worst-case must be applied anyway; i.e. the analysis of the $2^q$ elements in the juxtaposed set of matrices $\mathcal{C}(\mathbf{T}_q, \mathbf{R})$, where $q$ is the number of transistors.

The existence of negative feedback structures implies that the transistors involved change of state for each of the DC solutions. This fact permits the assignment of a binary code to each one of the solutions to be searched. The method of search is thus started at values of junction voltages determined by the binary code corresponding to a particular solution. Not only does the method find the quantitative values of the electrical variables constituting the solutions, it is also able to determine whether the solutions are stable or unstable. This point is of primary importance for all circuit designers, because unstable DC solutions are worthless, in that they are unobservable in practice.

In summary, a systematical method has been developed to solve the DC problem for a class of transistor circuits. This class does not constitute the universe of the electronic circuits nor of transistor circuits, but for a large number of the transistor circuits used in electronics, this partitioning method is perfectly applicable.

7-2 Future research

The method used here for bipolar transistors can be extended in order to solve the same problem for circuits containing IGFETs o combinations of BJTs and IGFETs. The only requirement is that the model used for the nonlinear part contains strictly monotone increasing functions. In fact, the operating point of any IGFET can be modeled by a point lying on a line, which allows the use of the method here discussed in an almost straightforward form.

Another matter of interest for further research is the use of a more complex bipolar transistor model. Effects of variable $\alpha$'s could be, for instance, a topic for circuits with more than two transistors. In this case,
the complexity of the problem increases enormously, since it necessitates
the searching of the whole interval of variation of the $\alpha$'s. Among others,
bulk effects and Early voltage could also be matter of future studies.

The automatic recognition of some well-known transistor structures
in order to determine a priori the behavior of a particular section of the
circuit, and consequently to speed up the algorithm, constitutes another
issue for further work. In this form, a library of very commonly used
transistor structures (e.g. differential pair, cascode stages, Darlington-
like structures) can be stored and used to follow a heuristical method,
which allows us to obtain more reduction on the number of calculations.

Finally, the adaptation and application of this topological approach
to solve the problem of determining an upper bound on the number of DC
solutions for a more general class of nonlinear circuits (e.g. containing
devices modeled by non-monotone functions) could be also a challenging
item.
Appendix A

Introduction to juxtaposed sets

In this appendix we introduce the concept of $\mathcal{C}$ sets (or juxtaposed sets) in order to obtain a closed form for $\det [\mathbf{A} \mathbf{D} + \mathbf{B}]$ and to demonstrate the Theorem 4.1.

A-1 Some useful definitions

In this section we deal with juxtaposed sets. For each pair of real $n \times n$ matrices $(\mathbf{X}, \mathbf{Y})$, the set of matrices $\mathcal{C}(\mathbf{X}, \mathbf{Y})$ consists of all $n \times n$ matrices that can be constructed by juxtaposing columns taken either from $\mathbf{X}$ or $\mathbf{Y}$ while maintaining the original relative ordering of the columns. Clearly $\mathcal{C}(\mathbf{X}, \mathbf{Y})$ contains $2^n$ matrices.

A-1-1 Set $\theta = \mathcal{C}(\mathcal{D}, \mathcal{I})$

The definition of the most basic juxtaposed set ($\Delta = \mathcal{C}(\mathcal{I}, \phi)$) has been given in the chapter 4. Another important juxtaposed set corresponds to that formed when the identity and a diagonal matrix are involved. We denote it by:

$$\theta = \mathcal{C}(\mathcal{D}, \mathcal{I})$$  \hspace{1cm} (A.1)

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where \( I \) is the identity matrix and \( D = \text{diag} \left[ d_1, d_2, d_3, \ldots, d_{n-1}, d_n \right] \).

Each \( \theta_i \in \theta \) is given as\(^1\):

\[
\begin{align*}
\theta_0 &= \text{diag} \left[ d_1, d_2, d_3, \ldots, d_{n-1}, d_n \right] = D \\
\theta_1 &= \text{diag} \left[ d_1, d_2, d_3, \ldots, d_{n-1}, 1 \right] \\
\theta_2 &= \text{diag} \left[ d_1, d_2, d_3, \ldots, 1, d_n \right] \\
\theta_3 &= \text{diag} \left[ d_1, d_2, d_3, \ldots, 1, 1 \right] \\
&\quad \vdots \\
\theta_{2^n-1} &= \text{diag} \left[ d_1, 1, 1, \ldots, 1, 1 \right]
\end{align*}
\]

\[
\begin{align*}
\theta_{2^n-1} &= \text{diag} \left[ 1, 1, 1, \ldots, 1, 1 \right] = I \\
\theta_{2^n-2} &= \text{diag} \left[ 1, 1, 1, \ldots, 1, d_n \right] \\
\theta_{2^n-3} &= \text{diag} \left[ 1, 1, 1, \ldots, d_{n-1}, 1 \right] \\
\theta_{2^n-4} &= \text{diag} \left[ 1, 1, 1, \ldots, d_{n-1}, d_n \right] \\
&\quad \vdots \\
\theta_{2^n-1} &= \text{diag} \left[ 1, d_2, d_3, \ldots, d_{n-1}, d_n \right]
\end{align*}
\]

By combining this set of equations with the set \( \Delta = \mathcal{C} \left( I, \phi \right) \), it can be obtained:

\[
\begin{align*}
\theta_0 &= D \Delta_{2^n-1} + I \Delta_0 = D \\
\theta_1 &= D \Delta_{2^n-2} + I \Delta_1 \\
\theta_2 &= D \Delta_{2^n-3} + I \Delta_2 \\
\theta_3 &= D \Delta_{2^n-4} + I \Delta_3 \\
&\quad \vdots \\
\theta_{2^n-1} &= D \Delta_{2^n-1} + I \Delta_{2^n-1}
\end{align*}
\]

The elements \( \theta_a \) and \( \theta_b \), both \( \in \mathcal{C} \left( D, I \right) \), form a complementary pair when \( a + b = 2^n - 1 \). Then the pair is given by:

\[
\begin{align*}
\theta_a &= D \Delta_{2^n-1-a} + I \Delta_a \\
\theta_b &= D \Delta_{2^n-1-b} + I \Delta_b
\end{align*}
\]

or

\[
\begin{align*}
\theta_a &= D \Delta_{2^n-1-a} + I \Delta_a \\
\theta_b &= \theta_{2^n-1-a} = D \Delta_a + I \Delta_{2^n-1-a}
\end{align*}
\]

A pair is thus denoted by two matrices \( \theta_{\text{pair}} \left( \theta_a, \theta_{2^n-1-a} \right) \). Clearly:

\[
\theta_i \theta_{2^n-1-i} = D
\]

and

\[
\theta_i + \theta_{2^n-1-i} = I + D
\]

\(^1\)The elements of the juxtaposed set have been displayed in such a form, that the complementary-pair structure results more obvious.
A-1-2 Set $C = \mathcal{C}(A, B)$

A most general case occurs when two generic matrices $A$ and $B$ are involved. This set is denoted as:

$$C = \mathcal{C}(A, B)$$

(A.2)

where $A = [a_1, a_2, a_3, \ldots, a_{n-1}, a_n]$, $B = [b_1, b_2, b_3, \ldots, b_{n-1}, b_n]$ and $a_i, b_i$ represent columns.

Each $C_i \in C$ is given as:

$$
\begin{align*}
C_0 &= [a_1, a_2, a_3, \ldots, a_{n-1}, a_n] = A \\
C_1 &= [a_1, a_2, a_3, \ldots, a_{n-1}, b_n] \\
C_2 &= [a_1, a_2, a_3, \ldots, b_{n-1}, a_n] \\
C_3 &= [a_1, a_2, a_3, \ldots, b_{n-1}, b_n] \\
\vdots \\
C_{2^n-1} &= [a_1, b_2, b_3, \ldots, b_{n-1}, b_n]
\end{align*}
$$

By combining this set of equations with the set $\Delta = \mathcal{C}(I, \phi)$, it can be obtained:

$$
\begin{align*}
C_0 &= A \Delta_{2^n-1} + B \Delta_0 = A \\
C_1 &= A \Delta_{2^n-2} + B \Delta_1 \\
C_2 &= A \Delta_{2^n-3} + B \Delta_2 \\
C_3 &= A \Delta_{2^n-4} + B \Delta_3 \\
\vdots \\
C_{2^n-1} &= A \Delta_{2^n-1} + B \Delta_{2^n-1}
\end{align*}
$$

The terms $C_a \in \mathcal{C}(A, B)$ and $C_b \in \mathcal{C}(A, B)$ form a complementary pair when $a + b = 2^n - 1$. These matrices are given by:

$$
\begin{align*}
C_a &= A \Delta_{2^n-1-a} + B \Delta_a \\
C_b &= C_{2^n-1-a} = A \Delta_a + B \Delta_{2^n-1-a}
\end{align*}
$$

A-2 \quad \det [AD + B]

In this section we make use of the above definitions to determine a closed form for the determinant of the Jacobian matrix.

We first introduce the following theorem [1]:
Theorem A.1 Given the following generic matrices

\[ A = \begin{bmatrix} a_1 & a_2 & \cdots & a_r & \cdots & a_n \end{bmatrix}, \]

\[ B = \begin{bmatrix} a_1 & a_2 & \cdots & b_r & \cdots & a_n \end{bmatrix} \]

and

\[ C = \begin{bmatrix} a_1 & a_2 & \cdots & a_r + b_r & \cdots & a_n \end{bmatrix} \]

where \( a_i \) (resp. \( b_i \)) represents the \( i \)-th column of \( A \) (resp. \( B \)). i.e. \( C = [c_v] \) is a matrix such that \( v \neq r, c_v = a_v \) and for \( v = r, c_v = a_r + b_r \), then

\[ \det(C) = \det(A) + \det(B) \]

This theorem is used to demonstrate the following theorem:

Theorem A.2 Given the following generic matrices

\[ A = \begin{bmatrix} a_1 & a_2 & \cdots & a_n \end{bmatrix} \]

\[ B = \begin{bmatrix} b_1 & b_2 & \cdots & b_n \end{bmatrix} \]

where \( a_i \) (resp. \( b_i \)) is the \( i \)-th column of \( A \) (resp. \( B \)). Then:

\[ \det(A + B) = \sum_{i=0}^{2^n-1} \det C_i = \sum_{i=0}^{2^n-1} \det[A\Delta_{2^n-1-i} + B\Delta_i] \]

where \( C_i \in C(A, B) \).

proof:

The sum of \( A \) and \( B \) is given by:

\[ C = A + B = \begin{bmatrix} a_1 + b_1 & a_2 + b_2 & \cdots & a_n + b_n \end{bmatrix} \]

So that:

\[ \det C = \det \begin{bmatrix} a_1 + b_1 & a_2 + b_2 & \cdots & a_n + b_n \end{bmatrix} \]
Then by applying the theorem A.1 to the first column:

$$\det C = \det \begin{bmatrix} a_1 & a_2 + b_2 & \cdots & a_n + b_n \end{bmatrix} + \det \begin{bmatrix} b_1 & a_2 + b_2 & \cdots & a_n + b_n \end{bmatrix}$$

By applying it successively to the other columns, we obtain:

$$\det C = \det \begin{bmatrix} a_1 & a_2 & \cdots & a_n \end{bmatrix} + \det \begin{bmatrix} a_1 & a_2 & \cdots & b_n \end{bmatrix} + \det \begin{bmatrix} a_1 & b_2 & \cdots & a_n \end{bmatrix} + \det \begin{bmatrix} a_1 & b_2 & \cdots & b_n \end{bmatrix} + \det \begin{bmatrix} b_1 & a_2 & \cdots & a_n \end{bmatrix} + \det \begin{bmatrix} b_1 & a_2 & \cdots & b_n \end{bmatrix} + \det \begin{bmatrix} b_1 & b_2 & \cdots & a_n \end{bmatrix} + \det \begin{bmatrix} b_1 & b_2 & \cdots & b_n \end{bmatrix}$$

It is easy to recognize that the terms of the right-hand member belong to the set $C(A, B)$.

By applying the result of the previous theorem to equation (4.5) we obtain:

$$\det [AD + B] = \sum_{i=0}^{(2^n-1)} \det [AD\Delta_{2^n-1-i} + B\Delta_i]$$

(A.3)

which proves Theorem 4.1.

Finally, equation (4.6) can be also expressed as:

$$\det [AD + B] = \sum_{i=0}^{2^n-1} \det C_i \det \theta_i$$

where $C_i \in C(A, B)$ and $\theta_i \in C(D, I)$.

**Bibliography**

Appendix B

Analysis of various element types

In this section, the process of analysis for some subsets of $C$ ($T, B$) is done. It is demonstrated which subsets do not need to be evaluated. Along this section, the matrix $B$ represents the admittance matrix of the linear part of the circuit. Its elements are denoted by $g_{ij}$ instead of $b_{ij}$ in order to point out this fact.

$$B = \begin{bmatrix}
g_{11} & g_{12} & g_{13} & g_{14} & \cdots & g_{1,n-1} & g_{1n} 
g_{21} & g_{22} & g_{23} & g_{24} & \cdots & g_{2,n-1} & g_{2n} 
g_{31} & g_{32} & g_{33} & g_{34} & \cdots & g_{3,n-1} & g_{3n} 
g_{41} & g_{42} & g_{43} & g_{44} & \cdots & g_{4,n-1} & g_{4n} 
\vdots & \vdots & \vdots & \vdots & \ddots & \vdots & \vdots 
g_{n-1,1} & g_{n-1,2} & g_{n-1,3} & g_{n-1,4} & \cdots & g_{n-1,n-1} & g_{n-1,n} 
g_{n1} & g_{n2} & g_{n3} & g_{n4} & \cdots & g_{n,n-1} & g_{nn}
\end{bmatrix} \quad \text{(B.1)}$$

This matrix has the following characteristics:

- $g_{ij} = g_{ji} \ \forall i \neq j$
- $g_{ii} > 0$
- $g_{ii} \geq |g_{ij}|$

This makes $B$ to be positive definite.
Figure B.1: Structure of the matrix for an $\mathcal{E}^0$ element

**B-1 Subset $\mathcal{E}^0$**

In these cases $2n-1$ columns of $B$ and one column of $T$ are taken. An example of element of this subset is an element denoted by the index $[11 \ 01 \ 11]$.

The structure of the matrix for any element of this subset is depicted in fig. B.1, where the shadowed areas represent non-zero entries. In this figure the unique column taked from the matrix $T$ is placed as the $m$-th (last) column; however for another position of it, the same structure results by applying some permutations on columns and rows. The element $\alpha_z^{(i)}$ is given by:

$$\alpha_z^{(i)} = \begin{cases} 
\alpha^{(m/2)} & \text{for } m \text{ even} \\
\alpha_f^{(m+1/2)} & \text{for } m \text{ odd}
\end{cases}$$

We demonstrate now that any matrix of this subset is positive definite, by applying the following theorem [1]:

**Theorem B.1** If a general matrix $A = [a_{ij}]$ is a $n \times n$ positive definite matrix, then for any distinct $i$ and $j$ ($i, j = 1, 2, \ldots, n$), $a_{ii}a_{jj} \geq |a_{ij}|^2$
A matrix for this subset can be denoted as:

\[
M^{(0)} = \begin{bmatrix}
\hat{A} & \hat{B} \\
\hat{C} & \hat{D}
\end{bmatrix}
\]  \hspace{1cm} (B.2)

The sub-matrix \(\hat{A}\) is a \((j-2 \times j-2)\) matrix with the same structure as the admittance matrix \(B\), i.e. it is also positive definite. Consequently, the \((2 \times 2)\) submatrices to be checked are:

- The matrix \(\hat{D}\)
  
  It refers here to the determinant of \(\hat{D}\), which is always positive and given by:

  \[
  \det \hat{D} = g_{kk} + \alpha_x^{(i)} g_{mk}
  \]

- One element of the main diagonal of \(\hat{A}\) and \(g_{kk}\)

\[
\begin{bmatrix}
g_{ii} & g_{ik} \\
g_{ki} & g_{kk}
\end{bmatrix}
\]

- Element of the main diagonal of \(\hat{A}\) and 1

\[
\begin{bmatrix}
g_{ii} & 0 \\
g_{mi} & 1
\end{bmatrix}
\]

which are always positive.

This result can be given in the form of the following theorem:

**Theorem B.2** Given the matrices \(T\) and \(B\) which represent respectively the transistor relationships and the linear part of the circuit, then all elements of the subset \(E^0 \in C(T, B)\) are positive definite.

**B-2 Subset \(E^1\)**

In these cases, \(2n-1\) columns of \(T\) and one column of \(B\) are taken. An example of this subset is an element denoted by the index [00 00 01].

The structure of the matrix for any element of this subset \(E^1\) is depicted in fig. B.2. The unique column taken from the matrix \(B\) is placed
Figure B.2: Structure of the matrix for an $E^1$ element

as the $k$-th (last) column. As for the previous case, this structure may be obtained for any position of this column by applying permutations on columns and rows. The element $\alpha^{(i)}_z$ is given by:

$$\alpha^{(i)}_z = \begin{cases} 
\alpha^{(\frac{i}{2})}_f & \text{for } i \text{ even} \\
\alpha^{(\frac{i+1}{2})}_r & \text{for } i \text{ odd}
\end{cases}$$  \hspace{1cm} (B.3)

The structure described in figure B.2 yields the following general matrix for this subset:

$$M^{(1)} = \begin{bmatrix} \hat{T} & \hat{B} \\
\hat{C} & \hat{D} \end{bmatrix}$$ \hspace{1cm} (B.4)

Because $\hat{C}$ has only zero entries, the determinant is given by:

$$\det M^{(1)} = (g_{kk} + \alpha^{(i)}_z g_{jk}) \prod_{i=1}^{q-1} \det T_i$$

where: $\det T_i = (1 - \alpha^{(i)}_r \alpha^{(i)}_f)$, which makes the determinant always non-negative. This result can be also expressed by the following:
Theorem B.3  Given the matrices $T$ and $B$ which represent respectively the transistor relationships and the linear part of the circuit, then all elements of the subset $\mathcal{E}^1 \in \mathcal{C}(T, B)$ are positive definite.

![Diagram of matrix structure for $\mathcal{E}^P$ element](image)

Figure B.3: Structure of the matrix for an $\mathcal{E}^P$ element

B-3  Subset $\mathcal{E}^P$

In these cases $k$ column-pairs of $T$ and $l$ column-pairs of $B$ are taken. An example of element of this subset is an element denoted by the index $[001100]$.

Fig. B.3. shows the structure of the matrix for any $\mathcal{E}^P$ element. The columns corresponding to the matrix $T$ occupy until the $2q$-th column.
Figure B.4: Structure of the matrix for an $E^{P-1}$ element

The rest correspond to those columns from $B$. This structure yields:

$$M^{(P)} = \begin{bmatrix} \tilde{T} & \hat{B} \\ \hat{C} & \hat{D} \end{bmatrix}$$

(B.5)

Because $\hat{C}$ has only zero entries, the determinant is given by:

$$\det M^{(P)} = \det \hat{D} \prod_{i=1}^{q} \det T_i$$

The matrix $\hat{D}$ has the same structure as the original admittance matrix $B$, i.e. it is also positive definite. This result can be given as:
Theorem B.4 Given the matrices \( T \) and \( B \) which represent respectively the transistor relationships and the linear part of the circuit, then all elements of the subset \( \mathcal{E}^P \in \mathcal{C}(T, B) \) are positive definite.

B-4 Subset \( \mathcal{E}^{P-1} \)

In these cases column-pairs of \( T \) and of \( B \) are taken, except one. An example of this subset is an element denoted by the index \([00\ 11\ 01]\).

Fig. B.4. shows the structure of the matrix for any \( \mathcal{E}^{P-1} \) element. It can be denoted by the following expression:

\[
M^{(P-1)} = \begin{bmatrix}
\bar{T}_p & \hat{B} \\
C & \hat{D}
\end{bmatrix}
\]

(B.6)

In order to demonstrate that this subset has non-negative matrices, the peculiar structure shown in figure B.4 is used. Notice that the matrix \( \bar{T}_p \) represents always a positive definite matrix and \( \hat{D} \) has the same structure of \( \mathcal{E}^0 \). This last has been demonstrated to be positive. This leads to the following:

Theorem B.5 Given the matrices \( T \) and \( B \) which represent respectively the transistor relationships and the linear part of the circuit, then all elements of the subset \( \mathcal{E}^{P-1} \in \mathcal{C}(T, B) \) are positive definite.

The theorems found here separately, can be recast in a complete one, which constitutes Theorem 4.2.

Bibliography

Appendix C

Case of two transistors

In this appendix we analyze the case for two transistors and conclude that not all 16 elements of the summation need to be evaluated. The expansion of the juxtaposed set $C(T,B)$ is here written down. The binary index has been added as a help in order to follow the analysis in a better form.

$$C(T,B) =$$

\[
\begin{bmatrix}
1 & -\alpha_r^{(1)} & 0 & 0 \\
-\alpha_f^{(1)} & 1 & 0 & 0 \\
0 & 0 & 1 & -\alpha_r^{(2)} \\
0 & 0 & -\alpha_f^{(2)} & 1
\end{bmatrix}
\begin{bmatrix}
\text{0000} \\
\text{b_{11}} & \text{b_{12}} & \text{b_{13}} & \text{b_{14}} \\
\text{b_{21}} & \text{b_{22}} & \text{b_{23}} & \text{b_{24}} \\
\text{b_{31}} & \text{b_{32}} & \text{b_{33}} & \text{b_{34}} \\
\text{b_{41}} & \text{b_{42}} & \text{b_{43}} & \text{b_{44}}
\end{bmatrix}_{(1111)}
\]

\[
\begin{bmatrix}
1 & -\alpha_r^{(1)} & 0 & b_{14} \\
-\alpha_f^{(1)} & 1 & 0 & b_{24} \\
0 & 0 & 1 & b_{34} \\
0 & 0 & -\alpha_f^{(2)} & b_{44}
\end{bmatrix}
\begin{bmatrix}
\text{0001} \\
\text{b_{11}} & \text{b_{12}} & \text{b_{13}} & 0 \\
\text{b_{21}} & \text{b_{22}} & \text{b_{23}} & 0 \\
\text{b_{31}} & \text{b_{32}} & \text{b_{33}} & -\alpha_r^{(2)} \\
\text{b_{41}} & \text{b_{42}} & \text{b_{43}} & 1
\end{bmatrix}_{(1110)}
\]

\[
\begin{bmatrix}
1 & -\alpha_r^{(1)} & b_{13} & 0 \\
-\alpha_f^{(1)} & 1 & b_{23} & 0 \\
0 & 0 & b_{33} & -\alpha_r^{(2)} \\
0 & 0 & b_{43} & 1
\end{bmatrix}
\begin{bmatrix}
\text{0010} \\
\text{b_{11}} & \text{b_{12}} & 0 & b_{14} \\
\text{b_{21}} & \text{b_{22}} & 0 & b_{24} \\
\text{b_{31}} & \text{b_{32}} & 1 & b_{34} \\
\text{b_{41}} & \text{b_{42}} & -\alpha_f^{(2)} & b_{44}
\end{bmatrix}_{(1101)}
\]
\[
\begin{bmatrix}
1 & -\alpha_f^{(1)} & b_{13} & b_{14} \\
-\alpha_f^{(1)} & 1 & b_{23} & b_{24} \\
0 & 0 & b_{33} & b_{34} \\
0 & 0 & b_{43} & b_{44}
\end{bmatrix}^{(0011)} \quad \begin{bmatrix}
b_{11} & b_{12} & 0 & 0 \\
b_{21} & b_{22} & 0 & 0 \\
b_{31} & b_{32} & 1 & -\alpha_r \\
b_{41} & b_{42} & -\alpha_f^{(2)} & 1
\end{bmatrix}^{(1100)}
\begin{bmatrix}
1 & b_{12} & 0 & 0 \\
-\alpha_f^{(1)} & b_{22} & 0 & 0 \\
0 & b_{32} & 1 & -\alpha_f^{(2)} \\
0 & b_{42} & -\alpha_f^{(2)} & 1
\end{bmatrix}^{(0100)} \quad \begin{bmatrix}
b_{11} & -\alpha_r^{(1)} & b_{13} & b_{14} \\
b_{21} & 1 & b_{23} & b_{24} \\
b_{31} & 0 & b_{33} & b_{34} \\
b_{41} & 0 & b_{43} & b_{44}
\end{bmatrix}^{(1011)}
\begin{bmatrix}
1 & b_{12} & 0 & b_{14} \\
-\alpha_f^{(1)} & b_{22} & 0 & b_{24} \\
0 & b_{32} & 1 & b_{34} \\
0 & b_{42} & -\alpha_f^{(2)} & b_{44}
\end{bmatrix}^{(0101)} \quad \begin{bmatrix}
b_{11} & -\alpha_r^{(1)} & 0 & b_{14} \\
b_{21} & 1 & 0 & b_{24} \\
b_{31} & 0 & 1 & b_{34} \\
b_{41} & 0 & -\alpha_f^{(2)} & b_{44}
\end{bmatrix}^{(1010)}
\begin{bmatrix}
1 & b_{12} & b_{13} & 0 \\
-\alpha_f^{(1)} & b_{22} & b_{23} & 0 \\
0 & b_{32} & b_{33} & -\alpha_f^{(2)} \\
0 & b_{42} & b_{43} & 1
\end{bmatrix}^{(0110)} \quad \begin{bmatrix}
b_{11} & -\alpha_r^{(1)} & 0 & 0 \\
b_{21} & 1 & 0 & 0 \\
b_{31} & 0 & 1 & -\alpha_f^{(2)} \\
b_{41} & 0 & -\alpha_f^{(2)} & 1
\end{bmatrix}^{(1001)}
\begin{bmatrix}
1 & b_{12} & b_{13} & b_{14} \\
-\alpha_f^{(1)} & b_{22} & b_{23} & b_{24} \\
0 & b_{32} & b_{33} & b_{34} \\
0 & b_{42} & b_{43} & b_{44}
\end{bmatrix}^{(0111)} \quad \begin{bmatrix}
b_{11} & -\alpha_r^{(1)} & 0 & 0 \\
b_{21} & 1 & 0 & 0 \\
b_{31} & 0 & 1 & -\alpha_f^{(2)} \\
b_{41} & 0 & -\alpha_f^{(2)} & 1
\end{bmatrix}^{(1000)}
\]

C-1  Terms $C_0$ and $C_{15}$: $T$ and $B$

The determinants of the original matrices $T$ and $B$ correspond to the terms with subindices (0000) and (1111). For the matrix $T$ we obtain:

$$\delta_0 = (1 - \alpha_f^{(1)} \alpha_r^{(1)})(1 - \alpha_f^{(2)} \alpha_r^{(2)})$$

which is always positive.

However, for the det $B$, we conclude that it is always positive because it corresponds to a passive network. Both are always positive.
C-2 Terms with one column of B

Here are included those terms with only a one in the subindex, i.e. those corresponding to the following terms:

\[
\begin{bmatrix}
1 & -\alpha_r^{(1)} & 0 & b_{14} \\
-\alpha_f^{(1)} & 1 & 0 & b_{24} \\
0 & 0 & 1 & b_{34} \\
0 & 0 & -\alpha_f^{(2)} & b_{44}
\end{bmatrix}
\]

\[
\begin{bmatrix}
1 & -\alpha_r^{(1)} & b_{13} & 0 \\
-\alpha_f^{(1)} & 1 & b_{23} & 0 \\
0 & 0 & b_{33} & -\alpha_r^{(2)} \\
0 & 0 & b_{43} & 1
\end{bmatrix}
\]

\[
\begin{bmatrix}
1 & b_{12} & 0 & 0 \\
-\alpha_f^{(1)} & b_{22} & 0 & 0 \\
0 & b_{32} & 1 & -\alpha_r^{(2)} \\
0 & b_{42} & -\alpha_f^{(2)} & 1
\end{bmatrix}
\]

\[
\begin{bmatrix}
b_{11} & -\alpha_r^{(1)} & 0 & 0 \\
b_{21} & 1 & 0 & 0 \\
b_{31} & 0 & 1 & -\alpha_r^{(2)} \\
b_{41} & 0 & -\alpha_f^{(2)} & 1
\end{bmatrix}
\]

These terms can be expressed also like:

\[
\delta_1 = (1 - \alpha_f^{(1)} \alpha_r^{(1)}) b_{44} (1 + \alpha_r^{(2)} k_{34})
\]

\[
\delta_2 = (1 - \alpha_f^{(1)} \alpha_r^{(1)}) b_{33} (1 + \alpha_f^{(2)} k_{43})
\]

\[
\delta_4 = (1 - \alpha_f^{(2)} \alpha_r^{(2)}) b_{22} (1 + \alpha_f^{(1)} k_{12})
\]

\[
\delta_8 = (1 - \alpha_f^{(2)} \alpha_r^{(2)}) b_{11} (1 + \alpha_r^{(1)} k_{21})
\]

where:

\[
k_{12} = \frac{b_{12}}{b_{22}} \quad k_{21} = \frac{b_{21}}{b_{11}}
\]

\[
k_{34} = \frac{b_{34}}{b_{44}} \quad k_{43} = \frac{b_{43}}{b_{33}}
\]

Because of the paramouncticity of B, it is possible conclude that each \(b_{ii} > 0\) and for all k's, \(0 \leq |k_{ij}| \leq 1\). So that the determinants above are always positive.
C-3 Terms with one column of $T$

Those terms with only a zero in the subindex are going to be treated here:

\[
\begin{bmatrix}
  b_{11} & b_{12} & b_{13} & 0 \\
  b_{21} & b_{22} & b_{23} & 0 \\
  b_{31} & b_{32} & b_{33} & -\alpha_r^{(2)} \\
  b_{41} & b_{42} & b_{43} & 1 \\
\end{bmatrix}_{(1110)} \quad \begin{bmatrix}
  b_{11} & b_{12} & 0 & b_{14} \\
  b_{21} & b_{22} & 0 & b_{24} \\
  b_{31} & b_{32} & 1 & b_{34} \\
  b_{41} & b_{42} & -\alpha_r^{(2)} & b_{44} \\
\end{bmatrix}_{(1101)} \\
\begin{bmatrix}
  b_{11} & -\alpha_r^{(1)} & b_{13} & b_{14} \\
  b_{21} & 1 & b_{23} & b_{24} \\
  b_{31} & 0 & b_{33} & b_{34} \\
  b_{41} & 0 & b_{43} & b_{44} \\
\end{bmatrix}_{(1011)} \quad \begin{bmatrix}
  1 & b_{12} & b_{13} & b_{14} \\
 -\alpha_f^{(1)} & b_{22} & b_{23} & b_{24} \\
 0 & b_{32} & b_{33} & b_{34} \\
 0 & b_{42} & b_{43} & b_{44} \\
\end{bmatrix}_{(0111)}
\]

Each determinant can be expressed as:

\[
\delta_i = \det [\hat{B}] + \alpha_{[f,r]}^{(k/2)} \det [\hat{B}] 
\]

where:

\(i = 14, 13, 11, 7\)
\(j = 4 - \log_2 (2^4 - 1 - i)\)
\(\alpha_f\) for odd \(j\)
\(\alpha_r\) for even \(j\)

\(k = \begin{cases} 
  j + 1 & \text{for } j \text{ odd} \\
  j - 1 & \text{for } j \text{ even}
\end{cases}\)

\(\hat{B} = B\) cancelling \(j\)-th row and column
\(\hat{B} = B\) cancelling \(j\)-th column and \(k\)-th row

Because the paramounicity of \(B\), these determinants are always positive.

C-4 Terms with one column-pair of $T$

Here are included the following terms:

\[
\begin{bmatrix}
  1 & -\alpha_r^{(1)} & 0 & 0 \\
 -\alpha_f^{(1)} & 1 & b_{13} & b_{14} \\
 0 & 0 & b_{23} & b_{24} \\
 0 & 0 & b_{43} & b_{44} \\
\end{bmatrix}_{(0011)} \quad \begin{bmatrix}
  b_{11} & b_{12} & 0 & 0 \\
  b_{21} & b_{22} & 0 & 0 \\
  b_{31} & b_{32} & 1 & -\alpha_r^{(2)} \\
  b_{41} & b_{42} & 0 & 0 \\
\end{bmatrix}_{(1100)} \\
\begin{bmatrix}
  1 & -\alpha_r^{(1)} & b_{13} & b_{14} \\
 -\alpha_f^{(1)} & 1 & b_{23} & b_{24} \\
 0 & 0 & b_{33} & b_{34} \\
 0 & 0 & b_{43} & b_{44} \\
\end{bmatrix}_{(0011)} \quad \begin{bmatrix}
  b_{11} & b_{12} & 0 & 0 \\
  b_{21} & b_{22} & 0 & 0 \\
  b_{31} & b_{32} & 1 & -\alpha_r^{(2)} \\
  b_{41} & b_{42} & 0 & 0 \\
\end{bmatrix}_{(1100)}
\]

By expanding the expressions on the right-hand side:

\[
\delta_3 = (1 - \alpha_f^{(1)} \alpha_r^{(1)}) b_{33} b_{44} (1 - k_{34} k_{43})
\]
\[
\delta_{12} = (1 - \alpha_f^{(2)} \alpha_r^{(2)}) b_{11} b_{22} (1 - k_{12} k_{21})
\]
C-5. TERMS IN THE $\mathcal{O}$ SUBSET

Again, because of the paramouncty of $B$, it is possible to conclude that both determinants are always positive.

C-5 Terms in the $\mathcal{O}$ subset

As we can conclude from the previous sections, all terms analyzed are always non-negative and thus they do not need to be evaluated. The only elements which need to be evaluated are the remaining terms which are marked with the the binary subindices (0101), (0110), (1001), and (1010). These terms correspond to the $\mathcal{O}(T, B)$ subset.

\[
\begin{bmatrix}
1 & b_{12} & 0 & b_{14} \\
-\alpha_f^{(1)} & b_{22} & 0 & b_{24} \\
0 & b_{32} & 1 & b_{34} \\
b_{42} & -\alpha_f^{(2)} & b_{44} \\
\end{bmatrix}_{0101} \quad \begin{bmatrix}
1 & b_{12} & b_{13} & 0 \\
-\alpha_f^{(1)} & b_{22} & b_{23} & 0 \\
0 & b_{32} & b_{33} & -\alpha_r^{(2)} \\
0 & b_{42} & b_{43} & 1 \\
\end{bmatrix}_{0110}
\]

\[
\begin{bmatrix}
1 & b_{12} & 0 & b_{14} \\
-\alpha_r^{(1)} & b_{21} & 0 & b_{24} \\
b_{31} & 0 & 1 & b_{34} \\
b_{41} & 0 & -\alpha_f^{(2)} & b_{44} \\
\end{bmatrix}_{1001} \quad \begin{bmatrix}
b_{11} & -\alpha_r^{(1)} & b_{13} & 0 \\
b_{12} & 1 & b_{33} & 0 \\
b_{31} & 0 & b_{33} & -\alpha_r^{(2)} \\
b_{41} & 0 & b_{43} & 1 \\
\end{bmatrix}_{1010}
\]

By expanding each determinant, it is possible to obtain:

\[
\delta_5 = b_{22}b_{44} \left[ (1 + k_{21}\alpha_f^{(1)}) (1 + k_{43}\alpha_f^{(2)}) - (k_{42} + k_{41}\alpha_f^{(1)})(k_{24} + k_{23}\alpha_f^{(2)}) \right]
\]

\[
\delta_6 = b_{22}b_{33} \left[ (1 + k_{21}\alpha_f^{(1)}) (1 + k_{34}\alpha_r^{(2)}) - (k_{32} + k_{31}\alpha_f^{(1)})(k_{23} + k_{24}\alpha_r^{(2)}) \right]
\]

\[
\delta_9 = b_{11}b_{44} \left[ (1 + k_{12}\alpha_r^{(1)}) (1 + k_{43}\alpha_f^{(2)}) - (k_{41} + k_{42}\alpha_r^{(1)})(k_{14} + k_{13}\alpha_f^{(2)}) \right]
\]

\[
\delta_{10} = b_{11}b_{33} \left[ (1 + k_{12}\alpha_r^{(1)}) (1 + k_{34}\alpha_r^{(2)}) - (k_{31} + k_{32}\alpha_r^{(1)})(k_{13} + k_{14}\alpha_r^{(2)}) \right]
\]

It can be demonstrated [1, 2], that the only element that can become negative is $\delta_5$, i.e. the element involving both $\alpha_f$'s.

Bibliography

Summary

In this thesis, a topological description of transistor circuits is used to determine an upper bound on the number of DC operating points along with the calculation of these operating points. This leads to a method useful for a class of transistor circuits.

In Chapter 1, the phenomenon of multiple DC solutions in electronic circuits is outlined. A survey is given of the principles of the main methods used to solve this problem. The usual methods start basically from a mathematical representation of the circuit and then they try to solve the resulting equilibrium equations. Clearly, they do not make use of valuable information from the circuit to its full extent. In fact, part of the information that is related to the topology of the circuit is lost. Therefore, a method which makes use of this information in a proper manner is more useful when trying to solve the problem of multiple DC operating points. In addition, this chapter gives an overview of the general structure of the circuit simulation programs.

In Chapter 2, some fundamentals of graph theory and circuit topology, which are applicable to circuit analysis are presented. There is also a review of the most commonly used network analysis methods.

In Chapter 3, the formulation of the equilibrium equations for DC analysis for the modified nodal analysis representation is explained. The
Newton-Raphson algorithm represents the tool most frequently used to solve the nonlinear algebraic equations obtained from DC formulation. In this chapter, an outline of this method is given as well as its discretized linear resistive equivalent. Finally, an overview of the methods used to find more than one DC operating point is also presented, and their properties are briefly exposed. The necessity of a topological approach is here highlighted in view of the deficiencies of those methods.

In Chapter 4, the problem of finding multiple solutions is formulated from a point of view which takes into account the topology of the circuit. In order to obtain such a formulation, a model which separates the linear part from the nonlinear part of the circuit is used. This results in a canonical representation of the circuit in the form of a $2q$ port, where $q$ is the number of transistors. The port contains only the linear part of the circuit constituted by linear positive resistors and independent sources. Therefore, the model can be described by setting up two matrices, the first one related to the linear part of the circuit and the second matrix related to the part containing the transistors. From this pair of matrices a juxtaposed set is formed and the topological implications of each of the matrices in the set are derived.

In Chapter 5, the characteristics of both matrices are widely analyzed and a first main result is achieved. This result concerns a partitioning procedure of the circuit aimed to obtaining subcircuits to be searched for the possible existence of feedback structures. In this chapter, the solution to the DC problem of transistor circuits is fully treated as the solution to the following items: the determination of the uniqueness of the DC operating point, the upper bound on the number of DC operating points and the finding of all operating points. Two main results are established for the first questions: the uniqueness is tested by checking if one element of the juxtaposed set has negative value, and the upper bound on the number of DC solutions is assessed from the feedback structures found embedded in the circuit. In an further step, a restricted search procedure is set up in order to solve the third point.

In Chapter 6, the method is tested by several examples. Among these, typical benchmarks used by various authors are treated.

Finally, the conclusions of the present work are given in Chapter 7; as well as some recommendations for future research.
Samenvatting

Dit proefschrift behandelt het bepalen van de bovengrens van het aantal DC-oplossingen en de daarbij behorende oplossingen met behulp van een topologische beschrijving. Hierbij is een methode ontwikkeld die bruikbaar is voor een grote klasse van transistor schakelingen.

In Hoofdstuk 1 wordt het fenomeen van meervoudige DC-oplossingen van electronische schakelingen belicht. Er wordt een overzicht gegeven van de uitgangspunten van bekende methoden om dit probleem op te lossen. In bijna al deze methoden wordt uitgegaan van een mathematische beschrijving van het circuit waarna getracht wordt uit de gegenereerde vergelijkingen voor het instelpunt de oplossing te vinden. Bij het opstellen van de mathematische vergelijkingen gaat echter waardevolle informatie van de kenmerken van het circuit verloren. In het bijzonder geldt dit voor de informatie die voortkomt uit de topologie van het netwerk. Een methode die wel van deze informatie gebruikt maakt kan wellicht bruikbaarder zijn om het probleem van meervoudige DC-instelpunten op te lossen. Verder wordt in Hoofdstuk 1 nog een overzicht gegeven van de gebruikelijke opzet van circuit simulatie programma's.

Hoofdstuk 2 behandelt enige grondbeginselen van graphen-theorie en topologie van netwerken zoals die in circuit-analyse worden toegepast. Tevens geeft het een overzicht van de meest gebruikelijke netwerk-analyse
methoden.

In Hoofdstuk 3 worden met behulp van de gemodificeerde knooppuntsanalyse de DC instellings-vergelijkingen opgesteld. De hier ontstane niet-liniaire algebraïsche vergelijkingen worden meestal met behulp van het Newton-Raphson algoritme opgelost. Naast de beschrijving van de opzet van de knooppunt-analyse wordt ook een hieraan equivalente geliniearizeerde weerstandsbeschrijving gegeven. Ten slotte wordt er een overzicht gegeven van enkele methoden die in voorkomende gevallen in staat zijn meer dan één oplossing te vinden. Hun kenmerken worden in het kort beschreven. De noodzakelijkheid om ook een topologische benadering te gebruiken om tegemoet te komen aan de tekortkomingen van deze methoden zal hier duidelijk aan het licht komen.

Met gebruikmaking van de topologische informatie wordt in Hoofdstuk 4, de manier om meervoudige oplossingen te vinden, geformuleerd. Hiertoe wordt een model gehanteerd dat in staat is om het liniaire gedeelte van het netwerk te scheiden van het niet-liniaire gedeelte van het netwerk. Het resultaat is een kanonieke representatie die bestaat uit een $2q$-poort. Hierin is $q$ het aantal transistoren. Deze poort bestaat alleen uit het liniaire gedeelte van het netwerk dat opgebouwd is uit alle liniaire, positieve weerstanden en onafhankelijke bronnen. Het gevolg van deze opzet is dat het netwerkmodel kan worden beschreven met behulp van twee matrices. Hiervan is één matrix opgebouwd uit het liniaire deel van het netwerk en de tweede matrix is gerelateerd aan de transistoren. Met deze twee matrices wordt één 'juxtaposed' set matrices samengesteld en de topologische informatie, die in elk van de matrices opgesloten ligt, wordt bepaald.

De karakteristieke gegevens van beide matrices worden in Hoofdstuk 5 verder geanalyseerd en het eerste belangrijke resultaat wordt hier bereikt. Dit resultaat bestaat uit een verdelingsprocedure van het netwerk om sub-netwerken te verkrijgen. Deze sub-netwerken worden daarna onderzocht op het bestaan van terugkoppellussen. In dit hoofdstuk wordt het probleem van de DC-analyse geheel benaderd als de oplossing van de volgende onderdelen: ten eerste het bepalen van de eenduidigheid van de DC-instelling en ten tweede het bepalen van de bovengrens van het aantal DC-oplossingen en ten derde het vinden van deze oplossingen. Twee belangrijke resultaten zijn behaald voor de eerste twee onderdelen: de eenduidigheid wordt getest door het onderzoek of een element van de
vergelijkingen-set een negatieve waarde heeft en de bovengrens van de DC-oplossingen wordt bepaald uit de terugkoppellussen die het circuit bevatten. In de laatste stap wordt een beperkte zoekprocedure opgezet om ook het derde onderdeel op te lossen.

Hoofdstuk 6 beschrijft de uitwerking van deze methode aan de hand van een aantal voorbeelden. Hieronder zijn een aantal typische benchmarks welke door meerdere auteurs zijn gebruikt.

Ten slotte worden in Hoofdstuk 7 conclusies getrokken en aanbevelingen voor toekomstig onderzoek gegeven.
Acknowledgments

I am indebted to my promotor Prof. Jan Davidse for the opportunity to join the Delft University’s Electronics Laboratory. His suggestions and technical discussions during the elaboration of this thesis have been of considerable help in concluding this work.

I would like to express my sincere appreciation to Dr. Eduard Kleihorst from whom I received the most direct guidance. His experience in the field of circuit simulation techniques has been for me of inestimable benefit.

To my colleagues of the sub-culture of CAD in our group:
Hans Stoffels for his patience during my learning process in computer programming.
Kees van Reeuwijk for providing TM, a programming tool which saved a lot of work in the implementation of my algorithm.
Martin Middelhoek for his companionship.
Jan Nusteling and Rob Janse for their wilful support in the area of computer facilities.

There are many administrative issues which I consider to be closely related to the purely academical ones. Being a foreigner, these issues often become insurmountable obstacles, at least if you do not get the right person on your side. I would like to specially thank David van Maaren for his open disposition for being that person for these years.

I am much obliged to Ms. Jane Zaat-Jones, who patiently corrected the manuscript.

To Riet Kleihorst, who did the splendid correction to the Dutch summary.

It is impossible to name everybody, without leaving someone out. I would like to thank all members of the staff of the Electronics Laboratory, who provided the environment in which I could work during my thesis.

I thank also to the Mexican Consejo Nacional de Ciencia y Tecnología for the economic support provided during a part of this thesis.

And certainly, to Guadalupe for her support and understanding.
Biography

Librado Arturo Sarmiento Reyes was born in Veracruz, México on August 17th 1958. When he was eight, he decided that he would become electrical or chemical engineer, mainly because of the fact that these courses were given at the best school in town. Later, in 1976, he was admitted to the Instituto Tecnológico de Veracruz, where he followed courses in electronics. He obtained the title of Ingeniero Industrial en Eléctronica in 1979. In May 1980, he was admitted to the Instituto Nacional de Astrofísica Optica y Electrónica (INAOE) at Puebla and started Master of Sciences courses in electronics. After his graduation in 1983, he obtained a position of assistant researcher at INAOE and worked until 1988 in the areas of analog filters and electronic design. In September 1988, he joined the Electronics Research Laboratory at the Faculty of Electrical Engineering of the Delft University of Technology and worked towards his Ph.D., which led to the current thesis.