A Low-Power Thermal Wind Sensor in CMOS Technology

by

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Abstract

Wind sensors are widely used in many critical applications, such as navigation, weather forecast, aerospace and wind energy assessment. The thermal wind sensor can measure wind speed and direction at the same time, by measuring the temperature gradient on the sensor’s surface which is induced by the wind flow. Compared to traditional mechanical wind sensors, there are two main advantages for thermal wind sensors: Firstly, thermal sensors can measure the wind flow without any moving parts, thus no maintenance is required. Secondly, the sensing elements of the thermal wind sensor (such as heaters, thermopiles, etc) as well as its interface circuitry can be realized in a single CMOS chip. Therefore, the robustness of the sensor system can be enhanced. Despite these advantages, the existing CMOS thermal wind sensor’s relatively high power consumption strictly limits its applications. The scope of this thesis is the design and realization of a low-power CMOS thermal wind sensor with the competitive sensing accuracy as its mechanical counterparts. In order to achieve this, the constant power mode instead of traditional constant temperature difference mode is applied to the thermal wind sensor to reduce the power consumption. The advantage of the constant power mode is that the power consumption of the sensor can be controlled by an external digital signal, instead of being limited by the sensing inaccuracy of the temperature sensors. Based on the existing sensing elements, only by adding an extra comparator, the air-flow induced temperature gradient $\delta T$ can then be directly converted into digital bit-stream by a thermal $\Sigma \Delta$ modulator. Because the noise-shaping provided by the thermal loop filter of the first-order thermal $\Sigma \Delta$ modulator is not sufficient, for given sensing resolution, the heater’s power consumption of the thermal wind sensor is limited by the quantization noise. By cascading the thermal filter with an electrical integrator, the resulting second-order thermal $\Sigma \Delta$ loop can provide more noise-shaping than the first-order system, to further reduce the quantization noise, thus required heating power consumption. To achieve reduced error due to the self-heating of the circuit, the chopping amplifier instead of traditional auto-zeroing amplifier, is used to interface the thermopile output signal. Two prototypes of the thermal wind sensor have been realized in standard CMOS process. The feasibility of the second-order thermal
ΣΔ modulator has been verified by the first proof-of-concept prototype. Measurements in wind tunnel show that the wind speed and direction accuracy are ±4% and ±2˚ respectively. Among the existing CMOS thermal wind sensors, the first-prototype achieves the lowest power consumption, which is 50mW in total. In the second prototype, system-level chopping is applied to reduce the offset of the interface circuit, to further reduce the power consumption to 25mW. Since the phase delay of the thermal filter is a monotonic function of the temperature, by measuring the peak frequency of the second-order thermal ΣΔ modulator’s output square wave, temperature sensing can be achieved with the same thermal wind sensor chip. Measurements in the oven show that the resolution of the temperature sensing is about ±1˚C with the range of [-40˚C 50˚C].
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Chapter 1 Introduction

Wind sensors are useful in many applications, e.g. weather forecast, environmental monitoring, aerospace and sailing, etc. Compared to traditional mechanical wind sensors, the main advantage of thermal wind sensors is that they do not need mechanical moving parts. Thus, they are more robust and require much less maintenance. In addition, thermal wind sensors and their read-out circuitry can be batch fabricated in a single chip using integrated circuit (IC) technology, enabling enhanced reliability and reduced manufacture cost. This thesis addresses the main problem that prevents the wide-spread use of the thermal wind sensors fabricated in IC technology: their relatively high power consumption. Several new techniques are introduced to reduce the sensor’s total power consumption. The effectiveness of these techniques will be demonstrated by two sensor prototypes.

This chapter begins with the introduction of the basic operating principles and classification of the various thermal wind sensors that can be realized using integrated circuit (IC) technology, and a brief literature review of previous research works. This is followed by the motivation and objective of this thesis. Finally, the organization of the thesis is presented.

1.1 Thermal Wind Sensors

Much effort has been devoted to the realizations of wind sensors in integrated circuit (IC) technology, which is quite suitable for the volume production of low-cost products. In addition, wind sensors which are fabricated in IC technology can then be combined with its interface circuitry on the same chip. Such integrated wind sensors have distinct advantages compared to the conventional sensors which are realized with separate wind sensor and interface circuit: they can directly communicate with the micro-computer in a standard digital format, thus increasing the modularity of the system. Furthermore, the local processing of the sensor’s output signal, including the amplification, analog to
digital conversion, makes the measurement more robust to external electrical interference.

There are different ways of realizing a wind sensor in IC technology, which include measuring a physical deflection, heat loss, or pressure variation induced by the air flow [1]. However, the overwhelming majority of silicon wind sensors found in open literature are operated in the thermal domain[2]. This is mainly because the heaters and temperature sensors which are required in the thermal wind sensor, are readily available in IC technology. The operation of a thermal wind sensor is based on the thermal interaction between a heated silicon chip and an air flow. In general, heat will be transferred from the heated chip to the air flow. Furthermore, the heated chip will be cooled in a non-uniform manner, with its upstream region experiencing more cooling than the downstream region. Thus, a temperature gradient will be induced in or around the heated object. Depending on whether they measure the object’s heat loss or the temperature gradient induced by the wind, thermal wind sensors can be grouped into two main classes: thermal anemometers and calorimetric wind sensors[2,3]. In the following section, their working principles will be described respectively.

Figure 1-1 Schematic illustrating the working principles of thermal flow sensors: (a) Thermal anemometers (b) Calorimetric wind sensors
1.1.1 Thermal anemometers

Thermal anemometers determine wind speed by measuring the absolute heat loss of a heated object. Thermal anemometers are also named as hot-film sensor or hot-plate in literatures[1-3]. The relationship between the heating power $P$ dissipated in the object and the flow speed $U$ was first derived by King for a thin wire and is thus referred to as King’s Law[4]. The equation is shown in (1- 1):

$$\frac{P}{\Delta T} = A + B\sqrt{U}$$  (1- 1)

where $A$ and $B$ are constants and $\Delta T$ is the overheat temperature, i.e. the difference between the temperature of the heated object and the ambient temperature. The constant $A$ and $B$ represent the wire’s heat loss by conduction (to its supports) and convection (to the wind), respectively. The parameters $A$ and $B$ depend on the sensor’s geometry and the physical properties of the flow, such as its thermal conductivity, density, viscosity etc[5].

The working principle of the thermal anemometer is shown in Figure 1- 1(a). Based on King’s law, the speed of the airflow can be determined if the sensor’s power dissipation $P$ and overheat temperature $\Delta T$ are known. In practice, one of the two parameters is kept constant while the other one is measured. Thus the sensor can work in two different operating modes: constant power (CP) mode or constant temperature difference (CTD) mode[6]. In the CP mode, the wind sensor chip dissipates constant power $P$, and the overheat temperature $\Delta T$ of the chip is then a measure of flow speed. By contrast, in CTD mode, the overheat temperature of the sensor $\Delta T$ is kept constant by a feedback loop. The heating power $P$ needed to maintain this constant overheat $\Delta T$ is then a measure of flow speed[3].

1.1.2 Calorimetric Wind Sensor

Because the heated chip is cooled in a non-uniform manner, with its upstream region experiencing more cooling than the downstream region, a temperature gradient will be induced around the heated chip. By measuring the flow-induced temperature difference between two symmetrical points located around the heaters, the wind speed component
in a certain direction can be determined. Based on this principle, both one-dimensional and two-dimensional flow sensors can be realized [6]. This kind of wind sensor is known as a calorimetric wind sensor. An example of a one-dimensional calorimetric wind sensor is shown in Figure 1-1(b). It consists of three resistors in a silicon chip. The resistor at the center is used as a heater. The other two resistors are used as temperature sensors, i.e. the thermistors, and are arranged symmetrically. At zero wind flow, the heat distribution in the sensor is symmetric, and so the temperature difference between the two temperature sensors, i.e. $\delta T$, will be zero. In the presence of wind, the upstream thermistor will be cooled, while the downstream thermistor will be heated by heat transported from the heater by the flow. By measuring the temperature gradient $\delta T$, the wind speed can be determined.

By regulating either the total power consumption $P$ or the overheat temperature $\Delta T$ of the sensor, a calorimetric wind sensor, like a thermal anemometer, can also be operated in CP mode or CTD mode. A more detailed description and comparison of these two working modes of calorimetric wind sensor will be given in Chapter 2.

1.1.3 Realization of thermal wind sensor

As can be seen from the previous sections, thermal wind sensor’s operation requires heaters and temperature sensors. In standard IC processes, there are a number of elements with which these can be realized. These are resistors, bipolar transistors, and thermocouples. The first two can be used as heaters, while all of them can be used as temperature sensors. Because the temperature gradient sensing can be realized by using resistor, bipolar transistor/diode or thermocouple, the thermal wind sensors can be categorized into three different types: thermoresistive, thermoelectric and thermoelectronic [6], respectively.

**Realization of heaters**

In standard IC technology, the heaters are usually realized with on-chip resistors, which are usually made of doped silicon, doped poly-silicon, or interconnect metal [1,2,6]. By appropriate biasing, a bipolar transistor can also be used as a heater[6]. The power consumption of the heater can be actually controlled by adjusting the driving voltage (or current) of the heater [3].
Realization of temperature sensors

(1) Resistors

In standard IC technology, on-chip resistors can be used as temperature sensors by exploiting their non-zero TCR (Temperature Coefficient of Resistance). On one hand, a high absolute TCR is desired for the resistor since sensitivity to temperature change is proportional to its TCR. On the other hand, high resistivity of the material is also required since it is the resistance change that is being detected. A higher nominal resistance will increase sensitivity. The ease of material fabrication processing in IC technology is also very important to the material selection. The thermal and electrical properties of commonly used resistance materials in standard IC technology are listed in Table 1-1. Platinum[7-9], gold[10], polysilicon[11,12] have been used for the thermistors. Also, thermistors made of germanium were also employed[13-15].

<table>
<thead>
<tr>
<th>Material</th>
<th>Resistivity, ρ(Ω·m) at 20°C</th>
<th>TCR(10⁻⁴/K)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Aluminum</td>
<td>2.69x10⁻⁸</td>
<td>42.0</td>
</tr>
<tr>
<td>Copper</td>
<td>1.67x10⁻⁸</td>
<td>43.0</td>
</tr>
<tr>
<td>Gold</td>
<td>2.30x10⁻⁸</td>
<td>39.0</td>
</tr>
<tr>
<td>Platinum</td>
<td>10.6x10⁻⁸</td>
<td>37.7</td>
</tr>
<tr>
<td>Silver</td>
<td>1.63x10⁻⁸</td>
<td>41.0</td>
</tr>
<tr>
<td>Polysilicon</td>
<td>4x10⁻⁶⁻¹x10⁻¹¹⁷⁻²⁰</td>
<td>-250-10</td>
</tr>
</tbody>
</table>

Due to process spreading, the absolute value of the integrated resistors with IC technology can vary by several tens of percent. Thus, resistors, when used as absolute temperature sensors, are quite inaccurate. However, the matching between adjacent on-chip resistors can be much better: mismatch errors of a few thousand ppm can be realized with standard IC technology. Thus, resistors are often used in a Wheatstone bridge configuration to measure temperature differences, i.e. the so-called “relative temperature”. As indicated in [3], resistor mismatch can still induce relative temperature sensing errors of a few degrees. For better accuracy, the Wheatstone bridge can be
trimmed either by hand or by laser. However, the calibration will dramatically increase fabrication cost.

(2) Bipolar transistors

A bipolar transistor can also be used as an absolute temperature sensor because its base-emitter voltage $V_{BE}$ decreases in an almost linear manner with increasing temperature[3]. Empirically, it has been found that at room temperature (300K), $V_{BE}$ has a negative temperature coefficient of -2mV/°C. Therefore, by measuring the $V_{BE}$, the absolute temperature can be measured accordingly. However, due to process variation, the spreading of $V_{BE}$ will be in the order of several millivolts, resulting in temperature sensing errors of several degrees [3]. A more accurate way of measuring the absolute temperature involves measuring the change of $V_{BE}$, i.e. $\Delta V_{BE}$, which occurs when the same transistor is biased at two different collector currents. This $\Delta V_{BE}$ is proportional to the absolute temperature (PTAT) and is independent of process variations. As indicated in literature [21], by using this method, un-calibrated temperature sensing errors of less than ±2°C can be achieved. The bipolar transistors are commonly used to measure both the ambient and thermal wind sensor’s temperatures to regulate the overheat temperature of the sensor, $\Delta T$ [3].

(3) Thermopiles

When two different conducting materials are ohmically connected and differentially heated at two ends, a self-generated potential difference between the two terminals of the structure will be created (Figure 1-2). This is referred as the Seeback effect [1]. The output voltage of a thermocouple $V_{AB}$, is given in (1-2)

$$V_{AB} = (\alpha_A - \alpha_B)(T_{hot} - T_{cold}) = \alpha_{AB}(T_{hot} - T_{cold})$$

where $\alpha_A$ and $\alpha_B$ are the Seebeck coefficients of the two different materials, $\alpha_{AB}$ is the Seebeck coefficient of the thermocouple, $T_{hot}$ and $T_{cold}$ are the temperatures of the hot and cold junctions, respectively (Figure 1-2). The Seebeck coefficients and thermal conductance of thermoelectric materials which are commonly fabricated in IC technology are listed in Table 1-2. On-chip thermocouples can be used as relative temperature sensors.
sensors to measure a temperature difference $\delta T$ which is induced by the wind flow. Thermocouples for temperature detection have been made out of aluminum/polysilicon [22], platinum/high boron doped silicon [23], n-polysilicon/p-polysilicon [24], gold/polysilicon [25], and aluminum/p+ doped silicon [26]. Semiconductor thermopiles are more sensitive than metal thermopiles because of their higher Seebeck coefficient. Thus, thermopiles fabricated from polysilicon and metal are commonly used in thermoelectric flow sensing[27].

![Operating principle of a thermocouple](image)

**Figure 1-2 Operating principle of a thermocouple [27]**

<table>
<thead>
<tr>
<th>Material</th>
<th>Seebeck coefficient ($\mu$V/K) @ 27°C</th>
<th>Thermal Conductance (W/K·m)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Aluminum</td>
<td>-1.7</td>
<td>250</td>
</tr>
<tr>
<td>Copper</td>
<td>1.70</td>
<td>401</td>
</tr>
<tr>
<td>Gold</td>
<td>1.79</td>
<td>318</td>
</tr>
<tr>
<td>Platinum</td>
<td>-4.45</td>
<td>70</td>
</tr>
<tr>
<td>p+ silicon</td>
<td>300~1000</td>
<td>149</td>
</tr>
<tr>
<td>n+ silicon</td>
<td>-500~200</td>
<td>149</td>
</tr>
</tbody>
</table>

Because the Seebeck effect is a self-generating effect, thermocouples are intrinsically free of offset. Their offset-free property makes them well suited for use as thermal zero-crossing detectors [3]. The output voltage of a single thermocouple is usually quite small ($\mu$V level). Therefore, a number of thermocouples are connected in series to form a so-called “thermopile” to enlarge the output voltage.
1.1.4 Smart Wind Sensor System Overview

An integrated two-dimensional smart wind sensor is shown in Figure 1-3. The overheat $\Delta T$ of the heated silicon chip can be modulated by the air-flow. In addition, the air-flow cools the heated silicon chip in an asymmetrical manner, thus inducing a temperature gradient $\delta T$ in the chip. This gradient will then be digitized then translated into wind speed and direction readings.

The analog-to-digital converter (ADC) of a thermal wind sensor can operate in two different ways: open loop or closed loop. In an open-loop system, the temperature sensor’s output will first be amplified and then be converted to the digital domain. By contrast, in a closed loop system, the temperature sensors, the heaters and the thermal mass of the silicon sensor can all be embedded in the feedback loop to read out the temperature gradient $\delta T$. After the sensor’s calibration in the wind tunnel, the ADC output can then be translated into wind velocity (speed & direction) by using the physical model of the sensor. The sensor can communicate with the outside world via a digital interface peripheral, such as I2C or RS232. The details of this system will be described in the following chapters.

Figure 1-3 Block diagram of an integrated smart wind sensor

1.2 Literature Review

Over the past several decades, many research efforts have been devoted to the general-purpose thermal gas-flow sensors, whose working principle, operating modes and interface circuitry can also be good reference for the thermal wind sensors. Thus, the following literature review is not only limited to the thermal wind sensors, but covers the general-purpose thermal gas-flow sensors.
As a general rule, the lower the thermal mass of the thermal gas-flow sensor (including the heater, temperature sensors and their support structure) and the greater its thermal isolation from the ambient environment, the faster the sensor responds to changes in flow speed and the higher is its sensitivity[1,2,6]. Therefore, many thermal gas-flow sensors, are fabricated on a suspending thermally isolated structure with so called “MEMS techniques”, such as bulk/surface/epi-layer silicon substrate etching [27]. The supporting structure of the sensor can be a cantilever that extends into the flow[28], very thin membranes[9,14,15, 29-32], or bridges across the flow path[10,12,33]. However, because the support structure can be quite thin due to the etching of the silicon substrate, the sensor is prone to be damaged in the packaging process. By contrast, the thermal gas-flow sensors can be also fabricated on a thick silicon substrate (500~800µm thick) with standard CMOS technology [3]. Compared to their MEMS counterparts, the CMOS thermal flow sensors have thicker silicon supporting structure, thus more mechanical strength and robustness [8,13,34-41], which are essential for the wind sensing applications in the outdoor environment. The power consumption of the CMOS thermal wind sensors, however, are reported to be higher [1,2,3,6] than its MEMS counterparts. Depending on the thermal flow sensor is fabricated either on the silicon supporting structure thinned by MEMS techniques, or on thick silicon substrate by standard CMOS technology, the thermal gas-flow sensors can be generally classified into two categories: MEMS or CMOS thermal gas-flow sensors.

The following literature review is firstly split into two sections: thermal anemometer and calorimetric flow sensors. In each section, both the MEMS and CMOS thermal gas-flow sensors will be introduced in aspects of working principle, operating mode, readout circuit and packaging, etc.

1.2.1 Thermal Anemometer

The first thermal gas-flow anemometer fabricated on silicon was presented by Van Putten et al.(1974) in TU Delft [42]. The anemometer adopted the thermoresistive principle and its readout configuration was a Wheatstone bridge consisting of four p-type diffused resistors. The chip, mounted on a ceramic substrate, was placed in a tube with its plane in parallel to the flow to be measured. Beginning with the hot-film principle, the
sensor was developed to an integrated silicon double bridge anemometer[43] in 1983 in the same group.

Tai et al. (1985) firstly applied the newly emerging MEMS micro-fabrication techniques to develop another thermoresisitve silicon flow anemometer, which is consisted of a polysilicon bridge[44]. The underlying silicon of the flow sensing elements (resistors, thermopiles and etc) are selectively etched away such that the supporting structure can be well (thermally) isolated from the massive silicon substrate. Thus, most of the heat transfer should be due to the gas-flow while other thermal losses due to heat transfer through silicon substrate or electrical leads can be minimized. This work prompted great interest in the development of MEMS-based flow sensors which continues until this day.

Stemme et al. (1988) reported a gas-flow anemometer (Figure 1- 4), with the heater and temperature sensors (diodes) are located on a silicon cantilever (0.3mm x 0.4mm x 50µm) for thermal isolation. The heating resistor was thermally isolated from the downstream temperature sensor using a polyimide trench [45]. In contrast to the conventional thermal anemometer, the heating resistor is controlled by using the pulse-modulation of current to keep the overheat temperature of the sensor, ΔT, constant. The output pulse-width ratio is then a sensitive measure of gas flow velocity. The velocity measured error is ±3% in the range of 2-30 m/s range. The gas-flow sensors with diodes as temperature sensors were also published in [46].

![Figure 1- 4 The sensor element is located on a silicon cantilever [45]](image)

In 1992, Yoon and Wise (1992) presented an integrated mass flow sensor with on-chip CMOS interface circuits, which were capable of measuring gas type, flow velocity, direction, temperature, and pressure [47]. The sensors were suspended on MEMS dielectric windows with areas of 0.5 mm x 0.5 mm (Figure 1- 5). In flow velocity sensing, the heater and detector were interleaved to achieve tight thermal coupling. With the
window heated and maintained at constant overheat, i.e. in CTD mode, gas was allowed to flow over the chip surface with increasing the convective heat flow. The input power was required to be increased to maintain the overheat temperature to be constant. The increased electrical power was used to indicate the flow velocity. This sensor can also measure the flow direction by using the calorimetric sensing principle.

Hung et al. (2000) developed a thermal flow sensor with the mesh-membrane structure [48] (Figure 1-6). The sensor was fabricated by using MEMS techniques to deposit an initial titanium barrier layer with a thickness of approximately 200 Å on a silicon substrate and then a platinum layer with a thickness of 1,800 Å. The thermoresistor was patterned using a standard lift-off technique. For flow velocities
greater than 1.5 m/s, the flow meter incurred a power consumption of 14.56mW and demonstrated a sensitivity of approximately \(0.01433 \text{ mA (m/s)}^{-1/2}\) when operated in a constant-voltage mode (CV mode). Finally, in a constant current mode, the device was found to have a sensitivity of more than \(7.98 \text{ mV (m/s)}^{1/2}\) and a power consumption of 45.10mW [2]. According to [48], the main advantages of this sensor are a simpler fabrication, an improved reproducibility, a greater sensitivity and an enhanced linearity.

In 2003, Chen et al. (2003) presented a hot-wire anemometer (HWA) which was enabled by a three-dimension assembly technique called plastic deformation magnetic assembly (PDMA) [49]. As shown in Figure 1-7, the HWA used a thermal element (hot wire) made of Pt/Ni/Pt film with a measured TCR of 2,700 ppm/°C. The thermal element was elevated from the substrate to a predetermined height that corresponded to the length of the support prongs. By elevating the thermal element away from the bottom of the velocity boundary layer, the thermal element could experience greater fluid flow velocity and exhibit better sensitivity[50].
Domínguez et al. (2008) created a wind sensor for use in Martian atmosphere on a space probe. Pyrex structures were used to maximize thermal isolation to increase sensor sensitivity since Martian pressure is very low which impedes heat convection compared to normal atmosphere [51]. It uses a closed thermal feedback loop based on thermal sigma–delta modulation. The sensitivity is expected to be 0.5 m/s in a Mars-like environment. Liu et al. (2009) present a novel MEMS thermal anemometer system realized by a technique using a film depositing processes and incorporating a standard printed circuit [52]. Sensor electrodes and electronic circuits are preprinted on a flexible PCB (printed circuit board). The sensor can be packed efficiently at high-density and integrated with signal processing circuits without additional pads. Polymer substrates have been used to create flexible sensors that can be placed on curved surfaces [53,54].

The commercialized gas-flow sensor from the Fraunhofer Institute can be manufactured at extremely low cost, as the processing is CMOS compatible and the small chip dimensions enable several hundred sensors to be fabricated on a single wafer. The sensor can measure bidirectional air mass flow velocities. Photographs of the sensor chip can be seen in Figure 1-8 and Figure 1-9, respectively. MEMS gas flow sensors are also available from Leister Process Technologies, Switzerland, and SLS Micro Technology GmbH, Germany [1].

![Figure 1-8 Side view of the thermal air flow sensor by Fraunhofer Institute for Silicon Technology, Germany.](image)
1.2.2 Calorimetric gas-flow sensors

The first commercialized calorimetric flow sensor developed by Honeywell Physical Sciences Center (1987) consists of temperature sensitive platinum resistors laminated within a 1 mm thin thermal isolated silicon nitride layer, which are suspended in the form of two bridges over an etched pit in the silicon[55] (Figure 1- 10). This thermo resistive sensor chip is located in a flow channel. The heater is kept on a constant temperature and creates by zero-flow a symmetrical temperature distribution around itself. The upstream and downstream temperature sensing resistors measure the asymmetry of the temperature distribution caused by the flow. The resistance difference can be evaluated using a Wheatstone bridge and a differential instrumentation amplifier [6].

In the flow sensor developed by Moser et al. (1993), a polysilicon heater and n/p-silicon thermopiles as temperature sensors are in use. The sensor was fabricated by using the standard CMOS process followed by silicon MEMS processing [56]. Integrated
thermopiles were placed on free-standing cantilever beams and measured the temperature differences between the heated tips of the beams and the bulky silicon substrates as the gas flow varied. Further developments of this sensor with thermopiles made from aluminium/polysilicon were published in [57,58,59]. The two-dimensional version of this sensor was published in [58] (Figure 1-11 and Figure 1-12). The measured error of the flow direction was less than ±3.1° with power consumption of 5mW.

Figure 1-11 Operating principles and schematic cross-section of the microbridge-based gas flow sensor. Two poly-silicon aluminum thermopiles measure the thermal asymmetry $\Delta T$ induced by a gas flow. [58]

Figure 1-12 SEM Micrograph of the sensor shown in Figure 1-12. [58].
Kaltsas et al. (1999) developed an integrated thermal gas-flow sensor that implements a heater and a pairs of thermopiles, symmetrically situated on both sides of the heater (Figure 1-13). The flow measurements were performed in both the calorimetric and anemometer principles with the different modes of operation: constant voltage (CV), constant current (CC) and constant temperature (CT) [60,61,62,63].

![Flow direction](image)

**Figure 1-13** thermopiles from polysilicon and aluminum (Al). Thermopile hot contacts were placed close to the polysilicon heater while cold contacts were placed on the silicon substrate [60].

Van Oudheusden et al. at TU Delft, developed a series of flow sensors for measuring flow rate and flow direction [64,65,66,67]. In these sensors, thermopiles (silicon–aluminium coupling) in a two-dimensional arrangement are in use. The heater resistor is located on a suspended thin silicon plate for improvement of the heat isolation. Makinwa and Huijsing(2002) in the same lab developed the “smart wind sensor” by combining a two-dimensional thermal flow sensor and all the required interface electronics on a single chip in standard CMOS technology [3,34,35,40,68,69,70]. The wind sensor chip was composed of a square silicon substrate on which four heaters, four thermopiles and a central diode in a thick silicon substrate, as shown in Figure 1-14(a). The packaging of the sensor is shown in Figure 1-14(b). The on and off-chip diode measures the ambient and on-chip temperature to operate the sensor in CTD mode. Three on-chip thermal sigma-delta (TΣΔ) modulators control and simultaneously digitize the flow-dependent heat distribution in the sensor. Their bitstream outputs represent two orthogonal components of wind velocity and the total heating power dissipated in the sensor. In the study, it showed the sensor was capable of measuring wind speed and direction with an accuracy of ±4% and ±2°, respectively, over the range 1–25 m/s, with power consumption of appr. 450mW [35].
Kim et al. (2003) proposed a circular-type thermal flow direction sensor consisting of a heater surrounded by four sensing resistors made all by Pt [37]. As shown in Figure 1-15(a), the resistor in the center, $R_h$, is the heater and $R_n$, $R_s$, $R_e$, $R_w$ are used as temperature sensor. The sensor can evaluate both the flow direction and the flow velocity by measuring the relative changes in the output signals of the four resistors and monitoring the changes in the power signal supplied to the heater unit, respectively [39]. The sensor contacts the gas-flow directly and the packaging of the sensor is shown in Figure 1-15(b).
Figure 1-15 Thermal wind sensor proposed by Kim (a) schematic view (b) package [37]

Bruschi et al. (2005) created a two-dimensional wind sensor based on the thermopiles in a calorimetric fashion over a silicon oxide membrane. Two thermally isolated heaters instead of one were used in between two thermopiles and thermal feedback maintained equal temperature between the two heaters under varying flow conditions[71, 72, 73]. The device consists of a cylinder with a channel network connecting the internal flow sensors with the lateral surface. The sensor is operated in CP mode and the power required by the sensor is only 4 mW with a sensitivity of 0.002 sccm (standard cubic cm per minute). The uncalibrated wind velocity and direction error can be ±12% and ±2° [73].

Tong et.al at South-east University developed the flow sensor with an integrated amplifier in the sensor chip in 1987. Heater and temperature sensors are field effect
transistors [74]. Qing et. al proposed two-dimensional CMOS thermal wind sensor with poly diodes as its temperature sensors [75]. Q. Huang et al. in the same lab developed a series of two-dimensional thermal wind sensors with two different packaging [76,77,78,79]. One is that the front side of the silicon wind sensor was flip-chip packaged on the ceramic substrate using a copper pillar bumps technology [76]. The thermal interactions between the sensor and the airflow were achieved via the copper pillar bumps and the thin ceramic substrate. However, if both the sensing parts and heaters are fabricated on silicon substrate by using a standard IC fabrication process, wet etching is usually used to undercut the substrate so that heaters are fabricated on a suspended film to minimum the heat capacity. In this case, the fragile structure is difficult to be packaged. The other is that the sensor was fabricated directly on ceramic wafers [77, 78] or glass wafers [79]. However, if the sensing parts are fabricated directly on ceramic substrate or glass, unacceptable deviations of the sensing thermistors will be introduced. Inconsistency of the thermistor’s resistance and temperature coefficient greatly increases the calibration cost. In the latest study, Dong et al. reported a new type of thermal wind sensor which is consisted of two separate chips: a sensing chip and a packaging chip [5], as shown in Figure 1-16. The heaters are fabricated on packaging chip (ceramic substrate) by using lift-off process, and the sensing parts are fabricated on sensing chip (silicon substrate) by using a standard IC process. Wafer-level Au–Au bonding process was used to bond the sensing chip on the front side of the packaging chip. It is found that the consistency of the sensing parts fabricated on silicon substrate by using a standard IC process has been improved greatly compared to the reference designs. Since the sensor and heater are in different chip, there is no fragile structure to be packaged. The sensor is operated in CTD mode. With overheat temperature of 6 °C, the power consumption is from 2mW to 111.2mW for wind speed range of 0m/s to 40m/s. The errors in the measured flow speed and direction are ±4% and ±2° after calibration, respectively.
Cubukcu et al. (2010) presented a two-dimensional thermal flow sensor with sub-mW power consumption [80]. The sensor is composed of a heater and several temperature sensors around it. Five thermistors are located on a 1.4µm thick, 1mm wide SiNₓ–SiOₓ diaphragm which is well thermally isolated from the silicon substrate to minimize the substrate thermal conduction loss (Figure 1-17). Highly sensitive amorphous germanium thermistors are used to provide a high temperature resolution and to achieve low velocity measurement limit (1 cm/s) at low power consumption (0.177mW_{rms}). In this design, deviations of resistance and temperature coefficient of the sensing thermistors, which are made of amorphous germanium, are much larger than the commonly used poly-silicon resistors. Therefore, each thermistor has to be extracted using its own temperature coefficient.
Sensirion AG, Switzerland, produces a flow sensor including the CMOS measurement electronics on the same chip [81]. The flow meters are based on Sensirion's CMOSens technology, and use the calorimetric flow measurement principle. They combine the thermal sensor element with the amplification and A/D converter circuit on one single CMOS chip (Figure 1-18). The sensor specifies $3.5V_{\text{IN-MIN}}$ and $3.5mA_{\text{MIN}}$ for the operation of its mass flow meter SFM4100 for gases with lowest power consumption. These specifications correspond to a power of $12.25mW_{\text{MIN}}$.  

Figure 1-17 (a) Magnified view of the thermal flow sensor and (b) a photograph of the realized chip [80].
Figure 1-18 Photograph of a CMOSens chip. On the right is the flow sensing element, and on the left the CMOS electronics [81].

The performance of most gas-flow sensors mentioned in this literature review is summarized in Table 1-3.
### Table 1-3 Summary of performance of the gas-flow sensors in the above literature review

<table>
<thead>
<tr>
<th>Ref</th>
<th>Time</th>
<th>Fabrication</th>
<th>Temp. Sensor</th>
<th>Interface circuit</th>
<th>Sensing range</th>
<th>Resolution</th>
<th>Power Consumption</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Anemometer</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Van Putten[42]</td>
<td>1974</td>
<td>Bipolar</td>
<td>Resistor</td>
<td>Wheatstone bridge</td>
<td>0~2m/s</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Tai[44]</td>
<td>1988</td>
<td>MEMS</td>
<td>Resistor</td>
<td></td>
<td>2~30m/s</td>
<td>±3% (Speed)</td>
<td>1.63mW</td>
</tr>
<tr>
<td>Stemme[45]</td>
<td>1988</td>
<td>MEMS</td>
<td>Diode</td>
<td></td>
<td>0~5m/s</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Yoon[47]</td>
<td>1992</td>
<td>MEMS</td>
<td>Resistor</td>
<td>Wheatstone bridge</td>
<td>0~11 m/s</td>
<td>CV 2V: 14.56 mW CV 4V: 50.83 mW CC 12.96mA: 45.10 mW CC 23.08 mA: 157.61 mW</td>
<td></td>
</tr>
<tr>
<td>Hung[48]</td>
<td>2000</td>
<td>MEMS</td>
<td>Resistor</td>
<td></td>
<td>0~1m/s</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Chen[49]</td>
<td>2003</td>
<td>MEMS</td>
<td>Resistor</td>
<td></td>
<td>0~20m/s</td>
<td>0.3m/s (speed)</td>
<td>14mW</td>
</tr>
<tr>
<td>Dominguez[51]</td>
<td>2008</td>
<td>MEMS</td>
<td>Resistor</td>
<td>Thermal ΣΔ</td>
<td>0~15m/s</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Liu[52]</td>
<td>2009</td>
<td>MEMS</td>
<td>Resistor</td>
<td>Wheatstone bridge</td>
<td>0~15 m/s</td>
<td>30mW</td>
<td></td>
</tr>
<tr>
<td><strong>Calorimetric</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Johnson[55]</td>
<td>1987</td>
<td>MEMS</td>
<td>Resistor</td>
<td>Wheatstone bridge</td>
<td>0~1.3m/s</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Tong[74]</td>
<td>1988</td>
<td>CMOS</td>
<td>MOSFET</td>
<td></td>
<td>0~25m/s</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Oudheusden[41]</td>
<td>1992</td>
<td>CMOS</td>
<td>Thermopile</td>
<td></td>
<td>0~25m/s</td>
<td>5% (angle)</td>
<td>&lt;5mW</td>
</tr>
<tr>
<td>Moser[56]</td>
<td>1993</td>
<td>MEMS</td>
<td>Thermopile</td>
<td></td>
<td>0~25m/s</td>
<td>±3.1% (angle)</td>
<td></td>
</tr>
<tr>
<td>Qing[75]</td>
<td>2001</td>
<td>CMOS</td>
<td>Diode</td>
<td></td>
<td>0~10m/s</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Makinwa[3]</td>
<td>2002</td>
<td>CMOS</td>
<td>Thermopile</td>
<td>Thermal ΣΔ</td>
<td>1~25m/s</td>
<td>±4% (speed) ±2° (angle)</td>
<td>450mW</td>
</tr>
<tr>
<td>Kim[39]</td>
<td>2004</td>
<td>MEMS</td>
<td>Resistor</td>
<td>Wheatstone bridge</td>
<td>0~15m/s</td>
<td>±5° (speed)</td>
<td></td>
</tr>
<tr>
<td>Shen[78]</td>
<td>2010</td>
<td>MEMS</td>
<td>Resistor</td>
<td>Wheatstone bridge</td>
<td>0~8m/s</td>
<td>±0.3m/s (speed) ±5° (angle)</td>
<td>50mW</td>
</tr>
<tr>
<td>Cubukcuca[80]</td>
<td>2010</td>
<td>MEMS</td>
<td>Resistor</td>
<td>Wheatstone bridge</td>
<td>0~5m/s</td>
<td></td>
<td>0.177mW</td>
</tr>
<tr>
<td>Dong[5]</td>
<td>2012</td>
<td>MEMS</td>
<td>Resistor</td>
<td>Wheatstone bridge</td>
<td>0.5~40m/s</td>
<td>±4% (speed) ±2° (angle)</td>
<td>2 mWmin 111.2 mWmax</td>
</tr>
</tbody>
</table>

### 1.3 Motivations and Objectives

As has been shown in previous sections, thermal wind sensors fabricated in IC technology can measure the wind speed and direction without any moving parts, resulting in virtually no maintenance. Despite this overwhelming advantage, only a
minority of the wind sensors applied today are based on IC technology. One reason for this may be the fact that the conventional mechanical wind sensors have been used successfully for decades, so engineers hesitate to adopt a new technology. Moreover, as illustrated in Table 1-3, the majority of the existing thermal sensors are fabricated mostly using MEMS etching process to reduce the thermal mass of the sensor, thus the total heating power consumption. However, till this day, the MEMS foundry service is not fully commercialized, thus the non-CMOS-compatible steps in MEMS fabrication (such as etching and sacrificial material release, etc.) can significantly increase the unit manufacturing cost of the sensor. Furthermore, the mechanical strength of the thermal wind sensor is often greatly reduced by the MEMS etching process such that they are prone to be damaged in the packaging process. As we know, the low manufacture cost and good robustness are exactly the advantages of the thermal wind sensors, compared to traditional mechanical sensors. Thus, in this thesis, thermal wind sensor based on MEMS processing are ruled out. The thermal wind sensors fabricated only with standard CMOS technology can make use of the mature CMOS foundry service to minimize the unit manufacture cost. More importantly, its relatively thick silicon substrate (500µm~800µm) can guarantee the sensor’s reliability both in packaging process and in real use.

The main challenge of massive commercialization of the CMOS thermal wind sensor is its relatively high power consumption. The lowest reported power consumption of a CMOS thermal wind sensor is about 450mW [3], as shown in Table 1-3. Wind sensors are often located in inaccessible places for long-term monitoring purposes. Thus, they can only be powered by batteries charged by solar cells. The power consumption of CMOS wind sensors of several hundreds of mW rules out its use in such applications. Therefore, the main aim of this thesis is to reduce the total power consumption of CMOS thermal wind sensors such that they can replace the mechanical wind sensors in such applications. Improvements in both the sensor’s operating mode and its interface circuitry will be mainly studied to achieve competitive power consumption and sensing accuracy, compared to its mechanical counterparts.

As introduced in literature review, the CMOS thermal wind sensor proposed by Makinwa can combine the wind sensing front-end and its interface circuitry in the same CMOS chip[3]. Besides this advantage, its thermal behavior modeling, operating mode
control, interface circuitry and packaging have been extensively studied in [3]. Therefore, this design will be taken as the main reference design in this thesis and its layout of the heater/thermopile and the packaging will be reused. This thesis will mainly focus on the innovation of the sensor’s operating modes and interface circuitry to achieve more power-efficient CMOS thermal wind sensor design than [3]. The power consumption of this design is targeted at 50mW, which is comparable to that of the mechanical wind sensors with similar sensing resolution. Table 1- 4 compared the specifications of this design and the reference design [3].

<table>
<thead>
<tr>
<th>Specification</th>
<th>This design</th>
<th>Ref design[3]</th>
</tr>
</thead>
<tbody>
<tr>
<td>Process</td>
<td>CMOS</td>
<td>CMOS</td>
</tr>
<tr>
<td>Wind sensing range</td>
<td>1~25m/s</td>
<td>1~25m/s</td>
</tr>
<tr>
<td>Speed resolution</td>
<td>±4%</td>
<td>±4%</td>
</tr>
<tr>
<td>Direction resolution</td>
<td>±2°</td>
<td>±2°</td>
</tr>
<tr>
<td>Power consumption</td>
<td>50mW*</td>
<td>450mW</td>
</tr>
</tbody>
</table>

*Estimated by the power consumption of the mechanical wind sensors with similar resolution

1.4 Thesis Organization

![Diagram](image)
Besides this introductory chapter, this thesis consists of six chapters. The organization of this thesis is shown in the block diagram of Figure 1-19. The basic principles of the proposed two-dimensional CMOS thermal wind sensor and its operating modes are first described in Chapter 2. The alternative operating modes are analyzed and compared in terms of their ease of realization and power consumption. By applying the CP mode instead of the CTD mode, it is shown that the power consumption of the sensor can be accurately controlled and, significantly reduced compared to the previous design [3].

Chapter 3 then discusses the system-level design of the sensor’s interfacing ADC, that can process the signal in both thermal and electrical domain. A thermal ΣΔ modulator is found to be well suited to the task of digitizing the flow-induced thermal signals in the thermal wind sensor. It is shown that the modulator’s quantization noise could be one of the main obstacles to reduced power consumption. Quasi-linear models of the thermal sigma-delta modulator were developed to compare first and second-order topologies in terms of noise and stability. The analysis shows that a second-order topology can significantly reduce in-band quantization noise and thus facilitate a significant reduction in the sensor’s power consumption for a given sensing resolution. Details of an appropriate decimation filter for the second-order system are also described.

In Chapter 4, dynamic-offset-cancellation techniques (chopping and auto-zeroing) are discussed and compared in terms of their residual noise and offset. In contrast to a reference design [3], the sensor’s interface circuitry was chopped instead of auto-zeroed.

In Chapter 5, the two realizations of the CMOS thermal wind sensors are demonstrate the effectiveness of both the system and circuit level improvements. The most recent prototype achieves a wind speed and angle inaccuracy of ±4% and ±2°, respectively, while dissipating only 25mW. Moreover, it turns out that the same sensor can be used as a temperature sensor with an untrimmed error of ±1°C between -40°C and 50°C. The results are also compared with previous works [3,5,8].

The thesis ends with a summary and conclusions in Chapter 6. Special sections have been included to highlight the original contributions and possible future trends to improve the work described in this thesis.
Chapter 2
A 2-D CMOS Thermal Wind Sensor

This chapter describes the operating principles of the proposed two-dimensional CMOS thermal wind sensor front-end design which will be used in this design. Since both the sensor’s average overheat temperature $\Delta T$ and the flow-induced temperature gradient $\delta T$ can either be measured or regulated, several operating modes are possible. Based on the characteristics of the sensor in these different modes, the most power-efficient mode will be chosen.

2.1 Introduction

In this thesis, a two-dimensional CMOS thermal wind sensor (Figure 2-1) realized in a standard CMOS process will be used to measure wind speed and direction. As shown in Figure 2-1(a), the wind sensor consists of a center-heated silicon chip glued to one side of a Aluminum Oxide ($\text{Al}_2\text{O}_3$) ceramic disc (0.25mm-thick), which has a good thermal conductivity. The sensor chip is bonded with metal wires and then encapsulated for protection purposes. The wind is passed over the other side of the ceramic disk, and so the chip makes good thermal contact with the flow while still being protected from direct mechanical contact. The wind cools the sensor asymmetrically, inducing a temperature gradient $\delta T$ on the surface of the ceramic disc. Wind speed and direction can then be determined by measuring orthogonal components $\delta T_{ns}$ and $\delta T_{ew}$ of the flow-induced temperature gradient with two pairs of on-chip thermopiles as shown in Figure 2-1(b). For example, the thermopiles at the north and south side of the chip are series-connected to measure the east-west component of the temperature gradient, i.e. $\delta T_{ew}$. The four on-chip heaters are made of poly-silicon resistors because they can be electrically isolated from the substrate and thus minimize crosstalk. P+ silicon/aluminum thermopiles are then used as these provide the best signal-to-noise ratio in standard CMOS process [3]. The wind sensor as shown in Figure 2-1 was first described in [41], and then developed into a commercial product by Mierij Meteo BV[82]. The latest version
of this type of sensor (i.e. reference design [3]) can measure wind speed and direction with errors of ±4% and ±2˚ respectively, while consuming about 450mW at a maximum wind speed of 25m/s.

2.2 Operating Modes

Since both the sensor’s average overheat ΔT as well as the flow-induced temperature gradient δT can either be measured or regulated, several operating modes are possible. Depending on whether the sensor’s overheat temperature ΔT or the total power consumption is kept constant, the operating modes can be subdivided into constant temperature difference (CTD) mode or constant power (CP) mode, as introduced in Chapter 1. Depending on whether the flow-induced temperature gradient δT is measured or regulated, the operating modes can also be subdivided into temperature gradient Mode (TG) and temperature balancing (TB) mode. According to different combinations, there are mainly four types of operating modes, i.e. CTD-TG, CP-TG, CTD-TB and CP-TG modes. The characteristics of the proposed CMOS wind sensor are greatly influenced by the chosen operating mode.

2.2.1 CTD Mode versus CP Mode

The total heater power dissipation P and the overheat ΔT above ambient temperature are the two important parameters that govern the operation of a thermal
wind sensor. In practice, one of the two parameters is kept constant while the other one is varied. Thus the sensor can work in two different operating modes: constant power (CP) mode or constant temperature difference (CTD) mode. In CP mode, as shown in Figure 2-2(a), a constant heating power $P$ is dissipated in the sensor while the overheat $\Delta T$ will then vary with flow speed. However, in CTD mode as shown in Figure 2-2(b), a feedback loop maintains the sensor at a constant overheat $\Delta T$ above ambient, in which case the heating power $P$ will increase with flow speed.

Constant Power Mode

![Diagram of Constant Power Mode]

(a)

Constant Temp. Difference Mode

![Diagram of Constant Temp. Difference Mode]

(b)

Figure 2-2 Operating Modes (CTD vs CP)

**CTD Mode**

In CTD mode, a feedback loop which consists of both an on-chip and an off-chip temperature sensor is required to maintain the sensor at a constant overheat $\Delta T$. The orthogonal components ($\delta T_{ns}$ and $\delta T_{ew}$) of the flow-induced temperature gradient, which can be measured by the thermopiles [3], are described in (2-1):
\[ \frac{\delta T_{ns}}{\Delta T} = S \sqrt{U_{ns}}, \quad \frac{\delta T_{ew}}{\Delta T} = S \sqrt{U_{ew}} \] (2-1)

where \( \Delta T \) is the constant overheat, \( S \) is a constant that depends on sensor geometry and fluid properties, \( U_{ns} \) and \( U_{ew} \) are the orthogonal components of flow velocity. Wind speed \( U \) and direction \( \Phi \) can be determined from (2-2) and (2-3), respectively:

\[ U = \sqrt{U_{ns}^2 + U_{ew}^2} = \sqrt{\frac{\delta T_{ns}^2 + \delta T_{ew}^2}{S\Delta T}} \] (2-2)

\[ \phi = a \tan \left( \frac{U_{ns}}{U_{ew}} \right) = a \tan \left( \frac{\delta T_{ns}}{\delta T_{ew}} \right) \] (2-3)

**CP Mode**

In CP mode, rather than regulating the overheat \( \Delta T \), a constant heating power \( P \) is dissipated in the heater. Noting that the sensor’s overheat \( \Delta T \) will not be a constant but be governed by King’s law, the resulting orthogonal components in CP mode, i.e. \( \delta T_{ns} \) and \( \delta T_{ew} \), can be described in (2-4):

\[ \delta T_{ns} = \frac{P \sqrt{U_{ns}}}{C + D \sqrt{U_{ns}}}, \quad \delta T_{ew} = \frac{P \sqrt{U_{ew}}}{C + D \sqrt{U_{ew}}} \] (2-4)

where \( C \) and \( D \) are sensor constants. As shown in (2-4), the temperature gradients, \( \delta T_{ns} \) and \( \delta T_{ew} \), are monotonically increasing functions of flow speed and are independent of variations in ambient temperature.

**CP versus CTD**

Figure 2- 3 shows the relationship between the normalized temperature gradient \( \delta T \) and the square root of wind speed \( U \). For CTD mode, the temperature gradient \( \delta T \) has a simple square-root law relationship with the wind speed, as shown in (2-1). In CP mode, however, the relationship between the normalized temperature gradient \( \delta T \) and square root of wind speed is more complex, as illustrated in (2-4). Compared to CTD mode, an extra sensor constant in (2-4) must be calibrated, which may result in increased sensing.
inaccuracy. Moreover, the sensitivity of the sensor in CP mode, is relatively higher at low wind speeds and lower at high wind speeds. The wind tunnel measurement results in reference design [3] show that the temperature δT in CP mode can flatten out and even decrease when the wind speed increases beyond a certain threshold (about 30m/s). Therefore, one of the drawbacks of CP mode is that is wind speed sensing range is limited.

![Figure 2-3 Normalized temperature gradient versus square root of wind speed (CP vs CTD)](image)

In CP mode, since the wind sensor’s overheat T varies with flow speed, its transient response might be expected to slower than when it is operated in CTD mode. Therefore, in the reference design [3], CTD mode was chosen. The required overheat regulation loop is illustrated in Figure 2-4. It consists of a comparator and two PNP bipolar transistors serving as on-chip and off-chip temperature sensors. Without calibration, the inaccuracy of the PNP temperature sensors was only expected to be about ±3°C [21], mainly due to process variation. Therefore, the overheat temperature ΔT (Figure 2-4) should be larger than 2X3= 6°C to avoid the risk that some of the wind sensor samples may fail to heat up at all. To leave some margin, the nominal overheat in the reference design [3], was set to 10°C. As from King’s law, the overheat ΔT is linearly proportional to the total power consumption P. Measurements on the reference design show that an overheat of 10°C can lead to a power dissipation of about 450mW. For application in
weather stations powered by solar cells or just batteries, this level of power consumption is simply not acceptable.

Compared to operation in CTD mode, operation in CP mode does not require an overheat regulation loop. Thus, both the complexity and manufacture cost of the sensor system can be reduced accordingly. Furthermore, since the overheat temperature of the thermal sensor is no longer limited by temperature-sensor inaccuracy, it can be regulated by modulating the duty-cycle of the heating resistor's drive current or voltage. Thus, the heating power can be accurately controlled then reduced.

As introduced in Chapter 1, the main motivation of this work is to reduce the sensor's power consumption. Moreover, literature[3] showed that there was no measurable difference in the wind sensor's transient response in CP and CTD modes. Thus, the use of CP mode rather than CTD mode will be explored in this work, at the cost of less sensing resolution at relatively high speeds, limited wind sensing range and more calibrated parameters. The comparison table of the CP and CTD mode is shown below in Table 2-1.
Table 2-1 Comparison Table between CP and CTD mode

<table>
<thead>
<tr>
<th>Operating Mode</th>
<th>CP Mode</th>
<th>CTD Mode</th>
</tr>
</thead>
<tbody>
<tr>
<td>Formula</td>
<td>(non-square-root law)</td>
<td>(square-root law)</td>
</tr>
<tr>
<td>$\delta T_{ns} = \frac{P \sqrt{U_{ns}}}{C + D \sqrt{U_{ew}}}$</td>
<td>$\delta T_{ew} = \frac{P \sqrt{U_{ew}}}{C + D \sqrt{U_{ew}}}$</td>
<td>$\frac{\delta T_{ns}}{\Delta T} = S \sqrt{U_{ns}}$ $\frac{\delta T_{ew}}{\Delta T} = S \sqrt{U_{ew}}$</td>
</tr>
<tr>
<td>Constants to be calibrated</td>
<td>2</td>
<td>1</td>
</tr>
<tr>
<td>Overheat regulation loop required</td>
<td>No</td>
<td>Yes</td>
</tr>
<tr>
<td>Heating power consumption</td>
<td>Controllable</td>
<td>Minimum heating power is limited by temperature-sensor inaccuracy</td>
</tr>
<tr>
<td>Transient response time</td>
<td>Almost the same[3]</td>
<td></td>
</tr>
</tbody>
</table>

2.2.2 TG Mode versus TB Mode

As introduced in section 2.1, if wind speed and direction are determined by directly measuring the wind-induced temperature gradient $\delta T$, the operating mode is referred to as the temperature gradient (TG) mode. In contrast, the temperature gradient $\delta T$ can be cancelled by dynamically adjusting the power consumption in the four separate heaters. The resulting heater power gradient $\delta P$ can be read out to also determine the wind speed and direction. This working mode is referred to temperature balancing (TB) mode.

In TG mode, the temperature gradient $\delta T$ will first be converted into an electrical signal by the thermopiles, as shown in Figure 2-5. This signal is firstly amplified and converted into a digital reading. Because this measurement chain is an open loop system, the non-idealities (non-linearity, sensitivity variations etc.) of the thermopiles as well as the interface circuit will both influence output of the sensor (Figure 2-5). Alternatively, the temperature gradient $\delta T$ can be cancelled by dynamically driving the two pair of opposing heaters in the sensor, as shown in Figure 2-6. Information about the wind flow is now contained in the resulting heating power gradient $\delta P$. This null-balance mode of operation is referred to as the temperature balance (TB) mode.

In reference design [3], the TB mode was applied by using the topology shown in Figure 2-6. Here a feedback loop cancels the temperature difference $\delta T_{ns}$ measured by
north-south thermopile, by driving either the north or south heaters (poly-silicon resistors) with pulses of constant power $P_{ref}$. The average value of these pulses is then a digital representation of the differential heater power $\delta P_{ns}$ required to cancel $\delta T_{ns}$. In a similar manner, $\delta P_{ew}$ is determined by another east-west thermal balancing loop. Wind speed and direction can then be determined from $\delta P_{ew}$ and $\delta P_{ns}$.

Compared to TG mode, the thermopiles are only used as null detectors in a feedback loop in TB mode. Thus, the sensor’s output will not be much influenced by the nonlinearity and gain of the thermopile and its readout circuit. Besides the existing thermopiles and heaters, the thermal balancing loop only requires an extra 1-bit comparator to convert the power gradient $\delta P$ into a digital reading directly. The interface circuitry design of the wind sensor is greatly simplified. Thus, TB mode instead of TG mode will be used.

Figure 2-5 Schematic of open loop measurement (TG mode)
In section 2.2.1, the equations describing wind speed and direction in the CTD-TG and CP-TG modes have been already discussed. The equations describing the CP-TB and CTD-TB modes will be introduced in the following.

In TB mode, the orthogonal components of the power gradient $\delta P$, i.e. $\delta P_{ns}$ and $\delta P_{ew}$, will be proportional to the cancelled temperature differences $\delta T_{ns}$ and $\delta T_{ew}$, respectively. Therefore, based on (2-1), the differential heating power $\delta P_{ns}$ and $\delta P_{ew}$ in CTD-TB mode are described in (2-5):

$$
\frac{\delta P_{ns}}{\Delta T} = S \sqrt{U_{ns}}, \quad \frac{\delta P_{ew}}{\Delta T} = S \sqrt{U_{ew}}
$$

(2-5)

where $\Delta T$ is the constant overheat, $S$ is a constant that depends on sensor geometry and fluid properties, $U_{ns}$ and $U_{ew}$ are the orthogonal components of flow velocity $U$.

Similarly, based on (2-4), the differential heating power $\delta P_{ns}$ and $\delta P_{ew}$ required to cancel the air-flow induced temperature gradient $\delta T$ of the sensor in CP-TB mode are derived in (2-6):

$$
\frac{\delta P_{ns}}{P} = \frac{\sqrt{U_{ns}}}{E + F \sqrt{U_{ns}}}, \quad \frac{\delta P_{ew}}{P} = \frac{\sqrt{U_{ew}}}{E + F \sqrt{U_{ew}}}
$$

(2-6)
where P is the total constant power dissipated in the sensor, E and F are constants
which need to be calibrated.

In conclusion, TB mode will be combined with CP mode in this work to achieve lower
power consumption, better linearity of the measurement and simplified interface circuitry
at the same time.

2.3 Summary

This chapter briefly discussed the proposed two-dimensional thermal wind sensor
and its possible operating modes. Since both the sensor’s overheat temperature ΔT and
flow-induced temperature gradient δT can be regulated or measured, the sensor can be
operated in four different modes: CTD-TG, CTD-TB, CP-TG, CP-TB respectively. In this
work, the sensor will be operated in CP-TB mode. The reasons for this are described as
follows. Firstly, CP mode does not require an extra control loop to regulate the overheat
ΔT, and thus simplifies the system. Secondly, CP mode also enables a reduction in
heater power, which, in CTD mode, is limited by the inaccuracy of the off-chip ambient
temperature sensor. Thirdly, TB mode is implemented since the thermopiles are just
used as zero-crossing detectors and so gain non-idealities of the thermopile and its
readout circuit, e.g. non-linearity, sensitivity variations etc., no longer influence the
sensor’s characteristics.

A summary of the equations governing the four different operating modes for thermal
wind sensors is shown in Table 2-2.

<table>
<thead>
<tr>
<th>Operating Mode</th>
<th>CTD-TG</th>
<th>CP-TG</th>
<th>CTD-TB</th>
<th>CP-TB</th>
</tr>
</thead>
<tbody>
<tr>
<td>Measured parameter</td>
<td>δT_{ns}, δT_{ew}</td>
<td>δT_{ns}, δT_{ew}</td>
<td>δP_{ns}, δP_{ew}</td>
<td>δP_{ns}, δP_{ew}</td>
</tr>
<tr>
<td>Formula</td>
<td>\frac{\delta T_{ns}}{\Delta T} = S\sqrt{U_{ns}}</td>
<td>\delta T_{ns} = \frac{P\sqrt{U_{ns}}}{C + DU_{ns}}</td>
<td>\frac{\delta P_{ns}}{\Delta T} = S\sqrt{U_{ns}}</td>
<td>\delta P_{ns} = \frac{\sqrt{U_{ns}}}{E + F\sqrt{U_{ns}}}</td>
</tr>
<tr>
<td></td>
<td>\frac{\delta T_{ew}}{\Delta T} = S\sqrt{U_{ew}}</td>
<td>\delta T_{ew} = \frac{P\sqrt{U_{ew}}}{C + DU_{ew}}</td>
<td>\frac{\delta P_{ew}}{\Delta T} = S\sqrt{U_{ew}}</td>
<td>\delta P_{ew} = \frac{\sqrt{U_{ew}}}{E + F\sqrt{U_{ew}}}</td>
</tr>
</tbody>
</table>
Chapter 3
Thermal ΣΔ Analog-to-Digital Conversion

This chapter discusses the design of the thermal sigma-delta (TΣΔ) analog-to-digital converter (ADC), which can interface the thermal wind sensor and convert the wind dependent differential heat loss δP of the sensor into a digital output. By digitizing the orthogonal components of δP (i.e. δP_{ns} and δP_{ew}), the wind speed and direction can then be computed. The TΣΔ modulator is realized with a temperature balancing loop, which cancels the temperature difference δT induced by the wind by driving opposing heaters in the sensor chip with pulses of constant power P_{ref}. The average value of the output bit-stream is then a digital representation of the δP/P_{ref}. Compared with electrical ΣΔ modulator, the input signal (heat loss δP) and summing node (chip’s thermal mass) of the TΣΔ modulator are both in the thermal domain. By incorporating the thermal sensor and heaters in a feedback loop, the TΣΔ modulator can be realized with rather simple circuitry, only by adding electrical comparators. Ideally, the resolution of the TΣΔ modulator should only be limited by the thermopile’s thermal noise such that the heating power consumption of the thermal wind sensor can be minimized for a given sensing resolution. However, the resolution of TΣΔ modulator with only the thermal filter as its loop filter is found to be limited by quantization noise, because noise-shaping provided only by the thermal filter is not sufficient. To overcome this limitation, a TΣΔ modulator which employs an additional electronic filter in the loop is proposed, to achieve more aggressive noise-shaping.

In Section 3.1, the operating principles of TΣΔ modulator will be introduced and compared with its electrical counterpart. Section 3.2 introduces a quasi-linear model of TΣΔ modulator which can be applied to separately analyze the quantization and thermal noise contribution to the in-band noise of TΣΔ modulators. By using this model, the noise performance of first-order and second-order TΣΔ modulator is then evaluated in Sections 3.3 and 3.4, respectively. In Section 3.4, a zero-tracking sinc2 decimation filter which is suitable for the second-order TΣΔ modulator is also discussed. Section 3.5 summarizes this chapter.
3.1 ΣΔ modulator: Operating Principle

This section starts with a brief explanation of the operating principles of the electrical ΣΔ ADC. The concept and properties of TΔΣ modulator are then introduced and compared with those of its electrical counterpart. This is followed by a description of the modeling of the thermal low-pass filter, which is used as the loop filter in TΣΔ modulator.

3.1.1 ΣΔ ADC: The Principles

A ΣΔ ADC consists of a ΔΣ modulator and a digital decimation filter (Figure 3-1). The ΔΣ modulator (Figure 3-2) comprises a feedback loop in which an analog signal $V_{IN}(t)$ is continuously balanced by a digital bit-stream $bs(n)$. This bit-stream is then converted into the analog domain by a DAC to obtain an instantaneous approximation of the input signal. This approximation is subtracted from the actual input signal $V_{IN}(t)$ to obtain the instantaneous quantization error $e(t)$ of the bit-stream. This error is continuously low-pass filtered by the low-pass loop filter and its output is thus a representation of the averaged quantization error of the bit-stream. The quantizer acts so as to drive this average error to zero, thus producing a bit-stream whose average value equals the input signal $V_{IN}(t)$ [3]. The decimation filter following the modulator removes the out-of-band quantization noise, resulting in the multi-bit output data $D_{out}$ (Figure 3-1).

![Figure 3-1 Block diagram of ΣΔ ADC](image-url)
According to the Nyquist theorem, the input signal of ADC must be sampled at a minimum frequency of twice the bandwidth \( f_b \) of the input signal to prevent aliasing. ADCs operated at \( 2f_b \) are referred to as Nyquist ADCs, while ADCs with faster sampling frequency than \( 2f_b \) are called as oversampling ADCs, and the ratio \( f_s/2f_b \) is defined as the oversampling ratio (OSR). Since the quantizer has finite resolution, the output will contain quantization noise. If the quantizer's input signal is "busy" enough, the quantization noise can be modeled as band-limited white noise which is uniformly distributed between DC and half the sampling frequency \( f_s/2 \). As for the Nyquist ADC, the quantization noise is all distributed in the signal-band (Figure 3-3a). However, if the input signal is oversampled, the quantization noise power will be spread over a larger frequency range as shown in Figure 3-3(b), which is called the noise spreading effect. The quantization noise in the band \( f_b \) to \( fs/2 \) can be then removed by decimation filter. Thus, the in-band quantization noise power will be reduced by the oversampling ratio, i.e. OSR. Oversampling enables sigma-delta ADCs to achieve a resolution higher than that of their own quantizer due to this "noise spreading" effect by \( \frac{1}{2} \) bit, i.e. 3dB resolution increase, per doubling of the OSR.

The loop filter can help to shape the spectrum of the quantization noise so as to move more of it outside the signal band, where it can be filtered out in the digital domain as shown in Figure 3-3(c). This is because the loop filter can suppress the quantization noise more effectively at low frequencies than high frequencies due to its high gain at low frequencies. It means if oversampling and quantization noise shaping are combined, more than \( \frac{1}{2} \) bit resolution increase per doubling of the OSR, can be obtained.
Figure 3-3 Signal and quantization noise spectrum for (a) Nyquist ADC, (b) ADC only with oversampling (c) ΣΔ ADC with oversampling and noise-shaping

In conclusion, by combining oversampling and noise shaping techniques, ΣΔ ADCs are able to achieve resolutions much higher than that of their own quantizers. That means for a given resolution, the requirement for precise analog components in the quantizer as well as in the feedback DAC can be relaxed. Therefore, ΣΔ ADCs are quite suitable to be implemented in sub-µm CMOS technology, which have faster circuitry but lack precisely matched analog elements (such as resistors and capacitors).
3.1.2 Thermal ΣΔ Modulator

As discussed in Chapter 2, in the proposed wind sensor, two orthogonal components (δP_{ew} and δP_{ns}) of the wind-induced heat loss δP, denoted here as the north-south and east-west components respectively, can be read out by thermal balancing loops. The north-south temperature balancing loop of the reference design [3], is re-drawn in Figure 3-4. The on-chip thermopile will transfer the air-flow induced north-south temperature gradient δT_{ns} into an electrical signal. By detecting the polarity of this signal with an auto-zeroed preamplifier and clocked quantizer, this loop can cancel the on-chip temperature difference δT_{ns}, by driving the opposing heaters in the chip with pulses of constant power P_{ref}. The average value of the temperature balancing loop’s output pulses is then a digital representation of the differential heater power δP_{ns} to compensate δT_{ns}. In a similar manner, δP_{ew} is determined by the east-west thermal balancing loop. Wind speed and direction can then be determined from δP_{ew} and δP_{ns}. As shown in Figure 3-4, the heater pairs serve as a single-bit thermal DAC, while the sensor’s thermal inertia serves as a thermal low-pass loop filter. Therefore this thermal balancing loop can be seen as a thermal sigma-delta (TΣΔ) modulator whose summing node and loop filter are realized in the thermal domain [3]. The block diagram of TΣΔ modulator is shown in Figure 3-5. The signal transition between the thermal and electrical domains can be made via the thermal “sensor” and “actuator”, i.e. the thermopile and the heater.

Figure 3-4 Block diagram of the temperature balancing loop [1]
The $\Sigma\Delta$ modulator can combine the benefits of feedback and analog-to-digital conversion with rather simple circuits. In addition to the elements of the sensor itself, i.e. heaters and thermopiles, only a clocked comparator is required. The sensor’s thermal mass can function as a low-pass filter in the thermal domain. The digital output of the modulator can be directly interfaced to a microprocessor for further signal processing. Like their electrical counterparts, the $\Sigma\Delta$ modulators can also employ oversampling and noise-shaping to accurately digitize the thermal input signal, $\delta P$. Because “wind” signals in the natural world are rather slow, the band of interest of the wind sensor can be limited to be between DC and 1Hz.

The major difference between $\Sigma\Delta$ modulators and their electrical counterparts is that the input signal, the summing node and the loop filter formed by the thermal mass, are all in the thermal domain (Figure 3-5). Thus, the behavior of the $\Sigma\Delta$ modulator will be mainly determined by the characteristic of its thermal loop filter. Because the thermal mass of the thermal wind sensor (silicon chip together with the ceramic disk) leaks heat to its surroundings, the thermal filter, unlike an ideal electrical integrator, has a finite DC gain. As a result, this thermal $\Sigma\Delta$ modulator loses its ability to achieve infinite precision with DC input signals. Besides, the low in-band gain of the thermal filter and low sensitivity of the thermopile can also lead to extremely small signals at the output of the thermopile. Thus, the noise performance of the $\Sigma\Delta$ modulator is then a primary concern. In the following section 3.1.3, the thermal filter will be modeled with thermal
resistors and capacitors such that it can be incorporated into a simulation environment to investigate the behavior of the TΣΔ modulator with simulation tools.

3.1.3 Modeling of Thermal Low-pass Filter

Using the analogy between the thermal and electrical domains (Table 3-1), the behavior of the thermal filter can be modeled by subdividing the wind sensor’s thermal mass into a large number of finite elements and then assigning a thermal resistance and capacitance to each element, as shown in Figure 3-6. The heat $P_{\text{heat}}$ dissipated in the heater, i.e. the thermal filter input, can be related to temperature difference $T_s$ measured by the thermopiles, i.e. thermal filter’s output, by modeling the thermal filter as a thermal impedance $Z_d$. For simplicity, the thermal model is illustrated in Figure 3-6 for a one-dimensional structure, and it can still be extended to two- even three-dimensional structures.

<table>
<thead>
<tr>
<th>Thermal Parameter</th>
<th>Unit</th>
<th>Electrical Parameter</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Temperature</td>
<td>K</td>
<td>Voltage</td>
<td>V</td>
</tr>
<tr>
<td>Heat flow</td>
<td>W</td>
<td>Current</td>
<td>A</td>
</tr>
<tr>
<td>Heat</td>
<td>$J=W\cdot s$</td>
<td>Charge</td>
<td>$C=A\cdot s$</td>
</tr>
<tr>
<td>Thermal Resistance</td>
<td>$K/W$</td>
<td>Resistance</td>
<td>$\Omega=V/A$</td>
</tr>
<tr>
<td>Thermal Capacitance</td>
<td>$J/K$</td>
<td>Capacitance</td>
<td>$F=C/V$</td>
</tr>
</tbody>
</table>

As shown in Figure 3-6, the heat pulse $P_{\text{heat}}$ generated by the heaters are the thermal filter’s input. It diffuses through the silicon substrate and the ceramic disk and
causes temperature fluctuations $T_s$, at the two ends of the relative temperature sensors (thermopiles in this design). The temperature fluctuations $T_s$, which are actually the thermal filter’s output, can then be converted into electrical signals by thermopiles. Because of the thermal inertia of the ceramic disk and the silicon substrate, the thermal filter, $Z_d$, exhibits a low-pass filtering characteristic.

The equivalent compact (RC) model as well as the corresponding parameters of the components can be derived by using 3-D finite element analysis. However, this process is computationally intensive and requires detailed knowledge of the thermal properties and dimensions of the silicon, ceramic disk and glue, which are not always available. Alternatively, the parameters of the thermal loop filter model can be derived experimentally, by measuring the thermal filter’s step response as follows. A heat step was applied to one of the heaters and the output of the thermopile was measured. From the step response, a compact model of the corresponding filter (Figure 3-7) was derived using a special-purpose software tool. The details of this modeling can be found in [3]. The advantage of this approach is that it can fully incorporate all aspects of the thermal behavior of both the wind sensor silicon chip and its package.

The thermal filter’s model as shown in Figure 3-7, consists of two Foster networks of (in total 20) RC stages that represent the transfer impedance between the heater and the two ends of the thermopile. Both networks are driven by identical current sources that represent the power $P_{\text{heat}}$ dissipated in the heater. The voltage drops across the networks correspond to the temperature difference at the two ends of the thermopile.
The electrical output of the thermopile is then proportional to the temperature difference \( \delta T \) between the two ends of the thermopile.

The frequency response of the thermal filter, as obtained from the compact model, is shown in Figure 3-8. Its low-pass filtering characteristic can clearly be seen. Since the thermal mass leaks heat to the surroundings, the thermal impedance, \( Z_d \) has a finite value at DC while it exhibits a first-order roll-off both for magnitude and phase at high frequencies [2]. Therefore, if the sampling frequency is above a few hundred hertz and only the thermal filter provides the noise-shaping, the TΣΔ modulator will behave as an electrical first-order ΣΔ modulator which is unconditionally stable. This compact model
can be incorporated into a MATLAB or Cadence environment for the modulator’s behavioral simulation.

As introduced in 0, the motivation for this work is to reduce the total power consumption of the thermal wind sensor, while still maintain similar sensing resolution compared to mechanical wind sensors. For a desired sensing resolution, the minimum heater power of the sensor should be only limited by the thermal noise of the thermopile, rather than the quantization noise of the TΣΔ modulator. In the following sections, a quasi-linear model of the TΣΔ modulator will be presented. Based on this model, the thermal and quantization noise of the TΔΣ modulator can be analyzed separately. Thus, the TΣΔ modulator can then be sought to be designed such that the in-band quantization noise adds a negligible resolution penalty. By doing this, for a given resolution, the required heating power consumption can be minimized.

### 3.2 Quasi-linear model of TΣΔ modulator

The highly nonlinear behavior of the single-bit quantizer makes direct analysis of the ΣΔ modulator difficult. The quasi-linear model [83,84] is a widely used approximation, which facilitates this analysis by replacing the nonlinear element with a variable, signal-dependent gain and additive noise, as shown in Figure 3-9. Although this model does not capture all aspects of the TΣΔ behavior, it enables the use of linear analysis and provides valuable insight about the stability and noise performance of the TΣΔ loop. The simulated output noise spectrum by applying this quasi-linear model and the real nonlinear model are compared in section 3.4.1.
In the quasi-linear model shown in Figure 3-9, the thermal filter is modeled by its s-domain transfer function \( H_{th}(s) \) which is derived by its lumped-RC model (Figure 3-7). \( H_{e}(s) \) is the transfer function of the electronic interface. The quantizer is modeled as a gain \( K \) and an additive quantization noise \( \frac{V_{qn}}{2} \). For a multi-bit quantizer, the gain \( K \) is naturally determined by the ratio of the quantizer’s output step size to the distance between its adjacent input thresholds. However, for a single-bit quantizer, \( K \) is not well-defined because a binary quantizer has only one threshold. The variable quantizer’s gain \( K \) should be inversely proportional to the superposition of the signal and the standard deviation of the noise at the quantizer input. The reason for this is that the output of the binary quantizer has a constant output amplitude [-1, +1]. Therefore, an increase of the quantizer’s input power leads to a proportional decrease in its gain \( K \) [83]. If the input of the quantizer is \( y \), the gain \( K \) can be derived in

\[
K = \frac{E[y]}{E[y^2]} \quad (3-1)
\]

As can be seen from (3-1), the effective gain \( K \) is derived in a statistical way. Actually it can be seen as an averaging of the gain of the quantizer.

The thermal DAC in the feedback path of the modulator consists of a pair of opposing heaters which are driven with pulses of constant power \( P_{ref} \). The input of the modulator is the differential heat loss \( \delta P \) induced by the air-flow. The three dominant
noise sources in the thermal ΣΔ modulator are input “wind noise” $P_{wd,n}^2$ induced by the random air currents from the sensor’s ambient environment, electrical noise $V_{en}^2$ at the input of the electrical interface, including the thermopile’s thermal noise and the input-referred noise of the readout circuit, and quantization noise $V_{qn}^2$. In the following analysis of this chapter, wind noise $P_{wd,n}^2$ will be neglected temporarily. However, its influence will be introduced in Error! Reference source not found..

By using the quasi-linear model shown in Figure 3-9, its output signal of the ΣΔ modulator, $V_o$, can be derived in (3-2) in s-domain

$$V_o(s) = STF(s) \cdot \delta P + NTF_{en}(s)V_{en}^2(s) + NTF_{qn}(s)V_{qn}^2(s)$$  \hspace{1cm} (3-2)

where $\delta P$ is the differential heat loss, i.e. the input signal of the modulator, $V_{en}^2(s)$ and $V_{qn}^2(s)$ are the s-transforms of the electrical noise and quantization noise of the modulator. The STF(s), NTF_{en}(s) and NTF_{qn}(s) are the s-domain transfer functions from the input signal, electrical noise and quantization noise, to the modulator’s output, respectively.

The signal transfer function in s-domain, i.e. STF(s), is derived in (3-3)

$$STF(s) = \frac{H_{th}(s)H_e(s)K}{1 + H_{th}(s)P_{ref}H_e(s)K} \approx \frac{1}{P_{ref}}$$  \hspace{1cm} (3-3)

If the term $H_{th}(s)P_{ref}H_e(s)K$ is much greater than one, the input signal transfer function is the inverse of the constant heating power $P_{ref}$. The differential heat loss $\delta P$, i.e. the input of the ΣΔ modulator, is proportional to the $P_{ref}$, as shown in (3-4)

$$\delta P = \alpha \cdot P_{ref}$$  \hspace{1cm} (3-4)

where $\alpha$ is the ratio between the differential heat loss $\delta P$ and the heating power $P_{ref}$. As shown in (2-6) and (2-7), the ratio $\alpha$, is actually a monotonic function of the wind speed.
It can be obtained by decimating modulator’s output bitstream. The wind speed and direction can then be calculated if $\alpha_{ns}$ and $\alpha_{ew}$ are obtained.

The signal component at the modulator’s output is

$$V_{o,\text{signal}}(s) = \frac{\delta P}{P_{\text{ref}}} = \frac{\alpha \cdot P_{\text{ref}}}{P_{\text{ref}}} \approx \alpha$$  \hspace{1cm} (3-5)

The s-domain transfer function from the electronic noise $\overline{V^2_{en}}(s)$ to the modulator output, i.e. $\text{NTF}_{en}(s)$, is shown in (3-6)

$$\text{NTF}_{en}(s) = \frac{H_e(s)K}{1 + H_{th}(s)P_{\text{ref}}H_e(s)K} \approx \frac{1}{H_{th}(s)P_{\text{ref}}H_e(s)K}$$  \hspace{1cm} (3-6)

The electronic noise can be considered to be shaped by the inverse of product of the thermal filter’s transfer function $H_{th}(s)$ and constant power $P_{\text{ref}}$. On one hand, because the thermal filter has low-pass characteristic, the electrical noise will be high-pass filtered. On the other hand, the in-band electrical noise is inversely proportional to the heating power $P_{\text{ref}}$. That means the in-band electrical noise can be suppressed by consuming more heating power $P_{\text{ref}}$.

The s-domain transfer function from quantization noise $\overline{V^2_{qn}}(s)$ to the modulator output, i.e. $\text{NTF}_{qn}(s)$, is shown in (3-7)

$$\text{NTF}_{qn}(s) = \frac{1}{1 + H_{th}(s)P_{\text{ref}}H_e(s)K} \approx \frac{1}{H_{th}(s)P_{\text{ref}}H_e(s)K}$$  \hspace{1cm} (3-7)

As illustrated in (3-7), the in-band quantization noise is also inversely proportional to the heating power $P_{\text{ref}}$. The target for this $\Sigma\Delta$ modulator design is to attenuate its in-band quantization noise to be below the electronic noise floor, such that the resolution is fundamentally limited by the thermal noise of the thermopile rather than quantization noise. By comparing $\text{NTF}_{en}(s)$ and $\text{NTF}_{qn}(s)$, it can be seen that the quantization noise can be shaped by the electrical filter or be attenuated by quantizer’s effective gain $K$. Thus, there are mainly two methods to further suppress the quantization noise. Firstly, by
increasing the in-band gain of the electronic interface’s transfer function \( H_e(s) \), the low-pass loop filter can provide more noise-shaping of the quantization noise. This can be realized by augmenting the thermal filter with extra electronic integrators, i.e. increasing the order of the loop filter. Secondly, increasing the equivalent quantizer gain \( K \) would also allow the quantization noise to be further attenuated relative to the electronic noise floor. However, this quantizer gain \( K \) is inversely proportional to its input amplitude. Thus, the designer does not have direct control over this parameter. In the next section, methods of increasing \( K \) will be introduced.

The s-domain output of the \( \Sigma \Delta \) modulator, \( V_o(s) \), is shown in (3-8)

\[
V_o(s) = \alpha + \frac{V_{en}^2(s)}{H_{th}(s)P_{ref}} + \frac{V_{qn}^2(s)}{H_{th}(s)P_{ref}H_e(s)K}
\]  

(3-8)

If the \( \Sigma \Delta \) modulator only uses the thermal filter as its loop filter, in the following sections, it will be called as “first-order” \( \Sigma \Delta \) modulator because the thermal filter’s frequency response is quite similar to that of first-order electrical filter (Figure 3-8). In the following section, the output-referred electrical and quantization noise in first-order \( \Sigma \Delta \) modulator will be separately analyzed and then compared by using the formulas which are derived with the quasi-linear model. Methods of further suppressing the in-band quantization noise relative to the electronic noise of the \( \Sigma \Delta \) modulator will then be discussed in details.

3.3 First-order \( \Sigma \Delta \) modulator

3.3.1 Model of first-order \( \Sigma \Delta \) modulator

Derivation of the effective gain \( K \) of the comparator

The behavioral model of a first-order \( \Sigma \Delta \) modulator, which can be incorporated into a Matlab/Simulink simulation environment, is shown in Figure 3-10.
The s-domain transfer function $H_{th}(s)$ of the thermal filter, as shown in Figure 3-10, can be derived from the compact model of the thermal filter $Z_d$ (Figure 3-7). The pre-amp gain of the comparator is modeled with “$C_{gain}$” which is equal to 60dB. The modulator’s input is a DC input differential heat loss $\delta P$ to cancel the temperature gradient induced by air-flow and its dynamic range is $[-Pre, Pre]$. The temperature difference $\delta T$, which is the output of the thermal filter, is converted into the electrical domain by a thermopile which consists of 12 series-connected thermocouples. The sensitivity of the thermopiles, $K_{th,E}$, is set to be approximately 12mV/K, which is already derived experimentally in the reference design [3]. To simulate the effect of the thermal noise of the thermopile’s resistance, white noise was added to the input of the comparator. The thermal noise $V_{en}$ is set to be 64µV (rms), a value which corresponds to thermopile’s thermal noise and its noise bandwidth [3]. In addition, $P_{ref}$ is set to be 25mW which is the target heating power consumption for one $T\Sigma\Delta$ modulator. The quantizer’s clocking frequency $f_s$ is set to be 8192Hz to achieve sufficiently high OSR. The parameters in the quasi-linear model of the first-order $T\Sigma\Delta$ modulator are summarized in Table 3-2. These parameters will also be applied to the rest of the simulations in this thesis unless indicated otherwise.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
<th>Note</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{en}$</td>
<td>64µV (rms)</td>
<td>The thermal noise of the thermopile</td>
</tr>
<tr>
<td>$K_{th,E}$</td>
<td>12mV/K</td>
<td>The sensitivity of the thermopiles</td>
</tr>
<tr>
<td>$C_{gain}$</td>
<td>60dB</td>
<td>Pre-amp gain of the comparator</td>
</tr>
<tr>
<td>$P_{ref}$</td>
<td>25mW</td>
<td>Heating power of one $T\Sigma\Delta$ modulator</td>
</tr>
<tr>
<td>$f_s$</td>
<td>8192Hz</td>
<td>Clock frequency of the quantizer</td>
</tr>
<tr>
<td>Band of interest</td>
<td>[0,1Hz]</td>
<td></td>
</tr>
</tbody>
</table>
The quantization noise is regarded as a white noise with the power spectral density shown in (3-9)

\[
V_{qn}(f)^2 = \frac{\Delta^2}{12} \cdot \frac{1}{f_s}
\]  (3-9)

where \(\Delta\) is the quantization step of the 1-bit comparator (\(\Delta=2\) in this simulation) and \(f_s\) is the clock frequency of the quantizer.

With extensive time-domain simulations in Simulink, the effective gain \(K\) of the quantizer in the quasi-linear model can be obtained by applying the formula shown in (3-10). The details of rigorous derivation for this formula are presented in [6].

\[
K = \frac{V_{in}}{V_{in}^2}
\]  (3-10)

where \(V_{in}\) is the quantizer's input as shown in Figure 3-10.

**Output noise spectrum derived by quasi-linear model**

The electrical noise spectrum density, \(V_{en}^2(s)\), can be calculated by using the number indicated in Table 3-2. The quantization noise \(V_{qn}^2(s)\), can be obtained with formula (3-9). The equivalent gain of the 1-bit quantizer, \(K\), is obtained with formula (3-10) and extensive time-domain simulations of the behavioral model shown in Figure 3-10. The transfer functions, i.e. \(NTF_{en}(s)\) and \(NTF_{qn}(s)\), are illustrated in (3-6) and (3-7) respectively. Thus, the power spectrum of the output-referred electronic and quantization noise of the first-order \(T\Sigma\Delta\) modulator can be plotted separately in Figure 3-11 by applying equation(3-8). It can be seen that both the quantization and electronic noise are shaped by the thermal loop filter up to about 100Hz, where a peak occurs. This peak corresponds to the frequency where the thermal filter's phase delay goes through -180°. As illustrated in Figure 3-11, the quantization noise floor in the band of interest near DC is obviously higher than that of the thermal noise. It can be concluded that the resolution of first-order \(T\Sigma\Delta\) modulator is mainly limited by the quantization noise rather than by thermal noise. That means if the quantization noise can be further suppressed, the
resolution of the modulator can be increased. In other words, for a given resolution, the heating power consumption $P_{\text{ref}}$ can be further reduced if the quantization noise is reduced. In the next section, the methods to suppress the in-band quantization noise will be investigated in details.

![Figure 3-11: Output electrical and thermal noise power spectrum density in first-order $\Sigma\Delta$ modulator](image)

Figure 3-11 also compares the output noise spectrum (with thermal noise and quantization noise combined) of the first-order $\Sigma\Delta$ modulator obtained from quasi-linear analysis with that obtained from numerical simulations of the behavior model with the nonlinear quantizer as shown in Figure 3-10. It can be seen that the output noise spectrum predicted from the quasi-linear model is consistent with that derived from real behavioral model. Thus, the conclusion can be drawn that the noise performance of $\Sigma\Delta$ modulator can be estimated reliably by applying the quasi-linear model.

### 3.3.2 Quantization Noise Suppression

In electronic $\Sigma\Delta$ modulators, in-band quantization noise can be reduced by increasing either the OSR or the order of the loop low-pass filter. Below we will evaluate the validity of both approaches in the context of electrical and $\Sigma\Delta$ modulators.

*Electrical $\Sigma\Delta$ modulator*
For a typical electrical first-order ΣΔ modulator which quasi-linear model is shown in Figure 3-12, by increasing the sampling frequency of the quantizer, the in-band quantization noise can be reduced mainly by two methods. Firstly, the quantization noise power can be reduced by 3dB for every doubling of the sampling frequency due to noise spreading effect. Secondly, as indicated in (3-10), the quantizer’s effective gain is inversely proportional to its input. As the sampling frequency increases, the output response of the loop filter to the feedback pulses should decrease due to the reduced time interval over which each pulse is applied to the loop filter. For a typical first-order electrical loop filter, if the sampling time is reduced by half, the filter’s output response decreases by a factor of 2 for constant pulse amplitude. This is equivalent to a reduction of 6dB/oct of the filter’s output amplitude, resulting in a corresponding increase of 6dB/oct in the quantizer’s gain. The input and effective gain $K$ of the quantizer in first-order electrical ΣΔ modulator are illustrated by simulation in Figure 3-13 (a) and (b) respectively, as the sampling frequency increases. The net result is that the in-band quantization noise at the output decreases by 9 dB for every doubling of the sampling frequency as shown in Figure 3-14 (6 dB due to the increase of the quantizer gain and 3 dB due to the noise spreading effect).

![Figure 3-12 Quasi-linear model of first-order electrical ΣΔ modulator](image-url)
Figure 3-13 First-order electrical ΣΔ modulator's quantizer
(a) input amplitude (b) effective gain versus sampling frequency, $f_n=8192$Hz
Figure 3-14 In-band noise density versus sampling frequency $f_s$ for first-order $T\Sigma\Delta$ modulator ($f_n=8192\text{Hz}$, band of interest=DC to 1Hz)

**First-Order Thermal $\Sigma\Delta$ Modulator**

As shown in Figure 3-15(a), with or without presence of the thermopile’s electronic noise, the input of the quantizer of a first-order $T\Sigma\Delta$ modulator will “saturate” as the sampling frequency increases. This is quite different from the behavior of the first-order electrical $\Sigma\Delta$ modulator as illustrated above. As a result, the equivalent gain $K$ of the quantizer will also converge to a certain value as the sampling frequency increases, as shown in Figure 3-15(b). Thus, the in-band noise density at the modulator’s output (Figure 3-16) decreases by only about 3 dB for every doubling of the sampling frequency only due to the noise spreading effect when the sampling frequency is larger than $f_n$ ($f_n=8192\text{Hz}$). This behavior may be explained as follows.

As shown in the modulator’s output spectrum simulated by the behavioral model (Figure 3-11), both the quantization and electronic noise is shaped by the thermal loop filter up to about 100Hz until a peak occurs. The quantizer’s input will thus be dominated by a sine-wave at this peak frequency, $f_{\text{peak}}$, as shown in Figure 3-17 (simulated without electronic noise). If the sampling frequency is much faster than the sine wave’s peak frequency, the quantizer behaves in asynchronous way. As a result, increasing the sampling frequency larger than this peak frequency ($f_{\text{peak}}\approx 100\text{Hz}$) will not have much impact on the waveforms present in the first-order $T\Sigma\Delta$ modulator. In other words, compared to the sampling frequency, the thermal filter is “too slow” and so the modulator behaves like an asynchronous $\Sigma\Delta$ modulator. It can be concluded that increasing the
sampling frequency beyond certain threshold frequency will only reduce in-band quantization noise due to the noise-spreading effect, i.e. at the rate of 3dB/oct (Figure 3-16). However, the sampling frequency will usually be limited by practical considerations, such as the quantizer’s speed, etc. This, in turn, limits the attainable resolution of the first-order ΣΔ modulator.

Figure 3-15 First-order ΣΔ modulator’s quantizer’s
(a) input amplitude (b) effective gain K versus sampling frequency, \( f_n = 8192 \text{Hz} \)
Impact of the thermal noise in TΣΔ modulator

In an electrical ΣΔ modulator, electronic noise contribution from the later stages of the loop-filter is negligible due to the high in-band gain of the first electrical integrator. However, for a first-order TΣΔ modulator, as shown in Figure 3-8, the thermal filter’s in-band gain is limited such that the thermopile’s thermal noise can have a significant impact on the behavior of the modulator. Figure 3-16 compares the output referred in-band noise density with and without the presence of electronic noise. The in-band noise is increased by about 6dB due to the presence of electronic noise. There are two
ways for the electronic noise to contribute to the modulator’s output. Firstly, due to the relatively low in-band gain of the thermal filter, as indicated in formula (3-6), the electronic noise can directly contribute to the in-band noise. However, as illustrated in Figure 3-11, the in-band noise is still mainly dominated by the quantization noise. Thus, this “direct” contribution is not the most significant. Secondly, the input of the quantizer will increase in the presence of electronic noise as shown in Figure 3-15(a). Therefore, the equivalent gain $K$ of the quantizer is reduced accordingly as shown in (3-10) and the output-referred quantization noise will be higher. The conclusion is then that the presence of electronic noise can cause the in-band quantization noise to be increased compared with the level without electronic noise and this effect is called by “boosting effect” of the electronic noise in $T\Sigma\Delta$ modulator.

It can be concluded that by increasing the clocking frequency, i.e. OSR of the comparator in $T\Sigma\Delta$ modulator, the in-band quantization noise can not be suppressed as effectively as its electrical counterpart. Therefore, further suppression of the in-band quantization noise of $T\Sigma\Delta$ modulator requires more aggressive noise-shaping, by augmenting the $T\Sigma\Delta$ modulator’s thermal filter with an electrical integrator. Because of the gain provided by the electrical integrator, the thermopile’s thermal noise is expected to have less “boosting effect” on quantization noise. In conclusion, the integrator provides additional noise-shaping and in-band gain such that the resulting “second” order modulator is expected to have significantly more resolution than the first-order $T\Sigma\Delta$ modulator. This will be discussed in the next section.

### 3.4 Second-order thermal $\Sigma\Delta$ modulator

#### 3.4.1 Noise Analysis

The analysis in the previous section suggests that in-band quantization noise of the $T\Sigma\Delta$ modulator can be further suppressed by augmenting the thermal filter with an electrical integrator, which provides extra in-band gain without amplifying the out-of-band noise. The behavioral model of second-order $T\Sigma\Delta$ modulator which can be simulated in a Matlab/Simulink environment, is shown in Figure 3-18.
Figure 3-18 Behavioral model of the second-order $\Sigma\Delta$ modulator in Simulink

To illustrate the effect of additional electrical filter on the noise-shaping, Figure 3-19 compares the simulated output noise of a second-order $\Sigma\Delta$ modulator to that of the first-order modulator by using the equation (3-8), with the parameters shown in Table 3-2. As illustrated in Figure 3-19, the additional noise shaping provided by the added electronic filter further suppresses the quantization noise of second-order $\Sigma\Delta$ modulator significantly to be below the electronic noise floor. The resolution of second-order modulator is now fundamentally limited by the thermopile's thermal noise, rather than quantization noise. Thus, for a given resolution, by adding an electrical integrator in the loop filter, the heating power $P_{ref}$ in $\Sigma\Delta$ modulator can be minimized.

**Peak tone in output spectrum**

As illustrated in Figure 3-19, it can be noticed that, a peak tone occurs at about 20 Hz in the output quantization noise spectrum of the second-order $\Sigma\Delta$ modulator. The loop filter in second-order $\Sigma\Delta$ modulator consists of the thermal filter and an electrical integrator in cascade. This peak tone corresponds to the frequency ($f_{peak}$) where the phase delay of the loop filter goes through -180°. Since the integrator always has a 90° phase shift, this peak tone is actually located at the frequency where the thermal filter's phase delay is 90°.
In time domain, the quantizer’s input of a second-order $\Sigma\Delta$ modulator is dominated by a sine wave at the peak tone frequency $f_{\text{peak}}$ (Figure 3-20). Because the quantizer's clock frequency $f_s$ is much larger than $f_{\text{peak}}$, it (nearly) operates in asynchronous way. Therefore, further increasing the clock frequency $f_s$, which is much larger than this peak frequency $f_{\text{peak}}$ ($f_{\text{peak}} \approx 20\text{Hz}$) has little impact on the behavior of comparator, thus the second-order $\Sigma\Delta$ modulator. The quantizer's input amplitude and thus its equivalent
gain will both saturate as the comparator’s clock frequency increases as shown in Figure 3-21. Similar to the first-order $\Sigma\Delta$ modulator, increasing the clock frequency $f_s$ will only reduce in-band quantization noise due to the noise-spreading effect, i.e. at the rate of 3dB/oct as shown in Figure 3-22.

Figure 3-21 Second-order $\Sigma\Delta$ modulator’s quantizer
(a) input and (b) effective gain versus sampling frequency, $f_n=8192$Hz
Impact of the electronic noise

As already explained in section 3.3.2, due to the low DC gain of the thermal filter, the presence of electronic noise can “boost” the in-band quantization noise of a first-order TΣΔ modulator. Compared to first-order TΣΔ modulator, due to the gain provided by the electrical filter, the boosting effect of the electronic noise can be reduced. As shown in Figure 3-21, with or without the presence of the electronic noise, the input and effective gain of the quantizer versus the sampling frequency $f_s$ in second-order TΣΔ modulator, are almost the same. Thus, as shown in Figure 3-22, with electronic noise, the total in-band noise will be higher, because the in-band noise of second-order TΣΔ modulator is dominated by the electronic noise.

Nonlinear Model vs Quasi-linear model

The output noise spectrum of the first-order and second-order TΣΔ modulator’s were obtained from simulations of the quasi-linear model (Figure 3-19) and the actual nonlinear system (Figure 3-23), respectively. It can be noticed that second-order TΣΔ modulator’s output spectrum in Figure 3-23 exhibits strong peak tones not only at a fundamental frequency (about 20Hz) and but also its harmonics. The peak tone can be well predicted by the quasi-linear model (Figure 3-19), in which the quantizer is linearly modeled. However, in fact, the behavior of the binary quantizer is not linear. The
approximate relationship between the quantizer’s input \( V_{q,in} \) and output \( V_{q,out} \) is illustrated in (3-11)

\[
V_{q,out} = k_1 V_{q,in} + k_2 V_{q,in}^2 + \cdots + k_n V_{q,in}^n
\]  

(3-11)

The details about the nonlinear modeling of the binary quantizer in \( \Sigma\Delta \) modulator can be found in [83]. Because the quantizer is actually non-linear, harmonics of the peak tone will also appear in the output spectrum (Figure 3-23). The peak tone and its harmonics can be filtered out by the decimation filter, which will be discussed in section 3.4.6.

Figure 3-23 The output noise spectrum of the first-order and second-order \( T\Sigma\Delta \) modulator, which is obtained from numerical simulation of the actual nonlinear system

3.4.2 \( T\Sigma\Delta \) Modulator’s Nonlinearity

Because the leakage of its thermal filter may give rise to some non-linearity, in this section the DC transfer function of the \( T\Sigma\Delta \) modulator will be examined. The quantization error \( \mu - \delta P/\text{P}_{\text{ref}} \) of both the first-order and second-order \( T\Sigma\Delta \) modulator is plotted in Figure 3-24 and Figure 3-25, respectively with the simulation of the behavioral model (Figure 3-12 and Figure 3-18). The simulation parameters in Table 3-2 were applied. The bit-stream is decimated by 8192-tap sinc4 filter and the simulation is done in the absence of the electronic noise. As shown in Figure 3-24 (a), the DC transfer characteristic of the first-order modulator is only linear around \( \delta P=0 \), while it exhibits a gain error elsewhere.
due to the leakage of the thermal filter. This gain error can be corrected by applying a constant gain factor $\alpha$. After the gain correction, the first-order $\Sigma\Delta$ modulator can then achieve 9-bit resolution over roughly half of the total input range as shown in Figure 3-24 (b). In contrast, as shown in Figure 3-25, the second-order $T\Sigma\Delta$ modulator can achieve 14-bit resolution over the whole input range without gain correction and the DC transfer function only exhibits a very small gain error. The linearity improvement is mainly due to the extra DC gain provided by the added electrical filter in the second-order $T\Sigma\Delta$ modulator.

![Graph](image)

(a)

![Graph](image)

(b)

Figure 3-24 DC transfer curve’s non-linearity of the first-order $T\Sigma\Delta$ modulator
(a) no gain correction (b) after gain correction (simulation without the electronic noise)
As illustrated in Figure 3-26 and Figure 3-27, the nonlinearity of the first-order and second-order TΣΔ modulator can also be examined with the presence of the electronic noise. For the first-order TΣΔ modulator, the added noise at the comparator’s input acts as a dither signal that improves the linearity of the DC transfer curve, as shown in Figure 3-26 (a). After gain correction, 9-bit resolution can be achieved over about 80% of the input range. By contrast, the second-order TΣΔ modulator can still achieve 14-bit resolution over the 80% of the input range without gain correction even with the presence of electronic noise. In conclusion, by augmenting the thermal filter with an electrical integrator, the DC gain of the TΣΔ loop filter is boosted. Thus, the linearity of a TΣΔ modulator can be improved, accordingly.
Figure 3- 26 DC transfer curve's non-linearity of the first-order $\Sigma\Delta$ modulator
(a) no gain correction (b) after gain correction (simulation with the electronic noise)
3.4.3 Thermal filter’s output swing

The output temperature swings of the thermal filter, $\delta T$ (i.e. temperature gradient), should be kept small to make sure $\Sigma \Delta$ modulator can operate the sensor in temperature balancing (TB) mode. The output swing $\delta T$ of the thermal filter versus the input of the modulator $\delta P/P_{ref}$, in the first-order and second-order $\Sigma \Delta$ modulators are shown in Figure 3-28 (a) and (b), respectively. In the first-order modulator, $\delta T$ is only about 6mK, while for the second-order modulator, the thermal filter output swing is about 40mK. For both the first-order and second-order systems, the small output swings of the thermal filter prove that the $\Sigma \Delta$ modulator will indeed operate the sensor in temperature balancing (TB) mode. The larger output swing of the thermal filter in the second-order system is due to its stronger oscillation at the peak frequency, as shown in Figure 3-23.
3.4.4 Stability analysis

As shown in Figure 3-23, in the output spectrum of the second-order thermal $\Sigma\Delta$ modulator, there is a big peak tone at the frequency at which the loop filter’s phase delay goes through $-180^\circ$. It seems that this closed-loop system is prone to be “unstable”. Therefore, it is necessary to carefully check the stability of the second-order $\Sigma\Delta$ modulator.
The stability for ΣΔ modulator is rigorously defined [85] as follows:

An n-th order ΣΔ modulator is stable if and only if all of its integrator’s outputs are bounded inside a certain interval, i.e. the maximum allowed output swing.

![Graph of thermopile output swing](image)

![Graph of electrical filter output swing](image)

Figure 3-29 Output swing of (a) the thermopile and (b) electrical filter
The output swings of the thermal and electrical filter in second-order thermal \( \Sigma \Delta \) modulator with different heating power, \( P_{\text{ref}} \), have been investigated as shown in Figure 3-29 (a) and (b). It can be seen that, over the modulator’s full input range, the normalized outputs of both the thermopile and electrical integrator are still within the allowable range. Thus, the second-order \( T \Sigma \Delta \) loop is stable by definition.

In general, instability appears at the modulator output as a large-amplitude low-frequency oscillation, leading to long strings of alternating 1’s and -1’s. As a result, the decimated output of the modulator is not related to the input any more. However, as shown in the DC transfer function of the second-order thermal \( \Sigma \Delta \) modulator (Figure 3-25 and Figure 3-27), the system can still convert the input into a digital reading with 14-bit resolution for the whole input dynamic range.

In conclusion, the operation of the second-order \( T \Sigma \Delta \) modulator is stable. It behaves more like duty-cycle modulator than a traditional \( \Sigma \Delta \) modulator, and its output consists of a square-wave whose duty-cycle is proportional to the input differential heat power \( \delta P \) required to cancel the differential \( \delta T \) induced by the air-flow, as shown in Figure 3-30. The result is a strong peak tone in the modulator’s output spectrum, whose frequency \( \sim 20\text{Hz} \) corresponds to the frequency at which its loop filter has a phase shift of 180°.

![Figure 3-30 Output bit-stream of the second-order thermal \( \Sigma \Delta \) modulator](image)

In the second-order thermal \( \Sigma \Delta \) modulator, height of the peak tone in the output spectrum (Figure 3-23) can be reduced by applying phase compensation to the loop, e.g. by adding a feedback or feed-forward path as illustrated in Figure 3-31. However, there are several reasons not to implement the phase compensation path.
Firstly, there is a tradeoff between phase compensation and in-band quantization noise suppression. By adding the phase compensation path, the phase margin of the $\Sigma\Delta$ loop is indeed increased (Figure 3-32a) and height of the peak tone in the output spectrum is reduced as expected (Figure 3-32b). However, NTF of $\Sigma\Delta$ loop with phase compensation path will be less aggressive compared to that of the pure second-order loop. Thus, the height of the peak tone in the output spectrum is actually reduced at the cost of increased in-band quantization noise. Since the second-order $\Sigma\Delta$ loop is proven to be inherently stable as indicated in previous section, there is no obvious motivation of implementation of the phase compensation path.

Secondly, the peak tone in the spectrum is located at the frequency $f_{\text{peak}}$, where the thermal filter’s phase delay is $90^\circ$. As indicated in the next section, thermal filter’s phase delay is a monotonic function of chip temperature, which means that $f_{\text{peak}}$ will also be a function of temperature. Therefore, the chip temperature can be determined by measuring the peak tone frequency $f_{\text{peak}}$. However, this new feature will be lost if phase compensation is applied.

In summary, the feed-forward/feedback phase compensation path will not be implemented in second-order $\Sigma\Delta$ loop to reduce the height of the peak tone.
3.4.5 Temperature sensing with second-order ΣΔ loop

Figure 3-33 shows a more detailed cross section of the thermal filter used in the thermal ΣΔ modulator. It can be seen that the heat pulses generated during the modulator’s operation will diffuse through the silicon substrate and cause differential temperature fluctuations $\delta T_{NS}$. The thermal phase shift experienced by these heat pulses will then be determined by the thermal diffusivity of silicon, which has been proven to be
a well-defined function of temperature [86,87]. Therefore, the associated phase shift of the thermal loop filter, $\Phi_{TF}$, will also be temperature-dependent.

As already explained in previous sections, there is a strong peak tone in the second-order $T\Sigma\Delta$ modulator's output spectrum, whose frequency, $f_{peak}$ corresponds to the same frequency where phase shift of the thermal filter, $\Phi_{TF}=180^\circ$. Since the electrical integrator's phase shift is designed to be almost exactly $90^\circ$, $f_{peak}$ will be determined by the thermal filter's phase-shift and hence by the temperature of the silicon substrate [86]. In turn, the chip's temperature can be determined by measuring peak tone frequency $f_{peak}$. In this work, by applying the CP working mode and the second-order thermal $\Sigma\Delta$ modulator, the required total heater's power consumption can be reduced to 25mW for which the sensor's self-heating is estimated to be less than 1°C. As such, the temperature of the sensor is close approximation of ambient temperature.

In next section, the self-tracking digital decimation filter which is suitable for the second-order $T\Sigma\Delta$ modulator, will be presented. The method to measure the peak frequency $f_{peak}$ will also be introduced.

![Figure 3-33 The detailed cross section of the thermal filter](image)

### 3.4.6 Self-tracking Sinc$^2$ decimation filter

In order to provide the flexibility, the digital processing of the $T\Sigma\Delta$ modulator's output and the computation of wind speed and direction will be done in an external micro-controller. A sinc$^2$ filter can be easily implemented in most micro-controllers. However, as indicated in previous section, the peak tone frequency, $f_{peak}$, will vary with temperature. Therefore, a fixed-length sinc$^2$ filter is not suitable for this application. A sinc$^4$ filter can provide enough attenuation but it is too complex to be easily realized in a low-cost micro-controller.
The need for a complex digital decimation filter can be avoided by using a simple self-tracking sinc\(^2\) filter for the decimation of the TΣΔ modulator’s bit-stream. As shown in Figure 3-34, the output bit-stream is a periodic duty-cycle signal whose period \(T_{peak}\), is the inverse of the peak tone frequency of the modulator, i.e. \(=1/f_{peak}\). \(T_{peak}\), which is equal to the duration time between two rising edges of the bit-stream, can then be precisely measured using a reference clock signal. The triangular window length of the sinc\(^2\) filter is dynamically adjusted by the measured \(T_{peak}\). Thus, the resulting decimation filter always has notches exactly at the peak tone frequency \(f_{peak}\) and its harmonics. The modulator’s output bit-stream during each period \(T_{peak}\), which consists of a few hundred digital bits, is then decimated using the adjusted window. The final decimated output is the average of \(n\) such decimated values (\(n=20\) in this work). The peak tone frequency \(f_{peak}\) can also be obtained by averaging \(n\) such periods (\(n=20\) in this work) to measure the ambient temperature, as indicated in previous section. Filtering the bit-stream with this proposed self-tracking sinc\(^2\) filter results in an estimated SNR of 80dB relative to \(P_{ref}\) (in the presence of the electronic noise). By contrast, the SNR obtained with an ideal brick-wall filter with the same noise bandwidth (from DC to 1Hz) is 82dB, which is only 2dB higher. Thus, it can be concluded that the self-tracking sinc\(^2\) filter can sufficiently suppress the out-of-band quantization noise and peak tones with varying ambient temperature.

![Figure 3-34 Operation of the self-tracking sinc\(^2\) decimation filter.](image-url)
The performance comparison of the first-order and second-order $\Sigma\Delta$ modulators is compared in Table 3-3.

### Table 3-3 Comparison between first-order and second-order modulator

<table>
<thead>
<tr>
<th>Parameter</th>
<th>First-order $\Sigma\Delta$ modulator</th>
<th>Second-order $\Sigma$ modulator</th>
</tr>
</thead>
<tbody>
<tr>
<td>Reference design</td>
<td>[3]</td>
<td>[This work]</td>
</tr>
<tr>
<td>Sampling frequency ($f_s$)</td>
<td>8192 Hz</td>
<td></td>
</tr>
<tr>
<td>$P_{\text{ref}}$</td>
<td>25mW (total power=50mW for two orthogonal $\Sigma\Delta$ modulators)</td>
<td></td>
</tr>
<tr>
<td>Band of interest</td>
<td>[0, 1Hz]</td>
<td></td>
</tr>
<tr>
<td>In-band noise</td>
<td>Quantization noise dominated</td>
<td>Electronic noise dominated</td>
</tr>
<tr>
<td>In-band SNR</td>
<td>67dB</td>
<td>80 dB</td>
</tr>
<tr>
<td>(with electronic noise)</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Nonlinearity</td>
<td>9-bit (80% input range)</td>
<td>14-bit (80% input range)</td>
</tr>
<tr>
<td>(with electronic noise)</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Thermal filter's output swing</td>
<td>±0.006K</td>
<td>±0.04K</td>
</tr>
</tbody>
</table>

### 3.5 Summary

As the interface of a thermal wind sensor, a $\Sigma\Delta$ modulator combines the benefits of thermal feedback and analog-to-digital conversion while only requiring rather simple circuitry. The $\Sigma\Delta$ modulator should be designed such that its resolution is only limited by the thermopile’s thermal noise rather than by quantization noise. By doing this, for a given resolution, the heating power of the thermal wind sensor can then be minimized.

In order to minimize the in-band noise of $\Sigma\Delta$ modulator, the thermal and quantization noise will be separately analyzed. To do this, a quasi-linear model of the $\Sigma\Delta$ modulator was developed. For the first-order $\Sigma\Delta$ modulator, simulations show that its in-band resolution is limited by quantization noise, because the noise shaping only provided by its thermal loop filter is insufficient. There are mainly two methods to further reduce the in-band quantization noise: by increasing the sampling frequency or the order of loop filter. The simulation shows that increasing the sampling frequency only reduces quantization noise only by 3dB/oct. Moreover, the sampling frequency will usually be limited by many factors, such as the quantizer’s speed, etc. Thus, it is more practical to
further suppress the in-band quantization noise by augmenting the thermal filter with an electrical integrator. The resulting second-order $\Sigma\Delta$ modulator has more aggressive noise shaping than the first-order $\Sigma\Delta$ modulator. The simulation shows that the in-band noise is indeed limited by the thermopile’s thermal noise and the in-band resolution is increased. Due to the high in-band gain of the extra electrical integrator, the linearity of the DC transfer function is also greatly improved. The second-order $\Sigma\Delta$ modulator achieves 14-bit linearity over 80% of the input range while the first-order system achieves only 9-bit over the same range.

In the output spectrum of the second-order $\Sigma\Delta$ modulator, there is a big peak tone at the frequency at which the loop filter’s phase delay goes through -180°. It seems that this closed-loop system is prone to be “unstable”. However, the fact that both the thermal and electrical integrator outputs are bounded within the allowable range, and the system can still convert the input into a digital reading with 14-bit resolution for the 90% of input dynamic range, proves that the system is stable.

Interestingly, ambient temperature can be determined by measuring the peak tone frequency, because the phase shift of the thermal filter is a monotonic function of the temperature. The need for a complex digital decimation filter is avoided by using a simple self-tracking sinc$^2$ filter, whose notches can track the peak tone frequency and its harmonics. Filtering the bit-stream with this self-tracking sinc$^2$ filter results in an estimated SNR of 78dB relative to the $P_{\text{ref}}$, which is only 2dB lower than that of the brick-wall filter.
Chapter 4
Low-offset Interface Circuit Techniques

As indicated in previous chapter, due to the low gain of the thermal filter as well as low sensitivity of the thermopile, the output amplitude of the thermopile could be quite small (at µV level). Thus, the input-referred in-band noise and DC offset of the thermopile’s interface amplifier can become the major source of the error in the conversion of TΣΔ modulator. Dynamic offset cancellation techniques, such as auto-zeroing or chopping, are often applied to reduce the offset and 1/f noise of the CMOS amplifier.

This chapter will firstly analyze and model the input-referred offset and noise of CMOS amplifiers. The operating principles of the auto-zeroing and chopping amplifiers will be briefly introduced and compared in the context of thermopile’s interface amplifier design for the TΣΔ modulator.

4.1 Offset and noise of CMOS amplifiers

The input-referred noise spectrum of a typical CMOS amplifier is shown in Figure 4-1, which includes offset, drift, 1/f noise and thermal noise. In high frequency domain, the input-referred noise is mainly dominated by the white thermal noise. At lower frequencies, by contrast, the noise is dominated by the flicker noise, which is also called by 1/f noise since this noise decrease linearly with the frequency. The point where the thermal noise becomes dominant over the flicker noise is called the 1/f noise corner frequency or $f_{\text{knee}}$ [21]. The input-referred offset can drift due to aging and variations of the temperature. This implies that it has a certain bandwidth and can therefore be considered to be a form of ultra-low-frequency 1/f noise. As shown in Figure 4-1, the band of interest of the TΣΔ modulator is set to be [0,1Hz]. In the following text, the terms of “in-band” or “baseband” both refer to the band of interest.
As introduced in previous chapter, by augmenting the thermal filter with an electrical integrator, the resolution of the resulting second-order \( T\Sigma\Delta \) modulator should be fundamentally limited by the thermal noise of the thermopiles, i.e. \( V_{n,\text{tp}} \) as shown in Figure 4-2. In practice, however, the input-referred offset \( V_{\text{os}} \) and noise \( V_{n,\text{ic}} \) of the thermopile’s interface amplifier, can also introduce errors in the \( T\Sigma\Delta \) conversion. Dynamic offset cancellation techniques are always applied to the interface amplifier to reduce those errors. The fundamentals of these techniques (auto-zeroing and chopping) will be introduced in next section.

![Figure 4-1 Noise spectrum of the standard CMOS amplifier](image)

![Figure 4-2 Noise and offset at the input of the thermopile interface amplifier in second-order T\( T\Sigma\Delta \) modulator](image)
4.2 Dynamic offset cancellation techniques

There are mainly two kinds of dynamic offset cancellation techniques which are widely used: auto-zeroing and chopping [88]. The fundamental difference between them is the handling of the offset. In auto-zeroing amplifier, the offset is firstly measured in one phase and then subtracted in the other phase. By contrast, in chopping amplifier, the offset is firstly modulated away from DC to higher frequency then filtered out. By using the dynamic offset cancellation techniques, the offset can be compensated continuously. Moreover, these techniques can also help to reduce the 1/f noise.

4.2.1 Auto-zeroing techniques

An example of the auto-zeroing amplifier is shown in Figure 4-3 to show the basic principles of this technique. The amplifier consists of a trans-conductor $g_{m1}$ with output impedance $R_{out}$, an auxiliary input trans-conductor $g_{m2}$, auto-zeroing capacitor $C_{az}$ and switches $S_1$~$S_4$. The input referred offset voltage of the $g_{m1}$ and $g_{m2}$ are $V_{os1}$ and $V_{os2}$, respectively.

![Auto-zeroing amplifier with an auxiliary input stage and integrating capacitor](image)

(a) auto-zeroing phase  
(b) amplifying phase

Figure 4-3 Auto-zeroing amplifier with an auxiliary input stage and integrating capacitor  
(a) auto-zeroing phase (b) amplifying phase
The offset cancellation is done in two phases in auto-zeroing amplifier (Figure 4-3). In auto-zeroing phase $\phi_{AZ}$, the input of $g_{m1}$ is shorted so that its offset $V_{os1}$ causes an output offset current $I_{os}$. This offset-induced current is fed into capacitor $C_{az}$ that drives an auxiliary $g_{m2}$ so as to cause an offset compensating current $I_{comp}$. The voltage $V_{cap}$ across the auto-zeroing capacitor $C_{az}$ will reach a steady state till $I_{os}$ is equal to $I_{comp}$. In the subsequent amplifying phase $\phi_{AZ}$, the integration capacitor $C_{az}$ is disconnected from the output of the amplifier. As a result, the voltage $V_{cap}$ is held constant, and continues to cancel the offset currents $I_{os}$ via $g_{m2}$.

The residual offset of the auto-zeroing amplifier can be determined by:

1. Charge injection on $C_{az}$ at the opening of the switch $S_3$.
2. Leakage on $C_{az}$ during the amplifying phase $\phi_{AZ}$
3. Limited voltage DC gain of the $g_{m1}$ and $g_{m2}$ stages.

In steady state during auto-zeroing phase $\phi_{AZ}$, the voltage across the capacitor, $V_{cap}$ is equal to

$$V_{cap} = V_{os1}g_{m1}R_{out} + (V_{os2} - V_{cap})g_{m2}R_{out}$$  \(4-1\)

Thus,

$$V_{cap} = \frac{V_{os1}g_{m1}R_{out} + V_{os2}g_{m2}R_{out}}{1 + g_{m2}R_{out}}$$  \(4-2\)

while during the signal phase $\phi_{AZ}$, the following equation applies:

$$V_{out} = (V_1 + V_{in})g_{m1}R_{out} - V_{cap}g_{m2}R_{out} = g_{m1}R_{out}V_{in} + \frac{V_{os1}g_{m1}R_{out}}{1 + g_{m2}R_{out}} + \frac{V_{os2}g_{m2}R_{out}}{1 + g_{m2}R_{out}}$$  \(4-3\)

The residual offset due to finite gain of the main and auxiliary amplifiers can be expressed by:

$$V_{os,\text{res, gain}} = \frac{V_1}{1 + g_{m2}R_{out}} + \frac{V_{os2}g_{m2}R_{out}}{g_{m1}R_{out}} \approx \frac{V_{os1}}{g_{m2}R_{out}} + \frac{V_{os2}}{g_{m1}R_{out}}$$  \(4-4\)
Except for the limited voltage gain of the main and auxiliary amplifiers, additional residual offset is also caused by the differential charge-injection mismatch \( \Delta Q_{\text{inj}} \) of switches \( S_3 \) and the leakage of the capacitor \( C_{az} \) during the signal phase. The input referred residual offset caused by the charge-injection mismatch is equal to:

\[
V_{os,\text{res, inj}} = \frac{g_{m2} \Delta Q_{\text{inj}}}{g_{m1} C_{az}}
\]  

(4-5)

Thus the total residual input referred offset for the auto-zeroing amplifier is

\[
V_{os,\text{res}} = \frac{V_{os1}}{g_{m2} R_{\text{out}}} + \frac{V_{os2}}{g_{m1} R_{\text{out}}} + \frac{g_{m2} \Delta Q_{\text{inj}}}{g_{m1} C_{az}} = \frac{V_{os1}}{A_1} + \frac{V_{os2}}{A_2} + \frac{g_{m2} \Delta Q_{\text{inj}}}{g_{m1} C_{az}}
\]

(4-6)

where \( A_1 \) and \( A_2 \) are the voltage gain of the main and auxiliary amplifiers.

Since \( V_{os1} \) and \( V_{os2} \) will be in the millivolt range, the first and second term in (4-6) can be easily reduced to the several microvolt level by ensuring that DC gain, \( A_1 \) and \( A_2 \) are both larger than 60dB. In order to reduce the third term, minimum size transistors can be used in switch \( S_3 \) to reduce the injected charge into the auto-zeroing capacitor. The residual offset due to charge injection can be attenuated by increasing the ratio \( g_{m1}/g_{m2} \) when referred to the input.

The auto-zeroing can also reduce the input-referred 1/f noise. The reduction depends on the sampling frequency and is maximized if this sampling frequency is higher than the 1/f corner frequency. A quantitative noise calculation is provided by Enz [88]. A more qualitative analysis will be given as follows in order to understand the auto-zeroing effect on the 1/f noise intuitively.

As shown in Figure 4-3, the auto-zeroing capacitor \( C_{az} \) and switch \( S_3 \) act as a sample-and-hold filter. This filter samples the offset and noise of the amplifier during the auto-zeroing phase. In the following amplifying phase, the sampled offset and noise are subtracted from the output. Since the sampling and subtraction do not occur at the same time but sequentially, only the static offset and slow-changing, i.e. low-frequency noise can be cancelled. Furthermore, because the amplifier’s output needs to settle during auto-zeroing phase, the amplifier’s bandwidth \( f_{\text{null}} \) in auto-zeroing phase, as expressed in
(4-7), should be N times (N=3~5) larger than the auto-zeroing frequency $f_{az}$. Thus, broadband noise of the auto-zeroing amplifier will be under-sampled on $C_{az}$, which means that noise above the auto-zeroing frequency will be folded-back to the low-frequency domain due to noise-aliasing [88]. The input-referred residual thermal noise of the auto-zeroing amplifier in the low frequency domain is boosted approximately by the ratio of the auto-zeroing amplifier’s bandwidth $f_{null}$ and the sampling frequency $f_{az}$, as shown in Figure 4-4. Due to different handling of the offset, the noise-aliasing penalty can be avoided by using chopping amplifier instead, which will be introduced in next section in details.

$$f_{null} = \frac{g_{m2}}{2\pi C_{az}}$$  (4-7)

![Figure 4-4 Input-referred residual noise spectrum of the auto-zeroing amplifier](image)

4.3 Chopping techniques

The chopping technique modulates the offset into higher frequency domain and uses a low-pass filter to remove that. An example of a chopping amplifier is shown in Figure 4-5. This amplifier consists of two frequency modulators (choppers), CH1 and CH2, a voltage amplifier $A_1$ and a low-pass filter (LPF). The input signal $V_{in}$ is modulated by the input chopper CH1 by a square wave signal $\Phi$, at a frequency $f_{CH}$. The modulated signal is amplified then demodulated back to the baseband by another output chopper CH2. The offset of the amplifier, in contrast, is only modulated to the chopping frequency and
its harmonics. These components will then be removed by the low-pass filter [21]. The waveforms in the chopping amplifier in both time and frequency domain are shown in the Figure 4-6 and Figure 4-7 respectively.

Figure 4-5 Chopping amplifier

Figure 4-6 Waveforms of the chopping amplifier in time domain
As shown in Figure 4-7, the chopping technique can completely remove the 1/f noise when $f_{CH}$ is higher than the 1/f noise corner frequency. As a result, the low-frequency white noise level is almost equal to the wideband thermal noise. The advantage of the chopping technique over the auto-zeroing amplifier is that the input signal of the amplifier is not sampled but modulated thus the wideband noise will not be folded back to the baseband. A typical input-referred noise spectrum is shown in Figure 4-8.
4.3.1 Auto-zeroing vs Chopping in ΣΔ modulator

Because auto-zeroing amplifier has the noise-folding back effect, to achieve similar residual in-band input referred noise, the wideband thermal noise floor of the auto-zeroing amplifier should be N times lower (N=\(f_{\text{null}}/f_{\text{AZ}}\)) than that of the chopping amplifier, as illustrated in Figure 4-4 and Figure 4-8.

The thermal noise of the thermopile’s interface amplifier is illustrated in (4-8)

\[
V_{th,n}^2 = 4k_B T \left( \frac{2}{3} g_m \right) \Delta f
\]

where \(g_m\) is the trans-conductance of the input stage of the interface amplifier, \(k_B\) is Boltzmann’s constant, \(T\) is the absolute temperature and \(\Delta f\) is the band of interest.

As a result, to achieve the same in-band thermal noise, the \(g_m\) in auto-zeroing amplifier should be designed to be N times larger than that of the chopping amplifier, which means more power consumption of the interface circuit. Though the power consumption of the circuit is much smaller than the power consumption of the heaters, it can still induce differential self-heating in the wind sensor chip. This can lead to wind measurement errors if the circuit’s power consumption is comparable to the differential heat loss \(\delta P\) induced by the air-flow. Thus, the interface circuit’s power consumption should be kept as small as possible to minimize the errors induced by self-heating.

Because there is no broadband noise folding back effect for chopping amplifier, for a given in-band noise floor, the input \(g_m\) of a chopping amplifier can be N times smaller than that of an auto-zeroing amplifier. Accordingly, the power consumption of the circuit will be N times smaller (N=3~5), which means less error induced by the circuit’s self-heating. It can be concluded that in this design, a chopping amplifier rather than an auto-zeroing amplifier is used to interface the thermopile.

4.4 Summary

The resolution of the second-order ΣΔ modulator should be fundamentally limited by the thermal noise of the thermopiles. In practice, however, the input-referred offset noise of the thermopile’s interface amplifier can also become the major source of the error in the conversion of ΣΔ modulator. This chapter firstly analyzes and models the
input-referred offset and noise of CMOS amplifiers. Dynamic offset cancellation techniques (auto-zeroing and chopping) can be applied to the interface amplifier to reduce those errors. The main difference in performance between auto-zeroing and chopping is the residual noise in the band of interest. The chopping reduces the 1/f noise to the minimum thermal noise floor, while auto-zeroing has an increased noise due to the noise-folding back effect. As a result, to achieve the same in-band thermal noise, the $g_m$ in auto-zeroing amplifier should be designed to be several times larger than that of the chopping amplifier, which means more circuit power consumption, thus more self-heating. Self-heating can introduce a measurement error of the differential heat loss $\delta P$ induced by the air-flow. Thus, in this design, a chopping amplifier rather than an auto-zeroing amplifier will be used to interface the thermopile.
Chapter 5 Realizations

This chapter describes two realizations of thermal wind sensor chip: a first proof-of-concept prototype and a final prototype. Both chips were realized in a standard 0.7μm CMOS process. The concept of second-order ΣΔ modulator was firstly successfully verified with the proof-of-concept prototype. In the reference design [3], the output of the thermopile was interfaced with an auto-zeroing amplifier, which boosted in-band thermal noise due to the noise-folding back. In this work, the thermopile’s interface amplifier will be implemented with a chopping amplifier instead. For a given in-band noise power, the chopping amplifier dissipates less power than the auto-zeroing amplifier, resulting in smaller wind measurement error caused by circuit’s self heating effect. The wind tunnel measurement shows the proof-of-concept prototype dissipated 50mW and achieved wind speed and angle errors of ±4% and ±2°, respectively. Because further reduction of the power consumption appeared to be limited by the interface amplifier’s residual offset and its drift, a system-level chopped amplifier was realized in the final prototype to interface the thermopile. The final prototype dissipated only 25mW, while maintaining the same measurement accuracy as the first prototype. As introduced in Chapter 3, ambient temperature can be determined by measuring the frequency of the peak tone in the modulator’s output. Without trimming, the measurement error was less than ±1°C for temperatures ranging from -40°C to 50°C.

This chapter firstly derives the specifications of the thermopile’s interface circuit based on the requirements of the ΣΔ modulator. The design/realization and measurement results of the first and second prototype will be described afterwards. Finally, a performance comparison table will be given.

5.1 Specifications of the thermopile interface circuit

5.1.1 Offset/Drift

The input-referred offset $V_{os}$ of the thermopile’s interface amplifier can be considered as noise at DC. The electronic noise’s transfer function from the input of the thermopile’s
interface amplifier to the output of the modulator, i.e. $NTF_{en}$, is illustrated in equation (3-6). Because the gain of thermal filter is finite, the DC gain of $NTF_{en}$ is not zero. Thus, at the output of modulator, there is output-referred offset $V_{os,\text{out}}$ induced by the thermopile interface amplifier's offset $V_{os}$, as shown in (5-1)

$$V_{os,\text{out}} = NTF_{en}(0) \cdot V_{os} \quad (5-1)$$

The DC gain of $NTF_{en}$, i.e. $NTF_{en}(0)$, versus the heater power consumption was simulated with the quasi-linear model (Figure 5-1). The spec of heater power consumption $P_{\text{ref}}$ of the first prototype is set to be 25mW, which means $NTF_{en}(0)=57$dB.

![Figure 5-1 Simulated DC gain of the $NTF_{en}$ versus heater power consumption $P_{\text{ref}}$ ($P_{n}=25$mW)](image)

If the offset of the thermopile interface amplifier $V_{os}$ is static, the output-referred error $V_{os,\text{out}}$ can be calibrated (The details of the calibration will be introduced in section 5.2.8.) In practice, the offset error $V_{os,\text{out}}$ will, in general, drift due to aging or ambient temperature variation, resulting in offset drift $\Delta V_{os,\text{out}}$. That means the wind sensor's measurement inaccuracy will be increased due to the offset drift in the outdoor environment. Because the resolution of second-order $\Sigma\Delta$ modulator is specified to be 14-bit, the maximum allowable output-referred offset drift $\Delta V_{os,\text{out,max}}$ should be smaller than 1 LSB, as shown in (5-2)
\[ \Delta V_{os,\text{out, max}} < \frac{V_{\text{out}}}{2^{14}} = \frac{2}{2^{14}} = 0.12 mV \]  

(5-2)

where \( V_{\text{out}} \) is the normalized output swing of the quantizer, which is 2V in this design.

If the output-referred offset error is referred to the input of the thermopile interface amplifier, the maximum allowable input offset drift \( \Delta V_{os,\text{max}} \) of the thermopile interface amplifier is illustrated in (5-3)

\[ \Delta V_{os,\text{max}} = \frac{\Delta V_{os,\text{out}}}{NTF_en(0)} = \frac{0.12 mV}{57 dB} \approx 0.18 \mu V \]  

(5-3)

According to [89], the average temperature drift of the offset per 1°C is proportional to the offset itself, the ratio is defined as the offset temperature coefficient, i.e. TC, which is about 100ppm/°C [89]. For the whole specified temperature range [-40°C, 50°C], the offset of the interface amplifier \( V_{os} \) should satisfy:

\[ V_{os} \cdot TC \cdot \Delta T < \Delta V_{os,\text{max}} \]  

(5-4)

where \( \Delta T=90°C \), thus

\[ V_{os} < 2 \mu V \]  

(5-5)

The specification of the thermopile interface amplifier’s offset can also be obtained based on the performance of the reference design [3]. In the reference design, the offset of the thermopile’s interface amplifier, which is less than 25 \( \mu V \), can result in satisfactory performance with a heater power consumption of about 450mW. In this design the target total heater power consumption is supposed to be reduced by 9x, i.e. from 450mW to 50mW. As shown in Figure 5- 1, \( NTF_{en}(0) \) is inversely proportional to the heater power consumption. For a given output referred offset error, if the total power consumption is reduced by 9x compared to the reference design [3], the input-referred offset budget should be also reduced by 9x, to about 2.75 \( \mu V \). This offset requirement is a little larger than that in (5-5). To keep some margin in this work, the specification for the maximum allowable offset of the thermopile interface amplifier is set to 2.0 \( \mu V \).
5.1.2 Trans-conductance $g_m$

The thermal noise density of the thermopile and interface amplifier are shown in (5-6) and (5-7), respectively.

\[ V_{n,R_{th}}^2 = 4kTR_{th} \]  \hspace{1cm} (5-6)
\[ V_{n,gm}^2 = 4kT \frac{2}{3} g_m \]  \hspace{1cm} (5-7)

where $k$ is Boltzmann’s constant, $T$ is the absolute temperature, $R_{th}$ is the resistance of the thermopile and $g_m$ is the trans-conductance of the thermopile interface amplifier.

To ensure that the thermopile’s resistance is the dominant source of thermal noise, the input-referred thermal noise of the thermopile’s interface amplifier should be less than thermopile’s thermal noise. Thus, the $g_m$ of the interface amplifier should satisfy that:

\[ g_m > \frac{2}{3R_{th}} \]  \hspace{1cm} (5-8)

In this design, the resistance of the thermopile is estimated to be 168kΩ so the input trans-conductance was set to be larger than 20µs for margin.

5.1.3 Chopping frequency $f_{CH}$

As discussed in Chapter 4, the chopping frequency of the chopper amplifier, $f_{CH}$, should be set to be higher than the 1/f noise corner frequency such that the in-band 1/f noise can be completely removed. For a CMOS amplifier with reasonable input transistor size, the simulated 1/f corner frequency is around 1 kHz as shown in Figure 5-2. Thus, the chopping frequency is set to be larger than 1 kHz, to leave some margin.
5.1.4 Low-pass filter’s pole frequency

As explained in Chapter 3, the second-order $\Sigma\Delta$ modulator will oscillate at a certain frequency, where the phase shift of the loop filter equals 180°. This manifests itself as a strong peak tone in the output spectrum of the modulator at this frequency, i.e. $f_{\text{peak}}$, which is around 20Hz (Figure 3-23). The thermal low-pass filter’s pole frequency, i.e. $f_{\text{pole}}$, in second-order $\Sigma\Delta$ modulator should be designed to be much smaller than $f_{\text{peak}}$ such that its phase shift at $f_{\text{peak}}$ will be a constant 90°. As a result, $f_{\text{peak}}$ will be only determined by the thermal filter’s phase-shift and hence by the temperature of the silicon substrate. In turn, chip’s temperature can be determined by measuring $f_{\text{peak}}$. The details of temperature measurement will be introduced in section 5.3.5. In this design, the pole frequency of the electrical integrator, $f_{\text{pole}}$, will be designed to be less than 1 Hz, which is much smaller than the peak tone frequency $f_{\text{peak}}$.

5.1.5 Specification summary

The specifications for the thermopile’s interface amplifier in the second-order $\Sigma\Delta$ modulator are summarized in Table 5-1.

<table>
<thead>
<tr>
<th>Specifications</th>
<th>Value</th>
<th>Note</th>
</tr>
</thead>
<tbody>
<tr>
<td>$g_m$</td>
<td>&gt;20µS</td>
<td></td>
</tr>
<tr>
<td>$f_{\text{CH}}$</td>
<td>&gt;1 kHz</td>
<td>chopping frequency</td>
</tr>
<tr>
<td>$V_{\text{os}}$</td>
<td>&lt;2µV</td>
<td>input-referred residual offset</td>
</tr>
<tr>
<td>$f_{\text{pole}}$</td>
<td>&lt;1Hz</td>
<td>low-pass filter’s pole</td>
</tr>
</tbody>
</table>
5.2 Proof-of-Concept Prototype realization

This section describes the implementation details of the first proof-of-concept prototype. The major purpose of this design is to verify whether the second-order TΣΔ modulator can properly work or not. The heater power consumption of the thermal wind sensor in this design is supposed to be reduced by combining the second-order TΣΔ modulator and CP mode, compared to the reference design [3]. In order to compare the performance of first-order and second-order TΣΔ modulators, an auto-zeroed amplifier together with a chopped integrator are both realized in the same chip, as the interface circuit of the thermopile (Figure 5-3). Via a pair of multiplexers, the thermal wind sensor can be switched between first-order and second-order mode.

![Block diagram of the first proof-of-concept prototype.](image)

(a) first-order TΣΔ Modulator with auto-zeroed amplifier. (b) second-order TΣΔ modulator with chopped Integrator.

5.2.1 Specifications of the chopped integrator

As shown in Figure 5-3, for the second-order TΣΔ modulator, the chopped integrator is realized using a continuous-time passive OTA-C stage. It should be noticed that the offset of OTA, $V_{os}$, can generate an output offset current $I_{os}$, as shown in (5-9)

$$I_{os} = g_{m} V_{os}$$  \hspace{1cm} (5-9)
In this chopped integrator, this offset current will be modulated by the output chopper and then integrated into the capacitor $C_{\text{int}}$, giving rise to a triangular output ripple with amplitude proportional to the initial input offset. If the sampling of the following quantizer is synchronized with the chopper and takes place at the zero-crossing of the output ripple, no sampling errors will be introduced by the ripples (Figure 5-4).

![Timing diagram of the output ripple and sampling clock of the quantizer](image)

In order to achieve the pole frequency $<1$ Hz, the output resistance $R_{\text{out}}$ of 1.5 GΩ and the integrating cap $C_{\text{int}}$ of 120pF are used. The specifications for the chopped OTA-C integrator are listed in Table 5-2.

<table>
<thead>
<tr>
<th>Specifications</th>
<th>Value</th>
<th>Note</th>
</tr>
</thead>
<tbody>
<tr>
<td>Temp. range</td>
<td>-40°C ~ 50°C</td>
<td></td>
</tr>
<tr>
<td>$g_m$</td>
<td>&gt;20μS</td>
<td>trans-conductance</td>
</tr>
<tr>
<td>$C_{\text{int}}$</td>
<td>120pF</td>
<td>integrating capacitor</td>
</tr>
<tr>
<td>$R_{\text{out}}$</td>
<td>1.5GΩ</td>
<td>output resistance</td>
</tr>
<tr>
<td>$f_{\text{pole}}$</td>
<td>&lt;1Hz</td>
<td>low-pass filter’s pole freq</td>
</tr>
<tr>
<td>$V_{\text{os}}$</td>
<td>&lt;2μV</td>
<td>residual input-referred offset</td>
</tr>
</tbody>
</table>

5.2.2 Circuit implementations of the chopped integrator

Figure 5-5 illustrates the chopper amplifier circuit used in the electrical integrator in second-order $T\Sigma\Delta$ modulator. It is a conventional fully differential folded-cascode topology with PMOS input pair. In order to reduce the amplifier’s input referred 1/f noise and initial offset, the PMOS input transistors $M_4$ and $M_5$ are matched with a cross-coupled layout and a relatively large transistor size. The input transistors $M_4$, $M_5$ are
biased in weak inversion and the transistors M_{13}, M_{14}, M_{19}, M_{20} are biased in strong inversion. This leads to \((g_m/id)_{4,5}\) of about 20 and \((g_m/id)_{13,14,19,20}\) of about 5. The input transistors contribute to the input referred noise and offset directly while the noise and offset contributions of the active load transistors M_{13}, M_{14} and current source transistors M_{19}, M_{20} are reduced by the ratio of their trans-conductance to that of the input transistors. Therefore, when the noise and offset of M_{13}, M_{14}, M_{19}, and M_{20} are referred to input, they can be suppressed by a factor of about 4. The noise contribution of the cascode transistors M_{15}, M_{16}, M_{17}, and M_{18} can be neglected because of source degeneration due to their common gate connection.

**Common-mode feedback**

The common mode output control consists of two transistors M_{11} and M_{12} biased in their linear resistive region and connected at their drains with an equal drain source voltage \(V_{DS,11}=V_{DS,12}=V_{DS}\). The overdrive voltage \(V_{GT}\) of these two transistors is then set to be larger than \(V_{DS}\), as shown in (5-10)

\[
V_{GT} = V_{GS} - V_{TH} > V_{DS} \tag{5-10}
\]
Therefore, the transistor $M_{11}$ and $M_{12}$ are biased in triode region and their drain current $I_D$ is equal to

$$I_D = \mu C_{ox} \frac{W}{L} V_{DS} (V_{GS} - V_{TH} - \frac{1}{2} V_{DS})$$  \hspace{1cm} (5-11)$$

The sum of drain currents of transistor $M_{11}$ and $M_{12}$ is shown in (5-12)

$$I_{DS,11} + I_{DS,12} = \mu C_{ox} \left( \frac{W}{L} \right)_{11,12} V_{DS} (V_{GS,11} + V_{GS,12} - 2V_{TH} - V_{DS})$$  \hspace{1cm} (5-12)$$

Because

$$I_{D,10} = I_{D,19} = I_{D,20}$$  \hspace{1cm} (5-13)$$

And

$$I_{D,1} = I_{D,6}$$  \hspace{1cm} (5-14)$$

Thus the sum of the drain currents of transistors $M_{11}$ and $M_{12}$ is then shown in (5-15)

$$I_{D,11} + I_{D,12} = I_{D,19} + I_{D,20} - I_{D,1} = 2I_{D,6} - I_{D,1} = I_{D,6}$$  \hspace{1cm} (5-15)$$

which means

$$\mu C_{ox} \left( \frac{W}{L} \right)_6 V_{DS} (V_{GS,6} - V_{TH} - \frac{1}{2} V_{DS}) = \mu C_{ox} \left( \frac{W}{L} \right)_{11,12} V_{DS} (V_{GS,11} + V_{GS,12} - 2V_{TH} - V_{DS})$$  \hspace{1cm} (5-16)$$

Because
Thus

\[ V_{GS,6} = \frac{V_{GS,11} + V_{GS,12}}{2} \]  

(5-18)

Because the gate voltage of \( M_6 \) is biased at \( V_{CM} \) and the gates of \( M_{11} \) and \( M_{12} \) are connected to \( V_{out+} \) and \( V_{out-} \) respectively, the output common mode voltage is then regulated to be equal to \( V_{CM} \) as shown in (5-19)

\[ V_{CM} = \frac{V_{out-} + V_{out+}}{2} \]  

(5-19)

**Chopper design**

As shown in Figure 5-5, the input and output choppers are placed at the input of the amplifier and the source nodes of the cascode transistors. The schematic diagram of the chopper is shown in Figure 5-6. In the ideal case, the offset as well as the 1/f noise of the amplifier can be completely removed by chopping. However, because of non-ideal choppers, a residual offset can still exist. In the following sections, the reasons for the non-zero residual offset of chopper amplifiers will be discussed in detail.

![Figure 5-6 Schematic diagram of the chopper](image-url)
5.2.3 Residual offset of the Chopper Amplifier

The chopping technique is used to reduce the input referred offset of the amplifier. A good rule of thumb is that the chopping can be expected to reduce the initial offset with a factor of 100 to 1000. However, with offset specification of less than 2µV, the causes for the residual offset of the chopper amplifier still needs to be carefully analyzed.

Residual Offset due to Chopper Clock Feed-through

The residual offset due to unbalanced chopper clock feed-through can be explained with Figure 5-7 and Figure 5-8. The parasitic capacitances between the clock node of the input chopper $C_{H1}$ ($\phi_{CH}$) and the two input nodes ($V_{a+}$ and $V_{a-}$) of the amplifier are modeled as $C_1$ and $C_2$, respectively. Moreover, the parasitic capacitances between the clock node of the output chopper $C_{H2}(\phi_{CH})$ and the two output nodes ($V_{b+}$ and $V_{b-}$) of the amplifier are modeled as $C_3$ and $C_4$, respectively. The ON-resistances of the switches in the input chopper are modeled as $R_{in,1}$ and $R_{in,2}$ respectively, while $R_s$ is the resistance of the thermopile.

Figure 5-7 Charge injection model in a chopped amplifier [21]
Firstly, the effect of input chopper switch mismatch in the chopper amplifier will be analyzed. Because there is a slight mismatch between the MOS switches in the input chopper, a difference $\Delta C$ between $C_1$ and $C_2$ can exist. The clock signal can feed-through via the unbalanced $C_1$ and $C_2$ so that there are voltage spikes at the amplifier’s input, $V_a$, as shown in Figure 5-8. The spikes at $V_a$ will be translated into a residual offset, because these spikes are actually demodulated to the same polarity by the input chopper towards $V_{in}$, which is the input of the chopper amplifier (Figure 5-8).

Each time the chopper clock changes its polarity, charge will be injected into the input. The differential charge is expressed in (5-20)

$$q_{inj, in} = \Delta C \cdot V_{CH}$$

where $V_{CH}$ is the driving voltage of clock $\Phi_{CH}$.

This charge is injected two times per clock period and the induced offset current will run through the resistors $R_s$, $R_{in1}$ and $R_{in2}$. Therefore, the residual offset can be expressed as:

$$V_{os, res1} = 2\left( R_{in1} + R_{in2} + R_o \right) \Delta C \cdot V_{CH} \cdot f_{CH}$$

(5-21)
where $f_{CH}$ is the chopping frequency. An obvious way to reduce this residual offset is to reduce chopping frequency $f_{CH}$. However, the chopping frequency should be at least higher than the 1/f noise corner frequency.

The mismatch of capacitors $C_3$ and $C_4$ depicted in Figure 5-7 can also cause residual offset. If there is a slight mismatch between the two capacitors ($C_3$ and $C_4$), a differential current spike will appear at $V_b$. Each time the chopper clock changes its polarity, charge will be injected into the output of amplifier, $V_b$. The differential charge is expressed in (5-22)

$$q_{inj,out} = |C_3 - C_4| \cdot V_{CH} \quad (5-22)$$

The induced output-referred unbalanced current $I_{os,out}$ is shown in (5-23)

$$I_{os,out} = 2|C_3 - C_4| \cdot V_{CH} \cdot f_{CH} \quad (5-23)$$

When the offset current is referred to the input of the chopper amplifier, the residual offset can be expressed by:

$$V_{os,res2} = \frac{2|C_3 - C_4| \cdot V_{CH} \cdot f_{CH}}{g_m} \quad (5-24)$$

where $g_m$ is the trans-conductance of the chopped amplifier.

In conclusion, the residual offset induced by the chopper clock feed-through is expressed in (5-25)

$$V_{os,res} = V_{os,res1} + V_{os,res2} \quad (5-25)$$

In order to reduce this residual offset $V_{os,res}$, several methods can be applied:

1) Minimize the chopping frequency $f_{CH}$.

As shown in (5-21) and (5-24), the residual offset caused by the clock's unbalanced charge injection can be reduced by decreasing the chopping frequency $f_{CH}$. At the same
time, $f_{CH}$ should be slightly higher than the $1/f$ noise corner frequency of amplifier to minimize the residual $1/f$ noise and offset.

(2) Optimized matching between the MOS transistors in chopper

**Residual Offset due to OTA’s Cascode Transistor Mismatch**

As shown in Figure 5-9, residual offset of the chopper amplifier can also be induced by the mismatch between the cascode transistors in the main branch of the PMOS-input folded-cascode amplifier [90].

![Figure 5-9 Main branch of a folded-cascode amplifier with embedded chopper [90]](image-url)
The upper PMOS current sources are $I_1$ and $I_2$, and the chopper is located at the source of the cascode transistors $M_{17}$ and $M_{18}$. The threshold voltage mismatch between transistors $M_{17}$ and $M_{18}$ can be modeled as an offset voltage $V_{os}$ as shown in Figure 5-9. Thus, a DC voltage is established at the sources of the cascode transistors and then modulated by the chopper. A square-wave voltage $V_d$, which appears at the drain nodes of the transistors $M_{19}$ and $M_{20}$ (Figure 5-10) can periodically charge and discharge the parasitic capacitors $C_{p1}$ and $C_{p2}$, resulting in an AC current $I_{p1}-I_{p2}$. Furthermore, due to the finite output impedances of $M_{19}$ and $M_{20}$, square-wave voltage $V_d$ can induce another AC current $I_{d19}-I_{d20}$. The sum of these two AC currents, $I_{CH1}-I_{CH2}$, will be rectified by the chopper itself into an output offset current $I_{S17}-I_{S18}$. The average of this offset current $I_{S17}-I_{S18}$ is $I_{os}$, as expressed in (5-26) [90].
\[ I_{os} = 2f_{CH}(C_{p1} + C_{p2})|v_d| + \frac{|v_d|}{R_{out,19} - R_{out,20}} \quad (5-26) \]

The chopper located at the source of the PMOS cascode transistors can also induce a similar offset current. When the output offset current is referred to the input, the offset voltage can then be derived as (5-27)

\[ V_{os} = \frac{4f_{CH}(C_{p1} + C_{p2})|v_d| + \frac{2|v_d|}{R_{out,19} - R_{out,20}}}{g_m} \quad (5-27) \]

The methods to minimize the chopper amplifier’s offset caused by the mismatch between cascode transistors, are discussed as follows.

(1) Minimize the parasitic capacitance \( C_{p1} \) and \( C_{p2} \)

As shown in Figure 5-9, the size of the \( M_{19} \) and \( M_{20} \) transistors should be as small as possible since the \( C_{p1} \) and \( C_{p2} \) are mainly dominated by their drain-gate capacitances, \( C_{gs19} \) and \( C_{gs20} \). However, mismatch between \( M_{19} \) and \( M_{20} \) will be larger if the transistor size is reduced. The offset current could be increased accordingly. Thus, there is a tradeoff between the drain parasitic capacitance \( C_{p1} \) and \( C_{p2} \) and mismatch of \( M_{19} \) and \( M_{20} \).

(2) Minimize the amplitude of \( V_d \)

Because the minimum size transistors are always used as chopper switches, the ON-resistance of the switching transistors is not negligible. When the biasing current goes through the mismatched chopper switches, the voltage drop mismatch across two parallel paths through the chopper will also contribute to \( V_d \). Hence there is a tradeoff between the size of the chopper switch transistors and \( V_d \). In addition, \( V_d \) can also be reduced by better layout matching between the cascode transistors.
(3) Increase the trans-conductance $g_m$

### 5.2.4 Simulation results of the chopper amplifier

In the temperature range [-40°C, 50°C], simulation results of the chopper amplifier (Table 5-3) show that it can meet the requirements as shown in Table 5-2.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Unit</th>
<th>Min.</th>
<th>Typ.</th>
<th>Max.</th>
<th>Note</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{dd}$</td>
<td>V</td>
<td>5</td>
<td>5</td>
<td></td>
<td>supply voltage</td>
</tr>
<tr>
<td>$f_{CH}$</td>
<td>Hz</td>
<td>8192</td>
<td></td>
<td></td>
<td>chopping frequency</td>
</tr>
<tr>
<td>$C_{int}$</td>
<td>pF</td>
<td>125</td>
<td></td>
<td></td>
<td>integrating MOS cap</td>
</tr>
<tr>
<td>temp. range</td>
<td>°C</td>
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<td>20</td>
<td>50</td>
<td></td>
</tr>
<tr>
<td>band of interest</td>
<td>Hz</td>
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<td>1</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Simulation result</th>
<th>Unit</th>
<th>Min.</th>
<th>Typ.</th>
<th>Max.</th>
<th>Note</th>
</tr>
</thead>
<tbody>
<tr>
<td>$I_{supply}$</td>
<td>μA</td>
<td>4.2</td>
<td>5</td>
<td>6.3</td>
<td>circuit’s current consumption</td>
</tr>
<tr>
<td>$g_m$</td>
<td>μS</td>
<td>21</td>
<td>25</td>
<td>31.3</td>
<td>trans-conductance</td>
</tr>
<tr>
<td>$f_{3dB}$</td>
<td>Hz</td>
<td>0.52</td>
<td>0.75</td>
<td>0.97</td>
<td>low-pass filter pole freq</td>
</tr>
<tr>
<td>residual offset</td>
<td>μV</td>
<td>1.41</td>
<td>1.7</td>
<td>2.0</td>
<td>&lt;2.0</td>
</tr>
<tr>
<td>residual noise density</td>
<td>nV/√Hz</td>
<td>12</td>
<td>15</td>
<td>19</td>
<td>should be smaller than the thermopile’s thermal noise density $\sqrt{V_{n,Res}^2} = \sqrt{4kT/Rth} &lt; 2.0$</td>
</tr>
</tbody>
</table>

### 5.2.5 Auto-zeroing amplifier design

In order to compare the performance of first-order and second-order TΣΔ modulators, an auto-zeroed amplifier is also realized in the wind sensor chip, as interface circuit of the thermopile (Figure 5-3). Via a pair of multiplexers, the thermal wind sensor can then be switched between first-order and second-order mode. The operating principles of the applied auto-zeroing amplifier circuit with auxiliary input were already discussed in section 4.2.1. The schematic diagram and circuit realization of the auto-zeroing amplifier with differential input are shown in Figure 5-11 and Figure 5-12, respectively. The residual input-referred offset was derived in equation (4-12). It is re-shown here in (5-28).

$$V_{os,ref} = \frac{V_{os1}}{g_{m2}R_{out}} + \frac{V_{os2}}{g_{m1}R_{out}} + \frac{g_{m2}ΔO_{aj}}{g_{m1}C_{az}} = \frac{V_{os1}}{A_2} + \frac{V_{os2}}{A_1} + \frac{g_{m2}ΔO_{aj}}{g_{m1}C_{az}} \quad (5-28)$$
To reduce the initial input-referred offset $V_{os1}$, the input PMOS transistors ($M_4$ and $M_5$) of the main amplifier are matched with cross-coupled layout and relatively large transistor size (400/1). The same techniques were also applied to the auxiliary input transistors ($M_7$ and $M_8$) to reduce the offset voltage, $V_{os2}$. Since $V_{os1}$ and $V_{os2}$ are both estimated to be less than 3mV, the first and second terms in (5-28) can be reduced to less than 1µV by ensuring that DC gain of the $A_1$ and $A_2$ are about 70dB. In order to reduce the third term in (5-28), minimum size transistors (1/0.7) are used in switch $S_{cap}$ and $C_{az}$ is set to be as large as 80 pF. The residual offset due to charge injection can also be attenuated by the ratio $g_{m2}/g_{m1}$ when referred to the input. Due to the noise-folding effect, to achieve the same in-band thermal noise level as the chopper amplifier, $g_{m1}$ is designed to be 3~5 times larger than the specification in Table 5-1. The tail current of the auxiliary input branch should be biased to be sufficiently large to cancel the offset current induced by the main input branch. The common-mode feedback is similar to that of the chopper amplifier (section 5.2.2.)

![Auto-zeroing amplifier](image)

Figure 5-11 Auto-zeroing amplifier used in first-order ΣΔ Modulator
5.2.6 Simulation results of the auto-zeroing amplifier

In the temperature range [-40°C, 50°C], the simulation results of the auto-zeroing amplifier is shown in Table 5-4. It can be seen that, compared to the chopper amplifier, the auto-zeroing amplifier achieved similar input-referred noise and offset while consuming about 4 times more current. It can be proven that the chopper amplifier will introduce smaller wind measurement error due to its smaller self-heating caused by the circuit’s power consumption.
Table 5-4 Simulation results of the auto-zeroing amplifier

<table>
<thead>
<tr>
<th>Parameters</th>
<th>Unit</th>
<th>Min.</th>
<th>Typ.</th>
<th>Max.</th>
<th>Note</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{dd}$</td>
<td>V</td>
<td>5</td>
<td></td>
<td></td>
<td>supply voltage</td>
</tr>
<tr>
<td>$f_{AZ}$</td>
<td>Hz</td>
<td>8192</td>
<td></td>
<td></td>
<td>auto-zeroing freq.</td>
</tr>
<tr>
<td>$C_{az}$</td>
<td>pF</td>
<td>80</td>
<td></td>
<td></td>
<td>auto-zeroing cap</td>
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<tr>
<td>temp. range</td>
<td>°C</td>
<td>-40</td>
<td>20</td>
<td>50</td>
<td></td>
</tr>
<tr>
<td>band of interest</td>
<td>Hz</td>
<td>0</td>
<td>1</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Simulation result</th>
<th>Unit</th>
<th>Min.</th>
<th>Typ.</th>
<th>Max.</th>
<th>Note</th>
</tr>
</thead>
<tbody>
<tr>
<td>$I_{supply}$</td>
<td>µA</td>
<td>20.52</td>
<td>23</td>
<td>24.6</td>
<td>circuit’s current consumption</td>
</tr>
<tr>
<td>$g_{m1}$</td>
<td>µS</td>
<td>112.7</td>
<td>125</td>
<td>132.3</td>
<td>trans-conductance of the main amplifier</td>
</tr>
<tr>
<td>$g_{m2}$</td>
<td>µS</td>
<td>22.5</td>
<td>25</td>
<td>26.6</td>
<td>trans-conductance of the auxiliary amplifier</td>
</tr>
<tr>
<td>$V_{os1}$</td>
<td>mV</td>
<td>1.23</td>
<td>1.5</td>
<td>1.81</td>
<td>input-referred offset of the main amplifier</td>
</tr>
<tr>
<td>$V_{os2}$</td>
<td>mV</td>
<td>2.71</td>
<td>3.1</td>
<td>3.42</td>
<td>input-referred offset of the auxiliary amplifier</td>
</tr>
<tr>
<td>$A_1$</td>
<td>dB</td>
<td>80.3</td>
<td>83</td>
<td>84.3</td>
<td>DC gain of the main amplifier</td>
</tr>
<tr>
<td>$A_2$</td>
<td>dB</td>
<td>71.2</td>
<td>74</td>
<td>76.3</td>
<td>DC gain of the auxiliary amplifier</td>
</tr>
<tr>
<td>residual offset</td>
<td>µV</td>
<td>1.25</td>
<td>1.5</td>
<td>1.93</td>
<td>&lt;2</td>
</tr>
<tr>
<td>residual noise density</td>
<td>nV/√Hz</td>
<td>17</td>
<td>22</td>
<td>27</td>
<td></td>
</tr>
</tbody>
</table>

5.2.7 Chip Micrograph

The micrograph of the first proof-of-concept prototype is shown in Figure 5-13. The chip was realized in a 0.7 um 1-poly 2-metal CMOS process and occupies 4mm×4mm of silicon area. Four poly-silicon resistors act as heaters, while four p+/Al thermopiles sense the on-chip temperature differences. Opposing thermopiles on the north and south side of the chip, are connected in series to sense the east-west component of the temperature gradient $\delta T$, which is induced by the air-flow. Similarly, the thermopiles on the east and west side of the chip, are connected in series to sense north-south component of the temperature gradient $\delta T$. The readout circuits are located in the middle of the chip. The resistor in the chip’s north-west corner is used as a heater for test
purpose, to generate a temperature gradient on the surface of the chip. The feasibility of a thermal wind sensor with a second-order $\Sigma\Delta$ interface was first demonstrated by this proof-of-concept chip [91]. Its wind tunnel measurement results are discussed in the following section.

![Figure 5-13 Micrograph of the wind sensor chip (first proof-of-concept prototype)](image)

### 5.2.8 Wind sensor measurement

**Wind Tunnel**

The picture of the wind tunnel used to calibrate and test the thermal wind sensor is shown in Figure 5-14. To perform the test, the wind sensor is placed in the sensor’s room. The wind direction can be accurately adjusted by rotating the sensor. The specifications of the wind tunnel are summarized in Table 5-5.

<table>
<thead>
<tr>
<th>specifications</th>
<th>unit</th>
<th>value</th>
</tr>
</thead>
<tbody>
<tr>
<td>wind speed range</td>
<td>m/s</td>
<td>0.5~25</td>
</tr>
<tr>
<td>resolution of wind speed</td>
<td>m/s</td>
<td>0.1</td>
</tr>
<tr>
<td>resolution of wind direction</td>
<td>degree</td>
<td>0.1</td>
</tr>
</tbody>
</table>
Figure 5-14 The wind tunnel used to calibrate and test the thermal wind sensors

**Performance of $\Sigma \Delta$ modulator**

The power spectrum of the sensor’s bit-stream output was measured at wind speeds of 0m/s and 25m/s (Figure 5-15) with $P_{ref}$ of 25mW. The output-referred Signal-to-Noise ratio (SNR) of the modulator can be calculated with the formula shown in (5-29)

\[
SNR = 20 \log_{10} \left( \frac{V_{out}}{\sqrt{V_{n, out}^2}} \right)
\]  

(5-29)

where $V_{out}$ is the output swing of modulator and $\sqrt{V_{n, out}^2}$ is the square root of the total integrated in-band noise.

As shown in Figure 5-15, with wind speed of 0m/s, the SNR in first-order mode was calculated to be about 66dB, which means an 11-bit resolution was achieved. In second-order mode, the in-band noise floor was further suppressed by about 20dB due to the noise shaping provided by the extra electrical integrator. The SNR of the second-order $\Sigma \Delta$ modulator was calculated to be 84dB, i.e. about 14-bit resolution, which is quite
close to the estimated resolution from simulations with the quasi-linear model of the $T\Sigma\Delta$ modulator (Table 3-3).

Figure 5-15 also shows the measured output spectrum of the first and second-order $T\Sigma\Delta$ modulator at 25m/s. It should be noticed that in second-order mode, there is a "1/f noise like" spectrum in low-frequency domain which does not appear with zero wind speed. It is found that this low-frequency noise is caused by wind turbulence or random air currents. This noise can be modeled with the input "wind noise" $P_{\text{wind},n}$ as shown in Figure 3-9. In fact, in order to measure the second-order modulator’s true output noise floor at 0m/s, the sensor has to be shielded by a small box to avoid any possible random air currents. However, this "wind noise" was not detected at all by the first-order $T\Sigma\Delta$ modulator as shown in Figure 5-15. Thus, it can be proven by this experiment that the sensitivity of the thermal wind sensor is indeed increased by applying the second-order $T\Sigma\Delta$ modulator.

As predicted by the behavioral model in Chapter 3, the output of the second-order $T\Sigma\Delta$ modulator is a square-wave with a flow-dependent duty-cycle. Its spectrum exhibits strong tones at a fundamental frequency (about 40Hz) and its harmonics. The modulator’s bit-stream will be decimated by the self-tracking sinc$^2$ filter which was already introduced in section 3.4.6.

![Figure 5-15 Measured output spectrum of the first and second order $T\Sigma\Delta$ modulators at wind speeds of 0m/s and 25m/s.](image-url)
Calibration of the thermal wind sensor

Typically, the values which a sensor can directly measure are different from the values a sensor is supposed to output. For example, many temperature sensors firstly measure the output $\Delta V$ of a Wheatstone bridge and convert it into a temperature reading. The function that can convert the sensor’s measured value into its supposed output, is defined as the sensor’s transfer function. The parameters of this transfer function can be different for each single sensor. Thus, it is necessary to calibrate each sensor to determine these parameters. With reference inputs and the according sensor’s measured values, the parameters of the transfer function can be fitted. For the two-dimensional thermal wind sensor, the outputs are the decimated output of the north-south and east-west $\Sigma \Delta$ modulators, as shown in (5-30)

$$\mu_{ns} = \frac{\delta P_{ns}}{P_{ref}}, \mu_{ew} = \frac{\delta P_{ew}}{P_{ref}}$$ (5-30)

The sensor chip was built into an aerodynamic housing and then measured in a wind tunnel with reference wind speeds and directions. The decimated outputs of the north-south and east-west $\Sigma \Delta$ modulators, i.e. $\mu_{ns}$ and $\mu_{ew}$, are sinusoidal functions of wind direction whose amplitudes are monotonic functions of wind speed (Figure 5-16).

The transfer functions of the wind sensor which can convert $\mu_{ns}$ and $\mu_{ew}$ into the wind speed $U$ and direction $\Phi$ reading are shown in (5-31) and (5-32).

$$\mu_{ns} = \frac{\sqrt{U}}{A_{ns} + B_{ns} \sqrt{U}} \sin (\phi + \varepsilon_{ns}) + D_{ns} \sqrt{U} + E_{ns}$$ (5-31)

$$\mu_{ew} = \frac{\sqrt{U}}{A_{ew} + B_{ew} \sqrt{U}} \cos (\phi + \varepsilon_{ew}) + D_{ew} \sqrt{U} + E_{ew}$$ (5-32)

where $A_{ns}, A_{ew}, B_{ns}, B_{ew}$ are the parameters correlated to the sensor’s geometry and properties of air-flow, and $\varepsilon_{ns}, \varepsilon_{ew}$ are the direction offset constants. It should be noticed that besides the constant $E_{ns}$ and $E_{ew}$, there are offset terms which are proportional to the square root of the wind speed, $\sqrt{U}$. 111
Based on the reference wind speeds/directions and measured decimated modulator's outputs $\mu_{ns}/\mu_{ew}$ shown in Figure 5-16, the parameters in (5-31) and (5-32) can be fitted. When the wind sensor is in use, the $\mu_{ns}$ and $\mu_{ew}$ can be calculated by decimating the north-south and east-west $\Sigma\Delta$ modulator's output bit-stream. $\mu_{ns}$ and $\mu_{ew}$ can then be substituted into the nonlinear equation (5-31) and (5-32), which can be solved by the Newton-Raphson method, resulting in the outputs of wind speed and direction.

![Figure 5-16 Measured output of the north-south (o) and east-west (+) modulators.](image)

**Wind Tunnel Measurement**

Figure 5-17 compares the measured wind velocity of the reference mechanical sensor and thermal wind sensor. It can be seen that the output of the calibrated thermal wind sensor are quite close to the output of the reference mechanical sensor. As shown in Figure 5-18, the errors in the wind speed and direction are less than $\pm 4\%$ (speed) and $\pm 2^\circ$ (direction), for wind speeds between 1 m/s and 25 m/s. Compared to the reference design [1], the CP mode and second-order $\Sigma\Delta$ interface are both applied in the new thermal wind sensor design. The measurement results show that the thermal wind sensor which uses the first proof-of-concept chip, can maintain the similar wind sensing accuracy, while achieving 9x smaller total power consumption [91].
Figure 5-17 Measured wind velocity of the reference mechanical sensor and the thermal wind sensor.

Figure 5-18 Measured wind speed and direction error of the first proof-of-concept prototype.
5.3 Final Prototype realization

5.3.1 Motivation for the second prototype

(1) Reduce the input-referred offset of the thermopile’s interface amplifier, to further reduce the heater power consumption $P_{\text{ref}}$.

As shown in Figure 5-15, with $P_{\text{ref}}$ of 25mW, the second-order $\Sigma\Delta$ modulator’s true noise floor is now less than the “wind noise” $P_{\text{wind,ref}}^2$ caused by wind turbulences in the ambient air. In other words, the resolution of the second-order $\Sigma\Delta$ modulator is now limited by the “wind noise” rather than the thermal noise of the thermopile. Thus, the heater power dissipation $P_{\text{ref}}$ is possible to be further reduced while maintaining the same resolution of $\Sigma\Delta$ modulator, as long as the in-band noise contribution of the thermal noise of the thermopile is still less than the input “wind noise”. However, according to the analysis in section 5.1.1, if the heater power consumption $P_{\text{ref}}$ is reduced by N times, the DC value of the electronic noise transfer function, $|NTF_{\text{en}}(0)|$ will be boosted by N times. Therefore, the input-referred offset of the thermopile’s interface amplifier should also be reduced by N times as compared to the first prototype accordingly, to achieve similar error contribution cause by the offset drift at the output of modulator [3]. In the final prototype, system-level chopping will be applied to the existing chopper amplifier to reduce its offset to sub-µV levels, thus enabling a lower heater power consumption $P_{\text{ref}}$ than that for the first proof-of-concept design.

(2) Shrink the silicon area occupation of the interface circuit, to integrate the digital interface circuit (in a future design).

In order to integrate the digital interface circuit in the future, the chopped integrator can also be reconfigured into an auto-zeroing amplifier with shared OTA and capacitors, to save silicon area. By doing this, the first-order and second-order $\Sigma\Delta$ modulator’s performance can still be compared with the same chip while achieving less silicon area occupation as compared to the first proof-of-concept prototype.

In the following sections, the operating principles of the system-level chopping will be firstly introduced in 5.3.2. The re-configurable amplifier is presented in section 5.3.3. The chip micrograph and wind tunnel measurement results are illustrated in section 5.3.4 and
section 5.3.5 respectively. Temperature measurement results with the final prototype will be shown in section 5.3.5.

5.3.2 Introduction to the system-level chopping technique

Further suppression of the residual offset $V_{os}$ of the thermopile interface amplifier, can be obtained by system-level chopping as shown in Figure 5-19. Compared to the first prototype (Figure 5-3), the chopper switches at the input of the chopping integrator, CL1, and the output of quantizer, CL2, are added. The choppers CH1 and CH2 are fast choppers, which operate at high chopping frequency $f_H$ while the CL1 and CL2 are slow choppers or system choppers, which operate at low chopping frequency $f_L$ ($f_L$ has the value of about several Hz). The inner circuit amplifies and quantizes $V_{in} + V_{os}$ when $\phi_L = 1$, and $(V_{in} - V_{os})$ when $\phi_L = 0$. By averaging two outputs, the effect of offset $V_{os}$ can be (almost) removed. The system-level chopping is done at a relatively slow frequency, $f_L$, to reduce the residual offset due to charge-injection in the fast-chopper switches. Moreover, another slow chopper $C_{C1}$ that operates at low chopping frequency $f_L$, is added to invert the state of the integrator by swapping the integration capacitor $C$, to avoid disturbing the operation of the inner integrator when the slow choppers CL1 and CL2 change their polarity.

![Figure 5-19 Block diagram of system-level chopped thermopile interface circuit](image)

5.3.3 Reconfigurable thermopile interface circuit design

In the second prototype, a reconfigurable amplifier (Figure 5-20) is designed and realized such that the chopped integrator can also be reconfigured into an auto-zeroed
amplifier with shared OTA and capacitors. By operating the switches and choppers differently, the reconfigurable amplifier can switch between the auto-zeroing mode and system-level chopping mode, to compare the performance of the first-order and second-order $\Sigma\Delta$ modulators. The motivation of this OTA-sharing reconfigurable amplifier is to save silicon area for the on-chip digital circuits, such as decimation filters, for a future design. The reconfigurable amplifier in system-level chopping mode and auto-zeroing mode is shown in Figure 5-21 and Figure 5-22, respectively.

**System-Level chopping mode**

As shown in Figure 5-21, the thermopile’s interface circuit is configured into system-level chopping mode to realize a second-order $\Sigma\Delta$ modulator. The switches which are controlled by clock $\phi_{AZ}$ and $\phi_{ST}$ are all open and the trans-conductor $g_{m2}$ stage is powered off. The inner chopped integrator consists of the trans-conductor $g_{m1}$, an integration capacitor $C$ and fast choppers $C_{H1}$ and $C_{H2}$. The fast choppers ($C_{H1}$ and $C_{H2}$) which are driven at the same frequency $f_s$ as quantizer’s sampling clock $\phi_{comp}$, can modulate the input-referred offset of $g_{m1}$ into AC component, which is then filtered out by the integration capacitor $C$. The residual offset of the inner chopped integrator can be further reduced by another pair of choppers ($C_{L1}$ and $C_{L2}$) driven at the much lower frequency $f_L$ ($f_L=f_s/4096$).
In the operating temperature range [-40°C, 50°C], the simulation results of the system-level chopped integrator in the final prototype show that it can still meet the requirements as shown in Table 5-2 but with halved residual offset. This indicates that the heater power consumption $P_{\text{ref}}$ of the final prototype is possible to be reduced by 2x compared to the first prototype.

### Table 5-6 Simulation results of the system-level chopping amplifier

<table>
<thead>
<tr>
<th>Parameters</th>
<th>Unit</th>
<th>Min.</th>
<th>Typ.</th>
<th>Max.</th>
<th>Note</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{\text{dd}}$</td>
<td>V</td>
<td>5</td>
<td></td>
<td></td>
<td>supply voltage</td>
</tr>
<tr>
<td>$f_H$</td>
<td>kHz</td>
<td>15.625</td>
<td></td>
<td></td>
<td>fast chopping freq.</td>
</tr>
<tr>
<td>$f_L$</td>
<td>Hz</td>
<td>3.81</td>
<td></td>
<td></td>
<td>slow chopping freq.</td>
</tr>
<tr>
<td>$C$</td>
<td>pF</td>
<td>130</td>
<td></td>
<td></td>
<td>integration cap</td>
</tr>
<tr>
<td>temp. range</td>
<td>°C</td>
<td>-40</td>
<td>20</td>
<td>50</td>
<td></td>
</tr>
<tr>
<td>band of interest</td>
<td>Hz</td>
<td>0</td>
<td>1</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

### Simulation results

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Unit</th>
<th>Min.</th>
<th>Typ.</th>
<th>Max.</th>
<th>Note</th>
</tr>
</thead>
<tbody>
<tr>
<td>$I_{\text{supply}}$</td>
<td>µA</td>
<td>3.5</td>
<td>4.5</td>
<td>5.3</td>
<td>circuit’s current consumption</td>
</tr>
<tr>
<td>$g_{m1}$</td>
<td>µS</td>
<td>20</td>
<td>22</td>
<td>23.2</td>
<td>trans-conductance</td>
</tr>
<tr>
<td>$f_{3\text{dB}}$</td>
<td>Hz</td>
<td>0.35</td>
<td>0.5</td>
<td>0.75</td>
<td>low-pass filter pole freq.</td>
</tr>
<tr>
<td>residual offset</td>
<td>µV</td>
<td>0.6</td>
<td>0.8</td>
<td>1</td>
<td>as compared to the first prototype (Table 5-3), the residual offset is about halved due to system-level chopping</td>
</tr>
<tr>
<td>residual in-band noise</td>
<td>nV/√Hz</td>
<td>14</td>
<td>17</td>
<td>22</td>
<td>should be smaller than the thermopile’s thermal noise density $\sqrt{V_{\text{th}}}$ = $\sqrt{4kTnR_{\text{th}}} = 52nV / \sqrt{\text{Hz}}$</td>
</tr>
</tbody>
</table>

![Figure 5-21 Reconfigurable Amplifier in the system-level chopping mode](image)
Auto-zeroing Mode

The reconfigurable interface circuit (Figure 5-20) can also be configured into auto-zeroing mode as shown in Figure 5-22. In auto-zeroing mode, the integration capacitor \( C \) is reused as the offset auto-zeroing capacitor and the chopper switches \( C_{L1}, C_{L2}, C_{H1}, C_{H2} \) and \( C_{C1} \) are not swapping. The timing diagram of the waveforms of the reconfigurable amplifier in auto-zeroing mode is illustrated in Figure 5-23.

Compared to the traditional auto-zeroing amplifier which is used in first prototype, a slow settling technique was applied to the existing auto-zeroing amplifier, to further reduce the residual input-referred noise [93]. The detailed timing diagram of the waveforms in the auto-zeroing amplifier with slow-settling technique is shown in Figure 5-23. The switches controlled by \( \phi_{ST} \) are opened a few nanoseconds before switches controlled by the \( \phi_{AZ} \) are closed. By doing this, the output of the auto-zeroing amplifier can firstly settle, with only the loading of the parasitic capacitor rather than with the loading of the large integration capacitor \( C \). When the voltage at the output of the \( g_m \) stage is almost settled, the capacitor \( C \) will then be connected by the \( \phi_{ST} \) switches.

Traditionally, during the auto-zeroing phase \( \phi_{AZ} \), the amplifier’s bandwidth \( f_{null} \), should be several times larger than the auto-zeroing frequency \( f_{AZ} \) (e.g., by a factor of 3~5), so as to allow the \( V_{cap} \) to fully settle within one auto-zeroing phase. As a result, the broadband noise is under-sampled on the auto-zeroing capacitor \( C \), and the residual input-referred noise PSD in the low frequency domain is approximately increased by the ratio of \( f_{null} \) and the sampling frequency \( f_{AZ} \) as illustrated in Figure 4-4. By employing this slow-settling technique, the bandwidth of the auto-zeroing amplifier \( f_{null} \) can be set to be smaller than the auto-zeroing frequency \( f_{AZ} \). As a consequence, the voltage across the
integration capacitor $V_{\text{cap}}$, will no longer settle within one auto-zeroing phase, but requires multiple cycles to settle. Since leakage of the capacitor's charge is almost negligible, the voltage across the capacitor will finally reach its stable value after several auto-zeroing cycles as shown in Figure 5-23. After the $V_{\text{cap}}$ settles, it will be refreshed in each auto-zeroing phase. Thus, $V_{\text{cap}}$ will be maintained always to cancel the offset current of the main amplifier. The advantage with this slow-settling $V_{\text{cap}}$ is that the foldback noise, can be reduced since the ratio $f_{\text{null}}/f_{\text{AZ}}$ can be smaller than one [92].

![Figure 5-23 Timing diagram of waveforms in reconfigurable amplifier in auto-zeroing mode](image-url)
5.3.4 Chip Micrograph

Compared to the first prototype’s layout (Figure 5-13), there are several improvements in the layout design of the final prototype design (Figure 5-24):

1. Bonding pads were placed symmetrically around the chip to reduce the thermal offset caused by heat loss through the bonding wires.

2. To minimize thermal crosstalk between the heaters and the circuitry, sensitive circuit such as the input pairs of the amplifier were located near the center of the chip, where the thermal gradient is the smallest.

3. The interface circuit can be re-configured into auto-zeroing or system-level chopping mode. Therefore, the circuit is more compact in terms of layout than the first prototype.

![Figure 5-24 Micrograph of the wind sensor chip (second prototype) [92]](image)

5.3.5 Measurement results

**Modulator performance**

The power spectral density of the sensor’s bit-stream outputs was measured with $P_{\text{ref}} = 12.5\text{mW}$ and $f_s=15.625 \text{kHz}$, at wind speeds of 0m/s and 25m/s (Figure 5-25). In order to show the noise spectrum more clearly, the slow choppers ($C_{L1}$ and $C_{L2}$ in Figure 5-21)
were disabled. In first-order mode, 11-bit resolution was achieved into a 1Hz bandwidth. In second-order mode, the resolution increases to about 13.5 bits. The output spectrum of the second-order $\Sigma\Delta$ modulator shows that the in-band noise (measured in still air, i.e. 0m/s), is comparable with the noise caused by wind turbulence or random air currents (at 25m/s). Thus, the $P_{\text{ref}}$ of 12.5mW is almost minimized heater power consumption because the thermal noise of thermopile itself already becomes the limiting factor of the resolution of the modulator. That means if the $P_{\text{ref}}$ is reduced to be less than 12.5mW, the resolution of modulator will start to decrease. The output spectrum exhibits a tone at fundamental frequency (about 30Hz) and its harmonics which can be notched out by the self-tracking $\text{sinc}^2$ filter which was introduced in section 3.4.6.

![Figure 5- 25 Measured output spectrum of the first-order and second-order $\Sigma\Delta$ modulators at wind speeds of 0m/s and 25m/s.](image)

**Wind Tunnel Measurement**

As shown in Figure 5- 26, the decimated outputs of the two orthogonal second-order $\Sigma\Delta$ modulators in final prototype are sinusoidal functions of wind direction, and the amplitudes are monotonic functions of wind speed. Figure 5- 27 shows the measured error of speed and direction as compared to a calibrated reference mechanical wind sensor. The sensor's measured error is less than ±4% (speed) and ±2° (direction), respectively, for wind speeds between 1 and 25 m/s. By using the system-level chopping integrator, the final prototype consumes 25mW, which is another 2x less than the first
proof-of-concept prototype while maintaining the sensing resolution, as compared to the first prototype.

Temperature Measurement

As shown in Figure 3-23, the second-order $T\Sigma\Delta$ modulators oscillates at a frequency $f_{\text{peak}}$ of about 20Hz. The period of this oscillation can be measured by counting the number of zero-crossings in the output of either of the two $T\Sigma\Delta$ modulators during an 8-
second period. As expected, the result is a near-linear function of temperature (Figure 5-28 a). The average characteristics of three sensors were fitted to a master curve (a 5th order polynomial), which was then used to convert the measured period into a temperature reading. The noise in the measurements corresponds to an estimated resolution of about ±0.15°C, while the deviations from the master curve correspond to an untrimmed error of less than ±1°C for temperatures ranging from -40°C to 50°C (Figure 5-28 b). Because this sensor dissipates only 25mW, or 2x less power than the first prototype, the self-heating of the chip is estimated to be only 0.5°C.

Figure 5-28 (a) Measured oscillation period versus temperature for three samples (b) Measured temperature error for three samples.
5.4 Benchmarks

Table 5-7 compares the performance of the sensors discussed in this chapter with several previous works. The final prototype described in section 5.3 achieves, to date, the lowest power consumption among the reported thermal wind sensors which are fabricated in standard CMOS process. It is also the first reported thermal CMOS sensor that can simultaneously measure wind velocity and ambient temperature. The literature [5] reported a thermal wind sensor which is fabricated with a ceramic substrate and MEMS process. It can achieve a measurable wind speed range of [0.5m/s, 40m/s] by using CTD mode and an external control/read-out circuit. Its constant temperature overheat is regulated to be 6°C, resulting in a power consumption of 2mW with zero wind speed and 112mW with its maximum measurable wind speed, i.e. 40m/s. Compared to the thermal wind sensor presented in [5], the main advantages of the work described in this thesis ([91, 92] are its robustness (due to the integration of sensor and interface circuit in the same chip) and low manufacturing cost (due to the standard CMOS fabrication process).
<table>
<thead>
<tr>
<th>Parameter</th>
<th>This work section 4.5[92]</th>
<th>This work section 4.4[91]</th>
<th>Kofi [35]</th>
<th>Dong [5]</th>
</tr>
</thead>
<tbody>
<tr>
<td>Publication Year</td>
<td>2011</td>
<td>2011</td>
<td>2002</td>
<td>2012</td>
</tr>
<tr>
<td>Technology</td>
<td>CMOS 0.7 μm</td>
<td>CMOS 0.7 μm</td>
<td>CMOS 1.6 μm</td>
<td>MEMS (ceramic substrate)</td>
</tr>
<tr>
<td>Chip area</td>
<td>4 × 4 mm²</td>
<td>4 × 4 mm²</td>
<td>4 × 4 mm²</td>
<td>6 × 6 mm²</td>
</tr>
<tr>
<td>Read-out circuit</td>
<td>On-chip</td>
<td>On-chip</td>
<td>On-chip</td>
<td>Off-chip (IA+ADC)</td>
</tr>
<tr>
<td>Operating mode</td>
<td>CP</td>
<td>CP</td>
<td>CTD</td>
<td>CTD</td>
</tr>
<tr>
<td>Overheat</td>
<td>dependent on wind speed</td>
<td>dependent on wind speed</td>
<td>10°C</td>
<td>6°C(min)</td>
</tr>
<tr>
<td>Wind speed range</td>
<td>1~25 m/s</td>
<td>1~25 m/s</td>
<td>1~25 m/s</td>
<td>0.5~40 m/s</td>
</tr>
<tr>
<td>Speed error</td>
<td>±4 %</td>
<td>±4 %</td>
<td>±5 %</td>
<td>±4 %</td>
</tr>
<tr>
<td>Direction error</td>
<td>±2°</td>
<td>±2°</td>
<td>±3°</td>
<td>±2°</td>
</tr>
<tr>
<td>Power consumption</td>
<td>25 mW</td>
<td>50 mW</td>
<td>450 mW</td>
<td>2mW(0m/s) 112mW(40m/s)</td>
</tr>
<tr>
<td>(with max. wind speed)</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Ambient temp. output</td>
<td>YES</td>
<td>NO</td>
<td>NO</td>
<td>NO</td>
</tr>
<tr>
<td>Temperature error</td>
<td>±1°C</td>
<td>NA</td>
<td>NA</td>
<td>NA</td>
</tr>
</tbody>
</table>
Chapter 6 Conclusions

In this thesis, the operating modes and interface electronics of a two-dimensional thermal CMOS wind sensor have been investigated and then improved to reduce its total power consumption. This chapter summarizes the main findings of this thesis and highlights the original contributions.

6.1 Main Findings

The following list summarizes the main findings of this thesis.

(1) Compared to the CTD mode, the operation of the thermal wind sensor in CP mode simplifies the system (the overheat regulation loop is not necessary for CP mode), and enables a reduction of the total heating power consumption which was previously limited by the inaccuracy of the on-chip/ambient NPN temperature sensors. (Chapter 2)

As shown in reference design [3], the sensor was operated in CTD mode such that the heating power consumption was limited by the sensing inaccuracy of the on-chip/ambient temperature sensors (section 2.2.1). In CP mode, the power consumption is accurately controlled by a duty-cycled signal so that the overheat regulation loop is not required any longer. (section 2.2.2).

(2) Unlike the electrical ΣΔ modulator, the in-band quantization noise of the TΣΔ modulator can only be reduced by about 3dB/oct by doubling the sampling frequency, mainly due to the noise spreading effect in frequency domain. (Chapter 3)

As shown in the output spectrum of TΣΔ modulator (Figure 3-23), a peak will occur at the frequency where the loop filter’s phase delay goes through -180°. In time domain, the quantizer input is dominated by a sine-wave at this peak frequency. If the sampling frequency is much faster than this peak frequency, this quantizer will behave as if it works asynchronously. As a result, to increase the sampling frequency which is already
much larger than the peak frequency will have little impact on the behavior of the $\Sigma\Delta$ modulator. (Section 3.3 and 3.4)

(3) Both the resolution and linearity of the $\Sigma\Delta$ modulator can be improved by augmenting the thermal filter with an electrical integrator. (Chapter 3)

The $\Sigma\Delta$ interface should be designed so that the in-band resolution is only limited by the thermopile’s thermal noise rather than the quantization noise. For the first-order system, the simulation shows its in-band resolution is limited by the quantization noise, because the noise shaping provided by the thermal loop filter is not sufficient (Section 3.3.2). By augmenting the thermal filter with an electrical integrator, the resulting second-order $\Sigma\Delta$ modulator will have more aggressive noise shaping than the first-order $\Sigma\Delta$ modulator. As a result, the in-band noise can reach its fundamental limit set by its thermopile’s thermal noise (Section 3.4.1). Due to the high in-band gain provided by the extra electrical integrator, linearity of the DC transfer function of the second-order system is also greatly improved. The second-order $\Sigma\Delta$ modulator can achieve 14-bit linearity in 80% of the input range while the first-order system can only achieve 9-bit with the same input range (Section 3.4.2).

(4) Though the second-order $\Sigma\Delta$ modulator oscillates at the frequency where the loop filter’s phase delay goes through -180°, the operation of this modulator is considered to be still stable. (Chapter 3)

In the output spectrum of the second-order $\Sigma\Delta$ modulator, there is a big peak tone at the frequency at which the loop filter’s phase delay goes through -180° (Figure 3-23). It seems that this closed-loop system is prone to be “unstable”. However, the simulation shows that both the thermal and electrical integrator outputs are bounded and the system can still convert the input into a digital reading with 14-bit resolution for the 80% of the input dynamic range. Therefore, the system is considered to be stable (Section 3.4.4).
(5) By measuring the peak tone frequency of second-order TΣΔ modulator, the ambient temperature can be measured because the phase shift of the thermal filter is a monotonic function of the temperature. (Chapter 3)

There is a strong peak tone in the second-order TΣΔ modulator’s output spectrum, whose frequency (~ 20Hz) corresponds to the frequency at which its loop filter has a phase shift of 180°. Since the integrator’s phase shift is designed to be almost exactly 90°, \( f_{\text{peak}} \) will be determined by the thermal filter’s phase-shift. Because the phase shift of the thermal filter is a monotonic function of the temperature, the peak frequency \( f_{\text{peak}} \) will be only determined by the temperature of the silicon substrate. Thus, the chip’s temperature can be determined by measuring this peak frequency. By applying the CP mode and second-order TΣΔ modulator, the required power consumption can be less than 50mW and the sensor’s self-heating is estimated to be less than 1 °C. This will make the temperature of the silicon chip a very close approximation to the ambient temperature (Section 3.4.5).

(6) The thermopile’s interface circuit can be implemented with a chopper amplifier, to achieve smaller residual input-referred offset and in-band noise than an auto-zeroing amplifier which was used in the reference design [3]. (Chapter 4)

6.2 Original Contributions

The following list provides an overview of the main original contributions presented in this thesis. References to this thesis or to publications have been included.

(1) Development of the quasi-linear model of the TΣΔ modulator, which allows the analysis of in-band noise contribution of the quantization noise and thermal noise separately. (Section 3.2)

(2) Detailed analysis of the impact of the sampling frequency’s increase on the residual in-band quantization noise of the TΣΔ modulator. (Section 3.3 & 3.4)
(3) Invention of the second-order $\Sigma\Delta$ modulator, which can achieve a more aggressive quantization noise shaping than its first-order counterpart. (Section 3.4) [91]

(4) Detailed analysis of the stability of the second-order $\Sigma\Delta$ loop. (Section 3.4.4)

(5) Development of the ambient temperature sensor based on the second-order $\Sigma\Delta$ modulator, by measuring its oscillation frequency, which is a monotonic function of the chip’s temperature. (Section 3.4.5) [92]

(6) Development of a self-tracking sinc2 decimation filter, which can dynamically place zeros exactly at the second-order $\Sigma\Delta$ modulator’s oscillation frequency and its harmonics. (Section 3.4.6) [91]

(7) Development of a low-offset interface circuit that can combine an auto-zeroing amplifier and a chopper integrator with shared OTA and capacitor. (Section 5.3) [92]

6.3 Future works

The following topics could be interesting to address in the future work on CMOS thermal wind sensors.

(1) Development of the sensor chip with ultra-thin silicon wafer.

In this work, the silicon wafer was 6 inch and its thickness is 675 µm. In future works, ultra-thin wafers (250~100 µm) can be used instead. Due to the smaller thermal capacity of the chip, the transient response of the sensor will be faster. Furthermore, because the thermal conductance between the wind flow and the sensor becomes larger, better sensitivity can be achieved.

(2) Integration of the digital interface circuit in the same chip.
As shown in Figure 5-24, the compact layout design of the $\Sigma\Delta$ interface circuit enables the integration of other functional blocks, such as a digital interface circuit. The main advantages of the fully integrated thermal wind sensor are improved robustness and lower BOM (bill of materials) cost.

(3) Investigation of the sensor’s calibration system by using laser.

In this work, the sensor is calibrated in the wind tunnel with three different wind speeds. The major manufacturing cost of the thermal wind sensor is due to its calibration process. This cost can be reduced by using the laser calibration technique. A laser can make a moving hot spot on top of the thermal sensor. This hot spot can cause a similar thermal unbalance effect as is induced by the wind flow. Thus, it is possible to calibrate the sensor with only the laser. As a result, both the calibration time and cost for each sensor can be reduced.
Reference


