Circuit Design
with
Metallic Single-Electron Tunnel Junctions

R.H. Klunder
Propositions belonging to the thesis:

Circuit Design with Metallic Single-Electron Tunnel Junctions

Roelof H. Klunder

1. Modelling a SET junction by a resistor limits the design of circuits based on single-electron tunnel behaviour (chapter 2 and 3).

2. When a physical SET-circuit is modelled by electronic network components, the tunnel capacitance in the model should be extended with a dissipating element to obtain energy conservation, for example a current source or (when time is not important) a resistor (chapter 3).

3. A maximal voltage amplification in a circuit built with SET junctions is obtained when using circuits based on single-electron tunnel effects, which are not limited to global tunnel currents (chapter 5).

4. A top-down design approach without a direct translation from a system to a circuit concept will always result in an analysis instead of a synthesis (chapter 8).

5. A SET-transistor is not an example of a single-electron electronics component, due to the fact that outside the Coulomb blockade more than one electron tunnels (chapter 9).

6. The nano-character of a nano-system is lost when many nano-systems are coupled (chapter 11).

7. Black and white photography is (almost) not usable; this type of photography should be called grey-scale photography.

8. Internet is no competition for television and radio as long as it is not capable of supplying information to a large group of people at the same time.

9. Due to humanity and economic reasons only class-C amplifiers of maximal 1 Watt should be sold in Arabic countries and India.

10. Due to the road signs on the motorway people will lose their feeling of the geographic positions of cities in the future.

11. The outside of the refrigerator is only made of metal because of the extra accessories, like refrigerator magnets.

12. Only people who are separating their garbage have ‘rest-garbage’.

13. Enter is the most commonly used password.

14. The only one who reads a whole thesis is the spelling checker of the computer.

These propositions are considered defendable and as such have been approved by the supervisor Prof.dr.ir. P.M. Dewilde.
Stellingen behorende bij het proefschrift:

Circuit Design with Metallic Single-Electron Tunnel Junctions

Roelof H. Klunder

1. Modellering van een SET junctie door middel van een weerstand beperkt het ontwerpen van circuits gebaseerd op enkel-elektron tunnel gedrag (hoofdstuk 2 en 3).

2. Wanneer een fysisch SET-circuit met behulp van elektronische netwerk componenten wordt gemodelleerd, zal de tunnelcapaciteit in het netwerkmodel ten gevolge van energiebehoor moeten worden uitgebreid met een dissiperend element, bijvoorbeeld een stroombron of (als tijd niet belangrijk is) een weerstand (hoofdstuk 3).

3. Een maximale spanningsverstrekking in een circuit met SET juncties wordt verkregen bij schakelingen die een enkel-elektron tunnel effect gebruiken, en zich niet beperken tot globale stromen ten gevolge van tunnelen (hoofdstuk 5).

4. Een top-down design methode zonder een directe vertaling van systeem- naar circuit-concept zal altijd uiteinden op een analyse in plaats van een synthese (hoofdstuk 8).

5. Een SET-transistor is geen voorbeeld van een single-elektron elektronica component, omdat er buiten de Coulomb blokkade meer elektronen tunnelen (hoofdstuk 9).

6. Het nano-karakter van een nanoschakeling gaat verloren als meer nanoschakelingen aan elkaar worden gekoppeld (hoofdstuk 11).

7. Zwart-wit fotografie is onzinnig en (vrijwel) onbruikbaar; deze vorm van fotografie dient grijstinten fotografie genoemd te worden.

8. Internet is geen concurrentie van TV en radio zolang het niet in staat is grote groepen mensen gelijktijdig van informatie te voorzien.

9. Zowel vanwege humanitaire redenen als vanwege economische redenen moeten in Arabische landen en India klasse-C versterkers van maximaal 1 Watt verkocht worden.

10. Door de wegwijzers langs de snelwegen zal de mens in de toekomst het gevoel van geografische liggingen van plaatsen verliezen.

11. De buitenkant van koelkasten zijn alleen van metaal gemaakt vanwege de extra accessoires, zoals koelkastmagneetjes.

12. Alleen personen die aan afvalafscheiding doen, hebben 'rest-afval'.

13. Enter is het meest gebruikte wachtwoord.

14. De enige die een proefschrift echt helemaal doorwerkt is de spellingschecker op de computer.

Deze stellingen worden verdedigbaar geacht en zijn als zodanig goedgekeurd door de promotor Prof.dr.ir. P.M. Dewilde.
Circuit Design with Metallic Single-Electron Tunnel Junctions
Circuit Design with Metallic Single-Electron Tunnel Junctions

Proefschrift

ter verkrijging van de graad van doctor
aan de Technische Universiteit Delft,
op gezag van de Rector Magnificus prof.dr.ir. J.T. Fokkema,
voorzitter van het College voor Promoties,
in het openbaar te verdedigen op maandag 13 januari 2003 om 10:30 uur

door

Roelof Harm KLUNDER

elektrotechnisch ingenieur
geboren te Delft.
This work was supported by the European Mel-ari/NID "ANSWERS" project.

Cover: Honeybee photo by A.H. de Wilde, placed on a simulation result of the SET circuit of figure 9.42.

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Index of symbols

To prevent problems with the symbols we use:

- \( t \) for a point in time and \( \tau \) for a time span
- \( T \) for temperature, \( \tau_p \) for a (time) period, and \( T \) for the transmission coefficient
- \( e \) for elementary charge and \( \exp \) for base of the natural logarithm

The step function:

\[
\begin{align*}
\epsilon(t - t_0) &= 0 & t < t_0 \\
\epsilon(t - t_0) &= [0..1] & t = t_0 \\
\epsilon(t - t_0) &= 1 & t > t_0
\end{align*}
\]  

(1)

The delta function:

\[
\epsilon(t - t_0) = \int_{-\infty}^{t} \delta(\tau - t_0)d\tau \quad \forall t
\]

(2)

### Constants

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Meaning</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>( c )</td>
<td>The speed of light, ( c = 2.9979246 \cdot 10^8 \text{ [m/s]} )</td>
<td>m/s</td>
</tr>
<tr>
<td>( e )</td>
<td>The elementary charge, ( e = 1.602177 \cdot 10^{-19} \text{ [C]} ). The charge of a single electron is ( q_e = -e[C] )</td>
<td>C</td>
</tr>
<tr>
<td>( \exp )</td>
<td>The base of natural logarithm ( \exp(1) = 2.7182818 )</td>
<td></td>
</tr>
<tr>
<td>( h )</td>
<td>Planck’s constant, ( h = 6.6260755 \cdot 10^{-34} \text{ [Js]} )</td>
<td>Js</td>
</tr>
<tr>
<td>( h )</td>
<td>( \frac{h}{2\pi} = 1.05459 \cdot 10^{-27} \text{ [Js]} )</td>
<td>Js</td>
</tr>
<tr>
<td>( j )</td>
<td>The imaginary unit ( j = \sqrt{-1} )</td>
<td></td>
</tr>
<tr>
<td>( k_B )</td>
<td>Boltzmann’s constant: ( k_B = 1.380658 \cdot 10^{-23} \text{ [J/K]} )</td>
<td>J/K</td>
</tr>
<tr>
<td>( R_k, R_q )</td>
<td>The quantum resistance ( R_k = \frac{h}{2e^2} = 25.8 \text{ k\Omega} )</td>
<td>( \Omega )</td>
</tr>
</tbody>
</table>

\( \Re\{\cdot\} \) is the real part. So \( \Re\{a + jb\} = a \).

### General

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Meaning</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>( \alpha(t) )</td>
<td>The impulse response of a voltage between two nodes due to a voltage excitation elsewhere in the circuit</td>
<td></td>
</tr>
<tr>
<td>Symbol</td>
<td>Description</td>
<td>Unit</td>
</tr>
<tr>
<td>--------</td>
<td>-----------------------------------------------------------------------------</td>
<td>-------</td>
</tr>
<tr>
<td>$A(s)$</td>
<td>The Laplace transform of $\alpha(t)$</td>
<td></td>
</tr>
<tr>
<td>$\beta(t)$</td>
<td>The impulse response of a voltage between two nodes due to a current excitation elsewhere in the circuit</td>
<td></td>
</tr>
<tr>
<td>$B(s)$</td>
<td>The Laplace transform of $\beta(t)$</td>
<td></td>
</tr>
<tr>
<td>$\Gamma$</td>
<td>A tunnel rate</td>
<td>$\Omega$</td>
</tr>
<tr>
<td>$\delta$</td>
<td>The delta of dirac function</td>
<td>$1/s$</td>
</tr>
<tr>
<td>$\epsilon$</td>
<td>The step function</td>
<td></td>
</tr>
<tr>
<td>$\zeta$</td>
<td>A signal</td>
<td></td>
</tr>
<tr>
<td>$\Delta\zeta$</td>
<td>The difference between the maximal and minimal amplitude of the signal values</td>
<td></td>
</tr>
<tr>
<td>$\tilde{\zeta}$</td>
<td>A signal over a restricted interval</td>
<td></td>
</tr>
<tr>
<td>$\Delta\tilde{\zeta}$</td>
<td>The difference between the maximal and minimal amplitude of the information signal</td>
<td></td>
</tr>
<tr>
<td>$\theta$</td>
<td>A phase difference</td>
<td>$\text{rad}$</td>
</tr>
<tr>
<td>$\theta$</td>
<td>A vector of the used physical quantities</td>
<td>$\text{m}$</td>
</tr>
<tr>
<td>$\lambda$</td>
<td>A wavelength</td>
<td>$\text{V/Wb}$</td>
</tr>
<tr>
<td>$\xi(t)$</td>
<td>The relation between an independent flux and the voltage between two nodes</td>
<td></td>
</tr>
<tr>
<td>$\Xi(s)$</td>
<td>The Laplace transform of $\xi(t)$</td>
<td>$\text{V/Wb}$</td>
</tr>
<tr>
<td>$\rho$</td>
<td>A period</td>
<td></td>
</tr>
<tr>
<td>$\sigma$</td>
<td>A situation</td>
<td></td>
</tr>
<tr>
<td>$\varsigma$</td>
<td>A switch</td>
<td></td>
</tr>
<tr>
<td>$\tau$</td>
<td>A time span</td>
<td>$s$</td>
</tr>
<tr>
<td>$\tilde{\tau}$</td>
<td>An average time span</td>
<td>$s$</td>
</tr>
<tr>
<td>$\phi(t)$</td>
<td>A magnetic flux</td>
<td>$\text{Wb}$</td>
</tr>
<tr>
<td>$\Phi(s)$</td>
<td>The Laplace transform of $\phi(t)$</td>
<td>$\text{Wb}$</td>
</tr>
<tr>
<td>$\varphi$</td>
<td>The angle between the horizontal axis and the slope of the input-output relation</td>
<td>$\text{rad}$</td>
</tr>
<tr>
<td>$\psi(t)$</td>
<td>The impulse response of a voltage between two nodes due to an independent charge elsewhere in the circuit</td>
<td>$\Omega/s$</td>
</tr>
<tr>
<td>$\Psi(s)$</td>
<td>The Laplace transform of $\psi(t)$</td>
<td>$\Omega/s$</td>
</tr>
<tr>
<td>$\omega$</td>
<td>The radian frequency $\omega = 2\pi f$</td>
<td>$\text{rad/s}$</td>
</tr>
<tr>
<td>$a$</td>
<td>A constant, integer number, $a \in \mathbb{Z}$</td>
<td></td>
</tr>
<tr>
<td>$A$</td>
<td>An amplification</td>
<td></td>
</tr>
<tr>
<td>$A_r$</td>
<td>An area</td>
<td></td>
</tr>
<tr>
<td>$b$</td>
<td>A constant, integer number, $b \in \mathbb{Z}$</td>
<td></td>
</tr>
<tr>
<td>$B$</td>
<td>The transmission matrix of a coupling block</td>
<td></td>
</tr>
<tr>
<td>$C$</td>
<td>A capacitance (see figure 1a for the circuit symbol)</td>
<td>$\text{F}$</td>
</tr>
<tr>
<td>$d$</td>
<td>An integer number used for summations, $d \in \mathbb{N}$</td>
<td></td>
</tr>
<tr>
<td>$D$</td>
<td>The density of states</td>
<td></td>
</tr>
<tr>
<td>$E$</td>
<td>An energy</td>
<td>$\text{J}$</td>
</tr>
<tr>
<td>$f$</td>
<td>A frequency $f = \frac{1}{\tau_p}$</td>
<td>$\text{Hz}$</td>
</tr>
<tr>
<td>$F$</td>
<td>The function of a (sub-)circuit</td>
<td></td>
</tr>
<tr>
<td>$g$</td>
<td>A function</td>
<td></td>
</tr>
<tr>
<td>$G$</td>
<td>A conductance $1/R$</td>
<td>$\text{S}$</td>
</tr>
<tr>
<td>$H$</td>
<td>An input-output relation</td>
<td></td>
</tr>
<tr>
<td>$H^*$</td>
<td>An input-output relation shifted by the bias sources</td>
<td></td>
</tr>
<tr>
<td>Symbol</td>
<td>Definition</td>
<td></td>
</tr>
<tr>
<td>--------</td>
<td>------------</td>
<td></td>
</tr>
<tr>
<td>H</td>
<td>The matrix of all possible input-output relations</td>
<td></td>
</tr>
<tr>
<td>i(t)</td>
<td>A current (see figure 1e for the circuit symbol)</td>
<td></td>
</tr>
<tr>
<td>I(s)</td>
<td>The Laplace transform of i(t)</td>
<td></td>
</tr>
<tr>
<td>J</td>
<td>The inverse of K, J = K^{-1}</td>
<td></td>
</tr>
<tr>
<td>JJ</td>
<td>A Josephson junction</td>
<td></td>
</tr>
<tr>
<td>k</td>
<td>An integer number k ∈ N</td>
<td></td>
</tr>
<tr>
<td>K</td>
<td>The transmission matrix of a function block</td>
<td></td>
</tr>
<tr>
<td>K</td>
<td>The equilibrium phase correlation function</td>
<td></td>
</tr>
<tr>
<td>l</td>
<td>The function to indicate the shape of the tunnel current</td>
<td></td>
</tr>
<tr>
<td>L</td>
<td>An inductance</td>
<td></td>
</tr>
<tr>
<td>Ł</td>
<td>The Laplace operator</td>
<td></td>
</tr>
<tr>
<td>M</td>
<td>The product of prime modulo numbers</td>
<td></td>
</tr>
<tr>
<td>m</td>
<td>A (prime) modulo number</td>
<td></td>
</tr>
<tr>
<td>М</td>
<td>The ratio between the product of the prime modulo numbers and a prime modulo number</td>
<td></td>
</tr>
<tr>
<td>n</td>
<td>The number of electrons</td>
<td></td>
</tr>
<tr>
<td>N</td>
<td>A constant</td>
<td></td>
</tr>
<tr>
<td>p</td>
<td>The poles of the input-output relation</td>
<td></td>
</tr>
<tr>
<td>P</td>
<td>A power</td>
<td></td>
</tr>
<tr>
<td>P(E)</td>
<td>The change that the electron will exchange energy E with its environment</td>
<td></td>
</tr>
<tr>
<td>q(t)</td>
<td>A charge</td>
<td></td>
</tr>
<tr>
<td>Q(s)</td>
<td>The Laplace transform of q(t)</td>
<td></td>
</tr>
<tr>
<td>r</td>
<td>The residue of a modulo function</td>
<td></td>
</tr>
<tr>
<td>R</td>
<td>A resistance (see figure 1c for the circuit symbol)</td>
<td></td>
</tr>
<tr>
<td>R</td>
<td>The ratio between impedances</td>
<td></td>
</tr>
<tr>
<td>s</td>
<td>The Laplace operator s = jω</td>
<td></td>
</tr>
<tr>
<td>S</td>
<td>A source, current or voltage</td>
<td></td>
</tr>
<tr>
<td>t</td>
<td>A point in time</td>
<td></td>
</tr>
<tr>
<td>T</td>
<td>A temperature</td>
<td></td>
</tr>
<tr>
<td>TJ</td>
<td>A SET junction (see figure 1b)</td>
<td></td>
</tr>
<tr>
<td>T</td>
<td>The transmission coefficient</td>
<td></td>
</tr>
<tr>
<td>u(t)</td>
<td>A potential difference or voltage source (see figure 1d for the circuit symbol of the voltage source)</td>
<td></td>
</tr>
<tr>
<td>Δu</td>
<td>A voltage difference between two voltages</td>
<td></td>
</tr>
<tr>
<td>U(t)</td>
<td>∫ u(t)dt</td>
<td></td>
</tr>
<tr>
<td>U(s)</td>
<td>The Laplace transform of u(t)</td>
<td></td>
</tr>
<tr>
<td>v(t)</td>
<td>A potential</td>
<td></td>
</tr>
<tr>
<td>V(s)</td>
<td>The Laplace transform of v(t)</td>
<td></td>
</tr>
<tr>
<td>w</td>
<td>A floating node (island)</td>
<td></td>
</tr>
<tr>
<td>x</td>
<td>A variable</td>
<td></td>
</tr>
<tr>
<td>X</td>
<td>A constant</td>
<td></td>
</tr>
<tr>
<td>Y(s)</td>
<td>An admittance</td>
<td></td>
</tr>
<tr>
<td>z</td>
<td>The zeros of the input-output relation</td>
<td></td>
</tr>
<tr>
<td>Z(s)</td>
<td>An impedance</td>
<td></td>
</tr>
</tbody>
</table>
Figure 1: The symbols used in this thesis, for some of the circuit elements. b) The symbol of the SET junction TJ according to the “Saclay notation” [7].

### Specials

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Meaning</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>$\beta_n$</td>
<td>The relation between the tunnel current $i$, and the voltage drop due to a tunnel event</td>
<td>$\Omega$</td>
</tr>
<tr>
<td>$B_n$</td>
<td>The Laplace transform of $\beta_n</td>
<td>$\Omega$</td>
</tr>
<tr>
<td>$\Gamma$</td>
<td>The tunnel rate from the positive to the negative side of the junction</td>
<td>1/s</td>
</tr>
<tr>
<td>$\overline{\Gamma}$</td>
<td>The tunnel rate from the negative to the positive side of the junction</td>
<td>1/s</td>
</tr>
<tr>
<td>$\zeta_A, \zeta_B$</td>
<td>A binary logic signal (0,1)</td>
<td></td>
</tr>
<tr>
<td>$\zeta_{b,h}$</td>
<td>The bias signal to obtain a horizontal shift in the input-output relation</td>
<td></td>
</tr>
<tr>
<td>$\zeta_{bias}$</td>
<td>The bias signal</td>
<td></td>
</tr>
<tr>
<td>$\zeta_c$</td>
<td>The output signal due to all the sources in the circuit, except the current source modelling the charge on the island under investigation, and the input voltage source capacitively coupled to the same island.</td>
<td></td>
</tr>
<tr>
<td>$\zeta_h$</td>
<td>The extra applied signal to shift the input-output relation horizontal</td>
<td></td>
</tr>
<tr>
<td>$\zeta_{hi}$</td>
<td>The input signal of the designed sub-circuit</td>
<td></td>
</tr>
<tr>
<td>$\zeta_{ho}$</td>
<td>The output signal of the designed sub-circuit</td>
<td></td>
</tr>
<tr>
<td>$\zeta_i$</td>
<td>An input signal</td>
<td></td>
</tr>
<tr>
<td>$\tilde{\zeta}_i$</td>
<td>The inverted version of $\zeta_i$</td>
<td></td>
</tr>
<tr>
<td>$\tilde{\zeta}_{in}$</td>
<td>The used input signal</td>
<td></td>
</tr>
<tr>
<td>$\Delta\zeta_{in}$</td>
<td>The difference between the maximal and minimal amplitude of the input signal that can be processed correctly</td>
<td></td>
</tr>
<tr>
<td>Symbol</td>
<td>Description</td>
<td></td>
</tr>
<tr>
<td>--------</td>
<td>-------------</td>
<td></td>
</tr>
<tr>
<td>$\Delta \tilde{c}_{in}$</td>
<td>The difference between the maximal and minimal amplitude of the input signals that is used for the information</td>
<td></td>
</tr>
<tr>
<td>$\tilde{c}_{max}$</td>
<td>The maximal amplitude of the input information signal</td>
<td></td>
</tr>
<tr>
<td>$\tilde{c}_{min}$</td>
<td>The minimal amplitude of the input information signal</td>
<td></td>
</tr>
<tr>
<td>$\tilde{c}_{in}$</td>
<td>The “begin” signal of the operating window</td>
<td></td>
</tr>
<tr>
<td>$c_o$</td>
<td>An output signal</td>
<td></td>
</tr>
<tr>
<td>$\tilde{c}_{out}$</td>
<td>The amplitude of the output signal</td>
<td></td>
</tr>
<tr>
<td>$\Delta \tilde{c}_{out}$</td>
<td>The difference between the maximal and minimal amplitude of the output signals that is used for the information</td>
<td></td>
</tr>
<tr>
<td>$\zeta_r$</td>
<td>The rest or residue signal</td>
<td></td>
</tr>
<tr>
<td>$\zeta_T$</td>
<td>A thresholded signal</td>
<td></td>
</tr>
<tr>
<td>$\zeta_v$</td>
<td>The extra applied signal to shift the input-output relation vertically</td>
<td></td>
</tr>
<tr>
<td>$\theta_e$</td>
<td>An extra undesired shift</td>
<td></td>
</tr>
<tr>
<td>$\theta_{hi}$</td>
<td>The physical quantity vector applied to a sub-circuit</td>
<td></td>
</tr>
<tr>
<td>$\theta_{ho}$</td>
<td>The physical quantity vector of the output of a designed sub-circuit</td>
<td></td>
</tr>
<tr>
<td>$\theta_{in}$</td>
<td>The physical quantity vector applied to a sub-system</td>
<td></td>
</tr>
<tr>
<td>$\theta_{out}$</td>
<td>The physical quantity vector of the output of a sub-system</td>
<td></td>
</tr>
<tr>
<td>$\tau_{cl}$</td>
<td>The period of a clock cycle $\tau_{cl} = 1/f_{cl}$</td>
<td></td>
</tr>
<tr>
<td>$\tau_{cyc}$</td>
<td>The total time span of the electron pump to pump in both directions</td>
<td></td>
</tr>
<tr>
<td>$\tau_d$</td>
<td>A dead-time</td>
<td></td>
</tr>
<tr>
<td>$\tau_g$</td>
<td>The period of the signal applied to the gate</td>
<td></td>
</tr>
<tr>
<td>$\tau_p$</td>
<td>A period time</td>
<td></td>
</tr>
<tr>
<td>$\tau_t$</td>
<td>The barrier traversal time, also called the tunnel time, $t_a - t_b$</td>
<td></td>
</tr>
<tr>
<td>$\tau_w$</td>
<td>The dwell time or wait time, the time span between $t^{cr}$ and $t_b$</td>
<td></td>
</tr>
<tr>
<td>$\bar{\tau}_w$</td>
<td>The average wait time</td>
<td></td>
</tr>
<tr>
<td>$\bar{\tau}_{wt}$</td>
<td>The total average time to transport one electron through the whole structure</td>
<td></td>
</tr>
<tr>
<td>$\omega_0$</td>
<td>A circuit constant, $\omega_0 = \frac{E_s}{h} = \frac{\pi}{R_k C_j}$</td>
<td></td>
</tr>
<tr>
<td>$A_i$</td>
<td>A current amplification</td>
<td></td>
</tr>
<tr>
<td>$A_q$</td>
<td>A charge amplification</td>
<td></td>
</tr>
<tr>
<td>$A_u$</td>
<td>A voltage amplification</td>
<td></td>
</tr>
<tr>
<td>$B_w$</td>
<td>The bandwidth</td>
<td></td>
</tr>
<tr>
<td>$B_i$</td>
<td>The transmission matrix of the input coupling block</td>
<td></td>
</tr>
<tr>
<td>$B_o$</td>
<td>The transmission matrix of the output coupling block</td>
<td></td>
</tr>
<tr>
<td>$C_1, C_2$</td>
<td>The capacitance of a non-tunneling capacitors</td>
<td></td>
</tr>
<tr>
<td>$C_\Sigma$</td>
<td>The sum of all capacitances connected/seen from a node</td>
<td></td>
</tr>
<tr>
<td>$C_b$</td>
<td>The capacitance of a non-tunneling capacitor to connect a bias voltage source</td>
<td></td>
</tr>
<tr>
<td>$C_{bc}$</td>
<td>The capacitor connecting the bias voltage source $u_{bc}$ with the island</td>
<td></td>
</tr>
<tr>
<td>$C_{bs}$</td>
<td>The capacitor connecting the bias voltage source $u_{bs}$ with the island</td>
<td></td>
</tr>
<tr>
<td>Symbol</td>
<td>Description</td>
<td></td>
</tr>
<tr>
<td>--------</td>
<td>-------------</td>
<td></td>
</tr>
<tr>
<td>$C_{bi}$</td>
<td>The capacitor connecting the bias voltage source $u_{bi}$ with the island</td>
<td></td>
</tr>
<tr>
<td>$C_c$</td>
<td>The capacitance of a non-tunneling capacitor</td>
<td></td>
</tr>
<tr>
<td>$C_{co}$</td>
<td>A couple capacitor</td>
<td></td>
</tr>
<tr>
<td>$C_{cr}$</td>
<td>A cross capacitance</td>
<td></td>
</tr>
<tr>
<td>$C_e$</td>
<td>The capacitive environment of the SET junction of a capacitive circuit, $Z_e = \frac{1}{\omega C_e}$</td>
<td></td>
</tr>
<tr>
<td>$C_{eff}$</td>
<td>The effective capacitance seen between the two nodes of a capacitive circuit, at which the junction is connected, $C_{eff} = C_e + C_j$</td>
<td></td>
</tr>
<tr>
<td>$C_g$</td>
<td>The gate capacitor</td>
<td></td>
</tr>
<tr>
<td>$C_{gL}$</td>
<td>The load capacitor connected to the gate</td>
<td></td>
</tr>
<tr>
<td>$C_i$</td>
<td>The island-to-substrate capacitance</td>
<td></td>
</tr>
<tr>
<td>$C_{in}$</td>
<td>A non-tunneling capacitor to connect the input voltage source</td>
<td></td>
</tr>
<tr>
<td>$C_j$</td>
<td>The junction capacitance</td>
<td></td>
</tr>
<tr>
<td>$C_L$</td>
<td>A load capacitance</td>
<td></td>
</tr>
<tr>
<td>$C_{L,in}$</td>
<td>The capacitance of the input source</td>
<td></td>
</tr>
<tr>
<td>$C_{max}$</td>
<td>The maximal capacitance of the components used</td>
<td></td>
</tr>
<tr>
<td>$C_R$</td>
<td>The capacitance of SET junction $TJ_R$, to couple the bias voltage source</td>
<td></td>
</tr>
<tr>
<td>$C_{su}$</td>
<td>The capacitance to the substrate</td>
<td></td>
</tr>
<tr>
<td>$C_{th}$</td>
<td>The Thévenin capacitance</td>
<td></td>
</tr>
<tr>
<td>$C_w$</td>
<td>The capacitance due to connected wires and filters</td>
<td></td>
</tr>
<tr>
<td>$D_f$</td>
<td>The density of states on the final side</td>
<td></td>
</tr>
<tr>
<td>$D_i$</td>
<td>The density of the states on the initial side</td>
<td></td>
</tr>
<tr>
<td>$E_a$</td>
<td>The energy of the circuit after a tunnel event $E_a = E(t_a)$</td>
<td></td>
</tr>
<tr>
<td>$E_b$</td>
<td>The energy of the circuit before a tunnel event $E_b = E(t_b)$</td>
<td></td>
</tr>
<tr>
<td>$E_c$</td>
<td>A circuit constant, $E_c = \frac{e^2}{2C_j}$</td>
<td></td>
</tr>
<tr>
<td>$E_{cs}$</td>
<td>The energy of a current source</td>
<td></td>
</tr>
<tr>
<td>$\Delta E_{cs}$</td>
<td>The energy difference of a current source due to a tunnel event</td>
<td></td>
</tr>
<tr>
<td>$\Delta E_i$</td>
<td>The energy difference of the current source, which models the tunnel event</td>
<td></td>
</tr>
<tr>
<td>$E_j$</td>
<td>The energy of the junction</td>
<td></td>
</tr>
<tr>
<td>$\Delta E_j$</td>
<td>The energy difference of the junction</td>
<td></td>
</tr>
<tr>
<td>$E_{ja}$</td>
<td>The energy of the junction just after the tunnel event $E_{ja} = E_j(t_a)$</td>
<td></td>
</tr>
<tr>
<td>$E_{jb}$</td>
<td>The energy of the junction just before the tunnel event $E_{jb} = E_j(t_b)$</td>
<td></td>
</tr>
<tr>
<td>$E_R$</td>
<td>The energy dissipated in a resistor</td>
<td></td>
</tr>
<tr>
<td>$\Delta E_R$</td>
<td>The difference of the energy of a resistor due to a tunnel event</td>
<td></td>
</tr>
<tr>
<td>$\Delta E_s$</td>
<td>The energy delivered by a voltage source $u_s$ between two moments in time</td>
<td></td>
</tr>
<tr>
<td>$\Delta E_{sa}$</td>
<td>The difference in the energy stored on the capacitors and junctions</td>
<td></td>
</tr>
<tr>
<td>Symbol</td>
<td>Description</td>
<td>Unit</td>
</tr>
<tr>
<td>------------</td>
<td>------------------------------------------------------------------------------------------------</td>
<td>--------</td>
</tr>
<tr>
<td>$\Delta E_{tot}$</td>
<td>The total charge in energy in the circuit</td>
<td>J</td>
</tr>
<tr>
<td>$\Delta E_x$</td>
<td>The energy difference of one or more components between two moments in time</td>
<td>J</td>
</tr>
<tr>
<td>$f_{cl}$</td>
<td>The applied clock frequency</td>
<td>Hz</td>
</tr>
<tr>
<td>$f_g$</td>
<td>The frequency of the applied gate signal</td>
<td>Hz</td>
</tr>
<tr>
<td>$f_t$</td>
<td>The noise corner frequency</td>
<td>Hz</td>
</tr>
<tr>
<td>$H_c$</td>
<td>The critical value of the magnetic field</td>
<td>A/m</td>
</tr>
<tr>
<td>$H_{ui}$</td>
<td>The input current - output current relation</td>
<td>Ω</td>
</tr>
<tr>
<td>$H_{uu}$</td>
<td>The input current - output voltage relation</td>
<td>S</td>
</tr>
<tr>
<td>$H_{ui}$</td>
<td>The input voltage - output current relation</td>
<td>A</td>
</tr>
<tr>
<td>$H_{uu}$</td>
<td>The input voltage - output voltage relation</td>
<td>A</td>
</tr>
<tr>
<td>$i_{bgc}$</td>
<td>The current modelling the background charge changes</td>
<td>A</td>
</tr>
<tr>
<td>$i_{b,h}$</td>
<td>A bias current source to achieve a horizontal shift in the input-output relation</td>
<td>A</td>
</tr>
<tr>
<td>$i_{bias}$</td>
<td>A bias current source</td>
<td>A</td>
</tr>
<tr>
<td>$i_{b,v}$</td>
<td>A bias current source to achieve a vertical shift in the input-output relation</td>
<td>A</td>
</tr>
<tr>
<td>$i_{b,vc}$</td>
<td>A bias current source (not connected to the output) to achieve a vertical shift in the input-output relation</td>
<td>A</td>
</tr>
<tr>
<td>$i_c$</td>
<td>The dielectric current through a non-tunneling capacitor</td>
<td>A</td>
</tr>
<tr>
<td>$i_{cj}$</td>
<td>The dielectric current through the insulator of a non-tunneling SET junction</td>
<td>A</td>
</tr>
<tr>
<td>$i_{cs}, i_s$</td>
<td>The current delivered by a current source</td>
<td>A</td>
</tr>
<tr>
<td>$I_{con}$</td>
<td>A constant current</td>
<td>A</td>
</tr>
<tr>
<td>$i_d$</td>
<td>The bias current source connected between drain and source of a SET transistor</td>
<td>A</td>
</tr>
<tr>
<td>$i_{d1}, i_{d2}$</td>
<td>The Norton equivalent current source of $u_{d1}, u_{d2}$</td>
<td>A</td>
</tr>
<tr>
<td>$i_{ds}$</td>
<td>The drain-source current, current through a SET transistor</td>
<td>A</td>
</tr>
<tr>
<td>$\hat{i}_{ds}$</td>
<td>The peak value of the drain-source current of a SET transistor</td>
<td>A</td>
</tr>
<tr>
<td>$i_g$</td>
<td>A dielectric current through the gate oxide</td>
<td>A</td>
</tr>
<tr>
<td>$i_{gs}$</td>
<td>The input signal current source, connected between gate and source of a SET transistor</td>
<td>A</td>
</tr>
<tr>
<td>$i_{hi}$</td>
<td>The input current of a designed sub-circuit</td>
<td>A</td>
</tr>
<tr>
<td>$i_{ho}$</td>
<td>The output current of a designed sub-circuit</td>
<td>A</td>
</tr>
<tr>
<td>$i_i$</td>
<td>The current modelling the total independent charge on a floating node (island)</td>
<td>A</td>
</tr>
<tr>
<td>$I_i$</td>
<td>The Laplace transform of $i_i$</td>
<td>A</td>
</tr>
<tr>
<td>$i_{in}$</td>
<td>The input current of a (sub-)circuit</td>
<td>A</td>
</tr>
<tr>
<td>$\Delta i_{in}$</td>
<td>The difference between the maximal and minimal amplitude of the input current</td>
<td>A</td>
</tr>
<tr>
<td>$i_{init}$</td>
<td>The current modelling the initial charge</td>
<td>A</td>
</tr>
<tr>
<td>$i_j$</td>
<td>The current flowing to a junction</td>
<td>A</td>
</tr>
<tr>
<td>$i_{ne}$</td>
<td>The current modelling the independent charge due to previous tunnelled electrons</td>
<td>A</td>
</tr>
<tr>
<td>$i_{nf}$</td>
<td>The $1/f$ noise current</td>
<td>A</td>
</tr>
<tr>
<td>Symbol</td>
<td>Description</td>
<td>Page</td>
</tr>
<tr>
<td>--------</td>
<td>-------------</td>
<td>------</td>
</tr>
<tr>
<td>$i_{ni}$</td>
<td>The noise current of the circuit transformed back to the input of the amplifier</td>
<td>A</td>
</tr>
<tr>
<td>$i_{ns}$</td>
<td>The shot noise current</td>
<td>A</td>
</tr>
<tr>
<td>$i_{out}$</td>
<td>The output current of a (sub-)circuit</td>
<td>A</td>
</tr>
<tr>
<td>$\Delta i_{out}$</td>
<td>The difference between the maximal and minimal amplitude of the output current</td>
<td>A</td>
</tr>
<tr>
<td>$i_p$</td>
<td>The current through an electron pump structure</td>
<td>A</td>
</tr>
<tr>
<td>$\Delta i_p$</td>
<td>The difference in current through the electron pump, when pumping in both directions</td>
<td>A</td>
</tr>
<tr>
<td>$i_R$</td>
<td>The current through a resistor</td>
<td>A</td>
</tr>
<tr>
<td>$I_R(t)$</td>
<td>$\int_{t_0}^{t} i_R(t)dt = [I_R(t)]_{t_0}$</td>
<td>A</td>
</tr>
<tr>
<td>$i_t$</td>
<td>The tunnel current, model for the transport of one electron</td>
<td>A</td>
</tr>
<tr>
<td>$I_t$</td>
<td>The Laplace transform of $i_t$</td>
<td>A</td>
</tr>
<tr>
<td>$i_{ubv}$</td>
<td>The current through the voltage source $u_{b,ve}$</td>
<td>A</td>
</tr>
<tr>
<td>$i_{ug}$</td>
<td>The Norton equivalent current source of $u_g$</td>
<td>A</td>
</tr>
<tr>
<td>$i_{us}$</td>
<td>The current through the voltage source $u_s$</td>
<td>A</td>
</tr>
<tr>
<td>$i_x$</td>
<td>The current through one or more components</td>
<td>A</td>
</tr>
<tr>
<td>$k_a$</td>
<td>The total number of capacitances in a circuit</td>
<td>A</td>
</tr>
<tr>
<td>$k_c$</td>
<td>The number of components connected to a node</td>
<td>A</td>
</tr>
<tr>
<td>$k_{cr}$</td>
<td>The number of cross capacitances in the circuit</td>
<td>A</td>
</tr>
<tr>
<td>$k_d$</td>
<td>The number of bias voltage sources</td>
<td>A</td>
</tr>
<tr>
<td>$k_f$</td>
<td>The number of independent magnetic fluxes</td>
<td>A</td>
</tr>
<tr>
<td>$k_g$</td>
<td>The number of gates</td>
<td>A</td>
</tr>
<tr>
<td>$k_i$</td>
<td>The number of current sources in the circuit</td>
<td>A</td>
</tr>
<tr>
<td>$k_{in}$</td>
<td>The number of inputs of a (sub-)circuit</td>
<td>A</td>
</tr>
<tr>
<td>$k_j$</td>
<td>The number of capacitors and junctions in a circuit</td>
<td>A</td>
</tr>
<tr>
<td>$k_n$</td>
<td>The number of nodes in the circuit</td>
<td>A</td>
</tr>
<tr>
<td>$k_{nf}$</td>
<td>The number of floating nodes in the circuit</td>
<td>A</td>
</tr>
<tr>
<td>$k_p$</td>
<td>The number of poles in the input-output relation</td>
<td>A</td>
</tr>
<tr>
<td>$k_q$</td>
<td>The number of independent island charges in the circuit</td>
<td>A</td>
</tr>
<tr>
<td>$k_r$</td>
<td>The number of residues</td>
<td>A</td>
</tr>
<tr>
<td>$k_s$</td>
<td>The sum of the number of junctions, capacitors, and voltage sources in a circuit $k_s = k_j + k_u$</td>
<td>A</td>
</tr>
<tr>
<td>$k_{st}$</td>
<td>The number of steps used in the calculation</td>
<td>A</td>
</tr>
<tr>
<td>$k_t$</td>
<td>The number of tunnel events that took place before $t = t_{ne}$</td>
<td>A</td>
</tr>
<tr>
<td>$k_u$</td>
<td>The number of voltage sources in the circuit</td>
<td>A</td>
</tr>
<tr>
<td>$k_z$</td>
<td>The number of zeros in the input-output relation</td>
<td>A</td>
</tr>
<tr>
<td>$P_{in}$</td>
<td>The power delivered by the previous stage(s) or the input signal source</td>
<td>W</td>
</tr>
<tr>
<td>$P_{out}$</td>
<td>The power delivered to the next stage(s)</td>
<td>W</td>
</tr>
<tr>
<td>$P_{ubv}$</td>
<td>The power delivered by the voltage source $u_{b,ve}$</td>
<td>W</td>
</tr>
<tr>
<td>$q_a$</td>
<td>The charge just after the tunnel event $q_a = q_j(t_a)$</td>
<td>C</td>
</tr>
<tr>
<td>$q_b$</td>
<td>The charge just before the tunnel event $q_b = q_j(t_b)$</td>
<td>C</td>
</tr>
<tr>
<td>$q_{bgc}$</td>
<td>The independent random background charge</td>
<td>C</td>
</tr>
<tr>
<td>$Q_{bgc}$</td>
<td>The Laplace transform of $q_{bgc}$</td>
<td>C</td>
</tr>
<tr>
<td>$q_{cj}$</td>
<td>The charge on the plates of the capacitor which models a SET junction in Coulomb blockade</td>
<td>C</td>
</tr>
<tr>
<td>Symbol</td>
<td>Description</td>
<td>Units</td>
</tr>
<tr>
<td>--------</td>
<td>------------------------------------------------------------------------------</td>
<td>-------</td>
</tr>
<tr>
<td>Δq_{cj}</td>
<td>The difference in charge on the capacitor of the SET junction model</td>
<td>C</td>
</tr>
<tr>
<td>q_{i}</td>
<td>The total independent charge on a floating node</td>
<td>C</td>
</tr>
<tr>
<td>Q_{i}</td>
<td>The Laplace transform of q_{i}</td>
<td>C</td>
</tr>
<tr>
<td>Δq_{in}</td>
<td>The difference between the maximal and minimal amplitude of the input charge</td>
<td>C</td>
</tr>
<tr>
<td>q_{init}</td>
<td>The independent initial charge</td>
<td>C</td>
</tr>
<tr>
<td>Q_{init}</td>
<td>The Laplace transform of q_{init}</td>
<td>C</td>
</tr>
<tr>
<td>q_{j}</td>
<td>The charge on the plates of the junction</td>
<td>C</td>
</tr>
<tr>
<td>dq_{j}</td>
<td>A small change in charge on the capacitance of a SET junction due to a tunnel event</td>
<td>C</td>
</tr>
<tr>
<td>q_{j}^{cr}</td>
<td>The critical charge</td>
<td>C</td>
</tr>
<tr>
<td>Δq_{out}</td>
<td>The difference between the maximal and minimal amplitude of the output charge</td>
<td>C</td>
</tr>
<tr>
<td>q_{ne}</td>
<td>The total independent charge as a consequence of previous tunneled electrons, still on the node at time t_{ne}</td>
<td>C</td>
</tr>
<tr>
<td>q_{node}</td>
<td>The total independent charge on a node</td>
<td>C</td>
</tr>
<tr>
<td>q_{s}</td>
<td>The charge transferred through a voltage source</td>
<td>C</td>
</tr>
<tr>
<td>R_2</td>
<td>A resistor</td>
<td>Ω</td>
</tr>
<tr>
<td>R_{Σ}</td>
<td>The sum of all the tunnel resistors R_T</td>
<td>Ω</td>
</tr>
<tr>
<td>R_b</td>
<td>A bias resistor</td>
<td>Ω</td>
</tr>
<tr>
<td>ΔR_{bias}</td>
<td>The difference between the bias resistors used</td>
<td>Ω</td>
</tr>
<tr>
<td>R_c</td>
<td>The impedance of the controlled source</td>
<td>Ω</td>
</tr>
<tr>
<td>R_f</td>
<td>A feedback resistor</td>
<td>Ω</td>
</tr>
<tr>
<td>R_j</td>
<td>A (non-)linear junction resistor</td>
<td>Ω</td>
</tr>
<tr>
<td>R_s</td>
<td>A series resistor</td>
<td>Ω</td>
</tr>
<tr>
<td>R_T</td>
<td>The tunnel resistance R_T = 2πe^2</td>
<td>T</td>
</tr>
<tr>
<td>R_{T,R}</td>
<td>The tunnel resistor of a junction T_{JR}</td>
<td>Ω</td>
</tr>
<tr>
<td>R_{w}</td>
<td>The resistance of a wire</td>
<td>Ω</td>
</tr>
<tr>
<td>S_{ds}</td>
<td>The bias source connected to the drain and source of a SET transistor (either of a current or a voltage source)</td>
<td>s</td>
</tr>
<tr>
<td>t_0</td>
<td>The moment in time when a discrete event takes place</td>
<td>s</td>
</tr>
<tr>
<td>t_a</td>
<td>The point in time just after the tunnel event</td>
<td>s</td>
</tr>
<tr>
<td>t_b</td>
<td>The point in time just before the tunnel event</td>
<td>s</td>
</tr>
<tr>
<td>t_{bgc}</td>
<td>The point in time when a background charge appears, this is random fluctuating</td>
<td>s</td>
</tr>
<tr>
<td>t_{cr}</td>
<td>The point in time when the tunnel condition is met</td>
<td>s</td>
</tr>
<tr>
<td>t_{ne}</td>
<td>The point in time when we are looking at previous tunneled electrons</td>
<td>s</td>
</tr>
<tr>
<td>t_x, t_y</td>
<td>A moment in time</td>
<td>s</td>
</tr>
<tr>
<td>T_c</td>
<td>The critical temperature</td>
<td>K</td>
</tr>
<tr>
<td>u_{12}</td>
<td>The voltage between node 1 and node 2</td>
<td>V</td>
</tr>
<tr>
<td>u_A, u_B</td>
<td>A voltage in a (sub-)circuit</td>
<td>V</td>
</tr>
<tr>
<td>Δu_A, Δu_b</td>
<td>A voltage drop</td>
<td>V</td>
</tr>
<tr>
<td>u_{bc}</td>
<td>The bias voltage of a threshold circuit</td>
<td>V</td>
</tr>
<tr>
<td>u_{bgc}</td>
<td>The voltage between two nodes, as a consequence of the independent background charge</td>
<td>V</td>
</tr>
<tr>
<td>Symbol</td>
<td>Description</td>
<td></td>
</tr>
<tr>
<td>--------</td>
<td>-------------</td>
<td></td>
</tr>
<tr>
<td>$u_{b,h}$</td>
<td>A bias voltage source at the input to achieve a horizontal shift in the input-output relation</td>
<td></td>
</tr>
<tr>
<td>$u_{b,he}$</td>
<td>A bias voltage source, not placed in series with the input, to achieve a horizontal shift in the input-output relation</td>
<td></td>
</tr>
<tr>
<td>$u_{bi}$</td>
<td>The bias voltage source of an inverter circuit</td>
<td></td>
</tr>
<tr>
<td>$u_{bias}$</td>
<td>A bias voltage source</td>
<td></td>
</tr>
<tr>
<td>$u_{b,fv}$</td>
<td>One of the bias voltage sources attached to the junction, to achieve a vertical shift in the input-output relation</td>
<td></td>
</tr>
<tr>
<td>$u_{bs}$</td>
<td>The bias voltage of an EXOR circuit</td>
<td></td>
</tr>
<tr>
<td>$u_{b,v}$</td>
<td>A bias voltage source at the output to achieve a vertical shift in the input-output relation</td>
<td></td>
</tr>
<tr>
<td>$u_{bv,ve}$</td>
<td>A bias voltage source (not connected to the output) to achieve a vertical shift in the input-output relation</td>
<td></td>
</tr>
<tr>
<td>$u_{c}$</td>
<td>The voltage used for charge compensation</td>
<td></td>
</tr>
<tr>
<td>$u_{ca}$</td>
<td>The output voltage representing the (binary) carry of an adder</td>
<td></td>
</tr>
<tr>
<td>$u_{cs}$</td>
<td>The voltage across a current source</td>
<td></td>
</tr>
<tr>
<td>$U_{cs}$</td>
<td>( \int_{t_z}^{t_y} u_{cs}(t) , dt = [U_{cs}(t)]_{t_z}^{t_y} )</td>
<td></td>
</tr>
<tr>
<td>$u_{csa}$</td>
<td>The voltage across a current source at time $t_a$, $u_{csa} = u_{cs}(t_a)$</td>
<td></td>
</tr>
<tr>
<td>$u_{csb}$</td>
<td>The voltage across a current source at time $t_b$, $u_{csb} = u_{cs}(t_b)$</td>
<td></td>
</tr>
<tr>
<td>$U_{con}$</td>
<td>A constant voltage</td>
<td></td>
</tr>
<tr>
<td>$u_d$</td>
<td>The applied bias voltage source</td>
<td></td>
</tr>
<tr>
<td>$U_d$</td>
<td>The Laplace transform of $u_d$</td>
<td></td>
</tr>
<tr>
<td>$u_{ds}$</td>
<td>The drain-source voltage, voltage between the drain and the source of a SET transistor</td>
<td></td>
</tr>
<tr>
<td>$u_{cr}$</td>
<td>The maximal drain-source voltage at which no current flows</td>
<td></td>
</tr>
<tr>
<td>$u_{cr1}$</td>
<td>The maximal drain-source voltage at which no electron can tunnel through TJ1</td>
<td></td>
</tr>
<tr>
<td>$u_e$</td>
<td>An error voltage</td>
<td></td>
</tr>
<tr>
<td>$u_g$</td>
<td>The gate voltage source, used as input signals or clock</td>
<td></td>
</tr>
<tr>
<td>$U_g$</td>
<td>The Laplace transform of $u_g$</td>
<td></td>
</tr>
<tr>
<td>$u_{ga}$</td>
<td>The gate-source voltage, the voltage between the gate and the source of a SET transistor</td>
<td></td>
</tr>
<tr>
<td>$\Delta u_h$</td>
<td>The horizontal voltage distance to the vertical axis</td>
<td></td>
</tr>
<tr>
<td>$u_{hi}$</td>
<td>The input voltage of a designed sub-circuit</td>
<td></td>
</tr>
<tr>
<td>$u_{ho}$</td>
<td>The output voltage of a designed sub-circuit</td>
<td></td>
</tr>
<tr>
<td>$u_{ih}$</td>
<td>An input voltage, which represents the logic level '1'</td>
<td></td>
</tr>
<tr>
<td>$u_{il}$</td>
<td>An input voltage, which represents the logic level '0'</td>
<td></td>
</tr>
<tr>
<td>$u_{in}$</td>
<td>The input voltage of a (sub-)circuit</td>
<td></td>
</tr>
<tr>
<td>$U_{in}$</td>
<td>The Laplace transform of $u_{in}$</td>
<td></td>
</tr>
<tr>
<td>$\Delta u_{in}$</td>
<td>The difference between the maximal input voltage and the minimal voltage amplitude</td>
<td></td>
</tr>
<tr>
<td>$\tilde{u}_{in}$</td>
<td>The inverted input signal</td>
<td></td>
</tr>
<tr>
<td>$\hat{u}_{in}$</td>
<td>The maximal input voltage</td>
<td></td>
</tr>
<tr>
<td>$u_{init}$</td>
<td>The initial voltage shift due to $q_{init}$</td>
<td></td>
</tr>
<tr>
<td>Symbol</td>
<td>Description</td>
<td>Unit</td>
</tr>
<tr>
<td>--------</td>
<td>-------------</td>
<td>------</td>
</tr>
<tr>
<td>$u_j$</td>
<td>The voltage across the junction</td>
<td>V</td>
</tr>
<tr>
<td>$u_{j}^{cr}$</td>
<td>The critical voltage, the maximal voltage across a junction such that no electron can tunnel</td>
<td>V</td>
</tr>
<tr>
<td>$\Delta u_j$</td>
<td>The difference in voltage across the junction due to a tunnel event $\Delta u_j = u_{ja} - u_{jb}$</td>
<td>V</td>
</tr>
<tr>
<td>$u_{ja}$</td>
<td>The voltage across the junction after tunneling, $u_{ja} = u_j(t_a)$</td>
<td>V</td>
</tr>
<tr>
<td>$u_{jb}$</td>
<td>The voltage across the junction before tunneling, $u_{jb} = u_j(t_b)$</td>
<td>V</td>
</tr>
<tr>
<td>$u_{jR}$</td>
<td>The voltage across junction TJ$_R$</td>
<td>V</td>
</tr>
<tr>
<td>$u_n$</td>
<td>The output voltage of a (sub-)circuit when we apply no input signal(s)</td>
<td>V</td>
</tr>
<tr>
<td>$u_{ni}$</td>
<td>The noise voltage of the circuit when the total noise is transformed back to the input</td>
<td>V</td>
</tr>
<tr>
<td>$u_{nt}$</td>
<td>The noise voltage due to thermal or Johnson noise</td>
<td>V</td>
</tr>
<tr>
<td>$u_o$</td>
<td>The voltage offset in the output voltage</td>
<td>V</td>
</tr>
<tr>
<td>$u_{oc}$</td>
<td>The open circuit voltage (Thévenin)</td>
<td>V</td>
</tr>
<tr>
<td>$u_{oh}$</td>
<td>An output voltage, which represents the logic level '1'</td>
<td>V</td>
</tr>
<tr>
<td>$u_{ol}$</td>
<td>An output voltage, which represents the logic level '0'</td>
<td>V</td>
</tr>
<tr>
<td>$u_{out}$</td>
<td>The output voltage of a (sub-)circuit</td>
<td>V</td>
</tr>
<tr>
<td>$u_{out}^{cr}$</td>
<td>The output voltage of a (sub-)circuit at which in the (sub-)circuit the critical voltage is reached, and thus an electron is allowed to tunnel</td>
<td>V</td>
</tr>
<tr>
<td>$\Delta u_{out}$</td>
<td>The voltage difference between the maximal output amplitude and the minimal output amplitude</td>
<td>V</td>
</tr>
<tr>
<td>$\hat{u}_{out}$</td>
<td>The maximal value of the output voltage</td>
<td>V</td>
</tr>
<tr>
<td>$u_R$</td>
<td>The voltage across a resistor</td>
<td>V</td>
</tr>
<tr>
<td>$u_s$</td>
<td>The voltage of a voltage source</td>
<td>V</td>
</tr>
<tr>
<td>$u_{sa}$</td>
<td>The voltage across the sample</td>
<td>V</td>
</tr>
<tr>
<td>$u_{su}$</td>
<td>The output voltage representing the (binary) sum of the input voltages</td>
<td>V</td>
</tr>
<tr>
<td>$\Delta u_v$</td>
<td>The vertical voltage distance to the horizontal axis</td>
<td>V</td>
</tr>
<tr>
<td>$u_x$</td>
<td>The voltage across one or more components</td>
<td>V</td>
</tr>
<tr>
<td>$u_d$</td>
<td>The drain potential</td>
<td>V</td>
</tr>
<tr>
<td>$v_g$</td>
<td>The gate potential</td>
<td>V</td>
</tr>
<tr>
<td>$v_s$</td>
<td>The source potential</td>
<td>V</td>
</tr>
<tr>
<td>$w_d$</td>
<td>The floating drain node of a SET transistor</td>
<td>V</td>
</tr>
<tr>
<td>$w_o$</td>
<td>The floating gate node of a SET transistor</td>
<td>V</td>
</tr>
<tr>
<td>$X_{A}, X_{B}, X_{con}$</td>
<td>A constant</td>
<td></td>
</tr>
<tr>
<td>$X_{ii}$</td>
<td>The amplification factor of a current controlled current source (see figure 1d)</td>
<td></td>
</tr>
<tr>
<td>$X_{iu}$</td>
<td>The factor between the output voltage and the input current of a current controlled voltage source (see figure 1b)</td>
<td>$\Omega$</td>
</tr>
<tr>
<td>$X_{th}$</td>
<td>A threshold level</td>
<td></td>
</tr>
<tr>
<td>$X_{ui}$</td>
<td>The factor between the output current and the input voltage of a voltage controlled current source (see figure 1c)</td>
<td>$S$</td>
</tr>
</tbody>
</table>
\( X_{uu} \)  The amplification factor of a voltage controlled voltage source (see figure 1a)  
\( Y_{cE} \)  The admittance seen by the tunnel current source \( i_t \), \( S \)  
\( Y_{cE}(s) = Y_e(s) + sC_j \)  
\( Y_e \)  The admittance of the (passive) environment of the SET junction \( Y_e = \frac{1}{Z_e} \)  
\( Z_{12} \)  The impedance between node 1 and node 2 \( \Omega \)  
\( Z_{cE} \)  The impedance seen by the tunnel current source \( i_t \) \( \Omega \)  
\( Z_e \)  The impedance of the environment of the SET junction \( \Omega \)  
\( Z_{in} \)  The input impedance (seen from the input signal source) of the (sub-)circuit \( \Omega \)  
\( Z_L \)  The impedance of the load \( \Omega \)  
\( Z_{out} \)  The output impedance (seen from the load) of the (sub-)circuit \( \Omega \)

![Diagram of controlled sources](image_url)

**Figure 2:** The symbols used in this thesis for controlled sources.
Transistors are the basic building blocks in today's electronic circuits. Scaling down of transistor sizes will unavoidably result in transistors with a completely different behavior. Even before the physical limits are reached there are strong indications that severe engineering problems will occur. Undesired effects like tunnel currents through the thin gate oxides are already occurring in today's complementary metal-oxide semiconductor (CMOS) transistors, which have gate oxide thickness in the nanometer scale (see for example [14, 67, 94]).

Tunneling of electrons is a phenomenon which has been known and been investigated for several decades now. Instead of thinking of tunneling as a disadvantage, one could look for mechanisms that operate at the nanoscale and exploit the quantum effects like tunneling. The objective of this thesis is to discuss the possibilities for circuit design with one of the proposed nanoscale devices, called the Single-Electron Tunneling (SET) junction. Due to the small size of the junction a chip with SET circuits can have a high packing density.

The SET junction is a device through which electrons can tunnel. Tunneling of an electron through an insulator is quantum mechanically possible and it has been measured already in the sixties (see for example [80, 85]). Nowadays it is possible to fabricate and measure the SET transistor accurately enough to check the existing theory. This theory is called the Orthodox theory of single-electron tunneling and it was developed in the nineties [16]. In 1986, Likharev [5] spoke of a Single-Electron Tunneling transistor and people started to investigate small circuits, like logical gates based on the standard CMOS structures (for example the inverter [114]).

Much research has been done and many theses have been written about the SET device. All those theses were written from a device point of view and they use the SET devices in the current-voltage regime. In this kind of research at best an ad-hoc design method can be used, usually based on the standard CMOS structures. A model for the SET junction was developed, which is able to explain the measurements done on SET structures. In the years following the development of the SET junction model no serious steps were taken to develop a method to synthesize circuits that
contain SET junctions. Some steps were taken towards designing circuits, but those steps were either mimicking CMOS designs or they were analyses of SET structures.

Like predicted in the technology roadmap for nanoelectronics [37] these SET structures can not compete with the current CMOS structures, and probably will never be able to do so. Their speed is one of the main problems (they are too slow, only mega-hertz). The limiting speed occurs only in circuits in which the current flows through the SET structure.

This thesis is a first attempt to set up a structured design method for circuits that contain SET junctions. The research described in this thesis should form the bridge between the device modelling and circuit analysis on one side and circuit synthesise (design) on the other. The new model described in this thesis makes it possible to create circuits based on single-electron transitions (which make SET circuits much faster), but also opens the door to designing hybrid circuits, in which SET junctions can be combined with other kinds of circuit components.

1.1 Objective and scope of this thesis

The main scope of this thesis is the design of electronic circuits that contain metal single-electron tunnel (SET) junctions and operate with single electrons. This is done in three steps

1. The design of models for the devices we need in single-electron electronic circuits.

2. The creation of design rules using these models.

3. The design of some example circuits, using these design rules. And explain the measurement results of some basic structures with the help of the developed models.

The models we developed describe the single-electron behaviour, which is specific for the SET junction. They are supposed to replace the current models described in the literature. The model developed models single-electron tunnel events, making it possible to design circuits that operate with one electron only. The transitions between the different states of a circuit based on this single-electron electronics are very fast in comparison with the limited speed of SET structures based on currents. Another advantage of structures that work with a single electron is their very low power consumption (the current is only one electron).

The model developed for the island charge makes it possible to obtain a linear circuit, due to which circuit synthesise and circuit analyse are much easier.

1.2 Outline of the thesis

This thesis is divided in three parts

- Part I: Modelling of SET junctions and independent island charges
- Part II: Methods to design SET circuits
- Part III: Examples and measurements
1.2 Outline of the thesis

Part I starts in chapter 2 with a brief summary of the theory behind tunneling used until now to analyse SET structures and to explain measurement results of those structures. Because the models proposed in the literature only work for tunnel currents and not for a single-electron tunnel event, new models need to be developed.

In the next chapter (chapter 3) our newly developed device models for the SET junction and the independent island charge are given. The tunnel condition derived in the same chapter is based on two voltages: the voltage across the junction just before the tunnel event and the voltage just after the tunnel event.

To be able to use this model in a design strategy we look in more detail at simplifications we can use in chapter 4. The junction model is simplified by creating a tunnel condition expressed in a single voltage (the critical voltage), including a tunnel time to be able to include resistors and other components in a SET circuit, and by some rules of thumb for simplifications of the rest of the circuit.

With the help of these models we are able to make a first attempt at creating a structured circuit design method. This method is discussed in part II. We start with a method to determine the necessary bias condition for a SET structure to get a desired input-output relation in chapter 5.

In chapter 6 we pay some extra attention to periodicity because this is one the characteristics of SET devices. We prove that the input-output relation will be periodic when the structure consists of at least one island and one junction. In chapter 7 we discuss one of the well known problems in SET circuits: the random fluctuating background charges. And we end this part with another problem: the coupling of the designed SET circuits, in chapter 8.

Part III gives examples and validation. In starts with a number of circuit examples in chapter 9, which were designed with the help of the in part II discussed design method. Two of the circuit examples (the SET transistor and the electron pump) are not designed in this way, but exist for some time already. Those circuits are analysed with the help of the models of part I.

In chapter 10 the demands on the measurement equipment are discussed as well as the measurement results of the SET transistor and the electron pump.

The thesis ends with the conclusions in chapter 11.
Part I

Models for the SET junction and the island charge
"Physics is a blind alley again. In any case, it has become too difficult for me, and I would prefer to be a comedian in the cinema, or something like that, and hear no more about physics."

Wolfgang Pauli

La Forge: "Everything was normal, and then, suddenly, it's like the laws of physics went right out the window." Q: "And why shouldn't they? They're so inconvenient."

Star Trek 'True Q'

Problems with the existing theory

New devices are developed based on quantum mechanical mechanisms. One of those devices is the single-electron tunnel (SET) junction. Due to the decreasing dimensions of fabricated devices it is possible to fabricate circuits with SET junctions. For the design of a circuit with SET junctions models are needed. The phenomena that describe the behaviour of the tunnel junction should be included in the model. It is desirable that these circuit models are in agreement with the basic electronic circuit theories. In this chapter an abstract is given only on the models for the SET junction that can be found in the literature. Also a discussion is held, if those proposed models are indeed able to describe a junction in a way needed for a circuit design approach.

A SET junction can be described as two metal conductors (the plates of the junction) separated by a very small gap. The insulator between the conductors is in the classical theory a border that cannot be overcome by electrons. In quantum theory there is a certain chance an electron will pass through this insulator. To have an acceptable chance the electron will tunnel within a short time, the distance between the plates needs to be in the order of a few nano-meter.

Until now results obtained from measurements of SET junctions are explained in the literature with the help of the so called Orthodox theory of single-electronics, first formulated by Averin and Likharev [6].

In the literature an unambiguous definition of the Orthodox theory can not be found, so we will use the term Orthodox theory of single-electronics for the different parts of the existing theory discussed in this chapter.

In many articles the behaviour of the SET junction is described according to this Orthodox theory. Only a brief summary of this theory will be given in this chapter, for further reading see for example [16, 130]. The main goal of this chapter is to show the need for a different model to be able to design circuits with SET junctions. The new model that has been developed is discussed in chapter 3.

The model of the SET junction should at least be in agreement with the theory behind the model. In this chapter we will show some basic circuits, which theoretically give the right answer but when using the circuit model proposed in the Orthodox theory, the answer is incorrect. The model of the SET junction should also fulfill
the demands of a circuit model. It should, for example, be possible to connect the SET junction to other circuit elements, like a resistor or capacitor. Also the tunnel condition should be expressed in terms that can be used in circuit design. Problems of the existing Orthodox theory and the model of the SET junction with these demands, are discussed in this chapter.

For our purposes, namely the design of SET-based circuits, only the behaviour of the SET junction expressed in current (charges) and voltages is important, and not so much the quantum mechanical effect which is the reason for that behaviour.

The first section, section 2.1, describes the assumptions made in the Orthodox theory of single-electronics. To describe the behaviour of the tunnel junction, the condition for the electron to tunnel needs to be included, this condition is described in section 2.2. A simple tunnel condition expressed in a voltage, called the critical voltage, is described in section 2.3. Some extensions are made on the tunnel condition due to the circuit environment the junction is placed in, these extensions are described in section 2.4. The model used in the literature, which claims to describe the SET junction, is discussed in section 2.5. We end this chapter with an enumeration of all the limitations and problems found in the Orthodox theory, which should be solved before a circuit design with SET junctions is possible.

## 2.1 Assumptions made in the Orthodox theory

The Orthodox theory makes the following assumptions

- The electron energy quantizations inside a conductor can be ignored [89].
- The barrier traversal time of the tunneling electron, is called the tunnel time in this thesis. The non-vanishing duration of this tunnel time, τₜ, is neglected [6]. For a circuit which contains resistors and current sources the tunnel time should be made zero.
- Electrons are treated as particles, making it possible to localize them on islands [130].
- Electrons tunnel one-by-one [6]. Let Rₜ be the tunnel resistor (discussed in section 2.5.2) and let Rₖ be a constant called the quantum resistance. The quantum resistance¹ is defined as

\[
Rₖ = \frac{h}{e^2} = 25.8k\Omega
\]  

(2.1)

The tunneling one-by-one is stated to be valid when the tunnel resistor \( Rₜ \gg Rₖ \) [89].

¹The quantum resistor is also called the von-Klitzing resistor. According to [66] the quantum resistor is equal to \( Rₖ = \frac{h}{2e^2} \) and \( Rₖ = \frac{h}{2e^2} \) is used for Josephson junctions to account for Cooper pairs. The quantum resistor is also written as \( R_q \). While most articles indeed define this quantum resistor as \( Rₖ = \frac{h}{2e^2} \) (see for example [30, 45, 49, 51, 84, 117]), also the condition \( Rₖ = \frac{h}{4e^2} = \frac{2h}{2e^2} \) is often used [5, 8, 44, 46, 82, 83, 88, 97, 114, 113, 126, 128, 127]. Some other definitions are also used. To give just a few examples: in [20, 24, 42] they define the resistor as \( Rₖ = \frac{h}{2πe^2} = \frac{h}{e^2} \), and in [28, 35, 53, 54, 95] it is defined as \( Rₖ = \frac{h}{2e^2} = \frac{2h}{e^2} \).
2.2 The tunnel condition

Let us consider a system with at least one SET junction (see figure 2.1). An electron can tunnel through the insulator of the SET junction when the free (electrostatic) energy of the system under consideration will decrease due to this tunnel event [89]. Let $E_a$ be the energy of the complete system after tunneling, and $E_b$ the energy before the tunnel event, then it is possible to write for the tunnel condition (at absolute zero temperature, $T = 0$)

$$E_a < E_b$$

(2.2)

When the condition of equation 2.2 is not met it is called the Coulomb blockade. So the energy condition for the Coulomb blockade is equal to

$$E_a \geq E_b$$

(2.3)

**Definition 2.1** A junction is in Coulomb blockade when a tunnel event can not take place because the free (electrostatic) energy will not be decreased.

For low temperatures the effect of the thermal energy can be neglected, making circuit calculations easy. This neglecting of the thermal energy is normally done in the literature about the Orthodox theory.

![Diagram](image)

Figure 2.1: The system under consideration: a SET junction TJ combined with all kinds of circuit elements in an arbitrary way. The circuit elements can be for example: an other SET junction TJ, a capacitor $C_c$, an inductor $L$, a resistor $R$, a voltage source $u_s$, or a current source $i_s$.

The moment in time when the electron tunnels is stochastically determined. Those stochastics are determined by the physical quantities of the junction, like the distance between the plates of the junction, materials from which the SET junction is made, etc. In this thesis only those structures are investigated where the distance between the plates is very small (nm-regime), which results in an acceptable chance that the electron will tunnel through the insulator within a certain time.
Because the assumption is made that the tunnel time can be neglected (see section 2.1), only capacitors, voltage sources, and junctions have a contribution to the energy change during a tunnel event. The energy change of a current source and the energy change of a resistor is discussed in section 2.2.1 and in section 2.2.2, respectively.

Two methods to calculate the free (electrostatic) energy of the system are considered in the literature, both will give the same answer:

- **Electrostatic energy.** Voltage sources can be included by treating them as very large capacitances \( C \to \infty \) with very large charges on them \( q \to \infty \) [124]. Let \( C \) be the capacitance, \( q \) the charge on the capacitance, and \( k_s \) the sum of the number of capacitors, SET junctions, and voltage sources, then the electrostatic energy \( E \) can be written as

\[
E = \sum_{d=1}^{k_s} \frac{q_d^2}{2C_d} \tag{2.4}
\]

- **Free energy.** This is a method that is more commonly used in the literature than the electrostatic energy method described above. The free energy is the electrostatic energy (without including the voltage sources as capacitances) minus the work done by the voltage sources. The work done by the voltage sources is the transportation of a charge \( q_s \) across the potential difference of the source \( u_s \) [129].

Let \( q \) be the charge on the capacitors and junctions, and \( C \) the capacitance of the capacitors and junctions, \( u_s \) the voltage of the voltage source, \( q_s \) the charge transferred through the voltage source, \( k_j \) the total number of capacitors and junctions in the circuit, and \( k_u \) the number of voltage sources, then the free energy \( E \) can be written as

\[
E = \sum_{d=0}^{k_j} \frac{q_d^2}{2C_d} - \sum_{d=0}^{k_u} u_s q_s d \tag{2.5}
\]

In appendix A.1 an example is given of this method of energy calculation for a circuit consisting of two junctions in series excited by a voltage source.

In the next two subsections the energy contributions to the total change in the system energy during a tunnel event of two commonly used components, the current source and the resistor, are discussed.

### 2.2.1 The effect of a current source

The energy delivered by a current source should also be included in the energy calculations. In the literature this is not done because this energy can be neglected in the case of very small currents [88]. It can also be neglected if the assumption is made that the tunnel time is very small or zero, which is one of the assumptions of the Orthodox theory that was mentioned in section 2.1. The derivation of the energy change of a current source for a zero tunnel time can be found below.

Let \( E_{cs} \) be the energy of a current source, and \( i_{cs} \) and \( u_{cs} \) the current delivered by the source and the voltage across the source respectively (see figure 2.2). Then we
can write for the energy of the current source

\[ E_{cs} = \int u_{cs}(t)i_{cs}(t)dt \] (2.6)

Let \( t_b \) be the time just before the tunnel event starts and \( t_a \) the time just after the tunnel event, then the energy change \( \Delta E_{cs} \) of the current source due to the tunnel event somewhere in the circuit is equal to

\[ \Delta E_{cs} = \int_{t_b}^{t_a} u_{cs}(t)i_{cs}(t)dt \] (2.7)

![Circuit Diagram](image)

Figure 2.2: The system under consideration: a current source \( i_{cs} \) is connected to a circuit, which can contain all kinds of circuit elements in an arbitrary way. The circuit elements can be for example: a tunnel junction TJ, a capacitor \( C_c \), an inductor \( L \), a resistor \( R \), a voltage source \( u_s \), or an other current source \( i_s \).

When the current source delivers a constant current \( i_{cs} \) during the tunnel event, equation 2.7 can be rewritten into

\[ \Delta E_{cs} = i_{cs} \int_{t_b}^{t_a} u_{cs}(t)dt \] (2.8)

**Continues voltage**

Let \( u_{cs} \) be a **continuous** function, let \( U_{con} \) be a constant, and let \( U_{cs} \) be defined by

\[ \int u_{cs}(t)dt = U_{cs}(t) + U_{con} \] (2.9)

Then we can write

\[ [U_{cs}(t)]_{t_x}^{t_y} = \int_{t_x}^{t_y} u_{cs}(t)dt \] (2.10)

The change in energy of the current source will be

\[ \Delta E_{cs} = i_{cs} [U_{cs}(t)]_{t_b}^{t_a} \] (2.11)
Because in the Orthodox theory a tunnel time of zero is assumed, which means $t_a \rightarrow t_b$, equation 2.11 can be rewritten into

$$\Delta E_{cs} = i_{cs} \lim_{t_a \rightarrow t_b} [U_{cs}(t_a) - U_{cs}(t_b)]$$  \hspace{1cm} (2.12)

$$\Delta E_{cs} = 0$$  \hspace{1cm} (2.13)

In words: The current source (with a constant current from $t_b$ to $t_a$) has no contribution to the change in energy of the system during a tunnel event with tunnel time zero, when the voltage across the current source is a continuous function.

**Discrete voltage**

Discrete jumps are of interest here because a tunnel time of zero can imply a discrete jump in the voltage across the current source. Let $\epsilon$ be the step function, which can be defined as

$$\epsilon(t - t_0) = \begin{cases} 0 & t < t_0 \\ [0..1] & t = t_0 \\ 1 & t > t_0 \end{cases}$$  \hspace{1cm} (2.14)

Discrete events appear due to tunnel events (with tunnel time zero) somewhere else in the circuit. In the case of discrete events the energy change will also be zero. This energy change will be zero due to

$$\Delta E_{cs} = i_{cs} \int_{t_b}^{t_a} u_{cs}(t) dt$$  \hspace{1cm} (2.15)

with (see figure 2.3)

$$u_{cs}(t) = u_{csb} - (u_{csb} - u_{csa}) \epsilon(t)$$  \hspace{1cm} (2.16)

Figure 2.3: When an electron tunnels through a junction somewhere in the circuit at the moment in time $t_0$ and the tunnel time $\tau_t = t_a - t_b = 0$, the voltage across the current source can be a step shaped function.

Equation 2.15 combined with equation 2.16 gives

$$\Delta E_{cs} = i_{cs} u_{csb} \int_{t_b}^{t_a} \left( u_{csb} - u_{csa} \right) \epsilon(t) dt$$  \hspace{1cm} (2.17)
2.2 The tunnel condition

with
\[ \lim_{t_a \to t_b} i_{cs} u_{csb} (t_a - t_b) = 0 \]  \hspace{1cm} (2.18)

and
\[ \lim_{t \to 0} \int_0^t \epsilon(t-x)dt = \lim_{t \to 0} \mathcal{L}^{-1}\left\{\frac{1}{s} \frac{\exp(-xs)}{s}\right\} \]  \hspace{1cm} (2.19)

Using the initial value theorem of Laplace [55] this expression can be rewritten into
\[ \lim_{t \to 0} \int_0^t \epsilon(t-x)dt = \mathcal{L}^{-1}\left\{\lim_{s \to \infty} \frac{1}{s} \frac{\exp(-xs)}{s}\right\} \]  \hspace{1cm} (2.20)
\[ = \mathcal{L}^{-1}\left\{\lim_{s \to \infty} \frac{\exp(-xs)}{s}\right\} \]  \hspace{1cm} (2.21)
\[ = 0 \]  \hspace{1cm} (2.22)

In words: A discrete change in voltage across a current source (with a constant current from \( t_b \) to \( t_a \)) has no contribution to the energy of the system, during the time the discrete voltage change took place.

For a non-zero tunnel time \( (\tau_t \neq 0) \), the energy delivered by the constant current source should be included in the energy calculation. Because the Orthodox theory assumes a zero tunnel time this is not done in the literature about the Orthodox theory.

Charge redistribution

The next question that needs to be answered is: how much charge is distributed through the current source during a tunnel event? By definition charge can be written as
\[ dq = idt \]  \hspace{1cm} (2.23)

Let \( q_b \) be the charge just before the tunnel event, and \( q_a \) the charge just after the tunnel event. For the tunnel event equation 2.23 can be written as
\[ \int_{q_b}^{q_a} dq = \int_{t_b}^{t_a} i_{cs} dt \]  \hspace{1cm} (2.24)

The current \( i_{cs} \) delivered by the current source is assumed to be constant during the tunnel event. The tunnel time is assumed to be zero, so \( t_a \to t_b \). Equation 2.24 can be rewritten into
\[ q_a - q_b = i_{cs} \lim_{t_a \to t_b} (t_a - t_b) \]  \hspace{1cm} (2.25)
\[ q_a - q_b = 0 \]  \hspace{1cm} (2.26)

So no charge distribution is possible within a tunnel time of zero.

Concluding: A current source, which has a constant value during the tunnel event, has no contribution to the energy of the system. Neither does it have a contribution to the charge rearrangement, so it can be replaced by an open connection in the circuit used for the energy calculations.
2.2.2 The effect of a resistor

For the energy change due to a tunnel event in a constant linear resistor $R$ a similar analysis as with the current source, can be carried out. Let $u_R$ be the voltage across the resistor $R$, $i_R$ be the current through this resistor (see figure 2.4), and $\Delta E_R$ be the energy difference due to a tunnel event. For this energy difference it is possible to write

$$\Delta E_R = \int_{t_b}^{t_a} i_R(t)u_R(t)dt = \frac{1}{R}\int_{t_b}^{t_a} u_R^2(t)dt$$  \hspace{1cm} (2.27)

Continuous voltage

Let $u_R(t)$ be a continuous function\(^2\), let $X_{con}$ be a constant, and let

$$x(t) = u_R^2(t)$$ \hspace{1cm} (2.28)

$$\int x(t)dt = X(t) + X_{con}$$ \hspace{1cm} (2.29)

Then we can write

$$[X(t)]_{t_a}^{t_b} = \int_{t_a}^{t_b} x(t)dt$$ \hspace{1cm} (2.30)

With the help of equation 2.30 equation 2.27 can be rewritten into

$$\Delta E_R = \frac{1}{R}[X(t)]_{t_b}^{t_a}$$ \hspace{1cm} (2.31)

Figure 2.4: The system under consideration: a resistor $R$ is connected to a circuit, which can contain all kinds of circuit elements in an arbitrary way. The circuit elements can be for example: a tunnel junction TJ, a capacitor $C$, an inductor $L$, an other resistor $R_2$, a voltage source $u_s$, or a current source $i_s$.

\(^2\)The dirac (or delta) function and the step function are not continuous functions.
2.2 The tunnel condition

Because in the Orthodox theory a tunnel time of zero is assumed, which means \( t_a \to t_b \), equation 2.31 can be rewritten into

\[
\Delta E_R = \frac{1}{R} \lim_{t_a \to t_b} \left[ X(t_a) - X(t_b) \right] \tag{2.32}
\]

\[
\Delta E_R = 0 \tag{2.33}
\]

In words: When the voltage across the resistor is a continuous function, a resistor has no energy contribution during a tunnel event with tunnel time zero.

Discrete voltage

Discrete events are of importance here, because a tunnel time of zero can imply a discrete jump in voltage across the resistor (and due to Ohm's law, also a discrete jump in the current). It is possible to prove that zero energy can also be found for discrete currents (or voltages). Because of the definition of the step function (equation 2.14) we can write

\[
\int_{t_b}^{t_a} \epsilon^2(t-x)dt = \int_{t_b}^{t_a} \epsilon(t-x)dt \tag{2.34}
\]

In which case we can use the same derivation as was used in equations 2.19-2.22. This will result also in a change in energy of

\[
\Delta E_R = 0 \tag{2.35}
\]

In the rare case where a delta shaped current is forced through the resistor, which is given here for the completeness, a problem arises with the energy of the resistor. Let the current forced through the resistor be equal to \( i_R(t) = X\delta(t) \), with \( X \) any constant. Let \( t_a = t_b + \frac{1}{N} \), and we define the delta function as

\[
\delta(t) = \begin{cases} 
N & \text{for } t_b < t < t_b + \frac{1}{N} \\
0 & \text{otherwise} 
\end{cases} \tag{2.36}
\]

So for the energy in such a case we can write

\[
\Delta E_R^2 = \int_{t_b}^{t_a} R i_R(t) dt \tag{2.37}
\]

\[
= RX^2 \int_0^{\frac{1}{N}} N^2 dt \tag{2.38}
\]

\[
= RX^2 N \tag{2.39}
\]

In the case of a zero tunnel time \((t_a \to t_b)\), \( N \to \infty \) and hence in this special case the energy of the resistor will go to infinity.
Charge redistribution

The charge redistribution through the resistor has to be calculated. Equation 2.23 can be rewritten into

\[ \int_{q_b}^{q_a} dq = \int_{t_b}^{t_a} i_R(t) dt \]  \hspace{1cm} (2.40)

Let \( I_{con} \) be a constant, and let \( I_R \) be defined by

\[ \int i_R(t) dt = I_R(t) + I_{con} \]  \hspace{1cm} (2.41)

Then we can write

\[ [I_R(t)]_{t_x}^{t_y} = \int_{t_x}^{t_y} i_R(t) dt \]  \hspace{1cm} (2.42)

With the help of equation 2.42 equation 2.40 can be rewritten into

\[ q_b - q_a = R \left[ I_R(t) \right]_{t_x}^{t_a} \]  \hspace{1cm} (2.43)

Using the assumption made in the Orthodox theory: the tunnel time is zero, which means \( t_a \rightarrow t_b \), equation 2.43 can be rewritten into

\[ q_b - q_a = \lim_{t_a \rightarrow t_b} \left[ I_R(t_a) - I_R(t_b) \right] \]  \hspace{1cm} (2.44)

\[ q_b - q_a = 0 \]  \hspace{1cm} (2.45)

So no charge redistribution is possible through a resistor in a time span of zero, in the case of a continuous current but also for a step shaped discrete change in current (due to equation 2.19 - 2.22). In appendix B an example is shown, which indeed shows a change in charge of zero.

Concluding: A resistor does not change the energy of the total system during the tunnel event, when this tunnel event occurs with tunnel time zero. There is also no redistribution possible through the resistor in a time span of zero. For that reason a resistor can be replaced by an open connection in the circuit used for the energy calculations during a tunnel event.

2.3 The critical voltage

Calculations with system energies are time consuming and sometimes difficult when the circuit consists of many components. To go back to the domain of voltages and currents, which a designer of circuits is used to, the term critical voltage is introduced.

**Definition 2.2** The critical voltage is defined as the maximum voltage that can be placed across the junction while it remains in blockade (at zero Kelvin, \( T = 0K \)).
Wasshuber ([129] page 57, [130] page 80) uses the Orthodox theory to calculate the critical voltage $u_j^c$. He uses a Thévenin equivalent circuit to find the critical voltage. The circuit to be analysed is assumed to consist only out of capacitive components (capacitors and junctions)$^3$.

When removing the junction of which the critical voltage is calculated from the circuit (figure 2.5a), a voltage is measured at one single moment in time between node 1 and node 2, which is called the open circuit voltage $u_{oc}$. This voltage is due to all the sources and island charges within the circuit.

![Diagram](image)

Figure 2.5: a) A SET circuit can be separated into the tunnel junction TJ and the rest of the circuit. b) When the rest of the circuit only consists of voltage sources, non-tunneling SET junctions, capacitors and is linear, it can be modelled as a voltage source $u_{oc}$ and a capacitor $C_{th}$ using Thévenin.

To determine the Thévenin capacitance $C_{th}$ all the sources and island charges should be made zero and the junction TJ should be removed. The capacitance that is now found between node 1 and node 2, is the Thévenin capacitance $C_{th}$. The entire circuit (with exclusion of the junction TJ), which consists of (other) junctions, capacitors, and voltage sources only$^4$, can be replaced by this capacitance. The total Thévenin circuit, with the open circuit voltage $u_{oc}$, the Thévenin capacitance $C_{th}$, and the tunnel junction TJ is drawn in figure 2.5b.

A remark should be made about the equivalent circuit of figure 2.5b: An electron that tunnels through junction TJ will not change the values of the Thévenin capacitance $C_{th}$ and the open circuit voltage $u_{oc}$. All the initial charges, also the ones from node 1 and node 2 of figure 2.5b, are modelled in $u_{oc}$. This open circuit voltage $u_{oc}$ is a function of the capacitance values of the used circuit components.

A complex SET circuit is now reduced to a circuit consisting of one junction, one capacitor and one voltage source, which can easily be analysed. Let $C_j$ be the capacitance of the tunnel junction TJ. For the energy difference, $\Delta E_{tot} = E_a - E_b$, one can write (see appendix A.1 for the derivation)

$$\Delta E_{tot} = -\frac{e}{C_{th} + C_j} \left( u_{oc} C_{th} - \frac{e}{2} \right) \quad (2.46)$$

$^3$Any resistor ($R \neq 0$) and current source in the circuit should be replaced by an open connection, as was discussed in the previous section.

$^4$Resistors and current sources are not included because they do not contribute to the energy calculation as was proven in the previous section.
Combined with the relation between the voltage across the junction $u_j$ and the open circuit voltage source $u_{oc}$

$$u_j = u_{oc} \frac{C_{th}}{C_{th} + C_j}$$  
(2.47)

this results in

$$\Delta E_{tot} = -e \left( u_j - \frac{e}{2(C_{th} + C_j)} \right)$$  
(2.48)

The transition between the Coulomb blockade and the current regime is where $\Delta E_{tot} = 0$ (the energy before the tunnel event ($E_b$) is equal to the energy after the tunnel event ($E_a$)), see section 2.2. Let $u_j^{cr}$ be the critical voltage, which is defined as the junction voltage $u_j$ when $\Delta E_{tot} = 0$. Rewriting equation 2.48 gives

$$u_j^{cr} = \frac{e}{2(C_{th} + C_j)}$$  
(2.49)

When dividing the junction voltage $u_j$ by the junction capacitor $C_j$ the so called critical charge $q_j^{cr}$ is found.

$$q_j^{cr} = \frac{e}{2 \left( \frac{C_{th}}{C_j} + 1 \right)}$$  
(2.50)

This equation is mentioned but not derived in [43], [66] (page 72), and [124] (page 33).

Wasshuber does not mention the limits imposed by the use of the Thévenin conversion. When using Thévenin in combination with the calculation of energies it should be done very carefully. Thévenin’s theorem holds for external voltages and currents, but does not necessarily lead to a correct internal electrical power [11, 63, 106].

To use Thévenin the supposed circuit must be a linear circuit [60]. A SET circuit with island charges is a non-linear circuit (see section 3.2.1), which can be made linear by using a separate source to model these independent charges [73].

When using Thévenin for calculating an energy difference based critical voltage only a correct answer is obtained when 1) the circuit is analysed at one single moment in time ($\tau_t \neq 0$), and hence 2) all the current sources and resistors are removed (see section 2.2.1 and section 2.2.2), and 3) all independent excitations are modelled as separate sources to make the circuit linear.

### 2.4 Theories to include resistors in the circuit

Capacitors and inductors will not be a problem in the Orthodox theory. But in real life sources and wires connected to a SET junction are not ideal. Resistors will always be present, but they cannot be included using a tunnel time equal to zero (because the change in energy will always be zero, independent of the resistor value, see section 2.2.2).

In the literature there are many theories to include resistors. In the next sections three theories are discussed:

1. Basic Orthodox theory, which includes the resistor in the energy based tunnel condition.
2.4 Theories to include resistors in the circuit

2. Extended Orthodox theory, which compares the environment of the junction $Z_e$ with a constant called the quantum resistor $R_k$.

3. The phase-correlation theory, which calculates the chance the electron exchanges energy with its environment.

To make the effects resistors have on the SET circuit more clear a simple basic circuit is investigated: one tunnel junction TJ with a resistor $R$ in series, see figure 2.6. The minimum voltage needed to let a current flow (the critical voltage) is investigated for all three theories.

![Figure 2.6: A simple circuit consisting of a tunnel junction TJ with resistor R in series.](image)

2.4.1 Basic Orthodox theory

The basic Orthodox theory of single-electronics uses a tunnel time $\tau_t = 0$. For the calculation of the energy difference due to a tunnel event, resistors in the circuit can be replaced by open connections in the case of zero tunnel time (as was shown in section 2.2.2). Due to the fact that all resistors ($R \neq 0$) have no effect on the energy calculations, a distinction between different environments is impossible.

Let $C_j$ be the capacitance of the tunnel junction TJ and $q_j$ the charge on this capacitance. After removing the resistor from the circuit (see figure 2.7), the energy difference between before the tunnel event and after the tunnel event can be written as

$$E_a - E_b < 0$$  \hspace{1cm} (2.51)

$$\frac{(q_j - e)^2}{2C_j} - \frac{q_j^2}{2C_j} < 0$$  \hspace{1cm} (2.52)

$$\frac{q_j}{C_j} (= u_j) > \frac{e}{2C_j}$$  \hspace{1cm} (2.53)

Due to the fact that the resistor is removed from the circuit (see section 2.2.2) a critical voltage, as described in section 2.3, can be calculated. This will give the same result as equation 2.53: a zero tunnel time results in a critical voltage equal to $\frac{e}{2C_j}$ for all resistors $R \neq 0$.

When there is no resistor in the circuit ($R = 0$, see figure 2.8), there will be an immediately redistribution of charge, because of Kirchhoff's voltage law

$$u_j = u_s \bigg|_{R=0}$$  \hspace{1cm} (2.54)
Figure 2.7: The equivalent circuit of figure 2.6 to calculate the tunnel condition. Because $R \neq 0$ the resistor has no contribution to the energy or to the charge redistribution (due to a zero tunnel time), so it can be replaced by an open.

The energy difference between before the tunnel event and after the tunnel event can be written as

$$E_a - E_b < 0 \quad (2.55)$$
$$\frac{q_j^2}{2C_j} - \left( \frac{q_j^2}{2C_j} - eu_s \right) < 0 \quad (2.56)$$
$$eu_s > 0 \quad (2.57)$$
$$u_s (= u_j) > 0 \quad (2.58)$$

So the critical voltage is equal to $u_j^{cr} = 0$. For these two situations ($R = 0$ and $R \neq 0$) the critical voltage $u_j^{cr}$ as function of $R$ is plotted in figure 2.10a.

Figure 2.8: The equivalent circuit of figure 2.6 to calculate the tunnel condition. Because $R = 0$ the resistor can be replaced by a short.

### 2.4.2 Extended Orthodox theory

A proposed solution to include resistors in SET circuits is to treat a low ohmic environment and a high ohmic environment separately. In many articles (like [64]) the environment impedance $Z_e$ (in figure 2.6: $Z_e = R$) is compared to a constant called the quantum resistor $R_k$ (for the value see page 8). It is called high ohmic if $Z_e \gg R_k$, and low ohmic if $Z_e \ll R_k$. To calculate the energy in those cases, the assumption is made in this extended Orthodox theory that in the low ohmic environment the resistor can be neglected (replaced by a short) and in the high ohmic environment the resistor should be removed (leaving the connection open).

Three regions can be distinguished (see figure 2.10b):
1. If the environment $R$ is much larger than $R_k$ the resistor $R$ is removed so no redistribution can take place, making the critical voltage equal to $\frac{e^2}{2C_j}$ (see equation 2.53).

2. If the environment, in this case $R$, is much smaller than $R_k$, $R$ can be neglected, making the critical voltage equal to zero (see equation 2.58).

3. The critical voltage between those two cases is not defined in this extended Orthodox theory.

### 2.4.3 Phase correlation theory

A third method to include resistors is the phase correlation theory also called the $P(E)$-theory. This theory is based on the chance $P(E)$ that the electron will “exchange energy $E$ with its environment” [130]. This theory uses the approximation in which any environment $Z(\omega)$ is modeled as an infinite number of LC oscillators [101].

The chance that the electron exchanges energy can be written as [66]

$$P(E) = \frac{1}{\hbar} \int_{-\infty}^{+\infty} \exp \left[ K(t) + \frac{jEt}{\hbar} \right] dt$$  \hspace{1cm} (2.59)

with

$$K(t) = 2 \int_{0}^{\infty} \frac{\Re \{Z(\omega)\}}{R_k} \frac{1}{\omega} \left[ \coth \left( \frac{1}{2k_BT} \hbar \omega \right) \left( \cos(\omega t) - 1 \right) - j \sin(\omega t) \right] d\omega$$  \hspace{1cm} (2.60)

$K(t)$ is known as the “equilibrium phase correlation function” [101].

In which $Z(\omega)$ equals the combination of the ohmic resistor $R$ and the junction capacitance $C_j$

$$Z(\omega) = \frac{R}{j\omega RC_j + 1}$$  \hspace{1cm} (2.61)

With the help of these equations the current through a junction as function of the voltage across the junction can be calculated. For four different values of the resistor $R$ (placed in the circuit of figure 2.6) this current is shown in figure 2.9a. The probability for different energies and different resistors is drawn in figure 2.9b.

A disadvantage of this method is that in general it is not possible to obtain analytical results [66]. To obtain the results shown in figures 2.9a and 2.9b a numerical method is used. For the used method see appendix C.

**Concluding:** The probability $P(E)$ can be very small, but will never be zero, making a Coulomb blockade impossible. Always some (small!) current is flowing (see figure 2.9a), in other words the critical voltage will always be zero, see figure 2.10c. A remark should be made about the $P(E)$ theory: it is normally used for the high current region, and not for the calculation of the critical voltage.
Figure 2.9: a) The current $i_j$ through the junction as function of the voltage $u_j$ across the junction for four different series resistors. b) $P(E)$ as function of $E$ for four different (Ohmic) series resistor at $T = 0$ [16, 103, 128, 130].

### 2.4.4 Discussion on the three theories

In the literature of the Orthodox theory of single-electronics the assumption is made that a critical voltage of $u_j^c = \frac{e}{2C_j}$ will only occur using a SET junction excited by a current source, which is modelled with resistors with a very high value. The Orthodox theory even gives a limit for the value of those resistors, namely $R \gg R_k$ [64, 128], which is a direct consequence of the assumptions made in the Orthodox theory, see section 2.1. And a critical voltage of $u_j^c = 0$ is expected for a very low valued series resistor. Both basic assumptions are discussed in more detail in section 2.5.

When the three methods described above are compared, the extended Orthodox theory, in which the series resistor is compared with $R_k$, is in best agreement with these basic assumptions. The problem with this theory is that it can not say anything about the region between $Z_e \gg R_k$ and $Z_e \ll R_k$, and it does not have a sharply defined border of the regions.

### 2.5 Junction model

In the Orthodox theory the behaviour of the SET junction is analysed by exciting the junction TJ with a voltage or a current source. These two extreme cases are well described in the literature.

The first situation, the voltage excited tunnel junction TJ (figure 2.11a), will result in a tunnel condition $|e u_s| > 0$ (for the derivation see equation 2.55 - 2.58). So for any $u_s$ an electron can tunnel, which results in a resistive-like behaviour, as shown
Figure 2.10: The critical voltage for the circuit of figure 2.6, for three different implementations of the Orthodox theory of single-electronics. a) Including a resistor in the energy calculation, b) using comparison between $R_k$ and the environment resistor $R$, and c) the $P(E)$ theory.

In figure 2.11b [54]. A current is assumed to consists of many electrons, making the stochastics of a single electron unimportant.

Figure 2.11: a) The SET junction TJ excited by the voltage source $u_s$. b) The static relation between the voltage across the junction and the current through the junction, of a voltage excited junction ($u_j = u_s$).

The second situation, the current excited junction TJ with a junction capacitance of $C_j$, shown in figure 2.12a, will have a tunnel condition $|u_j| > \frac{e}{2C_j}$, which results
in a saw tooth shaped voltage across the junction as a function of time, as shown in figure 2.12b [89]. The slopes of this saw tooth show the capacitive behaviour of the junction. The charging of the junction is assumed to be very slow, making it possible for the electron to tunnel at a voltage just above the critical voltage $\frac{e}{2C_J}$.

![Diagram](image)

Figure 2.12: a) The SET junction TJ excited by a current source $i_s$. b) The dynamic behaviour of a current excited junction ($i_j = i_s$).

The current source charges the junction until the critical voltage $u_j^{cr} = \frac{e}{2C_j}$ is reached. Then an electron will tunnel, lowering the voltage across the junction with an amount of $\frac{e}{C_j}$ (shown in figure 2.12b). The behaviour of the SET junction can be described by the charge on the junction plates $q_j$ as function of the voltage across the junction $u_j$ (figure 2.13). This response clearly shows a capacitive behaviour, with $C_j = \frac{q_j}{u_j}$. Because the charging of the junction is done by a current source, the charging is a function of time (as is shown in figure 2.12).

![Diagram](image)

Figure 2.13: The behaviour of the junction excited by a current source, described by the charge $q_j$ as function of the voltage across the junction, clearly showing a capacitive behaviour $C_j$. 
2.5 Junction model

2.5.1 The tunnel rate

Let $\Gamma$ be the tunnel rate. The current $i_j$ through the junction is determined by the number of electrons that tunnel per unit time, from the positive to the negative side of the junction $\Gamma$, minus the number of electrons that tunnel in the same time span from the negative to the positive side $\Gamma$ (see figure 2.14). Based on these definitions the current through the junction in the Orthodox theory is equal to [54]

$$i_j(\Delta E) = e \left( \Gamma(\Delta E) - \bar{\Gamma}(\Delta E) \right) \quad \forall \ T \tag{2.62}$$

![Diagram of current through a junction](image)

Figure 2.14: The definition of the tunnel rates.

For metal SET junctions the Orthodox theory states a tunnel rate $\Gamma$ of

$$\Gamma(\Delta E) = \frac{\Delta E}{e^2 R_T \left\{ \exp \left( \frac{\Delta E}{k_B T} \right) - 1 \right\}} \tag{2.63}$$

in which $\Delta E$ is the change in free energy, $\Delta E \equiv E_a - E_b$. From this equation it is clear that even if there is a Coulomb blockade ($\Delta E \geq 0$ according to equation 2.3), a current can still flow due to a temperature unequal to zero Kelvin. At zero temperature ($T = 0$) there is always a Coulomb blockade for $\Delta E \geq 0$

$$\Gamma(\Delta E) = \begin{cases} \frac{-\Delta E}{e^2 R_T} & \Delta E < 0 \\ 0 & \Delta E \geq 0 \end{cases} \tag{2.64}$$

This is also approximately true in case of $\Delta E \gg k_B T$.

Due to symmetry of the junction it is possible to write

$$\Gamma(\Delta E) = \bar{\Gamma}(-\Delta E) \tag{2.65}$$

This symmetry changes formula 2.63 into

$$\bar{\Gamma}(\Delta E) = \frac{\Delta E}{e^2 R_T \left\{ 1 - \exp \left( -\frac{\Delta E}{k_B T} \right) \right\}} \tag{2.66}$$

\(^5\)The direction of the electrons is opposite to the direction of the movement of a positive charge e.
At zero temperature this reduces to

$$\Gamma'(\Delta E) = \begin{cases} 0 & \Delta E < 0 \\
\frac{\Delta E}{e^2 R_T} & \Delta E \geq 0 \end{cases}$$

(2.67)

Which is also approximately true in case of $\Delta E \gg k_B T$.

Comparing equations 2.64 and 2.67 it is clear that at zero Kelvin only equation 2.64 gives a non-zero tunnel rate due to the tunnel condition $\Delta E < 0$.

### 2.5.2 Tunnel resistor and junction resistance

Let $R_T$ be the tunnel resistor [34], which is determined by the transmission coefficient $T$, and $D_i$ the density of the states on the initial side, and $D_f$ the density of states on the final side of the barrier. For a metal junction the density of states can be taken as a constant, while the density of states in a superconductor or a semiconductor is energy dependent [130]. In this thesis only the metal SET junction is treated. So the tunnel resistor holds

$$R_T = \frac{\hbar}{2\pi e^2 |T|^2 D_i D_f}$$

(2.68)

Let $R_j$ be the junction resistance, which is defined as

$$R_j = \frac{\partial u_j}{\partial i_j}$$

(2.69)

In the Orthodox theory of single-electronics the behaviour of the junction is described by two constants: the junction capacitor $C_j$ and the tunnel resistor $R_T$. In the literature on the Orthodox theory of single-electronics a difference between the tunnel resistor $R_T$ and the junction resistance $R_j$ is generally not mentioned. The model for the SET junction used in some references, for example [4, 28, 54, 58], consists of a capacitor $C_j$ and a junction resistance $R_j$ (see figure 2.15). They assume that the junction resistance $R_j$ (of equation 2.69) is equal to the tunnel resistor $R_T$ (of equation 2.68). It should be clear that this assumption is only true when the junction resistance $R_j$ is equal for all differences in junction voltages, hence $R_j$ should be linear. The junction resistance $R_j$ is linear when there is no Coulomb blockade ($u_{ij}^{\tau} = 0$) and the temperature is zero Kelvin (see figure 2.11b). This is only the case for a voltage excited junction (at $T = 0$), making the model of figure 2.15 unusable for any circuit design.

![Diagram](image)

Figure 2.15: The model for the SET junction used in the Orthodox theory [4, 18, 25, 28, 33, 58, 85, 102, 133].
Not only the fact that the junction resistance should be different than the tunnel resistor but also the unavoidable presence of a resistor in the model makes the model of figure 2.15 unusable for describing SET circuits. A current will always flow through the junction resistance $R_j$ in the model when there is a junction voltage $u_j \neq 0$. For this type of model it is impossible to maintain independent island charges, which is one of the basic requirements for SET circuits.

The model of figure 2.15b can easily be made more accurate solving the problem of maintaining independent charges on the islands as was mentioned above. A non-linear junction resistance $R_j$ can be introduced in the model (see figure 2.17). The junction resistance $R_j$ is in this model only equal to the tunnel resistor $R_T$ when the tunnel condition is satisfied ($|u_j| > u_j^{cr}$, see also figure 2.16)

$$R_j = \begin{cases} \infty & \text{if } |u_j| \leq u_j^{cr} \\ R_T & \text{if } |u_j| > u_j^{cr} \end{cases}$$

(2.70)

Figure 2.16: The definition of the junction resistance $R_j$. The junction resistance $R_j$ is only equal to the tunnel resistor $R_T$ in some special cases, in this figure when $|u_j| > u_j^{cr}$.

In some articles (for example [102]) an equivalent circuit is used with a junction resistance $R_j$ depending on the voltage across the capacitor.

Figure 2.17: A refinement on the model for the SET junction used in the Orthodox theory: replacing the linear junction resistance $R_j$ of figure 2.15 by a non-linear junction resistance $R_j$.

Floating nodes, which are needed to make the storage of independent island charges possible, are created in the cases when the non-linear resistance $R_j$ happens to be infinitely large ($R_j \rightarrow \infty$). But the model with the non-linear resistance
is still not capable of explaining some of the basic responses of a SET junction, like the current excited junction response of figure 2.12b. This is caused by the fact that the SET junction models described above are based on currents through the junction, and hence can only explain the static behaviour of the SET junction, and not the dynamic behaviour of a single tunnel event. The problem that occurs within the above described models is the negative junction voltage after a tunnel event, which can not be created with a capacitor and a resistor only.

The junction resistance is added to the model to explain the tunnel process. This junction resistance is not equal to zero, hence the tunnel event (which is the movement of a charge equal to the electron charge from one side of the junction to the other side) is a time consuming process. Because a zero tunnel time is assumed no charge can be transferred through the resistor, nor can any energy be dissipated in the resistor (see section 2.2.2). This makes it impossible to explain (with the help of the circuit model) what happens to the difference in energy during the tunnel event.

### 2.6 Summarizing the limitations of the existing theory

As discussed in this chapter the existing theory to model SET junctions is not useable for circuit design, for the following reasons:

- **There is no energy conservation in the system under consideration.** The tunnel condition is based on the loss of energy due to a tunnel event. The Orthodox theory described in the literature gives no satisfying answers as to what happens to this energy.

- **The energy calculations become time consuming when the circuit gets larger.** Charges due to tunneling of electrons should first be distributed on the junctions before the energy differences can be calculated.

- **The model used to describe the behaviour of a single junction is limited in use.** The dynamic behaviour of the SET junction that is the most interesting (the single-electron tunnel events) can not be modelled with a junction model proposed in the literature, because it is based on the static current behaviour.
  - Timing aspects of single-electron tunnel events can not be modelled by the proposed junction model. Due to the inclusion of a junction resistance in the model a charging time is imposed [114, 134].
  - Single-electron behaviour can not be modelled with the junction model proposed in the literature. The junction resistance just gives a current behaviour, a current consists of many electrons.
  - (related to the last item) The behaviour of the current source excited junction can not be modelled with the proposed junction model.

- **When analysing a SET circuit with resistors, the outcome is completely determined by the chosen method to include a resistor.**
2.6 Summarizing the limitations of the existing theory

- In the basic Orthodox theory (which uses a zero tunnel time, \( \tau_t = 0 \)) a junction with in series a resistor \( (R \neq 0) \) will always have a Coulomb blockade equal to \( \frac{\phi}{2e} \).

- Extended methods have been developed to solve the problem of the inclusion of resistors.
  1. The extended Orthodox theory model, which has an undefined region.
  2. The \( P(E) \)-theory, which is unusable for calculation of the critical voltage \( (\nu_{tr} = 0 \text{ always}) \).

- When including a tunnel time \( \tau_t \neq 0 \), calculations of energies to determine the tunnel condition always give \( \Delta E < 0 \) due to the energy dissipation of the resistor.

- Including tunnel times becomes hard. The basic theory assumes that this tunnel time will have almost no influence on the energy. When a circuit is excited by a current source with a large current and the tunnel time is not neglected, the energy delivered to the circuit by this source can not be neglected making the analysis of the circuit more complex.

- The derivation of the critical voltage is only true in very specific cases, due to the use of Thévenin when deriving this critical voltage based on an energy condition.

The Orthodox theory of single-electronics is a semi-classical description based on energies, which is sometimes combined with a quantum mechanical based \( P(E) \) theory to describe the environment (like resistors). To be able to design circuits the whole theory should be transformed to a complete semi-classical description. In the next chapter(s) a description of a new model for the SET junction is given, which is more suitable for circuit design. The new model solves the above problems and limitations.
Problems with the existing theory
"Unlearn what you have learned."

Yoda

"A model should be as simple as possible and yet no simpler."

Albert Einstein

New device models for circuit theory

In the analysis and design of electrical circuits, models are used to represent the physical behaviour of a device. Models are simplifications of reality, which describe the essential behaviour of those aspects we are interested in. An electrical model consists of an equivalent circuit, built with ideal components, which can be linear or non-linear components. This equivalent circuit describes the components behaviour in terms of currents and voltages. To be able to do circuit design with these models, we should be able to use basic network theorems like Kirchhoff's voltage and current law (charge and energy conservation). Some devices require a number of equivalent circuits to describe all the possible regimes of operation.

In the previous chapter a model for the single-electron tunneling (SET) junction was given, which is extensively used in the literature. Many problems appear when this model is used to explain the known behaviour, like tunneling of a discrete charge. In this chapter we discuss our model for the SET junction, which is able to model a single tunnel event appearing in SET circuits. Such a model is needed to design circuits containing SET junctions and to explain the results obtained from measurements of these circuits.

In the first section we shall show that the tunneling of an electron can be modelled with a current source. This model does not have the limitations and problems encountered in the previous chapter. In the second section we will describe a model for the independent charges, which is needed to make the circuit linear. The independent charge model consists of a current source as well. And we will end this chapter with some conclusions.

3.1 A new tunnel junction model

In this section we describe an equivalent model for the tunnel junction. This description is split into three parts. Firstly, we model the junction when no electron tunnels; hence the model of a linear capacitor is used. Secondly, we derive a tunnel condition based on energy differences due to the tunnel event. And we end this section with
the complete equivalent model, which results in energy conservation for the complete system.

### 3.1.1 No tunneling

A metal tunnel junction consists of two metal contacts separated by an insulator. When *no electrons are tunneling* we can model this structure as a linear capacitor (see figure 3.1). In the general model of the capacitor the amount of charge \( q_{ej} \) on each 'plate' of the metal junction, is proportional to the voltage \( u_j \) across the insulator between the plates. The constant between this voltage and the charge depends on the geometry of the metals and the thickness, shape and material used as an insulator. This constant is called the junction capacitance, \( C_j \).

\[
q_{ej}(t) = C_j u_j(t) \tag{3.1}
\]

In network theorems we normally use voltages and currents. Due to conservation of charge we can transform equation 3.1, with the help of the relation

\[
i_{ej} dt = dq_{ej} \tag{3.2}
\]

into the well known relation between voltage and current of a linear capacitor

\[
i_{ej}(t) = C_j \frac{du_j(t)}{dt} \tag{3.3}
\]

Because we assumed there was no tunneling we can also write

\[
i_{ej}(t) = i_j(t) \tag{3.4}
\]

and hence

\[
i_j(t) = C_j \frac{du_j(t)}{dt} \tag{3.5}
\]

In the derivation of this equation \( C_j \) is assumed to be independent on the voltage across the junction. For the metal SETs we are analysing here this is a correct assumption.

![Figure 3.1](image_url)

Figure 3.1: a) The symbol for the SET junction TJ. b) In the absence of tunneling the junction can be modelled as a linear capacitor \( C_j \).
3.1.2 Tunnel condition

The tunnel condition in the Orthodox theory of single-electronics (see section 2.2) is based on the total energy of the system before and after tunneling. A different method is to look at the cause of the energy change: the tunneling of the electron. The tunnel condition described here is based on this last method.

We can rephrase the tunnel condition of the Orthodox theory into saying that the electron is allowed to tunnel when this tunnel event lowers the energy of the junction: it radiates\(^1\) [61, 78]. Let \(E_{jb}\) be the energy of the junction before the tunnel event, and \(E_{ja}\) the energy of the junction just after the tunnel event. Let \(\Delta E_j\) be the change in energy of the junction, which is equal to

\[
\Delta E_j = E_{ja} - E_{jb}
\]

The junction will radiate when \(\Delta E_j < 0\).

To transform a quantum mechanical phenomenon into a classical (circuit) description some assumptions have to be made. A tunnel event of an electron can be seen as a discrete transfer of a charge \(e\) from one side of the junctions capacitor to the other side (see figure 3.2). Such a tunnel event appears within a time span zero, so this movement of charge can be modelled as a dirac (delta) shaped current, as is shown in figure 3.3.

![Figure 3.2: A tunnel event can be seen as the discrete transfer of a charge \(e\).](image)

![Figure 3.3: When an electron tunnels at the moment in time \(t_0\), this movement of a charge \(e\) due to the tunnel event can be modelled as a dirac function with \(i_t = e\delta(t - t_0)\).](image)

---

\(^1\)The energy radiated, using \(E = \frac{he}{\lambda}\), is in most cases converted into phonons. In the rare case that we apply a voltage across a junction (with a barrier of a few nm) almost equal to the break-through voltage, the smallest wavelength \(\lambda\) we can obtain is in the infrared region. Using \(t = \frac{1}{f} = \frac{\lambda}{c}\) we obtain \(t \approx 10^{-14}\) seconds. Due to the complex measurement setup (discussed in section 10.1) no measurement results are yet available to prove this.
Due to the zero tunnel time no current source or resistor will have a contribution to the voltage across the junction just after the tunnel event (see also section 2.2.1 and section 2.2.2), and hence current sources and resistors can be replaced by an open connection (removed from the circuit). In this way a purely capacitive circuit will result. The electron that has tunneled will cause a (direct, within the time span zero) redistribution of the charge. The amount of charge that is changed on the junction depends on the capacitance of the environment. Let \( C_e \) be the capacitance of the environment (see figure 3.4) and \( \Delta q_{cj} \) be change in charge on the capacitance of the junction \( C_j \), then we can write for this change in charge

\[
\Delta q_{cj} = e \frac{C_j}{C_j + C_e}
\] (3.7)

The junction capacitor can still be seen as a linear capacitor, due to the fact that the electron that has tunneled is modelled outside the capacitor (see figure 3.4), which makes it possible to use equation 3.5. So a delta shaped tunnel event will always cause a step shaped voltage drop across the junction (as shown in figure 3.5).

Figure 3.4: A tunnel event within a SET junction placed in a purely capacitive environment (with capacitance \( C_e \) will result in a voltage across the junction, which is the derivative of this current (multiplied by a constant).

Figure 3.5: When an electron tunnels at the moment in time \( t_0 \) and the tunnel time \( \tau_t = t_a - t_b = 0 \), the voltage across the junction is a step shaped function.

The time before the electron really starts tunneling (the so called wait time \( \tau_w \), see section 3.1.4) is stochastically determined. Let \( t_b \) be the moment in time the tunnel event starts and \( t_a \) the moment in time the tunnel event stops. Looking at figure 3.4 we can calculate the energy change of the junction capacitor, due to the tunnel event
3.1 A new tunnel junction model

(assuming a temperature of \( T = 0K \), by

\[
\Delta E_j = \int_{t_b}^{t_a} u_j(t)i_j(t)dt
\]  
\[(3.8)\]

Let \( u_{ja} = u_j(t_a) \) and \( u_{ja} = u_j(t_a) \) then we can, with the help of equation 3.5, rewrite equation 3.8 into

\[
\Delta E_j = C_j \int_{u_{ja}}^{u_{ja}} u_j(t)du_j
\]  
\[(3.9)\]

which is equal to

\[
\Delta E_j = \frac{C_j}{2} (u_{ja}^2 - u_{jb}^2)
\]  
\[(3.10)\]

This is the amount of energy radiated due to a tunnel event. As mentioned before the junction radiates (looses energy) when \( \Delta E_j < 0 \). To obtain the condition for tunneling we only need to determine the amount of energy change during such a tunnel event as a function of the voltage across the junction.

We can write the energy condition of the junction, based on equation 3.10

\[
\frac{C_j}{2} (u_{ja}^2 - u_{jb}^2) < 0
\]  
\[(3.11)\]

Because the capacitance \( C_j \) is always larger than zero we can rewrite this condition into

\[
u_{ja}^2 - u_{jb}^2 < 0
\]  
\[(3.12)\]

Equation 3.12 gives us four possible tunnel events, see table 3.1, which are shown in figure 3.6a-d. In this figure the energy is proportional to the distance to the horizontal axis. From this figure it is clear that the "after" situations, black dots, are closer to the horizontal axis than the "before" situations, the white dots. Which indicates that the energy after tunneling is lower than before.

Table 3.1: Four different tunnel conditions based on the voltage across the junction just before the tunnel event \( u_{ja} \) and just after the tunnel event \( u_{ja} \) (equation 3.12).

<table>
<thead>
<tr>
<th></th>
<th>( u_{ja} &lt; u_{jb} )</th>
<th>( u_{ja} &gt; 0 )</th>
<th>( u_{ja} &lt; 0 )</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>( u_{ja} - u_{jb} &lt; 0 )</td>
<td>( u_{ja} &gt; 0 )</td>
<td>( u_{jb} &gt; 0 )</td>
</tr>
<tr>
<td>2</td>
<td>( u_{ja} + u_{jb} &lt; 0 )</td>
<td>( u_{ja} &gt; 0 )</td>
<td>( u_{jb} &lt; 0 )</td>
</tr>
<tr>
<td>3</td>
<td>( -u_{ja} - u_{jb} &lt; 0 )</td>
<td>( u_{ja} &lt; 0 )</td>
<td>( u_{jb} &gt; 0 )</td>
</tr>
<tr>
<td>4</td>
<td>( -u_{ja} + u_{jb} &lt; 0 )</td>
<td>( u_{ja} &lt; 0 )</td>
<td>( u_{jb} &lt; 0 )</td>
</tr>
</tbody>
</table>

When the voltage across the junction after the tunnel event is smaller than the critical voltage (discussed in chapter 4) \( u_{ja} < |u_j^c| \) (see figure 3.6) the electron is not allowed to tunnel anymore, because in those cases the energy of the system would increase due to tunneling. This region in which the electron is not allowed to tunnel is called the Coulomb blockade region. Definition 2.1 can now be rewritten to a more simple definition
Figure 3.6: (a-d) The four possible voltage tunnel conditions. The numbers of the conditions correspond to the conditions in table 3.1. The difference in voltage (vertical drop) is the same for the same junction: the voltage drop due to tunneling of one electron.

**Definition 3.1** A junction is in Coulomb blockade when a voltage across the junction is present but no electron can tunnel through the SET junction.

The conclusions that can be drawn from figure 3.6 are:

- Conditions 1 and 4, and 2 and 3 are the same, only the voltage across the junction is mirrored.

- Condition 2 and 3 are always the last condition. After a tunnel event that satisfies this condition tunneling can not occur anymore until the voltage across the junction is changed. Condition 1 and 4 can be the last condition, but do not have to be.

These tunnel conditions are the starting point for the rest of the thesis.

### 3.1.3 Electron transport

Tunneling of an electron is the movement of a charge with value $-e$ Coulomb, through the insulator, from the side with a low potential to that with a high potential, in the
3.1 A new tunnel junction model

tunnel time $\tau_t$. The tunneling phenomenon is not included in classical linear circuit theory. To model the movement of charge due to tunneling, an external circuit is required. This external circuit should transfer a charge, exactly equal to the charge of one electron from, one side to the other side of the junction. In the proposed model a positive charge $e$ is transferred from the positive side of the junction capacitor to the negative side by using an external circuit in its simplest form: a current source\(^2\), with current $i_t$, in parallel with the junction (figure 3.7b).

Figure 3.7: a) The symbol for the SET junction TJ. b) The proposed model for the SET junction, in which tunneling through the insulator of the junction TJ is modeled by a current source. This model is called the impulse model in [62].

Let $t_b$ be the time just before the tunnel event starts, and $t_a$ the time when the electron has reached the other side of the barrier, then the tunnel time $\tau_t$ will be

$$\tau_t = t_a - t_b$$

(3.13)

For the tunnel current $i_t$ we can write

$$\int_{t_b}^{t_a} i_t(t)dt = e$$

(3.14)

By using a current source to model the electron tunneling, see figure 3.7b, we obtained an electrically correct equivalent circuit (charge conservation). The equivalent circuit also satisfies energy conservation. The change in energy caused by this tunnel current source is the same as the total energy change. For the case of a capacitive circuit this is proven in appendix A.3. In circuits with resistive elements, the total system energy is still conserved due to the fact that those resistive elements dissipate energy.

The reason to include a current source in the model is two fold:

1. To model the transfer of exactly one electron from one side of the capacitor to the other side.

2. To model the change in energy due to a tunnel event.

\(^2\)As a symbol for the tunnel current source we do not use the symbol of a voltage controlled current source because the current $i_t$ delivered by the source is independent of the applied junction voltage. Only the moment in time the tunnel event starts depends on the junction voltage.
3.1.4 Stochastic processes

When the tunnel condition is met, the electron will not tunnel immediately due to the stochastic behaviour of electron tunneling. Between the time \( t^{cr} \) when the tunnel condition is met and the time \( t_b \) just before the electron really tunnels, there is a certain wait time \( \tau_w \), see figure 3.8. In some papers (for example [116]) this is called: the dwell time.

![Diagram](image)

Figure 3.8: Definitions of different times during the tunnel process.

Depending on the circuit we want to design there are two possible methods to include this in the model:

1. For single-electron circuits: Enlarge the time just before the tunnel event, by adding a stochastic time \( \tau_w \). For every tunnel event this stochastic constant has to be calculated again. This method should be used when one is interested in the single-electron behaviour. A disadvantage is the relatively large computation time per tunnel event.

   When the junction is connected to a material that contains a large amount of electrons which are able to tunnel, the wait time before one of those electrons tunnels becomes very small.

2. For small current circuits: Calculate the average time of the Poisson distributed [116] wait time. This time depends on the voltage across the junction.

   Let \( \tau_w \) be the average waiting time. We should enlarge the tunnel time \( \tau_t \) with this average waiting time to calculate the averaged total time needed to let an electron tunnel. This average wait time depends on the voltage across the junction as we will describe in section 3.1.5. This method is possible when looking at a current, which is based on an average number of electrons that passed within a certain time.

3.1.5 Low current regime

When we are looking at a current through a SET junction we consider more than one electron. The electrons tunnel independent of each other and at random through the SET junctions, which makes it possible to describe the times between the tunnel events by a Poisson distribution [116].

**Definition 3.2** An electric current is defined as the net amount of charge that passes a point per unit time.
3.1 A new tunnel junction model

Let \( i_j \) be the current through the SET junction and \( \Delta q_{cj} \) be the change in charge on the 'plates' of the junction, between the moment in time \( t = 0 \) and the moment in time \( t = \tau \), then we can write

\[
\Delta q_{cj} = \int_{0}^{\tau} i_j(t) dt
\]  

(3.15)

Equation 3.15 can be used to determine the dwell time in those cases where the voltage across the junction is changed within this dwell time.

When we assume \( i_j \) to be constant\(^3\) (DC analyse) during the time interval \([0 - \tau]\) we can rewrite this expression into

\[
\Delta q_{cj} = i_j \tau
\]  

(3.16)

Let \( n \) be the number of electrons that have tunneled within the mentioned time span \([0 - \tau]\) and \( e \) the charge of an electron, then we can rewrite equation 3.16 into

\[
n e = i_j \tau
\]  

(3.17)

So one electron passes the measure point in an average time \( \bar{\tau} \)

\[
\bar{\tau} = \frac{\tau}{n}
\]  

(3.18)

Now we can express the current \( i_j \) as

\[
i_j = \frac{e}{\bar{\tau}}
\]  

(3.19)

As discussed in the previous section, due to the Poisson distribution we are able to calculate an average wait time \( \bar{\tau}_w \) for one electron to tunnel. The tunnel event itself takes \( \tau_t \), so in average the electron will take a total time of \( \bar{\tau} = \bar{\tau}_w + \tau_t \) to tunnel to the other side.

So for the current through the junction \( i_j \) we can write

\[
i_j = \frac{e}{\bar{\tau}_w + \tau_t}
\]  

(3.20)

Due to the fact that we are averaging, we are loosing the dynamics of single-electron behaviour. In this way we can calculate the static properties of SET devices, such as the current-voltage characteristics.

The waiting time \( \tau_w \) and the tunnel time \( \tau_t \) are independent. The tunnel time \( \tau_t \) is assumed to be constant (see section 4.2.1). We can rewrite the current into

\[
i_j = \frac{e}{\bar{\tau}_w + \tau_t}
\]  

(3.21)

For the average waiting time \( \bar{\tau}_w \) the following conditions should be met [75]:

\(^3\)For the measurements done (see chapter 10) this is a valid assumption, because those measurements are done with a slow varying junction current, or junction voltage (see for the relation between the junction voltage and the current equation 3.22).
• The waiting time should go to infinity when we bias the junctions in its Coulomb blockade

• The waiting time can not be negative

A current $i_j$ will flow through the junction when the voltage $u_j$ across the junction is higher than the critical voltage $u_j^{cr}$ (see figure 3.9). In the region where this current flows the slope of the graph is equal to $R_T = \frac{1}{G_T}$. So we can write

$$R_T = \frac{1}{G_T} = \frac{u_j - u_j^{cr}}{i_j - 0} \text{ for } u_j > u_j^{cr} \tag{3.22}$$

We should note here that this tunnel resistance $R_T$ by the above definition is only there when many electrons are tunneling sequentially. The resistance has no meaning when we look at single-electron behaviour only.

![Figure 3.9: The definition of the tunnel resistance $R_T = \frac{1}{G_T}$](image)

By combining 3.21 and 3.22 the average wait time (when $\bar{\tau}_w >> \tau_t$) can be written as

$$\bar{\tau}_w \approx \frac{eR_T}{u_j - u_j^{cr}} \text{ for } u_j > u_j^{cr} \tag{3.23}$$

The relation between the voltage across the junction $u_j$ and the total time until the electron has reached the other side of the junction, $\bar{\tau}_w + \tau_t$ is drawn in figure 3.10. The behaviour of the average wait time $\bar{\tau}_w$ of equation 3.23, is as expected, because in the two extremes: when the junction is biased in the Coulomb blockade no electron is able to tunnel ($\bar{\tau}_w \rightarrow \infty$). On the other hand when we apply an extremely large voltage, an electron will tunnel almost immediately ($\bar{\tau}_w \rightarrow 0$).

The wait time derived in this section is compared to the wait time derived from simulations in section 9.3.5 and is compared to the wait time derived from measurements in section 10.2.2. Both showing the expected behaviour of equation 3.23.

### 3.1.6 Speed of a junction

From the last section it is clear that the speed of the junction is mainly limited by the stochastic behaviour, $\bar{\tau}_w$. The average time for a tunnel event can theoretically be decreased to the tunnel time $\tau_t$, when it is possible to neglect the average wait
3.2 Independent charges

Figure 3.10: The sum of the average wait time \( \bar{\tau}_w \) and tunnel time \( \tau_t \) as function of the constant (no-time varying) voltage across the junction, \( u_j \).

time \( \bar{\tau}_w \). Equation 3.23 shows that we can decrease the wait time by increasing the voltage across the junction (compared to the critical voltage) or by decreasing the tunnel resistance \( R_T \) during fabrication of the junction.

When we are able to reduce the wait time to the order of the tunnel time \( \tau_t \) a junction can operate at frequencies of \(^4\) \( 10^{15} \) Hz.

3.1.7 Temperature

A high temperature gives the electron extra energy, which makes it easier to tunnel. It creates more states for the electron to be in, so its chance of tunneling will be larger. In the Orthodox theory of single-electronics the temperature is modelled in the tunnel rate (see equation 2.63), this makes it hard to model the temperature influence on a single electron tunneling event.

A temperature higher than zero Kelvin should lower the tunnel condition in all cases. And hence we can include a circuit model to model the influence due to a temperature of \( T \neq 0 \) in the tunnel condition. For example, adding a voltage source, which models this temperature, in series with a reference voltage source, modelling the critical voltage, can do this. In the rest of the thesis we will assume that the influence of the temperature can be neglected.

3.2 Independent charges

In the previous section we derived a tunnel condition expressed in voltages across the junction \( u_j \). Due to the fact that SET junctions are very small, charges in the order of one electron or less, play an important role on those voltages. The voltage across the junction is determined by the charge \( q_j \) on the 'plates' of the junction \( u_j = \frac{q_j}{C_j} \).

The charge \( q_j \) is the sum of two types of charges:

\(^4\)Assuming that the tunnel time is (almost) constant and in the order of \( 10^{-15} \) seconds, see section 4.2.1.
1. Source dependent charges on capacitor plates, due to voltage or current sources in the circuit.

2. Independent charges in the neighbourhood of the component. The existence of the independent charges are threefold

- Initial charges
- Background charges
- Tunneling charge: an integer number of the electron charge

It is important for circuit analysis, like the calculation of the junction voltage, that these independent charges are taken into account. To be able to do so, a useable circuit model should be made for those independent charges.

Let $q_{\text{node}}$ be the total independent charge on a node. This independent charge is distributed over all $k_c$ components connected to that node, in order to satisfy Kirchhoff’s voltage law. The amount of charge $q_d$ distributed over each component $d$ depends on the circuits topology (see for an example figure 3.11).

$$q_{\text{node}} = \sum_{d=1}^{k_c} q_d$$  \hspace{1cm} (3.24)

Figure 3.11: The C-SET transistor, with an independent charge $q_{\text{node}}$ on the island (node $w$). This independent charge is distributed across the connected junctions and the capacitor ($q_{\text{node}} = q_1 + q_2 + q_3$). Let $C_{j_1}$ be the capacitance value of tunnel junction TJ$_1$, and let $C_{j_2}$ be the capacitance value of tunnel junction TJ$_2$. The values of $q_1$, $q_2$, and $q_3$ depend on the applied sources, such that $u_g = -\frac{q_2}{C_{j_1}} + \frac{q_1}{C_{j_2}}$ and $u_b = -\frac{q_1}{C_{j_1}} + \frac{q_3}{C_{j_2}}$.

The independent charge on a node is only maintained when there is no charge ‘leakage’. Leakage does not occur when there are only capacitive elements connected to the floating node, no background charge appears, and no tunneling to or from that floating node takes place. In all the other cases the charge stored on a node is a function of time.

In a system charge is conserved: the sum of all charges in a circuit (including the substrate) should be zero. Let $k_n$ be the number of nodes in the circuit, and $q_{\text{node}}$
the total independent charge stored on the components connected to that node, then we can write

$$\sum_{d=1}^{k_n} q_{\text{node},d} = 0$$

(3.25)

### 3.2.1 Linear circuits

According to network theory the computation necessary to calculate voltages across or currents through a component can be reduced by using superposition in case of linear circuits. This reduction makes linear circuits very useful for designers of electronic circuits, it enables them to analyse the influence of each source independently.

We assume in this section that the circuit to be analysed has no non-linear elements (all non-linearities are taken out), making the theory described in this section only valid for the tunnel junctions when no electron is tunneling at the moment in time when we analyse the circuit.

A remark must be made concerning the existence of island charges. Island charges will create a non-linear term in the circuit description in the same way initial charge on capacitors do. By realising that an island charge is composed of "initial" charges on the capacitors and tunnel junctions that form the island, the circuit including island charges can be linearised by considering the "initial" conditions as sources in the same way this is done in circuits that take initial charges on capacitors into account [73].

**Superposition**

The superposition principle can be stated as [105]:

**Definition 3.3** The response of a linear electric circuit to a number of independent excitations is equal to the sum of the responses of each excitation separately (while the other excitations are given the value zero).

This means that:

- Independent charges on capacitors and independent magnetic flux in inductors, should be seen as separate excitations, just like independent voltage and current sources.

- The circuit (figure 3.12) consists of linear elements only, like linear resistors $R$, linear capacitors $C$, linear inductors $L$, and linear dependent sources (not drawn in the figure).

The voltage $u_{12}$ between the nodes 1 and 2 of a linear circuit (see figure 3.12) is determined by

- $k_u$ independent voltage sources $u$, which are related to the voltage $u_{12}$ by the circuit constant $\alpha$ with $L\{u(t)\} = U(s)$ and $L\{\alpha(t)\} = A(s)$.

- $k_i$ independent current sources $i$, which are related to the voltage $u_{12}$ by the circuit constant $\beta$ with $L\{i(t)\} = I(s)$ and $L\{\beta(t)\} = B(s)$.

- $k_q$ independent node charges $q$, which are related to the voltage $u_{12}$ by the circuit constant $\psi$ with $L\{q(t)\} = Q(s)$ and $L\{\psi(t)\} = \Psi(s)$.
Figure 3.12: Superposition is possible when the circuit consists of linear components, and the independent sources are modelled outside the circuit.

- $k_f$ independent magnetic fluxes $\phi$, which are related to the voltage $u_{12}$ by the circuit constant $\xi$ with $\mathcal{L}\{\phi(t)\} = \Phi(s)$ and $\mathcal{L}\{\xi(t)\} = \Xi(s)$.

The voltage between the nodes can be determined separately by summation (using superposition) of the effect each source has on the voltage $u_{12}$

$$u_{12}(t) = \mathcal{L}^{-1}\left\{ \sum_{d=1}^{k_u} A_d(s)U_d(s) + \sum_{d=1}^{k_i} B_d(s)I_d(s) + \sum_{d=1}^{k_q} \Psi_d(s)Q_d(s) + \sum_{d=1}^{k_f} \Xi_d(s)\Phi_d(s) \right\}$$

(3.26)

The calculation of the voltage $u_{12}$ is now split into $k_u + k_i + k_q + k_f$ easier parts, namely the calculation of the constants $A_d$, $B_d$, $\Psi_d$, and $\Xi_d$ which can be determined by straightforward linear network calculation. In the rest of this thesis the independent magnetic fluxes are not taken into account, as they are not often used in SET circuits.

**Linear circuit**

Superposition can only be used if the circuit is linear. A component or circuit is called linear when it satisfies both of the following properties [92]:

Let $\zeta_{in}$ be the applied quantity, $\zeta_{out}$ the response, and $X_A$ and $X_B$ any constant.

- **Scaling property**
  A component or circuit has scaling properties when the relation
  
  $$\zeta_{in}(t) \rightarrow \zeta_{out}(t)$$
  
  (3.27)

  can be scaled to
  
  $$X_A\zeta_{in}(t) \rightarrow X_A\zeta_{out}(t)$$
  
  (3.28)

- **Additive property**
  A component or circuit has the additive property when it satisfies
  
  $$\zeta_{in,1}(t) + \zeta_{in,2}(t) \rightarrow \zeta_{out,1}(t) + \zeta_{out,2}(t)$$
  
  (3.29)

Both properties can be combined in one expression

$$X_A\zeta_{in,1}(t) + X_B\zeta_{in,2}(t) \rightarrow X_A\zeta_{out,1}(t) + X_B\zeta_{out,2}(t)$$

(3.30)
3.2 Independent charges

An example

A linear circuit is made non-linear when an independent source, like an independent charge is included within the circuit. To illustrate this, a simple circuit of two capacitors is analysed, see figure 3.13a. The relation between the applied voltage $u_s$ and the voltage $u_2$ across capacitor $C_2$ is $\frac{C_2}{C_1 + C_2}$. Due to an independent charge $q_i$ on the node $w$, this relation is shifted from the origin by a factor $\frac{q_i}{C_1 + C_2}$ making it a non-linear relation, see figure 3.13b. Hence, any independent node charge $q_i$ has to be modelled as an independent source outside the circuit to make the circuit linear, which is necessary for superposition.

\[ u_2(t) = u_s(t) \frac{C_1}{C_1 + C_2} + q_i \epsilon(t) \frac{1}{C_1 + C_2} \] (3.31)

Figure 3.13: a) A simple circuit with two capacitors in series. b) Due to an independent charge on node $w$ a shift in the voltage relation appears.

If we assume that the independent charge $q_i$ was in the circuit at moment $t = 0$ we can model this independent charge by an independent voltage source or an independent current source, as shown in figure 3.14. To determine the output voltage $u_2$ we can now use superposition

Figure 3.14: The same circuit as shown in figure 3.13a, only the independent island charge $q_i$ is modelled as an independent current source. The grey area contains now a linear circuit.

\footnote{Due to charge conservation a charge of $-q_i$ will be the sum of the independent charges on the other nodes.}
3.2.2 Background charges

When we are looking at very small structures in the nanometer regime, small variations, like atomic vibration, or charge that arises due to the collision of particles from outside with the circuit or its direct environment, play an important role.

Charges which are fluctuating randomly in the background, called offset charges or background charges [137], can have a high impact on the behaviour of single-electron tunneling. Not only the amount of charge is stochastic but also the moment in time the background charge appears is stochastic.

The exact reason that these background charges appear is still not quite clear, researchers give different reasons for the appearance\footnote{There are some resemblances with 1/f noise. The origin of this 1/f noise is, like the random background charge, still open for speculations. It is shown that the 1/f noise is related to traps located in the oxide, number of carriers [123], mobility fluctuations, impurities, and defects [21].}.

A small (atomic scale) shift of a single charged impurity inside the tunnel barrier of the junction [88], or even near the tunnel junction [114] or island [129, 131] can lead to a considerable change of charge. Also work different work functions of electrodes [114], thermal excitations [104], trapping and de-trapping effects of electrons [90, 104, 131], or small random variations of the island size or shape [90] can cause these charge shifts to appear.

The reason for the fact that these background charges are random in time is in some cases quite clear: impurities can migrate, trapped electrons might get detrapped. The better the processing techniques will become, the more precise we can control the purity of materials used in SET junctions.

Due to these independent charges, which can be very large, the tunnel condition is met and some electrons will tunnel. This will cause the independent charge to be almost completely compensated by that of the tunneling electrons. However, this compensation can never be exact, because of discreteness (e-quantizations) of the electrical charge. According to Likharev [87] and Tucker [114] this charge can be considered as a random constant with an uniform probability distribution over the interval $[-\frac{e}{2}, \frac{e}{2}]$.

Such a change in the independent charge will always change the charge on (at least) two nodes in the circuit due to the charge conservation (see equation 3.25). Let $q_{bgc}$ be the independent random background charge. These charges give rise to a voltage drop across the component (with impedance $Z_{12}$) that is placed between the two nodes of which the charge is changed (see figure 3.15a) and can be modelled with a voltage $u_{bgc}$ or, by using the Norton equivalent current $i_{bgc}$ (see figure 3.15b). Usually we are not interested in the dynamic properties of the background charge. It suffices to model the charges from the moment they are there, which can be done by modelling the charges with a delta function. Let $t_{bgc}$ be the moment in time the independent background charges are in the circuit. Then we can write

$$i_{bgc}(t) = q_{bgc} \delta(t - t_{bgc})$$ (3.32)
3.2.3 Charges due to previous tunnel events

When we look at a circuit at a certain point in time, tunneling could have taken place before this time. Let \( t_{ne} \) be the moment in time we are looking at the circuit. Depending on the topology of the circuit a part of the charges due to the electrons that have tunneled can still be on that node. When the circuit contains floating nodes, the charge due to tunneling on these floating nodes is always an integer number of electrons.

Let \( t_d \) be the moment tunnel event \( d \) took place, which is independent of the number of electrons that already have tunneled. In figure 3.16a all the different tunnel events (at different moments in time) that took place before \( t_{ne} \) are summed over time, using the tunnel model of figure 3.7. With \( k_t \) the number of tunnel events that took place before time \( t_{ne} \).

When we analyse a circuit at \( t_{ne} \) we can model the total remaining charge as the sum of all those sources which appeared in the history of the circuit. Let \( q_{ne} \) be the total independent charge as a consequence of previously tunneled electrons, still on the node at \( t_{ne} \). Then the current can be written as (shown in figure 3.16b)

\[
i_{ne}(t) = q_{ne} \delta(t - t_{ne})
\]

3.2.4 Initial charges

At time zero \( (t = 0) \), the moment we start connecting the circuit to the external sources, an unknown independent charge can be initially present anywhere in the circuit, this is what we call initial charge. The existence of this charge can have many reasons, like fabrication errors in the substrate, or doping concentration, giving a constant charge offset. Also the two types of independent charges mentioned already: background charge and charge due to tunneling, are part of the initial charge when they appeared before time zero. The initial charge can be modelled by a current source, \( i_{init} \) between the two nodes, which have a difference in charge. Let \( Z_{12} \) be the impedance seen between those two nodes. The source \( i_{init} \) is in parallel with the impedance \( Z_{12} \) as is shown in figure 3.17. The current source that models the initial independent charge has a value of

\[
i_{init}(t) = q_{init} \delta(t)
\]
Figure 3.16: a) The current source modelling the different tunneling events of one electron at different moments in time \(k_i\) is the number of tunnel events that took place before time \(t_{ne}\). b) The simplified model for the charges due to previous tunnel events.

Figure 3.17: Modelling of the initial independent charge by a current source \(i_{init}\).

### 3.2.5 Total independent charge model

Due to equation 3.24 the total independent charge on a node is the sum of all independent charges on the connected components. As shown in the last three sections all these independent charges can be modelled as current sources.

A positive charge on a node, has a negative counter charge distributed across the other nodes, due to charge conservation, equation 3.25. Due to this all the independent charges on each node in the circuit can be modelled with a current source, connected between that node and one common node. The same current sources can be found using current source transportation (see figure 3.18), also known as the \(i\)-shift theorem [22]. By using this theorem we can change all the independent current sources, into current sources by connecting one side to a common node (0).

The total model for all the independent charges is shown in figure 3.19, in which the total current is equal to

\[
\begin{align*}
    i_i(t) &= q_{init}\delta(t) + q_{bgc}\delta(t - t_{bgc}) + q_{ne}\delta(t - t_{ne}) \\
    i_{i}(t) &= q_{node}\delta(t)
\end{align*}
\]

For a circuit with \(k_n\) nodes, including the ground node, we will have \(k_n - 1\) current sources connected to the common node for example ground to model all the independent charges. Due to charge conservation, equation 3.25, these are not
3.3 Conclusions

When no electrons tunnel through a SET junction it can be modelled as a capacitor. In the case that an electron tunnels through the insulator the movement of charge is modelled with a current source (in parallel to the junction capacitor). This is a phenomenological model. The current source is able to model not only the movement of the electron charge, but also the change in energy due to this tunnel event.

When the electron tunnels is determined by the tunnel condition. This tunnel condition is derived in this chapter by assuming a zero tunnel time, and hence taking only capacitive circuits into account. An electron can tunnel when this tunnel event lowers the energy of the junction, the junction radiates. The tunnel condition can be expressed in two voltages: the voltage just before the tunnel event and the one just after the tunnel event.

With the help of the derived tunnel condition, an expression can be found for the voltages across the junction for which no electrons are allowed to tunnel. When no electron is allowed to tunnel the junction is said to be in the Coulomb blockade. The same voltage values for the Coulomb blockade are derived with the help of the tunnel condition of the existing theories (described in chapter 2).

The independent island charges are modelled by a current source, to make the circuit linear, which allows us to use superposition in a circuit synthesis or analysis.
"Knowledge is a process of piling up facts; wisdom lies in their simplification."

Martin Fischer

"Order and simplification are the first steps toward the mastery of a subject."

Thomas Mann

The critical voltage

One of the most interesting behaviours of the single-electron tunnel (SET) junction is the discrete tunneling of electrons. To design or analyse a circuit using SET junctions we need to determine a simple condition when the electron starts to tunnel.

A simple voltage condition was developed by other researchers, based on the Orthodox theory described in chapter 2. This voltage condition was called the critical voltage, which is the maximal voltage across a junction to be in Coulomb blockade. In section 2.3 a formula was derived for the critical voltage based on the Orthodox theory. This formula is only valid for voltage driven capacitive circuits. In practical situations also other components, like resistors, should be included. In the Orthodox theory described in chapter 2 there was no satisfying way to include the effect a resistor has on the critical voltage (see section 2.4).

As was shown in section 2.2.2, a resistor will have no contribution to the system energy during the tunnel event (when we assume a zero tunnel time), independent of the resistive value of the resistor. When we introduce a resistor in a circuit and a non vanishing tunnel time, the energy change in the circuit during a time interval (unequal to zero) will always be zero (see also appendix A.4). Hence no tunnel condition can be derived based on this zero energy difference. For that reason we assume that the tunnel condition derived based on two voltages is still valid, even for a non-zero tunnel time. With the help of those two voltages we will derive a new tunnel condition in this chapter based on only one voltage: the critical voltage. And we will show the consequences of a non-zero tunnel time for circuits that contain resistors.

In the first section of this chapter we derive an equation for the critical voltage, which is also able to include other circuit elements (like the resistor). The starting point for this derivation is the local voltage condition derived in chapter 3 instead of the in the Orthodox theory of single-electronics used energy condition. Our formula for the critical voltage will give the same results as the formula for the critical voltage based on the Orthodox theory for the limiting cases: \( R = 0 \) and \( R \rightarrow \infty \).

In the second section of this chapter we discuss a method for analysing circuits with resistors or other non-capacitive circuit elements. We also discuss an example circuit that contains a resistor. This example shows the effect of the resistor value,
the tunnel time, and the shape of the tunnel current on the derived critical voltage. This chapter ends with some conclusions.

The methods described in this chapter are used in the rest of this thesis to design and analyse SET circuits.

4.1 The critical voltage

Tunneling of electrons is one of the most important aspects of the SET junction, so the tunnel condition should be made easy to calculate. In section 3.1.2 a tunnel condition was derived, which determines if the electron can cross the insulator. The tunnel condition is expressed in two local voltages: the voltage across the SET junction just before the tunnel event, and the voltage across the SET junction just after the tunnel event. To make the tunnel condition calculations easier, we should derive an expression for the tunnel condition based on one voltage only: the critical voltage. In this section we will derive a formula for the critical voltage.

An electron is allowed to tunnel when this tunnel event lowers the energy of the junction: this energy difference will be radiated (see section 3.1.2). Let \( u_j \) be the junction voltage, let \( t_b \) be the moment in time just before the tunnel event, and let \( t_a \) be the moment in time just after the tunnel event. We define the voltage across the junction, just before the tunnel event as \( u_j(t_b) = u_{jb} \) and the voltage across the junction just after the tunnel event as \( u_j(t_a) = u_{ja} \). For the energy difference of the junction we can write (equation 3.11)

\[
\frac{C_j}{2} (u_{ja}^2 - u_{jb}^2) < 0
\]  

which is equal to

\[
u_{ja}^2 - u_{jb}^2 < 0
\]  

When deriving the tunnel condition of equation 4.2 the assumption was made that the tunneling of one electron takes no time, it tunnels instantaneously. The inclusion of the model of this tunnel event (the current source) results in a conservation of energy, and hence no (new) tunnel condition, based on energy differences, can be derived when this current source is included in the model. From here on we assume that we are allowed to enlarge the tunnel time without changing the tunnel condition that has been found.

In figure 4.1 the SET junction TJ under investigation is drawn. This junction can be attached to all kinds of components and sources, modelled as 'the rest of the circuit'.

The critical voltage is defined as the maximal voltage across the junction such that the junction is still in Coulomb blockade, also see definition 2.2. When we apply a voltage across the junction higher than the critical voltage, an electron will tunnel.

4.1.1 The tunnel condition expressed in voltages

Two situations can be distinguished:

1. An electron tunnels from node 1 to node 2, so a positive charge \( e \) has moved from node 2 to node 1 (figure 4.2a). The voltage across the junction after the
tunnel event \( u_{ja} \) is increased by \( \Delta u_j \) due to this charge movement (figure 4.2b).

\[
  u_{ja} = u_{jb} + \Delta u_j
\]  

(4.3)

Combining this with equation 4.2 gives a condition for the voltage \( u_{jb} \), which is the voltage across the junction just before the tunnel event

\[
  u_{jb} < -\frac{\Delta u_j}{2}
\]  

(4.4)

2. An electron tunnels in the opposite direction, from node 2 to node 1, so a positive charge \( e \) has moved from node 1 to node 2 (figure 4.3a). The voltage across the junction after the tunnel event \( u_{ja} \) is decreased by \( \Delta u_j \) due to this charge movement (figure 4.3b).

\[
  u_{ja} = u_{jb} - \Delta u_j
\]  

(4.5)

Combining this with equation 4.2 gives the voltage \( u_{jb} \), just before the tunnel event, which is equal to

\[
  u_{jb} > \frac{\Delta u_j}{2}
\]  

(4.6)
The critical voltage

Figure 4.3: One of the two possible tunnel events: a) An electron tunnels through junction TJ from node 2 to node 1, which is the same as a positive charge tunneling from node 1 to node 2. b) Due to this tunnel event the voltage across the junction is decreased by $\Delta u_j$.

These voltages across the junction just before the tunnel event $u_{j0}$ determine the border between the Coulomb blockade and the region where tunneling is allowed, see figure 4.4. The voltage drop $\Delta u_j$ is a circuit topology depending constant.

Figure 4.4: The critical voltages $-\frac{\Delta u_j}{2}$ and $\frac{\Delta u_j}{2}$ determine the borders of the area where no current can flow, $i_j = 0$, the Coulomb blockade.

We define the maximal voltage across a junction (called the critical voltage $u_{jcr}$) to let no electron through that junction as

$$u_{jcr} = \frac{\Delta u_j}{2}$$  \hspace{1cm} (4.7)

The difference in voltage, $\Delta u_j$, is due to tunneling of an electron, this tunnel event is modelled as a current source $i_{t}(t)$. This current source is placed in parallel with the junction capacitor $C_j$ (see figure 3.7).
4.1.2 Derivation of the critical voltage

By modelling all the independent charges as current sources, as was discussed in section 3.2, we obtain a circuit that can be divided into sources (current and or voltage sources) and components (in a SET circuit mostly junctions and capacitors). If all the circuit elements used are linear we can use superposition. Let $\alpha$ and $\beta$ be the circuit depending constants ($L\{\alpha(t)\} = A(s)$ and $L\{\beta(t)\} = B(s)$), describing the relation between the voltage across the junction $u_j$ and the independent voltage and current source respectively. If we have $k_u$ voltage sources and $k_i$ current sources, we can write for this junction voltage $u_j$

$$u_j(t) = L^{-1} \left\{ \sum_{d=1}^{k_u} A_d(s) U_d(s) + \sum_{d=1}^{k_i} B_d(s) I_d(s) \right\} \quad (4.8)$$

It is only allowed to use superposition when no electron is tunneling, in that case the junction is modelled as a capacitor, which is a linear component. A note should be made about the model for the junction: the capacitance of a tunnel junction and the single electron that tunnels are independent of the voltage across the junction, making the use of superposition possible.

Equation 4.2 describes the relation between the junction voltage before and after a tunnel event. When calculating the change in voltage due to a tunnel event we assume that all sources are constant during the short time interval of this tunnel event (the tunnel time $\tau_t$). In that case the change in voltage $\Delta u_j$ is only due to the tunneling of the electron, making it possible to remove all the other sources from the circuit during the calculation. Let $t_b$ the moment in time just before the tunnel event, and $t_a$ the moment in time just after the tunnel event, then the tunnel time $\tau_t$ is equal to $\tau_t = t_a - t_b$.

In figure 4.5, the circuit is split up into the capacitor $C_j$ to model the capacitance of the tunnel junction, the current source $i_t$ to model the tunnel event, and the rest of the circuit, $Y_c$, containing no sources. Let $\beta_n$ be the circuit topology depending constant, which is the relation between the tunnel current $i_t$ and the voltage drop $\Delta u_j$ across the junction which has a capacitance of $C_j$. Then we can write for the voltage change $\Delta u_j$ due to only the tunnel current source $i_t$ (using equation 4.8)

$$\Delta u_j(t) = L^{-1} \{B_n(s) I_t(s)\} \quad (4.9)$$

Because $i_t(t)$ is an independent source, the critical voltage of a component has a fixed value depending on the circuit topology and does not depend on other sources in the circuit.

The tunnel current $i_t(t)$, which was in chapter 2 a dirac function, is now enlarged to a pulse by including a non-zero tunnel time. This tunnel current models the tunneling of a single electron, and should satisfy

$$\int_{t_b}^{t_a} i_t(t) dt = e \quad (4.10)$$

We can model all the circuit elements which are connected between two nodes as an impedance $Z_{cir}(s)$, which is the same as the input impedance seen for the tunnel
current source \( i_t(t) \) (see figure 4.5). Because the junction capacitance \( C_j \) is in parallel with the tunnel current source, we can write for the circuit constant \( \beta \)

\[
B_n(s) = Z_{cir}(s) = \frac{1}{Y_{cir}(s)}
\]

This means that we can write for \( \Delta u_j \)

\[
\Delta u_j(t) = \mathcal{L}^{-1} \left\{ \frac{I_t(s)}{Y_{cir}(s)} \right\}
\]

Figure 4.5: The circuit consists of a tunnel junction TJ, which is modeled as a capacitance \( C_j \) and a current source \( i_t \), and the rest with an admittance \( Y_e \).

The admittance \( Y_{cir} \) between the two nodes, across which we are calculating the voltage, can be separated into two parts: 1) the junction capacitance \( C_j \) and 2) the admittance of the environment of the junction, \( Y_e \) (see figure 4.5). Because we removed all the sources from the circuit (mentioned earlier in this section) and we assume that the components used in the rest of the circuit are linear components, the rest of the circuit called \( Y_e \) will be completely linear.

\[
Y_{cir}(s) = sC_j + Y_e(s)
\]

So we can rewrite equation 4.7 with the help of equation 4.12 into

\[
u_j^{cr}(t) = \frac{1}{2} \mathcal{L}^{-1} \left\{ \frac{I_t(s)}{sC_j + Y_e(s)} \right\}
\]

It should be noticed that the above critical voltage is a function of time. This time dependence is caused by the fact that the changes in the circuit due to a tunnel event continue after the tunnel event has taken place. These changes will end in some cases only for \( t \to \infty \), depending on the circuit.

The definition of the critical voltage is only meaningful at \( \tau_t \) (see figure 4.2b and 4.3b). In the derivation above we assumed that the tunnel event started at time zero \( (t_b = 0) \), and the time window \( t_a - t_b \) equals \( \tau_t \), which results in

\[
u_j^{cr} (t = \tau_t) = \frac{1}{2} \mathcal{L}^{-1} \left\{ \frac{I_t(s)}{sC_j + Y_e(s)} \right\} \bigg|_{t=\tau_t}
\]

One of the limitations of the Orthodox theory, see section 2.4, was the fact that all resistors unequal to zero give the same critical voltage. Our above derived formula for the critical voltage, equation 4.15, will give a different expression for the critical voltage for different resistors, due to a different \( Y_e(s) \).
4.2 Resistors and tunnel time

As will be shown in this section, resistors can be included in the derived critical voltage. The tunnel time and the chosen shape of the tunnel current sometimes play an important role in the outcome. When the shape (and tunnel time) of the tunnel current play a part in the node voltages and currents in the circuit. The environment and the capacitance $C_j$ of the tunnel junction under investigation determines if the shape (and tunnel time) of the tunnel current plays a role.

4.2.1 Neglecting the tunnel time

For a design it is not always needed to take everything into account, the tunnel time for example is of importance only in some special cases. This section gives some simple rules of thumb for the possibility to model the tunnel current with a delta function multiplied by the electron charge; $i_t = e\delta(t)$. In which case the tunnel time is neglected and hence the shape of the tunnel current has no influence anymore.

The tunnel time is defined as the time between just before the tunnel event, and just after the tunnel event, $\tau_t = t_a - t_b$. This time is needed for the electron to go from one side of the barrier to the other side, also called the barrier traversal time $\tau_t$ [15, 57, 59, 69].

We know that the tunneling will be a fast phenomenon, some papers report for metallic tunnel junctions tunnel times of the order of $10^{-15}$s [31], which tells us that the transportation of one electron from one side of the junction to the other side costs time. We assume in this thesis for simplicity that this tunnel time is a constant.

If we model the junction with the classical circuit component: the capacitor, in which it is not possible for the electron to be between the plates, and we will use a certain tunnel time ($\tau_t \neq 0$) we imply that the electron is gradually transferred from one side of the junction to the other side.

In the derivation of the tunnel condition, the duration $\tau_t$ of the tunnel event and the shape of the current pulse $i_t$ are not yet determined. The only thing that is given is the exact charge that is transferred through the insulator: $e$, the charge of one electron.

During the derivation of the critical voltage (in section 4.1.2) the assumptions were made that all sources within the circuit are assumed to be constant during the tunnel event, and only one tunnel event occurs at the same time. As a consequence all the sources within the circuit, except the current source modelling the tunnel event, can be removed during the analysis of the circuit. The circuit attached to the current source modelling the tunnel events, can be described as a passive circuit.

Let $k_s$ be the number of zeros of the impedance and $k_p$ the number of poles. For the impedance seen from the current source which models a tunnel event (so including the capacitance $C_j$ of the junction), see figure 4.5, we can write in general (with $s = j\omega$)

$$Z_{cir}(s) = \frac{b_{k_s}s^{k_s} + b_{k_s-1}s^{k_s-1} + \ldots + b_1s + b_0}{a_{k_p}s^{k_p} + a_{k_p-1}s^{k_p-1} + \ldots + a_1s + a_0} \tag{4.16}$$

\footnote{According to [31] this tunnel time depends on the transmission probability of the electron (with an amount of energy) to tunnel through the tunnel barrier [15].}
which can be rewritten into

\[ Z_{\text{cir}}(s) = \frac{b_{k_s} (s - z_1)(s - z_2) \ldots (s - z_{k_s})}{a_{k_p} (s - p_1)(s - p_2) \ldots (s - p_{k_p})} \]  

(4.17)

Because poles \( p_d \) \((p_d \in \{p_1 \ldots p_{k_p}\})\) and zeros \( z_d \) \((z_d \in \{z_1 \ldots z_{k_z}\})\) only play a part when they are in the area of interest, which is for the tunnel current \( \omega_t = \frac{2\pi}{\tau_t} \), we can simplify this expression by neglecting some of the poles and zeros. Four types of substitutions are allowed in equation 4.17

- When \( |p_d| \gg \omega_t \)

\[ (s - p_d) \Rightarrow -p_d \]  

(4.18)

- When \( |z_d| \gg \omega_t \)

\[ (s - z_d) \Rightarrow -z_d \]  

(4.19)

- When \( |p_d| \ll \omega_t \)

\[ (s - p_d) \Rightarrow s \]  

(4.20)

- When \( |z_d| \ll \omega_t \)

\[ (s - z_d) \Rightarrow s \]  

(4.21)

If the expression still contains poles and zeros unequal to zero after the substitutions above, the shape and tunnel time play a part in the derived critical voltage.

For two situations, which will be discussed next, it is easy to show that the shape of the tunnel current \( i_t \) plays no part in the derivation of the critical voltage.

**Low ohmic environment**

In one of the extreme cases no poles or zeros are in the expression after the substitutions of equation 4.18 - 4.21. This is only possible in those situations where a small resistance is placed in parallel with the junction (after the voltage sources are replaced by a short and the current sources are replaced by an open). An example of such a circuit is a voltage biased junction (see figure 4.6) with a low ohmic series resistor. For the situations were a low ohmic resistor is placed in parallel with the junction we can write

\[ Z_{\text{cir}}(s) \approx R \]  

(4.22)

\[ u_j^{cr}(t = \tau_t) = \frac{1}{2} \mathcal{L}^{-1}\left\{ R\mathcal{L}\{i_t(t)\}\right\} \]  

(4.23)

\[ u_j^{cr}(t = \tau_t) = \left. \frac{1}{2} R i_t(t) \right|_{t=\tau_t} \]  

(4.24)

Because the tunnel current \( i_t \) is zero at \( t = \tau_t \), the critical voltage will always be

\[ u_j^{cr} = 0 \]  

(4.25)

It should be clear that due to a resistor in series with the junction, the voltage across the junction is a function of time, as is the moment the tunnel condition is reached.
The critical voltage for a capacitive circuit

For the case only one pole equal to zero is left after the substitutions of equation 4.18 - 4.21, the remaining circuit is a capacitive circuit. This means that the circuit can be modeled as completely capacitive. The circuit only consists in that case of (non-tunneling) junctions\(^2\), capacitors, and current sources and voltage sources which are constant during the tunnel event. For the impedance we can write

\[
Z_{\text{cir}}(s) = \frac{1}{C_{\text{eff}} s} \tag{4.26}
\]

In which \(C_{\text{eff}}\) is equal to the effective capacitance seen between the nodes at which the junction is connected in the analysed SET circuit (so including the capacitance of the tunnel junction). We can model the environment of the junction (see figure 4.5) as a capacitor \(C_e\) (see figure 4.7). This replacement capacitor can be found by calculating the capacitance between node 1 and node 2 without taking the capacitance of the junction into account.

\[
Y_e(s) = sC_e \tag{4.27}
\]

So

\[
C_{\text{eff}} = C_e + C_j \tag{4.28}
\]

For a capacitive circuit we can write for the critical voltage

\[
u_j^{cr}(t = \tau_t) = \frac{1}{2} \mathcal{L}^{-1}\left\{ \frac{1}{C_{\text{eff}} s} \mathcal{L}\{i_i(t)\} \right\} \tag{4.29}
\]

Because in general

\[
\frac{1}{s} \mathcal{L}\{g(t)\} = \mathcal{L}\left[ \int_0^t g(x)dx \right] \tag{4.30}
\]

\(^2\)A junction is modelled as a capacitor in parallel with a current source modelling the tunnel event. As long as no electron is tunneling, the junction is a linear component.
Figure 4.7: In the case of a capacitive circuit, the environment of the tunnel junction can be modelled by a capacitance $C_e$.

we can rewrite equation 4.29 into

$$w^c_j(t = \tau_t) = \frac{1}{2C_{\text{eff}}} \mathcal{L}^{-1} \left\{ \mathcal{L} \left\{ \int_0^t i_t(t) \, dt \right\} \right\}$$

(4.31)

$$w^c_j = \frac{1}{2C_{\text{eff}}} \int_0^{\tau_t} i_t(t) \, dt$$

(4.32)

Using the conditions of the tunnel current, which are

$$i_t = 0 \text{ for } t < t_a$$

(4.33)

$$i_t = 0 \text{ for } t > t_b$$

(4.34)

$$t_a - t_b = \tau_t$$

(4.35)

$$\int_{t_b}^{t_a} i_t(t) \, dt = e$$

(4.36)

we can rewrite equation 4.32 into

$$w^c_j = \frac{e}{2C_{\text{eff}}}$$

(4.37)

From equation 4.37 we conclude that the circuit has no time dependence making it possible to model the tunnel current $i_t(t)$ as

$$i_t(t) = e\delta(t)$$

(4.38)

In this way we will find for the critical voltage, using equation 4.15

$$w^c_j = \frac{e}{2(C_j + C_e)}$$

(4.39)

this is the same result as equation 4.37 and as can be obtained with the critical voltage derived in section 2.3.
Concluding

In most cases we do not have to know the exact shape of the tunnel current. In some cases we can neglect the tunnel time $\tau_t$, and calculate the circuit with $\tau_t \to 0$.

\[
\lim_{\tau_t \to 0} \int_{t_b}^{t_a} i_t(t) \, dt = c
\]

with $\tau_t = t_a - t_b$. This makes it possible to calculate the behaviour of a circuit using an approximation: the delta or dirac function shaped tunnel current.

\[
i_t(t) = e \delta(t - t_0) \bigg|_{t_0 = t_n = t_b}
\]

The cases when this approximation is allowed can be divided into three situations:

1. A very high Ohmic (junction) environment

\[
Z_{\text{cir}}(s) \approx \frac{1}{s C_j}
\]

\[
u_{jr}^c = \frac{e}{2 C_j}
\]

2. A very low Ohmic environment

\[
Z_{\text{cir}}(s) \approx 0
\]

\[u_{jr}^c = 0
\]

3. A purely capacitive environment ($C_e$)

\[
Z_{\text{cir}}(s) \approx \frac{1}{(C_e + C_j) s}
\]

\[
u_{jr}^c = \frac{e}{2 (C_j + C_e)}
\]

These simplifications will give rise to a neglectable small error in the critical voltage.

4.2.2 An example of neglecting the wire resistance

In figure 4.8a a double junction voltage biased circuit is shown. Let $C_{j1}$ be the capacitance of tunnel junction TJ$_1$ and $C_{j2}$ the capacitance of tunnel junction TJ$_2$. From a circuit point of view we would expect that when the resistance of the wire $R_w$ is very small we are allowed to neglect this resistance, in which case we obtain a purely capacitive circuit with a critical voltage of junction TJ$_1$ of

\[
u_{jr}^{c1} = \frac{e}{2 (C_{j1} + C_{j2})}
\]
Figure 4.8: a) An example circuit: a double junction structure excited with a voltage source with a wire resistance $R_w$. In this example we only examine tunnel junction TJ$_1$. b) In this example is shown how to calculate the impedance $Z_{cir}(s)$ ‘seen’ by the current source $i_{t1}$ modelling the tunnel event through TJ$_1$.

For the derivation see section 4.2.1.

For the impedance $Z_{cir}(s)$ seen by the current source $i_{t1}$ modelling the tunnel event through TJ$_1$ (shown in figure 4.8b) we can write

$$Z_{cir}(s) = \frac{sC_{j1}}{sC_{j1} + R_w + \frac{1}{sC_{j2}}}$$

(4.49)

A same kind of expression can be written for the other junction (TJ$_2$). For now we only investigate the tunnel condition of junction TJ$_1$. Which can be rewritten into

$$Z_{cir}(s) = \frac{1}{C_{j1}} \left[ \frac{s + \frac{1}{R_wC_{j2}}}{s \left( s + \frac{C_{j1} + C_{j2}}{C_{j1}C_{j2}R_w} \right)} \right]$$

(4.50)

Assuming the capacitance of both junctions to be in the atto-farad range and the resistor having a resistance of just a few ohms we can simplify this expression with the help of the substitutions of equations 4.18 - 4.21 into

$$Z_{cir}(s) = \frac{1}{C_{j1}} \left[ \frac{R_wC_{j2}}{s \left( \frac{C_{j1} + C_{j2}}{C_{j1}C_{j2}R_w} \right)} \right]$$

(4.51)

which is equal to

$$Z_{cir}(s) = \frac{1}{s \left( C_{j1} + C_{j2} \right)}$$

(4.52)

Which indeed gives us what was expected: an impedance which is purely capacitive, resulting in the critical voltage of equation 4.48.

It is easy to see that the case for a very large resistance of $R_w$ also gives the expected outcome, namely a junction which can be seen as isolated from its environment, hence

$$u_{j1}^c = \frac{e}{2C_{j1}}$$

(4.53)
4.2 Resistor and tunnel time

4.2.3 Shape of the tunnel current

In any useable circuit, resistors and time depending sources are involved. If in such a circuit, after the substitutions of equations 4.18 - 4.21 more than one pole is left, there is a need to know what the shape of the tunnel current pulse during the tunnel time is.

The choice for such a shape depends on the accuracy we need, and if we are using a simulator, which has discrete time steps. When using such a simulator we should neither use a discrete function (like the step function) nor a function with steep slopes to model the shape of the current, to make sure we do not have time step problems.

As an example of the difference in critical voltages, due to the different shapes of the tunnel current, we analyse a simple circuit: just a tunnel junction TJ with a resistor $R$ in series (figure 4.9). Let $C_J$ be the capacitance of the tunnel junction TJ. To analyse this circuit for a wide range of resistor values we have to assume a specific shape of the tunnel current. In this section we will show the difference obtained when choosing two different tunnel current shapes.

![Figure 4.9: A simple circuit consisting of a tunnel junction TJ with resistor $R$ in series.](image)

For this example two simple shapes are analysed:

1. The delta function with a dead-time $\tau_d$ (figure 4.10a).
2. The block shaped current pulse (figure 4.10b).

For these shapes we derive the relation between the critical voltage and the series resistor. Both current shapes are discussed below.

In the first example we assume that the tunnel current is just a delta shaped function, with a dead-time, equal to $\tau_d$. This dead-time is in case of a delta shaped function equal to the total tunnel time $\tau_t$ (see figure 4.10a). For the tunnel current $i_t$ we can write

$$i_t(t) = e \delta(t)$$

which results (using equation 4.15) in

$$u_j^c(t = \tau_t) = \mathcal{L}^{-1} \left\{ \frac{e}{2s + \frac{1}{RC_j}} \right\}_{t = \tau_t}$$

This is equal to

$$u_j^c(t) = \frac{e}{2C_J} \exp \left( -\frac{\tau_t}{RC_J} \right)$$

---

3 For an implementation in a simulator we could use for example a sin-form shape or a parabolic shape, both not discussed in this thesis.
Figure 4.10: a) The delta shaped tunnel current with a dead-time $\tau_d$ and b) the block shaped tunnel current. Both are in agreement with equation 4.10.

This gives a plot like drawn in figure 4.11a.

For the second example we assume that the tunnel current is a block pulse shaped current

$$i_t(t) = \frac{e}{\tau_t} \{ \epsilon(t) - \epsilon(t - \tau_t) \} \quad (4.57)$$

which results (using equation 4.15) in

$$u_{j\tau}^c(t = \tau_t) = \left. \left\{ \frac{eR}{2\tau_t} \left( 1 - \exp \left( -\frac{\tau_t}{RC_j} \right) \right) (\epsilon(t) - \epsilon(t - \tau_t)) \right\} \right|_{t = \tau_t} \quad (4.58)$$

This is equal to

$$u_{j\tau}^c(t) = \frac{eR}{2\tau_t} \left( 1 - \exp \left( -\frac{\tau_t}{RC_j} \right) \right) \quad (4.59)$$

This gives a plot drawn in figure 4.11b.

In the limiting cases $R = 0$ ($u_{j\tau}^c = 0$) and $R \to \infty$ ($u_{j\tau}^c = \frac{e}{2C_j}$) the results obtained are the same as predicted by the Orthodox theory (as was described in section 2.4). But the calculations in this section also give a well defined result for finite non-zero values of $R$ which depends on the chosen shape of the tunnel current!

### 4.2.4 Current behaviour

In the current regime, outside the Coulomb blockade, the electron will tunnel. Between the tunnel events there is a certain wait time $\tau_w$ shown figure 4.12a (also see section 3.1.4). When we calculate the current through a tunnel junction we are not allowed to use the substitution of equation 4.18 - 4.21, because this current will give a voltage drop across a resistor. Such a voltage drop decreases the voltage across the junction, and thus changes the wait time (see section 3.1.5).

The wait time is usually much bigger than the tunnel time $\tau_t$. In those cases we can neglect the tunnel time $\tau_t$, and model the tunnel current with a delta function multiplied by an elementary charge $e$ (figure 4.12b).

This does not change the critical voltage nor does it tell us if we are allowed to remove the resistor from the circuit, this simplification can only be used for the calculation of high currents.
Figure 4.11: The critical voltage $u^c_j$ as a function of the resistor $R$ in series, for a tunnel current that is a) delta shaped with a dead-time or b) block shaped. We assumed the tunnel time to be $\tau_t = 1 \cdot 10^{-15}s$ and the junction capacitance $C_j = 1\alpha F$.

Figure 4.12: a) Definitions of different times during the tunnel process. b) the tunnel time $\tau_t$ is neglected.

4.3 Conclusions

The tunnel condition, which needs to be satisfied before an electron can tunnel, is expressed in two local voltages. This can be simplified in one voltage condition: the critical voltage. The critical voltage is the maximal voltage across the junction, such that no electron is allowed to tunnel. To include the effect different resistor values will have on this critical voltage, a non-vanishing tunnel time needs to be introduced. This tunnel time is assumed to be constant namely $10^{-15}s$ [31]. Some simplifications of the circuit can be done when components introduce time constants, which are much larger or smaller than this tunnel time.
Part II

Circuit design methodology
Some scientists claim that hydrogen, because it is so plentiful, is the basic building block of the universe. I dispute that. I say there is more stupidity than hydrogen, and that is the basic building block of the universe.

Frank Zappa

5

The design of functional blocks

With the help of the models and simplifications described in the previous chapters we are able to build blocks to implement a certain function. One of the main functions often discussed is amplification. In this chapter we show how we can obtain desired functions like signal amplification.

The approach used in this chapter is to investigate the input-output relation of a certain structure. How the input-output relation can be synthesized or changed is not discussed in this chapter. The obtained input-output relation of SET circuits is usually expressed in capacitance values of which the structure is build. In chapter 6 we will discuss one of the main features of the input-output relation when analysing SET circuits: periodicity, and how we can synthesize structures when using this periodicity. For now we just assume we have a structure, which has a desired part within its input-output relation.

The type of input-output relation we obtain depends on the signal where the information is coded in. In circuit design it is common to use input and output currents or voltages, which leaves us with four different input-output relations. Depending on which behaviour we are looking for, a choice can be made between these different input-output relations, only one can be used at the time.

The interesting part of the input-output relation, the part we want to operate in, is what we will call the operating window. After the input and output signal quantities are chosen the input-output relation should be shifted by applying bias sources, in such a way that the interesting part fits inside the operating window. In this chapter we will discuss the biasing needed to be able to use the operating window.

After we have designed the basic function blocks, also called sub-circuits, we need to couple them to obtain a larger circuit. This coupling is the topic of chapter 8.

This chapter starts with choosing the physical quantity to carry the information. After which we discuss the biasing in the second section. In the third section one of the possible sub-system functions is described: amplification of signals. We end this chapter with some conclusions.

In this chapter \(\zeta_{\text{in}}\) is the designated input signal and \(\zeta_{\text{out}}\) is the designated response signal. We will assume that initial island charges, which were modelled by a current
source as was described in section 3.2.4, do not affect the input-output relation for \( t \geq 0 \). And we assume that the purely capacitive, voltage driven, circuits settle at \( t = 0 \) and immediately after each tunnel event (due to the lack of resistive components).

\[ \text{5.1 Information signals} \]

We have many options in choosing the input and the output signals shape and quantity of the circuit to be implemented. To obtain the maximum design freedom we do not restrict ourselves to choosing a signal quantity as a first design step. Depending on which input-output relation we want, we chose the input and output quantities.

When there are more input-output relations containing the desired behaviour we can chose the physical quantity based on certain advantages the quantity has above another quantity. The disadvantages of current and charge as signal quantity is discussed in section 5.1.2.

For a larger circuit the input quantities of the present stage should be equal to the output quantities of the previous stage. In the design of functional blocks, discussed in this chapter and in chapter 6, we will not limit our design by this demand. When the coupling of all the implemented functions is discussed (chapter 8) the desired signal transformation from one quantity to another is discussed, and implemented in so called coupling-blocks.

\[ \text{5.1.1 Useable signal space} \]

Let \( \Delta \zeta_{\text{in}} \) be the total range of values of the input signal that the device can still process correctly, and let \( \Delta \zeta_{\text{out}} \) be the range of values the input signal will use for the information (see figure 5.1). In general the range of values of the information signal \( \Delta \zeta \) should be less than the possible range of the signal values \( \Delta \zeta \), so in this case

\[
\Delta \zeta_{\text{in}} \leq \Delta \zeta_{\text{out}}
\]

(5.1)

Let \( \zeta_{\text{in}}^{\text{max}} \) be the maximal value the input information signal will have, and \( \zeta_{\text{in}}^{\text{min}} \) the minimal value the input information signal will have, then we can write

\[
\Delta \zeta_{\text{in}} = \zeta_{\text{in}}^{\text{max}} - \zeta_{\text{in}}^{\text{min}}
\]

(5.2)

The part of the (non-linear) input-output relation that is used will be called signal window in the rest of this thesis.

**Definition 5.1** A signal window is the part of the total input-output relation, which consists of the relation between the limited range of possible input values \( \Delta \zeta_{\text{in}} \) and their corresponding range of output values \( \Delta \zeta_{\text{out}} \).

The width of such a signal window (as drawn in figure 5.4) is equal to the range of possible input values of the limited input signal \( \Delta \zeta_{\text{in}} \) applied to the building block.

Opposed to standard electronics, like the bipolar junction transistor (BJT) or the field effect transistor (FET), which can be driven into saturation when the input signal or the bias signal is chosen too large, the amplitude of the signals is not limited in the case of SETs \((-\infty < \zeta_{\text{in}} < \infty)\). The signals are only limited due to the thickness
of the oxide through which the electrons tunnel. Hence the applied signals should not cause a voltage across the junction higher than the breakthrough voltage. Such a voltage will destroy the SET junction permanently.

Large signals should not be used for a different reason: Because SET circuits consist mainly of capacitors, large signals will cause a non-neglectable signal on many nodes in the circuit, because every node is coupled capacitively to the others (a big problem in SET circuits, see also appendix E).

5.1.2 Signal domain

Up to now most SET circuits that are designed consist mainly of capacitors\textsuperscript{1}. For capacitive circuits the physical quantity chosen as a signal carrier can be voltage, current, or charge. The tunnel condition is expressed in voltages. When we apply a current signal to the circuit, this current will charge the capacitance of the SET junction, and hence the moment of tunneling will be time dependent. This should be taken into account when designing with current sources.

Sub-circuits, which have charge as an output signal, have a problem with coupling to the next stage. In figure 5.2a an example is drawn of a sub-circuit which has two types of output: an independent island charge output \( q_i \) and a voltage output \( u_{\text{out}} \), both showing a different behaviour (this type of sub-circuit is discussed in more detail in section 9.2).

Let \( C_j \) be the capacitance of the tunnel junction TJ. The input-output voltage relation is a periodic function (figure 5.2b), with a period equal to \( \frac{e}{C_r} \). After one period an extra electron tunnels to the island through the tunnel junction TJ, and by doing so it decreases the island charge \( q_i \), as is shown in figure 5.2c. As a consequence the island charge \( q_i \) can be seen as the integer number of the division of the input voltage \( u_{\text{in}} \) by the sub-circuit constant \( \frac{e}{C_r} \) (multiplied by \(-1\)). The output voltage \( u_{\text{out}} \) is equal to the remainder of this division, with an offset of

\[
    u_0 = \frac{e}{2(C_c + C_j)}
\]

This offset can be tuned by a biasing scheme, see section 5.2.

\textsuperscript{1}Junctions through which no electron tunnels, are also modelled as capacitors.
Figure 5.2: a) A 'mod-div'-function implemented by an electron-box. b) One of the input-output relations: the output voltage is the remainder (with an offset $u_0$, see equation 5.3) when the input voltage is divided by the sub-circuit constant $\frac{e}{C_c}$. c) Another input-output relation: the independent island charge $q_i$ equals the integer number of the division (multiplied by minus one).

A problem with the information placed in the island charge is the transfer to the next stage. It is not possible to connect the next stage directly. A solution is the conversion of this island charge into a voltage; in that case an extra capacitor is needed. The problem that then arises is how to get the island charge on the capacitor without destroying the basic idea behind the sub-circuit. Another problem of this extra capacitor is the influence it has on the behaviour of the sub-circuit, for instance the critical voltage is changed.

Concluding: Charge is not a quantity we can use directly and current as signal carrier will give time depending tunnel events. For those reasons we prefer voltages as physical quantity for the information carrier.

### 5.2 Biasing

In the literature it is common to speak of a DC operating point, this is the point on the input-output relation for which holds: $\dot{q}_{in} = 0$, see figure 5.3.

**Definition 5.2** Biasing a circuit is shifting the origin of the axes of the input-output relation to the chosen operating point, by adding DC sources [125].
5.2 Biassing

A circuit is only in its DC operating point when all signals are zero. After we determined the desired operating window we should bias the circuit such that it will be in the desired DC operating point when no signals are applied.

Figure 5.3: In the case of $\tilde{\zeta}_{\text{in}}^{\min} = -\tilde{\zeta}_{\text{in}}^{\max}$, the DC operating point will be in the (horizontal) middle of the operating window.

5.2.1 Operating window

Let the maximal input signal that carries information be $\tilde{\zeta}_{\text{in}}^{\max}$, and the minimal input signal be $\tilde{\zeta}_{\text{in}}^{\min}$ (see also figure 5.1), which are assumed to be known by the designer. Then those information signals form a defined, so called, signal window, as shown in figure 5.4. The width of this window is limited by the input signals and is equal to $\Delta \tilde{\zeta}_{\text{in}}$ (see figure 5.4). While the height of the signal window ($\Delta \tilde{\zeta}_{\text{out}}$) is determined by the maximal and minimal output signals reached within the signal window (this height can change when the input-output relation within the window changes).

The complete input-output relation, the relation between all possible inputs $\zeta_{\text{in}}$ and outputs $\zeta_{\text{out}}$, can show an interesting behaviour somewhere. If we want to use this interesting part of the input-output relation for the function of our building block we should make sure that this relation is mapped onto the signal window. We capture the desired behaviour in a so called operating window (see figure 5.4).

**Definition 5.3** An operating window is defined as the desired input-output relation that should be mapped onto the signal window using bias sources.

The width of the operating window is equal to the width of the signal window (see figure 5.4), which will only be a small part in the range of all possible inputs.

By defining the window in this way we are sure that the device or sub-circuit, with a certain input-output relation, will not operate outside this window, hence the name operating window. A disadvantage of defining the operating window in this way is that we need a priori the maximum and minimum input signals.
Figure 5.4: An example of an input-output relation, in which we can define an operating window in such a way that the device will have a behaviour as an inverter.

Because we only use a small part of the functionality of the complete input-output relation we are able to simplify the expression for the used input-output relation. We are now also able to use the same type of device or sub-circuit (with a known input-output relation) for different functions, just by placing the operating window on different parts of the input-output relation. In this way we are able to design building blocks which can change from function by just adjusting the bias source, making the functions programmable [76] (discussed in more detail in section 9.2.1).

5.2.2 Horizontal and vertical shifts of the input-output characteristic

The input-output relation (for example figure 5.5a) can be shifted using extra sources. A horizontal shift can be obtained by using an extra input signal (see figure 5.5b). A vertical shift can be obtained when an extra signal is added to the output signal (see figure 5.5c).

In the case of figure 5.4 we should shift the input-output relation in a horizontal direction such that the chosen operating window falls within the signal window. The begin point $\zeta_0$ of the operating window should be mapped on the minimal input signal $\zeta_{in}^{min}$. So this shift can be reached by adding an input bias signal $\zeta_{b,h}$ equal to

$$\zeta_{b,h} = \zeta_0 - \zeta_{in}^{min}$$  \hspace{1cm} (5.4)

A series voltage source can be used when the input signal $\zeta_{in}$ quantity is a voltage ($u_{in}$). A parallel current source can be used when the input signal quantity $\zeta_{in}$ is a current ($i_{in}$). A vertical shift at the output can be obtained, in case of an output voltage, by adding a series output voltage source. In case of an output current, a vertical shift can be obtained by a parallel output current source.

Let $H_{uu}$ be the input voltage - output voltage relation, and let $H_{ii}$ be the input current - output current relation. The extra DC source for the vertical shift and the
Figure 5.5: a) An example of an input-output relation. b) Due to an extra input signal $\zeta_h$, a horizontal shift occurs. c) When an extra output signal $\zeta_v$ is added to the output signal a vertical shift occurs.

extra DC source for the horizontal shift are both called bias sources, see figure 5.6a for the case of an input-output relation $H_{uu}$ and figure 5.6b for the case of an input-output relation $H_{ii}$. But also the two combinations, input voltage - output current and input current - output voltage, both not drawn, are possible.

The bias sources together with the original function $H$ will form a new input-output relation $H^*$.

5.2.3 Bias Implementations

A voltage bias source in series, so without one side of the source connected to ground, is hard to implement in realistic bias schemes.

In case of a current bias scheme a bias current source with one side connected to ground can be achieved using the current source transformation (already discussed in section 3.2.5). For that reason we will not go into more detail about this. So we will focus on the implementation of a voltage bias scheme.

The first step to change the positions of the bias sources is the transportation of the voltage sources. Voltage sources in a circuit can be transported using the voltage source transportation (also known as Blakesly transformation, the E-shift [96, 105], or v-shift [22]) as shown in figure 5.7.

A horizontal shift due to $u_{b,h}$

For example the sub-circuit shown in figure 5.8a is biased with $u_{b,h}$. For simplicity we assume no independent charge on the middle node (node $w$ in figure 5.8a). Let $C_j$
Figure 5.6: The new input-output relation $H^*$ includes also a) the bias voltage sources or b) the bias current sources.

Figure 5.7: The voltage source transportation.

be the capacitance of the tunnel junction TJ and $C_\Sigma = C_{in} + C_b + C_j$ then we can write for the output voltage

$$u_{out}(t) = \frac{C_{in}}{C_\Sigma} (u_{in}(t) + u_{b,h}(t)) \quad (5.5)$$

Hence, as long as no tunneling occurs the input-output relation is equal to

$$H = \frac{C_{in}}{C_\Sigma} \quad (5.6)$$

In most applications it is hard to realise a voltage source that is not connected on one side to ground. The bias source $u_{b,h}$ (figure 5.8a) can be transformed into a current source $i_{b,h}$ using its norton equivalent (figure 5.8b).

$$i_{b,h}(t) = L^{-1}\left\{ sC_{in}U_{b,h}(s) \right\} \quad (5.7)$$

This current source can also be drawn parallel to capacitor $C_b$ because $u_{in}$ is independent of $i_{b,h}$ (figure 5.8c).
Using the Thévenin equivalent we can transform the current source $i_{b,h}$ back into a voltage source $u_{b,he}$ in series with $C_b$ (figure 5.8d), with

$$u_{b,he}(t) = \frac{C_{in}}{C_b} u_{b,h}(t)$$  \hspace{1cm} (5.8)

When we assume $C_{in} = C_b$ the bias source $u_{b,h}$ in series with the signal source $u_{in}$ can also be placed in series with capacitor $C_b$.

![Figure 5.8](image)

Figure 5.8: a) An example sub-circuit biased with a voltage source $u_{b,h}$. b) Using the norton equivalent of $u_{b,h}$ which is $i_{b,h}$. c) Because $i_{b,h}$ is independent of $u_{in}$ the current source $i_{b,h}$ can be drawn parallel to $C_b$. d) Using the Thévenin equivalent gives us the commonly used bias scheme.

**Conclusion:** We can change the position of the series input bias source $u_{b,h}$ (see figure 5.8a), which is hard to implement in practical circuits, to a position in which the bias source has one side connected to ground. This can be achieved by placing the source in series with an extra capacitor $C_b$ (see figure 5.8d), with $C_b = C_{in}$.

The bias scheme has no influence on the slopes or on the tunnel condition for the junction. In the example given this means that the maximal output voltage is still $u_j^{cr}$.

It can easily be proven that the same holds when we want to attach to the sub-circuit more input signal voltage sources. Each extra input can be attached by a capacitance $C_{in}$. The only thing that is changed in the circuit is $C_{Σ}$. 
A vertical shift due to $u_{b,v}$

Another bias source is the bias source $u_{b,v}$ which causes a vertical shift of the operating window. An example sub-circuit is drawn in figure 5.9a. The output voltage is equal to

$$u_{out}(t) = u_{b,v}(t) + \frac{C_{in}}{C_{\Sigma}} u_{in}(t) \quad (5.9)$$

By using the voltage source transportation (see figure 5.7) we obtain figure 5.9b. All three voltage source $u_{b,v}$ shown in figure 5.9b can be transformed into current sources using the Thévenin equivalent (see figure 5.9c) using Laplace, with

$$i_{b,v1}(t) = \mathcal{L}^{-1}\left\{sC_b U_{b,v}(s)\right\} \quad (5.10)$$

$$i_{b,v2}(t) = \mathcal{L}^{-1}\left\{sC_j U_{b,v}(s)\right\} \quad (5.11)$$

$$i_{b,v3}(t) = \mathcal{L}^{-1}\left\{sC_{in} U_{b,v}(s)\right\} \quad (5.12)$$

Due to the fact that $u_{b,v}$ is independent of $u_{in}$ we can add all three current sources, and replace them by one current source $i_{b,ve}$ (using $C_\Sigma = C_{in} + C_j + C_b$) as shown in figure 5.9d.

$$i_{b,ve}(t) = i_{b,v1}(t) + i_{b,v2}(t) + i_{b,v3}(t) = \mathcal{L}^{-1}\left\{sC_\Sigma U_{b,v}(s)\right\} \quad (5.13)$$

This current source can be transformed back into a voltage source using its Thévenin equivalent (see figure 5.9e)

$$u_{b,ve}(t) = \frac{C_\Sigma}{C_j} u_{b,v}(t) \quad (5.14)$$

This voltage source should be shifted outside the two nodes between which the junction voltage $u_j$ is measured (see figure 5.9f).

The two floating voltage sources, which are in the loop of $u_j$ and TJ can be added together

$$u_{b,ju}(t) = u_{b,ve}(t) - u_{b,v}(t) = \frac{C_b + C_{in}}{C_j} u_{b,v}(t) \quad (5.15)$$

This is drawn in figure 5.9g.

Because the voltage source $u_{b,ju}$ can not easily be implemented, it is commonly neglected (figure 5.9h). This causes that the vertical shift of the complete input-output relation is unequal to $u_{b,v}$. The starting point ($u_{in} = 0$) is lifted with the amount of $u_{b,v}$, due to the extra bias source $u_{b,ve}$, but the output voltage where one electron can tunnel ($u_{out}^{cr}$) is not the desired $u_j^{cr} + u_{b,v}$ but is now due to the neglecting of the voltage source $u_{b,ju}$ equal to $u_j^{cr} + u_{b,ve}$. As long as no electron tunnels the desired vertical shift is obtained. When an electron tunnels the error made is equal to $u_{b,ju}$ (see figure 5.10), as was expected.

Due to the change in output voltage when the electron is allowed to tunnel, the input voltage $u_{in}$ necessary to cause such a tunnel event is also different, as can be seen by the horizontal shift in figure 5.10.

**Concluding:** We can replace the output series bias source $u_{b,v}$ (see figure 5.9a), which is hard to implement in practical circuits, by a voltage source (with a different
Figure 5.9: a) An example sub-circuit biased with a voltage source \( u_{b,v} \). b) Using the voltage source transportation on the circuit it will result in three voltage sources \( u_{b,v} \). c) Using the Norton equivalent we can transform the three voltage sources, which are directly in series with capacitances (or the junction), into three current sources. d) The three current sources can be replaced by one current source, because they are independent of \( u_{in} \). e) This current source can be transformed back into a voltage source. f) The voltage source is shifted outside the two nodes between which the junction voltage \( u_j \) is measured. g) The complete new bias scheme. h) Bias scheme when neglecting the voltage source \( u_{b,jv} \). This will give a change in the critical output voltage.
Figure 5.10: A simulation (done with SIMON [131]) result of figure 5.9h with $C_b = 2aF$, $C_{in} = 3aF$, $C_j = 1aF$. A vertical shift equal to $u_{b,v}$ is obtained, as can be seen between two slopes. Because the source $u_{b,j,v}$ is neglected in figure 5.9h an extra error equal to this voltage is obtained after an electron tunnels for situation a) and is compensated again when an electron tunnels in situation b). With the component values we can calculate $u_{b,v} = 3.3mV$ and $u_{b,j,v} = 16.67mV$, which is indeed the outcome of the simulation. An extra shift occurred due to the fact that for $u_{in} = 0V$ the critical voltage is already reached for the SET junction ($u_{j,c} = \frac{\phi}{2C_j} > \frac{C_{in} + C_b}{C_j} u_{b,ve}$), hence an electron tunnels through the junction. This causes the output at $u_{in} = 0V$ to be $u_{out} = \frac{C_j}{C_j + u_{b,ve}} + \frac{\phi}{C_j} = 30mV$.

value) placed in series with the tunnel junction TJ (as shown in figure 5.9h). As a consequence of the neglecting of one voltage source, the voltage at the output at which an electron can tunnel is also changed with $u_{b,j,v} = u_{b,v} + u_{b,j,v}$. Using the scheme discussed in the previous section the undesired horizontal shift can be compensated.

Applying this kind of bias scheme to the electron-box example will shift the whole graph in horizontal and vertical direction. The slopes and the voltage drop due to a tunnel event are unaltered. Also the tunnel condition expressed in the voltages across the junction is not changed.

### 5.2.4 Multiple operating windows

Due to the discrete behaviour of electron tunnel events in SET junctions or due to multi-level signals, more than one operating window can be used (see for example figure 5.11a). A jump from one window to the next can be implemented by the effect
Table 5.1: All possible situations for the 2-input EXOR function. The numbers of the operating windows are those used in figure 5.11a.

<table>
<thead>
<tr>
<th>$\zeta_{in,1}$</th>
<th>$\zeta_{in,2}$</th>
<th>$\sum \zeta_{in}$</th>
<th>operating window</th>
<th>$\zeta_{out}$</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
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<td>0</td>
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<td>1</td>
<td>1</td>
<td>2</td>
<td>2</td>
<td>0</td>
</tr>
</tbody>
</table>

of a tunnel event or by discrete levels of the input information signal $\tilde{\zeta}_{in}$ which are separated by a forbidden gap (the space between two operating windows).

In figure 5.11 an example is drawn. In this figure we assume that the input $\tilde{\zeta}_{in,1}$ and $\tilde{\zeta}_{in,2}$ are digital signals (which have discrete amplitude levels). The sum of these input signals is taken (called $\Sigma \tilde{\zeta}_{in}$), see figure 5.11d. This summed information signal is fed as an input signal (see figure 5.11c) to the input-output relation $H$ which has three operating windows. The resulting output (figure 5.11b) shows the behaviour of an EXOR function (see table 5.1). This is graphically determined in figure 5.11a-c. The width of the operating windows determines the allowed amount of fluctuations on the amplitude of the input signals.

Figure 5.11: a) An example of an input-output relation with four operating windows. The number in the operating window indicates the sum of the inputs that are high. b) The belonging output signal when c) is applied as an input. d) An overview of the system under consideration. When both inputs ($\tilde{\zeta}_{in,1}$ and $\tilde{\zeta}_{in,2}$) are 'high' the sum is '2', which results in a low output, hence the name EXOR function.
5.3 Signal amplification

One of the basic functions that need to be implemented in basic building blocks is amplification. It is claimed in some literature [50] that SET structures have only a limited amount of amplification. In this section we will discuss amplification in SET structures.

Definition 5.4 The amplification $\mathcal{A}$ of a system biased in a given operating point is the relative response of a small variation of the input information signal (which is the output information signal $\Delta \tilde{\zeta}_{\text{out}}$) expressed in the same variation\(^2\) of the input information signal ($\Delta \tilde{\zeta}_{\text{in}}$) itself\(^3\).

$$\mathcal{A} = \frac{\Delta \tilde{\zeta}_{\text{out}}}{\Delta \tilde{\zeta}_{\text{in}}} \quad (5.16)$$

By this definition it is also possible to speak of amplification while the signal is not amplified but weekend ($\mathcal{A} < 1$). An amplification larger than one will be obtained when the variation of the output signal $\Delta \tilde{\zeta}_{\text{out}}$ divided by the variation of the input signal, $\Delta \tilde{\zeta}_{\text{in}}$ is larger than one. The relation between the input signal and the output signal can be discrete or continuous.

Amplification always involves transfer of energy from one place to another. To get an amplification of a signal, the energy should be delivered by any bias source.

A remark should be made here: due to definition 5.4 it is impossible to speak of amplification when two different physical quantities are compared, this is excluded by the definition above. In the case of SET circuits we can investigate three types of amplification

1. Voltage $u$: $\Delta u_{\text{out}} = \mathcal{A}_u \Delta u_{\text{in}}$

2. Current $i$: $\Delta i_{\text{out}} = \mathcal{A}_i \Delta i_{\text{in}}$

3. Charge $q$: $\Delta q_{\text{out}} = \mathcal{A}_q \Delta q_{\text{in}}$

If figure 5.12a a part of an input-output relation is shown. For the amplification $\mathcal{A}$ we can also write $\mathcal{A} = \tan(\varphi)$. Amplification $\mathcal{A} > 1$ can only be found when the input-output relation, which is the relation between the input signal $\zeta_{\text{in}}$ and the output signal $\zeta_{\text{out}}$, shows a slope (within the operating window) with an angle of more than $\frac{\pi}{4}$. The maximal amplification will be obtained when $\varphi = \frac{\pi}{4}$.

5.3.1 Voltage amplification

In general most proposed SET circuits would consist of junctions, capacitors, bias sources and independent island charges. Only in the case when the bias sources and the independent island charges are zero, and the tunnel condition is not met (so no electron will tunnel), we will obtain a linear input-output relation.

A SET circuit contains at least one SET junction. SET junctions can be modelled by a combination of a linear capacitor and a current source (modelling the tunnel

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\(^2\)The output variation can appear at a different moment in time with respect to the input variation.

\(^3\)By this definition a one-port cannot be described in terms of amplification.
event), see the junction model described in section 3.1. When the tunnel condition is not met, the current source can be left out, making the circuit a passive capacitive circuit. The relation between a variation at the output and the variation at the input ($A$) will always be less than one (see figure 5.12a), $A < 1$.

It is possible that island charges and bias sources are available in the circuit, but they only contribute to a shift in the input-output relation (see figure 5.12b), making it non-linear, but the slope which is a measure of the amplification remains the same: $\varphi < \frac{\pi}{4}$.

![Figure 5.12](image)

Figure 5.12: Graphical presentation of the input-output relation, the slope is a measure of the amplification. a) The linear input-output relation and b) the non-linear input-output relation.

Only in those cases in which the island charge is changing within the operating window we can obtain amplification $A > 1$. Such a change in charge makes the input-output relation (discrete) non-linear. To show such an amplification we analyse as an example the circuit of figure 5.13, in which $u_{in}$ is the input information signal and $C_j$ the capacitance of the tunnel junction TJ, we will obtain for the output information voltage $u_{out}$

$$u_{out}(t) = u_{in}(t) \frac{C_j}{C_j + C_c} - u_{bias}(t) \frac{C_j}{C_j + C_c} + q_i \epsilon(t) \frac{1}{C_j + C_c}$$

(5.17)

![Figure 5.13](image)

Figure 5.13: A simple circuit which can have amplification of $A > 1$ due to changes in the island charge $q_i$ as a consequence of tunnel events through the SET junction TJ.

When we assume that there are no initial or background charges we will obtain an input-output relation like drawn in figure 5.14. When we choose the operating
window in such a way that within this window the critical voltage is reached and thus a tunnel event can occur, we are able to obtain \( u_{\text{out}} > u_{\text{in}} \) and thus \( A > 1 \). Linear amplification of \( A > 1 \) can not be obtained outside the operating window (so the region in which no tunnel event can occur), because only capacitive dividing plays a role there, making the amplification \( A \) always less than one.

![Diagram](image)

Figure 5.14: The input-output relation of an electron-box (drawn in figure 5.13). By choosing an appropriate operating window a non-linear amplification of \( A > 1 \) can be obtained.

When we assume a delta function multiplied by the electron charge to model the tunnel current, a step in the input-output relation can be obtained. The tunnel event will now cause within the drawn operating window a slope of \( \varphi = \frac{\pi}{2} \). Which makes the amount of amplification of this type of input-output relation theoretically unlimited (\( A \to \infty \)). In practical cases the amplification is limited (\( A \) will be finite) due to a tunnel time unequal to zero and the environment that can contain resistors.

**Concluding:** By choosing a correct operating window we are able to get \( u_{\text{out}} > u_{\text{in}} \). For an amplification with \( A > 1 \) in SET circuits we need tunneling of electrons to/from an island.

### 5.3.2 Basic blocks

The conclusion about amplification, drawn in section 5.3.1, is that we need an island to obtain an amplification of \( A > 1 \), and a separate input and output. When designing circuits that are as simple as possible, and satisfy the obtained condition for amplification with \( A > 1 \), we obtain four different circuits, drawn in figure 5.15. These four is what we will call in this thesis: building blocks of type 1. In this thesis these blocks are indicated with the number 1.

A big disadvantage of these four building blocks is the fact that the island (middle node) is directly influenced by the attached building block due to the fact that it is the output node.

When using a floating node (called island), which is independent of the attached building block, we can distinguish eight different circuits, drawn in figure 5.16. These eight different building blocks will be called in this thesis: building blocks of type 2. In this thesis these building blocks are indicated with the number 2.

Not all of the in figure 5.15 and in figure 5.16 drawn building blocks are of interest for circuit design. For example amplifications can only be obtained when the independent charge on the island can be changed. When there is no junction in the
Figure 5.15: Basic building blocks of type 1: The simplest possible basic configurations with one island that is also the output node (so amplification of $A > 1$ is possible), which can be made with SET junctions and capacitors. With a) a pure capacitive network, b) two SET junctions in series, and c) and d) the electron-box.

circuit, see figure 5.15a and figure 5.16a, the island charge can not be changed (only by unwanted phenomena like random background charge). In this case we can not get any amplification making such a building block less interesting.

Another example of a less interesting basic building block for circuit design are those blocks where a junction is placed in series with the input, like in figure 5.15b, and d and in figure 5.16b, e, f, and g; because electrons can flow from the input source. In most situations this is unwanted, in those cases the electrons should be delivered by the previous stages. When we have a building block design method, like described in chapter 8, the less impact the second stage has on the first, the easier the design.

This leaves us with two types of basic blocks

1. The single junction connected to two capacitors (figure 5.16c,d), which is a type of electron-box structure as was drawn in figure 5.15c.

2. Two SET junctions in series with an input capacitor (figure 5.16h), known as the C-SET transistor. This structure has as a disadvantage the fact that two junctions are placed in series, parallel to the output (see figure 5.16h). Therefore it is possible for an output current of many electrons to flow. Making it power consuming but less sensitive for stochastic behaviour of a single tunnel event.

When the basic blocks of figure 5.15 and 5.16 are used in a circuit, the basic block can be enlarged with an extra capacitor to the island, for biasing or an extra input as was discussed in section 5.2.3.

5.4 Conclusions

When the complete input-output relation of a basic block is known, a desired region within this input-output relation should be selected called the operating window. With the knowledge of the possible input signals a signal window can be defined. By
biasing the basic block the operating window can be shifted on to the signal window, due to which the basic block operates in the desired region of the input-output relation.

One of the desired input-output relations is the region in which voltage amplification can be obtained. Only structures with (at least) one island and (at least) one SET junction connected to it show the desired voltage amplifications in their input-output relations.
In this chapter the periodic behaviour, which is a characteristic of the combination of the new circuit elements: the SET junction and the island, is discussed. Two properties are valid for SET circuits build with both circuit elements; 1) only an integer number of electrons can tunnel, and 2) charge can be stored on an island. As we will show in this chapter these two properties together result in a periodic response. The periodic behaviour gives rise to a new way of designing circuits.

Up to now most of the (digital) SET circuits discussed in the literature are a transformation from the standard CMOS logic [20, 68, 115], in which many SET junctions are needed. We propose another way of designing. We use the special features of SET junctions and floating nodes (islands), and combine these with the features of known components, CMOS transistors, BJT, etc, to come to the best (fastest, smallest, etc) solution of a large problem. So, instead of trying to compete with standard well known components like CMOS FETs we should use the difference in behaviour in our design with SETs. For instance: buffering and amplification can best be done by standard components. So in this chapter we will answer the question: what can we do with one of the basic behaviours of the SET junction: the periodic behaviour, which is not easy to do with well-known components?

Periodicity can give us extra functionality. It is hard (it takes up a lot of chip area) to build a structure with standard components that has a periodic relation between the input and the output. By using the periodicity of the SET junction it is possible to accomplish the same digital function with a different structure than the standard CMOS, making the total structure much smaller and less power consuming.

Only a few other people use the periodic behaviour of the device for design purposes. Examples of the use of this periodicity are

- Weight factors of neural nets [48]
- Fault tolerance by using periodicity as redundancy [90]

In the first section we distinguish between three types of periodicity that can be used in circuits. In the second section we explain the origin of the periodicity of SET
circuits. Because modulo functions can easily be made with the help of the periodic SET behaviour, we discuss modulo functions and its applications in the third section. In this third section we will discuss the EXOR function as an example application of the modulo function. The EXOR function can be made with a large number of SET junctions when the structure is based on the standard CMOS solution. Or one single junction, using its periodic behaviour, can implement an EXOR function. We end this chapter with some conclusions.

In this chapter we assume that there are no fluctuating background charges during the operation of the proposed SET structures, solutions for the random background charge problem are discussed in chapter 7. And we assume the circuit is settled at \( t = 0 \), and due to the lack of resistive elements the circuit will settle immediately after a tunnel event.

### 6.1 Different types of periodicity in electronic circuits

We can distinguish periodicity in the forms

1. Periodic signal in time
2. Periodic input-output relation
3. Periodic signal processing

These three periodic forms will be discussed in more detail in the following subsections.

#### 6.1.1 Periodic signal in time

A signal \( \zeta \) can be periodic in time. Let \( t \) be the time, and \( \tau_P \)\(^1\) the period time, with \( \tau_P \in \mathbb{R} \), which is a constant for a periodic signal.

**Definition 6.1** A signal \( \zeta \) that is fluctuating in time is periodic when

\[
\zeta(t + \tau_P) = \zeta(t) \quad \forall \ t
\]

(6.1)

See figure 6.1 for a signal which is periodic in time with \( \tau_P \).

When we want to code information in a periodic signal, the information that can be coded is very limited. An example of such a structure is the oscillator. Information can be placed in period \( \tau_P \) (or frequency \( f = \frac{1}{\tau_P} \)), amplitude, or phase. Of a pure periodic signal these are constants. When we want to code more information we can define a certain time window in which the signal is periodic.

One of the proposed SET circuits that showed an output signal periodic in time, is the single junction excited with a current source [5]. The current source charges the junction until the critical voltage (see chapter 4) \( v_j^c \) is reached (shown in figure 6.2), after which an electron will tunnel.

\(^1\)In the literature \( T \) is commonly used for period in time. To avoid confusion we use \( \tau \) for a time span and \( T \) for temperature in this thesis, also see page ix.
6.1 Different types of periodicity in electronic circuits

Figure 6.1: A signal $\zeta$ that is periodic in time $t$ with period time $\tau_p$.

(a) \hspace{1cm} (b)

Figure 6.2: a) A SET junction is charged by a current source. b) Periodic behaviour of this simple structure due to the fact that when the critical voltage $u_{cr}^j = \frac{e}{2C_j}$ is reached an electron will tunnel.

Interference is one way of using a periodic time signal. We can use the signal at the output of an oscillator, which is a periodic time signal. When we apply a controllable phase shift in one signal path and no phase shift in the other signal path we are able to design structures based on the principle of interference. When the signals are in phase they will amplify, and when they are out of phase they will interfere destructively. A system operating on this principle can be used to overcome the effects of random fluctuating background charges and is for that reason discussed in more detail in section 7.4.

More complex structures, like the SET transistor, show periodicity in the input-output relation, which is time independent and hence easier to use in signal processing.

6.1.2 Periodic input-output relation

Let $H$ be the (non-linear) input-output relation, $\zeta$ the signal, and $\rho$ the period ($\rho \neq 0$).

**Definition 6.2** The input-output relation $H$ is periodic when we can write for an input signal $\zeta$

$$H(\zeta) = H(\zeta + \rho) \ \forall \ \zeta$$  \hspace{1cm} (6.2)

In figure 6.3 a periodic (non-linear) input-output relation $H$ is drawn. When we sweep the input across a number of periods of this periodic input-output relation, the output signal will be a periodic time signal.
Figure 6.3: A periodic input-output relation $H$ with period $\rho$.

An example of such a periodic input-output relation is shown in figure 6.4b. This is the input-output relation of the electron-box (shown in figure 6.4a). The electron-box consists of a SET junction $TJ$ with a capacitance $C_j$ and one 'normal' (non-tunneling) capacitor $C_c$. Between these two components an island is created. As will be shown in section 6.2, the combination of an island and a SET junction will result in a periodic input-output relation with a period $\frac{e}{C_c}$.

Figure 6.4: a) The basic electron-box structure and b) its periodic input-output relation.

6.1.3 Periodic signal processing

Periodic processing is a processing that uses periodic signals. Two examples of periodic signal processing in common electronics are switch-capacitor circuits and sigma-delta converters.

The electron pump is a SET circuit that is based on periodic signal processing. The electron pump (discussed in more detail in section 9.4) consists of three SET junctions in series. Both islands are capacitively coupled to gate voltage sources (as is shown in figure 6.5).

By applying two oscillating signals on both gates, which are $\frac{\pi}{2}$ out of phase, an electron is forced through the structure\(^2\), hence the name electron pump. The applied gate voltages and the independent island charges due to tunneling are shown in figure 6.6. Let $q_1$ be the independent charge on node $w_1$ and let $q_2$ be the independent charge on node $w_2$. As can be seen from the simulations one electron is transferred

\(^2\)Explained in more detail in section 9.4.2.
from the bias voltage source $u_d$ to island $w_1$, after which it tunnels to island $w_2$ and then to ground. Hence a controllable flow of one electron is obtained.

When the gate signals are periodic signals with a small period (hence a high frequency), a measurable current results. Let $f_g$ be the frequency of the applied gate signals, then we can write for the current $i_p$ through the pump [29, 40, 99, 100]

$$i_p = e f_g$$

(6.3)

So the electron pump can be used in a regime in which it operates as a frequency to current converter, by applying correct (out of phase) gate voltages.

Figure 6.6: The two gate voltages which results in the change of the independent charge on the islands. For the simulation of the circuit of figure 6.5 all three junction capacitances and both gate capacitance were $C = 1aF$, and $u_d = 1mV$. 

![Diagram of the electron pump and gate voltages](image-url)
6.2 Origin of periodic behaviour

Let $q_i$ be the independent charge on an island. We can model this independent charge using a current source, as was discussed in section 3.2. This is represented in figure 6.7a where the independent island charge $q_i$ is modelled by a current source with value $q_i \delta(t)$. We assume that the input voltage $u_{in}$ is capacitively coupled to the same node (shown in figure 6.7a) and that the node is floating (forming a so called island). The voltage source can be replaced by a current source using its Norton equivalent, shown in figure 6.7b.

Let the total current flowing to the island be $i_i$ ($C_{in}$ is also part of the island), then we can write

$$I_i(s) = Q_i + sC_{in}U_{in}(s) \quad (6.4)$$

![Figure 6.7](image)

Figure 6.7: a) An island of which the independent charge $q_i$ is modelled by a current source. To the same island the input voltage source $u_{in}$ is capacitively coupled. b) The voltage source $u_{in}$ is changed into a current source $i_{in}$ using the Norton equivalent, $i_{in}(t) = \mathcal{L}^{-1}\{sC_{in}U_{in}(s)\}$.

Through a SET junction only an integer number of electrons can tunnel. When a SET junction is connected to an island, the electrons that have tunneled can be stored on the island. On such an island an initial charge (see section 3.2.4) and a background charge fluctuation can appear. Let $q_{init}$ be the initial charge (charge at $t = 0$), $q_{bgc}$ the background charge (see section 3.2.2), $n$ the number of independent electrons that have tunneled from the island, and $e$ the electron charge, then we can write for the independent island charge (at one moment in time)

$$q_i = en + q_{init} + q_{bgc} \quad (6.5)$$

The sum of the two current sources drawn in figure 6.7b can become equally large while the values of the current source $i_{in}$ is different in both situations. This is
possible when the independent island charge is changed and the input voltage $u_{in}$ is changed from situation $\sigma$ to situation $\sigma + 1$. Let $u_{out}$ be the output voltage, which is a function of the input voltage. The input-output relation is called periodic (see definition 6.2) with period $\rho$ when

$$u_{out}(u)\bigg|_{u_{in}^{\sigma+1}} = u_{out}(u)\bigg|_{u_{in}^{\sigma} + \rho} \quad \text{for } \rho \neq 0$$  (6.6)

This also holds for currents

$$i_{out}(u)\bigg|_{u_{in}^{\sigma+1}} = i_{out}(u)\bigg|_{u_{in}^{\sigma} + \rho} \quad \text{for } \rho \neq 0$$  (6.7)

For the rest of the derivation we only investigate the situation of an output voltage. It is easy to see the whole derivation also holds for an output current.

Using superposition (not taking the effect of other sources in the circuit into account) we can write (see figure 6.8)

$$U_{out}(s) = H_{iu}(s)I_i(s)$$  (6.8)

Using equation 6.4 this can be rewritten into

$$U_{out}(s) = H_{iu}(s)\left[Q_i + sC_{in}U_{in}(s)\right]$$  (6.9)

Filling this in equation 6.6 we obtain

$$\left(Q_i + sC_{in}U_{in}(s)\right)^{\sigma+1} = \left(Q_i + sC_{in}U_{in}(s)\right)^{\sigma}$$  (6.10)

Which is equal to (using equation 6.5)

$$\left(en + Q_{init} + Q_{bgc} + sC_{in}U_{in}(s)\right)^{\sigma+1} = \left(en + Q_{init} + Q_{bgc} + sC_{in}U_{in}(s)\right)^{\sigma}$$  (6.11)

Figure 6.8: The current $i_i$ injected into the island will give an output signal equal to $H_{iu}(s)I_i(s)$. In this figure we assumed an output voltage, $u_{out}$.

The initial charge is by definition equal for both situations

$$Q_{init}^{\sigma} = Q_{init}^{\sigma+1}$$  (6.12)
When we assume the background charge is equal for both situations as well

\[ Q_{bgc}^{\sigma} = Q_{bgc}^{\sigma+1} \tag{6.13} \]

and we assume that one electron has tunneled to the island

\[ n^{\sigma+1} = n^{\sigma} - 1 \tag{6.14} \]

we can simplify equation 6.11 into

\[ e(n^{\sigma} - 1) + s C_{in} U_{in}^{\sigma+1}(s) = e n^{\sigma} + s C_{in} U_{in}^{\sigma}(s) \tag{6.15} \]

\[ U_{in}^{\sigma+1}(s) = U_{in}^{\sigma}(s) + \frac{e}{s C_{in}} \tag{6.16} \]

With the help of equation 6.6 we can find

\[ U_{in}^{\sigma+1}(s) = U_{in}^{\sigma}(s) + \mathcal{L}\{\rho\} \tag{6.17} \]

From this equation it is clear that the periodicity \( \rho \) due to the discrete tunneling of an electron in a structure which contains an input voltage source capacitively coupled to an island is equal to

\[ \rho = \frac{e}{C_{in}} \tag{6.18} \]

So the periodicity (expressed in voltages) is always determined by the capacitance the input voltage source is coupled with.

As an example the C-SET transistor, as drawn in figure 6.9, is analysed. The simulated (by SIMON) output voltage and the output current are drawn in figure 6.10a and 6.10b respectively. In both cases the periodicity is indeed equal to equation 6.18.

![C-SET transistor schematic](image)

**Figure 6.9:** The SET transistor with an input voltage source \( u_{gs} \) and a bias source \( S_{ds} \), which can be a current source or a voltage source.

The fact that island charge and input voltage source can be exchanged, can and is used to compensate for initial charge and background charge.

When background or initial charges appear in this circuit a horizontal shift is obtained in the periodic input-output relation. This shift will give a phase offset in the signal, but the periodicity itself is not influenced by these undesired charges, also see chapter 7.
6.3 Modulo functions and their applications

Figure 6.10: The simulated results of the circuit shown in figure 6.9. The junction capacitances are both $500aF$ (and both tunnel resistors are $100k\Omega$). The gate capacitance is $C_g = 10aF$, so $\frac{C_s}{C_g} = 16mV$. a) The output voltage $u_{ds}$ when the bias source $S_{ds}$ is a current source with $i_{ds} = 1pA$ and b) the output current $i_{ds}$ when the bias source $S_{ds}$ is a voltage source with $u_{ds} = 50\mu V$.

6.3 Modulo functions and their applications

Modulo functions are one of the few functions which need a periodic input-output relation. For that reason we describe the modulo function and some of its specific behaviours here.

Modulo functions are often used in daily life. Examples can be found in many places; the time indication can be seen as a modulo function (seconds are modulo 60, hours are modulo 24 or 12), the same holds for the date, and our money indication (cents, euros, etc.).

A lot of mathematical research has been done on modulo functions; in the first subsection we will mention a few of the obtained results. In the second subsection we describe the EXOR function, which is a periodic function, as a possible digital binary building block. System concepts can also use modulo functions, as an example the Chinese remainder theorem will be described, which makes use of modulo functions, in the third subsection.

6.3.1 Mathematics of the modulo function

In this subsection we describe some of the basic mathematics of modulo functions. This will be used in the next subsections for the calculation of the Chinese remainder theorem.
Notation and simple arithmetic

Let $m$ be the number of times $x$ can fit in $g$, and let $r$ be the so called remainder or residue, then the relation between a number $x$ and a number $g$ can be written as follows

$$g = mx + r \quad \{x, g, m, r\} \in \mathbb{Z} \quad (6.19)$$

The numbers $x$ and $g$ are said to be modulo $m$ when the remainder is zero ($r = 0$). Notation

$$r = g \pmod{m} \quad (6.20)$$

Or in some literature written as: $r = [g]_m$.

Let $a$ and $b$ be integer numbers, $(a, b \in \mathbb{Z})$. Algebraic functions: addition, subtraction, and multiplication can be proven (not shown here) to be equal to

$$a \pmod{m} + b \pmod{m} = (a + b) \pmod{m} \quad (6.21)$$
$$a \pmod{m} - b \pmod{m} = (a - b) \pmod{m} \quad (6.22)$$
$$(a \pmod{m}) \times (b \pmod{m}) = (ab) \pmod{m} \quad (6.23)$$

Division can not be defined in this way, because the answer is not always unique$^3$.

Fermat’s little theorem

If $m$ is a prime, then for all integers $a \ (a \in \mathbb{Z})$

$$a^m = a \pmod{m} \quad (6.24)$$

This is known as Fermat’s little theorem, and can be rewritten into

$$a^{m-2}a \pmod{m} = 1 \quad (6.25)$$

If $ab \pmod{m} = 1$ (with $0 \leq (a, b) < m$) we call $a$ the multiplicative inverse of $b \pmod{m}$, this is written as

$$a = \frac{1}{b} \pmod{m} \quad (6.26)$$

We will use this theorem to determine the constants of the Chinese remainder theorem in section 6.3.3.

6.3.2 The EXOR function

Up to now most of the (digital) circuits made with SET junctions described in the literature, are transformations of the standard CMOS logic, in which many SET junctions are needed. As an example the by Jeong et al. [68] proposed EXOR function with SETs is shown in figure 6.11b. This is a direct transformation of a CMOS EXOR function (shown in figure 6.11a). The EXOR Jeong et al. proposed contains 16 SET junctions and needs a normal input voltage $u_{in}$ as well as the inverted version $\bar{u}_{in}$.

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$^3$Division in modulo functions is a complex theory and is beyond the scope of this thesis.
With the help of a modulo function it is easy to create an EXOR function. Let $\zeta_{out}$ be the output signal of the EXOR function, and $\zeta_{in}$ one of the input signals of the EXOR function. For a binary EXOR function with $k_{in}$ inputs we can write

$$\zeta_{out} = \left[ \sum_{d=1}^{k_{in}} \zeta_{in,d} \right] \pmod{2} \quad (6.27)$$

We propose an EXOR that is based on the periodicity obtained from the input-output relation of a SET electron-box structure.

To implement an EXOR function, the operating windows (see section 5.2) should be placed in such a way that the output voltage is low when the sum of the inputs is even and the output should be high when the sum is odd. In figure 6.12 the desired input-output relation of a multi input electron-box is shown, the number indicates the total number of the inputs that are high.

The distance between two operating windows is constant, and should be equal to the amplitude of the input signal. The electron-box should be biased such that it reaches operating window '0' without signals at the input (DC operating point).

For simplicity we assume that we wish to implement an EXOR function with two inputs (see figure 6.13a) of which both capacitances $C_{in,1}$ and $C_{in,2}$ are equal. The SET structure of figure 6.13a will have an input-output relation as shown in figure 6.13b.
Figure 6.12: The input-output relation of a multi input electron-box with the chosen operating windows to create an EXOR function. The number of the operating window is equal to the total number of inputs that are high.

Figure 6.13: a) A two input electron-box with two extra bias sources $u_{b,ve}$ and $u_{b,he}$ to shift the input-output relation in vertical and horizontal direction respectively. b) The input-output relation of the two input electron-box with bias sources. Let $C_j$ be the capacitance of the tunnel junction TJ, then $C_\Sigma = C_j + C_{in,1} + C_{in,2} + C_c$.

Because the input-output relation of figure 6.13b is not equal to the desired input-output relation of figure 6.12 bias sources are needed to shift the total input-output relation. With the help of the bias sources $u_{b,he}$ and $u_{b,ve}$ shown in figure 6.13 this can be done. The calculation of the necessary values for these bias sources will be described in section 9.2.2.

The simulation results of the output as a function of time is shown in figure 6.14. These simulation results confirm the expected output of an EXOR function.

The EXOR function implemented with the electron-box has no gain, which can simply be solved by buffering the EXOR before coupling it to other structures. To get some gain it can for example be connected to one of the well-known circuit elements (BJT, FET, etc.).
6.3 Modulo functions and their applications

Figure 6.14: The simulated response of a two input electron-box biased as an EXOR function as a function of time. The test conditions were: $T = 0K$, $C_{in,1} = C_{in,2} = C_{in} = 80\mu F$, $u_{b,ve} = 0.25mV$, $u_{b,he} = -0.24mV$, and $C_j = C_c = C_{in}$. The horizontal axis is in arbitrary time units. For the derivation of the component values used see section 9.2.2.

6.3.3 Residue number systems

On the one hand analog signals can be used in a circuit. When analog signals are used, there are no limitations in the dynamic range but noise is not easy to eliminate and it is very hard to make corrections to the signal. On the other hand binary digital signals could be used. In this last case the signal only consists of a logic '1' and '0' making reconstructions of damaged signals easier, but the used dynamic range is very limited, and the number of interconnects between the building blocks is much higher.

First of all, the transportation of signals should be done parallel to obtain a maximal transfer speed, but in case of binary signals we need a lot of interconnects (one interconnection for every bit). Secondly for signal processing of binary signals all bits should be received at the same time or stored somewhere in memory, because processing of the information needs the possibility of changing all signals, the transportation and processing of carry bits is needed. This makes complete independent parallel processing impossible.

The combination of multilevel signals and modulo functions give the possibility of less connections between processing units (more information on every interconnection, but still the possibility to reconstruct the signal after errors occur) and no communication between the signals is needed, making complete independent parallel processing possible.

Using modulo functions implies that we have as signals the residues of the arithmetic functions. Systems which uses residues are called residue number systems (RNS) [107]. The output of such a system still contains residues. To convert these
residues back into the desired analog signal a theorem called the Chinese remainder theorem (CRT) can be used.

During the whole processing of the signals in a residue-based system, no synchronisation is needed between the different interconnections. Only when using the CRT to convert the residues back into an analog signal, the data should be synchronised just before it enters the CRT conversion block. During the rest of the processing the data can be asynchronous.

The CRT is often used for computing, cryptography, and codes [32]. The use of the CRT in these areas is not discussed in this thesis. The fact that the three regions are gaining popularity in today's world, due to internet security etc, shows that the use of SET circuits in those areas can give a boost to the implementations. In this subsection only the CRT principle and its use for parallel processing is discussed.

An example

If we for example want to add\(^4\) two numbers, which will give an expected outcome below\(^5\) 255 we can do this in a number of ways. Three of them are

1. Analog (see figure 6.15). Each interconnection can contain a signal up to 255 distinguishable levels, hence creating the need for a large dynamic range. An analog adder that is linear in this complete range is needed. This approach has one advantage: there is a need for one adder only.

2. Binary (see figure 6.16). Each interconnection contains a zero or a one, creating a low dynamic range on each interconnection, and making the implementation of the adder very simple. After addition, a carry signal should be transferred to the higher bit.

3. Residues (see figure 6.17). The system contains only of three interconnections, with a dynamic range of up to 9 levels maximum in this example. No larger modulo or extra branch is needed because this circuit can handle numbers upto \(5 \times 7 \times 9 (> 255)\). There is also no need for any carry transfer.

![Figure 6.15: Schematic diagram of the implementation of an analog adder.](image)

\(^4\)Due to the use of modulo functions, next to addition also multiplication and subtraction are possible algebraic functions.

\(^5\)We assume an eight bit binary system.
6.3 Modulo functions and their applications

Figure 6.16: Schematic diagram of the implementation of a binary adder.

Figure 6.17: Schematic diagram of the implementation of a residue adder. The six (dotted) modulo functions directly connected to the inputs are only necessary at these inputs when we also want to limit the dynamic range of the input interconnections.

When we have for example \( \zeta_{in,1} = 129 \) and \( \zeta_{in,2} = 13 \) then in case of the modulo adder we obtain as input for the CRT block

\[
\begin{align*}
(129 + 13) \pmod{5} &= 2 \quad &(6.28) \\
(129 + 13) \pmod{7} &= 2 \quad &(6.29) \\
(129 + 13) \pmod{9} &= 7 \quad &(6.30)
\end{align*}
\]

The conversion of the residues into an analog signal can be done by the Chinese remainder theorem (CRT).
The Chinese remainder theorem

Let \( g \) be an integer, \( r \) be the residue representation of this integer, and \( m \) the modulo \( (g = mx + r) \). The Chinese Remainder Theorem (CRT) makes it possible to convert the residue representation of the integer back to \( g \pmod{M} \), so it is limited to \( g \) in the range \([0..M - 1]\).

Let \( m_d \) be the modulo belonging to residue \( r_d \), and let \( k_r \) be the number of residues, if and only if the greatest common divisor of the residues is 1. Then we can define

\[
M = \prod_{d=1}^{k_r} m_d
\]  
(6.31)

and

\[
\mathcal{M}_d = \frac{M}{m_d}
\]  
(6.32)

In the literature \( \mathcal{M}_d \) is also written as \( \overline{m}_d \).

In equation form the CRT can be written as [107]

\[
g \pmod{M} = \left[\sum_{d=1}^{k_r} \mathcal{M}_d \left\{ \frac{r_d}{\mathcal{M}_d} \pmod{m_d} \right\} \right] \pmod{M}
\]  
(6.33)

Because \( r_d < m_d \) this can be rewritten into

\[
g \pmod{M} = \left[\sum_{d=1}^{k_r} r_d a_d \right] \pmod{M}
\]  
(6.34)

with \( a_d \) a constant, namely (using Fermat’s little theorem, see section 6.3.1)

\[
a_d = \mathcal{M}_d \left[\mathcal{M}_d^{m_d^{-2}} \pmod{m_d} \right]
\]  
(6.35)

This can simply be implemented in hardware: just multiply the residue \( r_d \) with a constant factor \( a_d \), add all the results and modulo this answer with \( M \) (see figure 6.18).

No actual complete circuit for the CRT is given here. One of the reasons is the lack of a good analog multiplier in SET technology. Hence the proposed structure has to be a hybrid circuit with SET junctions (for the modulo implementation) and standard electronics for the analog multiplication. No simulator is able to simulate such a hybrid circuit yet.

The proof that the result found when using the CRT is always \( g \pmod{M} \) is beyond the scope of this thesis. As long as \( M \) is smaller than the outcome, the outcome gives the correct value.

To come back to the example that was drawn in figure 6.17: we obtained three residues \( r_1 = 2, r_2 = 2, \) and \( r_3 = 7 \), which belong to the modulo functions \( m_1 = 5, m_2 = 7, \) and \( m_3 = 9 \). And hence \( M = 315 \) (see equation 6.31). With the help of
equation 6.32 and 6.35 we are able to determine the constants

\[
\begin{align*}
    a_1 &= \frac{315}{5} \left( \frac{315}{5} \right)^3 \pmod{5} = 126 \quad (6.36) \\
    a_2 &= \frac{315}{7} \left( \frac{315}{7} \right)^5 \pmod{7} = 225 \quad (6.37) \\
    a_3 &= \frac{315}{9} \left( \frac{315}{9} \right)^7 \pmod{9} = 280 \quad (6.38)
\end{align*}
\]

Using the CRT system concept of figure 6.18 and the residues that were found, we obtain

\[
g = \left( 2 \times 126 + 2 \times 225 + 7 \times 280 \right) \pmod{315} = 142 \quad (6.39)
\]

which was indeed the outcome of the example.

From this example another conclusion can also be drawn: the high accuracy due to a high dynamic range of possible signals is now also needed in the CRT block. So instead of using it for every multiplication, addition, and subtraction within the circuit, it is now only needed at the final conversion stage, where the residues are converted back into a single analog signal.

### 6.4 Conclusions

In simulators all parameters can be chosen ideal. In a practical setup, which can become realistic in the near future, many parameters of the proposed structure can give an undesired reaction. The use of the periodicity mentioned in this chapter is very sensitive to some of the following aspects.

- The period of a SET structure is completely determined by the capacitor with which the input voltage source is coupled to the island. The accuracy of a
designed periodicity is completely determined by the accuracy with which this capacitor can be fabricated. The maximal applied input voltage is only determined by the breakthrough voltage of the insulator inside the SET junction, and hence depends on the fabricated SET junction.

- For the operation of a building block which design depends on the periodicity, the appearance of random background charges also play an important role. For example the proposed electron-box structure to implement a modulo function will generate completely wrong output signals when a background charge occurs. To create a reliable building block a method should be used to compensate for these background charges. Methods to compensate for the background charges are discussed in chapter 7.

- When background charges form no problem, and the capacitances of the input capacitors as well as the capacitances of the tunnel junctions can be made very accurately, timing aspects can play a role as well. At this moment it is not known what the tunnel time of one electron is exactly, hence we can only estimate that the speed and the timing aspects of the proposed structures will be around $10^{-15}s$ (see section 4.2).

- When structures are made very small (atomic scale) the number of electrons that can tunnel decreases rapidly. Due to this, stochastics will also play a role in the output voltage.

- Also some special care should be taken when the proposed structures are coupled to other blocks, this problem will be discussed in more detail in chapter 8.
Solutions for the random background charge problem

In this chapter we study how to overcome the problem of the random background charge. Random background charges manifest themselves as random fluctuating independent island charges as was discussed in section 3.2.2. These random fluctuations of static and dynamic background charge are a serious problem in single-electron tunneling (SET) circuits [137].

Even when we are able to design a sub-circuit in the way we want it (as was discussed in chapters 5 and 6), and we are able to couple it (as will be discussed in chapter 8) to other stages, and we are able to fabricate such small structures, there are still some phenomena which should be also taken into account. The background charge fluctuations are one of them.

Because of the small geometry of a SET device small fluctuation in the surrounding of the junction (the material, fabrication, impurities etc.) will cause a direct change in the island charge. These fluctuations can completely destroy the desired behaviour of the sub-circuit build, due to the fact that an independent charge is added to an island. Such an independent charge can have any value; it is not necessarily equal to the elementary charge of an electron.

Some of the origins of the random background charge fluctuations are constant (static) and need to be tuned only once. This tuning should be done for each island. Tuning by hand, which is done in the current measurements, will be a big problem when a circuit contains many islands. Other origins of the random background charge are random, and can change in time (from seconds to days), the so-called dynamic background charges. Automatic tuning needs to be done to compensate for these dynamic changes.

When we want to design circuits which are not sensitive to background charge fluctuations we can use a few methods to reach this goal. In this chapter we will discuss some of them.
1. We could try to find out the exact reason why this change in charge fluctuation exists and try to solve it. This is hard to do; a lot of researchers have tried this already. There are a lot of different explanations for the existence of the background charge (this 'solution' is not discussed in this chapter).

2. Design a circuit which has a lot of circuit redundancy so a change in charge can be averaged-out. A neural network concepts [48, 122] can be used to implement this hardware redundancy (in the form of a distributed memory) and to learn the network to cope with static and dynamic background charges. The problem of this idea is that because of this redundancy a larger circuit is designed than required.

3. Design a feedback loop, which can compensate for a change in the random background charge. A problem of this solution is that the feedback loop itself should be insensitive to background charge; otherwise we also need a compensation for this background charge.

4. Use information coding which can be made insensitive to background charge. Using a number of periods of the periodic SET transistor function for example creates the necessary redundancy. The problem with this idea is that we can not use the basic SET building blocks described in different papers.

This chapter will start with a section about the influence of the random background charge on the input-output relation of a SET structure (which contains at least one island). From that analysis it is clear that the background charge manifests itself in a horizontal shift in this input-output relation.

In the second section of this chapter we will show how to code the information in the amplitude or the period of the signal. Because the random background charge manifested itself in a horizontal shift, the maximal output signal (the amplitude), and the period in which no background charge appeared are constant.

In the third section we show how to use a feedback circuit for every island to compensate for random background fluctuations in sub-circuits with only one island. In the fourth section we show a system design for logic signals based on interference, which makes it possible to sense and compensate the random background charge for a larger circuit.

We end this chapter with some conclusions.

### 7.1 The influence of background charge

As was discussed in section 3.2.2 independent background charges can be modelled by a current source, see figure 7.1. Due to the fact that we have charge neutrality in the circuit, a background charge will always appear on two places in the circuit. Hence the model of this charge is a current source connected between those two nodes in the circuit.

In figure 7.2a an island is drawn which is capacitively coupled to a voltage source. Let \( \sigma \) be a situation and \( \sigma + 1 \) another situation, \( u_{in} \) be the input voltage capacitively coupled by \( C_{in} \). The independent island charge \( q_{i} \) is due to the initial charge, the random background charge, and the number \( n \) of electrons (with elementary charge
7.1 The influence of background charge

Figure 7.1: The change in charge on node 1 and node 2 due to a background charge can be modelled by a current source.

e) that have tunneled (see section 3.2). Let \( q_{\text{init}} \) be the initial charge, \( q_{\text{bge}} \) the random background charge, and \( ne \) the charge due to \( n \) electrons that have tunneled from the island. So we can write

\[
Q_i = Q_{\text{init}} + Q_{\text{bge}} + ne
\]

(7.1)

Figure 7.2: a) An island of which the independent charge \( q_i \) is modelled by a current source. The input voltage source \( u_{in} \) is capacitively coupled to the same island. b) The voltage source \( u_{in} \) is changed into a current source \( i_{in} \) using the Norton equivalent, \( i_{in}(t) = L^{-1}\{sC_{in}U_{in}(s)\} \).

Using the method that was also used in determining the periodicity (section 6.2) we can write both situations of the output signal as a function of the input voltage and the independent charge. We assume that the circuit under investigation is a linear circuit, so we are allowed to use superposition (as was discussed in section 3.2.1). The output signal is measured somewhere else in the circuit (not drawn). Let \( \zeta_{out} \) be the output signal. For both situations \( \sigma \) and \( \sigma + 1 \) we can get the same output signal when

\[
\zeta_{out}^{\sigma}(t) = \zeta_{out}^{\sigma + 1}(t)
\]

(7.2)
Except for the current source modelling the charge on the island we are investigating, and the input voltage source which is capacitively coupled to that node, we assume that all other current sources and voltage sources in the circuit, which normally would contribute to this output signal, are identical in situation $\sigma$ and $\sigma + 1$. Let $\zeta_e$ be their contribution to the output signal, so

$$\zeta_e^\sigma (t) = \zeta_e^{\sigma+1} (t)$$  \hspace{1cm} (7.3)

The capacitively coupled input voltage source can be transformed into a current source, using the Norton equivalent (see figure 7.2). Let $i_i$ be the sum of this current source and the current source modelling the total independent island charge of equation 7.1, and let $H$ be the relation between this current injected on the island under investigation and the output signal $\zeta_{out}$ (see figure 7.3). We can write for the total current injected into the island $i_i$

$$I_i(s) = Q_i + sC_{in}U_{in}(s)$$  \hspace{1cm} (7.4)

Figure 7.3: The current $i_i$ injected into the island will give an output signal equal to $H(s)I_i(s)$. The dimension of $H$ depends on the physical quantity of the output signal (either voltage or current).

So we can rewrite equation 7.2 into

$$I_i^\sigma(s)H(s) + \zeta_e^\sigma(s) = I_i^{\sigma+1}(s)H(s) + \zeta_e^{\sigma+1}(s)$$  \hspace{1cm} (7.5)

Using equation 7.3 this can be rewritten into

$$I_i^\sigma(s) = I_i^{\sigma+1}(s)$$  \hspace{1cm} (7.6)

We assume that between situation $\sigma$ and $\sigma + 1$ one electron has tunneled to the island and the background charge has changed from $q_{bgc}^\sigma$ to $q_{bgc}^{\sigma+1}$. The initial charge $q_{init}$ is by definition equal for both situations;

$$Q_{init}^\sigma = Q_{init}^{\sigma+1}$$  \hspace{1cm} (7.7)

Now we can simplify equation 7.6, using equation 7.1, and 7.4 into

$$U_{in}^\sigma(s)sC_{in} + Q_{bgc}^\sigma + ne = U_{in}^{\sigma+1}(s)sC_{in} + Q_{bgc}^{\sigma+1} + (n - 1)e$$  \hspace{1cm} (7.8)
This expression can be written as

\[ U_{in}^{\sigma+1}(s) - U_{in}^{\sigma}(s) = \frac{e}{sC_{in}} + \frac{Q_{bgc}^{\sigma} - Q_{bgc}^{\sigma+1}}{sC_{in}} \]  

(7.9)

Let \( \Delta q_{bgc} \) be the change in background charge, so

\[ \Delta q_{bgc} = q_{bgc}^{\sigma} - q_{bgc}^{\sigma+1} \]  

(7.10)

Combining equation 7.9 with equation 7.10 shows that the period, which is normally equal to \( \frac{e}{C_{in}} \) (see section 6.2), will have an offset of \( \frac{\Delta q_{bgc}}{C_{in}} \) due to a change in background charge. This offset is expressed in input voltage, and is equal to

\[ \Delta u_{in} = \frac{\Delta q_{bgc}}{C_{in}} \]  

(7.11)

From this we can conclude that the independent background charge can be compensated by a change in the input voltage source.

When a background charge appears, the graph of the input-output relation will shift in the horizontal direction, as shown in figure 7.4 and equation 7.11. When the background charge changes with an integer number of electrons, this shift will not be visible. The background charge only influences the horizontal position of the input-output relation, but not the amplitude or the period.

Almost all the proposed digital circuitry with SET junctions is based on CMOS structures, and hence they are based on current - no-current transitions. The input-output relation of these proposed circuits can be completely altered into an undesired relation due to the random background charges.

As an example we analyse the behaviour of two junctions in series (see figure 7.5a). Let \( C_{j1} \) be the capacitance of tunnel junction TJ1 and let \( C_{j2} \) be the capacitance of tunnel junction TJ2, and let \( C_{\Sigma} = C_{j1} + C_{j2} \). SET junction TJ2 of those two junctions in series (see figure 7.5a) has a critical voltage \( u_{j2}^{cr} \) of

\[ u_{j2}^{cr} = \frac{e}{2C_{\Sigma}} \]  

(7.12)

The voltage across junction 2 is equal to

\[ u_{j2}(t) = u_{s}(t) \frac{C_{j1}}{C_{\Sigma}} + q_{t} \epsilon(t) \frac{1}{C_{\Sigma}} \]  

(7.13)

So the Coulomb blockade ends for TJ2 when

\[ \frac{e}{2C_{\Sigma}} \equiv u_{s}(t) \frac{C_{j1}}{C_{\Sigma}} + q_{t} \epsilon(t) \frac{1}{C_{\Sigma}} \]  

(7.14)

We can express this equation in a condition for the source voltage \( u_{s} \)

\[ u_{s}(t) = \frac{e}{2C_{j1}} - q_{t} \epsilon(t) \frac{1}{C_{j1}} \]  

(7.15)

For an independent island charge of \( q_{t} = 0 \) the expected Coulomb blockade of \( \frac{e}{2C_{j1}} \) is indeed found. The proposed function of these kind of structures is based on this
Figure 7.4: a) The electron-box structure. b) The input-output relation for situation \( \sigma \), in which the background charge is zero. c) The input-output relation for situation \( \sigma + 1 \), in which the background charge is unequal to zero, causing the input-output relation to shift in the horizontal direction. As indicated in this figure the effect of the background charge is equal to an extra input voltage of \( \Delta u_{in} = \frac{\Delta q_{bac}}{C_{in}} \).

Figure 7.5: a) Two SET junctions in series excited by a voltage source \( u_s \), with an independent island charge \( q_i \). b) The current \( i_{vs} \) through the voltage source as a function of the applied voltage \( u_s \), when the capacitance of both junctions is \( C \). For a more detailed description of this graph (like the slopes etc.) see chapter 9.

charge value of zero. But when an independent background charge of \( q_i = \frac{e}{2} \) has appeared, no Coulomb blockade is found (see figure 7.5b), and a current will always flow through the structure.
When sweeping the input voltage across a few periods of a periodic input-output relation a jump in output voltage will occur when a background charge (unequal to an integer number of electron charges) appears. In the periodic output voltage a phase change takes place. The total phase change stays changed after the background charge has appeared, and will only change back to its original position when the exact same background charge leaves the island, or an extra charge appears which makes the total change in charge equal to an integer times \( e \).

As an example of a shift in the input-output relation we again analyze the electron-box structure of figure 7.4a and we assume that a background charge appears at \( t_{bgc} \) during a sweep of the input voltage. The output voltage as function of time is shown in figure 7.6.

![Diagram](image)

Figure 7.6: The output voltage of an electron-box structure, as was shown in figure 7.4a. A background charge occurring at moment \( t = t_{bgc} \) will cause a phase shift in the periodic output voltage.

To make the information background charge insensitive it is possible to code the information in the amplitude or in the period of the input-output relation, and not in an one-on-one relation between the input and the output of figure 7.6. The two options (information in amplitude or in period) are discussed in section 7.2.

### 7.2 Signal level solution

Independent of the type of circuit, as long as it contains at least one island and one SET junction, it will have a periodic input-output relation (as was shown in section 6.2). Consider the case that we sweep the input voltage over a few periods of the input-output relation in a certain time. Let \( C_{in} \) be the capacitance which couples the sweeping source with the island, then the period will be equal to \( \frac{e}{C_{in}} \).

As an example of a SET circuit we will consider the capacitively coupled SET (C-SET) transistor (discussed in more detail in section 9.3), which consists of two tunnel junctions in series.\(^1\) Let \( C_{j1} \) be the capacitance of TJ\(_1\) and \( C_{j2} \) be the capacitance of TJ\(_2\). In the middle an island is formed, the floating node \( w \). By adjusting the input voltage \( u_{in} \) in series with an input capacitor \( C_{in} = C_g \), the current through the tunnel junctions can be controlled.

---

\(^1\)Any circuit with a periodic input-output relation could have been chosen.
For a current excited C-SET transistor as shown in figure 7.7, the relation between $u_{out}$ and $u_{in}$ is shown in figure 7.8, in case of $C_L \gg \max\{C_{j1}, C_{j2} + C_g\}$ [74]. The shape of this input-output relation is completely determined by the device parameters.

![Capacitively coupled SET transistor excited by a current source.](image)

Figure 7.7: The capacitively coupled SET transistor excited by a current source.

![Input-output relation of a capacitively coupled SET transistor.](image)

Figure 7.8: The input-output relation of a capacitively coupled SET transistor, for $C_{j2} + C_g > C_{j1}$. The initial island charge $q_{init}$ and background charge $q_{bgc}$ are zero.

The idea for the method of information decoding is to use that part of the input-output relation, which is insensitive to background charge. The input-output relation of the current biased C-SET transistor changes in horizontal direction when a background charge change takes place (as was discussed in section 7.1).

Because of this phase shift in the output voltage, the information can be coded in the amplitude or in the period, for both a variable capacitance is needed. Likharev and Korotkov [90] also proposed a memory based on SET junctions using the amplitude of the input-output relation to become independent of random background fluctuations.

For information coding in the amplitude an extra (variable) capacitor needs to be connected to the island. For information coding in the period the normally constant gate capacitor needs to be replaced by a variable one.

Because the shift caused by the background charge can be anything from a small part of one electron till a few electrons (this can not be seen because of the periodicity of the input-output relation), we should sweep the input-output relations over a few periods. So redundancy in information is used to cope with the background charge problem. To be able to use the amplitude or the period for the information coding, we need to be able to shift through a certain part of the input-output relation. This can easily be done by applying a ramping oscillation signal (for example a saw-tooth shaped signal) as an input voltage to the gate of the transistor.

The amplitude coding is less sensitive for background charge fluctuations. Destroying the coded information in that case can only be done when the background charge fluctuation appears just before the maximum output voltage is reached.
If the background charge changes (with an amount unequal to an integer number of electrons) in the middle of a sweep of the input voltage, that period will not be equal to \( \frac{e}{C_g} \) (see figure 7.6). As long as there are significantly less background changes appearing than there are periods during one sweep in time, we can extract information that is coded within a period.

To code the information in amplitude or in period a transformation from a voltage change into a change in a capacitive value is needed. This can be done by for example using diodes (pn-junctions) as converters for converting an (input) voltage change into a desired change in the capacitance value. The relation between the voltage and the capacitance depends on the temperature and on the chosen fabrication values, like material constants and impurities. Because the choice for temperature also depends on the tunnel junctions we are not able to freely choose this parameter. This leaves us with the choice of fabrication and material, which should still give us enough degrees of freedom to come up with an usable design.

### 7.2.1 Information coded in the amplitude

As a starting point we define two signals: a '1', which represents a periodic signal with a high amplitude, and a '0', which represents a periodic signal with a low amplitude.

As an example we use the building block shown in figure 7.9. Its input-output relation is phase independent, so it is also background charge fluctuation independent. The decoder in this figure senses the amplitude of the input \( \xi_{in,2} \). The output of the decoder is 0 if the amplitude of the \( \xi_{in,2} \) signal is low ('0'), and the output is 1 if the amplitude is high ('1'). The values of the output signal of the decoder are constant and not periodic like respectively '0' and '1' of the signals applied to the inputs \( \xi_{in,1} \) and \( \xi_{in,2} \). The switch \( \xi \) is normally closed; if \( a = 0 \) the switch will stay closed, and when \( a = 1 \) the switch will open. We can define now four possible input-output relations, which are shown in figure 7.10. The output of the building block can only be '1' when the amplitude of input \( \xi_{in,1} \) is '1' and the input amplitude of \( \xi_{in,2} \) is '0', in formula

\[
\xi_{out} = \xi_{in,1} \cdot \overline{\xi_{in,2}}
\]  

(7.16)

This function is known as the "non-implication". With this function a complete set of logical functions can be created if the signals '0' and '1' are available.

Because the total capacitance connected to the island of a C-SET transistor is directly responsible for the amplitude of the input-output relation (see figure 7.8), and hence the amplitude of the output signal, the information has to be coded into a capacitance. Let \( C_\Sigma \) be the sum of all the capacitances connected to the island of the C-SET transistor, and \( u_{out} \) the maximal value the output voltage can have. For this peak value of the output signal of a current biased C-SET transistor we can write

\[
u_{out} = \frac{e}{C_\Sigma}
\]

(7.17)

So the larger the sum of the capacitances connected to the island, \( C_\Sigma \), the smaller the amplitude and vice versa.

By adding an extra capacitance \( C_{g2} \) to the island which is variable (see figure 7.11), we can change the total capacitance, \( C_\Sigma \), which changes the amplitude, \( \frac{e}{C_\Sigma} \), of the input-output relation.
Figure 7.9: The building block used for processing signals. The decoder transforms a periodic signal into a 0 or a 1. The switch $\zeta$ itself is not a real switch in the sense that it is an open or a short connection between $\zeta_{\text{in},1}$ and $\zeta_{\text{out}}$. It switches information, so either a change in amplitude (as shown in figure 7.10) or a change in frequency (as shown in figure 7.13).

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Figure 7.10: Corresponding input and output signals of the building block of figure 7.9 when information is coded in the amplitude. The decoder of figure 7.9 can be seen as a rectifier followed by a threshold.

Let $C_{j1}$ be the capacitance of tunnel junction TJ$_1$, and let $C_{j2}$ be the capacitance of tunnel junction TJ$_2$, then the total capacitance connected to the island will be

$$C_{\Sigma} = C_{j1} + C_{j2} + C_{g_1} + C_{g_2}$$  \hspace{1cm} (7.18)

When we sweep the gate voltage over a few periods of the input-output relation, we get a periodic output voltage with an amplitude depending on the value of the variable capacitance. The peak of the voltage signal applied to the second input ($u_{\text{in}2}$) is obtained by using a rectifier. By doing so the amplitude of $u_{\text{in}2}$ determines the value of the extra capacitance $C_{g_2}$.

A high output voltage of the rectifier ($a = 1$) causes the capacitance $C_{g_2}$ to increase, and hence the amplitude of the output voltage $\zeta_{\Sigma}$ to decrease. When the output of the rectifier is a low voltage ($a = 0$) the gate capacitance $C_{g_2}$ is not changed. So the amplitude of the output voltage is a constant.

When $u_{\text{in},1}$ is a signal with a small amplitude only a small part of the input-output relation is used, so only a small change in output amplitude is obtained. When $u_{\text{in},1}$
has a large amplitude, it sweeps across a few periods of the input-output relation, and hence the maximal output amplitude \( \frac{i_s}{C_p} \) is obtained.

So we have the same function as the building block in figure 7.9.

![Figure 7.11: A SET implementation of the building block of figure 7.9 with information coded in the amplitude. The decoder of the building block shown in figure 7.9 is implemented as a rectifier, and the amplitude coding is implemented by a voltage controlled capacitor.](image)

In figure 7.12 two simulation results are shown, made with SIMON [131]. These results show that the amplitude indeed changes when the capacitance value of \( C_{g2} \) changes, and that the period is unaltered.

![Figure 7.12: Simulated input-output relation for the circuit of figure 7.11 for two different gate capacitances \( C_{g2} = 40aF \) (solid line) and \( C_{g2} = 120aF \) (dotted line), with \( C_{g1} = 40aF \), \( C_L = 40fF \), \( i_s = 1pA \), and the capacitance \( C_j \) of both tunnel junctions TJ, \( C_j = 40aF \).](image)
7.2.2 Information coded in the period

Information can also be coded in the period. As a starting point we again define two signals: a '1', which represents a periodic signal with a short period, and a '0', which represents a periodic signal with a long period. We use figure 7.9 as a building block again. The decoder in this figure senses the period of the input signal $\zeta_{in,2}$. The output of the decoder ($a$) is 0 if the period of the signal $\zeta_{in,2}$ is long ('0'), and the output is 1 if the period is short ('1'), these values are constant and not periodic like respectively '0' and '1' of the signals. The switch is a normally closed switch; if $a = 0$ the switch will stay closed, and when $a = 1$ the switch will open. The four possible input-output relations are shown in figure 7.13.

![Figure 7.13: Corresponding input and output signals of the building block of figure 7.9 when the information is coded in the period. When $a = 0$ the switch will be closed, and hence $\zeta_{out} = \zeta_{in,1}$, when $a = 1$ the switch will be open, and hence $\zeta_{out} = '0'$, which means in this case of period coding: a long period.]

Because the period of the input-output relation of the C-SET transistor depends on the gate capacitance (see figure 7.8), we need to change this gate capacitance in order to change the period. By changing the gate capacitance into a variable capacitance (see figure 7.14), we can change the period, $\frac{C}{C_g}$, and thus the period of the input-output relation. When we sweep the gate voltage over a few periods of the input-output relation, we get a periodic output voltage with a period depending on the value of the variable gate capacitance. The period of the signal $u_{in,2}$ determines the value of the gate capacitance.

A high output of the rectifier ($a = 1$) (so $u_{in,2}$ has a short period) decreases the gate capacitance $C_g$ and hence the period of the output signal ($\frac{C}{C_g}$) will be long. A signal $u_{in,2}$ with a long period ($a = 0$) does not change the gate capacitance $C_g$.

When $u_{in,1}$ is a rapidly changing signal it will sweep over many periods of the input-output relation when the gate capacitance is unaltered ($a = 0$), and hence create many periods in the output signal.

When $a = 1$, the gate capacitance is decreased, and hence the period is increased. Due to this a rapidly changing signal $u_{in,1}$ will only be able to sweep across a few periods and create a slow varying output. For example (see figure 7.15) a signal $u_{in,1}$ with an amplitude of $2mV$ will have for $a = 0$ ($C_g = 60aF$) two output periods per sweep, while it has only one period per sweep for $a = 1$ ($C_g = 40aF$).
For a slow varying signal \( u_{in,1} \) (so a long period) it can only sweep over a few periods and hence the output will contain only a few periods.

In this way we created the same function as the building block in figure 7.9.

\[ u_{in,1} \]

\[ u_{in,2} \]

\[ u_{out} \]

Figure 7.14: A SET implementation of the building block of figure 7.9 with information coded in the period. The voltage applied to the second input \((u_{in,2})\) is first filtered by a filter which passes the high frequencies, after which this signal is fed into a rectifier. The output voltage of the rectifier changes the voltage depending gate capacitance \( C_g \).

For the period of the input-output voltage relation of the circuit of figure 7.14 we can write (see section 6.2)

\[
\Delta u_{in,1} = \frac{e}{C_g} 
\]  

(7.19)

Let \( C_{j1} \) be the capacitance of tunnel junction TJ1, let \( C_{j2} \) be the capacitance of tunnel junction TJ2, and let \( \dot{u}_{out} \) be the maximal output voltage as function of the input voltage. Then we can write for the amplitude of the input-output voltage relation

\[
\dot{u}_{out} = \frac{e}{C_{j1} + C_{j2} + C_g} 
\]  

(7.20)

In figure 7.15 two simulation results are shown, made with SIMON [131]. These results show that the period indeed changes when the gate capacitance changes. Note that the amplitude is also somewhat lower for a gate capacitance of \( C_g = 60aF \), than for \( C_g = 40aF \) (due to equation 7.20). This change in amplitude can be minimised by choosing \( C_g \ll \min\{C_{j1}, C_{j2}\} \)

### 7.3 Circuit level solution

From equation 7.11 it should be clear that island charges can be compensated with voltage sources which are capacitively coupled to the island where the charge appears [130].

When we apply no input signal to a SET circuit, the output should correspond to this no-input signal \((u_n)\). If the output value \((u_{out})\) is different then the one belonging to this input (defined by the known input-output relation for \( q_{egc} = 0 \)), this difference \(\Delta u\) is due to a background charge on the island \(w\). For that reason
we can compensate during zero input signals. If we apply an input signal which contains a zero signal during a certain time span (called sync-signal), see figure 7.16a, we can measure the difference in voltage $\Delta u$ due to the background charge. In figure 7.16b the principle block diagram is drawn. During the sync-signal the switch $\varsigma$ is closed. From the measured output voltage $u_{out}$ the normal output voltage $u_n$ is subtracted. This difference $\Delta u$ is amplified to $u_c$ such that

$$u_c C_c = -q_b g_c \quad (7.21)$$

A problem of this background solution is that it only works when each sub-circuit contains only one island and for every island such a feedback system should be designed.

The normal output voltage value ($u_n$) is circuit dependent and is usually a function of the capacitors used. This normal output voltage $u_n$ should be a DC source, rather than a charged capacitor, due to the fact that background charges can also appear on such a charged capacitor.

If background charges appear somewhere in the feedback circuit, like on the floating node created to charge the feedback capacitors to a voltage $u_c$, this will result in an error. This error will appear until the next sync-signal. Hence the proposed circuit compensation for background charges is not totally insensitive for background charges itself, but will create only an error when a background charge occurred in the compensation network between two sync-signals.
Figure 7.16: a) A possible input signal, which includes a moment of zero input, called the sync-signal. b) The principle to compensate for background charge in SET subcircuits, which contain only one island (node w). All the mentioned voltages are between the indicated node and the ground node.

7.4 System level solution

Another way to compensate for random background charges is using the fact that a background charge appearing on an island will result in a phase error when sweeping the input signal over a few periods of the periodic input-output relation.

A solution to be able to work with these kinds of phase errors is to work asynchronous. To work asynchronous means that the processing of signals should not depend on the phase of other signals. Working asynchronous makes it impossible to add two signals in the way as is shown in figure 7.17b. A phase error between the input and the output of a function $F_1$ shown in figure 7.17a will cause only a difference in phase between the input and the output of the whole system. While due to an undesired phase difference between the input and the output of the function $F_1$ shown in figure 7.17b, the outcome will be totally wrong.

As a consequence of the phase errors the system, which needs to be designed, should be made (if possible) in an asynchronous series connection of basic blocks.

Figure 7.17: a) A series connection of two blocks with the functions $F_1$ and $F_2$. b) The parallel connections of two blocks with the functions $F_1$ and $F_2$. A phase difference between the input and the output of building block with function $F_1$ will generate a bigger problem in figure b.
In the case of logical functions for example, we should use a series connection rather than a parallel connection, when we are trying to design random background insensitive circuits. In figure 7.18a the series connection is drawn of a system to implement the logic OR function $\zeta_A + \zeta_B$, while in figure 7.18b the parallel connection is drawn.

![Diagram](image)

Figure 7.18: a) A series connection to implement an OR function. b) The parallel connections to implement the same logic function.

In the case of figure 7.18a we need an extra inverter (as is drawn), so the function which is implemented is

$$\zeta_{out} = \overline{\zeta_A} \cdot \overline{\zeta_B} = \zeta_A + \zeta_B$$  

(7.22)

In case of figure 7.18b we need a limiter (in the figure indicated by 'lim 1') to obtain a maximal output of '1'. This is needed due to the fact that when both switches are closed, and the signals at the output of the switches are in phase, the output signal $\zeta_{out}$ will have a double amplitude. When a phase difference appears within any of the switches, the summed output signal $\zeta_{out}$ will be wrong.

A possible implementation of such a switch is shown in figure 7.19. The phase shift depends on the input signal $\zeta_{in}$. When there is no phase shift ($\zeta_{in} = 0$) the output signals are added, hence the amplitude of the output will be twice as high as the amplitude of the oscillator. When a signal is applied at the input ($\zeta_{in} = 1$), a phase difference of $\pi$ will appear, hence both signals are out of phase and the output will be zero. So for the phase $\theta$ we can write

$$\theta = 2 \cos^{-1}(\zeta_{in})$$  

(7.23)

The blocks of figure 7.19: the phase shifter due to an input signal $\zeta_{in}$ and the adder, are easy to implement in SET circuits. A C-SET transistor can be the implementation of each block. A phase shift in the adder will not influence the output signal, also see the discussion about figure 7.17, while a phase shift in the phase shifter will destroy the correctness of the outcome. Let $\theta$ be the desired phase shift (so $\theta = \{0, \pi\}$) and $\theta_e$ the extra phase shift due to background phenomena. Then we can write for this
circuit\textsuperscript{2}

\[ \zeta_{out} = \sin(\omega t) + \sin(\omega t + \theta + \theta_e) \]  
\[ (7.24) \]

Using geometric equations we can rewrite this equation into

\[ \zeta_{out} = 2 \cos\left( \frac{\theta + \theta_e}{2} \right) \sin\left( \omega t + \frac{\theta + \theta_e}{2} \right) \]  
\[ (7.25) \]

Let \( \hat{\zeta}_{out} \) be the amplitude of the output signal. For this amplitude we can write (see equation 7.25)

\[ \hat{\zeta}_{out} = 2 \cos\left( \frac{\theta + \theta_e}{2} \right) \]  
\[ (7.26) \]

When the desired phase shift \( \theta \) is known, the error shift \( \theta_e \) can simply be derived. During the error phase detection a constant known signal (sync-signal) should be applied, which is available during an integer number of periods. Equation 7.26 is equal to

\[ \hat{\zeta}_{out} = 2 \left[ \cos\left( \frac{\theta_e}{2} \right) \cos\left( \frac{\theta}{2} \right) - \sin\left( \frac{\theta_e}{2} \right) \sin\left( \frac{\theta}{2} \right) \right] \]  
\[ (7.27) \]

When we choose a different signal level for the sync-signal than the possible values of the input signal, it is possible to distinguish between an input signal and a sync signal. So for example we choose an amplitude \( \zeta_{in} = 0.5 \) as a sync-signal, which is neither one of the binary signals (0 and 1). When we apply \( \zeta_{in} = 0.5 \) we obtain a desired phase shift of (see equation 7.23) \( \theta = \frac{\pi}{3} \), and hence an output amplitude of

\[ \hat{\zeta}_{out} = \sqrt{3} \cos\left( \frac{\theta_e}{2} \right) - \sin\left( \frac{\theta_e}{2} \right) \]  
\[ (7.28) \]

With the help of this equation the phase error \( \theta_e \) can be calculated. After which the necessary compensation can be obtained by a feedback network, as was already indicated in figure 7.16b. Only in this case the feedback can be attached to any of the islands in the 'switch'.

\textsuperscript{2} For simplicity we assume sin-shaped signals, which is a correct assumption for the output signals of a C-SET transistor when the operating temperature is unequal to zero, \( T \neq 0 \).
The solution described here gives no limit for the number of islands to implement the switch function. For the whole implementation of the 'switch' only one feedback is needed. This is a big advantage compared to the feedback network, described in section 7.3, which needs to be implemented for every island in the designed circuit.

7.5 Conclusions

In this chapter we have shown some methods to cope with random background charge fluctuations. These fluctuations manifest themselves as horizontal shifts in the periodic input-output relation of a (capacitive) SET circuit. Because of this undesired horizontal shift, information can be coded in the amplitude or in the period of the input-output relation. By sweeping the input signal across a few periods of the input-output relation the output signal will be a periodic signal with information coded respectively in the amplitude or in the frequency. More than one period is needed to create a redundancy to cope with the possibility that the background charge appeared in that specific period. For this type of background insensitive circuits there is a need for at least a rectifier. A possible implementation of such a rectifier is given in section 9.1.

Due to the use of more than one period, such a solution for coping with background charges is a slow signal processing solution. Another method proposed in this chapter is to compensate for background charges for each island separately. In the implementation of such a solution each building block is enlarged with a sensing circuit, which senses the error due to the appearance of a background charge, and compensates for this background charge. This is a possible solution for each separate island.

A disadvantage of the last solution is the fact that each island needs a complete circuit to compensate for background charges; hence the advantage of the small size of circuits build with SET junctions is lost. A solution for this is to use a system concept in which not every island needs a compensation circuit, but only each building block. This principle only works for the situations in which a compensation signal can be applied anywhere within the building block.

Which of the above solutions is best suited for a specific problem depends on the circuit in which the problem due to background charges appeared. For the appearance of background charges in a single C-SET transistor, in which the speed is no topic, the mentioned signal redundancy method can be used. But the moment the circuits are getting larger (more islands), the solutions have to be found in a different system approach, in which we can compensate for any error within the complete building block.
8

Coupling of SET sub-circuits

The first step in transforming a desired function into a circuit is to describe the function on a system level. After that, it is possible to split this desired function into smaller parts, the sub-systems (see figure 8.1). This is called the top-down approach.

![Diagram of a system and its sub-systems](image)

Figure 8.1: A complex function $F$ is split up into 5 less complex functions.

To translate the desired sub-system into sub-circuits is usually a big problem. The sub-circuits should not influence each other’s input-output relation. And a sub-circuit has two input and two output quantities (current and voltage), which are a direct consequence of the sub-circuits attached, while a (sub-)system has only one carrier for the information transferred between the sub-systems.

For a circuit implementation of those sub-systems, we have to choose a physical quantity (current or voltage) as a carrier for the information and make sure that no other physical quantities play a role. Ideally we can solve the problem by decoupling the sub-circuits in such a way that only one quantity (the information carrier) is transferred at the time.
When we are able to solve both problems: 1) The sub-circuits do not have any effect on each others input-output relation, and 2) only one quantity is the information carrier, a kind of system approach for circuit design is possible. The above-mentioned two problems are what we will call the problem of coupling. The output signal of one stage should be the input quantity of the next stage. When in an implemented function those quantities are different it should be converted to the same quantity. In the designed coupling circuits this conversion can be an extra task for the coupling block.

In practical situations we have to accept a non-ideal coupling with all its consequences. This will result in a certain deviation between the designed circuit and the desired system concept.

In this chapter we discuss a few aspects, which play an important part in the top-down design method described above. We start the chapter with a discussion about converting a system concept into a circuit, which results in a demand for the chosen coupling scheme. The second section contains a discussion on practical implementations and demands of the coupling blocks to maintain the system design approach. And we end this chapter with some examples to show the possible implementation of the methods discussed.

### 8.1 From a system design to a circuit design

In a system design only one quantity is the signal carrier. To go from a system design to a circuit design we should make sure that the physical quantity that is not the signal carrier, does not influence the behaviour of the desired function. In this section we describe the ideal solution for this problem: the use of ideal coupling blocks.

#### 8.1.1 The use of coupling blocks

In figure 8.2 the parts of a basic building block are drawn: 1) the transmission matrix\(^1\) of the designed sub-circuit \(K\), 2) the transmission matrix of the input coupling scheme \(B_i\), and 3) the transmission matrix of the output coupling scheme \(B_o\). The desired input-output function \(H\) is an element of the transmission matrix \(K\).

![Figure 8.2: The implementation of a sub-system with an input-output relation \(H(s)\) by the use of a sub-circuit \(K\) and two coupling blocks \(B_i\) and \(B_o\).](image)

\(^1\)The transmission matrix is also called chain-matrix and its parameters are also known as ABCD parameters.
The total building block, described by the input-output relations $H$, should have
one element equal to the desired input-output relation $H$. Some possible basic input-
output relations have been discussed in the chapters 5 and 6. Let $\psi$ be the physical
quantity vector. The matrix $H$ containing all possible input-output functions is de-
defined as
\[
\psi_{\text{out}} = H\psi_{\text{in}}
\]  
(8.1)
A sub-circuit has voltages and currents as input and output quantities, but also
charges can be an used quantity (charges are not described in this section).
Let $u_{hi}$ and $i_{hi}$ be the input voltage and the input current of the sub-circuit
respectively, and $u_{ho}$ and $i_{ho}$ be the output voltage and current of the sub-circuit
respectively (see figure 8.2).
\[
\begin{pmatrix}
  u_{hi} \\
  i_{hi}
\end{pmatrix}
= \begin{pmatrix}
  u_{ho} \\
  i_{ho}
\end{pmatrix}
= \begin{pmatrix}
  K_{11} & K_{12} \\
  K_{21} & K_{22}
\end{pmatrix}
\begin{pmatrix}
  u_{hi} \\
  i_{ho}
\end{pmatrix}
\]  
(8.2)
For the translation of a system concept to a circuit concept we need to make
sure that the single circuit quantity, which is the information signal carrier between
the desired sub-systems, is filtered from the other circuit quantities. For a complete
decoupling, such that only one physical quantity is transferred from the input to
the output, the coupling scheme connected to the input and to the output of the
transmission matrix $K$ (see figure 8.2), should contain one non-zero value only (and
the rest zeros).
Let the desired function of the sub-system be equal to the sub-circuits input-
output relation $K_{wy}$. In that case the other values of the total input-output matrix
$K$ should be made equal to zero. This can be obtained when adding an input and an
output coupling block, described by the functions $B_i$ and $B_o$ respectively.
For the sub-system we can write (see figure 8.2)
\[
\psi_{\text{in}} = B_iKB_o\psi_{\text{out}}
\]  
(8.3)
In the system concept we are free to choose a physical quantity (voltage or current)
to represent the signal.
Let $\zeta_{in}$ be the chosen physical quantity to represent the input signal, and let $\zeta_{out}$ be
the chosen physical quantity to represent the output quantity. Let the designed sub-
circuit have a desired input quantity $\zeta_{hi}$ and a desired output quantity $\zeta_{ho}$. The signals
quantity for $\zeta_{in}$ and $\zeta_{out}$ can be determined during the system level design, while the
signals quantities for $\zeta_{hi}$ and $\zeta_{ho}$ are determined by the sub-circuit implementation.
In other words: the position in the matrix $K$ of the desired input-output relation
determines the sub-circuits necessary input quantity ($\zeta_{hi}$) and output quantity ($\zeta_{ho}$).
We will call the series connection of an input coupling block, the sub-circuit, and
the output coupling block, as is shown in figure 8.2, a building block. Due to the
decoupling by the coupling blocks we are able to couple such a series connection
without destroying the desired function, hence the name building block.
Concluding: We can transform a sub-system, into a sub-circuit, which has only
one non-zero input-output relation, when we place an input and an output coupling
block. Both coupling blocks should have an input-output matrix with only a single
non-zero value.
8.1.2 Ideal coupling blocks

When assuming two possible input quantities \( u \) and \( i \) and two possible output quantities \( u \) and \( i \) there are four possible ideal coupling blocks, which will have a matrix with only one non-zero value. These four ideal coupling blocks are drawn in figure 8.3. For the rest of the derivation we will assume that the impedance \( R_c \) of the controlled source is zero for the ideal controlled voltage source and goes to infinity for the ideal controlled current source.

![Diagram of coupling blocks](image)

Figure 8.3: Four implementations of coupling blocks: a) a voltage to voltage converter, b) a current to current converter, c) a voltage to current converter, and d) a current to voltage converter.

A coupling block is in general

\[
\begin{pmatrix}
  u_{in} \\
  i_{in}
\end{pmatrix}
= B
\begin{pmatrix}
  u_{out} \\
  i_{out}
\end{pmatrix}
\]

(8.4)

The matrices belonging to the four possible coupling blocks are:

- Voltage to voltage converter (figure 8.3a, with \( R_c \to 0 \))

\[
\begin{pmatrix}
  u_{in} \\
  i_{in}
\end{pmatrix}
= X_{uu}
\begin{pmatrix}
  1 & 0 \\
  0 & 0
\end{pmatrix}
\begin{pmatrix}
  u_{out} \\
  i_{out}
\end{pmatrix}
\]

(8.5)

- Current to current converter (figure 8.3b, with \( R_c \to \infty \))

\[
\begin{pmatrix}
  u_{in} \\
  i_{in}
\end{pmatrix}
= X_{ii}
\begin{pmatrix}
  0 & 0 \\
  0 & 1
\end{pmatrix}
\begin{pmatrix}
  u_{out} \\
  i_{out}
\end{pmatrix}
\]

(8.6)

- Voltage to current converter (figure 8.3c, with \( R_c \to \infty \))

\[
\begin{pmatrix}
  u_{in} \\
  i_{in}
\end{pmatrix}
= X_{ui}
\begin{pmatrix}
  0 & 1 \\
  0 & 0
\end{pmatrix}
\begin{pmatrix}
  u_{out} \\
  i_{out}
\end{pmatrix}
\]

(8.7)

- Current to voltage converter (figure 8.3d, with \( R_c \to 0 \))

\[
\begin{pmatrix}
  u_{in} \\
  i_{in}
\end{pmatrix}
= X_{iu}
\begin{pmatrix}
  0 & 0 \\
  1 & 0
\end{pmatrix}
\begin{pmatrix}
  u_{out} \\
  i_{out}
\end{pmatrix}
\]

(8.8)
The use of these ideal coupling blocks is only needed when a full decoupling is desired. Only one of the four can be used a time.

8.2 Designing of coupling blocks

To design complex functions that are built from smaller (less complicated) structures, we should be able to couple those smaller basic functions. Coupling in nanoelectronics is a major problem, not only due to the fact that any change in environment also changes the behaviour (like the tunnel condition) but also due to the fact that the information signal is created by one or a few electrons.

The designed sub-circuit might work well, but combining the sub-circuits can cause a lot of problems. Even measuring these sub-circuits is not as easy as it looks. In this section some solutions are given for the coupling of the different kind of subcircuits, by adding so called coupling blocks.

There are some ideas posted about coupling of single-electron devices. One of those ideas is to couple the blocks by using ‘regular’ components, like CMOS [81, 110, 111], shown in figure 8.4a. A big disadvantage of this kind of coupling scheme is the current through the gate of the transistors (in the figure called $i_g$). This can be a very low current, but even an extremely low current is still too high for single-electron devices. In those devices it needs to be possible to store a single electron on a node, any current from that node will completely destroy this desired behaviour. A second structure proposed to couple the devices is coupling them by a buffer stage build with a single-electron tunneling transistor [83], shown in figure 8.4b. In spite of its name a current of many electrons ($i_{ds}$) will flow through such a structure, giving rise to high power dissipation. Also more complex structures, like the SET inverter from Tucker [114], can be used [83], see figure 8.4c.

The coupling scheme can be separated in a few tasks schematically drawn in figure 8.5. The different functions of the coupling scheme do not always take place.

1. Impedance decoupling: The behaviour of the attached building block should not be changed by the coupling scheme used. Because the functionality, like the critical voltage, is mainly influenced by the impedance seen, impedance decoupling is one of the functions that should be included in the coupling scheme.

But also the functionality of the coupling scheme itself is influenced by the impedance of the blocks attached to the coupling scheme, so impedance decoupling on both sides of the coupling scheme is needed.

2. Bias separation: The functionality of the coupling scheme depends on its biasing. To make sure biasing from the previous stage has no influence, bias separation is used.

For the building block that is coupled to the coupling block the same rule holds: the biasing of the coupling block should have no effect on the behaviour of the attached building block, so a second (output) bias separation is included in the coupling scheme.

3. Conversion: In some cases, when for example the output information signals quantity of the previous building block differs from the desired information
Figure 8.4: Three examples for coupling of single-electron devices. a) Coupling of the SET structure with the help of a CMOS structure. b) Coupling with the help of a C-SET transistor, or c) Coupling with the help of a SET inverter.

4. Directing: To make sure the signal variation at the output is not fed back to the input, some care should be taken in the coupling scheme for directing the information signal. An implementation of mainly capacitive components makes the coupling circuit bi-directional, hence can not be used.

5. Amplification: All the separate functions of the coupling scheme described here can cause a weakening of the information signal. To make sure the coupling block does not influence the information signals amplitude, a certain amplification is needed to get the information signal back on its old level, the total amplification should be $A = 1$. This can mean weakening ($A < 1$) or increasing ($A > 1$) the information signal.

When one or more of the problems above is not solved, a circuit design based on building blocks is impossible. There is one exception: some of the functions can be shifted into the functional block or the other coupling block, as long as it stays within the total building block the design based on building blocks is still possible.

Four of the above functions of the coupling block are discussed in more detail in the next four subsections (amplification was already discussed in section 5.3). In some cases more than one of the problems can be solved at the same time.
8.2 Designing of coupling blocks

![Image of coupling scheme]

Figure 8.5: The general functions of a coupling scheme, not always all the drawn functions are needed.

8.2.1 Impedance decoupling

The critical voltage in a given circuit depends on the impedance seen between the nodes where the junction is placed (see section 4.1). When the impedance is changed, due to the impedance of the next stage, the whole behaviour of the sub-circuit is changed. When synthesizing building blocks it is desirable to be independent of the impedance of the other blocks that are attached to the designed block. This can be obtained when the coupling scheme is implemented in such a way that the impedance of the next stage and the previous stage are neglectable or better not seen by the present stage (the stage under investigation). The impedance of the coupling scheme is in the ideal case also neglectable, but in practical cases this impedance is known. The impedance of the coupling block can be taken into account when synthesizing the building block.

![Diagrams of coupling blocks]

Figure 8.6: Four implementations of ideal coupling blocks: a) a voltage to voltage converter, b) a current to current converter, c) a voltage to current converter, and d) a current to voltage converter.

The ideal solutions were already shown in figure 8.3. When an input voltage is applied, the ideal solution for the impedance decoupling is an input coupling block with an input impedance $Z_{in}(s) \to \infty$ (see figure 8.6a and c). In case we have an output voltage, the output-impedance of the output coupling block should be $Z_{out}(s) \to 0$ (see figure 8.6a and d). And an ideal solution for the impedance decoupling, when a current signal is applied to a coupling block, is a coupling block with an input
impedance $Z_{in}(s) \to 0$ (see figure 8.6b and d). In case of an output current, the output impedance of the output-coupling block should be $Z_{out}(s) \to \infty$ (see figure 8.6b and c).

When we are able to design such an ideal voltage coupling circuit or current coupling circuit, the problem of directing the information (see section 8.2.4) does not exists anymore. Fan-out problems are solved also due to the fact that the ideal coupling blocks of figure 8.6 forms no load on the previous stage. To maintain a one-way direction this block is the best thinkable; any voltage (or current) applied to its output is not coupled to its input, hence it has only one direction! Also fan-in problems are solved due to the fact that the impedance is zero or infinite, and the source can deliver extra energy if needed.

A possible implementation of the voltage output coupling circuit, is the use of a large capacitor $C_L$ between the connecting wire of the two function blocks and ground. Due to such a large load capacitance the small input (gate) capacitance of the next stage is neglectable. In this way the input-output relation of the current stage is independent of the stages attached. This method is only possible for SET structures though which a high tunnel current is flowing, which makes it possible to charge this capacitor. In section 8.3 we will discuss a few examples with this kind of decoupling.

### 8.2.2 Separation of the bias signal from the information signal

In the previous section about impedance decoupling we assumed that there was only an information signal at the output. In practise we will also have a bias signal at the output. To bias each designed block independent we should separate the bias signal from the information signal.

In most circuits separation of bias and information signals is making a distinction between AC and DC signals. This is what is known as 'separation in the frequency domain'. It can simply be implemented by using a filter.

Another possible solution can be using a different physical quantity for the biasing as for the information signal. For instance when we choose a voltage information signal, we can use the current domain for the biasing. As mentioned earlier, section 5.1.2, a current will give rise to time dependencies due to a mostly capacitive circuit. Using current as a bias quantity will give the same problem: the biasing becomes time dependent.

In SET building blocks, like in circuits build with normal components, bias quantities determine the implemented function. When two building blocks are coupled, the DC signals play a direct part in the biasing of the coupled building blocks (capacitive dividing principle). To be able to split the circuit synthesis in an independent design of separate sub-circuits, there is the need for bias separation between those sub-circuits. A few solutions can be thought of, to separate the bias circuitries of the different sub-circuits. Some of those are described in this section.

Care should also be taken that there is no signal feedback through the designed bias circuitry.
Differentiator

In standard electronic designs we can decouple the bias of the different building blocks by so called coupling capacitors $C_{co}$. This only works in those cases where the input of the building blocks will have a resistive impedance making the combination of the coupling capacitor a differentiator, see figure 8.7. Constant offsets, like bias sources or constant environmental offsets are tuned away, differentiated to zero.

![Diagram of coupling capacitor and impedances](image)

Figure 8.7: The coupling capacitor $C_{co}$ in combination with the resistive part of the input impedance $Z_{in}(s)$ of the next circuit form a differentiator, so DC signals are not transferred to the next building block.

In the impedances $Z_{out}(s)$ and $Z_{in}(s)$ of figure 8.7 there should be a reactive part (real part). In SET structures (except the R-SET) this is not the case. A small change in the basic idea can help to overcome this problem; namely using a coupling resistor instead of a coupling capacitor.

A disadvantage of this kind of coupling scheme is, besides the fact that it is frequency dependent (filter function), it is unable to cope with constant levels, appearing in most digital signals. Digital signals with a constant value (in the binary case '1' or '0') are also differentiated to zero. Adding an integrator that starts to work after all the outputs of the circuit, due to the bias sources, have been differentiated to zero can solve this problem. This kind of coupling is possible but is hard to realise with a small circuit.

Another solution can be the use of a different coding scheme for digital signals. A scheme should be used in which the changes in the signal are an identification for the binary code ('0' or '1'). Examples of such coding schemes are on-off-keying (OOK), in which a carrier signal is switched on and off by the binary basis signal, or frequency-shift-keying (FSK), which is identical to modulating a carrier with a binary signal [26].

An other solution for overcoming the problem of bias signals at the output is by just subtracting those signals from the output [125], as is schematically drawn in figure 8.8. This kind of solution is also hard to implement because the multiplication factor $X_A$, with which the bias signal should be multiplied, depends on the output load of the block (depending on the circuit that is coupled to it). The impedance of the next circuit could be neglectable when using a correct impedance decoupling scheme (see section 8.2.1). This will make the multiplication factor $X_A$ a constant. The feedback through the adder can be a problem in practical situations.
Figure 8.8: A schematic overview of how to remove the bias signal from the output signal of the circuit by subtracting the bias signal.

8.2.3 Conversion of a signal quantity

To obtain some freedom in the function block design, described in the chapters 5 and 6, no demands were made on the choice in signal quantity. When signals need to be converted between the blocks this should be done by the coupling blocks, because the choice for the input signal of the input coupling block and the output signal of the output coupling block is determined on the system level. The choice of the input and output signal quantity in the implemented function is determined in the circuit design of that function.

In figure 8.6c the ideal conversion scheme is drawn for converting a voltage to a current with conversion factor $X_{ui}$ and in figure 8.6d the ideal conversion scheme is drawn for converting a current to a voltage with a conversion factor $X_{iu}$.

It is common in SET circuits to use three types of circuit elements: capacitors, junctions, and in some special cases resistors. Those three circuit elements can also be used for conversion, which will result in an approximation of the ideal conversion shown in figure 8.6c and d. For this reason it is important to know their limitations:

1. A resistor (figure 8.9a): A resistor is normally used for current to voltage (and visa versa) conversion. But a resistor combined with the capacitive SET junctions and capacitors create time dependent signals in the circuit. We prefer not to use resistors due to many problems like large chip surface, heating, inaccuracy, etc. A resistor also can make the circuit slower due to the introduction of $RC$-times.

2. A capacitor (figure 8.9b): A capacitor is normally used for charge to voltage (and visa versa) conversion. A capacitor makes a direct current path impossible, only dielectric current is flowing. This current, that will flow through the capacitor, is the derivative of the applied voltage, and hence it is time depending.

3. A SET junction (figure 8.9c): Through the insulator of the SET junction tunneling is possible, introducing some stochastics. When a constant voltage is applied across the junction the average tunnel current will have a resistor-like behaviour (see section 2.5). When the voltage across the junction is lower than the critical junction voltage $u_j^{cr}$ the junction will behave like a normal capacitor.
8.2 Designing of coupling blocks

Depending on the desired application one of the elements described above can be chosen for the conversion.

(a) \hspace{1cm} (b) \hspace{1cm} (c)

![Diagrams](image)

Figure 8.9: a) A resistor $R$, b) a capacitor $C_c$, and c) a SET junction TJ as a converting component.

8.2.4 Directing a signal

Ideally when a signal is processed within a building block no attention has to be paid to the undesired feedback (also called back propagation). The directing problem appears when the designed couple structure is based on components that are not uni-directional (like resistors and capacitors).

There should be no important feedback from the driven stage(s) by the coupled driver block. Feedback from the driven stage should be neglectable (so in figure 8.10 $H_3 \approx 0$). Also the signal coupling between two driver stages (figure 8.11a) or two stages which are driven (figure 8.11b) should be neglectable (so $H_2 \rightarrow 0$ and $H_3 \rightarrow 0$).

In the design of the directing function we should make sure that it is not possible for signals from the next stage to destroy the desired behaviour of the present stage. This can be done by implementing a directing block, which makes the flow of signals from the next stages to the present stage impossible.

![Diagram](image)

Figure 8.10: The feedback through $H_3$ should be neglectable, $H_3 \approx 0$.

In figure 8.12 a simple example is shown. During the design of the stages no special care was taken for directing the signals. Let $C_j$ be the capacitance of a tunnel junction TJ then we can write for the output voltage of stage one, $u_{out,1}$

$$u_{out,1}(t) = u_{in,1}(t) \frac{C_g}{C_\Sigma} + q_1 \epsilon(t) \frac{1}{C_\Sigma} + q_2 \epsilon(t) \frac{1}{C_\Sigma} \frac{C_g}{2C_g + C_j} + u_{in,2}(t) \frac{C_g}{C_\Sigma} \frac{C_g}{2C_g + C_j}$$

(8.9)
Figure 8.11: There should be no feedback between building blocks that are placed in parallel ($H_3 \to 0$ and $H_4 \to 0$), in case of (a) fanin or (b) fanout.

with

$$C_{\Sigma} = C_g + C_j + \frac{C_g (C_g + C_j)}{2C_g + C_j}$$

(8.10)

In the example shown any voltage change or change in the independent charge due to a tunnel event, somewhere in the circuit (for this example: $u_{in,2}$, $q_2$) will give a change in the output voltage of the first stage $u_{out,1}$. Also the capacitances of the second stage take part in the output voltage of the first stage. Both situations are undesired.

Figure 8.12: The output voltage of the first stage ($u_{out,1}$) is not only a consequence of the input of that stage ($u_{in,1}$), but also due to applied input voltage at the next stage ($u_{in,2}$) and the change in the independent island charge due to a tunnel event that occur in stage 2.

If the signal from the next stage is coupled back we should make sure it is coupled back only partially. So the voltage at the output of stage one of figure 8.12 should
be determined by everything that is happening in the following stages only by a very small fraction. This should be implemented in the designed coupling block.

Let $\mathbf{K}$ be the transmission coefficient of a coupling block (see figure 8.13a), with

$$\vartheta_{in} = \mathbf{K} \vartheta_{out}$$ (8.11)

And let $\mathbf{J}$ be the inverse of the $\mathbf{K}$ matrix (shown in figure 8.13b), so

$$\mathbf{J} = \begin{bmatrix} J_{11} & J_{12} \\ J_{21} & J_{22} \end{bmatrix} = \mathbf{K}^{-1} = \frac{1}{\det \mathbf{K}} \begin{bmatrix} K_{22} & -K_{12} \\ -K_{21} & K_{11} \end{bmatrix}$$ (8.12)

so

$$\vartheta_{out} = \mathbf{J} \vartheta_{in}$$ (8.13)

Figure 8.13: a) The transmission matrix $\mathbf{K}$. b) The inversion of the transmission matrix $\mathbf{J} = \mathbf{K}^{-1}$.

The desired coefficients of $\mathbf{J}$ of the designed coupling block, should be as small as possible, with at least the coefficient $K_{ij}$ larger than $J_{ij}$. Because

$$J_{11} = \frac{K_{22}}{\det \mathbf{K}} \quad \text{and} \quad J_{22} = \frac{K_{11}}{\det \mathbf{K}}$$ (8.14)

This implies that $\det \mathbf{K} > 1$. Due to this demand a two-port consisting of only resistors, capacitors, inductors, and transformers is never suited to function as a coupling block. Such a two port is called reciprocal, and has $\det \mathbf{K} = 1$ [9, 17, 27, 98, 105, 109].

A possible solution to the directing problem is drawn in the block diagram of figure 8.14a. In this case an input signal, which is the combination of the bias part and the input information signal, is compared to a certain value $\zeta_{th}$ (see figure 8.14b). When the signal reaches this threshold level it will be amplified with a factor $X_A$. The input-output relation of the threshold building block is drawn in figure 8.14b. After dividing it by a factor $X_A$, it will have the same amplitude as the initially applied signal. Due to the non-symmetrical threshold scheme this method is only useable without loss of information for positive signals.

The threshold value $\zeta_{th}$ should be a little bit higher than the bias level, so $\zeta_{th} > \zeta_{bias}$. If only the bias source is applied to this circuit, the input is weakened by the threshold and even further weakened by the $X_A$ divider.

This scheme also works for overcoming feedback from the next stage. A signal coming from the output (see figure 8.15c) will first be divided by $X_A$, now the amplitude is too low for the threshold level. When the threshold level block has an amplification
Figure 8.14: a) Block diagram for a coupling scheme for directing signals, using a threshold building block. b) The threshold function of the threshold block.

Figure 8.15: A digital signal (a) applied to the input of the coupling block of figure 8.14 will give an output as shown in (b). When the signal of figure (c) is applied to the circuit on the output, due to the $X_A$-dividing and the threshold, only a very small signal on the input can be measured (d).

of $A < 1$ for $\zeta_{in} < X_{th}$ the signal will even be made smaller by the threshold level block, in which case it will arrive at the input with almost no amplitude left (see figure 8.15d).

In figure 8.16 the implementation with SET junctions and capacitors of figure 8.14 is shown. The response in both directions is shown in figure 8.17. From this figure it is clear that a suppression of a signal from output ($u_B$) to input ($u_A$) is obtained (of
a factor $\frac{20}{0.03}$. While a signal applied at the input ($u_A$) is amplified 1.3 times to the output ($u_B$).

Figure 8.16: The realization of the proposed system of figure 8.14 in SET junctions, to solve the directing problem.

Figure 8.17: The simulation results of the circuit of figure 8.16. We replaced the input circuit and the output circuit by a capacitor of $C_{L,in} = C_L = 120aF$. For the other component values of the designed coupling circuit of figure 8.16: $C_1 = 1aF$, $C_2 = 2aF$, $C_3 = 1aF$, $C_f = 1aF$, $C_b = 1aF$, $C_{in} = 10aF$, and $u_{b,he} = 80.1mV$. The simulation is done with SIMON. In the top two pictures a voltage change in $u_A$ of $\Delta u_A = 20\mu V$ gives a response on $u_B$ with a change of $\Delta u_B = 26\mu V$. In the lower two pictures the signal is applied in the reverse direction. The basic signal is applied on $u_B$ with a change of $\Delta u_B = 20\mu V$ and we obtain a smaller change in the voltage $u_A$ equal to $\Delta u_A = 0.03\mu V$. 
8.3 Example circuits

In this subsection we will discuss a few examples: the voltage and current biased SET transistor, the three-junction structure, and the Tucker inverter. We will describe the five functions of a coupling block described in the previous section in all the examples: impedance decoupling, bias separation, conversion, amplification, and directing.

8.3.1 Voltage biased SET transistor

In figure 8.18 three voltage biased SET transistors, the basic blocks, are drawn.

![Figure 8.18: Three voltage biased SET transistors coupled using resistors.](image)

*Conversion:* The SET transistor is often expressed in a current through the SET junctions as a function of the voltage across both junctions (see figure 8.19). The only way to couple these transistors in that regime is when there is a conversion from the current through the present stage to an input voltage of the next stage. This conversion can be implemented by using a resistor (see figure 8.18).

*Amplification:* Due to the fact that there is a large current flowing through the device, which creates the output voltage drop across the resistor, the small amount of charge needed on the gate capacitor of the next stage can be neglected. This large current is controlled by a small charge that can be a part of an electron.

*Directing:* Because large currents are flowing through the structure, no directing problem will occur.

*Impedance decoupling:* By choosing the resistors such that the combination with the input capacitance is much smaller than the tunnel time, the resistor can be neglected (replaced by a short), or when the combination is much larger than the tunnel time,
Figure 8.19: A typically (simulated) drain-source current $i_{ds}$ as function of the drain-source voltage $u_{ds}$ of an asymmetrical C-SET transistor. For the simulation we used $q_i = 0C$, $C_g = 1aF$, the capacitance $C_j$ of both tunnel junctions is $C_j = 1aF$, and the tunnel resistor $R_T$ of both junctions is $R_T = 500k\Omega$.

the resistor can be seen as very high ohmic (replaced by an open). In the first case the output impedance of the previous stage and the input impedance of the next stage have no effect on the behaviour of the current stage. While in the second situation the impedance seen by the junctions of the current stage is determined by the output capacitance of the previous stage and the input capacitance of the next stage.

Separation of bias signals: The separation of the bias signal is implemented by the formation of a differentiator due to the couple resistor and the input capacitance $C_g$ as was discussed in section 8.2.2. And when the transistor is placed in Coulomb blockade the DC current through the structure is zero. This makes the amount of output voltage due to biasing zero in both cases.

8.3.2 Current biased transistor

It is also possible to bias the SET transistor with a current source. In this subsection, like in subsection 8.3.1, the topics needed for coupling of sub-circuits are discussed.

As a problem of this type of circuits the current source has to be mentioned. Each device should have its own current source. A current source is still hard to make in SET technology, and will cost a lot of space on the chip when it is implemented by standard circuit components.

The current delivered to the circuit should be low enough, so a tunnel event through one of the junctions can take place before the junction is recharged. Otherwise the capacitor $C_L$ will be charged to a very high voltage. So in formula; the current is
Figure 8.20: Two current biased SET transistors coupled by using large load capacitors $C_L$.

This current bias $i_{bias}$ is given by

$$i_{bias} = \frac{dq}{dt}$$  

(8.16)

The current through the junctions is formed by a series of tunnel events (as was discussed in section 3.1.5). An electron tunnels after an average wait time $\tau_w$. The tunnel event itself will take a so called tunnel time $\tau_t$. In which case the total tunnel event costs $\tau_w + \tau_t$ time. Within that time a charge build by the current source should be less than one electron, so (using equation 3.21)

$$i_{bias} < \frac{e}{\tau_w + \tau_t}$$  

(8.17)

Conversion: Conversion is not needed; we already have a voltage output due to the current biasing.

Amplification: Coupling of these structures (see figure 8.20) can be done by placing a large load capacitor $C_L$ in parallel to the output. When this load capacitor $C_L$ is much larger than the input capacitance of the transistor of the next stage (which is by approximation $\frac{2C_sC_j}{C_p+2C_j}$) we are able to couple circuits without significantly changing the individual critical voltage.

The load capacitor also makes the circuit slowly time varying. Due to the fact that the current source charges the capacitor we will have a time dependency. By choosing a large capacitor and a very small current value, the voltage change across the capacitor per time unit is very small. Total time independence is not possible in this structure, but the output voltage of the structure is made to vary slowly this way. The current source will always charge the capacitor until the voltage across one of the junctions is high enough to let an electron tunnel. Its behaviour is easy to predict as long as the change in output voltage due to the change in charge (injected by the current source) on the capacitor is neglectable, during the tunnel event (equation 8.17).

The output voltage $u_{out}$ will change because the load capacitor is charged and discharged by means of the current source and by the tunneling of electrons. The output voltage will follow the border between the Coulomb blockade region and the region of free tunneling. This is due to the fact that when the output voltage across the load capacitor is much larger than the Coulomb blockade many electrons will start
tunneling until the transistor is back in Coulomb blockade. The current source will put the transistor out of this Coulomb blockade region, making tunneling of electrons possible again. In this way there is a kind of feedback created, making the output voltage almost equal to the Coulomb blockade voltage.

**Directing:** The large number of electrons stored on the load capacitance $C_L$ will make sure that changes in the next stages (such as tunneling of electrons) are not of influencing the present stage.

**Impedance decoupling:** The large $C_L$ ($C_L \gg \{C_1, C_2, C_q\}$) will make the output impedance low ohmic, which is a good situation for a voltage driver. In this way the impedance decoupling is accomplished.

**Separation of bias signals:** There is no need for a circuit implementation to separate the bias signals due to the fact that we bias in the current domain and the signals are in the voltage domain.

### 8.3.3 Three junction structures

One of the basic blocks of type 2 is the C-SET transistor, which can be voltage or current biased (as was discussed in the previous two subsections). A current biased C-SET transistor will give a voltage output signal, and hence the input quantity as well as the output quantity is a voltage. The bias current source can be implemented by a voltage source $u_{b,he}$ with a large resistor in series. The current-voltage relation of a resistor can be mimicked by a voltage biased SET junction $TJ_R$, as will be discussed below. In this way we obtain a three junction structure as is shown in figure 8.21.

This three junction structure shows only the response of a current biased C-SET transistor when the load capacitor, the tunnel resistor of the SET junction $TJ_R$, and the bias voltage source $u_{b,he}$ are chosen big enough.

Let $C_R$ be the capacitance of the tunnel junctions $TJ_R$. A junction will have a very low critical voltage when the junction capacitance or a capacitance in parallel is very large. Such a junction will show (almost) no Coulomb blockade. A load capacitor $C_L$ with a very large capacitance value ($C_L \gg \{C_R, C_j, C_q\}$), will result in the three-junction structure in a very small critical voltage $u^{cr}_R$ of junction $TJ_R$, in the ideal case the critical voltage is zero. Let $C_j$ be the capacitance of a tunnel junction $TJ_j$, then we can write for the critical voltage of junction $TJ_R$

$$u^{cr}_R = \frac{e}{2\left(C_R + C_L + \frac{C_q(C_q+2C_j)}{2C_j+C_q}\right)} \approx \frac{e}{2C_L} \quad (8.18)$$

Let $u_{out}$ be the maximal output voltage. When a large bias voltage $u_{b,he}$ is used ($u_{b,he} \gg u_{out}$), the voltage across the tunnel junction $TJ_R$ is almost constant. Let $u_{jR}$ be the voltage across $TJ_R$, then we can write

$$u_{jR} = u_{b,he} - u_{out} \approx u_{b,he} \quad (8.19)$$

When this almost constant voltage is larger than the critical voltage of tunnel junction $TJ_R$ (so $u_{b,he} \gg \frac{e}{2C_L}$), a tunnel current can flow through the junction. Due to the almost zero critical voltage of SET junction $TJ_R$ and the fact that the voltage across the junction can be seen as constant, the tunnel current through the tunnel junction $TJ_R$ can be seen also as constant. The relation between the current through the
junction $TJ_R$ and the voltage across the junction will be the tunnel resistance of that junction $R_{TR}$, hence junction $TJ_R$ will show a resistor-like behaviour. So when applying a constant $u_{bias}$ this will result in a constant current, and hence we have created a current source.

For example Goossens [47] has used the three junction structure to simulate a SET transistor excited by a current source (see his appendix A). He implemented the current source in this way due to the fact that there were no SET simulators with current sources at that time.

![Diagram of SET transistor](image)

**Figure 8.21:** A basic block of type 2 called the C-SET transistor with in series a junction $TJ_R$ to convert the bias voltage $u_{b,he}$ into a bias current.

**Conversion:** No conversion is needed; the output signal and the input signal are both voltage signals.

**Amplification:** The amplification of the three junction structure is equal to the amplification of the current biased C-SET transistor discussed in section 8.3.2 when $C_L$ and $u_{b,he}$ are chosen very large, as was described in the beginning of this section. The amplification depends on the capacitive values of the junction and the normal capacitance of the used building block of type 2. The input-output function of the C-SET is periodic and hence the amplification obtained depends on the chosen position of the operating window.

In figure 8.22 the input voltage $u_{in}$ is shown. Due to the fact that this input voltage is swept across a few periods (a period is equal to $\frac{2}{f_0}$ as was discussed in section 6.2) of the periodic input-output relation, the output voltage $u_{out}$ is also periodic. The simulated input and output power, and the power delivered by the bias source are also shown.

**Directing:** Due to the large load capacitance $C_L$ a change inside the next stage will have a neglectable effect on the voltage across the load capacitor $C_L$, so the output of the present stage is not influenced.

**Impedance decoupling:** The structure with only three junctions (without a large $C_L$) has a problem with coupling to another SET structure; when we connect the next (same type of) stage this will directly influence the current stage. A decoupling in the form of a large load capacitor is commonly used to overcome this problem, see figure 8.21. The voltage output has a low ohmic impedance due to this load capacitor.
Figure 8.22: With SIMON simulated input and output voltage (respectively \( u_{\text{in}} \) and \( u_{\text{out}} \)) for the circuit of figure 8.21 with \( C_g = 60aF \), \( C_j = 40aF \), \( R_{Tj} = 100k\Omega \), \( C_L = 4fF \), and \( u_{b,he} = 1V \). For the junction TJ\(_R\) the parameters are \( C_R = 40aF \) and \( R_{TR} = 1T\Omega \). To determine the output power the 3 junction structure of figure 8.21 is coupled to the same structure (with the same component values). The input power \( P_{\text{in}} \) and output power \( P_{\text{out}} \) are determined by the first order approximation \( P_x \approx C_x u_x \frac{\Delta u_x}{\Delta t} \), with \( C_x \) the capacitance of respectively the output of the current stage \( (C_x \approx 4fF) \) and the input of the next stage \( (C_x \approx 34aF) \). The power delivered by the voltage source \( u_{b,he} \) \( (P_{ubv}) \), is calculated using \( P_{ubv} = i_{ubv} u_{b,he} \), with \( i_{ubv} \) the current through this voltage source.

*Separation of bias signals:* Using superposition we can write for the bias voltage across the output (other sources not taken into account).

\[
    u_{\text{out}} = u_{b,he} \left[ \frac{C_R}{C_R + C_L + \frac{C_j(C_g + C_j)}{2C_j + C_g}} \right] \approx u_{b,he} \frac{C_R}{C_L}
\]

By making the \( C_L \gg C_R \) the voltage at the output due to the bias source is neglectable.

### 8.3.4 The Tucker inverter

An other example of a SET structure is the Tucker inverter [114] also called the 3-island structure shown in figure 8.23. This structure consists of two building blocks of type 2: the C-SET transistors (each containing two junctions) connected in series. The blocks are decoupled by a large load capacitor to make both basic blocks voltage biased and independent of each other. If this load capacitor is chosen too small the basic blocks can not be described separately, the whole structure will function like 4 tunnel junctions in series. The design is based on a standard CMOS inverter; hence
we need two transistors in series of which only one is conducting at the time. This can be obtained in the structure by capacitively connecting extra bias sources to the island. For both basic blocks different bias values are needed to obtain, compared to the CMOS principle design, a p-type and a n-type transistor behaviour. These extra sources are not drawn in figure 8.23 to keep the structure simple, but they can be found in the literature about the inverter (for example [114]).

![Simplified circuit of the Tucker inverter](image)

Figure 8.23: Simplified circuit of the Tucker inverter: two voltage biased C-SET transistors in series, with a large output capacitor $C_L$ to decouple them.

**Conversion:** When the load capacitor $C_L$ is large, the current through one of the two basic blocks can be stored on the load capacitor. In this way the current is transformed into an output voltage $u_{out}$.

**Amplification:** The inverter structure is based on a standard CMOS inverter. One of the two basic blocks (C-SET transistors) is in Coulomb blockade, while the other conducts. A large current will flow, which charges or discharges the large load capacitor $C_L$. This makes it possible that a small input voltage can create a large output voltage (see figure 8.24), due to the sensitivity of this kind of structures. When the next stage is capacitively coupled with a small capacitance, as an input signal for the next stage a small charge is needed. A current is flowing through the inverter structure, making the movement of such a small charge neglectable.

In figure 8.24 the input voltage $u_{in}$ is shown. The output voltage $u_{out}$ shows one period, clearly the response of an inverter. Also the input power $P_{in}$ and output power $P_{out}$, and the power delivered by the bias source $P_{ubo}$ are shown.

**Directing:** A signal change in one of the next stages, is neglectable due to the large capacitor $C_L$, and as a consequence the large amount of stored charge.

**Impedance decoupling:** Also in this example the large load capacitance creates a low ohmic output, as can be expected from a (good) voltage signal driver.

**Separation of bias signals:** When the load capacitor $C_L$ is much larger than the capacitances of the tunnel junctions and gate capacitances the output voltage due to bias voltage source $u_{b,he}$ is neglectable.
Figure 8.24: With SIMON simulated input and output voltage (respectively $u_{in}$ and $u_{out}$) for the circuit of figure 8.23 with $C_g = 8aF$, $C_j = 1aF$, $R_T = 100k\Omega$, $C_L = 2.4fF$, and $u_{b,he} = 6mV$. The top island is coupled with a capacitance of $C_{b1} = 7aF$ to the ground, and the bottom island is coupled with a capacitance $C_{b2} = 7aF$ to the source $u_{b,he}$. The 3 island structure of figure 8.23 is coupled to the same structure (with the same component values) with a coupling capacitance $C_{co} = 100aF$. The input power $P_{in}$ and output power $P_{out}$ are determined by the first order approximation $P_x \approx C_x u_x \Delta u_x / \Delta t$, for $P_{in}$ and $P_{out}$ $C_x \approx 3.7aF$, and for $P_{out}$ $C_x \approx 2.4fF$. The power delivered by the voltage source $u_{b,he}$ ($P_{ubv}$), is calculated using $P_{ubv} = i_{ubv} u_{b,he}$, with $i_{ubv}$ the current through this voltage source.

8.3.5 Conclusions

The in this section shown circuit examples all have one resemblance: a current due to tunnel events, is flowing through the structure. Due to this current, these structures are less sensitive for directing problems. To be able to design each block separately a large load capacitor is placed at the output of each block. With this load capacitor a high capacitive output is created, and thus the capacitive input of the next stage is neglectable. Also the bias signals are due to this large capacitor, neglectable at the input of the next stage.
Part III

Examples and validation
In this chapter we will discuss some circuit examples. For the description of those circuits the methods described in the previous chapters are used. Like the critical voltage (section 4.1), the operating window (section 5.2), and the periodicity (section 6.2).

Due to the unavailability of simulators that can handle all components in agreement with our theory, most circuits discussed in this chapter contain only capacitances, junctions, and voltage source. Known simulators (SIMON [131] and MOSES [19]) give simulation results, for the circuits which consists of the mentioned basic elements, equal to the predicted outcome according to our theory, discussed in chapter 3.

We will only discuss a few structures, with which more insight is obtained due to the derivation using our theory. By doing so another functionality can be found for the described basic sub-circuits. Those structures can with the help of our theory be expressed in a clear formula describing their behaviour. These formulas can be used to derive the capacitance values from the measurement results (see chapter 10) or can be used to design more complex structures by coupling simple well-known building blocks (see chapter 8). Or they can even be used to synthesize a specific function (see chapter 5).

We start this chapter with a discussion of a structure in such a way as is common in the literature, hence a discussion about a current consisting of electrons tunneling through a junction. Our model can only give the voltage value (the critical voltage) of the border between current and no current, in other words the voltage value such that the structure is just in Coulomb blockade. The example is a double junction structure. With the help of the found expression for the borders of the Coulomb blockade we can bias the structure in such a way to function as a diode. With the help of such a structure we should be able to design the necessary rectifier for the in section 7.2 proposed methods to cope with random background charges.

Secondly we will discuss the electron-box structure. By using the operating window as was discussed in section 5.2 we are now able to synthesis complex functions with just a simple structure. The electron-box makes it possible to make complex
functions by using single-electron behaviour. Also the use of the periodicity to make more complex functions, as was discussed in chapter 6, can be implemented in an electron-box structure.

We end this chapter with two sections about the more generally accepted structures, respectively the C-SET transistor and the electron pump (two island structure). To be able to explain the measurements, both structures are analysed with the help of our models of the SET junction and the independent island charge. With the help of the analytically derived expressions the component values can be extracted from the measurement results, which will be done in chapter 10.

For all the simulations and calculations done in this chapter the assumption is made that no fluctuating background charges appear. We also assume that all the circuit examples discussed in this chapter are settled for $t = 0$ and will settle immediately after a tunnel event.

### 9.1 Double junction

In figure 9.1a two junctions are shown, placed in series\(^1\). The critical voltage of each junction depends on the direct surrounding (see chapter 4). Let $C_{J1}$ be the capacitance of SET junction $TJ_1$ and let $C_{J2}$ be the capacitance of tunnel junction $TJ_2$. For simplicity we will assume that the connected circuit is a voltage source or a circuit with a very large output capacitance $C_L$ (so $C_L \gg \{C_{J1}, C_{J2}\}$).

\[ u_{\text{in}}^{cr} = \frac{e}{2(C_{J1} + C_{J2})} \]  

(9.1)

Let $u_{j1}$ be the voltage across junction $TJ_1$, let $u_{j2}$ be the voltage across junction $TJ_2$, let $u_{\text{in}}$ be the input voltage, and let $u_{\text{bias}}$ be the bias voltage. We can express the junction voltages in terms of the bias voltage $u_{\text{bias}}$ and the input voltage $u_{\text{in}}$ (we

\(^1\)The sub-circuit described here is a one-port and hence not one of the basic blocks (see section 5.3.2) due to the lack of an input and an output with the same physical quantity.
9.1 Double junction

assume a zero independent charge on node \( w \).

\[
    u_{j1}(t) = \frac{C_{j2}}{C_{j1} + C_{j2}} u_{in}(t) + \frac{C_{j2}}{C_{j1} + C_{j2}} u_{bias}(t) \tag{9.2}
\]

\[
    u_{j2}(t) = \frac{C_{j1}}{C_{j1} + C_{j2}} u_{in}(t) + \frac{C_{j1}}{C_{j1} + C_{j2}} u_{bias}(t) \tag{9.3}
\]

An electron tunnels when one of the two junction voltages is larger than the critical voltage of equation 9.1. The voltage across the junction that has the smallest capacitance value will be the first one to reach this critical voltage, after which an electron can tunnel, and hence a current can flow. Let \( C_{\text{max}} = \max\{C_{j1}, C_{j2}\} \). The relation between the input current \( i_{in} \) and the input voltage \( u_{in} \) is shown in figure 9.1b.

To shift the whole graph such that the slope in the first quadrant of the graph of the current as function of the voltage goes through the origin, we need a bias voltage of

\[
    u_{bias} = \frac{e}{2C_{\text{max}}} \tag{9.4}
\]

In this case we obtain a function of which any positive input voltage results in a current and any (small) negative input voltage (\( |u_{in}| < \frac{e}{C_{\text{max}}} = 2u_{bias} \)) is blocked. This function can be used as a diode. The simulation results are shown in figure 9.2.

![Figure 9.2: Simulation results of the circuit of figure 9.1a for \( C_{j1} = C_{j2} = 1\mu F \) and \( u_{bias} = 80mV \). a) The applied input voltage \( u_{in} \) and b) the current \( i_{in} \) that flows through the structure.](image)

A disadvantage of this structure is that it has a different output quantity (current) as input quantity (voltage). Another disadvantage is that this structure allows a current to flow from the input, in the design step this should be taken into account.
9.2 Electron-box structures

One of the basic SET devices is the electron-box (see figure 9.3). It is well described in the literature, for example in [18, 31, 52, 84], and was already realized a long time ago [85].

![Diagram of electron-box structure]

Figure 9.3: The electron-box structure.

The electron-box consists of a single tunnel junction TJ with a capacitance $C_j$ and one 'normal' (non tunneling) capacitor $C_c$. Between these two components an island is created (node $w$). Let $u_j$ be the voltage across the tunnel junction TJ, and let $u_{b,he}$ be the voltage across the normal capacitor. A simulation result of the voltage across the junction due to the applied input voltage is shown in figure 9.4a. And in figure 9.4b the result of a simulation shows the well-known staircase of the electron-box.

Let $q_i$ be the independent charge on node $w$. For the electron-box it is easy to derive the two voltages $u_j$ and $u_{b,he}$

\[
  u_j(t) = u_{in}(t) \frac{C_c}{C_c + C_j} + \frac{q_i \epsilon(t)}{C_c + C_j} \quad (9.5)
\]

\[
  u_{b,he}(t) = u_{in}(t) \frac{C_j}{C_c + C_j} - \frac{q_i \epsilon(t)}{C_c + C_j} \quad (9.6)
\]

The independent charge $q_i$ on the floating node $w$ is due to initial charges, background charges, and discrete tunneling of electrons. When we assume that there are no background charges appearing in the circuit we obtain a period of (see section 6.2)

\[
  \Delta u_{in} = \frac{e}{C_c} \quad (9.7)
\]

From figure 9.4a we can directly see this periodicity which is occuring due to tunneling of electrons. We can also use this periodicity to make complex circuitry (see chapter 6). Or we can use the input-output relation of figure 9.4b to build multi level logic.

In the design of the NAND, NOR, inverter, and threshold, which we will discuss in the next subsections, it is enough to consider only the region near the first tunnel event. If we use a small $u_{in}$ we will only shift a little away from this event. A disadvantage of this, which we neglect for the moment, is the very sensitivity of random background charge fluctuations on the voltage relations drawn in figure 9.4, see also equation 9.5 and equation 9.6 and the discussion in chapter 7.
Figure 9.4: Simulation results obtained using SIMON of an electron-box as is shown in figure 9.3. a) The voltage across the junction \( u_j \) as function of the input voltage \( u_{in} \). b) The voltage across the normal capacitor, \( u_{b,he} \), as function of the input voltage \( u_{in} \). Both simulations are carried out with \( C_c = 40aF \), \( C_j = 40aF \).

We propose the sub-circuit depicted in figure 9.5, a more general case of the electron-box, as a programmable block. Let \( k_{in} \) be the number of inputs. The normal capacitor \( C_c \) is divided into \( k_{in} + 1 \) capacitors \( (C_{in,1}, \ldots, C_{in,k_{in}}, C_c) \), which allows us to create various digital building blocks. Let \( C_j \) be the capacitance of tunnel junction TJ, and let \( C_{\Sigma} \) be the sum of the capacitance values attached to node \( w \) (the island), so

\[
C_{\Sigma} = C_c + C_j + \sum_{d=1}^{k_{in}} C_{in,d}
\]  
(9.8)

We can write for the output voltage of the electron-box

\[
u_{out}(t) = \frac{u_{b,he}(t)C_c + \sum_{d=1}^{k_{in}} u_{in,d}(t)C_{in,d} + q_t \epsilon(t)}{C_{\Sigma}}
\]

(9.9)

The charge \( q_t \) is the total independent charge on the island, which is equal to \( ne \) (with \( n \) the number of electrons that left the island), when we assume that the background charge and the initial charge are zero. When the initial charge and background charge are not zero the bias voltage source \( u_{b,he} \) should be tuned until the effect of those charges is cancelled.

Let \( u_{j^*} \) be the critical voltage of junction TJ, which is equal to

\[
u_{j^*} = \frac{e}{2C_{\Sigma}}
\]

(9.10)
Figure 9.5: The proposed structure: an electron-box with $k_{in}$ extra input capacitors.

An electron can tunnel through tunnel junction TJ when the voltage across the junction is higher than this critical voltage.

The same results as discussed in the next subsections can be found for a few other bias voltages $u_{b,he}$ due to the periodic character of the electron-box.

9.2.1 A basic binary programmable building block

For the use of digital blocks it is of importance to define the logical levels. In this section we define a high input and a low input voltage respectively $u_{ih}$, $u_{il}$. For the output voltages we define a high and a low output voltage respectively $u_{oh}$, $u_{ol}$. This output voltage is equal to the voltage across the junction, see figure 9.5.

We also choose

$$ u_{il} = -u_{ih} \quad (9.11) $$

$$ u_{ol} = -u_{oh} \quad (9.12) $$

In general, if the output level is lower than the input level we need amplification to be able to connect the next block. In case the output level is higher than the input level we need to attenuate the output. Without tunneling the output signal of an electron-box will always attenuate the input signal. To have some fan-out we need amplification $A$ (also see section 5.3): $u_{oh} = u_{ih} A$, with $A > 1$. This can be obtained by biasing the junction close to its tunnel condition. Now only a small input voltage is necessary to let an electron tunnel, and by doing so a higher signal at the output can be reached than the original input signal.

Depending on how we choose the operating window we can implement different functions. When for example multiple operating windows are chosen, digital binary logic can be created, which is discussed below.

In the next three subsections we describe the basic binary blocks

1. NAND
2. NOR
3. Inverter

These basic blocks are based on the SET electron-box of figure 9.5. For simplicity we discuss the NAND and NOR function with only two inputs. More inputs can also be
Table 9.1: The 2-input NAND function, with \( u_{il} = -u_{ih} \). The numbers of the operating windows are those used in figure 9.6.

<table>
<thead>
<tr>
<th>( u_{in,1} )</th>
<th>( u_{in,2} )</th>
<th>( \sum u_{in} )</th>
<th>operating window</th>
<th>( u_{out} )</th>
</tr>
</thead>
<tbody>
<tr>
<td>( u_{il} )</td>
<td>( u_{id} )</td>
<td>( 2u_{il} )</td>
<td>0</td>
<td>( u_{ol} )</td>
</tr>
<tr>
<td>( u_{il} )</td>
<td>( u_{ih} )</td>
<td>0</td>
<td>1</td>
<td>( u_{ol} )</td>
</tr>
<tr>
<td>( u_{ih} )</td>
<td>( u_{il} )</td>
<td>0</td>
<td>1</td>
<td>( u_{ol} )</td>
</tr>
<tr>
<td>( u_{ih} )</td>
<td>( u_{ih} )</td>
<td>( 2u_{ih} )</td>
<td>2</td>
<td>( u_{oh} )</td>
</tr>
</tbody>
</table>

implemented in the same way. By changing the bias value of the voltage source \( u_{b,he} \), all three functions can be selected, while using the same structure.

The digital functions described in the next four subsections are simulated with the help of the simulator SIMON[131]. The simulation conditions were: \( T = 0K \), \( u_{ih} = -u_{il} = 100\mu V \).

**NAND**

To implement a NAND function, all the operating windows (using a multiple operating window scheme) should be placed in such a way that the output voltage is always high, except the highest placed operating window. In figure 9.6 the input-output relation of a two input electron-box is shown, in which the number indicates the number of inputs that is high (see also table 9.1). The highest operating window (for a two input NAND) is number '2', which indeed gives a low output voltage, hence the name: NAND function. The distance between two operating windows is a constant, and is determined by the amplitude of the applied input signals.

![Figure 9.6: The input-output relation of an electron-box with the chosen multiple operating windows to create a two input NAND function.](image)

Between operating window '1' and '2' an electron should tunnel (see the jump in voltage in figure 9.6). For the NAND we need to pull an electron to the island (so \( q_i \rightarrow q_i - e \)) when both of the inputs are high (\( \sum u_{in} = 2u_{ih} \)). Using equation 9.9 and equation 9.10 we obtain

\[
2u_{ih}C_{in} + u_{b,he}C_c > \frac{e}{2}
\]  

(9.13)
And the electron should tunnel when one of the inputs is low \((\sum u_{in} = 0)\)

\[ u_{b,he}C_c < \frac{e}{2} \quad (9.14) \]

Because we have chosen for positive and negative binary signals, the operating window '1' is true for \(\sum u_{in} = 0\), and hence the position of this window is completely determined by the bias condition (see figure 9.6). So the DC operating point should be within operating window '1'.

The output voltage should change as little as possible between the situation when one input is low and the situation that both inputs are low. From this we obtain the condition

\[ 2u_{il}C_{in} \ll e \quad (9.15) \]

When both inputs are low a difference in output voltage will arise compared to the situation where only one input is low, due to a slope of \(\frac{C_m}{C_x}\) in the input-output relation (see also figure 9.6). Let \(u_c\) be the maximally allowed difference in output voltage within one logic level, then we can write

\[ u_c = 2|u_{il}| \frac{C_{in}}{C_x} \quad (9.16) \]

This error voltage should be as small as possible. The output drop should be as large as possible compared to the error, so

\[ 2|u_{il}| \frac{C_{in}}{C_x} \ll \frac{e}{C_x} \quad (9.17) \]

Which is in agreement with equation 9.15.

In figure 9.7 the simulation results are shown for the electron-box biased as a NAND.

**NOR**

To implement a NOR function, all the operating windows (using a multiple operating window scheme) should be placed in such a way that the output voltage is always low, except for the lowest placed operating window. In figure 9.8 the input-output relation of a two input electron-box is used, the lowest operating window is number '0', which indeed gives a high output voltage, hence the name: NOR function (see table 9.2).

For the NOR we need to let an electron tunnel onto the island (and by doing so decrease the charge \(q_i, q_i \rightarrow q_i - e\) between operating window '0' and '1'. So the tunnel condition is in that case \((\sum u_{in} = 0)\)

\[ u_{b,he}C_c > \frac{e}{2} \quad (9.18) \]

And no electron should tunnel when both inputs are low

\[ 2u_{il}C_{in} + u_{b,he}C_c < \frac{e}{2} \quad (9.19) \]
Figure 9.7: The simulation results of the electron-box structure biased as a NAND, with $C_j = C_C = C_{in} = 40 aF$, $u_{b,he} = 1.9 mV$. In the figure is the error voltage also visible (at $t = 0.04s$). This error voltage is equal to $u_e = 50 \mu V$.

Table 9.2: The 2-input NOR function, with $u_{il} = -u_{ih}$. The numbers of the operating windows are those used in figure 9.8.

<table>
<thead>
<tr>
<th>$u_{in,1}$</th>
<th>$u_{in,2}$</th>
<th>$\Sigma u_{in}$</th>
<th>operating window</th>
<th>$u_{out}$</th>
</tr>
</thead>
<tbody>
<tr>
<td>$u_{il}$</td>
<td>$u_{il}$</td>
<td>$2u_{il}$</td>
<td>0</td>
<td>$u_{ol}$</td>
</tr>
<tr>
<td>$u_{il}$</td>
<td>$u_{ih}$</td>
<td>0</td>
<td>1</td>
<td>$u_{oh}$</td>
</tr>
<tr>
<td>$u_{ih}$</td>
<td>$u_{il}$</td>
<td>0</td>
<td>1</td>
<td>$u_{oh}$</td>
</tr>
<tr>
<td>$u_{ih}$</td>
<td>$u_{ih}$</td>
<td>$2u_{ih}$</td>
<td>2</td>
<td>$u_{oh}$</td>
</tr>
</tbody>
</table>

An error is obtained between the situation of $\Sigma u_{in} = 0$ (operating window ‘1’) and $\Sigma u_{in} = 2u_{ih}$ (operating window ‘2’), due to a slope in the input-output characteristic of the electron-box. Let $u_e$ be this error voltage, which is equal to

$$u_e = 2u_{ih} \frac{C_{in}}{C_S}$$  \hspace{1cm} (9.20)

This error should be small compared to the voltage drop due to a tunnel event, because that is the transition between high and low in the binary output, so

$$2u_{ih} \frac{C_{in}}{C_S} \ll \frac{e}{C_S}$$  \hspace{1cm} (9.21)

hence

$$2u_{ih}C_{in} \ll e$$  \hspace{1cm} (9.22)
Figure 9.8: The input-output relation of an electron-box with the chosen multiple operating windows to create a two input NOR function.

In figure 9.9 the simulation results are shown for the electron-box biased as a NOR.

Figure 9.9: The simulation results of the electron-box structure biased as a two input NOR, with $C_j = C_e = C_{in} = 40aF$, $u_{b,he} = 2.1mV$. In this figure the error voltage $u_e$ is visible (beginning at $t = 0.12s$). This error voltage is equal to $u_e = 50\mu V$.

**The inverter**

It is of course also possible to make the inverter from a NAND or a NOR by respectively making one input high or low. But in this way we would use one more capacitor than we really need.
To implement an inverter function, both the operating windows (using a multiple operating window scheme) should be placed in such a way that the output voltage is low, when the input is high and visa versa. In figure 9.10 the input-output relation of the electron-box is shown, the low operating window is number '0', which indeed gives a high output voltage, and the high operating window is '1' which gives a low output, hence the name: inverter function.

![Diagram of electron-box with multiple operating windows](image)

Figure 9.10: The input-output relation of an electron-box with the chosen multiple operating windows to create an inverter function.

For the inverter we need to pull an electron on the island when the input is high, making the output voltage drop

$$u_{ih}C_{in} + u_{b,he}C_c > \frac{e}{2} \quad (9.23)$$

No electron should tunnel if the input is low, to keep the output high, so

$$u_{il}C_{in} + u_{b,he}C_c < \frac{e}{2} \quad (9.24)$$

So the DC operating point (bias point) should be exactly in between the operating window '0' and the operating window '1′

$$u_{b,he} = \frac{e}{2C_c} \quad (9.25)$$

In figure 9.11 the simulation results are shown for the electron-box biased as an inverter.

**Programmable logic**

Because the logical functions implemented in the electron-box depends on the voltage applied as biasing, we can describe the logic presented in this section as programmable logic. By changing the bias voltage by a controller the total input-output relation can be controlled.

Because the position of the operating window is determined by the bias condition we can shift the operating windows by changing the bias voltages. In this way the logic developed with the same electron-box structure is changed when the bias voltage is changed, hence the name 'programmable logic'.
Figure 9.11: The simulation results of the electron-box structure biased as an inverter, with $C_j = C_c = C_{in} = 40aF$, and $u_{b,he} = 2mV$.

Table 9.3: The values of the bias voltages $u_{b,he}$ for three different digital functions.

<table>
<thead>
<tr>
<th>Function</th>
<th>$u_{b,he}$</th>
</tr>
</thead>
<tbody>
<tr>
<td>NAND</td>
<td>1.9mV</td>
</tr>
<tr>
<td>NOR</td>
<td>2.1mV</td>
</tr>
<tr>
<td>Inverter</td>
<td>2.0mV</td>
</tr>
</tbody>
</table>

The three digital functions, NAND, NOR, and inverter described above, have the same structure but a different bias voltage. The necessary bias voltages are shown in table 9.3.

The same results can be found for bias voltages $u_{b,he}$ which differ by the amount of $\frac{n e}{C_c}$ (with n an integer number) due to the periodic character of the electron-box. In that case the charge on the island changes between $n$ and $n - 1$ electron charge, instead of between zero and minus one electron charge.

9.2.2 Threshold function, EXOR and EXNOR

The EXOR, EXNOR and threshold function, which will be discussed in the next subsections, can use the same structure with only a difference in input capacitances $C_{in}$. 
Threshold blocks

A threshold function can easily be made with the help of the electron-box shown in figure 9.5. The design of a threshold is simple: just choose the number of operating windows equal to the threshold value minus one. For instance if we want to make a threshold function with a threshold equal to 5, we choose 4 operating windows to give a high output and the rest to give a low output. Care has to be taken that the maximal number does not reach the value where the output is high again (due to the periodic input-output relation of the electron-box). If this is the case either the width of the operating windows or the distance between the windows has to be reduced. The distance between the operating windows can be reduced by reducing either the input capacitance \( C_{in} \) or by reducing the input amplitude \( u_{ih} \). The width of the operating window can be reduced by allowing smaller fluctuations on the signal (using a stricter amplitude level for the high and the low voltages).

To get a positive threshold block (\( \geq \)), the electron-box as described here should be followed by an inverter stage. See figure 9.12 for the electron-box operating windows.

![Threshold blocks diagram](image)

Figure 9.12: The input-output relation of an electron-box with the chosen multiple operating windows to create a threshold function of < 5. When \( u_{il} = 0 \) the bias condition \( u_{b,he} C_c \) should be within operating window '0'.

So in this case of the threshold function < 5

\[
4u_{ih} C_{in} \ll \frac{e}{2}
\]

(9.26)

The maximal error voltage \( u_e \) obtained is (in case of \( u_{il} = 0 \))

\[
u_e = 4u_{ih} \frac{C_{in}}{C_\Sigma}
\]

(9.27)

As tunnel condition we should make sure the condition is reached between operating window '4' and operating window '5', we choose the middle (4.5)

\[
\frac{4.5u_{ih} C_{in} + u_{b,he} C_C}{C_\Sigma} = \frac{e}{2C_\Sigma}
\]

(9.28)

In figure 9.13 the simulation results are shown for the electron-box biased as an threshold function of < 5.
Figure 9.13: The simulation results of the electron-box structure biased as a threshold function of < 5, with $C_c = C_{in} = 40\mu F$, $C_j = 4\mu F$, and $u_{b,he} = 1.55mV$. As an input signal we used $u_{il} = 0$ and $u_{ih} = 100\mu V$.

**The EXOR function**

To implement an EXOR function, the operating windows (using a multiple operating window scheme) should be placed in such a way that the output voltage is high, when the sum of the inputs is odd and low when the sum is even.

In this section we define a high input and a low input voltage respectively $u_{ih}$, $u_{il}$. There are two methods to implement the EXOR function with an electron-box:

1. Using the same method as the in the previous subsection (section 9.2.1) described NAND and NOR, so a positive and a negative input level, and a limited number of inputs. The input signal $u_{ih}$ ('1') is a positive signal and the input signal $u_{il}$ ('0') is a negative signal: $u_{ih} = -u_{il}$.

2. Using the modulo function (as was discussed in section 6.3.2). For a binary EXOR function with $k_{in}$ inputs we can write

$$
\zeta_{out} = \begin{bmatrix} k_{in} \\ \sum_{d=1}^{k_{in}} \zeta_{in,d} \end{bmatrix} \pmod{2} \quad (9.29)
$$

which makes it possible to have an unlimited number of inputs. The input signal $u_{ih}$ ('1') is a positive signal and the input signal $u_{il}$ ('0') is zero.

Both will be discussed below.
Table 9.4: The 2-input EXOR function, with \( u_{il} = -u_{ih} \). The numbers of the operating windows are those used in figure 9.14.

<table>
<thead>
<tr>
<th>( u_{in,1} )</th>
<th>( u_{in,2} )</th>
<th>( \sum u_{in} )</th>
<th>operating window</th>
<th>( u_{out} )</th>
</tr>
</thead>
<tbody>
<tr>
<td>( u_{il} )</td>
<td>( u_{il} )</td>
<td>( 2u_{il} )</td>
<td>0</td>
<td>( u_{ol} )</td>
</tr>
<tr>
<td>( u_{il} )</td>
<td>( u_{ih} )</td>
<td>0</td>
<td>1</td>
<td>( u_{oh} )</td>
</tr>
<tr>
<td>( u_{ih} )</td>
<td>( u_{il} )</td>
<td>0</td>
<td>1</td>
<td>( u_{oh} )</td>
</tr>
<tr>
<td>( u_{ih} )</td>
<td>( u_{ih} )</td>
<td>( 2u_{ih} )</td>
<td>2</td>
<td>( u_{ol} )</td>
</tr>
</tbody>
</table>

The circuit looks the same in both cases, and is equal to the one drawn in figure 9.5, only the bias condition and/or the capacitor values are different for both implementations.

The first method uses a positive input signal as a '1' and a negative input signal as a '0'. We assume for simplicity a two input EXOR, so we can write down the four possible input-output relations, as is done in table 9.4.

The necessary operating windows for this kind of EXOR implementation are drawn in figure 9.14.

![Figure 9.14: The input-output relation of an electron-box with the chosen multiple operating windows to create an EXOR function with two inputs.](image)

Due to the fact that \( u_{ih} = -u_{il} \) the bias condition should be within operating window '1', so

\[
\frac{u_{b,he}}{C_c} = \frac{5}{4} e
\]  
(9.30)

The output voltage belonging to operating window '0' should be equal to the output voltage belonging to operating window '2', hence the distance between those two operating windows should be equal to (expressed in charges) one electron charge \( e \). So

\[
e = C_{in} \left( 2u_{ih} - 2u_{il} \right)
\]  
(9.31)

In figure 9.15 the simulation results obtained with SIMON are shown for this option.
Figure 9.15: The simulation results of the electron-box structure biased as a two input EXOR, with $C_j = C_c = 40aF$, $u_{b,he} = 5mV$, $C_{in} = 400aF$.

When we need to extend the EXOR function of this kind, to an EXOR function with three inputs (see table 9.5) we also need to change the bias voltage $u_{b,he}$. The DC operating point is determined in case of an even number of inputs, as a point within the operating window for which $\sum u_{in} = 0$. In case of an electron-box structure with an odd number of inputs the DC operating point is between the operating window for which $\sum u_{in} = u_{il}$ and the operating window for which $\sum u_{in} = u_{ih}$. This can be seen when comparing figure 9.14 to figure 9.16. The need for different bias conditions for electron-box structures with a different number of inputs is a disadvantage of this method to implement an EXOR function. For electron-box structures biased as modulo functions this will not be the case.

The second method was using a modulo function to implement the EXOR. This method has a disadvantage compared to the method described above: it needs an extra bias source (in series with the SET junction). To implement an EXOR function, the operating windows should be placed in such a way that the output voltage is low when the sum of the inputs is even and the output should be high when the sum is odd. In figure 9.17 the input-output relation of a multi input electron-box is shown, the numbers indicate the sum of the inputs that are high.

For simplicity we assume that we wish to implement an EXOR function with two inputs (see figure 9.18a) of which both capacitances $C_{in,1}$ and $C_{in,2}$ are equal. The SET structure of figure 9.18a will have an input-output relation as shown in figure 9.18b. This input-output relation is defined by the electron-box structure chosen. Let $u_0$ be the voltage offset of the input-output relation of the electron-box.

$$u_0 = \frac{C_j u_{b,ve} + C_c u_{b,he} + \frac{ne}{C_\Sigma}}{C_\Sigma}$$  \hspace{1cm} (9.32)

$$C_\Sigma = C_{in,1} + C_{in,2} + C_j + C_c$$  \hspace{1cm} (9.33)
Table 9.5: The 3-input EXOR function, with \( u_{il} = -u_{ih} \). The numbers of the operating windows are those used in figure 9.16.

<table>
<thead>
<tr>
<th>( u_{in.1} )</th>
<th>( u_{in.2} )</th>
<th>( u_{in3} )</th>
<th>( \sum u_{in} )</th>
<th>operating window</th>
<th>( u_{out} )</th>
</tr>
</thead>
<tbody>
<tr>
<td>( u_{il} )</td>
<td>( u_{il} )</td>
<td>( u_{il} )</td>
<td>( 3u_{il} )</td>
<td>0</td>
<td>( u_{ol} )</td>
</tr>
<tr>
<td>( u_{il} )</td>
<td>( u_{il} )</td>
<td>( u_{ih} )</td>
<td>( u_{il} )</td>
<td>1</td>
<td>( u_{oh} )</td>
</tr>
<tr>
<td>( u_{il} )</td>
<td>( u_{ih} )</td>
<td>( u_{il} )</td>
<td>( u_{il} )</td>
<td>1</td>
<td>( u_{ol} )</td>
</tr>
<tr>
<td>( u_{il} )</td>
<td>( u_{ih} )</td>
<td>( u_{il} )</td>
<td>( u_{il} )</td>
<td>2</td>
<td>( u_{oh} )</td>
</tr>
<tr>
<td>( u_{ih} )</td>
<td>( u_{il} )</td>
<td>( u_{il} )</td>
<td>( u_{il} )</td>
<td>1</td>
<td>( u_{ol} )</td>
</tr>
<tr>
<td>( u_{ih} )</td>
<td>( u_{il} )</td>
<td>( u_{ih} )</td>
<td>( u_{ih} )</td>
<td>2</td>
<td>( u_{ol} )</td>
</tr>
<tr>
<td>( u_{ih} )</td>
<td>( u_{il} )</td>
<td>( u_{il} )</td>
<td>( u_{il} )</td>
<td>2</td>
<td>( u_{oh} )</td>
</tr>
<tr>
<td>( u_{ih} )</td>
<td>( u_{ih} )</td>
<td>( u_{il} )</td>
<td>( u_{ih} )</td>
<td>3</td>
<td>( u_{ol} )</td>
</tr>
</tbody>
</table>

Figure 9.16: The input-output relation of an electron-box with the chosen multiple operating windows to create a three-input EXOR function.

Figure 9.17: The desired input-output relation of a multi input electron-box with the chosen operating windows to create an EXOR function based on the modulo function.

For the critical output voltage we can write

\[
u_{out}^{cr} = u_{j}^{cr} + u_{b,ve}
\]  

(9.34)
Further the period is known \( (\frac{e}{C_{in}}) \), the voltage drop due to a tunnel event is known \( (\frac{e}{C_{\Sigma}}) \), and the critical junction voltage is known \( (u_{ij}^{cr} = \frac{e}{2C_{\Sigma}}) \). With the help of these equations we can determine all the values of the components.

![Diagram](image)

Figure 9.18: a) A two input electron-box with two extra bias sources \( u_{b,ve} \) and \( u_{b,he} \) to shift the input-output relation. b) The input-output relation of the two input electron-box with bias sources.

The distance between two operating windows is constant and half a period (see figure 9.17), and should be equal to the amplitude of the high input signal.

\[
u_{ih}C_{in} = \frac{e}{2} \tag{9.35}\]

Equation 9.35 means that if we want to use the same input levels as defined with the NAND and the NOR we should use different input capacitors \( C_{in} \) than those of the NAND and NOR. Compare for example equation 9.35 with equation 9.22.

As an example we chose an input signal with an amplitude of \( u_{ih} = 1mV \) and \( u_{il} = 0mV \). The EXOR function is modulo 2 (see equation 9.29), so we need two input signals with a high amplitude to go to the next period (see figure 9.17). Using input signals with an amplitude of 1mV the period should be equal to 2mV. Because we assumed that both input capacitances are equal \( (C_{in,1} = C_{in,2} = C_{in}) \) we can derive the value of the input capacitors: \( C_{in} = 80aF \).

The electron-box should be biased such that it reaches operating window '0' without signals at the input. Because we want to use positive signals only, the whole input-output relation of figure 9.18b should be lifted to make it equal to figure 9.17, see figure 9.19a, so

\[
u_{out}^{cr} = \frac{e}{C_{\Sigma}} \tag{9.36}\]

See figure 9.19b for the necessary shifts.

Combining equation 9.36 with equation 9.34 we find for the voltage source \( u_{b,ve} \)

\[
u_{b,ve} = \frac{e}{2C_{\Sigma}} \tag{9.37}\]

Because a starting point \( u_0 = 0 \) is desired when all inputs are zero, this gives a direct consequence for the voltage source \( u_{b,he} \) (assuming no electrons have tunneled yet),
9.2 Electron-box structures

Figure 9.19: The graph should be shifted to obtain a positive input-output relation.
(a) After the correct bias sources are applied the output voltage is always positive and
is zero for zero input signals.  b) A horizontal shift equal to \( q_{b,h} \) and a vertical shift
equal to \( u_{b,v} \) should be applied by the bias sources.

which can be calculated using equation 9.32

\[
 u_{b,he} C_c + u_{b,ve} C_j = 0
\]  

(9.38)

Only the amplitude of the output voltage depends on the capacitance of \( C_j \) and \( C_c \), so
we are free to choose those. To get a signal which is as high as possible the capacitance
values should be chosen as small as possible. For simplicity we choose \( C_j = C_c \).

Because the electron will not tunnel directly when the critical voltage is reached
but rather when the voltage across the SET junction is a bit higher, and the electron
charge \( e \) is simplified in the calculations to \( 1.6 \cdot 10^{-19} \ C \), we need to compensate for
those small errors. This compensation can be done by choosing \( u_{b,he} \) slightly lower
than \( u_{b,ve} \), so \( u_{b,he} = -0.24mV \).

The simulated output voltage as function of time is shown in figure 9.20. The
simulation results confirm the expected output of an EXOR function.

The same results can be found for a few other bias voltages \( u_{b,he} \) due to the
periodic character of the electron-box. In that case the charge on the island does not
change between zero and minus one electron charge, but between \( n \) and \( n - 1 \) electron
charge.
The simulated response of a two input electron-box biased as an EXOR function based on modulo. The test conditions were: $T = 0K$, the amplitude of the input voltage $u_{in}$ is $u_{ih} = 1mV$, $C_{in,1} = C_{in,2} = C_{in} = 80aF$, $u_{b,he} = -0.24mV$, and $u_{b,we} = 0.25mV$. For simplicity we chose for the junction capacitance $C_j$ and the extra bias capacitance $C_c$ the same capacitive value as the input capacitors, $C_j = C_c = C_{in}$. The horizontal axis is in arbitrary time units.

The rise and fall time of figure 9.20 depend at this moment only on the simulator used, and are therefore not discussed here. The simulator used is based on an existing theory of tunneling that assumes a zero tunnel time. As long as the tunnel time is neglected the transition from high to low and visa versa, are in principle infinitely short.

The EXOR function implemented with the electron-box has no gain ($A < 1$), which can simply be solved by buffering the EXOR before coupling it to other structures. To get some gain it can for example be connected to one of the well-known circuit elements (BJT, JFET, etc.). Another method is to use an EXNOR and an inverter, in which case the last one amplifies the output signal to the correct amplitude again.

The EXNOR function

For the EXNOR we can use the same steps as for the EXOR. But in this case with a slightly different bias condition because the bias condition should be $\frac{3}{4}$ higher or lower than the one of the EXOR (compare figure 9.21 with figure 9.14). So equation 9.30 becomes

$$u_{b,he}C_c = \frac{3}{4}e$$  \hspace{1cm} (9.39)
or (due to the periodic behaviour)

\[ u_{b,he} C_c = -\frac{1}{4} e \]  

(9.40)

Figure 9.21: The input-output relation of an electron-box with the chosen multiple operating windows to create an EXNOR function.

See figure 9.22 for the simulation results. Also a modulo function can be used to implement the EXNOR. This is not further derived in this thesis, because it is the same procedure as for the EXOR function.

Figure 9.22: The simulation results of the electron-box structure biased as an EXNOR, with \( C_j = C_c = 40aF \), \( u_{b,he} = 3mV \), \( C_{in} = 400aF \).
9.2.3 The full-adder

The full adder can be made by combining the EXOR (with three inputs) and a building block with the threshold function $\geq 2$, see figure 9.23.

Figure 9.23: The basic circuit for a full adder. $\zeta_{su}$ is the output signal that represents the sum, and $\zeta_{ca}$ is the output signal that represents the carry.

In figure 9.24 the circuit, which is simulated, is represented. This combination of electron-boxes behave as described in table 9.6. The structure is a direct implementation of the system concept of figure 9.23. The simulation result for the two bit full adder is obtained by using the simulator SIMON, and is shown in figure 9.25. The amplitude of the output voltage of the carry ($u_{ca}$) is much larger than the voltage of the sum ($u_{su}$), due to the extra amplification obtained in the inverter.

Table 9.6: The full adder function.

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<tr>
<th>$\zeta_{in,1}$</th>
<th>$\zeta_{in,2}$</th>
<th>$\zeta_{in,3}$</th>
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9.2.4 An AD converter

With the help of electron-boxes it is also possible to create an analog to digital converter (ADC). In the literature some implementations of an ADC with SET junctions are proposed. For example Ahn and Kim [2] proposed a structure based on the SET inverter (3 islands, and 4 SET junctions). We propose a structure based on the electron-box.

There are different methods to design an ADC with electron-boxes. The methods discussed here are based on the residue after subtraction. In the analog signal the largest value of the binary representation (so 2, 4, 8, 16, 32, 64, etc) is subtracted
Figure 9.24: The implementation of a two bit full adder, of which the system concept is shown in figure 9.23. The implementation is done by electron-boxes. The adder is build by using a threshold logic \(< 2\), which is inverted to get the desired threshold function \(\geq 2\). The output of this threshold function is the carry of the two bit full adder.

and the residue is fed to the next stage where the same process takes place. The implementation of this method in electron-boxes can be done in a few ways.

1. Each following stage should have a threshold with a factor of two lower. The implementation of the threshold value can be done by choosing different capacitances. A disadvantage of this implementation is that by using electron-boxes, not only the threshold level is determined by the capacitance values, but also the amplitude of the output is determined by the same values. Hence this kind of scheme needs extra amplifiers with different amplification factors, to get all the output amplitudes back to one level.

2. The same scheme as the first implementation, only now the difference in threshold values is implemented by different bias schemes. Such an ADC needs to operate near the critical voltage. And the more stages (more bits) that need to be implemented, the more critical the bias voltage will become. This makes this kind of implementation hard to do in just a simple step, and it is very critical for small changes.

3. Design one block to implement the highest bit. By implementing amplification in the coupling block of a factor of two, no changes are needed in the biasing or
Figure 9.25: The simulation result of the two bit full adder drawn in figure 9.24. For device parameters we used as bias sources $u_{bs} = u_{bc} = 2mV$, $u_{bi} = 1mV$ and for the bias coupling capacitances $C_{bs} = C_{bc} = 40aF$ and $C_{bi} = 80aF$. The capacitances of the three SET junctions were $C_{js} = C_{jc} = C_{js} = 40aF$. For the two series of input capacitances we used $C_{in1s} = C_{in2s} = C_{in3s} = 400aF$, $C_{in1c} = C_{in2c} = C_{in3c} = 40aF$, and the coupling capacitance of the inverter was $C_{ini} = 4aF$.

in the capacitance values. Hence it will not have the problems of the previous two implementations.

By choosing the capacitance of the 'normal' capacitor much larger than the capacitance of the SET junction, an almost constant threshold level is obtained. This is because the slope between the input voltage of the electron-box and the voltage across the normal capacitor is very small ($\ll 1$). The rest of the voltage is in that case (as a consequence of Kirchhoff's voltage law) across the junction. When we apply this voltage to the next stage as an input (after multiplication by two) we can do the same thing over again. This concept is drawn in figure 9.26.

Let $\hat{u}_{in}$ be the maximal expected input voltage. To use the optimal range of the ADC the value for the constant $X$ of figure 9.26 should be chosen to be equal to

$$X \equiv \frac{\hat{u}_{in}(t)}{2}$$  \hspace{1cm} (9.41)

Let $\hat{u}_{out}$ be the amplitude of the output signal. We can write for this amplitude of the output signal

$$\hat{u}_{out} = \frac{e}{2C_\Sigma}$$  \hspace{1cm} (9.42)
Figure 9.26: An analog to digital converter concept, based on equal threshold levels. For each desired bit the same structure (with the same values) can be used. In this concept the value $X$ should be made equal to the voltage level at which the highest bit (most significant bit MSB) should be set to logic high. The indicated striped box can be implemented with a single-electron-box. $\zeta_r$ is the rest signal that is multiplied with 2 and fed to the next stage.

To prove our concept a 3-bit ADC is designed. This structure is shown in figure 9.27, and the simulated output is shown in figure 9.28.

Figure 9.27: The proposed electron-box structure to implement a 3-bit analog to digital converter with $X = \frac{E}{C^2}$.

9.3 C-SET transistor

When we place two junctions in series and on the so created floating node (the island) we connect another circuit element, a structure is created which is called SET transistor. Likharev was one of the first who spoke of a SET transistor [5]. Depending on the type of circuit element that is connected to the middle node the name for the structure is enlarged. There are a few types of SET transistors. When a capacitor is

\footnote{Only in case of a floating node the middle node $w$ is called island.}
connected to node \( w \) the SET transistor is called the C-SET transistor (shown in figure 9.29a). When a resistor is coupled to the middle node the transistor is called the R-SET transistor [88, 135] (shown in figure 9.29b). The middle node is not a floating node anymore. And when a diode is coupled to node \( w \) the transistor is called the D-SET transistor [77] (shown in figure 9.29c and d). A SET junction TJ\(_g\) can also be connected to node \( w \), which is called the J-SET, see figure 9.29e (also one of the basic building blocks of type 2 discussed in section 5.3.2). All kind of combinations are also possible. For example Wasshuber [130] discusses the RC-SET, which is a resistor and a capacitor (connected to node \( w \)) in series.

The C-SET transistor is the one discussed in this section and will be called SET transistor for short. This SET transistor consists of two SET junctions and at least one 'normal' capacitor coupled to the island (see figure 9.29a). The names used for the terminals are just like the ones of a Field Effect Transistor: source, drain, and gate.

The structure of figure 9.29a has two disadvantages compared to the electron-box structure described in the previous section.

- Two SET junctions are needed.
- A current will flow of a sequence of electrons that tunnel, it is impossible to speak of a single-electron input-output relation.

The SET transistor of figure 9.29a can be symmetrically biased by voltage sources (see figure 9.30a). The island charge can be modelled as a current source with value
Figure 9.29: Four different types of SET transistors a) the C-SET transistor, b) the R-SET transistor, c) and d) the D-SET transistor, and e) the J-SET transistor.

$q_i \delta(t)$, as was discussed in section 3.2. We can transport the voltage sources $u_{d1}, u_{d2}$ (shown in figure 9.30a), such that we get the circuit drawn in 9.30b.

The voltage sources directly in series with the capacitors and junctions can be changed into current sources, using the Norton equivalent, the result is shown in figure 9.30c. Let $C_{j1}$ be the capacitance of tunnel junction TJ$_1$ and let $C_{j2}$ be the capacitance of tunnel junction TJ$_2$. The current sources in figure 9.30c are equal to
(using Laplace $\mathcal{L}$)

\[
    i_{ug}(t) = \mathcal{L}^{-1}\left\{ U_g(s) sC_g \right\}
\]

\[
    i_{d1}(t) = \mathcal{L}^{-1}\left\{ U_{d1}(s) sC_{j1} \right\} \quad (9.44)
\]

\[
    i_{d2}(t) = \mathcal{L}^{-1}\left\{ U_{d2}(s) sC_{j2} \right\} \quad (9.45)
\]

Because the four current sources are now in parallel they can be added, in that way the circuit of figure 9.30d is formed, with

\[
    i_i(t) = i_{ug}(t) + i_{d1}(t) - i_{d2}(t) + q_i \delta(t)
\]

\[
    i_i(t) = \mathcal{L}^{-1}\left\{ U_g(s) sC_g + U_{d1}(s) sC_{j1} - U_{d2}(s) sC_{j2} + Q_i \right\} \quad (9.47)
\]

\[\text{(a)}\]

\[\text{(b)}\]

\[\text{(c)}\]

\[\text{(d)}\]

Figure 9.30: a) A symmetrical voltage biased C-SET transistor. b) Transporting the voltage sources $u_{d1}$ and $u_{d2}$ in the SET transistor of figure 9.30a. c) Using the Norton equivalent to convert the voltage sources $u_{gs}$, $u_{d1}$, and $u_{d2}$ of figure 9.30b into current sources. d) The simplified circuit of the SET transistor of figure 9.30a.

From the circuit of figure 9.30d we can calculate the voltages across the tunnel junctions. Let $u_{j1}$ be the voltage across tunnel junction $TJ_1$, let $u_{j2}$ be the voltage across $TJ_2$, and let $C_{\Sigma}$ be the sum of the capacitances connected to the island

\[
    C_{\Sigma} = C_{j1} + C_{j2} + C_g \quad (9.48)
\]
Then we can write for the voltages across the SET junctions
\[
\begin{align*}
  u_{j1}(t) &= u_{d1}(t) - \mathcal{L}^{-1} \left\{ \frac{I_i(s)}{s C_\Sigma} \right\} \\
  u_{j2}(t) &= \mathcal{L}^{-1} \left\{ \frac{I_i(s)}{s C_\Sigma} \right\} + u_{d2}(t)
\end{align*}
\] (9.49)
(9.50)

The critical voltage is reached when
\[
\begin{align*}
  u_{j1}(t) &= u_{j1}^c = \frac{e}{2 C_\Sigma} \\
  u_{j2}(t) &= u_{j2}^c = \frac{e}{2 C_\Sigma}
\end{align*}
\] (9.51)
(9.52)

### 9.3.1 The periodicity

The graph of the function of \( u_{ds} \) as a function of \( u_g \) will show periodicity due to tunneling to and from an island (as was discussed in section 6.2). In figure 9.31 this graph is shown. Following the same method as the one discussed in section 6.2 we can derive the period. Let \( \sigma \) be a situation and \( \sigma + 1 \) be another situation, then we obtain the same output voltage \( (u_{ds}) \) when

\[
Q_i^\sigma + s C_g U_g^\sigma(s) = Q_i^{\sigma+1} + s C_g U_g^{\sigma+1}(s)
\] (9.53)

If we assume that the random background charge \( q_{bg} \) is not changed, between situation \( \sigma \) and \( \sigma + 1 \), then one electron is the smallest amount of change in \( q_i \). This will give a periodicity of

\[
\Delta u_g = u_g^\sigma(t) - u_g^{\sigma+1}(t) = \frac{e}{C_g}
\] (9.54)

And hence a periodicity of \( \frac{e}{C_g} \) is obtained.

### 9.3.2 The slopes

Using the expressions in which the voltages across the SET junctions is equal to the critical voltage, equation 9.51 and equation 9.52, we can calculate the slopes we would obtain when we draw the graph in which we express the drain-source voltage as a function of the gate voltage (assuming \( u_{d1}(t) = u_{d2}(t) = u_d(t) \)).

\[
\begin{align*}
  U_d(s) - \left( \frac{Q_i}{s C_\Sigma} + \frac{U_g(s)s C_g}{s C_\Sigma} - \frac{U_d(s)s C_{j1}}{s C_\Sigma} - \frac{U_d(s)s C_{j2}}{s C_\Sigma} \right) &= \frac{e}{2 C_\Sigma} \\
  \left( \frac{Q_i}{s C_\Sigma} + \frac{U_g(s)s C_g}{s C_\Sigma} + \frac{U_d(s)s C_{j1}}{s C_\Sigma} - \frac{U_d(s)s C_{j2}}{s C_\Sigma} \right) + U_d(s) &= \frac{e}{2 C_\Sigma}
\end{align*}
\] (9.55)
(9.56)

Both equations can be simplified into respectively

\[
\begin{align*}
  U_d(s) \left( C_\Sigma - \frac{C_{j1}}{C_\Sigma} + \frac{C_{j2}}{C_\Sigma} \right) &= \frac{e}{2} + \frac{Q_i}{s} + U_g(s) C_g \\
  U_d(s) \left( C_\Sigma - \frac{C_{j2}}{C_\Sigma} + \frac{C_{j1}}{C_\Sigma} \right) &= \frac{e}{2} - \frac{Q_i}{s} - U_g(s) C_g
\end{align*}
\] (9.57)
(9.58)
So equation 9.51 can be rewritten into

$$U_d(s)\left(2C_{j2} + C_g\right) = \frac{e}{2} + U_g(s)C_g + \frac{Q_i}{s}$$  \hspace{1cm} (9.59)

For junction TJ$_1$ when $u_d = \frac{u_{ds}}{2}$ we will find a slope in the graph of $u_{ds} = f(u_g)$ of

$$\frac{u_{ds}}{u_g} = \frac{C_g}{C_{j2} + \frac{C_g}{2}}$$  \hspace{1cm} (9.60)

And for junction 2, we can rewrite equation 9.52 into

$$U_d(s)\left(2C_{j2} + C_g\right) = \frac{e}{2} - U_g(s)C_g - \frac{Q_i}{s}$$  \hspace{1cm} (9.61)

when $u_d = \frac{u_{ds}}{2}$ we will find a slope in the graph of $u_{ds} = f(u_g)$ of

$$\frac{u_{ds}}{u_g} = -\frac{C_g}{C_{j1} + \frac{C_g}{2}}$$  \hspace{1cm} (9.62)

The results obtained for both slopes (see figure 9.31) can also be found in the literature [5, 56, 83, 88].

![Graph of $u_{ds}$ as function of $u_{gs}$ for a symmetrically excited SET transistor](image)

Figure 9.31: The graph of $u_{ds}$ as function of $u_{gs}$ for a symmetrically excited SET transistor

### 9.3.3 The amplitude

The slopes expressed in equation 9.60 and equation 9.62 are slopes for which respectively junction TJ$_1$ and junction TJ$_2$ reach the critical value. These slopes will have an intersection point (this is defined as the point where they both have the same $u_g$ and the same $u_{ds}$). Let $u_{ds}^{cr1}$ and $u_{ds}^{cr2}$ be the critical values expressed in the drain-source...
9.3 C-SET transistor

voltage such that respectively tunnel junction TJ1 and tunnel junction TJ2 reach their critical voltage. So the intersection point will be

\[ u_{ds}^{cr1} = u_{ds}^{cr2} = u_{ds}^{cr} \]  \hspace{1cm} (9.63)

Using equations 9.51 and 9.52 we can find for this data point (see figure 9.31)

\[ u_{ds}^{cr} = u_{j1}^{cr} + u_{j2}^{cr} = \frac{e}{C \Sigma} \]  \hspace{1cm} (9.64)

9.3.4 Influence of load capacitors and island capacitors

In this section we discuss the influence a source has on the equation of the critical voltage of the tunnel junction of a C-SET transistor. For simplicity we use the asymmetrical C-SET transistor, which is biased with either a voltage source or a current source, connected between the drain and source. In this section it will be shown that when large capacitances are placed across the bias source and signal source, the critical voltage for both junctions will be independent of the types of sources used.

Let \( u_{ds} \) and \( i_d \) be respectively the voltage source and current source connected between the drain and source, and let \( u_{gs} \) and \( i_{gs} \) be respectively the voltage source and current source connected between the gate and source. Four situations are described in this section

1. \( u_{ds} \) and \( u_{gs} \) (figure 9.32a)
2. \( u_{ds} \) and \( i_{gs} \) (figure 9.32b)
3. \( i_d \) and \( u_{gs} \) (figure 9.32c)
4. \( i_d \) and \( i_{gs} \) (figure 9.32d)

Also the influence of the island capacitance \( C_i \) is described in the derived equations for the critical voltage.

The use of sources: \( u_{ds} \) and \( u_{gs} \)

The circuit of figure 9.32a is the SET transistor placed in a low ohmic environment. The voltage sources are ideal sources, so they have no internal resistance. The critical voltage for junction TJ1 and junction TJ2 is

\[ u_{j1}^{cr} = u_{j2}^{cr} = \frac{e}{2(C_i + C_{j1} + C_{j2} + C_g)} \]  \hspace{1cm} (9.65)

From this equation it is easy to conclude that extra load capacitors \( C_L \), and \( C_{gl} \) have no influence, this was already concluded by Averin and Likharev [5].

The use of sources: \( u_{ds} \) and \( i_{gs} \)

Due to the high ohmic impedance of the gate current source a floating node is created between the exciting source \( i_{gs} \) and the gate capacitance (see node \( w_g \) in figure 9.32b).
Figure 9.32: a) A SET transistor in a completely low ohmic environment. b) A SET transistor in a high ohmic gate environment. c) A SET transistor in a high ohmic drain environment. d) A SET transistor in a completely high ohmic environment.

The critical voltage for tunnel junction TJ₁ and tunnel junction TJ₂ is

\[ u_{j1}^{cr} = u_{j2}^{cr} = \frac{e}{2 \left(C_{j1} + C_{j2} + C_i + \frac{C_g C_{gl}}{C_g + C_{gl}} \right)} \]  (9.66)

From this equation we can directly see that an extra load capacitor \( C_L \) has no influence.

When \( C_{gl} \gg C_g \), which is a correct assumption from a practical point of view, we can simplify the equation such that we obtain equation 9.65.

**The use of sources: \( i_d \) and \( u_{gs} \)**

Due to the high ohmic impedance of the drain current source a floating node is created between the exciting source \( i_d \) and the tunnel junction TJ₁ (see node \( w_d \) in figure 9.32c).
The critical voltages for tunnel junction $TJ_1$ and tunnel junction $TJ_2$ are

\[
u_{j1}^{cr} = \frac{e}{2 \left( C_{j1} + \frac{C_L(C_{j1}+C_{j2}+C_g)}{C_{j1}+C_{j2}+C_g} \right)} \tag{9.67}
\]

\[
u_{j2}^{cr} = \frac{e}{2 \left( C_{j2} + C_i + \frac{C_{j1}C_L}{C_{j1}+C_L} \right)} \tag{9.68}
\]

It is clear that in this case the load capacitance $C_{gl}$ has no influence.

When $C_L >> C_{j1}$ and $C_L >> C_i + C_{j2} + C_g$, which is a correct assumption from a practical point of view, we can rewrite these equations, which then result in equation 9.65 again.

**The use of sources: $i_d$ and $i_{gs}$**

Due to the high ohmic environment two floating nodes are created; one between the exciting source $i_d$ and tunnel junction $TJ_1$ (node $w_d$ in figure refOmgevingd), and the other one between the exciting gate current source $i_{gs}$ and the gate capacitor (see node $w_g$ in figure 9.32d).

The critical voltages for tunnel junction $TJ_1$ and tunnel junction $TJ_2$ are

\[
u_{j1}^{cr} = \frac{e}{2 \left( C_{j1} + \frac{C_L C_{j1} + C_i + C_{j2} + C_g}{C_{j1} + C_{j2} + C_g + C_{gl}} \right)} \tag{9.69}
\]

\[
u_{j2}^{cr} = \frac{e}{2 \left( C_{j2} + C_i + C_{j1} + C_L \right)} \tag{9.70}
\]

When $C_L >> C_{j1}$ and $C_L >> C_i + C_{j2} + C_g$, and $C_{gl} >> C_g$, which are correct assumptions from a practical point of view, we can rewrite these equations. The results will be the same as equation 9.65.

### 9.3.5 Current-voltage characteristic

Usually it is not the drain-source voltage as a function of the gate voltage that is investigated in the literature, but the relation between the current through both junctions as a function of the drain-source voltage when a fixed gate voltage is applied. With these graphs a direct translation from standard circuits with CMOS transistors to SET transistors is possible.

Let $i_{ds}$ be the drain-source current, which is the current through both junctions. When we consider the current-voltage $(i_{ds} - u_{ds})$ relation of the SET transistor we can distinguish three regions (see figure 9.33):

1. **No current (region A).** This is called the Coulomb blockade. It appears when both junctions in the circuit do not satisfy the tunnel condition (equation 9.51 and equation 9.52). This region ends when the voltage across one of the junctions is higher than the critical voltage, so the condition is met for either junction

\[
u_{j1} > u_{j1}^{cr} \land \nu_{j2} \leq u_{j2}^{cr} \tag{9.71}
\]
or for junction 2

\[ u_{j1} \leq u_{j2}^{cr} \land u_{j2} > u_{j2}^{cr} \]  

(9.72)

Because the graphs are drawn for a constant gate voltage we can, using equations 9.59 and 9.61, rewrite these condition into (with \( u_{d1}(t) = u_{d2}(t) = u_d(t) \)), respectively

\[ \frac{\frac{\varepsilon}{2} \epsilon(t) + u_g(t)C_g + q_i \epsilon(t)}{2C_{j2} + C_g} < u_d(t) \leq \frac{\frac{\varepsilon}{2} \epsilon(t) - u_g(t)C_g - q_i \epsilon(t)}{2C_{j1} + C_g} \]  

(9.73)

or

\[ \frac{\frac{\varepsilon}{2} \epsilon(t) - u_g(t)C_g - q_i \epsilon(t)}{2C_{j1} + C_g} < u_d(t) \leq \frac{\frac{\varepsilon}{2} \epsilon(t) + u_g(t)C_g + q_i \epsilon(t)}{2C_{j2} + C_g} \]  

(9.74)

So we can rewrite this into the condition for the SET transistor, for the border between region A and B

\[ u_d(t) = \min \left\{ \frac{\frac{\varepsilon}{2} \epsilon(t) - u_g(t)C_g - q_i \epsilon(t)}{2C_{j1} + C_g}, \frac{\frac{\varepsilon}{2} \epsilon(t) + u_g(t)C_g + q_i \epsilon(t)}{2C_{j2} + C_g} \right\} \]  

(9.75)

In figure 9.33 region A is: 0 < \( u_{ds} = 2u_d < 6.8mV \).

2. Single-electron current (region B). This is the region where only one of the junctions of the circuit satisfies the tunnel condition. After tunneling of one single electron this junction is in blockade again, but immediately the other junction satisfies the tunnel condition.

This region ends when the voltage across both junctions is higher than the voltage needed to let an electron tunnel. So for the symmetrical SET transistor both conditions

\[ u_{j1} > u_{j1}^{cr} \]  

(9.76)

and

\[ u_{j2} > u_{j2}^{cr} \]  

(9.77)

are met. Using equations 9.59 and 9.61 this will give

\[ u_d(t) > \frac{\frac{\varepsilon}{2} \epsilon(t) - u_g(t)C_g - q_i \epsilon(t)}{2C_{j1} + C_g} \]  

(9.78)

and

\[ u_d(t) > \frac{\frac{\varepsilon}{2} \epsilon(t) + u_g(t)C_g + q_i \epsilon(t)}{2C_{j2} + C_g} \]  

(9.79)

So we can rewrite this into the condition for the SET transistor, for the border between region B and C

\[ u_d(t) = \max \left\{ \frac{\frac{\varepsilon}{2} \epsilon(t) - u_g(t)C_g - q_i \epsilon(t)}{2C_{j1} + C_g}, \frac{\frac{\varepsilon}{2} \epsilon(t) + u_g(t)C_g + q_i \epsilon(t)}{2C_{j2} + C_g} \right\} \]  

(9.80)

In figure 9.33 region B is: 6.8mV < \( u_{ds} = 2u_d < 22mV \).
Figure 9.33: A typically (simulated) drain-source current $i_{ds}$ as function of the drain-source voltage $u_{ds}$ of a C-SET transistor (see figure 9.30a), showing the different current regions. For the simulation we used $u_{d1} + u_{d2} = u_{ds}$, $u_g = 21 mV$, $q_i = 0C$, $C_g = 3aF$, $C_{j1} = 1aF$, $C_{j2} = 5aF$, $R_{T1} = 100k\Omega$, $R_{T2} = 900k\Omega$.

3. **High current (C).** The voltages across all the junctions are above the critical voltage and tunneling occurs all the time through both junctions. This region is approximately linear when the tunnel resistances are almost equal.

The fact that the island charge $q_i$ appears in equations 9.75 and 9.80 immediately shows that a SET transistor can be placed in or out side region B by random fluctuating charges as was discussed in section 7.1. For simplicity reasons we will assume that the initial charge and the background charge are zero for the rest of this section, so just before the first electron tunnels there is no independent charge at all on the island, $q_i = 0$, and after $n$ electrons have tunnelled, $q_i = ne$.

**Different times in single-electron tunneling behaviour**

When the voltage across the junction is larger than the critical voltage it is possible for an electron to tunnel. Due to the stochastic behaviour of electron tunneling the electron will not tunnel immediately but after a certain time, the wait time, $\tau_w$ (see section 3.1.4). Let $\tau_w$ be the wait time, $t_b$ be the moment in time just before the tunnel event, $t_a$ the moment in time just after the tunnel event, $t^{cr}$ the moment in time the critical voltage is reached across the junction, and $\tau_t$ the tunnel time, then we can write (see figure 9.34)

$$t_b = t^{cr} + \tau_w \quad (9.81)$$

When we are looking at a current we are looking at more than one electron. The average current is defined as the number of electrons that are passing the point where
we are measuring within one second. This can be written as

\[ i = \frac{ne}{\Delta t} \]  

\textbf{(9.82)}

\textbf{Behaviour of tunneling of one electron at a time}

Single-electron current can be reached when the junctions are biased in such a way that only one SET junction meets the tunnel condition \( u_j(t) > u_{jt} \).

We can force the symmetrically biased SET transistor (shown in figure 9.35) in region B of figure 9.33. For this region we should make the voltage \( u_d \), less than the one of equation 9.80 but larger than equation 9.75.

\textbf{Figure 9.35: The C-SET transistor.} The sources \( u_{d1} \) and \( u_{d2} \) are referred to as the bias sources, while \( u_g \) is the signal source. In this thesis we call the SET transistor symmetrical biased when \( u_{d1} = -u_{d2} \), and asymmetrical biased when \( u_{d1} = u_{ds} \) and \( u_{d2} = 0 \).

Because the SET transistor is biased in region B one junction is placed in blockade and the voltage across the other junction is larger than the critical voltage. In figure 9.36 the times are shown for the two tunnel moments. \( \tau_{\text{on1}} \) is the time between the moment the tunnel condition is met for junction TJ \(_1\) and the moment the electron really tunnels through junction TJ \(_1\). Immediately after the electron has tunneled through junction TJ \(_1\), the tunnel condition of junction TJ \(_2\) is met, and an electron
will tunnel through junction TJ2 after the wait time \( \tau_{w2} \) (see figure 9.36). We assume that the tunnel time, needed for the electron to go from one side of the barrier to the other side, can be neglected compared to the wait time \( \tau_w \gg \tau_t \).

Figure 9.36: The tunnel events, in which an electron tunnels through both junctions of a SET transistor.

One electron \( e \) is transferred through the whole circuit after a time \( \tau_{w1} + \tau_{w2} \). Let \( \overline{\tau}_{wt} \) be the total average time of \( n \) electrons, needed to transport an electron from source to drain, which is equal to

\[
\overline{\tau}_{wt} = \frac{\sum_{i=1}^{n} (\tau_{w1,i} + \tau_{w2,i})}{n} \tag{9.83}
\]

Because the tunnel times are independent of each other we can rewrite this into

\[
\overline{\tau}_{wt} = \frac{1}{n} \sum_{i=1}^{n} \tau_{w1,i} + \frac{1}{n} \sum_{i=1}^{n} \tau_{w2,i} \tag{9.84}
\]

\[
\overline{\tau}_{wt} = \overline{\tau}_{w1} + \overline{\tau}_{w2} \tag{9.85}
\]

Filling this in equation 9.82 gives

\[
i_{ds} = \frac{e}{\Delta t} = \frac{e}{\overline{\tau}_{wt}} \tag{9.86}
\]

\[
i_{ds} = \frac{e}{\overline{\tau}_{w1} + \overline{\tau}_{w2}} \tag{9.87}
\]

The expression found in section 3.1.5 for the wait time of junction \( x \) was (see equation 3.23) when we neglect the tunnel time

\[
\overline{\tau}_{wx} = \frac{eR_{T_x}}{u_{jx} - u_{cr}^{x}} \quad \text{for} \quad u_{jx} > u_{cr}^{x} \tag{9.88}
\]

If we extract data from a SIMON simulation for a symmetrically biased SET transistor, and using the region B of figure 9.33 we indeed find the relation of equation 9.88, see figure 9.37. In figure 9.37 a comparison is made between the total wait time
Figure 9.37: The straight line is the total wait time derived from a simulation of a C-SET transistor (see figure 9.35) with $C_{j1} = 1.3 F$, $R_{T1} = 100 k\Omega$, $C_{j2} + C_{g} = 5 aF$, $R_{T2} = 700 k\Omega$, $u_{d1} = u_{ds}$, $u_{d2} = 0$, $u_{g} = 0 V$, and $q_i = 0.5 eC$. Let $i_{ds}$ be the current through the voltage source $u_{d1}$. To calculated the total wait time equation 9.86 is used. The $o$ points are the summed wait times of both junctions, using equation 9.88. For the junction voltages we used $u_{j1} = u_{ds} \frac{C_{j2}}{C_{j1}+C_{j2}} - \frac{q_i}{C_{j1}+C_{j2}}$ and $u_{j2} = u_{ds} \frac{C_{j1}}{C_{j1}+C_{j2}} + \frac{q_i}{C_{j1}+C_{j2}}$.

obtained from a simulation with SIMON using equation 9.86, and the sum of both individual wait times calculated for each junction separately using equation 9.88. Both simulations yield the same result.

Filling in the formula for the wait time (equation 9.88 in equation 9.87) gives us an average current of

$$i_{ds} = \frac{1}{\frac{R_{T1}}{u_{j1}-u_{1}} + \frac{R_{T2}}{u_{j2}-u_{2}}}$$

(9.89)

Let $C_{j1}$ be the capacitance of junction TJ1, let $C_{j2}$ be the capacitance of junction TJ2. The critical voltage is for both junctions equal, and

$$u_{j1}^{cr} = u_{j2}^{cr} = \frac{e}{2C_{\Sigma}} \quad \text{with} \quad C_{\Sigma} = C_{j1} + C_{j2} + C_{g}$$

(9.90)

$$i_{ds} = \frac{\left(u_{j1} - \frac{e}{2C_{\Sigma}}\right)\left(u_{j2} - \frac{e}{2C_{\Sigma}}\right)}{R_{T1}\left(u_{j2} - \frac{e}{2C_{\Sigma}}\right) + R_{T2}\left(u_{j1} - \frac{e}{2C_{\Sigma}}\right)}$$

(9.91)

A note should be made about equation 9.91: it is only valid in region B of figure 9.33, hence exactly one of the two junctions is placed in the Coulomb blockade. For a positive $u_{d1}$, a negative $u_{d2} = -u_{d1}$, and a positive $u_{g}$ in case of the SET transistor of
figure 9.35 an electron will first tunnel through TJ₂. If we assume \( u_d = u_d1 = -u_d2 \), and \( ne \) the charge on the island (assuming zero initial charge and zero background charge), then we can write for the voltage across junction TJ₂

\[
    u_{j2} = u_d \frac{2C_{j2} + C_g}{C_\Sigma} + u_g \frac{C_g}{C_\Sigma} + \frac{ne}{C_\Sigma} \quad (9.92)
\]

After the tunnel event through junction TJ₂ an extra electron is on the island, hence \( n \rightarrow n - 1 \). So for the voltage across tunnel junction TJ₁ we can write

\[
    u_{j1} = u_d \frac{2C_{j1} + C_g}{C_\Sigma} - u_g \frac{C_g}{C_\Sigma} - \frac{(n - 1)e}{C_\Sigma} \quad (9.93)
\]

The result from this is a periodic current-gate voltage plot (see figure 9.38). In this figure the computed results (equation 9.91) shown in figure 9.38a, are compared to the simulation result obtained by SIMON. The simulation result obtained by SIMON (figure 9.38b) shows some 'noise' which is due to the used Monte Carlo analysis.

![Figure 9.38](image.png)

Figure 9.38: The periodic gate voltage current characteristic of a symmetrical biased C-SET transistor (figure 9.35), with \( C_{j1} = 1aF, C_{j2} = 5aF, C_g = 3aF, R_T1 = 100k\Omega, R_T2 = 900k\Omega, u_d1 = -u_d2 = 6mV \). a) The calculated current \( i_{ds} \) as function of the gate voltage \( u_g \) using equation 9.91 with the junction voltages given in equation 9.92 and equation 9.93. b) The simulation results of SIMON.
Peak value

One of the characteristics is the peak value of the drain current as function of the gate-source voltage. Let

\[ q_1 = u_d \left( 2C_{j1} + C_g \right) - \left( n - 1 \right) e - \frac{e}{2} \]  
\[ q_2 = u_d \left( 2C_{j2} + C_g \right) + n e - \frac{e}{2} \]  

(9.94)  
(9.95)

Then we can rewrite equation 9.91 into

\[ i_{ds} = \frac{(q_1 - u_g C_g) (q_2 + u_g C_g)}{C_{\Sigma} \left[ R_{T1} (q_2 + u_g C_g) + R_{T2} (q_1 - u_g C_g) \right]} \]  

(9.96)

For the special case: \( R_{T1} = R_{T2} = R_T \) this current can be simplified into

\[ i_{ds} = \frac{(q_1 - u_g C_g) (q_2 + u_g C_g)}{C_{\Sigma} R_T (q_2 + q_1)} \]  

(9.97)

The maximum current can be found using

\[ \frac{\partial i_{ds}}{\partial u_g} = 0 \]  

(9.98)

with

\[ \frac{\partial i_{ds}}{\partial u_g} = \frac{1}{C_{\Sigma} R_T (q_2 + q_1)} \left[ -C_g (q_2 + u_g C_g) + C_g (q_1 - u_g C_g) \right] \]  

(9.99)

Which can be simplified using equation 9.98 into

\[ 2u_g C_g = q_1 - q_2 \]  

(9.100)

For \( q_1 - q_2 \) can be written

\[ q_1 - q_2 = 2u_d \left( C_{j1} - C_{j2} \right) - (2n - 1)e \]  

(9.101)

So the maximum current can be found for a gate voltage \( u_g \) of

\[ u_g = \frac{u_d \left( C_{j1} - C_{j2} \right) - n e + \frac{e}{2}}{C_g} \]  

(9.102)

Let \( \hat{i}_{ds} \) be the maximum current which can be found by combining equation 9.97 with equation 9.100

\[ \hat{i}_{ds} = \frac{(q_1 - \frac{q_1 - q_2}{2}) (q_2 + \frac{q_1 - q_2}{2})}{C_{\Sigma} R_T (q_2 + q_1)} \]  

(9.103)

\[ \hat{i}_{ds} = \frac{q_1 + q_2}{4C_{\Sigma} R_T} \]  

(9.104)

For \( q_1 + q_2 \) we can write

\[ q_1 + q_2 = 2u_d C_{\Sigma} \]  

(9.105)
Which results in a maximal current of

\[ \hat{\dot{i}}_{ds} = \frac{u_d}{2R_T} \]  \hspace{1cm} (9.106)

for the case of \( R_T = R_{T1} = R_{T2} \), \( u_d = u_{d1} = -u_{d2} \) and region \( B \) as defined on page 182. Two remarks should be made about this equation:

1. The peak value of the current is independent on the capacitances used, as long as it is in region \( B \) (see figure 9.39). Only the gate voltage where the peak value of the current appears depends on these capacitances, see equation 9.102.

2. From equation 9.106 it is clear that the maximal current is half of the voltage between the drain-source of the transistor (\( u_{ds} \)) divided by the sum of the tunnel resistances.

\[ \hat{\dot{i}}_{ds} = \frac{u_d}{2R_T} = \frac{u_{ds}}{4R_T} = \frac{u_{ds}}{2R_{\Sigma}} \]  \hspace{1cm} (9.107)

![Graphs showing current vs. gate voltage for different capacitance values](image)

Figure 9.39: Simulation results obtained by SIMON with \( u_{d1} = u_{ds} = 15mV \), \( u_{d2} = 0 \), \( R_{T1} = R_{T2} = 500k\Omega \), \( C_g = 3aF \), \( C_{j2} = 1aF \). The horizontal line is the graphical implementation of equation 9.106. Both simulations differ in the capacitance of TJ1: a) \( C_{j1} = 1aF \), and b) \( C_{j1} = 6aF \).

**High current behaviour**

For the high current regime, region \( C \) in figure 9.33, we need to apply a high exciting voltage \( u_{ds} \) so that for both junctions \( u_{jx} \gg u_{jx}^{cr} \). When the voltage across both junctions is much larger than the critical voltage \( u_{jx}^{cr} \) the wait time of each junction is almost independent of the number of electrons on the island. The voltage across a junction is determined only for a small part by the electrons on the island, while in
the case of region B of figure 9.33 a change of one electron on the island is enough
to put one junction in blockade and the voltage across the other junction above its
critical voltage. For a high current the number of electrons that tunnelled through
both junctions should be equal, because otherwise a large amount of charge on the
island will be built up. So we can now write

$$\tilde{t} = \frac{e}{\tau_{w1}} = \frac{e}{\tau_{w2}}$$  \hspace{1cm} (9.108)

Let $u^{cr}_j$ be the critical voltage of one junction. The critical voltage for both junctions
is equal in the case for a voltage excited SET transistor, so $u^{cr}_j = u^{cr}_{j1} = u^{cr}_{j2} = \frac{e}{2C_\Sigma}$. 
Combining equation 9.88 with equation 9.108 we can write

$$\tilde{t}R_{T1} = u_{j1} - u^{cr}_{j1}$$  \hspace{1cm} (9.109)

$$\tilde{t}R_{T2} = u_{j2} - u^{cr}_{j2}$$  \hspace{1cm} (9.110)

$$\tilde{t} (R_{T1} + R_{T2}) = (u_{j1} + u_{j2}) - (u^{cr}_{j1} + u^{cr}_{j2})$$  \hspace{1cm} (9.111)

Let $R_T$ be the sum of both tunnel resistors, $R_{\Sigma} = R_{T1} + R_{T2}$, and $i_{ds} = \tilde{t}$. Because
$u_{ds}(t) = 2u_d(t) = u_{j1}(t) + u_{j2}(t)$ the current in the high current regime is equal to

$$i_{ds} = \frac{u_{ds} - \frac{e}{C_\Sigma}}{R_{\Sigma}}$$  \hspace{1cm} (9.112)

This forms the asymptote to which all lines will go for high currents. Equation 9.112
can be rewritten to

$$u_{ds} = \frac{e}{C_\Sigma} + i_{ds}R_{\Sigma}$$  \hspace{1cm} (9.113)

In figure 9.40 equation 9.113 and the simulation results of SIMON are shown.

The slope of the graph in the high current regime is always the same; only the slope
in the low current regime varies due to the gate voltage. This is a different conclusion
from the one found in the literature (see for example [47] formula 4.7); which states
that $u_{ds} = u_{th}(u_d) + iR_{\Sigma}$, in which $u_{th}$ is the threshold voltage, the voltage where
a current through the device is possible. This gives only the same result as equation
9.113 when $u_{th} = 2u^{cr}_j$, while the slope is always the same.

In figure 9.41 we compared two different simulations. Both have the same value
of the sum of the tunnel resistors (as can be derived from the slopes of figure 9.41a
and figure 9.41c). When both resistors are exactly the same the peak value is indeed
equal to equation 9.106, when the resistors are unequal the peak value will be larger
(compare figure 9.41b with figure 9.41d). In this way a test can simply be developed
to see if the resistors are (almost) equal or if they differ considerably.

### 9.4 Two island structure

One of the circuits analysed and measured, which contain more than the two junctions
of a SET transistor, is the two island structure also known as the electron pump [99].
This circuit can be operated in a regime in which electrons can tunnel through the
whole device one by one. In this way it can be used as a counter for electrons, and
by doing so create a standard for currents [112, 124]. Because of the principle of
pumping [38, 100] (discussed in section 9.4.2), the smallest possible structure for a single-electron pump contains two gates and two islands. This two-island structure is drawn in figure 9.42.

9.4.1 Input-output relations

Let \( a \) be equal to the number of the junction under investigation. Let \( k_g \) be the number of gates, let \( k_{nf} \) be the number of islands, and let \( k_d \) be the number of bias sources \( u_d \). Let \( \alpha \) and \( \beta \) be constants depending on the topology of the rest of the circuit. For the voltage across junction \( a \) we can write in general, using superposition (see section 3.2.1)

\[
u_{j,a}(t) = \mathcal{L}^{-1} \left\{ \sum_{b=1}^{k_g} A_{b,a}^g(s)U_{g,b}(s) + \sum_{b=1}^{k_{nf}} B_{b,a}(s)Q_{i,b}(s) + \sum_{b=1}^{k_d} A_{b,a}^d(s)U_{d,b}(s) \right\}
\]

(9.114)

As can been seen from equation 9.114 we do not need to know the so called tunnel resistor. Which is only a model to describe the amount of current that will flow, averaging a number of electron tunnel events.

Using the method discussed in appendix D.1 to calculate node potentials, we can derive the voltages across the tunnel junctions as a function of the bias voltages, the independent island charges, and both the gate voltages. The results and the derivation are both given in appendix D. A number of slopes for the plot \( u_{g,2} = f(u_{g,1}, \text{equal to the number of junctions, are found in the derivation.} \)
Figure 9.41: Simulation results of an asymmetrical biased C-SET transistor, with $C_{j1} = 1aF$, $C_{j2} = 1aF$, $C_g = 1aF$. In the case of equal resistors ($R_{T1} = R_{T2} = 500k\Omega$) we obtained figure a) where $u_{gs} = 0V$ and b) with $u_{ds} = 30mV$. Or in case of unequal resistors ($R_{T1} = 100\Omega$ and $R_{T2} = 900k\Omega$) we obtained figure c) where $u_{gs} = 0V$ and d) with $u_{gs} = 30mV$. In the figures b) and d) also the straight horizontal line of equation 9.106 is shown, which indeed gives the peak value for the case of equal tunnel resistors.

Figure 9.42: The circuit of an ideal two-island structure

The interception points on the lines periodically crossing the axes in the plot of $u_{g,2} = f(u_{g,1})$ should be equal because of the unlimited periodicity of $\frac{a}{C_{g1}}$ and $\frac{a}{C_{g2}}$ in respectively the horizontal direction and the vertical direction. For figure 9.43 this means that $\Delta u_{h1} = \Delta u_{h2}$, $\Delta u_{h3} = \Delta u_{h4}$, $\Delta u_{v1} = \Delta u_{v2}$, and $\Delta u_{v3} = \Delta u_{v4}$. Due to this and the fact that three junctions will have three types of slopes, the plot can have only a few different shapes: from a triangular shape to a hexagonal shape as indicated in figure 9.44. By increasing the bias voltage the shape of the stability diagram is changed from a hexagonal shape into a triangle shape (see also figure 9.45). When the voltage is further enlarged no region of Coulomb blockade exists any more, so
no shape is formed within the stability diagram. In figure 9.46 six simulation results obtained with SIMON are shown.

![Diagram](image)

Figure 9.43: Two of the three different slopes of a three junction pump. The distance to the axes are equal for all the periodically repeating lines, which intercept with these axes.

(a) ![Diagram](image)  (b) ![Diagram](image)

Figure 9.44: Two possible shapes that can be created due to the conditions shown in figure 9.43 and the fact that three junctions will result in three slopes. a) triangles and b) hexagonals. Within the shown shapes are the stable regions in which a fixed number of electrons can be defined on the islands.

**Slopes visible in the graph of** \( u_{g,2} = f(u_{g,1}) \)**

When we are interested in deriving the slopes of equal current in the graph of the gate voltage 1 as a function of the gate voltage 2, it suffices to calculate the relation
Figure 9.45: When the bias voltage is enlarged the lines in the stability diagram move. When the bias voltage is low the lines form a hexagonal shape, while a larger bias voltage creates a triangular shape.

Figure 9.46: To show the principle of figure 9.45 six simulations done at different bias conditions are shown. For the simulation is used $C_{g1} = C_{g2} = 5aF$, and all the junction capacitances are equal to $C_j = 5aF$ ($R_T = 100k\Omega$), $u_{d,2} = 0$, and $u_{d,1} = u_{ds}$.

(see equation 9.114)

$$\mathcal{L}^{-1}\left\{A_{1,a}^g(s)U_{g,1}(s) + A_{2,a}^g(s)U_{g,2}(s)\right\} = 0$$  \hspace{1cm} (9.115)

for all the three junctions $a = (1, 2, 3)$. For the expressions of the $A^g$s, see appendix D. The relation between the two gate voltages can be written for the three junctions
\[
\frac{u_{g,1}}{u_{g,2}}_{a=1} = \mathcal{L}^{-1} \left\{ \frac{A_{2,1}^g(s)}{A_{1,1}^g(s)} \right\} = \frac{C_{g2}}{C_{g1}} \frac{C_{j2}}{C_{j2} + C_{j3} + C_{g2}}
\]
(9.116)

\[
\frac{u_{g,1}}{u_{g,2}}_{a=2} = \mathcal{L}^{-1} \left\{ \frac{A_{2,2}^g(s)}{A_{1,2}^g(s)} \right\} = \frac{C_{g2}}{C_{g1}} \frac{C_{j1} + C_{g1}}{C_{j3} + C_{g2}}
\]
(9.117)

\[
\frac{u_{g,1}}{u_{g,2}}_{a=3} = \mathcal{L}^{-1} \left\{ \frac{A_{2,3}^g(s)}{A_{1,3}^g(s)} \right\} = \frac{C_{g2}}{C_{g1}} \frac{C_{j1} + C_{j2} + C_{g1}}{C_{j2}}
\]
(9.118)

The triple points

**Definition 9.1** The triple point is defined as the interception point in which all three lines are attached for a zero bias condition \((u_{d1} = u_{d2} = 0)\).

This will always be the case for a hexagonal stability plot \((u_{d1} \approx 0\) and \(u_{d2} \approx 0\)). In case of a larger bias condition \((u_{d1} > 0\) and \(u_{d2} < 0\)) the triple point is enlarged into a triple area. This is shown in figure 9.47 in which the original triple point is increased into a triple area. Below we will discuss how to derive the triple point and the borders of a triple area.

![Stability diagram](image)

Figure 9.47: The stability diagram of a simulation of the electron pump done with SIMON, with equal junction capacitance \(C_{j1} = C_{j2} = C_{j3} = 1aF\) and tunnel resistors \(R_{T1} = R_{T2} = R_{T3}\), \(C_{g1} = C_{g2} = 1aF\). When we apply a small bias voltage \(u_{d1} = -u_{d2} = 1\mu V\) we obtain one point in which the lines are attached. When these bias voltages are increased this region is increased. For \(u_{d1} = -u_{d2} = 7.5mV\) the simulation result is also shown, now the triple point is a triangular shaped area.

When two of the triple points are known (the easiest triple points to calculate are those around the origin), all the other triple points can be determined with the
help of the fact that the triple points are periodic in two directions. In the horizontal direction the periodicity is determined by $\frac{e}{C_{g1}}$ and in the vertical direction by $\frac{e}{C_{g2}}$ (as shown in figure 9.48).

![Diagram of a circuit with labeled points and voltage measurements](image)

Figure 9.48: With the help of just two known triple points $a$ and $b$ all the other triple points can be determined, and hence the hexagonal shape can be formed.

The first triple point ($a$ in figure 9.48) is the interception point of all three lines, for which there is no independent charge on either island, hence this triple point can be determined using two out of the three equations

$$\mathcal{L}^{-1}\left\{A_{1,1}(s)U_{g,1}(s) + A_{2,1}(s)U_{g,2}(s)\right\} = -u_{j1}^{cr} \quad (9.119)$$

$$\mathcal{L}^{-1}\left\{A_{1,2}(s)U_{g,1}(s) + A_{2,2}(s)U_{g,2}(s)\right\} = u_{j2}^{cr} + \frac{e}{C_{g2}} \quad (9.120)$$

$$\mathcal{L}^{-1}\left\{A_{1,3}(s)U_{g,1}(s) + A_{2,3}(s)U_{g,2}(s)\right\} = u_{j3}^{cr} \quad (9.121)$$

With the help of two out of these three equations we can determine $u_{g1}$ and $u_{g2}$ of the triple point.

For the next triple point ($b$ in figure 9.48), the only thing that is changed is the island charge. Line 1 (equation 9.119) shifts due to an extra electron on island 2 (which can be concluded from figure 9.51), so the new equation becomes

$$\mathcal{L}^{-1}\left\{A_{1,1}(s)U_{g,1}(s) + A_{2,1}(s)U_{g,2}(s) - eB_{2,1}(s)\right\} = -u_{j1}^{cr} \quad (9.122)$$

The equation for the second line (equation 9.120) stays the same. And line 3 (equation 9.121) changes due to an extra electron on island 1, so the new equation becomes

$$\mathcal{L}^{-1}\left\{A_{1,3}(s)U_{g,1}(s) + A_{2,3}(s)U_{g,2}(s) - eB_{1,3}\right\} = u_{j3}^{cr} \quad (9.123)$$

With the help of two of the three equations (equation 9.120, equation 9.122, and equation 9.123) the second triple point can be determined.
The six lines described above (equations 9.119 - 9.123) are shown in figure 9.49a. In figure 9.49b a simulation (done with SIMON) of that specific region is shown also. As was expected from the derivation: the two pictures show the same triple points.

Figure 9.49: a) The six lines described by the equations 9.119 - 9.123, with $C_{j1} = 5aF$, $C_{j2} = 7aF$, $C_{j3} = 11aF$, $C_{g1} = 1aF$, and $C_{g2} = 3aF$. b) The simulation result (obtained by SIMON) using the same component values as for figure a), with extra $u_{d,1} = 1nV$ and $u_{d,2} = 0$.

Calculating the borders of the triple areas

Due to non-zero bias voltages $u_{d,1}$ and $u_{d,2}$ the borders of the Coulomb blockade (the stable regions, which are needed for a correct functioning of the electron pump) changes. The region of the triple point becomes larger (see figure 9.47) to form so called triple areas. To determine the shifts of the borders of these stable region we can again use equation 9.114.

Let $\Delta u_{j,a}$ be the change in junction voltage of junction $a$ due to both bias sources, so

\[
\Delta U_{j,1}(s) = A_{1,1}^{d}(s)u_{d,1}(s) + A_{2,1}^{d}(s)u_{d,2}(s) \tag{9.124}
\]

\[
\Delta U_{j,2}(s) = A_{1,2}^{d}(s)u_{d,1}(s) + A_{2,2}^{d}(s)u_{d,2}(s) \tag{9.125}
\]

\[
\Delta U_{j,3}(s) = A_{1,3}^{d}(s)u_{d,1}(s) + A_{2,3}^{d}(s)u_{d,2}(s) \tag{9.126}
\]

To determine the shifts in the horizontal direction and in the vertical direction appearing in the plot where $u_{g,2}$ is shown as a function of $u_{g,1}$ (see figure 9.50), this change in junction voltage should be expressed in the gate voltage. Let $\Delta u_{g_{x,a}}$ be the change of the Coulomb blockade expressed in gate voltage $u_{g,a}$ of junction $a$. Then we can write for the shifts, for line 1

\[
\Delta U_{g1,1}(s) = \frac{\Delta U_{j,1}(s)}{A_{1,1}^{g}(s)} \tag{9.127}
\]

\[
\Delta U_{g2,1}(s) = \frac{\Delta U_{j,1}(s)}{A_{2,1}^{g}(s)} \tag{9.128}
\]

For the other equations see appendix D.3.
Figure 9.50: The amount of change in gate voltages due to applied bias sources. The interception point called triple point is enlarged into a triangular shaped region, called triple area. The numbers 1, 2, and 3 indicate the slopes due to respectively junctions 1, 2, and 3.

9.4.2 Principle of the electron pump

The stability figure (when no bias $u_d$ is applied) shows hexagonal shapes. Inside such a shape the number of electrons is fixed, this is shown in figure 9.51. And in figure 9.52 the Pumping principle is shown. In this example we start in stable region (1,1), which means on both islands one electron has arrived. To place an extra electron on the second island (indicated with (1,2) in figure 9.52a), which is transition a in figure 9.52c, the gate source $u_{g1}$ should remain constant, while gate source $u_{g2}$ should increase. To pump this extra electron through the proposed SET structure, the next stable region should be (2,1), hence the electron has tunneled through junction TJ$_2$ (transition b in figure 9.52c). To go to this region the gate source $u_{g2}$ should decrease while the gate source $u_{g1}$ should increase. To make the pump cycle complete this extra electron should also leave island 1 (transition c in figure 9.52c), such that the circuit is back into stable region (1,1). This last transition can be obtained by decreasing gate voltage $u_{g1}$ while gate voltage $u_{g2}$ is unaltered.

In figure 9.52b both shapes for the necessary gate voltages are shown. To let a constant current flow through the structure the two gate voltages should be periodic voltages with a phase difference of $\frac{\pi}{2}$. The direction of the electron transfer is only determined by which gate voltage changes first [99] and not by the bias voltages. The pumping principle only works as described above when the junctions can be placed in Coulomb blockade.

To be able to pump there should be a stable region, hence at least a triangle shape should exist. The smaller the triple area is, the easier it is to get a correct pumping.

9.4.3 Simulations

SIMON is used to verify the in this section derived equations. The simulation results for the relation $u_{g,1} = f(u_{g,2})$ are shown in figure 9.53. The three different slopes of
which the hexagonal figures are formed can be calculated using the slope equations 9.116, 9.117, and 9.118.

From the periodicity in vertical and horizontal direction we can easily determine the gate capacitances. And together with those results and the slopes determined using equations 9.116 - 9.118 we can determine all three the junction capacitances. By doing so we will find the same answers as the values put in the simulator (shown below figure 9.53), which shows the correctness of the expressions found.

### 9.4.4 Practical situations

In a practical situation we will find that $C_{j1} \approx C_{j2} \approx C_{j3}$ and $C_{g1} \approx C_{g2}$, and the junction capacitances will be larger than the gate capacitances. This results in a simplification of the slopes to

\[
\begin{align*}
\frac{u_{g,1}}{u_{g,2}} \bigg|_{a=1} & = -0.5 & (9.129) \\
\frac{u_{g,1}}{u_{g,2}} \bigg|_{a=2} & = +1 & (9.130) \\
\frac{u_{g,1}}{u_{g,2}} \bigg|_{a=3} & = -2 & (9.131)
\end{align*}
\]

In section 10.3 we will discuss some of the measurement results of the two island electron pump.
Figure 9.52: a) The hexagonal figures with indication of the number of electrons on the islands. When we circle around a triple point an electron is pumped through the structure. b) The necessary signals on both gates to control one electron through the pump. c) The pump structure with indicated the direction the electron charge is transferred.
Figure 9.53: The simulation by SIMON of a 2 island structure, with: $C_{j1} = 7aF, C_{j2} = 11aF, C_{j3} = 13aF, C_{g1} = 3aF, C_{g2} = 5aF, u_{d,1} = 1nV, u_{d,2} = 0V$, and $R_T = 100k\Omega$. 
"In theory practise and theory are the same, but in practise they are different."

Larry McVoy

"The demonstration that parameters can be chosen to fit experimental characteristics does not suffice to validate the application of the model to describe the experiment."

C.B. Duke [34]

Measurement results

To check whether the predictions of our theory are valid we performed some measurements. The main goal of doing the measurements on two of the SET structures analysed in chapter 9 is to see if the predicted behaviour is indeed visible. The SET structures measured are the C-SET transistor and the (two island) electron pump.

With the help of the equations derived for the slopes of the input-output voltage relation for the C-SET transistor obtained in section 9.3, the component values can be derived.

To validate the theory for including resistors in a SET circuit measurements were carried out. All the SET measurements discussed in this chapter are done on samples placed inside a cryostat. A disadvantage of measurements on samples placed within a cryostat is the fact that resistors placed outside the cryostat have no influence on the measurement results due to the large capacitive environment (as a consequence of filters and wires within the cryostat, a similar discussion was held in section 9.3.4). There can be no discussion about a correct model to include resistors as long as the resistors are not placed on the sample.

Another sample, the electron pump, is also measured. This sample has an extra feature: in series with the bias connections, two resistors are placed, which still have their resistance at low temperatures (due to the material chosen). The outcome of these measurements will give information about a correct model to include resistors.

Also the slopes in the relation between both gate voltages of the electron pump, which were derived in section 9.4 can be verified. With the help of these equations it should be possible to extract the component values for the electron pump.

The measurements, which are described in this chapter, are done at NMI van Swinden Laboratorium B.V. together with Paul Teunissen and Helko van den Brom of the department of Electricity and Magnetism. All the measured devices are fabricated by Sergey Lotkov from PTB (Physikalisch-Technische Bundesanstalt).

This chapter starts with a description of the measurement setup for both experiments. The experimental results and the extracted component values of the C-SET transistor are discussed in the second section. And in the third section the measure-
ments which are done on the three-junction electron pump are discussed. We end this chapter with some conclusions.

10.1 Measurement setup

The overview of the measurement system that was used is drawn in figure 10.1.

To measure signals due to single-electron tunneling we should prevent the thermal fluctuations destroying the signal. For this reason we need to cool the device well below 1K by using a cryostat. The temperature needed to let the device work in the single-electron tunneling regime is discussed in section 10.1.1. Other possible disturbing effects are light and vibration; they can give extra energy to the electron. These effects will be discussed in section 10.1.2.

For processing of the obtained measurement results we used a computer. To collect the measured signals analog to digital (A/D) converters are used. And to apply the gate voltage and drain-source voltage or current by the computer, digital to analog (D/A) converters are used.

Because the A/D and D/A converters used have voltage input and voltage output, respectively, there is a need for converters when currents are used. The signals coming from the sample are very small and should be amplified. Bias signals should be applied to the sample at the same connectors as where the measurements are done. For this reason it is best to combine the amplifier (and the conversion) with the bias source. The conversion, amplification, and bias method are discussed in section 10.1.3.

![Figure 10.1: A schematic overview of the measurement system.](image-url)

The sample consists of a very small (nm regime) insulator between the two junction plates. This makes the sample very sensitive for high voltages, static electricity, radiation, etc. Typically an aluminium oxide insulator with a thickness of a few nano-
meters is used. Aluminium oxide has a dielectric strength of $13.4\,kV/mm$, which is
equal to $13.4\,mV/nm$. Care should be taken to make sure the measurement setup
would not destroy the junctions.

The maximum output voltage of the $D/A$ converter is in the order of a few volts,
while we can not use more than only a few $mV$ across a junction. The $D/A$ converter
can be used in the low-voltage regime of a few $mV$, but then the accuracy is a few
bits only. For this reason an attenuator is used. In figure 10.1 the attenuator is
drawn. A voltage divider of 100 times was used for the experiment with the C-SET
transistor. This attenuator was placed in a room temperature environment. In the
experiment with the electron pump a special attenuator near the sample (so at very
low temperatures) was used. This setup has a problem: When currents flow through
this resistive attenuator, it will heat up and will also heat its surrounding (which is the
sample in this case). The effect the attenuators used have on the measurements are
ideally taken into account, in other words the outcome of the measurements discussed
in this chapter are scaled by a factor determined by the ideal attenuator.

One of the problems when using $A/D$ and $D/A$ converters, are the high frequency
(HF) signals which are generated within the $A/D$ and $D/A$ converters, necessary for
sampling. These HF signals give a direct rise of the sample temperature. To reduce
the influence of the HF signals, filters are placed in the measuring system, see also
the thesis of Bosch [13]. The filters used are discussed in section 10.1.4.

10.1.1 Cooling

Because cooling costs time and money, we should make sure that the sample is tested
before it is cooled down. The SET transistor can be tested by measuring its resistivity
at room temperature, this should be high ohmic ($k\Omega$ - $M\Omega$). If this is indeed the case
the cryostat can be closed.

If the measured resistance is too high (the insulator is to thick to let tunneling
occur) the SET transistor will not work, we just see a capacitor. If it is too low,
mostly zero ohm, the SET transistor is defect (the insulator is reduced to a thickness
of zero), and has become a wire due to a shortcut.

After the cryostat is closed the cooling to helium temperature (4.2K) starts. After
which we cool further using a Helium pump structure [72]. Temperatures below 20
mK are reachable. The complete cooling will take many hours. Because the sample
is placed in an almost vacuum box it takes a while to cool down; cooling can only
take place through the wires connected to the sample.

Influence of the temperature

For two reasons temperature is important:

1. When the temperature increases, electrons get a higher energy. This means the
electron can tunnel before the critical voltage is reached. To be able to neglect
the thermal energy $k_BT$ the energy needed to let the electron tunnel (found in

---

1The device should only be measured with very low voltages (a few milli volts), because of the
low dielectrical strength.
section 3.1.2) should be much higher than the thermal energy

\[ \frac{C_j}{2} (u_{ja}^2 - u_{jb}^2) \gg k_B T \]  
(10.1)

2. To be able to distinguish the change in voltage \( \Delta u_j \) due to the tunneling of an electron, the amplitude of the signal due to this tunneling should be higher than the thermal fluctuations. The condition for the critical voltage \( u_j^{cr} \) derived in section 4.1 was

\[ u_j^{cr} = \frac{\Delta u_j}{2} \]  
(10.2)

For the voltage excited C-SET transistor the critical voltage for both junctions is equal. Let \( C_{\Sigma} \) be the sum of both junction capacitances \( (C_{j1}, C_{j2}) \) and the gate capacitance \( (C_g) \), so \( C_{\Sigma} = C_{j1} + C_{j2} + C_g \) then we can write for the critical voltage of both junctions

\[ u_j^{cr} = \frac{e}{2C_{\Sigma}} \]  
(10.3)

Because we can only express the thermal influence in energy, we get for the C-SET transistor

\[ k_B T < e\Delta u_j = \frac{e^2}{C_{\Sigma}} \]  
(10.4)

Using the equations described above and substituting the expected junction capacitance values of 500\( aF \), gives us an operating temperature for this sample of less than \( T = 0.75K \).

Overcoming the problem of superconduction

When we measure below 1K we have to make sure the chip is not working in the superconducting mode. Let \( T_c \) be the critical temperature (the critical temperature for aluminium is \( T_c = 1.175 \pm 0.002K \)) below which an electrical conductor undergoes a transition from the normal state to the superconducting state. Let \( H_c \) be the critical value of the magnetic field. The relation between the temperature and the magnetic field which gives the separation between the normal phase and the superconducting phase can be approximated by [120]

\[ H_c = H_c(0) \left[ 1 - \left( \frac{T}{T_c} \right)^2 \right] \]  
(10.5)

\( H_c(0) \) is a constant and is for aluminium \( H_c(0) = 1.24A/m \). The critical magnetic field is drawn as function of the temperature according to the equation above in figure 10.2.

Because we are not interested in the junction in superconducting mode (Josephson junction) we add a magnetic field by mounting a magnet near the chip, see figure 10.3. Due to the fact that it is a constant magnetic field it will not influence the measured currents and voltages.
Figure 10.2: The relation between the magnetic field and the temperature.

Figure 10.3: A magnet placed on a chip to overcome the problem of superconductivity.

10.1.2 Influence of external light sources or external fields

The cryostat should be closed to make sure that there is no light shining on the sample (photon energy) and to be able to cool down. During cool down we want no direct
contact with the air in the room the setup is placed in. So we need to place the inner side of the cryostat in a vacuum chamber.

Fukushima et al. [39] also comment about this:

Photon energy in GHz range corresponds to thermal energy of the order of 1K. Therefore, radiation noise over GHz range should be reduced seriously to operate the single-electron device. A microwave filter using copper powder was developed as an effective passive noise filter at low temperatures [93].

The bandwidth of the copper powder filters used in the measurements is described by Teunissen et al. [112] and is around 10 GHz. The copper powder filter is also described by Fukushima et al. [41].

Because of the very small signals, the wire from sample to amplifier (which should be kept as short as possible) is very sensitive for radiation and movement. To minimize the influence of the vibrations the amplifier is placed on a foam-rubber pillow.

To make the influence of vibrations (phonon energy) on the sample as small as possible the cryostat is lifted from the ground, and is connected to the ceiling with ropes.

Due to the very small signals, earth and ground connections of the machines used and of the measurement equipment need special attention: so that no loops are formed.

### 10.1.3 Amplifiers and sources

The signals coming from the sample are very small currents or voltages, so amplification is necessary.

Earlier work in our group was directed towards developing an amplifier which can operate at low temperatures [121]. The problem in that design was the noise. Also Lee [86] and Starmark [108] designed low temperature amplifiers.

To overcome the problem of the use of a very high Power Supply Rejection Ratio (in other words to get enough suppression of the 50 Hz of the general power supply and other frequencies appearing on the power lines of the amplifier) we use a battery supply for the amplifiers and supply source.

The $A/D$ converter used gives us the limitation of using an output voltage. So when we measure a current, amplification alone is not enough, we should also convert this current to a voltage.

To describe the basic amplification and converting principle we use an amplifier model, called nullor (schematically it is a square with two plus and two minus signs, see figure 10.4a). This is an ideal amplifier with:

- A gain of infinity ($A \to \infty$).
- Voltage between the plus input and the minus input is always zero.
- The input impedance is infinity, so the input current will be zero.
- A noise of zero.
Noise

Because we want to measure very small signals the amplification of the amplifier is a less important characteristic than the noise.

We can define a few different types of noise, the most important in this amplifier design are [3]:

- **Thermal noise or Johnson noise**
  
  This kind of noise is induced by resistors and is due to the thermal velocity of electrons. Let \( f \) be the single sided frequency \((0 < f < \infty)\), and \( k_B \) the Boltzmann constant \((k_B = 1.38 \cdot 10^{-23} \text{ J/K})\) and \( T \) the temperature. Nyquist theoretically derived that a resistor \( R \) has a noise voltage \( u_{nt} \) of
  
  \[
  u_{nt}^2 = 4k_BTR\Delta f
  \]  
  (10.6)

- **Shot noise**

  The discrete nature of the charge carriers in diodes and transistors gives current through these devices a noisy character called shot noise. Let \( I \) be the applied current through the device and \( e \) the elementary charge of one electron \((e = 1.6 \cdot 10^{-19}\text{C})\), then the shot noise current \( i_{ns} \) can be written as
  
  \[
  i_{ns}^2 = 2eI\Delta f
  \]  
  (10.7)

- **1/\( f \) noise**

  Some components, like the field effect transistor and carbon resistors, show a noise component that depends on the frequency. Let \( f_i \) be the so called noise corner frequency of a device [96], then the noise can be modelled by
  
  \[
  i_{nf}^2 = 2eI\Delta f \frac{f_i}{f}
  \]  
  (10.8)

A more detailed description of noise in general is beyond the scope of this thesis but can be found in many books, see for example Bonani et al.[12].

It should be noticed that all the mentioned noise contributions contain a factor of \( \Delta f \). This is in general the complete frequency band, but when frequencies, due to limitations of the amplifier, can be neglected, those frequencies also have no contribution to the noise. So by making the bandwidth of the amplifier smaller we can reduce the influences of the noise.

**Measuring current**

Because we want to measure a current and change it into a voltage for the \( A/D \) converter used, we can use a basic circuit, as shown in figure 10.4a, which is a direct conversion from current to voltage with an amplification of \(-R_f\).

Because we assumed that the nullors have no noise, all the noise is a consequence of the resistors used. We can write the noise current source at the input of the amplifier of figure 10.4a as

\[
 i_{ni}^2 = \frac{4k_BT\Delta f}{R_f}
\]  
(10.9)
To reduce this noise as much as possible and to increase the amplification as much as possible, the resistor that is used should be as large as possible. The most important limitation is the availability of large resistors, resistors much larger than $R_f = 1 \Omega$ can not easily be obtained. Another problem with large resistors is the influence of its surrounding, which destroys the accuracy of the resistive value.

When we also want to include the bias voltage in the circuit of the amplifier, and a symmetrical input we can use a circuit as shown in figure 10.4b.

![Diagram](image)

Figure 10.4: a) A basic current to voltage converter with amplification $-R_f$. b) The voltage supply used with an implemented current to voltage amplifier. To minimize the noise influence of the operational amplifiers (OpAmps) used, low noise OpAmps (type BB OPA128) have been chosen.

The bias voltage across the sample $u_{s\alpha}$ is equal to

$$u_{s\alpha} = u_{bias} \frac{R_{b2}}{R_{b1} + R_{b2}}$$

(10.10)

The total output voltage

$$u_{out} = -u_{s\alpha} - R_f i_{in}$$

(10.11)

This means that the gain will be equal to

$$\frac{u_{out}}{i_{in}} = 20 \log(R_f)$$

(10.12)

The most important noise contribution of this circuit at bandwidths below $B_w = 1 MHz$ are the resistors $R_f/2$ (see figure 10.5). To be able to measure current signals with a value of $1 pA$ the bandwidth of the amplifier should be limited to $100 kHz$.

Measuring voltage

When we measure a voltage no conversion is needed to get an output voltage needed for the A/D converter, the basic circuit is shown in figure 10.6a. The amplification
Figure 10.5: a) The current noise at the input of the amplifier of figure 10.4b simulated in SPICE and the b) current noise of the resistors $R_f = 1G\Omega$.

of this amplifier is equal to

$$u_{out} = u_{in} \frac{R_{f1} + R_{f2}}{R_{f2}}$$  \hspace{1cm} (10.13)

Because the maximum output voltage is around $u_{out} = 10V$ (allowed due to the A/D converter used) and the expected input voltage is $u_{in} = 10mV$ we need a maximal amplification of 1000 times.

The noise voltage calculated back to the input, due to the resistors, is equal to

$$u_{ni}^2 = 4k_BT\Delta f \frac{R_{f1}R_{f2}}{R_{f1} + R_{f2}}$$  \hspace{1cm} (10.14)

Concluding we can say that we can make the noise of the voltage to voltage amplifier as small as possible by making the resistors as small as possible. This is in contradiction with the amplification demand (see equation 10.13).

To measure a drain-source voltage we should bias the sample with a drain-source current. For a current supply, needed for this kind of bias scheme, made with a high resistor $R_b$ and a voltage source $u_{bias}$ (see figure 10.6b) we have two demands:

1. The voltage across the sample $u_{in}$ should be much lower than the voltage source $u_b$ used. Because the current $i_{bias}$ is equal to

$$i_{bias} = \frac{u_{bias} - u_{in}}{2R_b}$$  \hspace{1cm} (10.15)

The current can be assumed to be independent of the voltage across the sample (just like an ideal current source), when $u_{bias} >> u_{in}$, in which case the current
is equal to

\[ i_{bias} = \frac{u_{bias}}{2R_b} \quad (10.16) \]

2. The resistance of the current source \( R_b \) should also be much larger than the resistance of the sample, \( R_{sa} \). This is linked to the previous point.

\[ u_{in} = \frac{R_{sa}}{2R_b + R_{sa}} u_{bias} \quad (10.17) \]

When \( 2R_b \gg R_{sa} \) the voltage across the sample \( u_{in} \) due to the voltage source \( u_{bias} \) can be neglected, which is needed to make the current bias source independent of the signal variations.

The first point is of importance when the sample is in Coulomb blockade because the junctions act like a capacitor then. The second point is of importance when the junctions are outside the Coulomb blockade, they then conduct, and have a resistance value of \( R_T \). For a two junction SET transistor we can write (when a large current is flowing through the sample) \( R_{sa} = 2R_T \).

![Figure 10.6](image_url)

Figure 10.6: a) The basic circuit of a voltage to voltage amplifier. b) The implementation: a current supply and the voltage amplifier, the OpAmps used are the OPA 2111.

The circuit of figure 10.6b is used to measured the voltage across the sample \( u_{in} \) and amplify this to a voltage which can be used for the A/D converter \( u_{out} \). For this circuit we can write for the output voltage

\[ u_{out} = \left( u_{in} + \frac{R_{sa}}{R_{sa} + 2R_b} \right) \frac{R_f1 + R_f2}{R_f2} \quad (10.18) \]

The noise of this amplifier is simulated (see figure 10.7). An important noise contribution of the circuit of figure 10.6b is the resistor \( R_{f2} \). The noise contribution
of the resistor $R_{f1}$ can be neglected compared to the noise contribution of resistor $R_{f2}$, because $R_{f1}$ will be much larger than $R_{f2}$. This is caused by the fact that we need a certain gain in practical situations. To obtain a amplification of 1000 (60dB) a chosen $R_{f1}/2 = 81.9k\Omega$ means that $R_{f2} = 163.8\Omega$. The noise contribution of resistor $R_{f2}$ is equal to

$$u_{ni} = \sqrt{4k_BTBR_{f2}}$$  \hspace{1cm} (10.19)

Figure 10.7: a) The SPICE simulations of the voltage noise of the amplifier of figure 10.6b and b) the voltage noise of the resistor $R_{f2} = 164\Omega$ (using equation 10.19).

To measure small voltage signals, low noise can be obtained when the bandwidth of the amplifier used is limited. From the simulations shown in figure 10.7 the conclusion can be drawn that if we limit our bandwidth to around 15Hz a signal to noise ratio of 0dB can be obtain for voltages of 20nV.

### 10.1.4 Filters in the measurement system

As shown in section 10.1.3 the biggest noise contribution is due to the resistors used. The amount of noise from those resistors depends on the bandwidth of the amplifier. To reduce the noise we can reduce the signals bandwidth. Making a bandwidth smaller can easily be done by using a filter. In the measurements described in this chapter we choose an RC filter with a frequency around 15 Hz.

The bias signals send to the sample, can contain high frequency components due to the digital measuring equipment used or radiated in from the direct surrounding. These high frequency components can heat up the sample [36]. Filtering is needed in that case to keep the sample as cold as possible. For this purpose we used an LC filter. This type of filter is a direct copy of the filter used by Bosch [13].

Two other types of filters are used in the cryostat (so at low temperatures).
- A copper powder filter [39, 93], which was already discussed in section 10.1.2
  - Thermocoax [136]

A copper powder filter was used to obtain the measurement results of the C-SET transistor described in section 10.2. For the electron pump (section 10.3) thermocoax was used as a filter.

10.1.5 Model of the environment setup

The sample is placed in the cryostat and the amplifiers are (still) placed outside the cryostat, this has as a consequence that long wires are used to connect the amplifier with the sample. These long wires introduce an impedance, which can not be neglected. To determine the influence of this impedance a simplified model for the wires is assumed, in which the impedance is expressed in a resistance and a capacitance.

In this section the measured capacitance and resistance of the wires from the amplifier to the sample and back are described. The wires from measurement equipment to the amplifiers are neglected because they do not have a big influence on the sample response, when the amplifier is designed correctly.

Wire resistance

Long wires give rise to the series resistance of the connection to gate, source, and drain. To measure this resistance we short circuited the sample and measured the resistance from outside. The value was $R_w = 1.47k\Omega$. A part of this value is due to 100$\Omega$ resistors used in the copper powder filter. The measured resistance is the resistance of the total wire, so we can model this as two resistors with value $R_w/2$ as shown in figure 10.8.

![Figure 10.8: The wire between the amplifier and the sample can be modeled with a resistor $R_w$ and a capacitor $C_w$.](image)

A note should be made: this resistance is measured at room temperature. The resistance will change when the circuit is cooled down.

The wires used should have a low thermal conductivity to make sure that heat is kept outside the cryostat. To transport very small electric signals the wires should have a high electrical conductivity. Unfortunately, most materials with a high electrical conductivity also have a high thermal conductivity. So optimizing wiring for a cryostat is often a compromise between the electrical and thermal requirements.

A wire connects the sample to the external world. To make sure the wire is of the same temperature as its surrounding it should be thermally connected to the stage it
10.1 Measurement setup

is passing. Extra information about the wires in a standard cryostat can be found in chapter 8 of Balshaw [10].

Capacitance of the setup

The capacitance is measured when the sample is removed. The measured capacitance is the total of the capacitance of the wires and of the sample holder. The value measured is $C_w = 3.41nF$. The high value is due to the fact that there is a filter placed near the sample to make sure that high frequencies from outside do not heat up the sample. The filter consists of 3 times $1nF$, the rest of the $C_w$ is due to the wires. Because these capacitances are integrated in the copper powder filter, we can model the capacitance value directly across the sample as is drawn in figure 10.8.

Like the resistance $R_w$, the capacitance $C_w$ is measured at room temperature.

10.1.6 Measuring errors

To summarize the problems with the measurement setup which can give errors in the measurement results:

- Noise. Because we are working with a very small signal, noise has a very large influence on the outcome.

  The influence of the noise added to the signal by the amplifiers can be minimized by using low-pass filters (see section 10.1.4), i.e. by reducing the bandwidth. This has a direct consequence for measuring high frequency behaviour, which is not possible any more. The filters used pass signals up to 10Hz.

  The applied signals are swept slowly, to make sure that due to the low pass filters, no charging or de-charging effects are measured.

  To overcome problems with low frequency noise we averaged the measured value. This has a direct consequence for signals with a high frequency; they will disappear in the measurement results. So with this setup we are unable to measure single-electron tunnel transitions.

- The large capacitance of the cryostat. This capacitance has to be charged by the signal coming from the sample. This makes the possible signal variation slow.

  A second problem with a large capacitance is that it will make the environment of the sample almost completely capacitive. As we have shown in section 9.3.4 this will result in the same critical voltages. Because of this effect it is impossible to externally connect a resistor to do measurements with different series resistors, to prove the proposed effect of resistors as was described in section 4.2.

- Offset voltages of the OpAmps used. For example the constant offset for the current bias circuit depends on the amplification. A higher offset is measured for lower amplifications, with a maximum offset of 2mV for a amplification of 1.
For the offset of the voltage biased circuit we measured an offset of 1\(pA\) for a gain of 2\(V/nA\) and an offset of 1\(nA\) for a gain of 2\(mV/nA\). When we short circuited the sample a constant offset of 0.55\(nA\) was measured.

- Differences in the resistors used. Because a symmetric supply is used (see section 10.1.3) difference in resistors used to make the current source give a shift in the horizontal direction (shown in figure 10.9). This has the same response as an initial island charge, which depends linear on the applied drain-source voltage.

![Figure 10.9: The measured voltage \(u_{ds}\) across a current biased C-SET transistor as function of the gate voltage \(u_g\) for three different currents \(i_{ds}\).](image)

From the shift of figure 10.9 we can conclude that the difference in the 1\(G\Omega\) resistors used is equal to \(\Delta R_{bias} = 50M\Omega\) (5%).

- The influence of temperature on the wires and capacitances placed in the cryostat are not taken into account. Also when the attenuators were placed in the cryostat (which was not the case in the measurement of the SET transistor), they will have a different attenuation then expected due to the low temperatures.

### 10.2 Measurements on the C-SET transistor

The sample consists of \(Al - Al_2O_3 - Al\) junctions. Fabricated by a shadow-evaporation technique [1, 130, 138]. The sample is not an ordinary SET-transistor with two junctions, but is a so called “SQUID-type”[23, 87] (see figure 10.10b). This means that two junctions are placed in parallel to form a small loop. This layout was originally designed to tune superconducting coupling by applying a magnetic flux. This feature does not affect the normal SET-transistor (the circuit of figure 10.10c)
performance when the superconduction is destroyed by applying a high field of 1 à 2 Tesla (see section 28).

![Figure 10.10: a) The symbol of a Josephson junction JJ. b) The schematic of the measured sample in the superconducting regime. c) The circuit of the measured sample when a high magnetic field is applied.](image)

### 10.2.1 Expected behaviour

In this section we will describe the results we expect to obtain from measurements. And the effect cross capacitance (see appendix E), island capacitance, and the environment of the sample created by the cryostat will have on this behaviour.

**Influence of other capacitances**

Three different types of capacitors can have some effect on the measurement results.

1. Between each node in a circuit a capacitance is formed. Capacitances between two nodes, which are not coupled by a junction or a desired capacitor, are called cross capacitances. The cross capacitances of the SET transistor are shown in figure 10.11a.

2. The capacitances from all nodes to the substrate have to be taken into account as well (figure 10.11b).

3. And we have to take into account an extra resistor and an extra capacitance due to the connection with the measuring wires as was discussed in section 10.1.5 (figure 10.11c).

All the extra capacitances, due to cryostat wires, substrate and cross capacitances, can be modelled into three capacitors. Due to the fact that the capacitances have large values, the resistance of the wires can be neglected in the model (compare figure 10.11c with figure 10.11d). If a current source with a small value is connected between ground and one of the inputs (drain d, source s, or gate g) it does not have a response like a current source but rather like a voltage source, due to the low current and large capacitors, as was discussed in section 9.3.4.

Because we are able to model the cross capacitances together with the external (outside the sample) wire capacitances, no special care has to be taken to cancel the effect the cross capacitances have. The same holds for the substrate capacitances of the gate, source, and drain connection.
Figure 10.11: a) The position of the cross capacitances. b) The position of the substrate capacitances (in the measurements described here the substrate is connected to ground). c) The sample coupled to the cryostat environment model. d) The circuit with all the extra capacitances modelled in 4 capacitors.

This leaves us with one extra capacitance to consider: $C_i$, the capacitance between island and substrate. An island will form a capacitance to the substrate. This capacitance has a finite value unequal to zero.

The island-substrate capacitance can be determined in the same way the gate capacitance is determined: by sweeping applied potential of the substrate. The measured periodicity will be equal to $\frac{q}{C_i}$ (see also section 6.2). This is not measured due to the fact that the substrate is connected to the ground of the cryostat, and hence can not be changed during the measurements.

When the source and the substrate are connected to ground the influence of $C_i$ is easy to see: the capacitance of SET junction TJ2 is enlarged by the amount of $C_i$. In the case of a symmetrical SET transistor, which is discussed here, the influence is less clear, but can be calculated. Let $C_{j1}$ be the capacitance of TJ1, $C_{j2}$ be the capacitance of TJ2, and $C_\Sigma$ be the sum of the capacitances connected to the island: $C_\Sigma = C_{j1} + C_{j2} + C_g + C_i$. The voltage across junction TJ1 is, with an island capacitance in case of a symmetrically biased SET transistor (shown in figure 10.12), equal to

$$u_{j1}(t) = u_{d1}(t) \frac{C_{j2} + C_g + C_i}{C_\Sigma} - u_g(t) \frac{C_g}{C_\Sigma} + u_{d2}(t) \frac{C_{j2}}{C_\Sigma} - \frac{q_{11}e(t)}{C_\Sigma} \tag{10.20}$$

and for junction TJ2

$$u_{j2}(t) = u_{d1}(t) \frac{C_{j1}}{C_\Sigma} + u_g(t) \frac{C_g}{C_\Sigma} + u_{d2}(t) \frac{C_{j1} + C_g + C_i}{C_\Sigma} + \frac{q_{11}e(t)}{C_\Sigma} \tag{10.21}$$
Hence the two slopes of the graph \( u_{ds} = f(u_g) \) (with \( u_{ds} = u_{d1} + u_{d2} \), with \( u_{d2} = u_{d1} \)) are equal to

\[
\frac{u_{ds}}{u_g} = \frac{C_g}{2C_{j2} + C_g + C_i} \quad (10.22)
\]

\[
\frac{u_{ds}}{u_g} = -\frac{C_g}{2C_{j1} + C_g + C_i} \quad (10.23)
\]

So the slopes will change a little due to the island capacitance. In practical situations the island capacitance will be much smaller than the capacitance of a SET junction, and the effect of the island capacitance can be neglected in the slopes found.

In the rest of this chapter we will neglect the effect of the island capacitance.

**Symmetrically biased**

It is common to measure a symmetrically biased SET transistor like drawn in figure 10.12. In general we can write for this circuit

\[
\begin{align*}
  u_{ds} &= v_d - v_s \quad (10.24) \\
  u_{gs} &= v_g - v_s \quad (10.25) \\
  v_d &= u_{d1} \quad (10.26) \\
  v_s &= -u_{d2} \quad (10.27)
\end{align*}
\]

Usually the assumption is made that \( u_{d1} = u_{d2} = u_v \), so

\[
u_v = \frac{u_{ds}}{2} \quad (10.28)
\]

With the help of the equations above, all equations already shown in section 9.3 can be transformed into the symmetrical case.

![Figure 10.12: A SET transistor in a low ohmic symmetrical environment.](image)

Let \( C_{j1} \) be the capacitance of the SET junction TJ1 and \( C_{j2} \) the capacitance of the SET junction TJ2. As shown in section 9.3.4 when \( C_{gL} \gg C_g \), and \( C_L \gg C_{j1} \) and \( C_L \gg C_{j2} + C_g \) we will get the same result for all environments, namely the one of the SET transistor placed in a completely low ohmic environment. For this reason the symmetrically biased SET transistor is only discussed in a completely low ohmic environment (as shown in figure 10.12).
Using the equations 10.20 and 10.21 with the neglection of the island capacitance \( C_i \) and the assumption \( u_{d1} = u_{d2} = \frac{u_d}{2} \), then we can write them as

\[
\begin{align*}
\frac{u_{j1}(t)}{2} &= \frac{u_d(t)}{C_i} \left( 2C_{j2} + C_g \right) - u_g(t) \frac{C_g}{C_i} - \frac{q_{i1}\varepsilon(t)}{C_i} \\
\frac{u_{j2}(t)}{2} &= \frac{u_d(t)}{C_i} \left( 2C_{j1} + C_g \right) + u_g(t) \frac{C_g}{C_i} + \frac{q_{i1}\varepsilon(t)}{C_i}
\end{align*}
\] (10.29)

The critical voltage for both junctions is

\[
u_{j1}^c = u_{j2}^c = \frac{e}{2C_i}
\] (10.31)

When we combine equation 10.29 and equation 10.30 with equation 10.31 we find for the drain source voltage for the case an electron can tunnel through junction TJ_1 and through junction TJ_2 respectively

\[
\begin{align*}
u_{ds}^{c1} &= \frac{e}{2 \left( C_{j2} + \frac{C_g}{2} \right)} + \frac{C_g u_g(t) + q_{i1}\varepsilon(t)}{C_{j2} + \frac{C_g}{2}} \\
u_{ds}^{c2} &= \frac{e}{2 \left( C_{j1} + \frac{C_g}{2} \right)} - \frac{C_g u_g(t) + q_{i1}\varepsilon(t)}{C_{j1} + \frac{C_g}{2}}
\end{align*}
\] (10.32)

(10.33)

### 10.2.2 Measurement results

The measurements were done when the C-SET transistor was symmetrically biased. Two kinds of measurements were done:

- The voltage across the sample, \( u_{ds} \), is kept constant. We sweep the gate voltage, \( u_g \) and measure the current through the device \( i_{ds} \). After which we change the voltage \( u_{ds} \) and start over again.

- The current through the sample, \( i_{ds} \), is kept constant. We sweep the gate voltage, \( u_g \) and measure the voltage across the device \( u_{ds} \). After which we change the current \( i_{ds} \) and start over again.

### Extracting the gate capacitance

A SET transistor input-output relation is periodic as has been proven in section 6.2. It is periodic with period

\[
\Delta u_g = \frac{e}{C_g}
\] (10.34)

With the help of this equation we can derive the gate capacitance from the measurement results. It is important to calculate this as precise as possible, because we need its value for determining the rest of the components values.

In figure 10.13a it can be seen that one of the periods is equal to 4.3mV, which means the gate capacitance is 37aF (using equation 10.34). In figure 10.13b it can be seen that one of the periods is equal to 4.9mV, which means the gate capacitance is 33aF. We expected no difference between the two methods; the fact that there is a difference can be caused by the difference in amplifiers used in the two measurements.
Figure 10.13: DC-measurements: a) The measured current $i_{ds}$ when the voltage $u_{ds}$ is kept constant. b) The measured voltage $u_{ds}$ when the current $i_{ds}$ is kept constant.

From these figures it is clear that we will obtain the same result for the gate capacitance when looking at a periodicity in drain-source current $i_{ds}$ or at a drain-source voltage $u_{ds}$.

**Extracting the junction capacitances**

The slopes of the input-output relation give us the values of the junction capacitances. These slopes are not effected by a high or low ohmic environment (see section 9.3.4), so it does not matter how we connect the SET transistor, we will find the same slope in the graph of $u_{ds}$ as function of the $u_{g}$.

The negative slope can be determined using equation 10.32 and is equal to

$$\frac{u_{ds}}{u_{g}} = -\frac{C_{g}}{C_{j1} + \frac{C_{g}}{2}}$$

(10.35)

This can be rewritten to

$$C_{j1} = C_{g} \left( \frac{1}{\text{neg.slope}} - \frac{1}{2} \right)$$

(10.36)

The positive slope can be determined using equation 10.33 and is equal to

$$\frac{u_{ds}}{u_{g}} = \frac{C_{g}}{C_{j2} + \frac{C_{g}}{2}}$$

(10.37)

This can be rewritten to

$$C_{j2} = C_{g} \left( \frac{1}{\text{pos.slope}} - \frac{1}{2} \right)$$

(10.38)
With these equations it is easy to calculate the junction capacitances $C_{j1}$ and $C_{j2}$. The method described above can only be done for the measurements of a constant current $i_{ds}$, so the figure 10.14 can be used. Using this figure we found: $C_g = 33aF$, $C_{j1} = 460aF$ and $C_{j2} = 500aF$.

![Graph showing voltage $u_{ds}$ as function of gate voltage $u_g$](image)

Figure 10.14: The measured voltage $u_{ds}$ as function of the applied gate voltage $u_g$ when the current $i_{ds}$ is kept constant at 12pA.

**Extracting the initial island charge**

When we do not apply any drain source voltage ($u_{ds} = 0$) we can rewrite equation 10.33 in

$$\frac{e}{2} - \left( C_g u_g(t) + q_{i1}\epsilon(t) \right) = 0$$

(10.39)

Let the background charge be $q_{bgc}$, the initial charge $q_{init}$, and the number of electrons that tunneled from the island $n$, then we can write for the island charge $q_{i1}$

$$q_{i1}\epsilon(t) = en\epsilon(t) + q_{bgc}\epsilon(t) + q_{init}\epsilon(t)$$

(10.40)

When we start increasing the gate voltage $u_g$ (so no electrons tunneled through the junctions to the island yet, $n = 0$) we would expect that we intercept with the first line in the graph when

$$u_g = \frac{e}{2 \cdot C_g} - \frac{q_{bgc} + q_{init}}{C_g}$$

(10.41)

This is shown in figure 10.15.

When we assume that there is no random background charge appearing at the moment of measuring, so $q_{bgc} = 0$, it is easy to determine the initial island charge $q_{init}$. This derivation only holds for the graph $u_{ds}$ as function of $u_g$. 
Looking at the measurements shown in figure 10.14, a horizontal voltage shift can be seen (the maximal \( u_{ds} \) is not exactly at \( u_g = 0 \)). Such a voltage shift can be explained by assuming an initial charge was on the island. The voltage shift is equal to \( u_{q_{init}} = 0.6mV \). Using the equation above and the found gate capacitance of \( C_g = 33aF \), this is equal to an initial charge of \( q_{init} = 0.2 \cdot 10^{-19}C \), which is one-eighth of an electron charge.

**Extracting the tunnel resistor**

A parameter that was also discussed in the calculations (in section 9.3.5) is one of the device constants called the tunnel resistance \( R_T \). This parameter is the ratio between the voltage and the average current (see section 3.1.5), but is not a 'real' resistance, which was already discussed in section 2.5.2. It is easy to determine by looking at the graph of the current \( i_{ds} \) through the junction as a function of the voltage \( u_j \) across the junction. For a SET transistor it is not possible to directly measure the voltage across a junction without destroying the properties of the device. So we can only measure the total voltage across both junctions \( u_{ds} \).

Let \( R_\Sigma \) be equal to the sum of the tunnel resistors, so \( R_\Sigma = R_{T1} + R_{T2} \). With the help of the in section 9.3.5 derived equation the total tunnel resistance \( R_\Sigma \) can be extracted from measurement results at high currents (where the graph is a straight line), see figure 10.16. The derived equation was (equation 9.112)

\[
i_{ds} = \frac{u_{ds} - \frac{e}{C_\Sigma}}{R_\Sigma}
\]  

(10.42)

A disadvantage of this method is that we do not know both the junction resistances separately but only the total.

To get a result like the one drawn in figure 10.16 we can do either measurements for the case of a constant voltage across the sample \( u_{ds} \) or we can look at the case of a constant current \( i_{ds} \) through the sample. In figure 10.17a and 10.17b these results are shown. In both cases the total junction resistance found is \( R_\Sigma = R_{T1} + R_{T2} \approx 1.5M\Omega \).
Figure 10.16: The average current through a tunnel junction as function of the voltage across the junction, when excited by a low ohmic connected voltage source.

Figure 10.17: a) The voltage $u_{ds}$ placed across the sample as a function of the measured current $i_{ds}$ (resulting in vertical lines). b) The measured voltage $u_{ds}$ as a function of the current $i_{ds}$ which was forced to flow through the sample (resulting in horizontal lines). In both cases (a) and b)) the darker regions are due to different gate voltages.

When the two resistances are very different we get a completely different UI-graph [132]. This graph will show a so called Coulomb staircase (for example [79]). With such a graph it is possible to determine the resistances separate. An example of such a graph is shown in figure 10.18a.

For almost equal resistors (so $R_\Sigma \approx 2R_T$) we expect to measure a peak value in current, equal to (see equation 9.106)

$$i_{ds} = \frac{u_d}{2R_T}$$

(10.43)
When we apply two voltage bias sources $u_d = u_{d1} = -u_{d2} = 42\mu V$, and the sum of the tunnel resistors is equal to $R_\Sigma = 1.5 M\Omega$ the expected current peak is

$$i_{ds} = \frac{u_d}{R_\Sigma} = 28 pA$$ (10.44)

When the measured current peak is higher than this current it can only mean that the tunnel resistors of the SET transistor are different. In figure 10.18c and d the measurement result of the measurement on a C-SET transistor are shown. Equation 10.43 is shown as a straight line in figure 10.18b and figure 10.18d. In figure 10.18d it is clear that the peak in the current is much higher than the expected value of equation 10.43, hence the tunnel resistors should be different. The best comparison between the simulation and the measurement results can be found when we simulate the SET transistor with $R_{T1} = 100k\Omega$ and $R_{T2} = 1.4 M\Omega$ (so a factor of 14 difference), see figure 10.18b. When both resistors are so different a Coulomb staircase is expected (see figure 10.18a), while this is not seen in the measurement result (see figure 10.18c).

Figure 10.18: Comparison between a simulation in SIMON and the measurements. The simulation results for a symmetrically biased C-SET transistor with $C_{j1} = 460aF$, $C_{j2} = 500aF$, $C_g = 37aF$, $q_{i1} = 0.4eC$ and two different tunnel resistors $R_{T1} = 100k\Omega$ and $R_{T2} = 1.4 M\Omega$ are drawn in figure a) for $u_g = 0V$ and b) with a bias voltage of $u_{d1} = -u_{d2} = 42\mu V$. And the measurement results of the C-SET are drawn in figure c) for $u_g = 0V$ and d) for $u_d = 42\mu V$. The straight line in the figure b) and d) is equal to equation 10.44.

Due to the fact that we are unable to measure the junction voltages separately, we are unable to derive the wait time of the different tunnel junctions (see section 3.1.4). With the measured drain-source current $i_{ds}$ and the drain-source voltage $u_{ds}$ we are able to derive the total average wait time. Let $\overline{\tau}_{u1}$ be the average wait time of tunnel junction TJ$_1$ and $\overline{\tau}_{u2}$ be the average wait time of tunnel junction TJ$_2$, then
we can define the total average wait time $\bar{\tau}_{wt}$ as

$$\bar{\tau}_{wt} = \bar{\tau}_{w1} + \bar{\tau}_{w2} = \frac{e}{I_d s} \quad (10.45)$$

In figure 10.19 a comparison is made between the simulated wait time and the measurement results.

Figure 10.19: Comparison between a simulation done in SIMON and the measurements. The simulation results for a symmetrically biased C-SET transistor with $C_{j1} = 460aF$, $C_{j2} = 500aF$, $C_g = 37aF$, $g_{d1} = 0.5eC$ and two different tunnel resistors $R_{T1} = 100k\Omega$ and $R_{T2} = 1.4M\Omega$. The measurement results of the C-SET are drawn as open circles in the figure. For both situations we derived the total average wait time $\bar{\tau}_{wt}$ (using equation 10.45) for those drain-source voltages for which one and only one junction is not in Coulomb blockade.

### 10.3 The 3 junction electron pump

The electron pump sample that was measured has been described in the literature by Zorin [91, 138]. Let $R_s$ be an extra resistor build out of chrome strips in series with the bias sources $u_{d,1}$ and $u_{d,2}$. The function of these extra resistors was to suppress the cotunneling (this is beyond the scope of this thesis, but is discussed in [138]).

The electron pump circuit that was measured consists of three junctions, two resistors, and two gates and is drawn in figure 10.20. The SEM picture of the measured electron pump is shown in figure 10.21. In [138] the fabrication method is described
which results in the expected component values (see also [91]) of

\[
\begin{align*}
C_j & \approx 150aF \quad - \quad 200aF \\
R_T & \approx 60k\Omega \quad - \quad 250k\Omega \\
C_g & \approx 20aF \\
R_s & \approx 30k\Omega \quad - \quad 80k\Omega
\end{align*}
\]  
(10.46)

![Figure 10.20: The circuit of the measured electron pump sample.](image)

![Figure 10.21: A SEM picture of the chip layout of the three junction pump with two series resistors [91, 138].](image)

### 10.3.1 Effect of cross capacitances

Cross capacitances (see appendix E) play an important role in the electron pump [71]. Let \( k_j \) be the total number of desired junctions and capacitors in the circuit, let \( k_n \) be the number of nodes in the circuit, and let \( k_{cr} \) be the number of cross capacitances. In the circuit of figure 10.20 there are eight nodes \((k_n = 8)\) and five desired capacitance (three junctions and two gates, \( k_j = 5 \)), using equation E.2, this means

\[
k_{cr} = \left( \frac{k_n}{2} \right) - k_j = \frac{k_n!}{2(k_n - 2)!} - k_j = 23
\]  
(10.47)
So there are 23 undesired (cross) capacitances. In the case of the simplified circuit of figure 10.24 there are 10 undesired cross capacitances. Due to some of these capacitances an undesired capacitive coupling arises between the gates and the islands (see figure 10.22).

![Figure 10.22: The two-island electron pump, with the two cross capacitances that couples an undesired amount of gate voltage to the other island.](image)

The effect of the two cross capacitance $C_{cr1}$ and $C_{cr2}$ shown in figure 10.22 can be eliminated by externally adding a fraction of the applied gate voltage, with opposite polarity, to the other gate [70]. The more gates the electron pump will have the harder this cancellation process it to do by hand. From the amount of extra voltage added to the other island the cross capacitance can be determined. To compensate for the undesired coupling to island 2 we can write

$$u_{g,1}C_{cr1} + u_{g,2}C_{g2} = 0$$ \hspace{2cm} (10.48)

In our measurements we needed to apply one-third of the signal of $u_{g,1}$ to $u_{g,2}$ to obtain a periodicity which was purely determined by $u_{g,1}$. So we can rewrite equation 10.48 into

$$u_{g,1}C_{cr1} - u_{g,1} \frac{1}{3}C_{g2} = 0$$ \hspace{2cm} (10.49)

$$C_{cr1} = \frac{1}{3}C_{g2}$$ \hspace{2cm} (10.50)

And to compensate for the undesired coupling to island 1 we can write

$$u_{g,1}C_{g1} + u_{g,2}C_{cr2} = 0$$ \hspace{2cm} (10.51)

To obtain a period which was only determined by $u_{g,2} = \frac{\pi}{C_{g2}}$ we needed to apply two-fifth of the signal applied to gate 2, to gate 1 in our measurements. Hence equation 10.51 can be rewritten into

$$-C_{g1} \frac{2}{5}u_{g,2} + u_{g,2}C_{cr2} = 0$$ \hspace{2cm} (10.52)

$$C_{cr2} = \frac{2}{5}C_{g1}$$ \hspace{2cm} (10.53)

For the rest of the measurements with the electron pump discussed in this section we used the method described above to compensate for the undesired phenomena created by the cross capacitances.
10.3.2 Measurement results

From the measurement results we can obtain a few parameters of the electron pump.

Extracting the gate capacitances

We can easily extract the gate capacitances from a graph with any graph as function of the gate voltage. The shape of the graph will show some periodicity due to tunneling of electrons. As was derived in section 6.2 the periodicity will be equal to

$$\Delta u_{g,a} = \frac{e}{C_{g,a}}$$

for both gates, $a = (1, 2)$.

With the help of equation 10.54 we extracted from the measurements (see figure 10.23)

$$C_{g1} = 7.1aF$$

$$C_{g2} = 8.7aF$$

Figure 10.23: The measurement results of the three-junction pump with two series resistors.

Extracting the junction capacitances

Depending on the theory we use to explain the measurement results, different outcomes can be found. Because the resistors in series have a value of $R_s \approx 30k\Omega - 80k\Omega$ which is larger than $R_k$ ($R_k = 25.8k\Omega$ see page 8) the theories for describing resistors can be divided into two parts (see section 2.4 for the descriptions):

1. The resistors in series have no influence at all on the critical voltage (the phase-correlation theory)
2. The resistors in series will disconnect the sources due to the high resistive values when deriving the critical voltage (basic Orthodox theory)

The extended Orthodox theory can not be used because the series resistor is not much smaller or larger than \( R_k \).

When the capacitances are larger than a few aF, the same answer as the basic Orthodox theory is expected when our own method (discussed in chapter 4) is used.

For the first method (phase-correlation theory) we can assume all the resistors to be short circuited. This will leave us with the basic circuit of a two island, three junction electron pump as was described and simulated in section 9.4. Let \( C_{jx} \) be the capacitance of tunnel junction \( TJ_{2} \). From figure 10.24 it is quite clear that there are 5 unknown device parameters: \( C_{j1}, C_{j2}, C_{j3}, C_{g1}, \) and \( C_{g2} \).

Figure 10.24: The circuit of an ideal two-island structure, in which the resistors are neglected.

Let \( \alpha \) be equal to the number of the junction under investigation. Let \( k_g \) be the number of gates, let \( k_{nf} \) be the number of islands, and let \( k_d \) be the number of bias sources \( u_d \). Let \( \alpha, \) and \( \beta \) be constants depending on the topology of the rest of the circuit. For the voltage across junction \( \alpha \) we can write in general, using superposition (see also equation 9.114)

\[
 u_{j,a}(t) = L^{-1} \left\{ \sum_{b=1}^{k_g} A_{b,a}^g(s) U_{g,b}(s) + \sum_{b=1}^{k_{nf}} B_{b,a}(s) Q_{i,b}(s) + \sum_{b=1}^{k_d} A_{b,a}^d(s) U_{d,b}(s) \right\} 
\]

In appendix D the derivation for all the capacitance ratios is shown for the two island electron pump. With the help of those ratios it is easy to derive expressions needed to extract the component values.

To explain the slopes of equal current of the \( u_{g,1} = f(u_{g,2}) \) relation it suffices to calculate the relation

\[
 A_{1,a}^g(s) u_{g,1}(s) + A_{2,a}^g(s) u_{g,2}(s) = 0 
\]
for all the three junctions \( a = (1, 2, 3) \). By doing so we find (see also equations 9.116 - 9.118)

\[
\begin{align*}
\frac{u_{g,1}}{u_{g,2 \ a=1}} &= -\frac{C_{g2}}{C_{g1}} \frac{C_{j2}}{C_{j1} + C_{j2} + C_{g2}} \\
\frac{u_{g,1}}{u_{g,2 \ a=2}} &= +\frac{C_{g2}}{C_{g1}} \frac{C_{j1} + C_{g1}}{C_{j3} + C_{g2}} \\
\frac{u_{g,1}}{u_{g,2 \ a=3}} &= -\frac{C_{g2}}{C_{g1}} \frac{C_{j1} + C_{j2} + C_{g1}}{C_{j2}}
\end{align*}
\]  

(10.59) (10.60) (10.61)

Because we already know the gate capacitances, we are left with three equations and three unknowns, which can be solved.

With the help of equations 10.59 - 10.61 and using the gate capacitances of equation 10.55 and 10.56 we extract from the slopes of figure 10.23 the junction capacitances

\[
\begin{align*}
C_{j1} &= 38.5aF \\
C_{j2} &= 31.3aF \\
C_{j3} &= 39.6aF
\end{align*}
\]  

(10.62) (10.63) (10.64)

To derive the slopes with the help of our own theory is a more complex method, because the resistors are not assumed to be zero. We use the fact that every slope is caused by a single junction. Hence we should calculate the voltage across junction TJ1 as function of \( u_{g,1} \) (with \( u_{g,2} = 0 \), using superposition) and as function of \( u_{g,2} \) (with \( u_{g,1} = 0 \)). These two voltages are depending on all component values. In the found expressions we can use the neglections indicated in section 4.2.1 (equations 4.18 - 4.21). After this we will find for the two expressions

\[
\begin{align*}
U_{j1}(s) &= \frac{1}{R_{s1}sC_{j1}} \frac{C_{j1}}{C_{g1} + \frac{C_{j2}C_{g2}}{C_{j2}+C_{g2}}} U_{g,1}(s) \\
U_{j1}(s) &= \frac{1}{R_{s1}sC_{j1}} \frac{C_{g1}}{C_{j2} + \frac{C_{g1}C_{g2}}{C_{j2}+C_{g2}}} U_{g,2}(s)
\end{align*}
\]  

(10.65) (10.66)

Hence the slope for junction TJ1 will be

\[
\frac{u_{g,1}}{u_{g,2 \ a=1}} = -\frac{C_{g2}}{C_{g1}} \frac{C_{j2}}{C_{j1} + C_{j2} + C_{g2}}
\]  

(10.67)

The same derivation can be done for junction TJ2 and TJ3, which results in

\[
\begin{align*}
\frac{u_{g,1}}{u_{g,2 \ a=2}} &= +1 \\
\frac{u_{g,1}}{u_{g,2 \ a=3}} &= -\frac{C_{g2}}{C_{g1}} \frac{C_{j1} + C_{g1}}{C_{j2}}
\end{align*}
\]  

(10.68) (10.69)

Because in figure 10.23 no slope is '1', we can not use this method to derive the slopes.
The effect of measurement errors

As a starting point to derive the capacitor values of the junctions and the gate capacitances from the measurements, we assume that the measured voltages (which are already scaled due to dividers which are placed in the measurement setup) are correct. Secondly, we assume that there are no resistors on chip so we can use the equations above. Simulating the pump with SIMON using the gate capacitance values of equation 10.55 and equation 10.56, and the junction capacitances of equation 10.62 - 10.64, results in the figure 10.25, which indeed shows a behaviour equal to the measurements.

According to the article of Lotkhov et al [91], in which he describes the same structure, the series resistors are in the order of 30kΩ. When adding those to the SIMON simulation, we obtain the result of figure 10.26, which also shows a result which can be compared to the measurement setup. One conclusion that can be drawn from these last two simulations is the fact that adding resistors in SIMON, does not change the shape of the simulation result, it does however change the necessary supply voltage.

![Simulation result](image)

Figure 10.25: The simulation results (obtained by SIMON) of the three-junction pump without the two series resistors. With $C_{j1} = 38.5aF$, $C_{j2} = 31.3aF$, $C_{j3} = 39.6aF$, $C_{g1} = 7.1aF$, $C_{g2} = 8.7aF$, $R_{T1} = R_{T2} = R_{T3} = 500kΩ$, $q_{i1} = 0$, $q_{i2} = -0.3eC$, and $u_{d,1} = -u_{d,2} = 0.9mV$.

When we again look at the article of Lotkov et al [91] it is clear that the found capacitances for the SET junctions are too low. According to the mentioned article the values should be $C_j \approx 250aF$, $C_g \approx 20aF$, and $R_s = 60kΩ$ (because two resistors are placed in parallel, the expected series resistor will be 30kΩ), see also the expected values discussed on page 227. When we assume their value indication is correct, this has a direct consequence for the found results. When we do a simulation in SIMON
Figure 10.26: The simulation results (obtained by SIMON) of the three-junction pump with the two series resistors, $R_{s1} = R_{s2} = 30k\Omega$. With the same component values as used for figure 10.25, except $u_{d1} = -u_{d2} = 2.2mV$.

with the component values described in the article we again obtain the same shapes as figure 10.25, only the values along the axes are different (see figure 10.27).

Figure 10.27: Simulation results of the three-junction pump obtained from SIMON, with $C_{j1} = C_{j2} = C_{j3} = 200aF$, $R_{T1} = R_{T2} = R_{T3} = 250k\Omega$, and $C_{g1} = C_{g2} = 20aF$. a) The pump without the two series resistors, with $u_{d1} = -u_{d2} = 150\mu V$.  b) The simulation with $R_{s1} = R_{s2} = 30k\Omega$ and $u_{d1} = -u_{d2} = 0.35\mu V$.

From this result it is clear that we can say nothing about the values along the axes of the measurement results, because the wire resistances, attenuators, etc determine those values. Sadly we are not able to measure the voltages directly on chip, and hence all those inaccuracies should be taken into account in the calculations. The
only thing we know for sure is that the attenuation for both the gate voltages is almost the same (the difference will be neglectable). From this we can conclude that the calculation of the slopes is unaltered by the values along the axes. So we have three equations (of the three slopes) to derive all capacitance values (5 pieces), and the two unknown resistors. We do not know both the island charges, and the exact bias voltages and gate voltages.

**Pumping principle**

To let the structure operate as it was meant to: to pump electrons in a controllable way, we need to apply two signals to the gates which are $\frac{\pi}{2}$ out of phase, see section 9.4.2. For this purpose we used the hardware designed at the National Institute of Standards and Technology (NIST), which was designed for six gates [70]. The clock frequency was divided into seven cycles (see figure 10.28). Let $f_{cl}$ be the clock frequency. Hence the frequency applied to one gate was $\frac{f_{cl}}{7}$.

![Image](image.png)

**Figure 10.28**: The six outputs of the gate signal generator used. The period of one gate signal is $\tau_g = 7\tau_{cl}$, with $\tau_{cl} = \frac{1}{f_{cl}}$.

Because the leakage current and offset current of the measurement setup are not known exactly, and we are measuring very small currents, the current through the pump is not measured. A different approach is chosen, not the current in one direction is measured but the difference between the currents flowing in both directions (in different time spans). Let $\tau_{cyc}$ be the time span in which the current is switched in both directions. The electron is transferred in one direction during $\frac{\tau_{cyc}}{2}$, after which it flows in the opposite direction (during a same amount of time). In this way a change in current occurs equal to twice the current that is flowing through the electron pump.
structure. Let \( \Delta i_p \) be the drop in current, then we can write (see also equation 6.3)

\[
\Delta i_p = 2e \frac{f_{cl}}{7}
\]  

(10.70)

See figure 10.29 for the measurement results.

Figure 10.29: The current measured through the pump structure, when a clock is applied of \( f_{cl} = 50 MHz \) which is divided into 7 channels. To be able to measure this accurately the pump is switched in two directions hence the current difference should be \( \Delta i_p = 2e f_{cl}/7 = 2.28 pA \).

10.4 Conclusions

We are unable to accurately measure the voltages across the sample placed in the cryostat. To predict the measured values, the measured values are divided by the amplification factor and multiplied by the attenuation factors. In this way the predicted voltages across the sample and the predicted currents through the sample can be obtained.

When the dimensions of the components can be made smaller in the future, the operating temperature will increase. Then we are able to measure at higher temperatures, so the effects of the low temperatures and the cryostat will play no role in the measurement results anymore. We expect that the predicted values will be in those cases in better agreement with the real sample values.
"A conclusion is the place where you got tired of thinking."
Martin H. Fischer

"People do not like to think. If one thinks, one must reach conclusions. Conclusions are not always pleasant."
Helen Keller

11 Conclusions

Even if it will be possible to accurately manufacture CMOS transistors in the future with a gate length of just a few nm which still operate as normal CMOS transistors, they will not have the advantages of circuits build with Single-Electron Tunnel (SET) junctions operating in the single-electron regime, which are: discrete controllable tunnel events, periodic behaviour, extremely low power (due to these single-electron currents), and very high speeds (tunneling of an electron is a process which is very fast).

One of the problems in circuit design with SET junctions and the fabrication of circuits with SET junctions are the cross capacitances. One way of dealing with this problem is by using large spaces between the different sub-circuits; hence we lose one of the main advantages of nano-scale devices, which was the possible high density on chip. So instead of looking at the size as the main aspect of interest in nano-scale devices, we should focus on the difference in the behaviour!

In our opinion it is better to use the special features of the SET (like periodicity, and discrete single-electron tunnel events) in combination with the behaviour of well known components like the CMOS transistor, instead of using SET transistors for reduction of size and copying the basic structures (like inverters) which almost all researchers are doing at this moment. In this last case the SET will lose the battle with CMOS due to fabrication defects, accuracy, and speed. Instead of trying to copy CMOS structures into SET structures we should use the extra features of SET sub-circuits and combine these sub-circuits with other (non-SET) components to achieve the best result.

The proposed model for the SET junction, discussed in the existing theories, is unable to model the single-electron behaviour of the SET junctions. This model is designed to model Coulomb blockade or tunnel currents (tunnel rate). Because of the already mentioned opinion that the single-electron behaviour of the SET is the most important feature, a new model should be created which emphasises this behaviour. With the help of this new model we are able to design structures using the specific single-electron behaviour.
The charge transfer of one electron from one side of the junction to the other side is modelled by a current source, which also makes our circuit satisfy the condition of energy conservation. The tunnel condition of our SET junction model is based on the energy loss due to a tunnel event.

The second model that has been developed is the model for the independent island charges. Due to the modelling of the independent island charges as separate excitations it became possible to use superposition. This makes it simpler to synthesis circuits with SET junctions.

The circuits discussed in this thesis are based on the single-electron behaviour (also known as single-electron electronics). To obtain this behaviour complex structures (like the electron pump), or simple (single junction) structures (like the electron-box) should be used. A lot of functions (like NAND, NOR, AD converter) can easily be implemented with an electron-box structure. Such a structure has some big disadvantages: it is hard to couple, and random background charges will destroy the desired behaviour. The advantages are: low power consuming (only one electron 'current'), fast (transition of one electron can go with a time $\tau_t = 10^{-15} s$), simple (only one junction is needed).
Part IV

Appendix
A

Energy calculations

A.1 Example of an energy calculations

In the Orthodox theory the tunnel condition is based on energy differences of the complete circuit. In this appendix we show how the energy calculation is done for a simple circuit: two SET junctions in series.

To find out if an electron is allowed to tunnel through junction TJ$_2$ (see figure A.1) we need to calculate the energy before this tunnel event and the energy after the tunnel event (see section 2.2). Let $E_b$ be the energy before and $E_a$ the energy after the tunnel event, then we can write for energy change

$$\Delta E = E_b - E_a \quad (A.1)$$

This energy should be less than zero, in other words the energy should be reduced, to let an electron tunnel.

![Diagram of a two junction circuit with a tunnel event through junction 2.](image)

Figure A.1: A two junction circuit with a tunnel event through junction 2.
Let $C_{j1}$ be the capacitance of tunnel junction TJ$_1$ and let $C_{j2}$ be the capacitance of tunnel junction TJ$_2$. Using Kirhoffs voltage law we find for this circuit

$$u_s = \frac{q_{j1}}{C_{j1}} + \frac{q_{j2}}{C_{j2}}$$  \hspace{1cm} (A.2)

After the electron has tunneled Kirhoffs voltage law should still hold. The charges on the junctions are changed a bit due to the tunnel event.

$$u_s = \frac{q_{j1} + dq_{j1}}{C_{j1}} + \frac{q_{j2} + dq_{j2}}{C_{j2}}$$  \hspace{1cm} (A.3)

Combining equation A.2 with equation A.3 gives the condition for the change in charge

$$\frac{dq_{j1}}{C_{j1}} + \frac{dq_{j2}}{C_{j2}} = 0$$  \hspace{1cm} (A.4)

The island charge is decreased with $e$, so

$$-dq_{j1} + dq_{j2} = -e$$  \hspace{1cm} (A.5)

Using equation A.4 and equation A.5 we can find for the charge change

$$dq_{j1} = e\frac{C_{j1}}{C_{j1} + C_{j2}}$$  \hspace{1cm} (A.6)

$$dq_{j2} = -e\frac{C_{j2}}{C_{j1} + C_{j2}}$$  \hspace{1cm} (A.7)

For the energy difference $\Delta E$ between the energy before the tunnel event $E_b$ minus the energy after the tunnel event $E_a$ ($\Delta E = E_a - E_b$) of the three components, we can write:

- The energy change of junction TJ$_1$ is

$$\Delta E_{j1} = \frac{(q_{j1} + dq_{j1})^2}{2C_{j1}} - \frac{q_{j1}^2}{2C_{j1}}$$  \hspace{1cm} (A.8)

After simplification and combination with equation A.6

$$\Delta E_{j1} = e\frac{q_{j1}}{C_{j1} + C_{j2}} + \frac{e^2 C_{j1}}{2(C_{j1} + C_{j2})^2}$$  \hspace{1cm} (A.9)

- The energy change of junction TJ$_2$ is

$$\Delta E_{j2} = \frac{(q_{j2} + dq_{j2})^2}{2C_{j2}} - \frac{q_{j2}^2}{2C_{j2}}$$  \hspace{1cm} (A.10)

After simplification and combination with equation A.7

$$\Delta E_{j2} = -e\frac{q_{j2}}{C_{j1} + C_{j2}} + \frac{e^2 C_{j2}}{2(C_{j1} + C_{j2})^2}$$  \hspace{1cm} (A.11)
• Energy is delivered by the voltage source during this tunnel event. A charge $dq_{j1}$ has been transported through the voltage source resulting in an energy of

$$\Delta E_s = dq_{j1}u_s$$  \hspace{1cm} (A.12)
$$\Delta E_s = e\frac{C_{j1}}{C_{j1} + C_{j2}}u_s$$  \hspace{1cm} (A.13)

The voltage source delivered this energy to the circuit.

The two energy changes (equations A.9 and A.11) combined with the independent charge on the island before the tunneling started

$$q_i = -q_{j1} + q_{j2}$$  \hspace{1cm} (A.14)

gives the total difference in stored energy on the capacitors is

$$\Delta E_{se} = \Delta E_{j1} + \Delta E_{j2}$$  \hspace{1cm} (A.15)
$$\Delta E_{se} = -e\frac{1}{C_{j1} + C_{j2}}(q_i - \frac{e}{2})$$  \hspace{1cm} (A.16)

A part of this energy is delivered by the voltage source. When we subtract the energy delivered by the voltage source from this difference in stored energy we get

$$\Delta E = \Delta E_{se} - \Delta E_s$$  \hspace{1cm} (A.17)
$$\Delta E = -e\frac{1}{C_{j1} + C_{j2}}\left(u_s C_{j1} + q_i - \frac{e}{2}\right)$$  \hspace{1cm} (A.18)

This energy is the change in the total energy due to the tunneling of one electron through junction TJ_2.

Remarkable is the fact that the island charge after the tunnel event is not directly included in equation A.18.

A.2 The change in energy expressed in voltages

The energy change derived in appendix A.1 can be expressed in voltages, after which it becomes possible to express the tunnel condition in voltages as well.

The total energy that has left the circuit can be rewritten to (starting by rewriting equation A.18)

$$\Delta E = -\frac{e}{2}\left(2u_s\frac{C_{j1}}{C_{j1} + C_{j2}} + \frac{2q_i - e}{C_{j1} + C_{j2}}\right)$$  \hspace{1cm} (A.19)
$$\Delta E = -\frac{e}{2}\left\{\left(u_s\frac{C_{j1}}{C_{j1} + C_{j2}} + \frac{q_i}{C_{j1} + C_{j2}}\right) + \left(u_s\frac{C_{j1}}{C_{j1} + C_{j2}} + \frac{q_i - e}{C_{j1} + C_{j2}}\right)\right\}$$  \hspace{1cm} (A.20)

Let $u_{b2}$ be the voltage across the SET junction TJ_2 before the tunnel event and $u_{a2}$ the voltage after the tunnel event. Then we can write for the change in charge $\Delta E = E_a - E_b$, using equation A.20

$$\Delta E = -\frac{e}{2}(u_{b2} + u_{a2})$$  \hspace{1cm} (A.21)
So the tunnel condition will be

\[ \Delta E = E_a - E_b < 0 \]  \hspace{1cm} (A.22)  
\[ -\frac{e}{2}(u_b2 + u_a2) < 0 \]  \hspace{1cm} (A.23)  
\[ u_b2 + u_a2 > 0 \]  \hspace{1cm} (A.24)

### A.3 Energy of the tunnel current source

By using a current source to model the electron tunneling, see figure A.2, we obtained an electrically correct equivalent circuit (charge conservation). The equivalent circuit should also have energy conservation. The amount of energy lost \( \Delta E_i \) in the current source is in general

\[ \Delta E_i = \int_{t_b}^{t_a} u_j(t)i(t)dt \]  \hspace{1cm} (A.25)

For the voltage \( u_j \) across the current source we can write (see figure A.3a)

\[ u_j(t) = u_{jb} - k(t)(u_{jb} - u_{ja}) \]  \hspace{1cm} (A.26)

with

\[ k(t) = 1 \quad \text{for} \quad t < t_a \]  \hspace{1cm} (A.27)  
\[ k(t) = 0 \quad \text{for} \quad t > t_b \]  \hspace{1cm} (A.28)

![Figure A.2](image_url)

Figure A.2: a) The symbol for the SET junction. b) The proposed model for a SET junction. In this model tunneling through the insulator of the junction with a capacitance \( C_j \) is modelled by a current source (copy of figure 3.7).

For the tunnel current \( i(t) \) we can write (see equation 3.14)

\[ i(t) = el(t) \]  \hspace{1cm} (A.29)  
\[ \int_{t_b}^{t_a} l(t)dt = 1 \]  \hspace{1cm} (A.30)
with \( l(t) \) the shape of the tunnel current \( i_t \) (figure A.3b), only the borders are of interest here, they are

\[
\begin{align*}
    l(t) &= 0 \quad \text{for} \quad t < t_b \\
    l(t) &= 0 \quad \text{for} \quad t > t_a
\end{align*}
\]  
(A.31)  
(A.32)

In the case of a pure capacitive network we can define the relation between \( k \) and \( l \)

\[
l(t) = \frac{dk(t)}{dt} \quad \forall \ t
\]  
(A.33)

![Diagram](image)

Figure A.3: a) The shape of the voltage \( u_j \) across the current source is still undefined during the tunnel event. b) Exactly a charge \( e \) is transferred, the shape of the tunnel current \( i_t \) is still undefined during the tunnel event.

For the energy of the current source we can write

\[
\Delta E_i = e \int_{t_b}^{t_a} \{ u_{jb} - k(t)(u_{jb} - u_{ja}) \} l(t) dt  
\]  
(A.34)

\[
\Delta E_i = e u_{jb} \int_{t_b}^{t_a} l(t) dt - e (u_{jb} - u_{ja}) \int_{t_b}^{t_a} k(t) l(t) dt  
\]  
(A.35)

\[
\Delta E_i = e u_{jb} - e (u_{jb} - u_{ja}) \int_{0}^{1} k(t) dk(t)  
\]  
(A.36)

\[
\Delta E_i = e u_{jb} - e (u_{jb} - u_{ja}) \frac{1}{2} [k(t)^2]_{0}^{1}  
\]  
(A.37)

\[
\Delta E_i = \frac{e}{2} (u_{jb} + u_{ja})  
\]  
(A.38)

\[
\Delta E_i = \frac{e}{2} (u_{jb} + u_{ja})  
\]  
(A.39)

The change in energy caused by the tunnel current source, equation A.39, is the same as the total energy change of the circuit, including the energy delivered or subtracted
by the other sources in the circuit (see for example appendix A.1 equation A.21). In this way we maintain not only charge conservation but also energy conservation of the whole circuit.

A.4 The energy change in a system with a resistor

Let $\Delta E_R$ be the change in energy in a resistor, $i_R$ the current through the resistor, and $u_R$ the voltage across the resistor. In general we can write for this energy change between $t_x$ and $t_y$ (with $t_x \neq t_y$)

$$\Delta E_R = \int_{t_x}^{t_y} i_R u_R dt$$ (A.40)

When a resistor $R$ is placed in series with a tunnel junction TJ and some other components (see figure A.4), the energy change of the resistor can also be written as

$$\Delta E_R = \int_{t_x}^{t_y} i_R (u_s - u_j - u_x) dt$$ (A.41)

![Figure A.4: A general circuit to determine the energy between time $t_x$ and time $t_y$ of a resistor, which is placed in series with a tunnel junction and some other circuit components.](image)

The current through all those elements in series is equal (Kirchhoff's current law) so equation A.41 can be rewritten as

$$\Delta E_R = \int_{t_x}^{t_y} i_{us} u_s dt - \int_{t_x}^{t_y} i_j u_j dt - \int_{t_x}^{t_y} i_x u_x dt$$ (A.42)

which is equal to the sum of all the energy differences in the circuit. Let $\Delta E_s$ be the energy delivered to the system by the source $u_s$, let $\Delta E_j$ be the energy difference of
the junction, and let $\Delta E_x$ be the difference in energy of the other components, then we can write

$$\Delta E_R = \Delta E_s - \Delta E_j - \Delta E_x$$  \hspace{1cm} (A.43)

Concluding: no matter how long the time between $t_x$ and $t_y$ is, the change in energy of the resistor will always be equal to the difference in energy in the total circuit. Hence there will always be energy conservation and no difference in system energy (due to losses that are not modelled).
In this appendix we calculate the change in charge due to a tunnel event, with zero tunnel time. The change in charge is calculated directly after the tunnel event. The circuit used for the example shown here is given in figure B.1. A remark should be made about this circuit: in the Orthodox theory no model is made for the tunnel event itself. For that reason we have drawn in the figure an arrow to indicate the movement of a charge equal to the elementary charge $e$ due to the tunnel event.

![Circuit Diagram](image)

Figure B.1: A simple circuit consisting of a tunnel junction TJ with resistor $R$ in series.

Let $i_R(t)$ be the current through the resistor $R$ and let $i_c(t)$ be the current through the capacitance of the tunnel junction. And using the fact that the Orthodox theory assumes a zero tunnel time the tunnel event itself should be written as a charge movement of $e\delta(t)$. For this reason we can write in the Laplace domain using Kirchhoff's current law

$$I_R(s) = e + I_c(s) \quad (B.1)$$

Let $u_R(t)$ be the voltage across the resistor $R$ and let $u_j(t)$ be the voltage across the junction, then we can write in the Laplace domain using Kirchhoff's voltage law

$$U_R(s) = U_s(s) - U_j(s) \quad (B.2)$$
Assuming the voltage source \( u_s \) is a constant source with value
\[
\begin{align*}
\quad u_s(t) &= X \\
\quad U_s(s) &= \frac{X}{s}
\end{align*}
\] (B.3) (B.4)

For the resistor Ohm's law holds
\[
U_R(s) = I_R(s)R
\] (B.5)

Using equation B.2 and B.4 we can rewrite this into
\[
I_R(s) = \frac{U_s(s) - U_j(s)}{R} = \frac{X}{sR} - \frac{U_j(s)}{R}
\] (B.6) (B.7)

For the capacitance \( C_j \) we can write (assuming it was charge up to \( X \) at \( t = 0^- \))
\[
I_c(s) = U_j(s)Cs - XC
\] (B.8)

Filling equations B.7 and B.8 in equation B.1 will result in
\[
\frac{X}{sR} - \frac{U_j(s)}{R} = e + \left( U_j(s)Cs - XC \right)
\] (B.9)

Which is equal to
\[
\begin{align*}
X - sU_j(s) &= eR_s + U_j(s)CRs^2 - XCRs \\
\left( -s - RCs^2 \right)U_j(s) &= -X + eR_s - XCRs \\
\left( s + RCs^2 \right)U_j(s) &= X \left( 1 + RCs \right) - eRs \\
U_j(s) &= \frac{X \left( 1 + RCs \right)}{s \left( 1 + RCs \right)} - e \frac{Rs}{s \left( 1 + RCs \right)} \\
U_j(s) &= X \frac{1}{s} - e \frac{R}{1 + RCs}
\end{align*}
\] (B.10) (B.11) (B.12) (B.13) (B.14)

Using the fact that the tunnel time is zero we need to use the initial value theorem of Laplace [55], which state
\[
\lim_{t \to 0} g(t) = \lim_{s \to \infty} sG(s)
\] (B.15)

So using this on equation B.14 will result in
\[
\begin{align*}
\lim_{s \to \infty} sU_j(s) &= \lim_{s \to \infty} s \left( X \frac{1}{s} - e \frac{R}{1 + RCs} \right) \\
\lim_{s \to \infty} sU_j(s) &= \lim_{s \to \infty} \left( X - e \frac{Rs}{1 + RCs} \right) \\
\lim_{s \to \infty} sU_j(s) &= X - e \lim_{s \to \infty} \frac{R}{\frac{1}{s} + RC} \\
\lim_{s \to \infty} sU_j(s) &= X - e \frac{R}{RC} \\
\lim_{s \to \infty} sU_j(s) &= X - e \frac{C}{R}
\end{align*}
\] (B.16) (B.17) (B.18) (B.19) (B.20)
So for the junction voltage \( u_j(t) \) just after the tunnel event we can write

\[
u_j(0^+) = X - \frac{e}{C}
\]

(B.21)

From equation B.21 it is clear that the change in voltage across the junction (due to the tunnel event) is equal to \( \frac{e}{C} \). So the change in charge on the “plates” of the SET junction TJ (due to the tunnel event) is equal to \( e \), hence no charge redistribution through the resistor took place.
The change in charge due to a tunnel event
Phase correlation theory

The Phase correlation is also known as the $P(E)$-theory.

C.1 Derivation of the $P(E)$ picture

In this appendix we will derive the equations needed for pictures that are shown in many articles and books. In such a picture the chance $P(E)$ as function of the energy $E$ is drawn. As a simplification we will use, like is done in those references:

- Zero temperature $T = 0K$
- A purely resistive environment $Z(\omega) = R$
- A simple circuit, consisting out of only a junction TJ

In figure C.1 the structure is drawn.

![Figure C.1: The analysed structure, consisting of a junction TJ with its environment modelled as a purely resistive $R$.](image)

The so called $P(E)$ theory starts with two equations. For the derivation of those equations see [66].

1. Fourier transform of the correlation function, see formula 50 of [66]. $P(E)$ is the probability that a tunneling electron will exchange energy $E$ with its
environment (Wasshuber [130] formula 2.58). \( P(E) \) gives the probability for a tunneling electron to loose the energy \( E \) to the environment: equation 2 of [65], or equation 4.26 of [101].

\[
P(E) = \frac{1}{h} \int_{-\infty}^{+\infty} \exp \left[ K(t) + \frac{jEt}{h} \right] dt \quad (C.1)
\]

2. The correlation function, formula 64 of [66], or equation 4.29 of [101]. Those are almost the same (only the borders differ) as equation 3 of [65] and the phase correlation function of Wasshuber formula 2.59 [130]

\[
K(t) = 2 \int_{0}^{\infty} \mathcal{R} \{ Z(\omega) \} \frac{1}{\omega} \left[ \coth \left( \frac{1}{2k_BT} \hbar \omega \right) (\cos(\omega t) - 1) - j \sin(\omega t) \right] d\omega \quad (C.2)
\]

Due to the above assumptions we can simplify these equations. A temperature of zero gives

\[
\coth \left( \frac{1}{2k_BT} \hbar \omega \right) = 1 \quad (C.3)
\]

So we can write for \( K(t) \)

\[
K(t) = 2 \int_{0}^{\infty} \mathcal{R} \{ Z(\omega) \} \frac{\exp(-j\omega t) - 1}{\omega R_k} d\omega \quad (C.4)
\]

Which is equation 73 of [66].

Let \( C_j \) be the capacitance of junction TJ. Due to the purely resistive environment we can write

\[
Z(\omega) = \frac{\frac{1}{j\omega C_j}}{R + \frac{1}{j\omega C_j}} \quad (C.5)
\]

\[
Z(\omega) = \frac{R}{j\omega RC_j + 1} \quad (C.6)
\]

\[
Z(\omega) = \frac{R}{j\omega RC_j + 1} \left( \frac{-j\omega RC_j + 1}{-j\omega RC_j + 1} \right) \quad (C.7)
\]

\[
Z(\omega) = \frac{R (1 - j\omega RC_j)}{\omega^2 R^2 C_j^2 + 1} \quad (C.8)
\]

\[
\mathcal{R} \{ Z(\omega) \} = \frac{R}{\omega^2 R^2 C_j^2 + 1} \quad (C.9)
\]

Combining of equation C.1, equation C.4, with equation C.9 will result in (see for the derivation [66])

\[
\int_{0}^{E} \mathcal{R} \left\{ Z \left( \frac{E - E'}{h} \right) \right\} P(E') dE' \quad (C.10)
\]
This is equation 75 of [66]. With the help of this equation we can write
\[
P(E) = \frac{2}{R_k} \int_0^E \mathcal{R} \left\{ Z \left( \frac{E-E'}{\hbar} \right) \right\} P(E')dE'
\]
\[
P(E) = \frac{2}{R_k} \int_0^E \mathcal{R} \left\{ Z \left( \frac{E-E'}{\hbar} \right) \right\} P(E')dE'
\]
\[
E
\]
\[
(C.11)
\]
According to [66] 'it is not possible to obtain analytical results for the Ohmic model'. So to get a picture showing \( P(E) \) as function of \( E \) we should use numerical methods. Equation C.11 enables us to calculate \( P(E) \) numerically by starting from an arbitrary \( P(0) \).

This picture can be done in three steps:\(^1\):

1. First we calculate the real part of the impedance \( Z \) at different energies. This real part was already determined, see equation C.9
\[
\mathcal{R} \{ Z(\omega) \} = \frac{R}{R^2 C_j^2 \omega^2 + 1}
\]
\[
(C.12)
\]
Because of equation C.11 and the normalizing of the axis, we use
\[
\omega = \omega_0 \frac{E}{E_c}
\]
\[
(C.13)
\]
with (using equation 108 of [66])
\[
\omega_0 = \frac{E_c}{\hbar} = \frac{\pi}{R_k C_j}
\]
\[
(C.14)
\]
and
\[
E_c = \frac{e^2}{2C_j}
\]
\[
(C.15)
\]
2. The second step is to calculate \( P(E) \) using a discrete version of equation C.11
\[
P(a) = \frac{2}{R_k} \sum_{d=1}^{a-1} \mathcal{R} \{ Z(a-d) \} P(d) \Delta E
\]
\[
(C.16)
\]
making use of \( E = a \Delta E \), with \( \Delta E \) the chosen step size between the calculated points
\[
\Delta E = \frac{\dot{E}}{k_{st}}
\]
\[
(C.17)
\]
with \( \dot{E} \) the maximal energy we want to show on the horizontal axes, and \( k_{st} \) the number of steps desired in the calculation.

3. After this we should normalize the result such that
\[
\int_{-\infty}^{+\infty} P(E)dE = 1
\]
\[
(C.18)
\]
\(^1\) Found with the help of a MS Quick Basic program written by A. Zorin.
This can be done by first calculating the area $A_r$ below the graph

$$A_r = \sum_{d=1}^{k_{st}} P(d) \Delta E$$  \hspace{1cm} (C.19)

After which every data point is divided by this $A_r$ to normalise it till '1'.

This results in figure C.2.

Figure C.2: Four different plots of $P(E)$ as function of $E$ due to a different series resistor.

### C.2 The i-u curve

Starting with equation 79 of [66]

$$i_j (u_j) = \frac{1}{eRT} \int_0^{eu_j} (eu_j - E) P(E) dE$$  \hspace{1cm} (C.20)

This can be simplified to

$$i_j (u_j) = \frac{1}{eRT} \left( eu_j \int_0^{eu_j} P(E) dE - \int_0^{eu_j} EP(E) dE \right)$$  \hspace{1cm} (C.21)

This can be solved numerical using

$$i_j (u_j) = \frac{1}{eRT} \left( eu_j \sum_{d=0}^{k_{st}} P(d) \Delta E - \sum_{d=0}^{k_{st}} d\Delta E P(d) \Delta E \right)$$  \hspace{1cm} (C.22)
with \( E = d\Delta E \) and \( cu_j = E \).

In figure C.3 the current as function of the voltage is drawn.

Figure C.3: The i-u plot of a single junction with a resistor in series, with \( R = 250\Omega, 2.5k\Omega, 25k\Omega, 250k\Omega \).
A general method to derive the node voltages

To be able to use the critical voltage a method is needed to calculate the voltage across a junction in a simple way. In this appendix we will discuss a method useable for linear circuits to calculate the potential on each node, and thus the voltage across a SET junction. With the help of that method it is also possible to calculate the impedance between two nodes, on which the critical voltage depends (see section 4).

To be able to calculate the voltage across a junction for large and complex circuits we should use some simple rules to describe the influence that a source, connected between two nodes, has on the nodes in the rest of the circuit. In this section we show a method to calculate the potential somewhere in the circuit or the voltage across a component.

For a circuit designer it is desirable (if possible) to get a first impression of the behaviour of a circuit based on simple circuit rules. The method described in this section is designed for simple calculations by hand. When using a computer more complex algorithms can be used to obtain the same results in a faster way and also more complex structures can be analysed. These types of algorithms are outside the scope of this thesis.

D.1 Node potentials

We assume that a SET circuit can be split into a linear circuit, containing linear components (resistors $R$, inductors $L$, and capacitors $C$), and sources. As was discussed in section 3.2 we have to model the independent node charge as a separate source to obtain a linear circuit. This is schematically drawn in figure D.1. The sources are:

1. Sources to model the tunnel events (see section 3.1)

2. Sources to model independent charges on nodes in the circuit (see section 3.2).
3. Signal sources (see section 5.1)

4. Bias sources (see section 5.2).

Figure D.1: The separation of the sources from a SET circuit, to make the remaining circuit linear. In this example the circuit only contains three sources $S_1$, $S_2$, and $S_3$.

Due to the fact that we assumed that the rest of the circuit is linear, each independent source $S$ (current or voltage source) can be treated separately (using superposition, as was discussed in section 3.2.1) to analyse the influence they have on the circuit.

Each independent source $S$ creates a certain potential $v$ at the nodes in the circuit. When we add all the potentials of one node due to each source, which is equal to using superposition, we obtain the total node potentials due to all the independent sources.

In figure D.2 four nodes (0, 1, 2, and 3) are drawn. Between node 1 and node 2 an impedance $Z_{12}(s)$ is placed, and the total impedance between node 0 and node 2 is called $Z_{02}(s)$. This is drawn for the source $S_1$ which is part of the circuit. We assume here that source $S_1$ is connected between node 0 and the reference potential node 1, resulting in a known voltage $u_{01}(t)$.

Figure D.2: An example: The circuit connected to source $S_1$. In this circuit we can calculate four potentials due to the five impedances.
When we are interested in the potential on node 2, we first calculate the voltage across $Z_{12}(s)$ due to source $S_1$

$$U_{12}(s) = \frac{Z_{12}(s)}{Z_{12}(s) + Z_{02}(s)} U_{01}(s) \quad (D.1)$$

When we relate all potentials to node 0 we can express this in potentials

$$V_1(s) - V_2(s) = \frac{Z_{12}(s)}{Z_{12}(s) + Z_{02}(s)} V_1(s) \quad (D.2)$$

Which is equal to

$$V_2(s) = \frac{Z_{02}(s)}{Z_{12}(s) + Z_{02}(s)} V_1(s) \quad (D.3)$$

This is only true when the source is connected to node 1.

The term $\frac{Z_{02}(s)}{Z_{12}(s) + Z_{02}(s)}$ is a constant, depending on the layout of the circuit, we call this ratio $\mathcal{R}_{1\rightarrow 2}(s)$, the arrow indicates that we are going from node 1 to node 2. So in a formula

$$\mathcal{R}_{1\rightarrow 2}(s) = \frac{Z_{02}(s)}{Z_{12}(s) + Z_{02}(s)} \quad (D.4)$$

$$\mathcal{R}_{1\rightarrow 2}(s) = 1 - \frac{Z_{12}(s)}{Z_{12}(s) + Z_{02}(s)} \quad (D.5)$$

In words $\mathcal{R}_{1\rightarrow 2}(s)$ means: if we know the potential on node 1 and we want to know the potential on node 2 due to the potential on node 1, we should multiply it by $\mathcal{R}_{1\rightarrow 2}(s)$, in a formula

$$V_2(s) = V_1(s) \mathcal{R}_{1\rightarrow 2}(s) \quad (D.6)$$

Because the potential on node 2 is now known, we can calculate other potentials in the circuit with the help of that potential. With the help of the potential on node 2 it is easy to calculate the potential on node 3 in the same way as was done in the beginning of this section. Using equation D.3

$$V_3(s) = V_2(s) \mathcal{R}_{2\rightarrow 3}(s) \quad (D.7)$$

$$V_3(s) = V_1(s) \mathcal{R}_{1\rightarrow 2}(s) \mathcal{R}_{2\rightarrow 3}(s) \quad (D.8)$$

If we want to know the potential difference between node 1 and node 2 we need to multiply the potential $v_1$ by a factor $(1 - \mathcal{R}_{1\rightarrow 2}(s))$, a result which can easily be obtained using Kirchhoff’s voltage law

$$U_{12}(s) = V_1(s) - V_2(s) \quad (D.9)$$

$$U_{12}(s) = V_1(s) - V_1(s) \mathcal{R}_{1\rightarrow 2}(s) \quad (D.10)$$

From the calculations above we can conclude that for a linear circuit for each source separately we can:

- (equation D.6) convert a potential (due to an independent source) from node 1 to node 2 by multiplying this voltage by $\mathcal{R}_{1\rightarrow 2}(s)$. 
(equation D.8) split up the impedance in smaller parts and write

\[ R_{1 \rightarrow k}(s) = R_{1 \rightarrow 2}(s)R_{2 \rightarrow 3}(s) \ldots R_{k-1 \rightarrow k}(s) \]

(D.11)

• determine the ratio \( R_{a \rightarrow b}(s) \) by

\[ R_{a \rightarrow b}(s) = \frac{Z_{b0}(s)}{Z_{ab}(s) + Z_{b0}(s)} \]

(D.12)

with 0 a common node.

• (equation D.10) calculate the potential difference between two nodes, node 1 and node 2, due to a potential on node 1, by multiplying it by \( 1 - R_{1 \rightarrow 2}(s) \).

The need for this simplification tool becomes clear when we try to analyse large capacitive circuits. An example of this is shown in section 9.4 where a 3 junction circuit (also known as the electron pump) is analysed. In the next section we derive all the necessary values for this pump structure.

D.2 Determining the circuit constants; \( A(s) \), \( B(s) \), and \( R(s) \)

The smallest possible structure for a single-electron pump contains two gates and two islands. This two-island structure is drawn in figure D.3. Let \( C_{jx} \) be the capacitance of junction \( T_{jx} \). Let \( a \) be the number of the junction under investigation, and let \( k_g \) be the number of gates, let \( k_d \) be the number of bias voltage sources, and let \( k_{nf} \) be the number of islands. Let \( \alpha \), and \( \beta \) be constants depending on the topology of the rest of the circuit. For the voltage across junction \( a \) we can write in general, using superposition (see section 3.2.1)

\[ u_{j,a}(t) = \mathcal{L}^{-1} \left\{ \sum_{b=1}^{k_g} A_{b,a}^g(s)U_{g,b}(s) + \sum_{b=1}^{k_{nf}} B_{b,a}(s)Q_{i,b}(s) + \sum_{b=1}^{k_d} A_{b,a}^d(s)U_{d,b}(s) \right\} \]

(D.13)

Figure D.3: The circuit of an ideal two-island structure.
We simplified the structure shown in figure D.3 by introducing $C_{a\rightarrow b}$ (see figure D.4) which are equal to

\[
C_{1\rightarrow 2} = \frac{C_{12} (C_{2\rightarrow 5} + C_{2\rightarrow 3})}{C_{12} + (C_{2\rightarrow 5} + C_{2\rightarrow 3})} \tag{D.14}
\]

\[
C_{2\rightarrow 1} = C_{12} \tag{D.15}
\]

\[
C_{2\rightarrow 3} = \frac{C_{23} (C_{3\rightarrow 6} + C_{3\rightarrow 4})}{C_{23} + (C_{3\rightarrow 6} + C_{3\rightarrow 4})} \tag{D.16}
\]

\[
C_{3\rightarrow 2} = \frac{C_{23} (C_{2\rightarrow 5} + C_{2\rightarrow 1})}{C_{23} + (C_{2\rightarrow 5} + C_{2\rightarrow 1})} \tag{D.17}
\]

\[
C_{3\rightarrow 4} = C_{34} \tag{D.18}
\]

\[
C_{4\rightarrow 3} = \frac{C_{34} (C_{3\rightarrow 6} + C_{3\rightarrow 2})}{C_{34} + (C_{3\rightarrow 6} + C_{3\rightarrow 2})} \tag{D.19}
\]

\[
C_{5\rightarrow 2} = \frac{C_{25} (C_{2\rightarrow 1} + C_{2\rightarrow 3})}{C_{25} + (C_{2\rightarrow 1} + C_{2\rightarrow 3})} \tag{D.20}
\]

\[
C_{2\rightarrow 5} = C_{25} \tag{D.21}
\]

\[
C_{6\rightarrow 3} = \frac{C_{36} (C_{3\rightarrow 2} + C_{3\rightarrow 4})}{C_{36} + (C_{3\rightarrow 2} + C_{3\rightarrow 4})} \tag{D.22}
\]

\[
C_{3\rightarrow 6} = C_{36} \tag{D.23}
\]

---

Figure D.4: The basic circuit of a three junction electron pump structure.
With the help of equation D.10 we can write

\[ R_{1 \rightarrow 2}(s) = 1 - \frac{C_{1 \rightarrow 2}}{C_{12}} \]  
\[ R_{2 \rightarrow 1}(s) = 1 - \frac{C_{2 \rightarrow 1}}{C_{12}} = 0 \]  
\[ R_{2 \rightarrow 3}(s) = 1 - \frac{C_{2 \rightarrow 3}}{C_{23}} \]  
\[ R_{3 \rightarrow 2}(s) = 1 - \frac{C_{3 \rightarrow 2}}{C_{23}} \]  
\[ R_{3 \rightarrow 4}(s) = 1 - \frac{C_{3 \rightarrow 4}}{C_{34}} = 0 \]  
\[ R_{4 \rightarrow 3}(s) = 1 - \frac{C_{4 \rightarrow 3}}{C_{34}} \]  
\[ R_{2 \rightarrow 5}(s) = 1 - \frac{C_{2 \rightarrow 5}}{C_{25}} = 0 \]  
\[ R_{5 \rightarrow 2}(s) = 1 - \frac{C_{5 \rightarrow 2}}{C_{25}} \]  
\[ R_{3 \rightarrow 6}(s) = 1 - \frac{C_{3 \rightarrow 6}}{C_{36}} = 0 \]  
\[ R_{6 \rightarrow 3}(s) = 1 - \frac{C_{6 \rightarrow 3}}{C_{36}} \]  

(D.24)  
(D.25)  
(D.26)  
(D.27)  
(D.28)  
(D.29)  
(D.30)  
(D.31)  
(D.32)  
(D.33)

For the admitances \( Y_a \) between node \( a \) and the common node (ground) we can write

\[ Y_1(s) = (C_{2 \rightarrow 1} + C_{2 \rightarrow 3} + C_{2 \rightarrow 5}) \]  
\[ Y_2(s) = (C_{3 \rightarrow 2} + C_{3 \rightarrow 4} + C_{3 \rightarrow 6}) \]  
\[ Y_3(s) = \infty \]  
\[ Y_4(s) = \infty \]  
\[ Y_5(s) = \infty \]  
\[ Y_6(s) = \infty \]  

(D.34)  
(D.35)  
(D.36)  
(D.37)  
(D.38)  
(D.39)

Not all these values are needed to do the calculation, but they are given here for completeness.
D.3 Calculating the border of the triple area

Formula D.13 can now be written for the three junctions of figure D.4. So for the first junction we can write

\[
    u_{j,1}(t) = \mathcal{L}^{-1} \left\{ \sum_{b=1}^{2} A_{d,1}^d(s) U_{d,b}(s) + \sum_{b=1}^{2} A_{g,1}^g(s) U_{g,b}(s) + \sum_{b=1}^{2} B_{b,1}(s) Q_{qi,b}(s) \right\}
\]

\[
    A_{d,1}^d(s) = + (1 - R_{1 \rightarrow 2})(s) \tag{D.40}
\]

\[
    A_{d,1}^g(s) = - R_{4 \rightarrow 3}(s) R_{3 \rightarrow 2}(s) (1 - R_{2 \rightarrow 1}(s)) \tag{D.41}
\]

\[
    A_{g,1}^g(s) = - R_{5 \rightarrow 2}(s) (1 - R_{2 \rightarrow 1}(s)) \tag{D.42}
\]

\[
    A_{d,1}^g(s) = - R_{2 \rightarrow 1}(s) (1 - R_{2 \rightarrow 1}(s)) \tag{D.43}
\]

\[
    A_{d,1}^g(s) = - R_{6 \rightarrow 3}(s) R_{3 \rightarrow 2}(s) (1 - R_{2 \rightarrow 1}(s)) \tag{D.44}
\]

\[
    B_{1,1}(s) = - Z_2(s) (1 - R_{2 \rightarrow 1}(s)) \tag{D.45}
\]

\[
    B_{2,1}(s) = - Z_3(s) R_{3 \rightarrow 2}(s) (1 - R_{2 \rightarrow 1}(s)) \tag{D.46}
\]

For the second junction we can write

\[
    u_{j,2}(t) = \mathcal{L}^{-1} \left\{ \sum_{b=1}^{2} A_{d,2}^d(s) U_{d,b}(s) + \sum_{b=1}^{2} A_{g,2}^g(s) U_{g,b}(s) + \sum_{b=1}^{2} B_{b,2}(s) Q_{qi,b}(s) \right\}
\]

\[
    A_{1,2}^d(s) = + R_{1 \rightarrow 2}(s) (1 - R_{2 \rightarrow 3}(s)) \tag{D.47}
\]

\[
    A_{d,2}(s) = - R_{4 \rightarrow 3}(s) (1 - R_{3 \rightarrow 2}(s)) \tag{D.48}
\]

\[
    A_{g,2}^g(s) = + R_{5 \rightarrow 2}(s) (1 - R_{2 \rightarrow 3}(s)) \tag{D.49}
\]

\[
    A_{g,2}^g(s) = - R_{6 \rightarrow 3}(s) (1 - R_{3 \rightarrow 2}(s)) \tag{D.50}
\]

\[
    B_{1,2}(s) = + Z_2(s) (1 - R_{2 \rightarrow 3}(s)) \tag{D.51}
\]

\[
    B_{2,2}(s) = - Z_3(s) (1 - R_{3 \rightarrow 2}(s)) \tag{D.52}
\]

And for the third junction

\[
    u_{j,3}(t) = \mathcal{L}^{-1} \left\{ \sum_{b=1}^{2} A_{d,3}^d(s) U_{d,b}(s) + \sum_{b=1}^{2} A_{g,3}^g(s) U_{g,b}(s) + \sum_{b=1}^{2} B_{b,3}(s) Q_{qi,b}(s) \right\}
\]

\[
    A_{1,3}(s) = + R_{1 \rightarrow 2}(s) R_{2 \rightarrow 3}(s) (1 - R_{3 \rightarrow 4}(s)) \tag{D.53}
\]

\[
    A_{d,3}(s) = - (1 - R_{4 \rightarrow 3}(s)) \tag{D.54}
\]

\[
    A_{g,3}(s) = + R_{5 \rightarrow 2}(s) R_{2 \rightarrow 3}(s) (1 - R_{3 \rightarrow 4}(s)) \tag{D.55}
\]

\[
    A_{g,3}^g(s) = + R_{6 \rightarrow 3}(s) (1 - R_{3 \rightarrow 4}(s)) \tag{D.56}
\]

\[
    B_{1,3}(s) = + Z_2(s) R_{2 \rightarrow 3}(s) (1 - R_{3 \rightarrow 4}(s)) \tag{D.57}
\]

\[
    B_{1,3}(s) = + Z_3(s) (1 - R_{3 \rightarrow 4}(s)) \tag{D.58}
\]

D.3 Calculating the border of the triple area

Due to non-zero bias voltages \(u_{d1}\) and \(u_{d2}\) the borders of the Coulomb blockade (the stable regions, which are needed for a correct functioning of the electron pump)
changes. The region of the triple area becomes larger, as was discussed in section 9.4. To determine the shifts of the borders of these stable region we can again use equation D.13.

Let \( \Delta u_{j,a} \) be the change in junction voltage of junction \( a \) due to both bias sources, so

\[
\begin{align*}
\Delta U_{j,1}(s) &= A_{1,1}^d(s)U_{d,1}(s) + A_{2,1}^d(s)U_{d,2}(s) \\
\Delta U_{j,2}(s) &= A_{1,2}^d(s)U_{d,1}(s) + A_{2,2}^d(s)U_{d,2}(s) \\
\Delta U_{j,3}(s) &= A_{1,3}^d(s)U_{d,1}(s) + A_{2,3}^d(s)U_{d,2}(s)
\end{align*}
\]  

(D.61)  
(D.62)  
(D.63)

To determine the shifts in horizontal direction and in the vertical direction appearing in the plot where \( u_{g,2} \) is shown as function of \( u_{g,1} \) (see figure D.5), this change in junction voltage should be expressed in gate voltage. Let \( \Delta u_{g_{x,a}} \) be the change of the Coulomb blockade expressed in gate voltage \( u_{g_{x}} \) of junction \( a \). Then we can write for the shifts, for line 1

\[
\begin{align*}
\Delta U_{g1,1}(s) &= \frac{\Delta U_{j,1}(s)}{A_{1,1}^q(s)} \\
\Delta U_{g2,1}(s) &= \frac{\Delta U_{j,1}(s)}{A_{2,1}^q(s)}
\end{align*}
\]  

(D.64)  
(D.65)

and for line 2

\[
\begin{align*}
\Delta U_{g1,2}(s) &= \frac{\Delta U_{j,2}(s)}{A_{1,2}^q(s)} \\
\Delta U_{g2,2}(s) &= \frac{\Delta U_{j,2}(s)}{A_{2,2}^q(s)}
\end{align*}
\]  

(D.66)  
(D.67)

and for line 3

\[
\begin{align*}
\Delta U_{g1,3}(s) &= \frac{\Delta U_{j,3}(s)}{A_{1,3}^q(s)} \\
\Delta U_{g2,3}(s) &= \frac{\Delta U_{j,3}(s)}{A_{2,3}^q(s)}
\end{align*}
\]  

(D.68)  
(D.69)
Which gives

\[
\Delta U_{g1,1}(s) = \frac{A^d_{1,1}(s)U_{d,1}(s) + A^d_{2,1}(s)U_{d,2}(s)}{A^q_{1,1}(s)} \quad \text{(D.70)}
\]

\[
\Delta U_{g2,1}(s) = \frac{A^d_{1,1}(s)U_{d,1}(s) + A^d_{2,1}(s)U_{d,2}(s)}{A^q_{2,1}(s)} \quad \text{(D.71)}
\]

\[
\Delta U_{g1,2}(s) = \frac{A^d_{1,2}(s)U_{d,1}(s) + A^d_{2,2}(s)U_{d,2}(s)}{A^q_{1,2}(s)} \quad \text{(D.72)}
\]

\[
\Delta U_{g2,2}(s) = \frac{A^d_{1,2}(s)U_{d,1}(s) + A^d_{2,2}(s)U_{d,2}(s)}{A^q_{2,2}(s)} \quad \text{(D.73)}
\]

\[
\Delta U_{g1,3}(s) = \frac{A^d_{1,3}(s)U_{d,1}(s) + A^d_{2,3}(s)U_{d,2}(s)}{A^q_{1,3}(s)} \quad \text{(D.74)}
\]

\[
\Delta U_{g2,3}(s) = \frac{A^d_{1,3}(s)U_{d,1}(s) + A^d_{2,3}(s)U_{d,2}(s)}{A^q_{2,3}(s)} \quad \text{(D.75)}
\]

Figure D.5: The amount of change in gate voltages due to applied bias sources. The interception point called triple point is enlarged into a triangular shaped triple region, called triple area.
A general method to derive the node voltages
Cross capacitances

Between each node in a circuit a capacitance is formed. The capacitance value is determined by the topology of the circuit (for example placing of the interconnects) and the materials used as insulators. We define cross capacitances as:

**Definition E.1** *Between two nodes a capacitor is formed due to the layout, when this capacitance is an undesired phenomena we call it a cross capacitance.*

The value of those cross capacitances is in general very low. In chip design with normal components and operating in the low frequency range, they will have a neglectable effect. Only when we scale down and the capacitances of the cross capacitors are not (or barely) scaled down they become a problem. In two fields the problem is even larger: nano-technology, and high frequency design.

In the SET design the cross capacitances make it harder to design a simple couple block (see section 8.2). The cross capacitances form an undesired coupling with other nodes [71]. This plays an important role in larger circuits. When many circuits are placed close to each other some sub-circuits will be capacitively coupled while this was not taken into account in the design. Due to the fact that even small capacitances have their influence, this can be one of the biggest problems in high density SET structures. A solution can be: using large distances between the components. In that way we will loose the advantages of nano-scale device, because a large part on chip can not be used.

The operating temperature is also effected by the cross capacitances. This temperature (see section 10.1.1) is determined by the capacitance values, and to get the temperature as high as possible (maybe even room temperature) we need very small capacitance values.

A way to overcome the problems introduced due to the cross capacitances is by designing circuits which have already capacitances or voltage sources across the cross capacitances. In that way those designed capacitances are just a bit higher in value. See for example the SET transistor of figure E.1.
Figure E.1: The cross capacitances \((C_{cr1}, C_{cr2},\) and \(C_{cr3}\)) of the voltage biased SET transistor will have no influence due to the low ohmic impedance of the voltage sources.

For a circuit with \(k_n\) nodes, \(k_a\) (two-pin) capacitances are formed in the circuit. \(k_a\) can be found using\(^1\)

\[
k_a = \binom{k_n}{2} = \frac{k_n!}{2(k_n - 2)!}
\]  \hspace{1cm} (E.1)

When there are \(k_j\) capacitances, which are designed to be there (like the junction capacitances, gate capacitor, etc.), the number of unwanted cross capacitances \(k_{cr}\) is reduced to

\[
k_{cr} = \binom{k_n}{2} - k_j = \frac{k_n!}{2(k_n - 2)!} - k_j
\]  \hspace{1cm} (E.2)

Also the number of ideal voltage sources \((k_u)\) will reduce this number with \(k_u\), as long as the sources are not in parallel with the desired capacitances.

In figure E.2 a few examples are shown of coupled capacitors and the cross capacitance that arise in those cases.

---

\(^1\) Capacitances in parallel are seen as one capacitance.
Figure E.2: Some coupled capacitors with their cross capacitances $C_{cr}$. a) A single capacitor (or junction) will have no cross capacitance. b) Two capacitors in series will have one cross capacitance. c) and d) three capacitors (so a four node network) will have three cross capacitances.
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"The saddest summary of a life contains three descriptions: could have, might have, and should have."
Louis E. Boone

Summary

Summary belonging to the thesis:
Circuit Design with Metallic Single-Electron Tunnel Junctions
Roelof H. Klunder

The goal of this thesis was to set up a circuit theory for the Single-Electron Tunnel (SET) junction. To design circuits based on these SET junctions a model has been presented to describe this tunnel behaviour. The accent of the model is on the phenomena of tunneling of single electrons, which differs from the models discussed in the literature that treat tunnel currents.

In this thesis we presented the following three main subjects

1. Modelling of SET junctions and independent island charges
2. Methods to design SET circuits
3. Examples and measurements

Modelling of SET junctions and island charges

In chapter 2 we gave an overview of the limitations of the existing models described in the literature. The limitations are due to the fact that there is no energy conservation in these models, the tunnel effect itself is not modelled, and the models consist of a so-called tunnel resistor in parallel with the junction capacitance. Due to this these models can only be used to model currents and they predict a too low value for the maximal speed of SET junctions (as a result of the RC times as a consequence of the tunnel resistor in the model). Also the independent island charge is not modelled in the literature. When an independent island charge is not modelled as a separate source, the circuit will be non-linear; hence no superposition can be used.

In chapter 3 we proposed models to solve the problems mentioned above. In these models a SET junction is seen as a normal linear capacitance with a current source parallel to it, which moves the charge of one electron from one side of the junction to the other when the tunnel condition is satisfied. We also derived this tunnel condition, which is based on two phenomena, both are identical to the ones used in the already existing theories: 1) an electron tunnels in one part, so there is a
discrete charge transfer. 2) The electron tunnels only when the energy of the system is lowered due to the tunnel event. With the help of this energy tunnel condition a tunnel condition based on local voltages across the junction itself can be derived. This voltage condition is based on voltages at two different moments in time: just before the tunnel event takes place, and just after the event.

The second model which is discussed in chapter 3 is the model for the independent island charges. Independent island charges arise due to tunneling of electrons, initial charges and random fluctuating background charges. This models is composed of a current source to let those charge shifts take place.

When we derived the tunnel condition we assumed that the tunneling goes infinitely fast. When we use this assumption it is impossible to explain the difference in behaviour due to a difference in impedance of the environment of the SET junction. In chapter 4 we introduce a tunnel time, the time needed for the electron to go from one side of the junction to the other side, and we stick with the in chapter 3 found tunnel condition. With the combination of the tunnel time and the voltage based tunnel condition we are able to model resistors in SET circuits. For the two extremes, a zero series impedance and an infinite series impedance, this method gives the same result for the value of the Coulomb blockade as the existing theories.

In chapter 4 we also simplified the tunnel condition. Instead of a tunnel condition based on two voltages (just before the tunnel event and just after the tunnel event) we derived a tunnel condition based on one voltage called the critical voltage, which forms the new tunnel condition. Due to the non-zero tunnel time, the shape of the tunnel current can play a role. In this chapter we have also discussed in which cases we were allowed to neglect this shape: when the environment of the tunnel junction is purely capacitive or very low ohmic. We end the chapter with some simple rules of thumb to neglect components that have no effect on the tunnel condition. All this is done to make the calculation of the critical voltage as simple as possible.

**Circuit design methods**

With the help of the model for the SET junction and for the independent island charge, discussed in part I, we are able to set up a circuit theory for SET junctions.

In chapter 5 we showed how to bias a SET structure to get a desired input-output relation. The discussed method is based on so-called “operating windows”. The operating window is placed across the part of the input-output relation that shows the desired behaviour, after which the bias condition can be derived (depending on the applied input signals). For digital applications such a method can also be used, with only a small modification: discrete operating windows are used. In this chapter we also showed how we could get voltage amplification with the help of single SET junctions. For amplification we need at least one island and one junction. Due to this demand we defined two types of basic blocks. Type 1: A basic block of which the output node is the island. And type 2: a basic block of which the output is coupled through a SET junction of a capacitor directly to the island. These two basic blocks are used throughout the rest of this thesis.

In chapter 6 we proved that the input-output relation will be periodic when the structure consists of at least one island and one junction. We prove that the period (expressed in input voltages) is always a direct function of the input capacitor $C_{in}$. 

By choosing the component values we are able to use this periodicity to implement modulo functions. In this chapter some examples were given of applications based on these modulo functions, like the EXOR function and a system concept based on the Chinese Remainders Theorem (CRT). For the correct functioning of these concepts it is needed that no random fluctuating background charges appear.

Because such random fluctuating background charges can appear in practical cases, we discuss some solutions in chapter 7. In this chapter we have given a few principles to either make the signal less sensitive to these fluctuations or to compensate for these fluctuations. Such a charge fluctuation can be seen as a slow process, so it suffices to use redundancy in the signal (when this signal is much faster than the charge fluctuations). The obtained output signal can be averaged, peaked (top detector), or fed to a block that decides which signals occurs most often. The disadvantage of this type of redundancy is the fact that it slows down the signal processing.

A different solution can be found in compensating for these charge fluctuations. Applying a synchronisation signal on fixed moments in time can simply do this. The used synchronisation signal has a known amplitude. When this signal is applied to the input of the circuit, we can measure the output and from the difference between the measured output and the expected output we can derive the amount of fluctuation in the charge.

Another solution is found after analysing the error obtained due to these fluctuating charges. This error is an error in phase between the input and the output signal. By designing a system in which such a phase fluctuation has almost no effect, or the effect can be compensated, we can deal with these charge fluctuations on a system level.

A big problem when designing large circuits is the coupling of all the designed basic blocks. In chapter 8 we discussed those factors that play a role when coupling building blocks which contain SET junctions. Not only is the tunnel condition directly dependent on the impedance connected to the junction, but also the fact that SET circuits are (almost) completely capacitive circuits plays a part in the coupling problems. As a result of the placement of the components on a single chip, capacitive coupling arises between all the components, due to which signals are fed back to other blocks. As a consequence the coupling between two (or more) basic blocks should be uni-directional: the electron (or parts of the charge transfer) should only be influenced by the applied input signals, and not by the parasitic feedback signals. To be able to implement this we proposed a coupling circuit, which is not reciprocal, hence this coupling circuit behaves differently for signals applied to its input than to its output.

Examples and measurements

To demonstrate the possibilities of the circuit design tools of part II, in part III of this thesis we discussed some examples and two circuits, which were also measured.

In chapter 9 we gave a large number of circuit examples. Many of these examples are implementations of well known functions, like the adder, digital building blocks like the NAND, NOR and the inverter, and also an analog to digital converter, build with an electron-box (which is just one junction combined with a number of normal
capacitors). All these are mentioned to show the possibilities of the principle of the operating windows.

In chapter 9 we discussed two circuits that are not chosen on their functionality, but on the fact that it is possible to fabricate these device and that we can measure them. These two circuits are the SET transistor and the electron pump, which we analysed with the help of the models discussed in part I.

In chapter 10 we discussed the demands on the measurement equipment. A few examples of the demands are: measurement equipment should not give a too high voltage because of the low breakthrough voltage of the thin layer of oxide within the SET junction, and the equipment should also not contain too much noise, because of the small signals which we are trying to measure. The extremely low temperature needed for the measurements was also a point of attention. The contribution of the thermal energy should be negligible, so the temperature during the measurements should be kept low enough. We showed that the temperature could increase when the devices are made smaller. We also showed the measurement results of both type of measured circuits (the SET transistor and the electron pump) and compared them to the predicted behaviour discussed in chapter 9.
Samenvatting

Samenvatting behorende bij het proefschrift:
Circuit Design met Metalen Enkel-Elektron Tunnel Juncties

Roelof H. Klunder

Het doel van dit proefschrift is het opzetten van een circuittheorie voor de Enkel-Elektron Tunnel (SET) junctie. Om circuits te ontwerpen die gebaseerd zijn op deze SET juncties is een model gepresenteerd die het tunnelgedrag beschrijft. Het zwaartepunt van het model ligt op het gedrag van het tunnelen van een enkel elektron, hierin verschilt ons model van de modellen beschreven in de literatuur die op tunnel stromen zijn gebaseerd.

In dit proefschrift presenteren we drie onderwerpen

1. Modelering van de SET junctie en onafhankelijke eiland ladingen
2. Ontwerpmethodes voor SET circuits
3. Voorbeelden en metingen van SET circuits

Modelering van SET juncties en eiland ladingen

In hoofdstuk 2 hebben we een overzicht gegeven van de beperkingen van de in de literatuur beschreven modellen. Deze beperkingen zijn het gevolg van het feit dat: deze modellen niet uitgaan van energiebehoud, dat het tunneleffect zelf niet is gemoduleerd en dat het model een zogeheten tunnelweerstand bevat, die parallel staat over de tunnelcapaciteit. Hierdoor kunnen deze modellen alleen worden gebruikt voor stromen en voorspellen ze een te lage maximale snelheid (deze is het gevolg van de RC-tijden die ontstaan door de tunnelweerstand in het model). Ook de onafhankelijke eilandlading wordt niet gemoduleerd in de literatuur. Het circuit zal niet-lineair zijn als de onafhankelijke eilandlading niet wordt gemoduleerd als een aparte bron, waardoor superpositie niet kan worden gebruikt.

In hoofdstuk 3 hebben we modellen gepresenteerd om bovengenoemde problemen op te lossen. In deze modellen wordt een SET-junctie gemonoduleerd als een normale lineaire capaciteit met een stroombron parallel. Deze stroombron verplaatst een lading gelijk aan die van een elektron van de ene kant van de junctie naar de andere kant als
aan de tunnelconditie is voldaan. We hebben ook de tunnelconditie afgeleid, gebaseerd op twee verschijnselen, beide gelijk aan die gebruikt in de bestaande theorie. 1) Een elektron tunnelt in zijn geheel, dus er is een discrete ladingsverplaatsing. 2) Het elektron tunnelt alleen als de energie van het systeem hierdoor wordt verlaagd. Met behulp van deze energie tunnelconditie, hebben wij een tunnelconditie afgeleid die is gebaseerd op lokale spanningen over de junction zelf. Deze spanningsconditie is gebaseerd op spanningen op twee momenten in de tijd: net voordat een elektron tunnelt en net erna.

Het tweede model, wat we in hoofdstuk 3 hebben beschreven is het model voor de onafhankelijke eilandlading. Onafhankelijke eilandladingen verschijnen door: het tunnelen van elektronen, initiële ladingen en willekeurig fluctuerende achtergrondladingen. Het model om deze ladingsverplaatsing plaats te laten vinden bestaat uit een stroombron.

Bij de afleiding van de tunnelconditie namen we aan dat het tunnelen oneindig snel gaat. Door deze aannames is het onmogelijk geworden om de invloed van de omgeving op het gedrag van de SET junction te verklaren. In hoofdstuk 4 introduceren we een tunnel-tijd. Dit is de tijd die een elektron nodig heeft om van de ene kant naar de andere kant van de junction te tunnelen. Door het combineren van de tunnel-tijd en de gevonden spanningstunnelconditie zijn we in staat om weerstanden in SET circuits te modelleren. Voor de twee extreme situaties, een nul Ohm serie-impedantie en een oneindig hoge serie-impedantie, geeft deze methode hetzelfde resultaat voor de Coulomb blockade als de bestaande theorie.

In hoofdstuk 4 hebben we de tunnelconditie vereenvoudigd. In plaats van een tunnelconditie gebaseerd op twee spanningen (net voor het tunnelen en net erna) hebben we een tunnelconditie gebaseerd op één spanning afgeleid, namelijk de kritische spanning. Door de tunnel-tijd ongelijk aan nul speelt de vorm van de tunnelstroom een rol. In dit hoofdstuk beschreven we ook in welke situaties het toegestaan is deze vorm te verwaarlozen, namelijk wanneer de omgeving van de junction puur capacitief is of zeer laag-Ohmig. We eindigen dit hoofdstuk met enkele simpele vuistregels om de componenten die geen effect hebben op de tunnelconditie te verwaarlozen. Dit wordt gedaan om het berekenen van de kritische spanning zo eenvoudig mogelijk te maken.

Ontwerpmethodes voor SET circuits

Met behulp van het model voor de SET junction en voor de onafhankelijke eilandlading, beide beschreven in deel I, zijn we in staat een circuit theorie voor SET junctions op te stellen.

In hoofdstuk 5 hebben we aangetoond hoe we een SET structuur moeten instellen om de gewenste relatie tussen de ingang en de uitgang te krijgen. De beschreven methode is gebaseerd op zogeheten “operating windows”. Een dergelijke operating window wordt geplaatst op dat deel van de relatie tussen de ingang en de uitgang die het gewenste gedrag vertoont. Hieruit volgt de instelling die afhankelijk is van de aangeboden ingangssignalen. Met een kleine wijziging kan deze methode ook worden gebruikt voor digitale toepassingen, namelijk door het gebruik van discrete operating windows. In dit hoofdstuk hebben we ook aangetoond hoe we spanningsversterking kunnen krijgen met behulp van SET junctions. Voor een dergelijke versterking hebben we minstens één eiland en één junction nodig. Door deze eis kunnen we twee typen
basisblokken definiëren. Type 1: een basisblok waarvan de uitgang het eiland is. Type 2: een basisblok waarvan de uitgang aan het eiland gekoppeld is door middel van een capaciteit of SET junctie. Beide basisblokken worden in de rest van het proefschrift gebruikt.

In hoofdstuk 6 hebben we bewezen dat de relatie tussen de ingang en de uitgang periodiek zal zijn wanneer de structuur uit minstens één eiland en één junctie bestaat. We hebben bewezen dat de periode, uitgedrukt in ingangsspanningen, altijd een functie is van de ingangscapaciteit. Door het kiezen van deze componentwaarde zijn we in staat met behulp van de periodiciteit modulofuncties te implementeren. In dit hoofdstuk gaven wij enkele voorbeelden van toepassingen van modulofuncties, zoals een EXOR functie en een systeemconcept gebaseerd op de Chinese resttheorie (CRT). Voor de correcte werking van deze concepten is het noodzakelijk dat er geen willekeurig optredende achtergrondladingen voorkomen.

Omdat zulke achtergrondladingen in de praktijk altijd voorkomen beschrijven we in hoofdstuk 7 enkele mogelijke oplossingen. In dit hoofdstuk geven we enkele principes die of het signaal minder gevoelig maken voor deze veranderingen, of in staat zijn hiervoor te compenseren. De ladingsfluctuaties kunnen worden gezien als een langzaam verschijnsel, zodat het voldoende is om redundantie in het signaal te gebruiken (wanneer dit signaal veel sneller is dan de ladingsfluctuaties). Het verkregen uitgangssignaal kan worden gemiddeld, er kan piek-detectie worden gebruikt of er kan worden gekeken welk signaal het meest voorkomt. Het nadeel van deze methodes is dat ze langzaam zijn.

Een andere oplossing kan worden gevonden in het compenseren van ladingsfluctuaties. Dit kan worden bereikt door het aanbieden van een synchronisatie signaal op vaste momenten in tijd. Het gebruikte synchronisatie signaal moet een bekende amplitude hebben. Wanneer dit signaal door een circuit wordt gestuurd, kunnen we het uitgangssignaal meten en aan de hand van het gemeten en het verwachte signaal het verschil ten gevolge van de ladingsfluctuaties bepalen.

Nog een andere oplossing is het analyseren van de fout ten gevolge van deze ladingsfluctuaties. De gevonden waarde is een maat voor de fout in fase tussen het ingangs- en het uitgangssignaal. Door een systeem te ontwerpen waarin deze fasefouten geen of vrijwel geen effect hebben of waarvan het effect kan worden gecompenseerd kunnen we met deze fasefouten op een systeemniveau omgaan.

Een belangrijk probleem bij het ontwerpen van grote circuits is de koppeling tussen de diverse ontworpen bouwblokken. In hoofdstuk 8 hebben wij de factoren beschreven die een rol spelen in het koppelen van bouwblokken die SET juncties bevatten. De koppelproblemen worden veroorzaakt door het feit dat de tunnelconditie direct afhankelijk is van de impedantie gezien door de junctie, en door het feit dat SET circuits vrijwel geheel capacitief zijn. Als gevolg van de plaatsing van de componenten op een enkele chip ontstaat er capacitatieve koppeling tussen alle componenten. Hierdoor worden ongewenst signalen tussen diverse blokken teruggekoppeld. De koppeling tussen twee of meer basisblokken moet uitsluitend in één richting plaatsvinden. Het elektron of delen van een ladingsverplaatsing mag alleen worden beïnvloed door de ingangssignalen en niet door de parasitaire teruggekoppelde signalen. Om dit te implementeren hebben we een koppelcircuit ontworpen. Deze is niet reciproc en gedraagt zich dus verschillend voor de signalen die worden aangeboden aan de ingang en de signalen die worden aangeboden aan de uitgang.
Voorbeelden en metingen van SET circuits

Om de mogelijkheden van de ontwerpmethodes uit deel II aan te tonen worden in deel III van dit proefschrift enkele voorbeelden beschreven. Twee van deze voorbeeld circuits zijn ook daadwerkelijk gemeten.

In hoofdstuk 9 hebben we een groot aantal voorbeeld-circuits beschreven. Veel van deze circuits zijn implementaties van bekende functies, zoals de opteller, digitale bouwblokken zoals de NAND, NOR en de inverter en ook een analoog naar digitaal-omzetter. Allen gebouwd met een zogeheten elektronbox, welke bestaat uit één junctie en een aantal capaciteiten. Deze voorbeelden worden beschreven om de mogelijkheden van de operating window aan te tonen.

In hoofdstuk 9 hebben we tevens twee circuits beschreven die niet zijn gekozen vanwege hun functionaliteit, maar vanwege het feit dat het mogelijk is met de huidige technieken deze circuits te fabriceren en te meten. Deze twee circuits zijn de SET transistor en de elektronenpomp. Beide zijn geanalyseerd met behulp van de modellen uit deel I.

In hoofdstuk 10 beschreven we de eisen aan de meetapparatuur. Een paar voorbeelden van de eisen zijn: de meetapparatuur mag geen hoge spanning afgeven, vanwege de lage doorslagspanning van de dunne oxide-laag van de SET junctie, de apparatuur mag ook niet teveel ruis, vanwege de kleine signalen die we proberen te meten. De bijdrage van de thermische energie moet verwaarloosbaar zijn, waardoor de temperatuur tijdens de metingen extreem laag moet worden gehouden. We tonen aan dat deze temperatuur mag toenemen voor componenten met kleinere afmetingen. Tevens presenteren wij de meetresultaten van beide circuits (de SET transistor en de elektronenpomp) en vergelijken we deze met het voorgestelde gedrag beschreven in hoofdstuk 9.
Dankwoord

Mijn promotie werk had ik niet alleen uit kunnen voeren. De vele mensen die mij inhoudelijk of ondersteunend geholpen hebben wil ik hiervoor bedanken. Hieronder wil ik enkele van hen persoonlijk bedanken. Ik zal ze niet in volgorde van belangrijkheid noemen, maar ingedeeld in een aantal groepen. Als eerste wil ik mijn promotor Professor Dewilde bedanken voor zijn bijdrage aan het tot stand komen van dit proefschrift.

Nano elektronica

Binnen de vakgroep elektronica startte mijn eerste professor Arthur van Roermund een nano-neurale elektronica groep, waar ik deel van uit maakte. Ik wil Arthur van Roermund dan ook bedanken voor het bieden van een afstudeer plek wat later uitgegroeide tot een promotie plaats in de nano elektronica.

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Roelof Klunder is born in Delft on April 17th in 1972. He started his technical career at Polytechnical school of electrical engineering at the Rijnmond MTS in Schiedam in 1988, with specialisation in electronics, which he finished (cum laude) in 1992.

He still wanted to learn more about electronics then the basic rules he was learned, so he started the same year the vocational training at university level for electrical engineering at the TH Rijswijk, with specialisation telecommunication. He finished this education (again cum laude) in 1996.

Still not satisfied he went on to study at the university. There he did his Master of Science study for electrical engineering, which he finished (also cum laude) in 1998. His master thesis was on the field of nano-electronics and got the Dutch title: "Een regelbare single elektron tunneling transistor".

In this way he came in contact with the nano-electronics and decided to go for his PhD at the electronics research laboratory, Delft University of Technology, which he started in October 1998, and finished in October 2002.
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