DELFT UNIVERSITY OF TECHNOLOGY

A Low Power 10-bit SAR ADC in a 45nm CMOS process

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Abstract

In this work a low power SAR ADC with 8.9 ENOB for wireless communication systems is presented. A capacitive charge redistribution DAC with a unit capacitor of 0.5fF is used. The implemented charge-sharing technique, allows the use of $2^{N-1}+1$ unit capacitors, instead of the conventional 2^N, thus decreasing the DAC area and the DAC switching power by a factor of 2. An asynchronous digital controller eliminates the need of an external high frequency clock. The test chip has been manufactured in a CMOS 45nm process. The measured power consumption is only $45\mu W$ at the sampling rate of 16MS/s. The total area of the ADC is only $0.01mm^2$. The achieved FoM of $5.9fJ/conv$ is comparable with state-of-the art.

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1

Introduction

An Analog-to-Digital converter (ADC) is one of the fundamental electronic components of the modern heavily digitized world. Its function is to map a continuous signal in time, i.e. with an infinite number of values, to a digital signal, consisting of a stream of binary codes, which can only take on two abstract values 'zero' or 'one', and is easily processed in the digital domain by microcontrollers and processors.

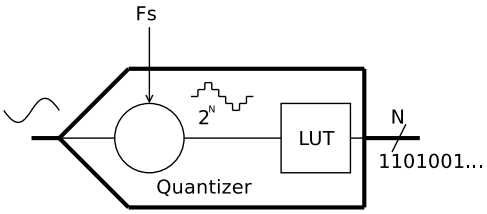


Fig. 1.1. ADC abstract representation

At a very abstract level, any ADC can be represented as a quantizer and a look-up table, as shown in Fig.1.1. In the quantizer, a continuous time input signal is translated to a finite set, whose elements can take values from 0 to $2^N - 1$, where N is the resolution of the ADC. This process is called quantization. Consequently, there are 2^N quantization levels in the amplitude domain. The look-up table links every quantization level to the corresponding binary representation and generates a digital code at the output.

The finite number of quantization levels gives rise to quantization error, which is the difference between the value of an actual signal and its quantized version (see Fig. 1.2). This fundamentally limits the Signal-to-Noise ratio (SNR) of Nyquist-rate ADCs. Unlike thermal noise, quantization error does not have a white noise spectrum and in general shows a quite non-linear behavior. However, if N=7 or more, it is possible to approximate the quantization error as white noise[2].

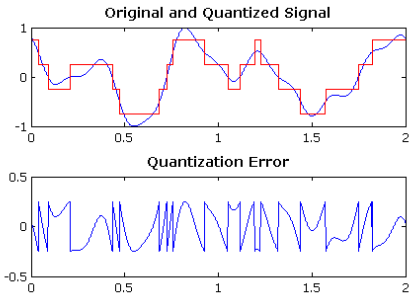


Fig. 1.2. Quantization error[1]

The sampling frequency Fs is another fundamental parameter that imposes limitations on the maximum frequency of the input signal. According to the sampling theorem [3], the quantized signal can be perfectly reconstructed from an infinite number of samples if the frequency of the input signal is less than $Fs/2$ and no other frequencies exist below it. $Fs/2$ is called the Nyquist frequency.

Different tasks require different ADC specifications. As an example, high resolution

and slow sampling rate are usually needed for sensor applications, whereas data links require high sampling rate and low resolution. Moreover, the full set of specifications such as INL/DNL, IM3, SFDR, power consumption, offset and others are often unique for every case. This thesis describes the design of a low-power ADC for wireless communication systems.

In this introductory chapter, a brief overview of the receiver, in which the ADC can be used, is given. This is followed by the goal and motivation of the thesis. The differences between design of the embedded and standalone ADCs will be examined. Finally, the structure of the thesis is presented.

1.1 The ADC application

A typical structure of a receiver is shown in Fig.1.3. A SAW filter is used to attenuate unwanted out-of-band signals, a low noise amplifier amplifies the input signal, which is later down-converted by a mixer. A filter after the mixer removes the high frequency mixing products. An IF amplifier boosts the input signal up to the full-scale ADC swing, maximizing the SNR at the output. Another function of the IF amplifier is to drive the ADC input. An anti-aliasing filter in front of the ADC provides additional attenuation of out-of-band unwanted signals. The demand for the low power and compact solutions leads to combining of digital and analog parts of the receiver on the same die and so, a submicron CMOS technology with the low supply voltages is often used.

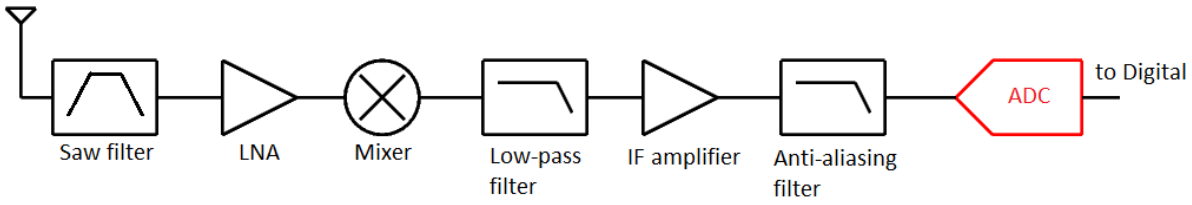


Fig. 1.3. Functional diagram of a receiver

1.2 Motivation and objectives

The ultra low power ADCs with moderate resolution and the speed of 0.1-20MHz are often required for the applications such as Bluetooth, IEEE 802.15.6 or ISM radios. The motivation of this work is the need for an easily-integrated, compact and low power A-to-D converter for the use in these applications. For this reason the following design steps have been followed:

- Choice of the ADC type
- Circuit and physical level implementation of the functional blocks and the ADC
- Design verification
- Prototype measurements

1.3 Standalone versus embedded design

Since embedded ADCs are manufactured on the same die with the other parts of a receiver, additional aspects of the ADC design associated with its embedded implementation should be considered. In comparison with stand-alone designs, new problems may arise, whereas others become less important or not important at all.

In a standalone implementation, the impedance of the external signal source can be quite large due to the interface with the real world via bond wires and the pins of a package. Bond wires, together with the parasitic capacitance of pads form unwanted LC-networks causing the ADC's input signal to 'bounce' when the sampling switch is turned on and off, thus degrading overall ADC performance. However, this problem does not occur in embedded ADCs since the input signal is generated by internal circuitry, providing a response much more similar to an ideal voltage source. The bounce on the supply rails is also much smaller for the embedded implementation because the use of internal LDOs is the common practice in SoC design.

Substrate noise may degrade performance in the embedded ADC due to the presence of various digital elements and high frequency interference from such blocks as VCOs and PLLs. Moreover, the LSB voltage of an embedded ADC is smaller than that of a standalone design, which makes the embedded ADC even more vulnerable to interference.

The technology used makes a difference as well. Normally, in standalone designs, BiCMOS processes with moderate length CMOS devices (0.35-0.6 um) and a high-beta BJTs are available, whereas in SoC design, deep sub-micron CMOS technology is often used with poor, or even, without BJTs. Good bipolar transistors simplify the design of reference circuits and provide better matching performance. The flicker noise of bipolar transistors is not as severe as in short-length CMOS devices. Also, for standalone ADCs, external voltage references are usually available, whereas for embedded ADCs this is not the case.

Since direct measurement of the ADC in a SoC is hardly possible, benefits of the digital environment around can be used. For example, data from a high-speed embedded ADC can be written to an internal buffer memory and then taken off chip using low frequency outputs.

Standalone ADCs are mostly counted as general purpose converters and so, their input bandwidth is designed as high as possible in order to give a user a freedom to choose any frequency to work at. Doing the same for the embedded ADC is a waste of power since the bandwidth and frequency of the input signal are always well known.

1.4 Organization of the thesis

The organization of this thesis repeats the steps which have been performed during the design and evaluation of the ADC, from defining the specification to measurements in the laboratory.

SAR and Sigma-delta ADCs are the main competitors for use in the receiver of a modern radio. Both choices have their own drawbacks and benefits. In chapter 2 a SAR ADC and a Sigma Delta ADC will be compared and the architectural choice will be made.

An overview of the binary search algorithm, implemented by a SAR ADC is described in chapter 3, as well as its general implementation. Several previous designs were considered and one was chosen as a starting point. The overall logic of the proposed ADC is described in this chapter.

Charge-sharing techniques can be used to decrease the area and power consumption of a SAR ADC. A new charge-sharing implementation is proposed in chapter 4. The ADC consists of three analog functional blocks: a DAC, a comparator, and a sampling switch. Each block affects the ADC performance and, therefore, the influence of every block should be considered separately. The accuracy of the capacitors in the DAC is estimated based on the available statistical data. The corresponding simulation results are shown. Non-idealities of the comparator are considered in this chapter, and the minimum requirements are defined. The total thermal noise of the ADC is calculated as well. Finally, the different implementations of a sampling switch are described and the most suitable solution is chosen.

Chapter 5 deals with the transistor-level implementation of the ADC blocks. The effect of the parasitics introduced by the actual layout is investigated as well.

Grounding and supply strategy is an important part of mixed-signal design and requires careful attention. Ground bounce and coupling between analog and digital lines can dramatically degrade the ADC performance. Chapter 6 discusses these problems.

Chapter 7 presents the PCB design for the test chip, measurement setup and achieved performance of the designed ADC. A comparison with state-of-the art is also made in this chapter. Finally, in chapter 8 the conclusions are drawn.

2

The ADC requirements

The purpose of this chapter is to make an architectural choice and to clearly define the specifications of the ADC.

About one or two decades ago, SAR and Sigma-Delta converters were considered as low frequency, high resolution converters. Sigma-delta converters had found their application in audio systems, where high resolution conversion for stereo sound was needed within the audio bandwidth 16-32000Hz. SAR ADCs were mainly used in low frequency control and measurement loops. However, technology scaling and the improvement of circuit techniques have made it feasible to broaden the application range of these converters. The higher achievable clock speed in deep-submicron processes improved the bandwidth and resolution of Sigma-Delta converters by boosting over-sampling ratio without increasing the order of a loop filter or the number of quantization levels of the quantizer. The accuracy of the capacitors and better switches improves the performance of Sigma-Delta converters as well, but the most remarkable impact is observed on SAR ADCs, allowing them to achieve good resolution with relatively small capacitors in the charge redistributing DAC. In turn, the smaller capacitors mean a higher input bandwidth and lower power consumption. Moreover, as for Sigma-Delta converters, higher clock speed also makes it possible to speed up the digital part of SAR ADCs.

Since a low power design is required, a more passive circuit design is preferable. 'Passive circuit design' means excluding transistors with fixed bias currents, or in other words, without amplifiers. This is possible for SAR ADCs, but not for Sigma-Delta ADCs, in which active integrators is inevitable. Moreover, low power amplifiers may introduce additional non-linearity. Another problem associated with Sigma-Delta converters is that, a higher frequency sampling clock is needed for the same conversion rate and so, larger clock buffers may be required, leading to additional power consumption. Mainly due to these reasons, a SAR ADC has been chosen.

The estimation of the ADC SNDR is based on many system parameters such as noise floor, the required system SNR, receiver sensitivity and the blocker requirements. The sampling frequency of the ADC is related to the IF frequency of a receiver. Importantly that increasing the sampling rate relaxes the requirements on the anti-aliasing filter and the ADC resolution. For example, increasing the sampling frequency by a factor of 4, gains an additional ADC's bit if the signal bandwidth remains the same.

Although the INL/DNL are considered as 'static' parameters of an ADC, they affect the dynamic performance as well. DNL creates the variations in the trip levels as the

input signal changes. This variation resembles random behavior and increases the ADC's noise floor. If a full-swing sine wave at the ADC input is assumed, the SNR due to the quantization error with finite DNL can be approximated as[2]:

$$SNR_{Q+DNL} = 6.02N - 9.03 - 10log\Big(\frac{1}{12} + \frac{DNL^2}{2n^2}\Big) \tag{2.1}$$

where n=3..4.
For example, with n=3 and DNL=1LSB, the SNR degradation is 2.2dB.

Since the INL represents the ADC transfer curve, any nonlinear deviation from the straight line causes harmonic distortion and limits the SFDR of an ADC. The rule of thumb is [4]

$$SFDR = 20log\Big(\frac{2^N}{INL}\Big) \tag{2.2}$$

For instance, a 10-bit ADC with INL=1LSB has SFDR=60dB.

The ADC will be manufactured in a 45nm CMOS process with the nominal supply voltage of 0.9V. However, low drop-out regulators are usually used in SoCs to provide a 'clean' supply voltage for data converters. Consequently, the ADC has to work with supply voltages as low as 0.8V.

It is convenient to use a figure-of-merit (FoM) to characterize the performance of an ADC. Usually, the FoM definition described in [5] is used:

$$FoM = \frac{Power}{SamplingFrequency \times 2^{ENOB}} \tag{2.3}$$

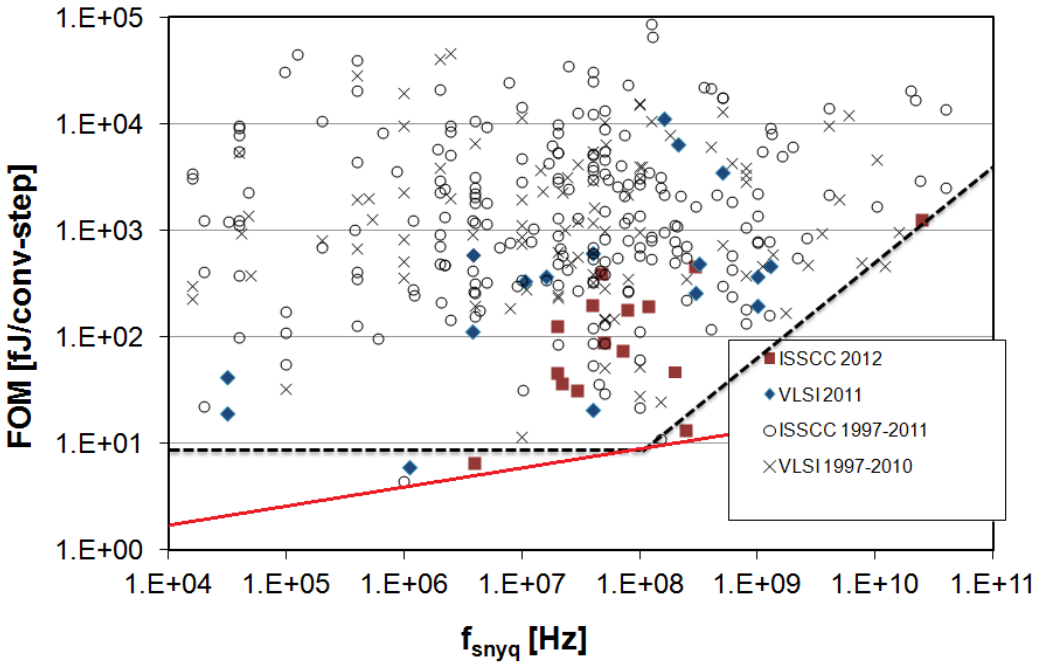


Fig. 2.1. State-of-the art ADCs [6]

The FoM versus sampling frequency of state-of-the art ADCs is shown in Fig. 2.1. The minimum targeting requirements for the ADC has been set in order to achieve the performance resulting in the point below the red line and are summarized in table 2.1.

Parameter	**Value**	**Units**
Resolution	10	bits
Sampling rate	16	MS/s
Input frequency	8	MHz
INL/DNL	0.5/0.5	LSB
Supply voltage	0.8	V
Current consumption	50	μW

Table 2.1. ADC requirements

3

SAR ADC architecture

The operation of a conventional SAR ADC and a description of its building blocks will be provided in this chapter. Several examples of state-of-the art low power SAR ADCs will be analyzed and the most suitable one will be chosen as a reference design. The proposed ADC topology and corresponding time diagram will be qualitatively described.

3.1 SAR ADC operation

With the continuously scaled-down technology and decreasing supply voltage, design of active circuits becomes more challenging since headroom decreases, whereas the SNR and the linearity performance must remain at the same level or even better due to the, seemingly unstoppable, increasing complexity of on-chip systems. With the demand for less power consumption, so-called 'digital' implementation of analog circuits becomes preferable since it implies the absence of DC bias current in a circuit. In other words, amplifiers should be avoided as well as current and reference sources. SAR ADCs provide a very attractive possibility to exclude any DC bias currents since they consist only of a sample-and-hold, a comparator, a charge redistribution DAC, a shift register and some, not very sophisticated, control logic.

Typically, SAR ADCs implement a binary search algorithm. In a sorted array, binary search rapidly estimates the position number of a given element. The basic principle of the algorithm is to sequentially half the search range and then perform a comparison to determine in which halve the required element is located. When the appropriate half is determined, it is halved and the comparison takes place again. This procedure is repeated until the position of the element is found. As an example, the point F in Fig. 3.1 is the final element, which has been found in 6 guesses.

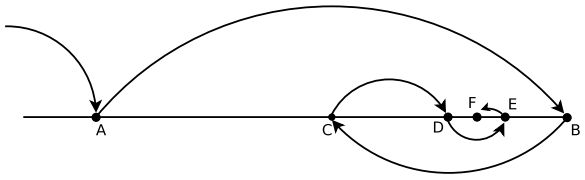


Fig. 3.1. Binary search algorithm

A great advantage of the binary search algorithm is that it can be easily implemented in hardware since only two mathematical, 'hardware friendly', operations are needed: a division by two, which is a 1-bit shift, and the comparison operation, which can be implemented using a high gain stage with or without positive feedback.

The main building blocks of a SAR ADC are shown in the generalized circuit of Fig.

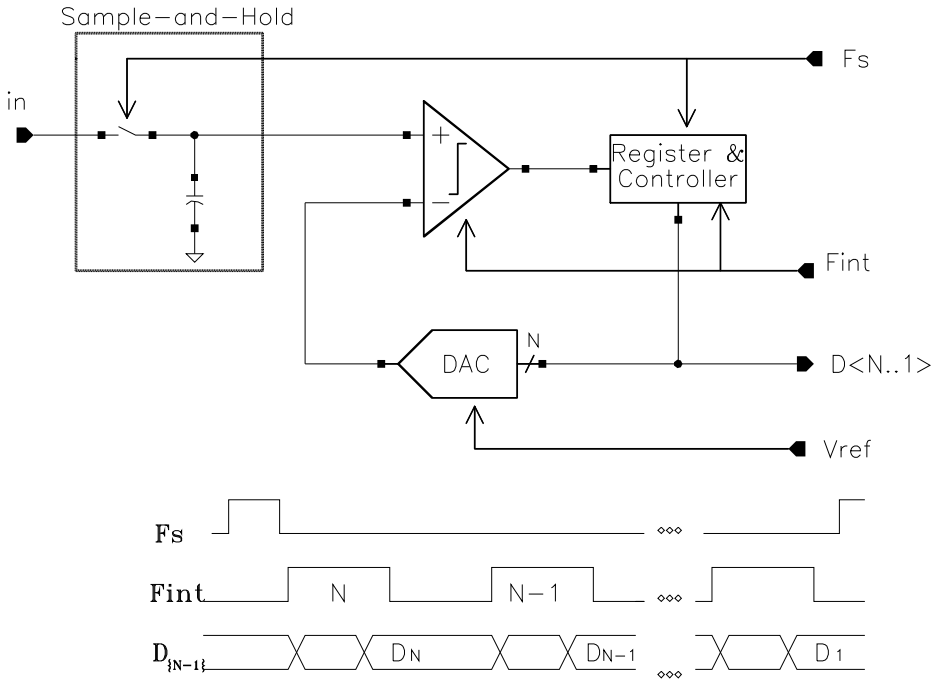


Fig. 3.2. A generalized circuit of a SAR ADC and corresponding time diagram

3.2. The sample-and-hold acquires the input voltage during the sampling phase and maintains a constant charge in the sampling capacitor during the conversion cycle. For a SAR ADC, the sample-and-hold circuit can be as simple as a switch and a capacitor, meaning that no amplifiers are needed. The comparator amplifies the difference between the inverting and non-inverting inputs to the extreme, i.e until the output hits the supply or ground rail, such that the output state can be interpreted as the digital 1 or 0. A large variety of comparators with very different performance are known. Among them are a number of fully dynamic comparators which do not require DC biasing [7, 8, 9]. The output of the comparator is connected to its inverting input through the digital register and the DAC, forming a negative feedback loop. As in any system with negative feedback, it tends to equilibrium, resulting in zero voltage difference between the positive and negative inputs of the comparator. The purpose of the register is to store intermediate data during a conversion cycle and to convert a serial stream of bits from the comparator into a parallel representation for the DAC. Any DAC with binary weighted coefficients can be used, such as R2R, current-steering or charge-redistributing DAC. To minimize total power consumption, a charge-redistributing DAC is used in this design.

The timing diagram of the circuit in Fig. 3.2 can be described as follows. The sampling signal 'Fs' enables the input switch and so the input voltage is applied across the sampling capacitor. After 'Fs' turns the sampling switch off, the input voltage is held on the sampling capacitor and the conversion process starts by initiating the 'Fint' clock with a frequency, approximately, N-times larger than the 'Fs' clock. Initially, 10 bits at the register output are set to 0 and, consequently, the voltage at the DAC output is 0V. With the first rising edge of 'Fint', the MSB of the register is set to 1, setting the DAC output to $V_{ref}/2$ and the first comparison takes place. If the voltage at the inverting

input is smaller than at the non-inverting, the MSB must be set to 1 since the sampled voltage (i.e. the input voltage) is larger than the half of the full-scale range. A larger voltage at the inverting input implies that the sampled voltage is smaller than half of the full-scale range and the MSB should be set back to 0. Then, data in the register is shifted right by 1 bit, the MSB-1 is set to 1, increasing voltage at the DAC output by $V_{ref}/4$ if MSB=1, or decreasing it by $V_{ref}/4$ if MSB=0, and the comparator makes a comparison again. The same actions will be performed until the last bit will be resolved.

3.2 SAR ADCs overview

Recently, a number of low power, low voltage SAR ADCs have been demonstrated with 8-10 bit resolution, sampling frequencies in the 1MHz range and sub-1mW power consumption [10, 11, 9, 12, 13, 14]. The common feature of these ADCs is that they employ an asynchronous digital controller. 'Asynchronous' means that an external high frequency clock is not needed and all required timing signals are generated inside of ADC. In this design, an asynchronous controller will be used as well. Some authors state that asynchronous logic decreases the overall power consumption of the ADC, however, the most important reason to use it in this design is the simplicity of integrating the ADC into a system since no high frequency clock driver and corresponding routing are needed.

A power consumption as low as $1.9\mu W$ for a 10-bit SAR ADC with a sampling frequency of $1MS/s$ and FoM=$4.4fJ/conv$ has been reported in [9]. Two techniques have been used to achieve this performance. To decrease the DAC switching power, intermediate switching steps have been introduced by using a stepwise charging of some capacitors in a charge-redistributing DAC [15], and a delay-line based SAR controller has been designed to minimize digital power consumption. The main idea behind the stepwise charging is to reuse the charge saved during a previous operation instead of drawing it from the power supply. The stepwise sharing for the MSB capacitor is shown in Fig. 3.3 and works as follows. When the left plate of the C_{MSB} capacitor must be discharged, the switches are enabled in the following sequence: 'B', 'C', and 'D' at the end, making the C_{MSB} capacitor discharge into C_{b1} and C_{b2}. When the left plate of the MSB capacitor has to be charged, the switches are enabled in the 'C', 'B', 'A' sequence, charging C_{MSB} from the big capacitors first and only then, from the supply source V_{ref}. Since during the charging of the MSB capacitor energy is taken from $C_{b1}$and C_{b2} instead of the supply source, the average power consumption decreases. The accuracy of the capacitors C_{b1} and C_{b1} is not important, but the values should be as large as possible. In [9], stepwise charging is implemented for the three most significant bits, thus considerably reducing the DAC switching power.

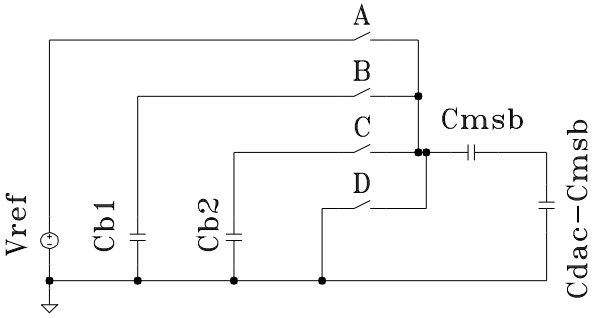


Fig. 3.3. Stepwise charging implementation with two intermediate step implementation from [9]

The drawback of this design is that the DAC's settling time limits the maximum

achievable speed of the ADC. Firstly, additional steps are required in the switching procedure. Secondly, additional time to charge and discharge C_{b1} and C_{b2} is needed. Taking into account that the reported sampling rate is only 1MS/s, achieving the desired 16MS/s is hardly possible with this architecture.

A 10-bit 50 MS/s SAR ADC with a FoM of $29fJ/conv$ has been reported in [12]. High speed and a relatively low current consumption of $680\mu A$ is achieved by a switching procedure in which the capacitors of a differential DAC are not switched differentially, i.e. depending on the comparator output, the voltage changes only at one side of the DAC. Thus, the voltage at the DAC output can be changed only in one direction. The flow diagram and the time-domain response are shown in Fig. 3.4. The obvious problem of this implementation is that the CM voltage at the comparator input changes, making the topology vulnerable to the dynamic offset of the comparator. This can cause very strong non-linearity and even missing codes in the ADC transfer function if the value becomes comparable with the LSB voltage.

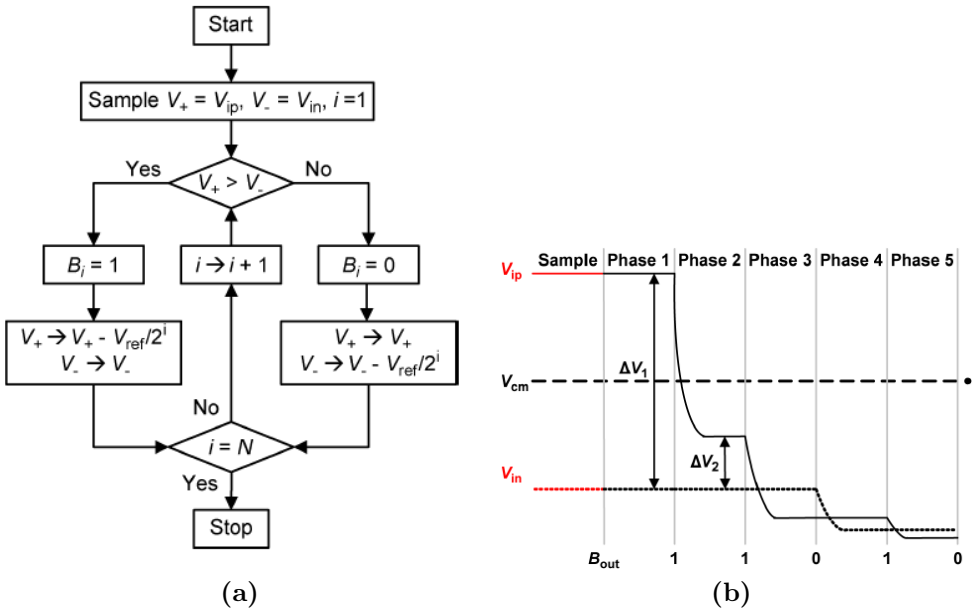


Fig. 3.4. Flow diagram (a), and the voltage at the DAC output (b)from [12]

Another interesting solution has been proposed in [11]. The key features of the design are the following. A very small unit capacitor with a value of $0.5fF$ is used, an asynchronous controller is implemented using custom-designed dynamic logic, minimizing the amount of transistors and reducing area. Moreover, a simple switching procedure makes it possible to use the supply voltage as the reference for the DAC. All of these features, make it feasible to achieve 8-bit resolution at a sampling frequency of 10 MS/s with a power consumption of $26.3\mu W$ from a 1V supply. The achieved FoM is $12fJ/conv$.

A simplified (5-bit) capacitor bank and the switching procedure of [11] are shown in Fig. 3.5 and can be described as follows. Initially, the sampling switch is closed and the input voltage is applied across the DAC's capacitors C1-C5 and C_h. The MSB is preset to 1 and the other DAC's bits to 0. At the moment the sampling switch is turning off, the input voltage is sampled on the DAC's capacitors and the conversion process is initiated. The comparator makes the first decision and determines the sign of the input voltage.

Based on this decision, the MSB of the DAC changes or keeps the same value, i.e. if $inputvoltage < Vref$, MSB keeps a preset value (1), but if $inputvoltage > Vref$, MSB changes to 0. Next, the MSB-1 flips and, consequently, the voltage at the DAC output changes. The second comparison takes place. If the voltage is higher than the reference level, the state of the MSB-1 is restored. If the voltage is still smaller, no change is made. This sequence of operation is continued until the LSB is reached. In Fig. 3.5, the input voltage is smaller than the reference voltage and the MSB remains at the previous level (i.e. 0). When the MSB-1 and MSB-2 values are found, the voltage at the DAC output first increases and then goes back since in both cases it exceeds the reference level. After the MSB-3 changes, the voltage at the comparator output is still smaller than the reference and so, this bit keeps 1.

When an inverter input goes from 1 to 0, the voltage at the DAC output changes to the value:

$$V_n = V_{n-1} + Vs \times \frac{C_n}{C_{dacnsw}}, \tag{3.1}$$

and when an inverter input changes from '0' to '1', the DAC output becomes:

$$V_n = V_{n-1} - Vs \times \frac{C_n}{C_{dacnsw}} \tag{3.2}$$

where, V_{n-1} is the voltage at the DAC output before switching, Vs is the supply voltage, C_n is the corresponding switched capacitor, and C_{dacnsw} is the total capacitance of the DAC minus C_n. C_h represents the total parasitic capacitance from the DAC output to ground. This capacitance is formed by parasitics of the sampling switch, comparator, unit capacitors and wiring. The important point is that, C_h only attenuates the input voltage and does not degrade the linearity of the ADC. Taking into account C_h, the full-scale input swing becomes:

$$V_{fs,pp} = Vdd \times \frac{C_{dac}}{C_{dac} + C_h} \tag{3.3}$$

where, C_{dac} is the total capacitance of the binary-weighted capacitors in the bank.

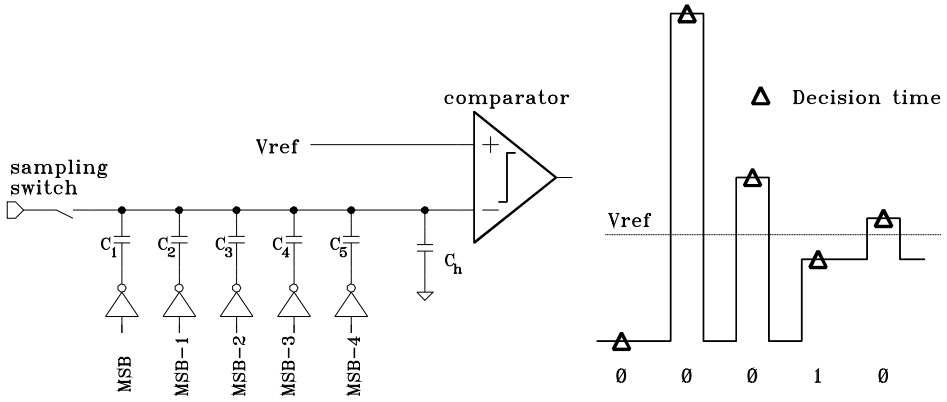


Fig. 3.5. Switching procedure from [11]

Taking into account that the proposing ADC will be manufactured in a 45nm process and the ADC from [11] has been designed in a 90nm CMOS process, improvement of the sampling speed from 10MS/s to 16Ms/s seems very realistic. In addition, the fully dynamic design corresponds to the ideology of a digital-like implementation of analog circuits. However, a 10-bit implementation instead of 8-bits means that x4 times improvement in accuracy is needed, whereas the technology is scaled only by a factor of 2. Nevertheless, the design in [11] is a good starting point and will be treated as a reference design. The feasibility study of the 10 bit ADC implementation based on the design of [11] will be performed in chapter 4.

3.3 Overall logic overview of the proposed ADC

The block diagram and the timing of the proposed ADC are shown in Fig. 3.6. The ADC consists of the following functional blocks. A 10-bit charge redistribution DAC generates analog signals at the comparator input corresponding to the digital code at the register output. The sampling switch, along with the capacitors in the DAC, performs the track-and-hold function. The SAR asynchronous logic drives the DAC and the comparator. The comparator determines the sign of the voltage at the DAC output and generates a control bit for the logic. To provide a parallel interface at the ADC output, a serial-input, parallel-output synchronous shift register is used. The stand-by control initiates and stops a conversion cycle.

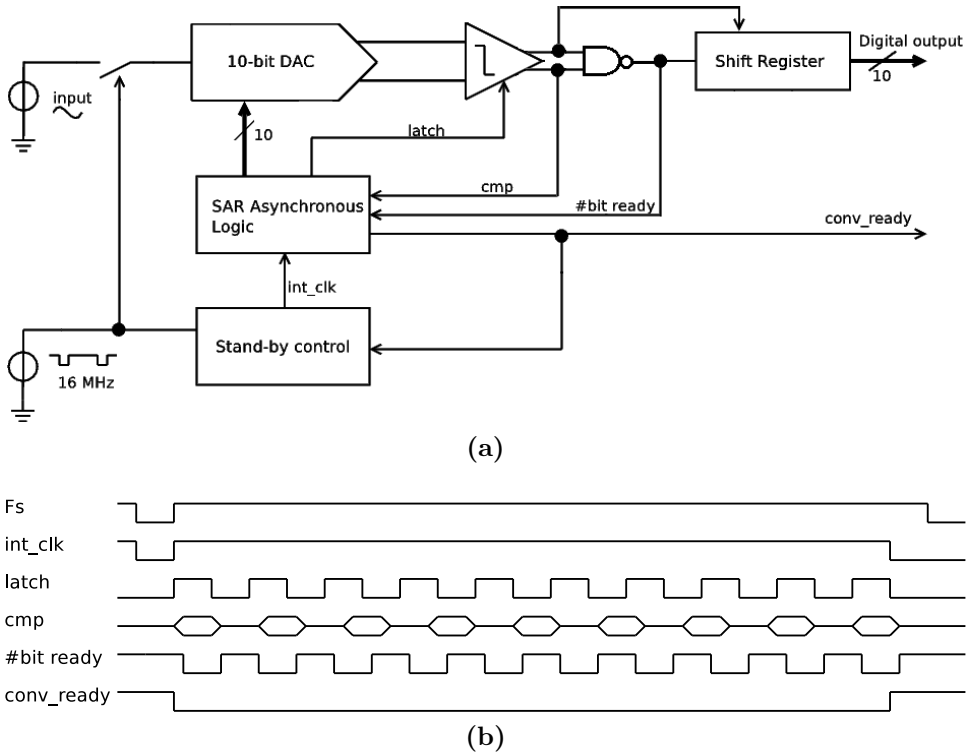


Fig. 3.6. The functional circuit (a) and timing (b) of the proposed ADC

The timing of the ADC can be described as follows. When 'Fs' is 0, the sampling switch starts to conduct, tracking the ADC input voltage on the sampling capacitor in

the DAC. When 'Fs' goes to 1 the stand-by control logic generates 'int_clk' and the conversion process starts. The first latch impulse is generated by the asynchronous logic with the rising edge of 'int_clk' and the comparator resolves the sign of the voltage at the DAC output. As the valid data at the comparator output appears, '#bit_ready' goes 0, indicating that the comparator output can be stored in the shift register and the search of the next bit can be started. This process continues until the last bit will be resolved. After the tenth cycle, the 'conv_ready' signal, generated by the asynchronous logic, indicates that the conversion is finished and the data can be taken from the output of the shift register.

The timing diagram in Fig. 3.6 is not necessary drawn to scale. In fact, the 10 internal cycles can be completed much earlier than the next tracking phase will be started if the speed of the asynchronous loop is fast enough. In this case, the ADC goes to the stand-by mode and waits the next 'Fs' clock.

A non-50% duty cycle for the 'Fs' signal is used. The duration when 'Fs' is 0 should be as small as possible to minimize the power consumption of the preceding driver due to the driving of the sampling capacitor in the DAC. If the tracking time is too short the settling error appears degrading ADC performance. However, since the switch resistance and the sampling capacitor represent a 1st order filter, only attenuation of the signal is expected. Of course, settling behavior will depend on the nature of the source impedance. For example, in the case of a standalone implementation, the inductance of the bond wires and parasitic capacitances forms a second-order filter, causing unwanted 'ringing' and degrading linearity if the tracking time is too short.

4

System level considerations

In order to enhance the resolution of the ADC without increasing the number of unit capacitors, existing charge sharing techniques will be discussed and an alternative implementation will be presented. The required accuracy of the unit capacitor will be studied as well as DNL caused by capacitor mismatch. Thermal noise is a fundamental limiter of the achievable resolution and so the minimum size of the unit capacitor will be calculated in this chapter. In a low voltage design, the comparator performance becomes crucial for the overall ADC performance and so, the non-idealities of the comparator should be considered during the first steps of the ADC implementation. A dynamic latched comparator will be discussed in this chapter as well. A sampling switch can be designed in many different ways. The most suitable implementation for this ADC will be chosen.

4.1 Charge sharing

One way to decrease the DAC area and the total switching power in a charge-redistributing SAR ADC is to use a charge sharing technique. The idea of this method is based on the following principle: if there are two equal capacitors and one of these capacitors is completely discharged and another one is charged to some value then the voltage across the capacitors after they are connected in parallel will be divided by a factor of 2. Since a SAR ADC represents the implementation of a binary search algorithm, two equal capacitors can be used to obtain the required voltage division. The capacitor bank of a 9-bit ADC from [10] is shown in Fig. 4.1.(a) and the corresponding timing diagram is shown in Fig. 4.1.(b). The capacitor bank consists of a binary-weighted array and a unit capacitors array. During the search of the first 5 MSBs, the unit capacitors are discharged and the bank with unit capacitors is disconnected from the binary weighted bank. So, an ADC performs a normal charge redistributing operation (switches that are used in the charge-redistributing operations are not shown in Fig. 4.1 to keep the schematic clear. An interested reader may refer to [10] for a detailed explanation). When the MSB-5 has to be resolved, the switch Sw_{sh1} connects C_{sh1} and C6 together and since C_{sh1} was previously discharged, the voltage at the node 'sh1' becomes twice smaller than the previous voltage across $C6$. Thus, the charge, which was previously in $C6$ is shared with C_{sh1} after Sw_{sh1} is turned on. Now, the node 'sh1' can be connected to a comparator and the comparison can be performed. Next, the 'share1' signal turns the switch Sw_{sh1} off and the switch Sw_{sh2} connects C_{sh1} and C_{sh2} together, dividing the voltage across C_{sh1} by

a factor of 2 again. These operations are repeated until the last capacitor in the unary array is reached. Only 35 unit capacitors in the bank are used for a 9-bit ADC.

The practical implementation of [10] is rather complex and has the following disadvantages. Apart from the DAC capacitors, additional sampling and tracking capacitors

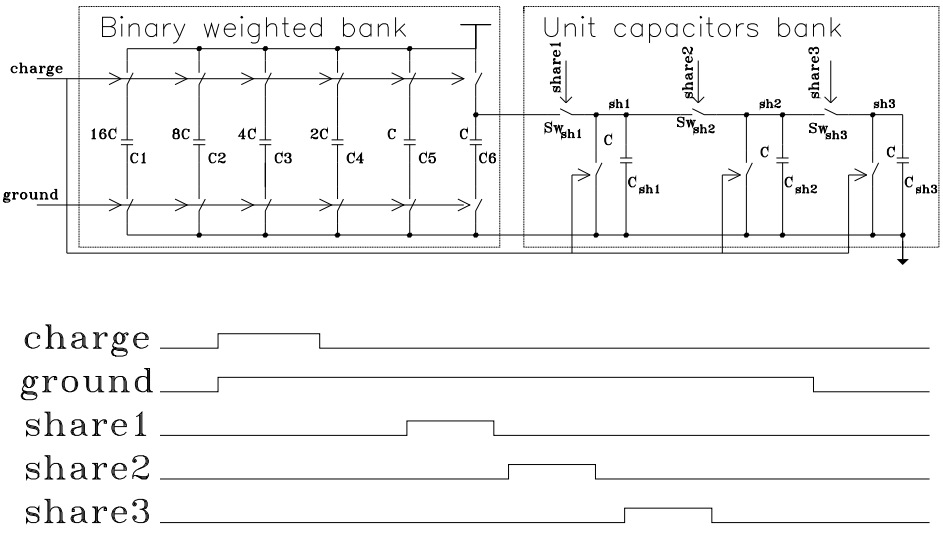


Fig. 4.1. The capacitor bank from [10](a) and the time diagrams corresponding to the charge sharing operation(b)

are used. These capacitors have to be large enough in order to provide sufficiently low kT/C noise. Also the relatively complicated switching procedure requires a large number of switches (every capacitor needs 6 switches), making the design more complex.

Another way of implementing charge sharing, which does not change the switching procedure of the reference design[11], is to connect a unit capacitor to the binary-weighted capacitor array when the last bit must be resolved as is shown in Fig. 4.2. While resolving the first N-1 bits, the sharing switches Sw_{sh} are OFF and the reset switches Sw_{rst} are ON, discharging C_{sh}. When the last bit is found, the 'reset' signal goes to 0 and 'share' goes to 1 as shown in the timing diagram of Fig. 4.2. As a result, the voltage at the 'outp' node increases and at the 'outn' node decreases. To generate the 'reset' and 'share' signals, a simple chain of inverters can be used. Thus, the control of the LSB is quite similar to the control of other bits.

The charges on the negative and positive sides of the DAC when the charge sharing capacitors are disconnected from the array are:

$$Q_{1n} = \Sigma C_{dac} \times V_{inn}, \tag{4.1}$$

$$Q_{1p} = \Sigma C_{dac} \times V_{inp} \tag{4.2}$$

where, C_{dac} is the total capacitance of the binary-weighted capacitor array, except C_{sh}.

When the charge sharing capacitors are connected to the capacitor bank, the charge becomes:

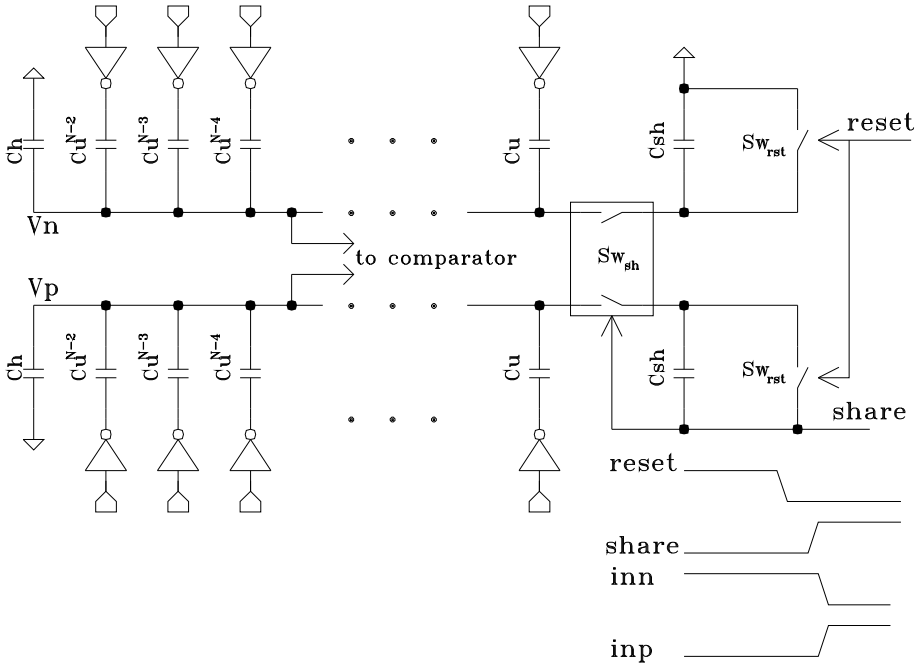


Fig. 4.2. Proposed DAC with charge sharing implementation

$$Q_{2n} = (\Sigma C_{dac} + C_{sh}) \times V_n, \tag{4.3}$$

$$Q_{2p} = V_p \times (\Sigma C_{dac} + C_{sh}) - V_{dd} \times C_{sh} \tag{4.4}$$

where, V_p and V_n are the voltages at the DAC output, after C_{dac} and C_{sh} are connected together.

Equating the charges before and after the charge sharing, the voltage at both sides can be calculated:

$$V_n = V_{inn} \times \frac{1}{1 + \frac{C_{sh}}{\Sigma C_{dac}}} = V_{inn} \times \frac{1}{1 + \frac{2}{2^N}}, \tag{4.5}$$

$$V_p = V_{inp} \times \frac{1}{1 + \frac{2}{2^N}} + \frac{2V_{dd}}{2^{N-1} + 2}. \tag{4.6}$$

The differential voltage at the DAC output is:

$$V_p - V_n = (V_{inp} - V_{inn}) \times \frac{1}{1 + \frac{2}{2^N}} + \frac{2V_{dd}}{2^N + 2} \tag{4.7}$$

If $2^N \gg 2$ and $\frac{2}{2^N} \ll 1$, equation (4.7) can be simplified to:

$$V_p - V_n = (V_{inp} - V_{inn}) + 2 \times \frac{V_{dd}}{2^N} \tag{4.8}$$

Equation (4.8) represents the voltage at the DAC output after the Nth switching step and corresponds exactly to the LSB step of an N-bit converter. Thus, an additional bit can be obtained by adding only two unit capacitors.

In fact, two errors occur due to the simplification that has been made to obtain (4.8): the '2' in the denominator of $\frac{2Vdd}{2^N+2}$ and the term $\frac{1}{1+\frac{2}{2^N}}$. The consequences of these errors are described below.

The DAC output voltage for a digital code k (where $k = [1, 2, 3...2^N]$) of an N-bit converter with proposed charge sharing can be modeled using equation below:

$$Vout_k = \left[\frac{\sum_{i=1}^{N} C_i D_i}{\sum_{i=1}^{N} C_i} + \frac{S_k}{2^N+2} \times \frac{1}{1+\frac{2}{2^N}}\right] \times V_{ref}, \tag{4.9}$$
$$C = \{2^{N-2}, 2^{N-3}, ..., 2^{N-N}, 1\} \times C_u,$$
$$S = \{1, 0, 1, 0, ..., 1, 0\}$$

where,

C_i is the set of the binary-weighted coefficients. For example, for a 10-bit DAC with a charge sharing $C = \{256, 128, 64, 32, 16, 8, 4, 2, 1, 1\}$,

D represents an N-bit binary word,

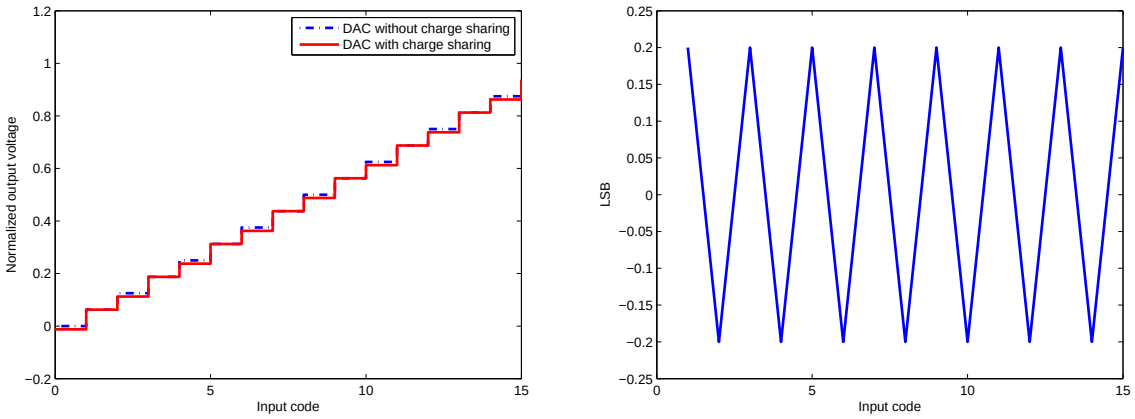


Fig. 4.3. The transfer functions of a 4-bit DAC with and without charge sharing (a) and the DNL error(b)

The LSB for a digital code k is always opposite to the LSB for the code $k-1$ and so, the toggling of the charge sharing capacitor is modeled by the set S with alternating zeros and ones. The length of the set S is 2^N.

A transfer function of the 4-bit DAC with proposed charge sharing implementation is compared with a transfer function of a conventional charge-redistributing DAC in Fig. 4.3(a). A DNL error is shown in Fig. 4.3(b) and is equal to +0.2/-0.2, but increasing the number of bits causes the error decrease. For example, the DNL is only +0.004/-0.004LSBs in case of a 10-bit DAC.

4.2 Asynchronous Logic

The simplified circuit of the asynchronous logic is shown in Fig. 4.4. It consists of the 10 digital slices and the combinatorial logic to generate the 'latch' signal for the comparator. Every slice controls a bit in the DAC. As a bit is resolved, the 'next' signal appears at the slice output, activating the next slice. The detailed description of a slice and corresponding timing diagrams will be given in chapter 5.

At this point it is necessary to point out that the operations of the first and the last slices are different. Referring to Fig. 3.5, the MSB-1 to LSB+1 slices change the DAC bit first and then restore or keep it, depending on the comparator output, whereas the MSB slice changes the corresponding bit of the DAC only after the comparator decision. For the LSB slice, there is no need to change the DAC bit after the comparator makes a decision since the conversion is completed.

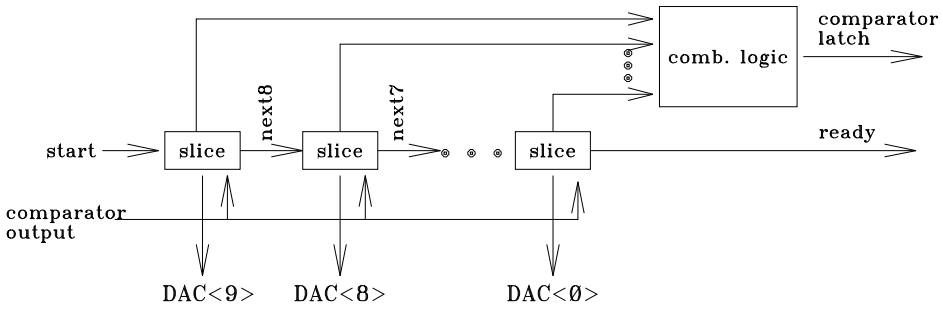


Fig. 4.4. The simplified circuit of the asynchronous logic

4.3 Capacitor matching

The accuracy of the capacitors in the DAC determines the maximum achievable resolution of the ADC. If the mismatch of the capacitors is too high and the desirable resolution cannot be achieved, a number of ways to eliminate the problem exist. For example, calibration, trimming, or a technology with better capacitor matching can be used. Of course, the simplest way is to increase the area of the capacitors but this will increase the DAC switching power.

To minimize the DAC switching current a small, 0.5fF unit capacitor, has been chosen. The available fringe capacitors in the process design kit(PDK) library can only be scaled to a minimum value of $2fF$. Therefore, a custom designed capacitor will be used. Unfortunately, statistical data for these kinds of capacitors does not exist because they have not been characterized before. However, the accuracy of fringe capacitors from the PDK is known and taking into account that the same LER (line-edge roughness) effect affects the accuracy of the custom designed capacitor, its matching parameters can be estimated to be similar, i.e. $A_c = 0.32\%\sqrt{fF}$. Therefore, 0.45% mismatch is expected for the $0.5fF$ capacitor.

For a binary-weighted charge-redistribution DAC, monotonicity requires that the capacitor mismatch satisfies [2]:

$$\delta = \frac{C_2 - C_1}{C_1 + C_2} < \frac{1}{2^N} \tag{4.10}$$

Obviously, only 7-8 bit resolution is achievable with the mismatch of 0.45%. However, it was pointed out in [16] that equation (4.10) leads to over-design because the variation of every unit capacitor has a normal distribution. Thus, it is necessary to consider the distribution of the random variables and their correlation.

Based on equation (4.10) and the distribution-based calculation from [16], the maximum attainable resolution versus the standard deviation of a unit capacitor in a charge-redistribution DAC is shown in Fig. 4.5. According to the plot, 10-bit resolution is achievable even with 0.7%-0.8% accuracy of a unit capacitor.

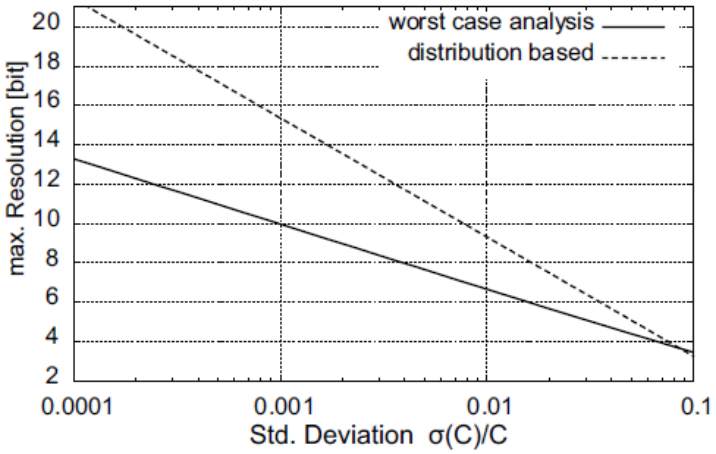


Fig. 4.5. Maximum resolution of a charge redistributing DAC versus the standard deviation of a unit capacitor $\sigma(C)/C$[16]

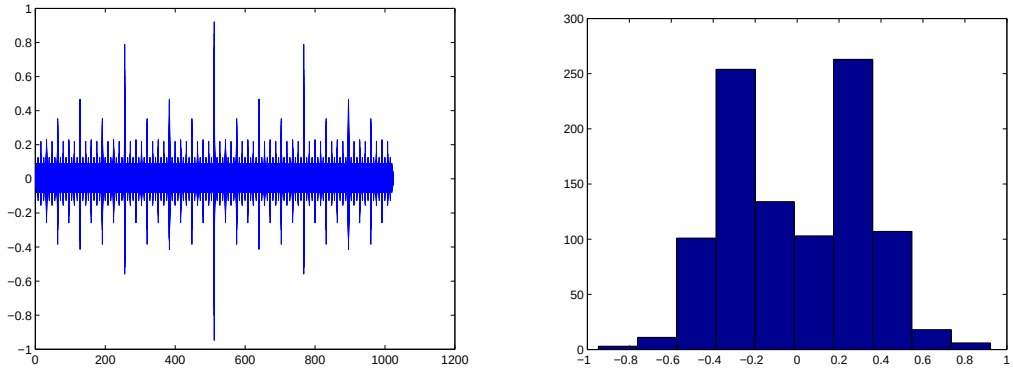
The DNL of a DAC is a very good measure of how well the unit capacitors are matched. Monte Carlo simulation to estimate the DNL distribution due to the random variation of the capacitors has been performed. In the model, for every unit capacitor, a normally distributed random error is generated and the transfer function using equation (4.10) is determined from the obtained coefficients C. The Matlab code is given in Appendix B.

The estimated 3σ DNL variation is 0.972LSB with the mean value at +0.4/-0.4LSB, based on 1000 Monte-Carlo runs (see Fig. 4.6).

To understand the gap in the DNL histogram, the following reasoning can be applied. To achieve a near zero DNL value, all capacitors in a DAC should be close to their nominal value. The probability of this event is smaller than the probability of having any capacitor with some deviation. Therefore, the largest number of events is shifted from the zero DNL value.

4.4 Comparator

A comparator is a crucial device for the overall ADC performance. Although a digital signal appears at the comparator's output, the input signal is analog and, consequently,



(a) **(b)**

Fig. 4.6. DNL plots of the 1000 MC simulations of the differential 10-bit DAC with charge sharing

all problems associated with amplifiers are common for comparators as well (i.e. offset, noise, finite gain, etc.). Moreover, a number of additional aspects due to non-linear behavior of a comparator appear. Depending on the ADC architecture, some of the non-ideal effects are very critical, whereas others can be quite tolerable.

A dynamic latched comparator during the comparison phase can be simplified to the circuit shown in Fig. 4.7. It consists from the input differential pair M0, M1, a positive feedback latch M2, M3, and the integrating capacitors C0, C1. The relation between the total input referred offset and the circuit parameters of the comparator can be express with [2]:

$$\sigma^2_{in,off} = \sigma^2_{Vth0,1} + \frac{gm^2_{3,4}}{gm^2_{0,1}}\sigma^2_{Vth2,3} + \frac{I^2_{load}\sigma^2_{R_{load}}}{gm^2_{0,1}R^2_{load}} \tag{4.11}$$

The first term in equation (4.4) represents static offset, the second term describes static and dynamic offset, and the third term is due to dynamic offset only. Static offset is independent of the input common-voltage and does not affect the ADC linearity since the same error is observed for every code, i.e. only shift of the transfer curve appears. In contrast, the value of dynamic offset changes with output codes, causing non-linear distortion.

Observing equation (4.4) several conclusions can be made. Static offset can be minimized by increasing the area of the input transistors and the latch. Transconductance of the input pair should be as large as possible to achieve the lowest static and dynamic offset. Smaller transconductance of the latch decreases offset at the expense of comparator speed. The third term in the equation implies that the load mismatch at the comparator output contributes to dynamic offset and so, should be very well matched. Another way to minimize this term is to make the load current as low as possible.

The methods to compensate for the static offset of a dynamic comparator are based on the implementation of a capacitor array at the comparator output, which is tuned by some control logic to equalize the slopes of the currents flowing through the integrating

capacitors $C0$, $C1$ (see Fig. 4.7). A reasonable offset attenuation can be achieved at the expense of design complexity. The answer whether offset compensation is needed or not depends on the system ADC will be used. The ADC's output is saturated if the signal with full-scale swing is fed into the ADC input with a presence of static offset. Obviously, the easiest way to manage this is to make sure that a signal at the ADC's input is small enough. This can be done via an AGC loop. However, it is necessary to bear in mind that the SNR becomes worse with decreasing input swing since the power of the quantization error remains the same. The SNR due to a not full-scale input voltage can be calculated as:

$$\begin{aligned} SNR_{dB} &= 20log_{10}\Big(\frac{v_{in(rms)}}{Q_{error}}\Big) = 20log_{10}\Big(\frac{\frac{v_{in(p-p)}}{2\sqrt{2}}}{\frac{v_{fs}}{2^N\sqrt{12}}}\Big) = \\ &= 20log_{10}(\frac{v_{in(p-p)}}{v_{fs}}2^{N-1}\sqrt{6}) \end{aligned} \tag{4.12}$$

Suppose, the input referred offset of a comparator is $50mV$. Then, the input differential swing must be lower than a full-scale range by a value of $100mV$ in order to avoid clipping at the ADC's output. This corresponds to $0.14 \times V_{fs}$, where $V_{fs} = 0.725mV$. Plug-in the numbers into equation (4.12), the SNR loss due to $50mV$ offset is only 1.3dB. This value is usually acceptable and so, a reasonable requirement of the comparator output offset is that it should be less than $50mV$.

The metastability condition (i.e. when the output is balanced between the digital 'one' and 'zero') at the comparator output occurs when the input voltage is so small that the output digital state cannot be resolved within a specific time interval. In this design, a comparator state is checked during every comparison cycle and so, no switching in the DAC occurs until the proper digital value appears at the ADC output.

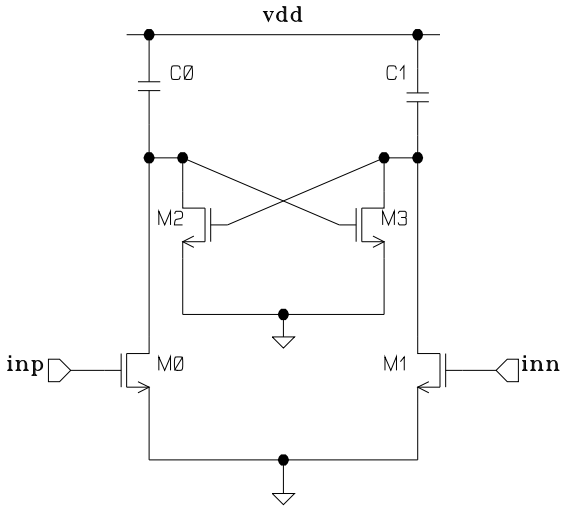


Fig. 4.7. Dynamic comparator during the latching mode

A sharp voltage change (commonly from rail to rail) at the comparator output, or feedthrough of the 'latch' signal to the input, creates kickback noise at the comparator input due to AC coupling between different components in a circuit. In ADCs with large number of comparators switching simultaneously, the kickback noise affects the reference and input voltage, resulting in harmonic distortions. The SAR architecture is less sensitive to this phenomenon since only one comparator is usually used, meaning that every digital code is affected by the kick-back voltage equally and so, non-linear effects do not appear .Also, the kickback noise is seen at the comparator input as common-mode voltage and so, a differential design allows to attenuate unwanted glitches.

Different comparators are affected by the kickback noise differently. In general, comparators with a fixed bias current in the input transistors and with a latch in the second

stage, have a low kickback noise because a large signal does not appear across the input transistors. Fully dynamic comparators have higher kickback noise since the input transistors are turning off and on during every comparison cycle, resulting in a sharp change of the transistors states, causing charging and discharging of its parasitic capacitances.

A comparator in a SAR ADC must recognize voltage difference as small as 1LSB and this makes it a bottleneck in a low-voltage design since the LSB voltage becomes comparable with the thermal noise of the comparator as resolution increases. Ideally, the input referred peak-to-peak noise of the comparator should not exceed 1LSB value to ensure that no wrong decisions occur. Since thermal noise has a normal distribution, its peak-to-peak value can be practically expressed as 5σ. Taking into account that the LSB voltage in this ADC is $725\mu V$, the rms noise value should not exceed $145\mu V$. To achieve this low value, a low noise preamplifier in front of a latch is desirable. A low noise amplifier requires transistors with a big area to minimize its flicker noise and a considerable drain current to decreases its thermal noise. Thus, there is a trade-off between resolution and power consumption.

4.5 Noise

There are four main sources of noise in this ADC: quantization noise, sampling noise, DAC noise and comparator noise. Noise from every source can be calculated and summed up together. After that, the SNR can be estimated by taking the ratio of the input full-scale amplitude and the total input referred ADC noise voltage.

For converters with resolution larger than 6-7 bits the quantization noise can be modeled as white noise in spite of the fact that it does not have a white spectrum [2]. In general, Nyquist-rate converters are designed in a way to make the quantization noise dominate over thermal noise. RMS quantization noise voltage for an N-bit converter can be calculated using a well-know formula:

$$V_n = \sqrt{\frac{A_{LSB}^2}{12}} = \frac{V_{full-scale}}{2^N\sqrt{12}} \tag{4.13}$$

where $V_{full-scale}$ is the peak-to-peak full swing input voltage.

It will be shown in chapter 5 that the full-scale range of the ADC is 0.725V with a 0.8V supply and so, the noise voltage due to the quantization error is 204μV.

The sampling capacitor consists of a binary-weighted capacitor bank with the total capacitance $C_{dac} = 256fF$, and redundant capacitance from the DAC output to ground $C_h = 280fF$ (see chapter 5). Thus, the total sampling capacitance is $536fF$. For a differential signal, the sampling capacitance is two times smaller and the sampling thermal noise due to the resistance in the sampling circuit can be calculated as:

$$V_n = \sqrt{\frac{kT}{C_{dac} + C_s}} = 124\mu V \tag{4.14}$$

Output resistance of the inverters in the DAC is the source of DAC noise. This noise is limited by the effective capacitance, which loads the inverters and, therefore, represents kT/C noise [11]:

$$V_n = \sqrt{\frac{2kT(C_{dac}+C_h)}{C_{dac}+C_h} \times \frac{C_{dac}}{C_{dac}+C_h}} = 129\mu V \tag{4.15}$$

Noise calculation of a dynamic comparator is not a straightforward task since the comparator is inherently a non-linear circuit. For comparators with a preamplifier in front of a latch, a common assumption is that the noise of the preamplifier dominates. This noise can be easily calculated since a preamplifier represents a linear amplifier. However, in the case of a dynamic comparator this assumption is not valid anymore. The cases are known, where a degradation of more than one bit has been observed due to the underestimated noise of a dynamic comparator[17, 10]. In this design, the guidelines to minimize the comparator noise are used [18, 19] and estimation of the noise is based on simulation results. Simulated comparator noise is 120μV. The total thermal noise of the ADC is a square root of the sum of squares of all noise voltage source and is equal to 215 μV.

In this design thermal noise is comparable with the quantization noise. The SNR of the ADC including quantization and thermal noise:

$$SNR = 20log\Big(\frac{V_{sigrms}}{V_n}\Big) = 58.76dB, \tag{4.16}$$

and corresponds to an ENOB of 9.5 bit.

4.6 Sampling switch

A sampling switch is the front-end of the ADC and requires careful attention during the design. The implementation of the switch depends on the required bandwidth and accuracy. Noise is out of concern because it is determined by the sampling capacitance.

The sampling switch can be designed with a single NMOS or PMOS transistor, a complementary CMOS switch or more complicated bootstrapping circuitry can be used. The simplest implementation is always preferable but rarely feasible.

The input signal swing of 0.4V and the supply voltage of 0.8V make it impossible to use a single transistor as a switch. A CMOS switch is able to cover a rail-to-rail input range, however, due to the low supply voltage there is a voltage range in which both NMOS and PMOS transistors are in the sub-threshold region. As a result, a conductance gap in the middle of the input range appears, degrading the linearity. Obviously, increasing the width of the transistors makes a switch more linear, but as transistors get larger, various dynamic effects start to degrade their linearity. These effects occur due to the charge redistribution processes between the voltage dependent parasitic capacitances of

the transistors and a sampling capacitor. According to the simulation results, the maximum achievable effective resolution of a CMOS switch with a 2 MHz, 0.55V peak-to-peak amplitude and 0.5pF loading capacitance is 9 bits.

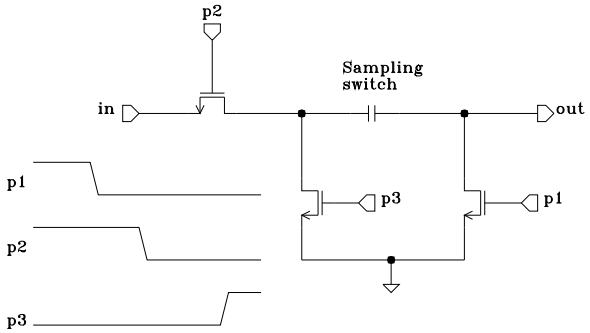


Fig. 4.8. Bottom plate sampling

Another reason of degrading the switch linearity is a charge injection phenomenon. When a transistor turns off, the charge leaves the channel and flows in two direction: to the signal source and to the sampling network. The part of a charge which flows into the sampling network creates an error on the sampling capacitor. The problem is that, the charge in the MOS channel depends on the source/drain potential, which changes with input voltage resulting in harmonic distortions. Since the amount of the released charge is proportional to the channel area, increasing transistor area leads to a larger charge and, consequently, larger distortions.

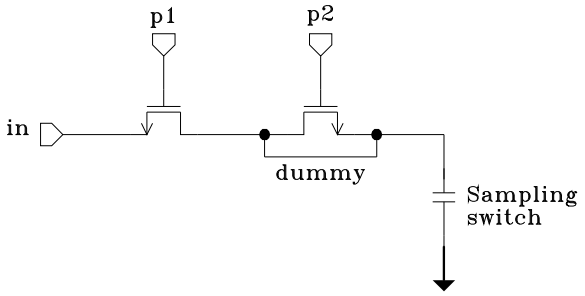


Fig. 4.9. Dummy switch for the charge injection cancellation

The well-known way to minimize the effect of charge injection is the use of bottom plate sampling. The idea of this method is to sample the input voltage on the 'grounded' plate of a sampling capacitor to eliminate a signal dependent error. The conceptual circuit is show in Fig. 4.8. However, such approach hardly fits into the chosen topology. Considerable redesign of the DAC is required to implement the bottom-plate sampling.

Another way to decrease charge injection is to use a dummy transistor as it is shown in Fig. 4.9 [20]. The length of the dummy transistor and the switch should be the same. The dummy width should be twice smaller than the width of the switch In addition, the clock signal p1 and its inverted version #p1 must be very symmetrical. Moreover, to achieve a good cancellation, impedances on the both sides of the switch should be the

same in order to equally spread the released charge. Although, the described method can cancel the released charge, it relies on perfect matching which is rarely achievable in practice.

Another implementation of a sampling switch uses a bootstrapping technique. The idea of this method is shown in Fig. 4.10. There are two phases of operation of the circuit. During the first phase, a bootstrapped capacitor is pre-charged to vdd and NMOS transistor is off. During the second phase, the bootstrapped capacitor is reconnected to the source and the gate of the switch transistor, making its gate-source voltage and, consequently, its on-resistance independent of the transistor's source voltage, drastically improving linearity of the switch. In fact, for low voltage ADCs this is usually the only way to achieve good performance of the sampling network since the input swing in these ADCs is comparable with the MOSFET's threshold voltage. The bootstrapped switch seems a very good choice and has been chosen for the ADC. Moreover, in this design there is no need to use a low-ohmic switch since the input bandwidth is limited to 8MHz and so, a small enough switch transistor can be used in order to minimize the error due to charge injection without using bottom-plate sampling.

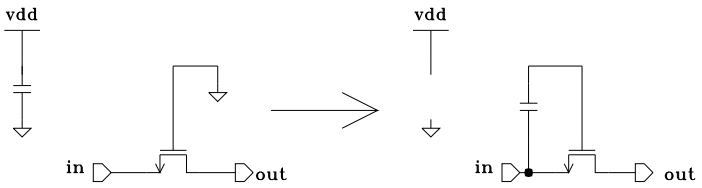


Fig. 4.10. Bootstrap technique principle

Summarizing this chapter, the following key building blocks have been chosen for the ADC implementation. Binary-weighted charge redistribution DAC with a charge sharing minimizes the ADC's power and area. A fully dynamic comparator is used in order to minimize the power consumption and to avoid DC bias. A bootstrapped switch is able to provide a good linearity. Also, the value of the unit capacitors has been chosen based on power, matching and noise considerations.

5

Circuit and Layout design

As was mentioned in chapter 3, the sampling switch should be designed to achieve a 10-bit linearity, meaning that the third harmonic should not decrease ENOBof the ADC, i.e. should be below -65...-70 dBc.The linearity of the converter can be affected by the DAC layout and so, the layout of the DAC will be discussed in this chapter. The charge accumulated on the sampling capacitors during the sampling phase must be kept constant during the whole conversion cycle and so, the charge sharing implementation should be done in such a way as to avoid injection or loss of charge at the sampling node. The comparator's performance affects the dynamic range and the SNR of the ADC. The asynchronous controller must be fast enough to provide the desired sampling rate. Since dynamic digital logic is used, the design should be robust against current leakage. All the above mentioned will be discussed in this chapter.

5.1 The sampling switch

As discussed in chapter 4, the basic components of a bootstrapped switch are an NMOS transistor, a switch and a bootstrapping capacitor. A few additional transistors are needed to provide proper control over the components and ensure the robustness of the circuit. One possible implementation is shown in Fig. 5.1, which is similar to [4]. The idea of the circuit is following. If 'sn' is low, the bootstrapped switch is in hold-mode, PMOS capacitor M1 is charged to the supply voltage through the transistors M3, M4, the gate of M0 is shorted to ground by M8, M9 and so there is no DC path from the input 'in' to the output 'out'. During track-mode, 'sn' is high and M3, M4 are turned off. The chain of transistors M5-M1-M2 connects the input voltage to the gate of the switch transistor M0 and so its gate potential is equal to the source voltage plus the supply voltage (vdd). Thus, the Vgs of transistor M0, and, therefore, its resistance, is independent on the input voltage.

There are several crucial aspects of this circuit. Firstly, to ensure reliable operation, the voltage across the gate oxide must never exceed the nominal breakdown voltage of a transistor (1.3 V). For this purpose, the sources of M7, M10 are connected to the drain of M4 instead of ground. If the sources were connected to ground, the gate-drain voltage of M10 and gate-drain/source of M2 would exceed the supply voltage during the track mode and this would cause circuit reliability concerns. To prevent breakdown of M8, M9 is placed between the drain of M8 and the gate of M0. Secondly, the gate of M0 is a high-

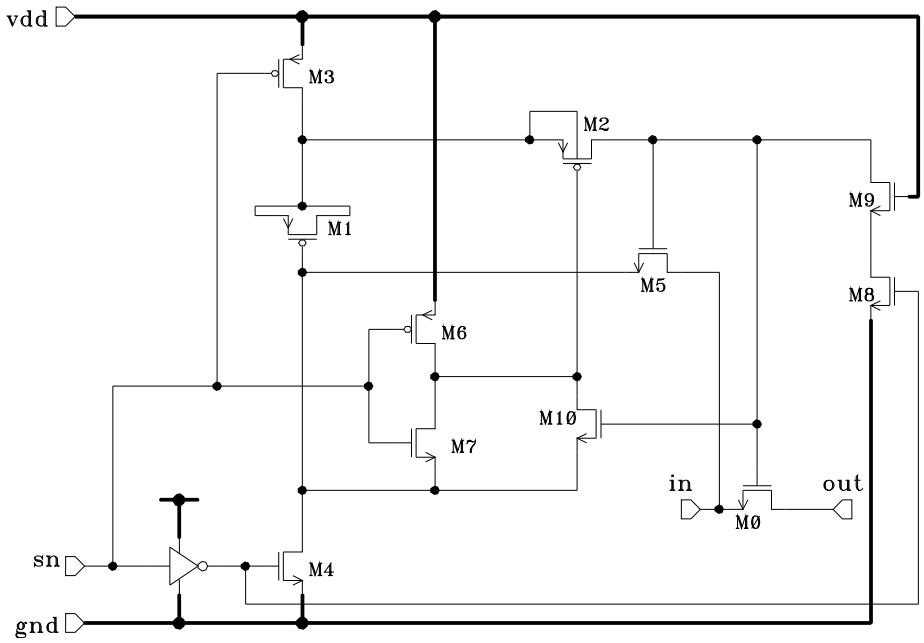


Fig. 5.1. A bootstrapped switch

impedance node, whose voltage is defined by the charge on capacitor M1. Consequently, any DC leakage path influences the voltage at this node by discharging the capacitor M1. To minimize this effect, the body of M2 is connected to the source instead of to vdd, preventing the source-nwell and drain-nwell junctions from becoming forward biased when the source/drain voltage of M2 exceeds the supply voltage. The drain-nwell junction or the source-nwell junction of M3 (depending on its NWELL connection) also introduces a DC leakage path that can be minimized by decreasing the transistor width. In a more advanced circuit topology of the bootstrapped switch [21], the problem is eliminated by making M3 an NMOS transistor. The disadvantage is that a clock-boosting circuit is needed to compensate for the voltage drop from the gate to the source of M3. Otherwise the bootstrapping capacitor will not be charged to the supply voltage. The clock boosting inevitably increases the area and the overall power consumption of the ADC.

A MOS capacitor is used as the bootstrapping capacitor since it has a larger capacitance value per square area than the available fringe capacitor. The value of the MOS capacitor is approximately 0.5pF at 0.4V.

In Fig. 5.2, the voltage at the top plate of the bootstrapping capacitor M1 is shown. To obtain this waveform, ideal switches instead of M2, M3, M4 and a capacitor M1 with a large capacitance are used. If a reasonably-sized capacitor instead of M1 is used, only voltage attenuation is observed (dashed line in Fig. 5.2). The actual response of the circuit is shown by the solid line. The discharge of capacitor M1 is clearly seen. It is necessary to point out that leakage current occurs not only via the source and drain junctions but is also due to the finite off-resistance of the PMOS transistor M3, which is a transistor with minimum channel length (45nm). The waveform can be significantly improved by increasing length and width of M3, however, simulations shows that HD3 is

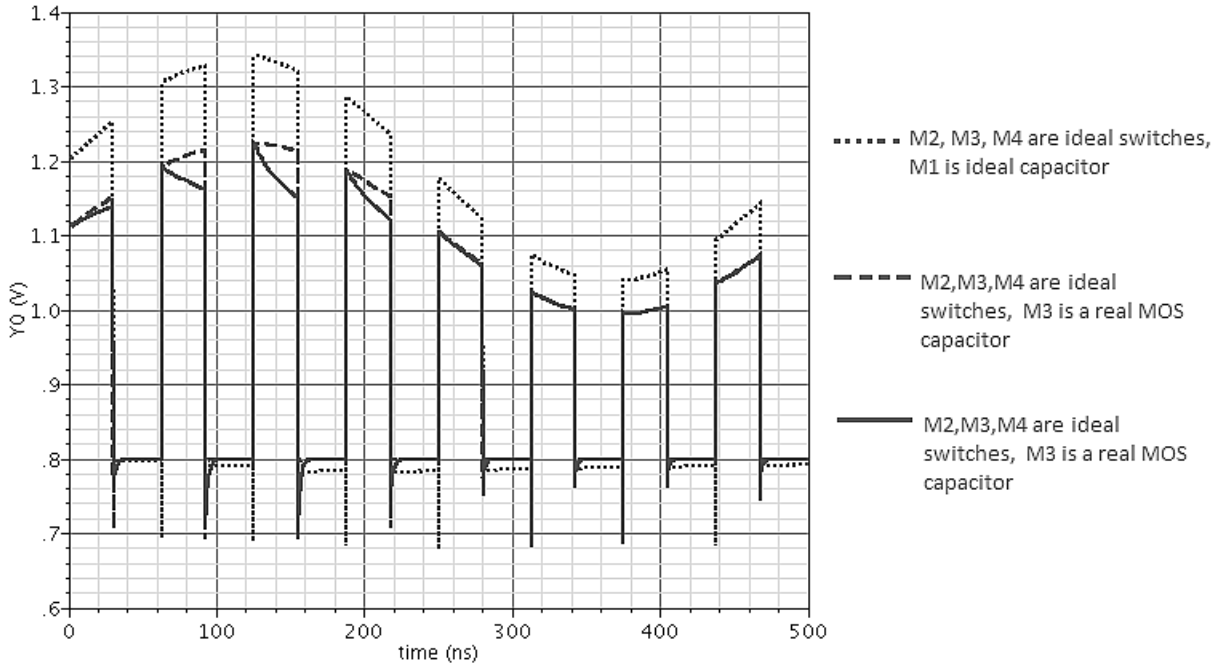


Fig. 5.2. Voltage at the top plate of the capacitor M1.

below -70dBc with PVT variations. This number is good enough for a 10 -bit ADC.

Sampling uncertainty appears due to the jitter of the sampling clock. A clock buffer is used to clean-up the external sampling clock. Jitter is simulated using the transient noise analysis and is $0.6ps$, which corresponds to SNR=84dB. This value is much better than is required for a 10-bit ADC.

5.2 The unit capacitor implementation

The unit capacitor layout is shown in Fig. 5.3. In order to maximize the effective capacitance and to minimize the capacitor's area, the minimum metal spacing is used. The active area of the capacitor is $0.75\mu m \times 0.25\mu m$.

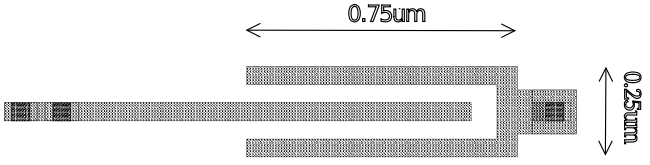


Fig. 5.3. A 0.5 fF capacitor [11]

This is a fringe-type capacitor because the active area is in between the metal wires. Therefore, the 'useful' capacitance is proportional to the length of the capacitor and the number of stacked metal layers. Besides the desired capacitance, a parasitic capacitance to the substrate appears. Since the area of the plates is different, the value of this parasitic capacitance is different as well and is equal to 145aF and 85aF respectively. As mentioned

in chapter 4, these capacitances only decrease the full-scale range of the ADC and do not degrade the linearity of the ADC.

There are seven available metal layers in the used process flow, but layers 6 and 7 are thick layers, and cannot be used for compact, low-parasitic capacitor implementation. Moreover, it is better to avoid the use of metal layers that are close to the substrate due to their larger parasitic capacitance. In this design, the unit capacitor has been implemented in metal layers 3 to 5 which turned out to be the optimum between the length of the wires and the number of stacked metals. Vias along the wires will increase the 'useful' capacitance but will most likely degrade the matching of the capacitors. So, vias are used only to connect the metal wires at the capacitor edges.

Assura and Assura Field Solver have been used to extract the capacitor values. According to the post-layout simulation, the absolute value of a capacitor varies by $1\% - 5\%$ depending on the tool used, but the ratio between two capacitors is the same with both tools.

5.3 The charge sharing capacitor

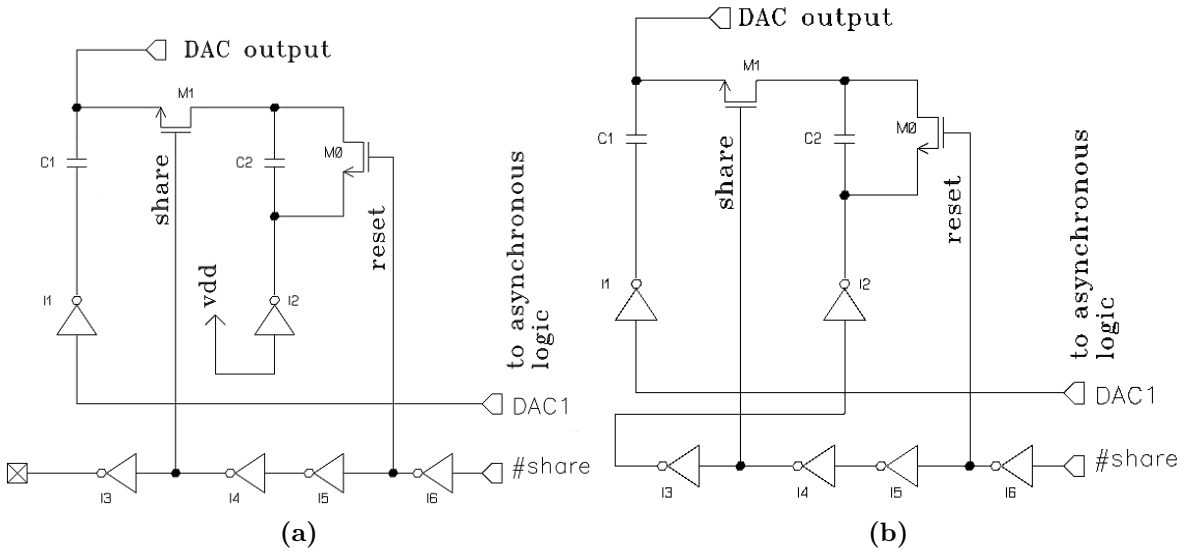


Fig. 5.4. Implementation of the charge sharing capacitor in the negative (a) and positive (b) sides of the DAC

The transistor level implementation of the charge sharing bit in the negative and positive sides of the DAC is shown in Fig. 5.4 (a) and (b), respectively. As the '#share' signal appears, the chain of inverters generates the 'share' and the 'reset' signals that control the switches M1 and M0 respectively. The input of I2 is connected to vdd in the DAC's negative side since on this side bottom plate of the sharing capacitor is always grounded, and to the output of I3 at the positive side because during the LSB search, the voltage has to be increased here. The top level schematic of the DAC is shown in Fig. A.5

Determining the last significant bit can be divided into three sequential phases. During each phase, different errors occur. The consequences of these errors on the DAC output

waveform are shown in Fig. 5.5.

During the first phase, the switch M0 shorts both terminals of a charge-sharing capacitor, discharging it from $0.5fF \times vdd/2$ to zero. The discharging process must be finished during resolving the first nine bits. Moreover, a small charge is always injected from the DAC output to the top plate of the sharing capacitor due to the finite impedance of the sharing switch M1 while processing of the previous bits. The size of the reset switch M0 determines how fast the charge of C2 will be reset to zero. The estimated on-resistance of the minimum-sized NMOS transistor is 10kΩ and since the value of a sharing capacitor is 0.5fF, the time constant is very small and so, the minimum-sized transistor for the reset switch has been chosen.

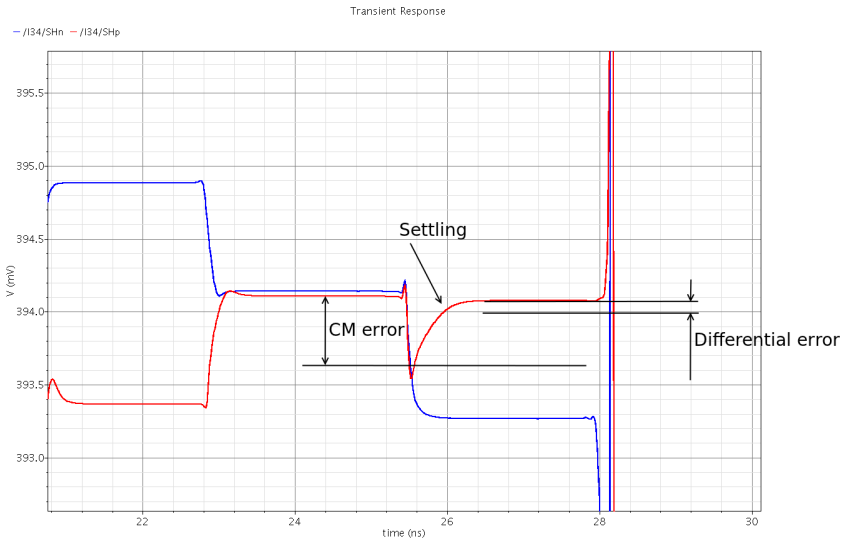


Fig. 5.5. The DAC output waveform during the last conversion cycle

During the second phase, the 'share' signal goes to 1 and M1 connects C2 to the DAC output. Clock feedthrough due to the gate-source and gate-drain capacitors of the transistor M1 contributes to common-mode error at the DAC output (see Fig. 5.5).

During the 3rd phase, a differential error appears due to the drain-source capacitance of M0 since the control signal changes from 0 volts to the supply only at the one side of the DAC. The routing wires and the vias at the source and drain sides of M0 contribute to additional parasitic capacitance. To minimize this capacitance, the source and drain active area of M0 has been increased in order to separate the source and drain interconnects farther apart. The finite resistance of the sharing switch M1 limits the time of a charge redistribution process between the sharing switch and the DAC. Thus, the size of M1 is chosen based on a compromise between the clock feedthrough during phase 2 and the settling time during phase 3.

5.4 The DAC

The DAC layout represents two strings of unit capacitors placed in the common-centroid way. Partial layout of the capacitor array is shown in Fig. 5.6. The bottom string consists of the binary-weighted capacitors and the upper string represents the capacitor

C_h, which attenuates the input range, ideally to $1 \times Vdd$. A slightly increased distance between the capacitors in the bottom string and the control wires $D9..D0$ provides a more accurate value of the MSB capacitor. The common centroid layout minimizes stress and temperature gradients across the capacitors and also makes the routing parasitic capacitance and resistance proportional to the capacitors value. The dummy capacitors at the edges of the string provide the identical environment for all capacitors. Since any irregularity of the DAC pattern disturbs the ratio between the capacitors, the sharing capacitor has been placed aside from the capacitor array, despite the matching between the sharing capacitor and the capacitors in the bank will be worse.

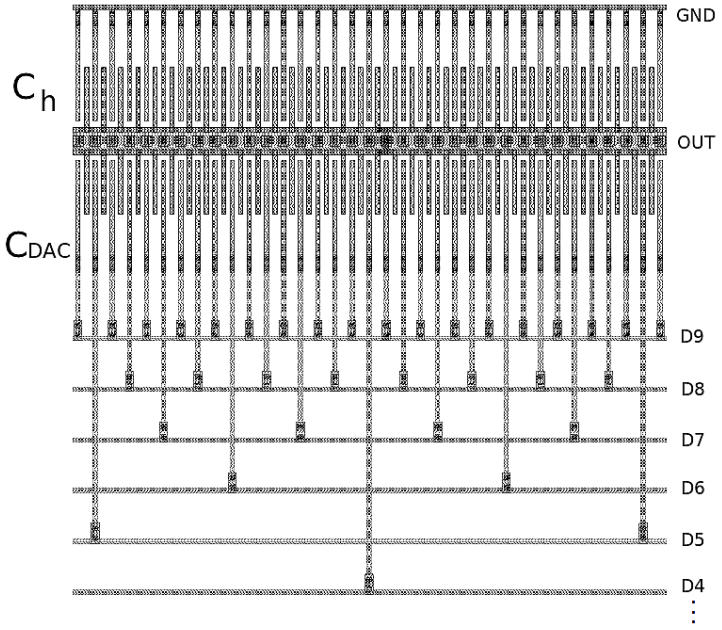


Fig. 5.6. Layout of the capacitor array

Inverters drive the capacitors in the DAC. Ideally, to provide the waveform identity for every code at the DAC output, the size of the inverters should be scaled proportionally to the capacitors, however, this is highly impractical since it dramatically increases the DAC's area. So, the size of inverters has been chosen only large enough to provide a 10-bit settling (7.6τ) within 3ns. This time corresponds to the approximate speed of the asynchronous controller.

The extracted capacitors are given in table 5.1. The capacitors in the string are not exact since a unit capacitor is very small and layout errors are very difficult to track using the existing tools. The best way to estimate whether the ratio between the capacitors is good enough or not is to build a DNL plot using the given capacitors.

The DNL of the DAC with the post-layout capacitors is shown in Fig. 5.7. The worst DNL error of $0.064LSB$ is considerably lower than the DNL error due to the random variation.

Post-layout extraction of the parasitic capacitance from the DAC output to ground shows $277.9fF$ and the total capacitance of the binary-weighted array is $256.9fF$. Ideally, both values should be equal to $256fF$. Using equation (3.3), the full-scale voltage swing

Capacitor value (fF)	Normalized value
128.473	256.3
64.2353	128.167
32.1172	64.073
16.0581	32.1172
8.02969	16.0581
4.01501	8.001
2.00734	4.005
1.00301	2.001
0.50126	**1.000**
0.51500	1.028

Table 5.1. Extracted capacitors and their normalized values

with a supply voltage $0.8V$ is equal to $0.768V$. However, this calculation does not include parasitic capacitance of the comparator and the switch. Post-layout simulation of the ADC results in $0.725mV$ differential full-scale input range.

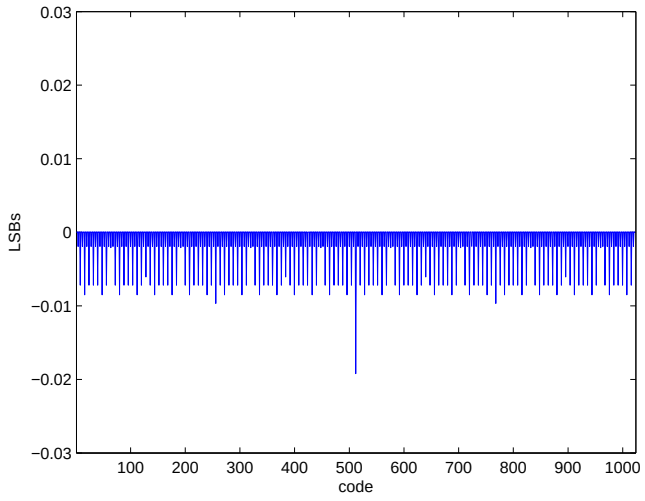


Fig. 5.7. The DAC DNL due to extracted systematic error

5.5 The comparator

In this design, a two-stage dynamic comparator [9] is used. The dynamic comparator is a good choice for low-power applications since it does not have DC power consumption. The circuit of the comparator is shown in Fig. 5.8. This topology has been chosen because it performed well in the reference design [11] and also provides more flexibility over the one-stage since it allows the amplification stage and the latch to be sized more or less independently.

The behavior of the circuit can be viewed as follows. When 'clk' is low, the 'an',

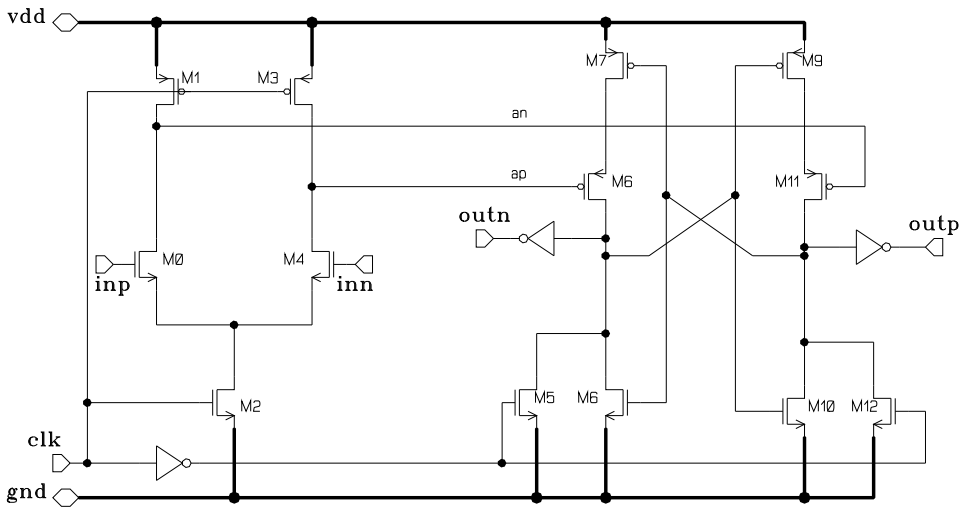


Fig. 5.8. Dynamic comparator

'ap' nodes are connected to the supply trough the transistors M1, M3. Thus, the total equivalent capacitance from the nodes 'an', 'ap' to the supply, formed by M1, M6 and M3, M11, is discharged. Both outputs of the latch are reset to zero volts by M0, M4. When 'clk' goes high, M0 and M4 start to work as current sources, feeding current into the previously discharged capacitors at the nodes 'an', 'ap'. The voltage at these nodes starts to decrease proportionally to the DC current, provided by M0, M4, and the capacitance from 'ap', 'an' to the supply. When the CM voltage at the nodes 'ap' and 'an' reaches a certain threshold level, the latch starts to regenerate the valid signal at the output. The comparator output depends on the ratio of the voltage change at the nodes 'ap' and 'an'. In turn, the ratio of this voltage change depends on the comparator input voltage.

Noise, offset and memory effect should be considered during the comparator design. Two approaches to the noise analysis of a dynamic comparator have been shown in [19] and [18]. In [18], the analysis is based on solving stochastic differential equations for different operating phases, whereas in [19], a linear time-varying model of a comparator is built and the contribution of every noise source is found after deriving Impulse Sensitivity Function. Both approaches give the same results. The following guidelines to minimize the noise of a dynamic comparator can be pointed out:

- The ratio W/L of the tail transistor M2 should be 2-6 times smaller than the ratio of the input differential pair M0, M4.
- Decreasing the overdrive voltage of the input M0, M4 transistors decreases noise.
- The input CM voltage has an optimum value for minimum noise.
- Slowing down the rise/fall time of the 'clk' signal decreases the noise.

Noise of the comparator is simulated using transient noise analysis. The input voltage is swept from several microvolts to several tens of millivolts. For each input voltage, a number of latch events occur. Due to noise in the circuit some decisions are 'wrong'. The 'wrong' decisions for every DC input voltage are counted. In the first approximation,

the distribution of the 'wrong' decisions must resemble a normal distribution since the source of error is thermal noise. Based on the collected statistics, the RMS value of the comparator noise can be found with:

$$Vn_{RMS} = \sqrt{k_1 v_{n1}^2 + k_2 v_{n2}^2 + k_3 v_{n3}^2 + \cdots + k_n v_{nn}^2} \tag{5.1}$$

where,
v_{nm}-input DC voltage at which k_m 'wrong' decisions occur.

The input referred noise of the comparator is estimated as $120\mu V$.

Since a comparator decision is related to the capacitance at the differential nets, any imbalance of the capacitance leads to an equivalent input DC offset. For example, it has been shown in [22] that mismatch at the latch output as small as 1fF can lead to the output offset of several tens of millivolts. Very symmetrical layout has been made to avoid any capacitance imbalance at the internal nodes of the comparator. Moreover, to avoid offset due to loading, two inverters have been placed as close as possible to the latch output. Also, transistors with a not minimum channel length of $100nm$ have been used to obtain a better matching. Post-layout Monte-Carlo simulation shows that 3σ offset is equal to $28mV$ with the mean value of $0.5mV$, which is due to systematic error in the layout.

Memory effects may appear if some of the capacitors are not reset to initial voltage during the reset mode. Transistors M5, M12 set the output voltage to a ground potential within the time $2/f_a$,where f_a is a frequency of the asynchronous loop. PMOS transistors M1, M3 set the supply voltage at the nodes 'ap' and 'an' during the reset.

5.6 The asynchronous logic

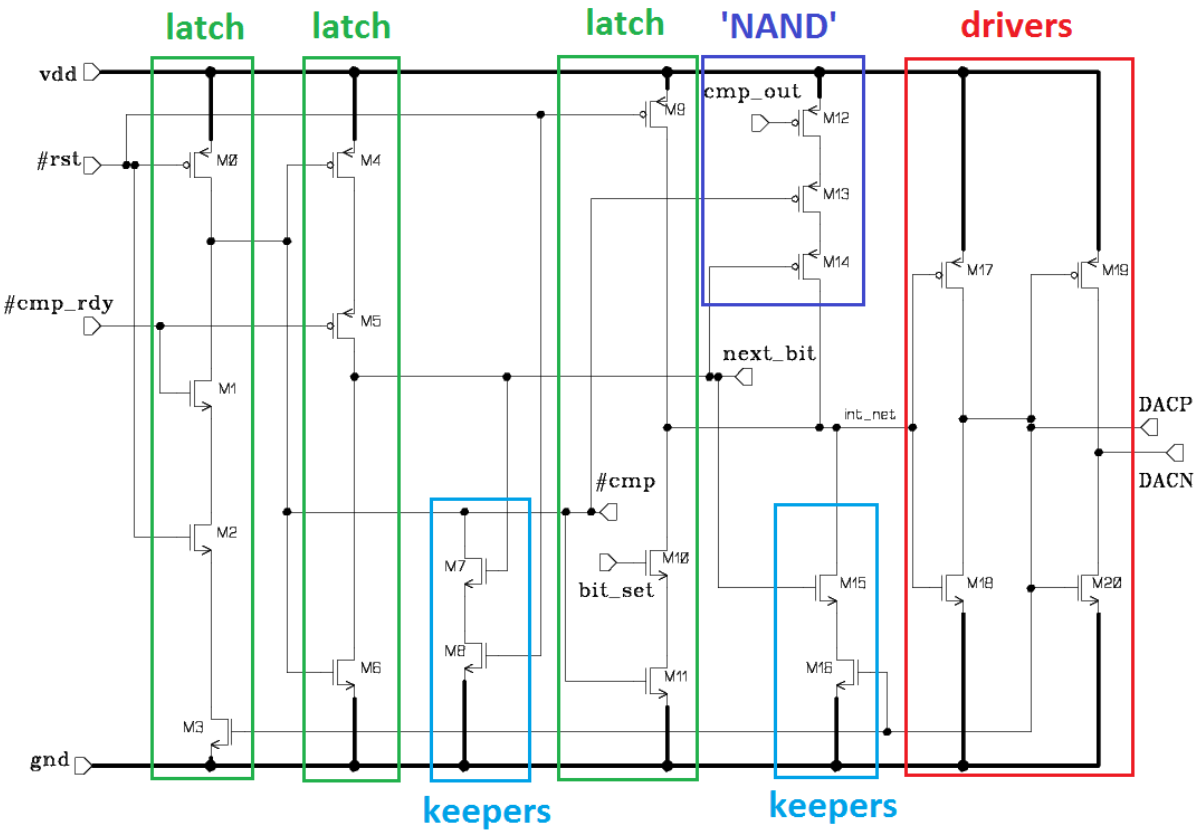


Fig. 5.9. Schematic of the digital slice

The circuit diagram of a digital slice is shown in Fig. 5.9. It consists of several blocks: the latches keep the states of the control signals, the keepers provide robustness of the circuit, the 'NAND' transistors perform a NAND logic function, changing the value of the 'int_net' from 0 to 1, and the drivers enhance the load-driving capability of the slice.

The description of the slice is given next and illustrated by the timing diagram in Fig. 5.10. Before starting the conversion process, the reset ('#rst') signal sets all nodes in the slice to the initial value: 'next_bit'=0, 'DACP'=0, 'DACN'=1, '#cmp'=1. Since 'next_bit' of the previous slice is connected to 'bit_set' of the following slice, 'bit_set' is also set to 0. When the previous bit has been found, the 'bit_set' signal of the current slice is set to 1 ,'DACP' changes to 1, M3 starts to conduct and '#cmp' goes from 1 to 0, initiating the comparison. As the comparator makes a decision, '#cmp_rdy' goes to 0, and the state of 'int_net' changes if the comparator output is 0, and remains 1 otherwise. If the comparator output is 0, the output of the slice goes back to the initial value ('DACP'=0, 'DACN'=1). The change of '#cmp_rdy' from 1 to 0 causes 'next_bit' to go to 1, turning the next slice on. The 'latch' signal is generated by the combinatorial logic, and '#cmp_rdy' by the AND gate at the comparator output (see the top level schematics of the asynchronous logic and the ADC in Fig. A.3 and A.2, respectively).'Next_bit' of the last slice rises the flag that conversion is ready.

Since the states of the signals '#cmp', 'next_bit', 'int_net' are kept in the loading capacitances, they can be easily lost due to leakage or parasitic coupling with the adjacent nets. To provide a reliable functionality of the circuit over PVT and in the presence of random mismatch, an additional capacitance might be added in between 'int_net' and ground [11] at the expense of larger area and speed degradation. A more efficient solution is to use 'keepers'. The minimum-sized transistors M15 and M16 sense the current state of the slice and short the net 'int_net' to ground if 'DACP'=1 and 'next_bit'=1. In the same way, the transistors M7 and M8 work for the '#cmp' net.

Another problem of any asynchronous logic is the racing effect. In this design, the problem may arise in the following points. Firstly, the DAC output should be set before the 'latch' signal has been generated to avoid settling errors. Careful simulations have been performed to fulfill this requirement. Secondly, the 'next_bit' signal in the slice should be generated after the 'cmp_out' signal reaches the gate of transistor M12. Otherwise, the DAC bit will not be set back if the comparator's decision is 0. To make sure this condition is satisfied, additional delay has been inserted between the AND gate at the comparator output and the asynchronous logic (see schematic of the ADC in Fig. A.2). Thirdly, if the 'int_net' net must be returned to the initial value after the comparator's decision, the speed of the transition should be fast enough to set 'int_net' to 1 before 'next_bit' changes from 0 to 1. If it is not the case, the 'int_net' net may get stuck somewhere at the 'grey' level, causing additional power consumption or even may leading to conversion errors. To avoid this, the widths of M12, M13 and M14 have been made considerably wide- $1.2\mu m$.

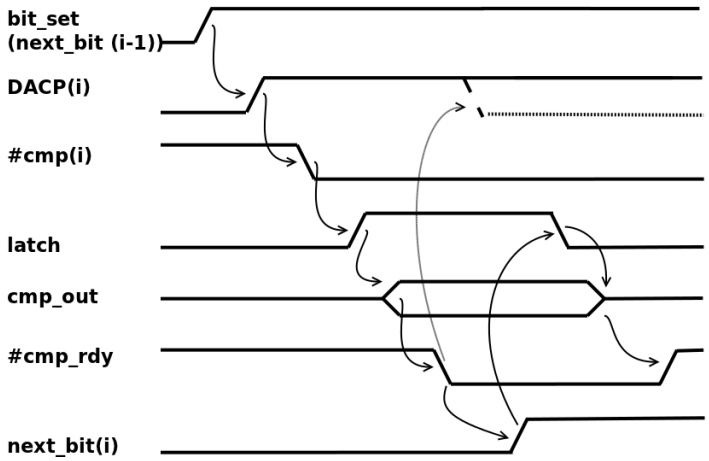


Fig. 5.10. Timing diagram of a digital slice

The first slice of the asynchronous logic is slightly different from the other ones. In contrast to other bits, to determine the MSB, the comparator makes a decision first and then the DAC output changes or keeps the initial value. The circuit diagram of the first slice is shown in Fig. 5.11. Since there is no need to change the slice output twice, the feedback from the 'DACP' output to the first latch in the slice (transistors M0-M3 in Fig.5.9) has been removed and M12 has been connected to vdd. The 'bit_set' input is reconnected to the comparator output and so, if it is high, the slice outputs (DACP'/'DACN') change their states. In order to prevent changes of 'DACP' and 'DACN' during the processing of the next bits, the gate of M11 is disconnected from the output of the first latch in the slice and connected to the '#cmp' output of the second slice.

If the sampled voltage is negative, 'int_net' does not go to 0 and remains equal to 1 during the whole conversion process. Additional positive charge is injected into 'int_net' when the '#rst' and 'next_bit' signals go to 1. As a result, the voltage at 'int_net' may

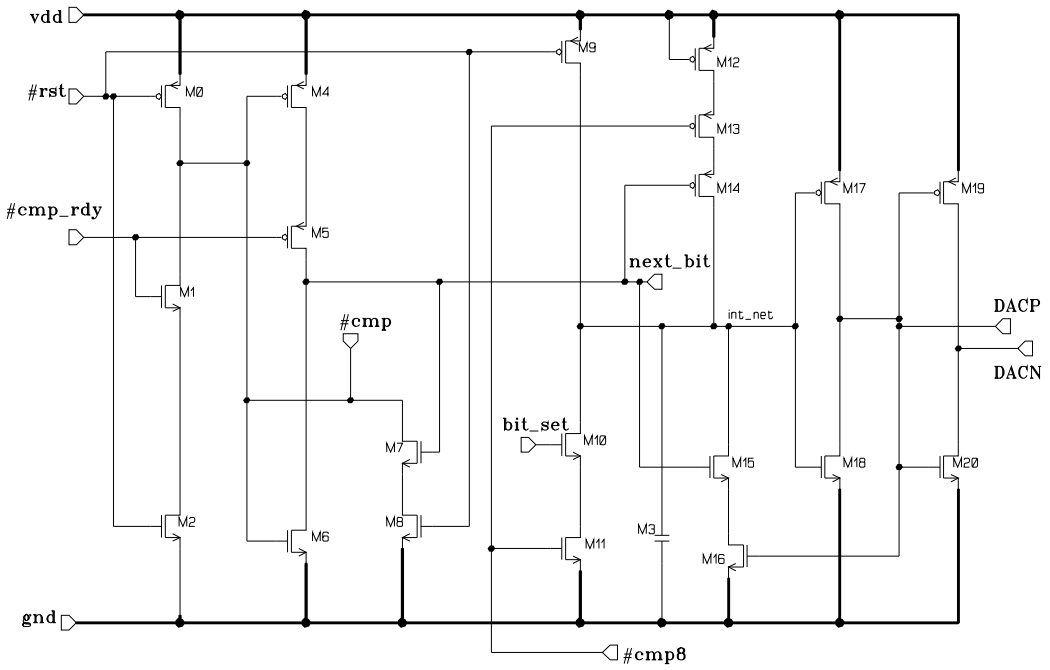


Fig. 5.11. The MSB digital slice schematic

exceed the supply voltage, potentially causing device failure in silicon. To make the net 'int_net' less sensitive to external interferences, the capacitor M3 has been connected between 'int_net' and ground.

The internal structure of the last slice is exactly the same as for bits 2-9, but the connection is slightly different. Since there is no need to return back the LSB in case of the wrong decision, the 'cmp_out' input of the slice is connected to the supply voltage instead of the comparator output.

The logic function of the 'latch' signal is shown in (5.2). The function is synthesized in a way to have only inverting gates for minimization of the number of transistors.

$$latch = \overline{\overline{\overline{(\overline{a_1+b_1})(\overline{a_2+b_2})(\overline{a_3+b_3})(\overline{a_4+b_4})}+ \overline{+(\overline{a_5+b_5})(\overline{a_6+b_6})(\overline{a_7+b_7})(\overline{a_8+b_8})}} + \overline{(\overline{a_9+b_9})(\overline{a_{10}+b_{10}})}}, \quad (5.2)$$

where, a_k and b_k- are the *#cmp* and *next_bit* signals of a digital slice for a bit k.

5.7 Floorplan

The layout of the ADC is shown in Fig. 5.12. The total area is $200\mu m \times 50\mu m$ including decoupling capacitors. The DAC occupies about 1/3 of the ADC core, whereas the area of the comparator and the logic is much smaller. To decrease unwanted coupling between the DAC and digital part through the substrate and also to avoid any crossing of the digital lines with the DAC output, the digital controller is placed at the opposite side of the ADC. The comparator is located close to the DAC to minimize length of the interconnects between them.

Excessive parasitics increase power consumption and decrease the digital controller speed and so the metal layers 4 and 5 have been used for routing.

The ring of decoupling capacitors around the ADC core performs two functions: to decouple the supply voltage of the ADC and to exclude any routing close to the ADC at the top level, since this may degrade accuracy of the capacitors in the DAC. The decoupling capacitors have been composed of a MOS and a fringe capacitor to increase the total capacitance per unit area.

There are three supply voltage domains used to minimize digital noise, and also for testing purposes during the evaluation: an analog domain for the DAC and two digital domains for the asynchronous logic and the output drivers. The supply and ground pins of the inverters represent DAC's reference voltage and so, they are connected to the analog domain.

Three separate DNWELLs for the DAC, the comparator, and the digital logic are used. Every DNWELL is surrounded by an N+ guard ring. A P+ guard ring separates the DAC from the comparator and the digital logic.

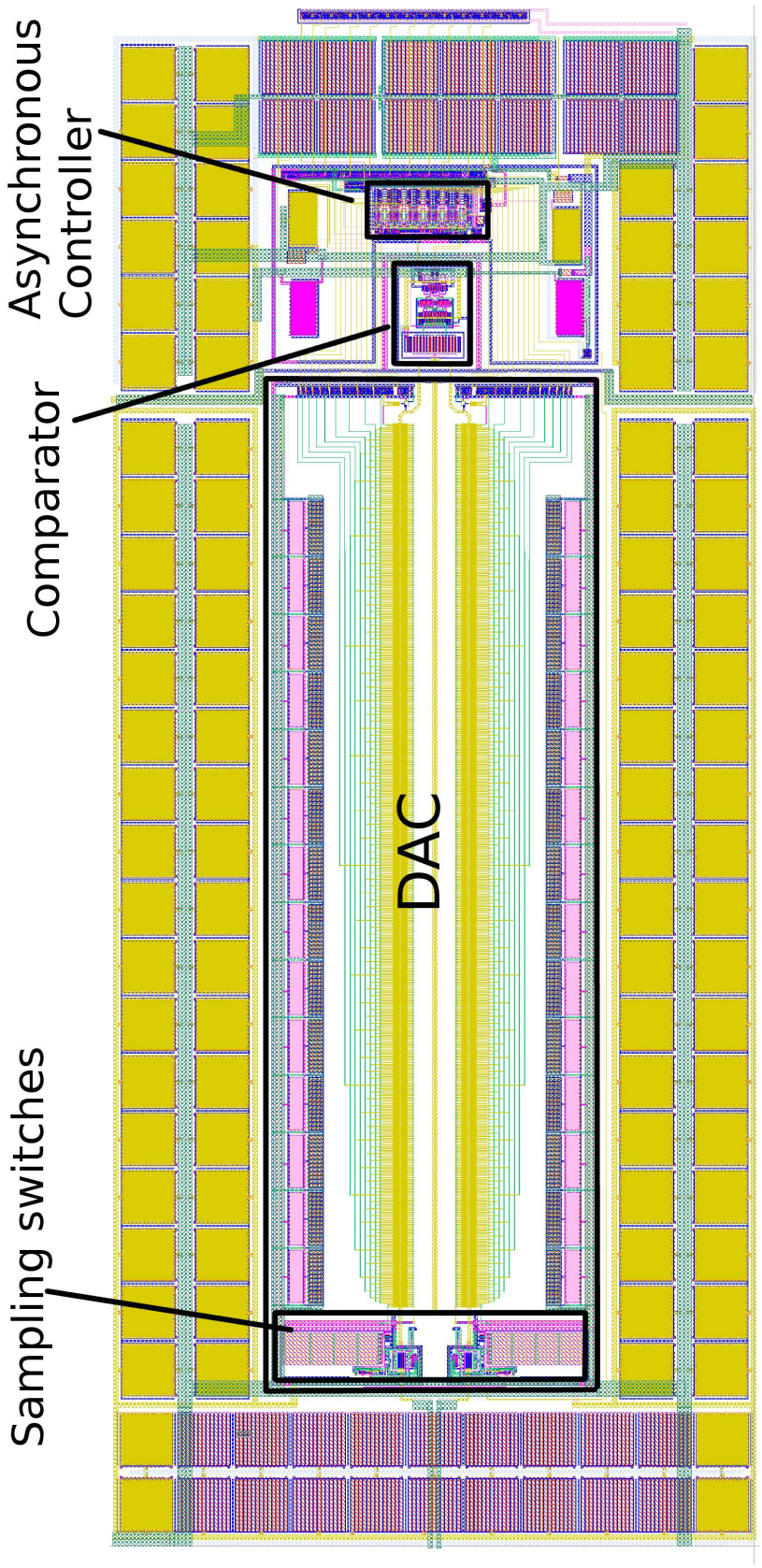


Fig. 5.12. ADC layout

6

Test chip

For the detailed evaluation of the ADC, a standalone version has been manufactured. A test chip has been designed and assembled in a HVQFN32(SOT617-1) package. Several issues related to standalone implementation and interfacing with outside world should be considered. These issues include the grounding and supply strategy, the output capacitance driving, packaging, ground and supply bounce, ESD protection and tiling.

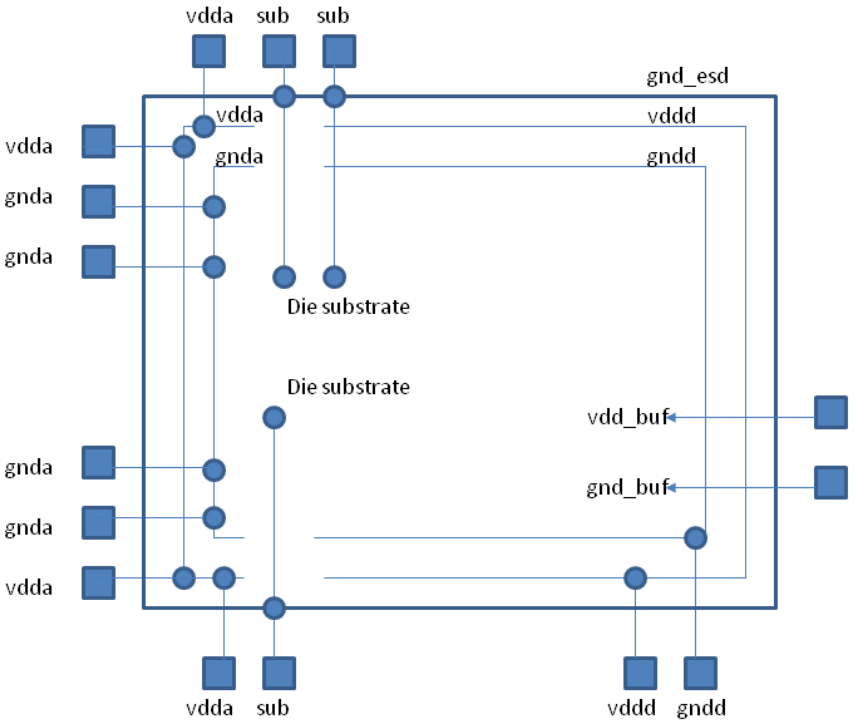


Fig. 6.1. Ground and VDD separation in the test chip

The padring is an essential peripheral structure around the die that includes bondpads,

several grounding and supply buses and ESD protection devices. In this design, standard analog I/O cells and VDD/GND pads has been used, provided by a foundry. The I/O cells include the built-in ESD protection diodes, which are reverse-biased during the normal operation and start to conduct only when an ESD event occurs. VDD/GND pads include an ESD clamp between the supply and ground buses. The ESD clamp is a MOS transistor, which operates in the snapback region when an ESD event occurs and which is turned off during normal operation. The rule of thumb is to keep the distance between two ESD-clamps no more than 1mm.

The proposed grounding strategy is shown in Fig. 6.1. There are three supply domains: the analog domain (vdda, gnda), the digital domain (vddd, gndd) and the output driver domain (vdd_buf and gnd_buf). The sensitive analog domain is located on the left side of the die while the digital domain is on the opposite side. The drivers use a separate domain in order to prevent switching currents from flowing through the signal ground in the chip. Secondly, separate domains will simplify the measurements since the current consumption of the output buffers should be excluded from the overall ADC power consumption. The padring includes two ground and one supply rings. Signal ground and supply are cut for domain separation. The outer ground ring is not cut to provide the proper path for the ESD currents during the ESD event between any two pads. No current flows through the *gnd_esd* bus during normal operation and so, it is connected to the substrate to provide a current-free substrate connection. Since the digital controller and the comparator are located in isolated NWELLs, the substrate is considered as 'quite'. The analog ground pads *gnda* and the substrate pads *sub* are connected to the diepad to provide a low-ohmic ground.

Due to the inductance of the bond wires has a high quality factor, considerable bounce appears on the ground and supply lines, caused by sharp current transaction during ADC operations. This disturbance of the supply lines spreads through the whole ADC due to various coupling capacitances and the substrate. The DAC output is especially vulnerable to this effect. To minimize bounce of the supply busses, a small resistance has been placed between the vdd/vdda pads and internal circuits, thereby decreasing the quality factor of the bond wires. Four pads are used for the analog ground, decreasing the overall impedance of the ground connection.

To estimate the effect of the ground and supply bounce on the ADC performance, additional simulation with bond wires has been performed. The bond wires are modeled with a $5nH$ inductor and a series resistance of 0.25Ω. According to simulation results, the voltage change at the DAC output is in the range of $60 - 80\mu V$, and FFT analysis shows no SNDR degradation.

The output drivers are implemented to drive a 50pF capacitance at 300 MHz frequency. Special care has been taken during layout to prevent latch-up due to the parasitic bipolar structures. The recommendation for preventing latch-up are given in the process design rules[23]:

- NMOS and PMOS transistors should be in different clusters and every cluster should be surrounded by unbroken guard ring.
- For NMOS transistors a P+ guard ring and for PMOS transistors an N+ guard ring are used

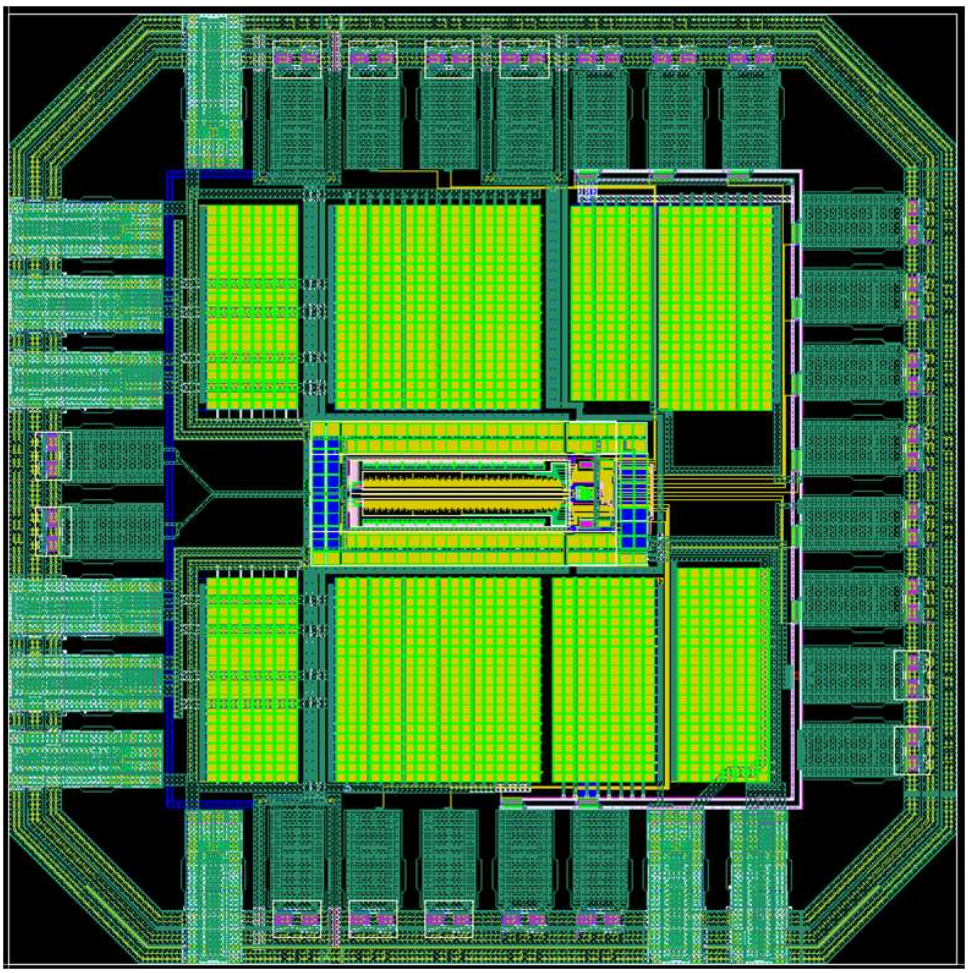


Fig. 6.2. Test chip

- The distance between PMOS and NMOS transistors should be not less than specified in the design rule manual.
- The width of the guard rings should be not smaller than the minimum size given in the design rule manual.
- N-well and substrate connections should be done with as many contacts as possible to provide a low-ohmic connection.

The screenshot of the test chip is shown in Fig. 6.2. The total area of the die with sealring (is not shown in Fig. 6.2) is $0.7 \times 0.7(mm)$.

Stress during the die sawing may affect the accuracy of the capacitors in the DAC. Since the strongest stress gradients occur at the die edges, the ADC is located in the middle of the die. The free space around the ADC is filled with decoupling capacitors. To satisfy the metal density rules, the die is covered by metal, poly and diffusion elements, except the DAC, since dummy metals can create an error in the capacitors ratios.

7

Measurements

7.1 PCB design

For evaluation of the standalone ADC, a PCB has been designed. The schematic of the PCB is given in appendix C. The purpose of the evaluation board is only to provide the necessary interfaces for the measurement equipment and so the design has been kept as simple as possible. Standard SMA connectors J2, J3 are used to connect the external signal source to the ADC inputs. Input capacitors C2 and C3 decouple the ADC input at DC. The values of these capacitors are chosen to have a low-pass -3dB bandwidth at 30 kHz. Resistors R3 and R4 provide a 50Ω matching with a signal source. 100pF capacitors C1 and C16 are connected with R3, R4 in parallel in order to provide a low impedance path for AC currents after switching of sampling switches. However, these capacitors and the bond wires can cause unwanted ringing. In this case, zero value resistors R1 and R2 should be replaced with $5 - 50\Omega$ resistors, or capacitors C1, C16 have to be removed.

There are three power connectors: one is for the analog supply, one is for the digital supply of the internal logic, and the other one for the digital supply of the ADC's internal buffers and external buffer U2. Separation of the supplies allows to set each voltage independently to monitor the current consumption of every domain and provides a better isolation between analog and digital parts of the ADC.

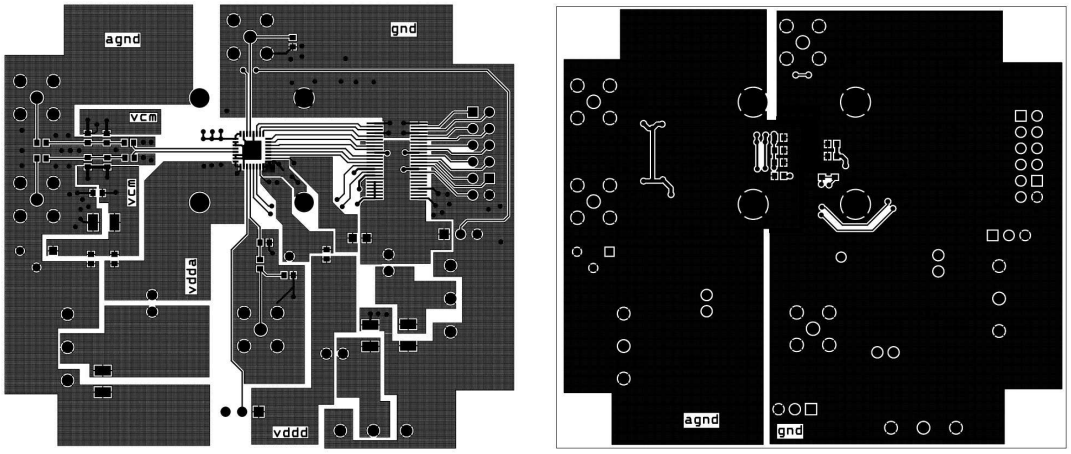
Common mode voltage at the ADC input is set by R22, R25. Decoupling capacitors C15 and C25 decrease the bandwidth at the common-mode node as much as possible to avoid CM noise.

Every supply pin of the ADC is decoupled with two capacitors 10uF and 0.1uF. The larger capacitor has more losses at high frequencies and is less efficient against the high frequency interference. On the other hand, a small capacitor cannot provide low impedance to ground at low frequencies, whereas a large capacitor does the job well. Thus, capacitors with different values broaden the filtration bandwidth.

There are two reasons to use an external interface buffer. The first one is to drive the long wire of a logic analyzer and the second one is to minimize loading of the ADC's buffers to decrease AC currents flowing through the IC.

A two layers PCB has been used. The analog and digital ground planes are located at the bottom layer and provide a low impedance path for return currents. The voltage supply polygons and signal wires have been routed on the top plate.

The PCB is separated to analog and digital parts . The analog part, which is located



(a) **(b)**

Fig. 7.1. Printed circuit board layout. Top layer (a) and bottom layer (b)

on the left side of the PCB (looking at the top layer, i.e. Fig. 7.1a), includes the input signal connectors, the analog supply connector and the CM reference. The digital supply connectors, the buffer, and the output digital bus are on the right side of the PCB. The digital and analog ground planes are connected together at one point under the ADC. Moreover, all analog traces have been routed above the analog ground plane, and all digital traces are above the digital ground plane to provide the shortest way for return currents.

The PCB has three power connectors to supply the analog (vdda), digital (vddd) and output buffers (vddbuf) separately.

7.2 Measurement setup

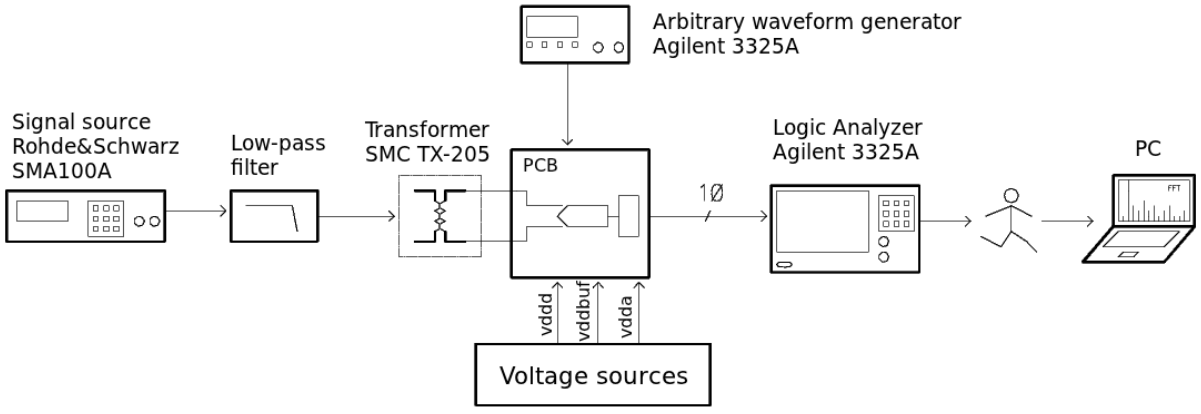


Fig. 7.2. Measurement setup

The measurement setup is shown in Fig.7.2. Low noise signal generator SMA100A provides the input signal for the ADC. A sharp low-pass filter with attenuation of 80 dB in

800 kHz bandwidth suppresses harmonic distortions of the signal generator. Transformer TX-205 converts the resulting single-ended signal into a differential one. An arbitrary waveform generator Agilent 3325A creates the sampling clock, which has a square shape with a non-50% duty-cycle. Logic analyzer Agilent 3325A writes the data from the ADC output for further post-processing in a PC.

7.3 Results

Parameter	**Value**	**Units**
SNDR	55.3	dB
ENOB	8.9	bits
SNR	56.5	dB
THD	-61.4	dB
SFDR	64.5	dBc
DNL	-1/0.8(-0.96/0.5)*	LSB
INL	-1.8/+1.9	LSB
Full-scale voltage	0.64	V
Current consumption	56	uA
FoM	5.9	fJ/conv

Table 7.1. Specification table

* if digital supply voltage $< 0.7V$

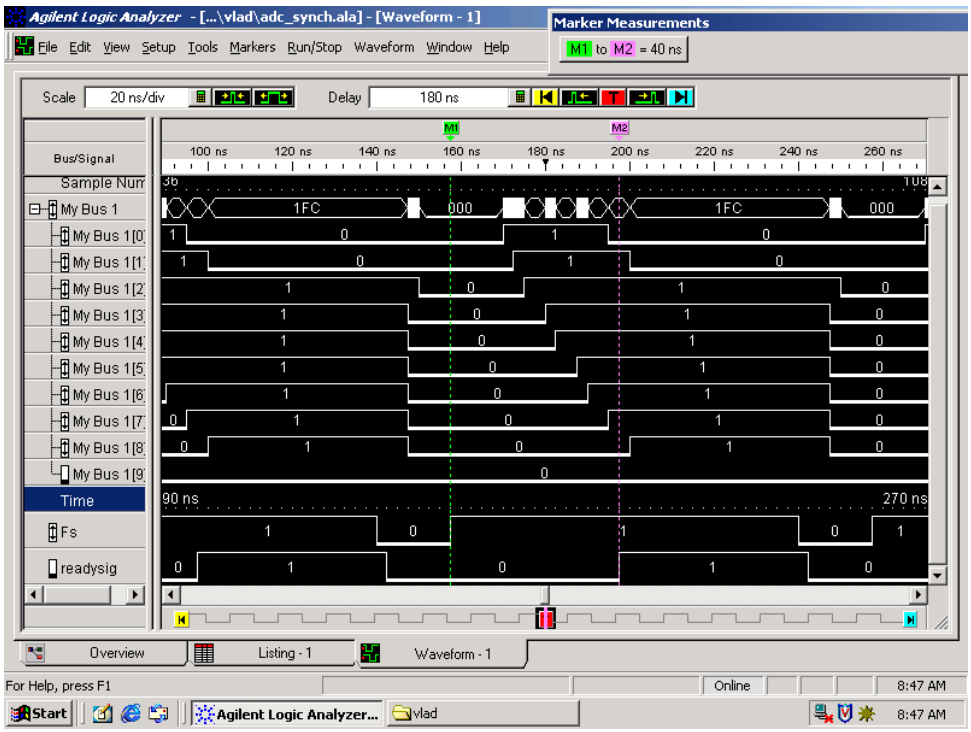
7.3.1 Digital controller speed

In Fig. 7.3 the time diagrams with 0.8V and 1.1V supply voltages are shown. 'Fs' signal is a sampling signal and 'readysig' is generated by the ADC when a conversion is ready. With a 0.8V supply the conversion time is 40ns, and with 1.1V is 22.5ns. If there is a signal at the ADC input, the conversion time changes from the given values by +/- 2ns, depending on the input voltage. The measured conversion time is somewhat larger than the actual one due to the propagation delay of the I/O output buffers and 2.5ns resolution of the Logic Analyzer.

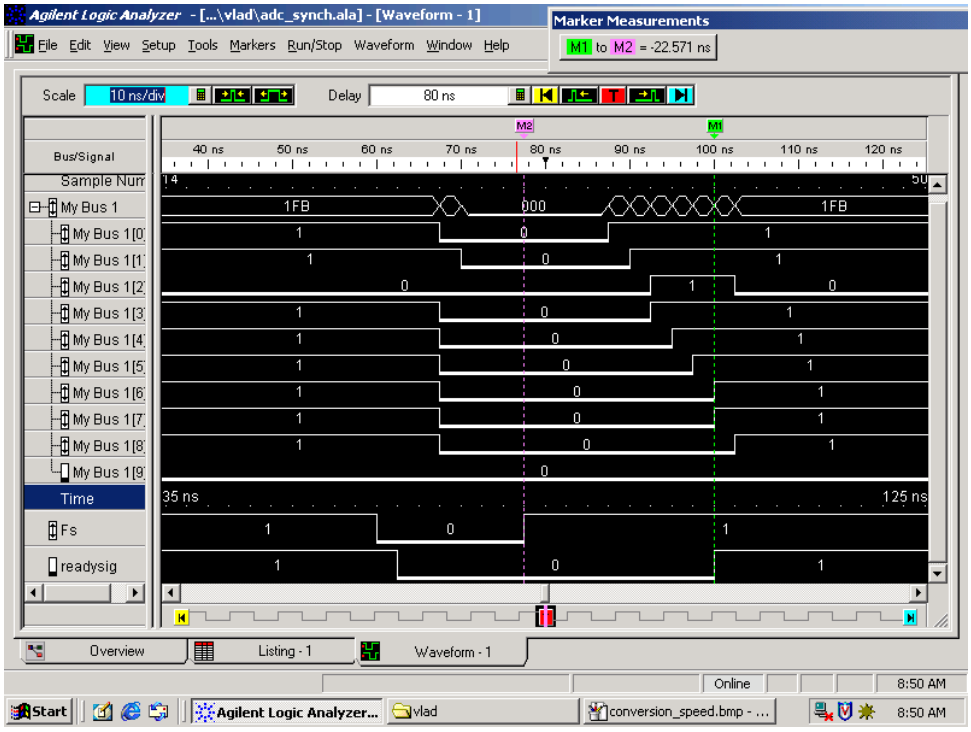
In Fig. 7.3 the last bit appears after the 'ready' signal due to delay of the buffers on the PCB since the 'ready' signal is measured directly at the ADC output, whereas the data is taken from the output of the buffers.

7.3.2 Noise floor

The ADC output with a zero input signal is shown in Fig. 7.4. The total integrated output noise is $228\mu V$. The quantization noise of the ADC is $Qn = V_{fs}/1024/\sqrt{12} = 184\mu V$. Therefore, with $V_{fs} = 640mV$ the excessive thermal noise is $135\mu V$.



(a)



(b)

Fig. 7.3. ADC output with DC input

7.3.3 Linearity

The DNL/INL curves are shown in Fig. 7.6. A missing code appears in the middle transaction, when the digital supply voltages are larger than 0.75V. Moreover, the DNL error increases towards the first and the last codes. In [24], a similar effect on DNL was observed due to poor PCB grounding [24]. However, in this design, the reason of a poor DNL is most likely due to coupling in the IC. This assumption is supported by the strong dependence of the DNL error on supply voltage, as it is shown in Fig. 7.6. The DNL pattern does not depend on the input frequency or the sampling frequency. Therefore, the sampling switch cannot be the source of the DNL degradation.

The INL shows a large mismatch of the MSB, MSB-1 and MSB-2 capacitors. INL and DNL plots have been measured with 10 dies and resulted in very similar shapes. Thus, it can be concluded that the INL/DNL error appears due to systematic mismatch, although there is no clear proof that would be supported by EDA tools.

7.3.4 Dynamic performance

The magnitude of the harmonic distortions decreases with increasing the amplitude of the input signal (see Fig. 7.7). This can be explained by observing the ADC transfer function (via the INL). Since the ADC input is biased to the midscale code, where the INL has the largest step, the distortions are noticeable even with small input amplitude. However, while the input amplitude increases, the signal starts to cover the larger part of the ADC transfer curve, which is more linear towards the first and the last codes. So, the magnitude of the harmonic distortions becomes smaller.

A large number of harmonics in the ADC spectrum is probably due to the high bandwidth of the charge-redistribution DAC. Moreover, the bandwidth of the DAC changes with input codes because the switches (the inverters) are not scaled proportionally to the binary-weighted capacitors. This may cause additional distortion.

A two tone ADC response with 1.674MHz and 1.586MHz input frequency is shown in Fig. 7.9.The intermodulation products appear at 1.762MHz and 1.498MHz. The IM3 product at 1.762MHz is 69.7 dBc.

There are several tones at low frequencies, which are due to the used signal generator: clearly seen a strong attenuation of these tones starting from 2MHz since the low-pass filter at the ADC input is used with a corner frequency at 2.1 MHz and attenuation 80dB from 2.1MHz to 2.9MHz.

7.3.5 Offset

Offset voltage of the 10 samples has been measured by setting the input amplitude to zero volts and observing the output code. The histogram of the output codes is shown in Fig. 7.10. The spread of the offset voltage is equal to 10LSB, or 6.25mV.

7.3.6 Current consumption

The measured rms supply current of the digital controller and the DAC are $41.5\mu A$ and $14\mu A$, correspondingly. Thus, the overall power consumption of the ADC with 0.8V is 44.4 μW.

The supply current scales linearly with sampling frequency as shown in Fig. 7.11. Slowing down the sampling rate twice, reduces the current almost by the factor of 2.

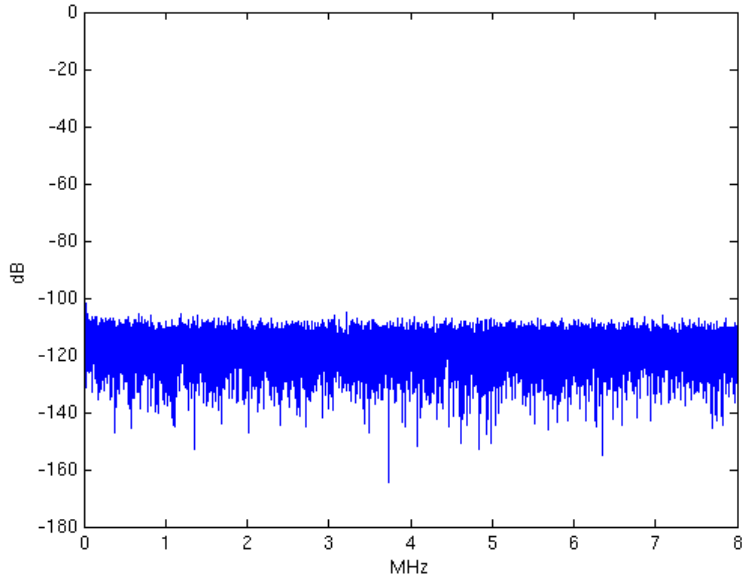


Fig. 7.4. Noise floor with zero input signal

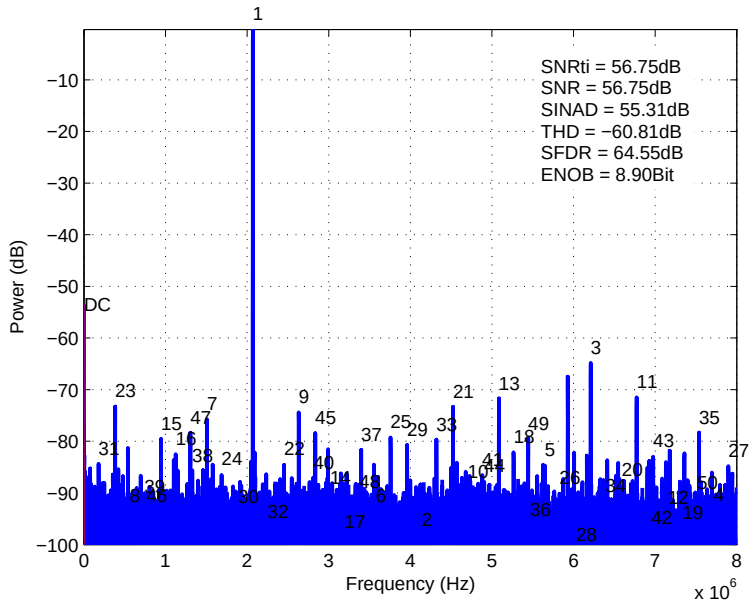


Fig. 7.5. ADC output spectrum

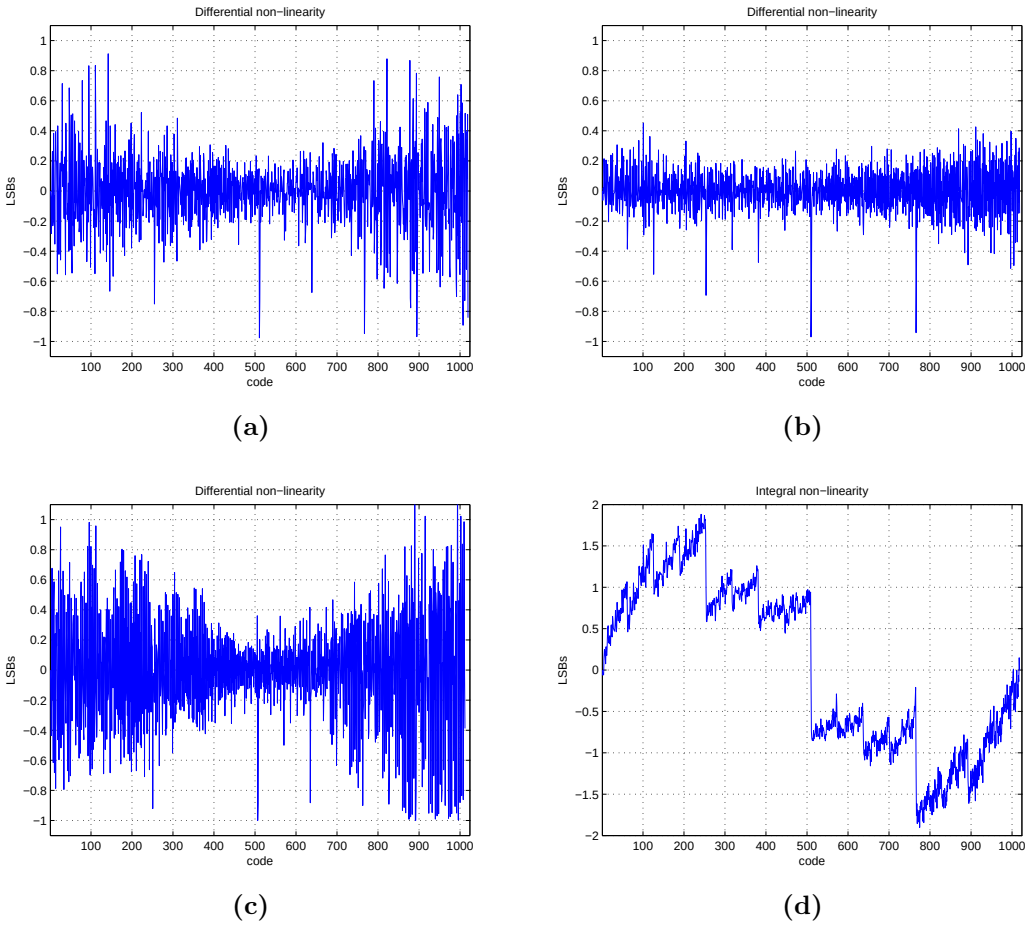


Fig. 7.6. DNL plots with a nominal supply voltages of 0.8V (7.6a), vddbuf=0.7V (7.6b), vddbuf=1.0V (7.6c), INL plot(7.6d)

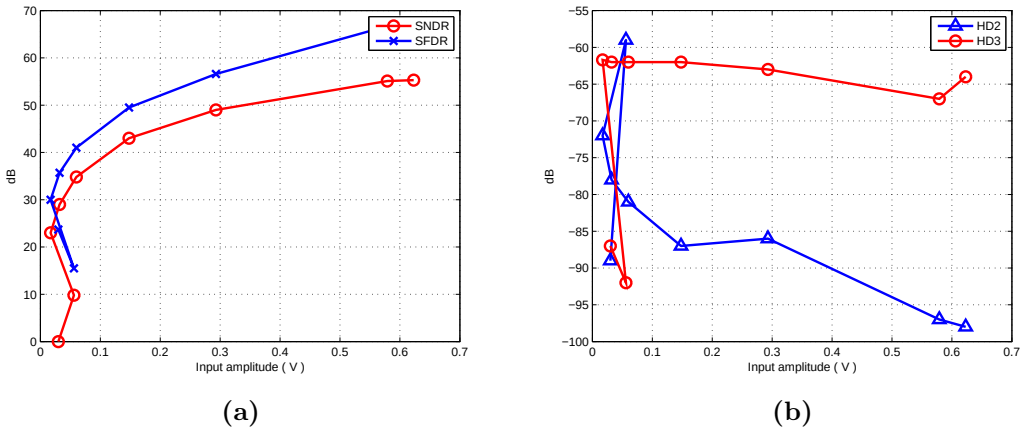


Fig. 7.7. SNDR/SFDR (a), 2nd/3rd harmonics(b) versus input amplitude

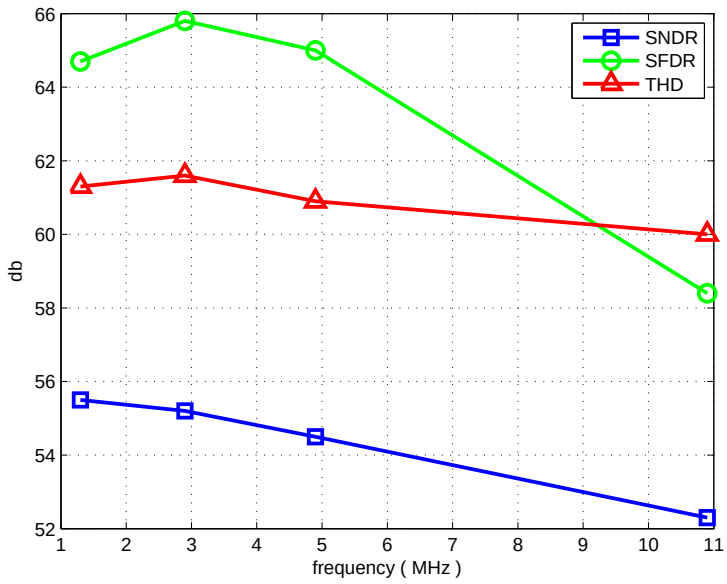


Fig. 7.8. SNDR, SFDR, THD versus input signal frequency

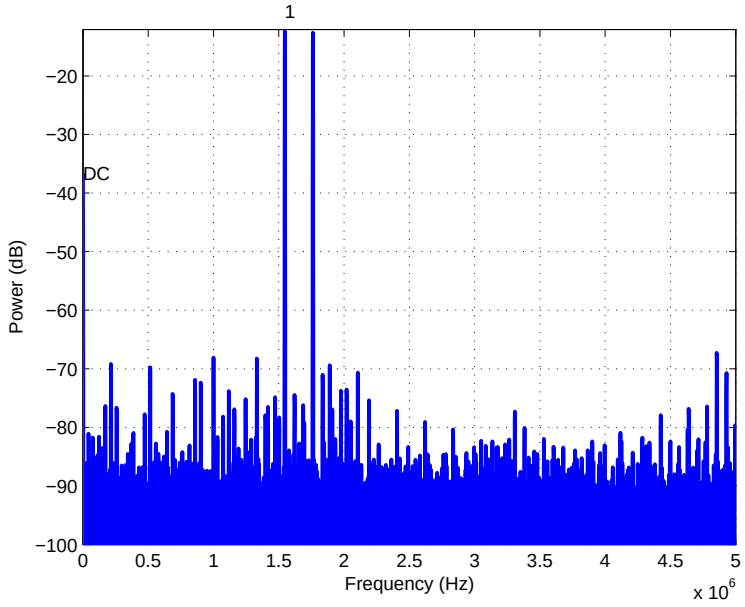


Fig. 7.9. A two-tone response

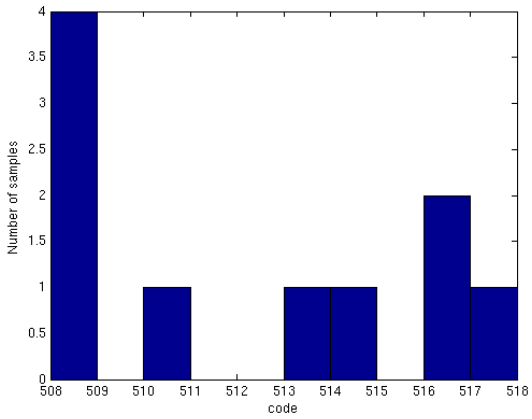


Fig. 7.10. Offset voltage histogram

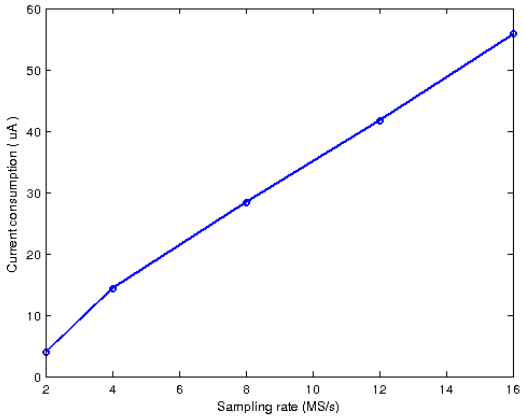


Fig. 7.11. Current consumption versus sampling rate

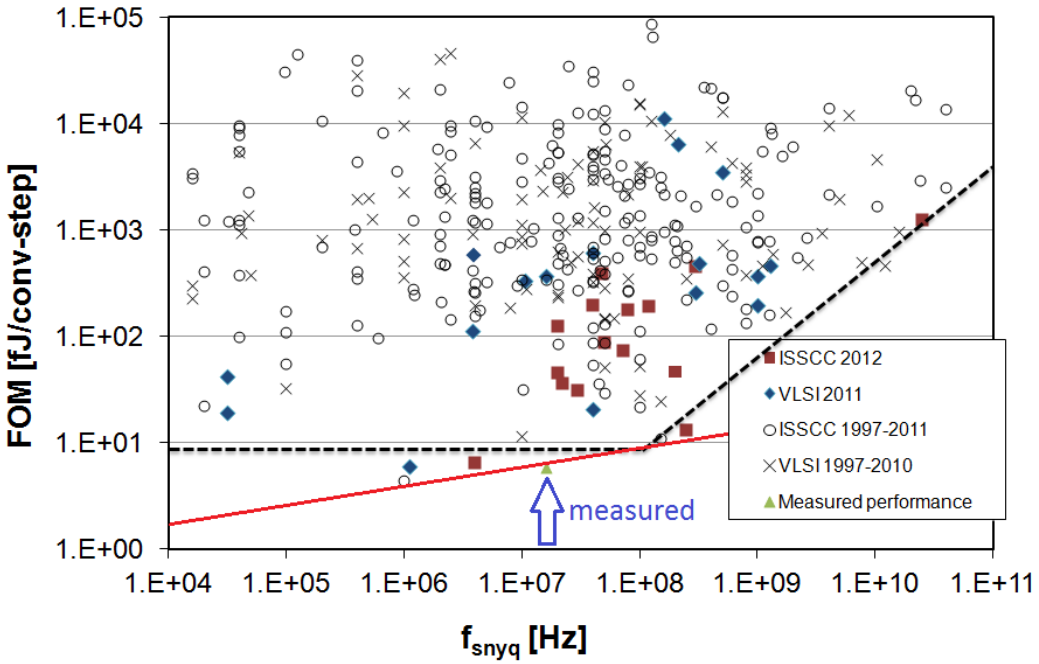


Fig. 7.12. Comparison with state-of-the art

	[25]	[26]	[9]	[27]	**This Work**
Process, nm	90	40	65	180	**45**
Resolution	10	10	10	10	**10**
Supply voltage, V	1.1	0.5	1	1	**0.8**
Sampling rate, MS/s	4	1.1	1.1	10	**16**
ENOB	9.4	7.5	8.75	9.1	**8.9**
SFDR, dB	61	58	no data	69	**64.5**
Power, uW	17.44	1.2	1.9	98	**45**
Area,mm^2	0.043	0.012	0.026	0.086	**0.01**
FoM	6.5	6.3	4.4	11	**5.9**

Table 7.2. Comparison with state-of-the art ADCs

8

Conclusions

In the presented work a 10-bit ADC for a low power transceiver has been successfully designed. The measured performance satisfies the given requirements. The concept of the proposed charge sharing technique has been proved.

The measured linearity degradation is larger than was predicted during the design due to the INL error. This error has a systematic nature and, most probably, cannot be found with the tools that has been used during the design since the absolute value of the error is in the range of 1-2fF.

The bandwidth of the DAC should be at least ten times larger than sampling rate in order to maintain the proper ADC operations. Due to the DAC non-linearity and its high bandwidth, the higher order harmonic distortions will appear at the ADC output, decreasing total linearity. The DAC bandwidth and the ADC resolution are not orthogonal parameters in this architecture and cannot be set separately. This can be a fundamental limitation if a high linearity is required.

The power efficiency of the ADC is comparable with state-of-the art. Moreover, for a given sampling frequency the FoM is the best.

In further work, trimming can be implemented to improve linearity and, consequently, total harmonic distortion. Since the INL error is caused by some systematic error, trimming can be done only once using software, without increasing the production cost. The DNL error can be decreased by improving the ADC grounding.

Appendix A

ADC Electrical circuits

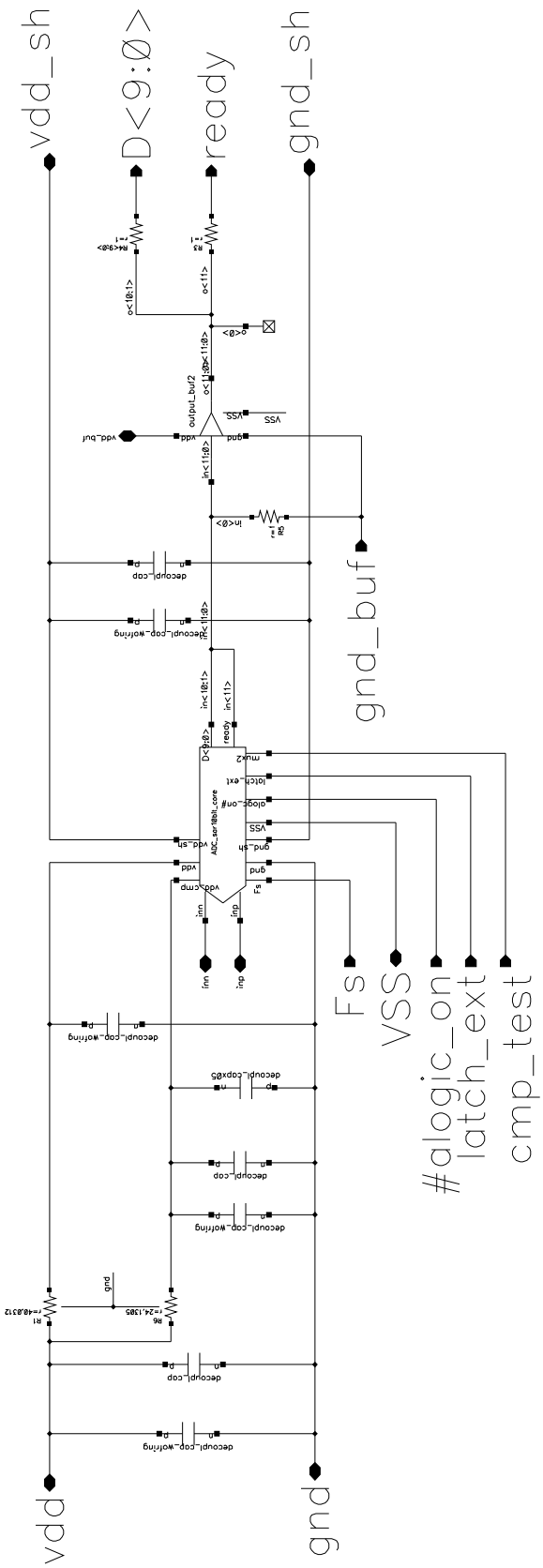


Fig. A.1. ADC top level schematic

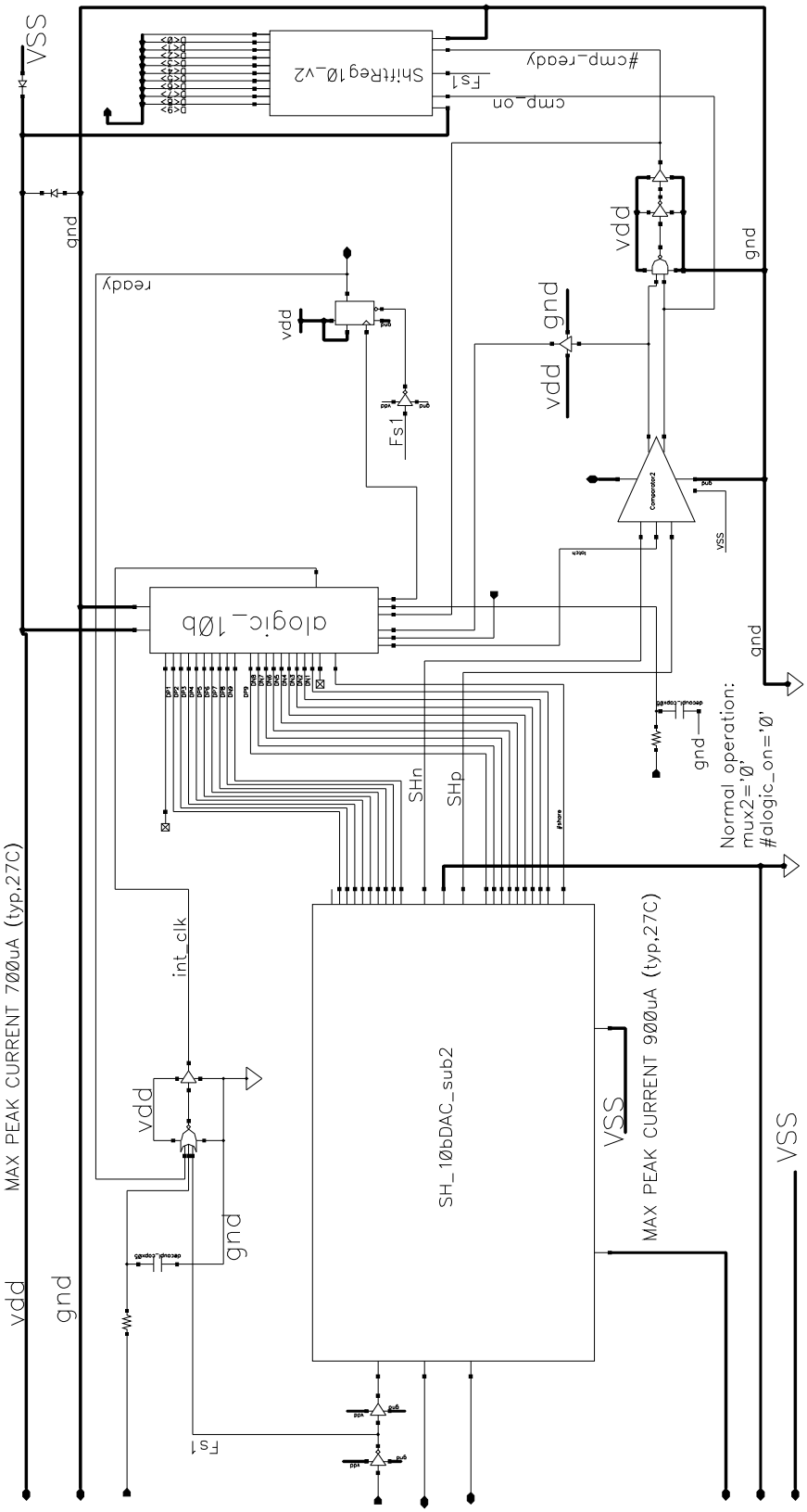


Fig. A.2. ADC core schematic

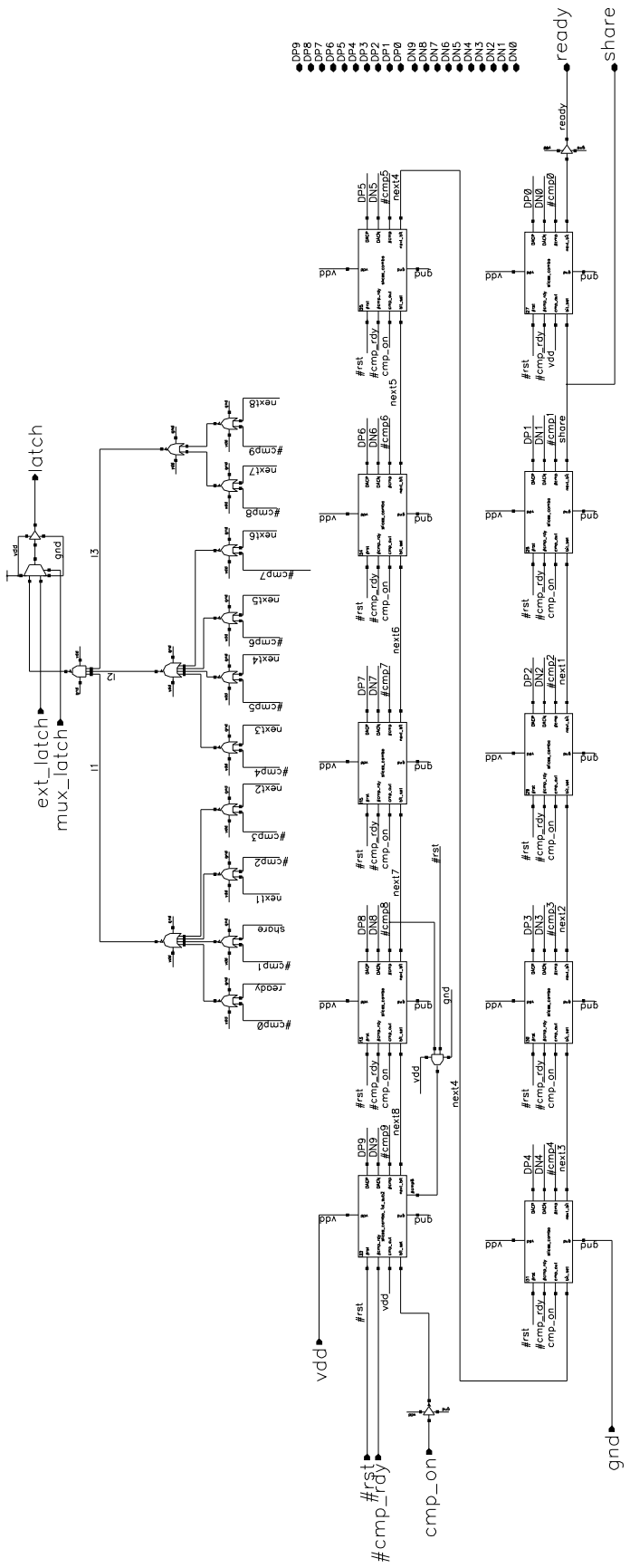


Fig. A.3. Asyncronous logic

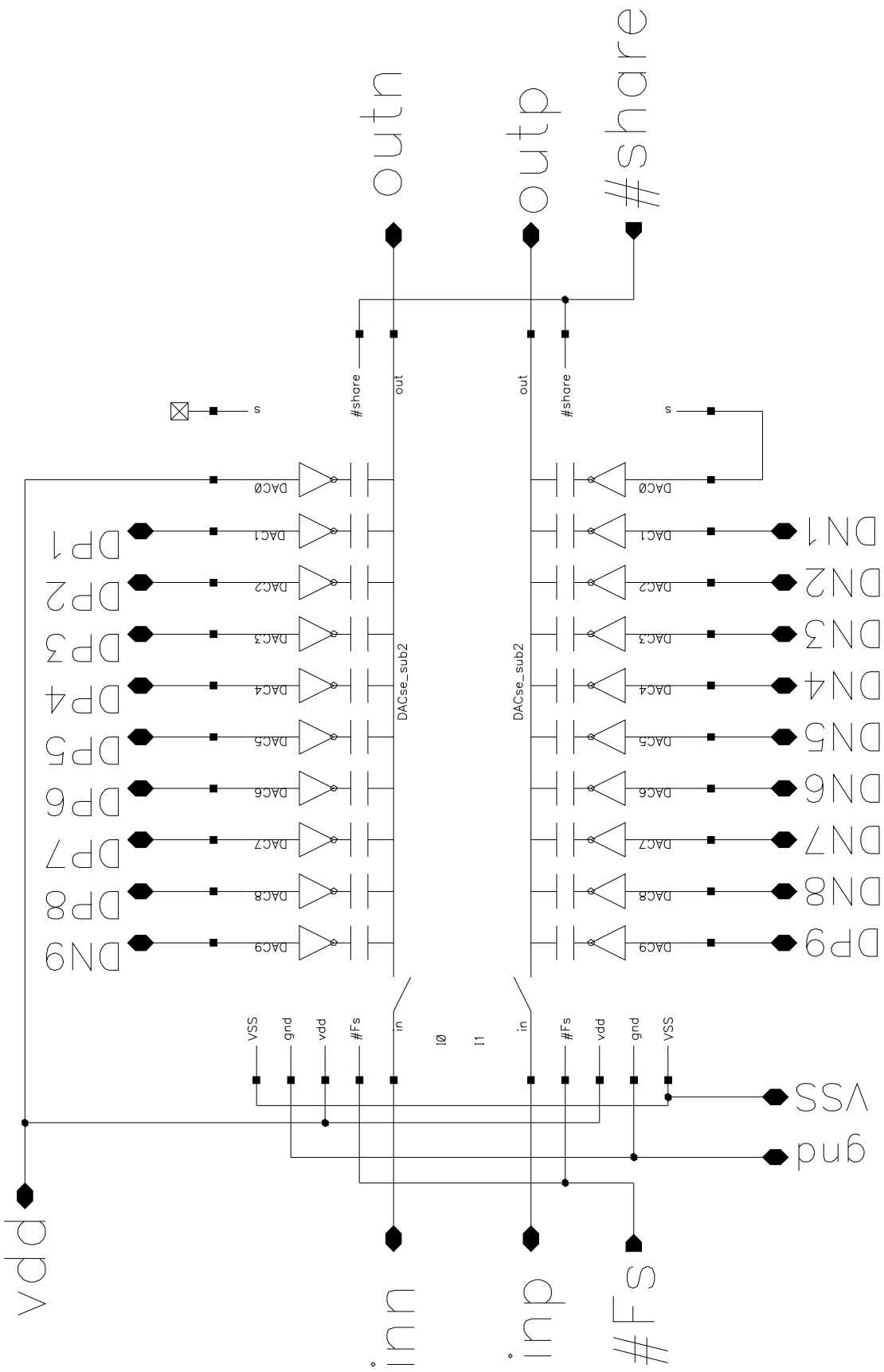


Fig. A.4. Differential DAC

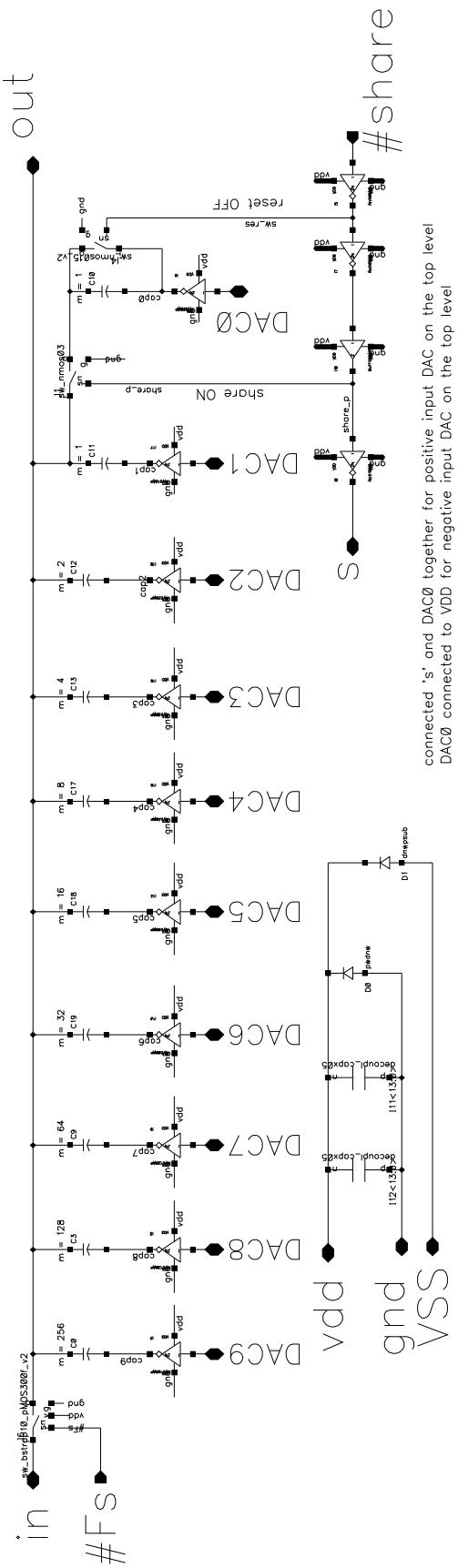


Fig. A.5. Capacitors bank with charge sharing

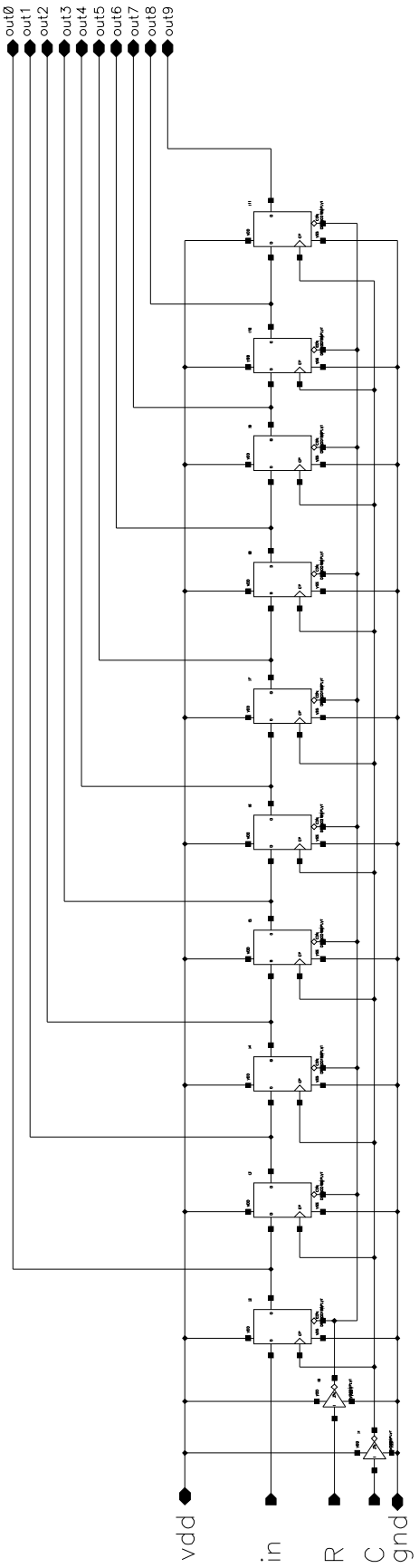


Fig. A.6. Shift register

Appendix B

Linearity simulation of the DAC with non-ideal coefficients

```
function [dec_code,nr_levels]=CrCapArr_chshar(C)
% The function returns normilized output voltage of a charge redistributing
% DAC with charge sharing.
%
% Charge sharing is modeled with LSB, toggling every cycle. The state
% of the LSB bit is controller by 'LSBflag' variable.
%
% C is an array of normilized capacitors.
% A vector with output values is returned to 'dec_code',
N=size(C); N=N(2);
nr_levels  = 2^N;
stat_error  =2;
LSB        = 1/(nr_levels+stat_error);
LSBflag=1;
dyn_error  = 1/(2*LSB+1);
den=sum(C);
dec_code=zeros(1,nr_levels);
for i=1:1:nr_levels
    str=dec2bin(i-1);
    s=size(str);
    s=s(2);
    a=N-s;
    for k=1:a
        str=strcat('0',str);
    end
    num=0;
    for k = 1:N
        if str(k)=='1'
            num=num+C(k);
        end
    end
    dec_code(i)=(num/den)+LSB*LSBflag*dyn_error; %eq. 4.9
    if LSBflag==0
        LSBflag=1;
    else LSBflag=0;
    end
```

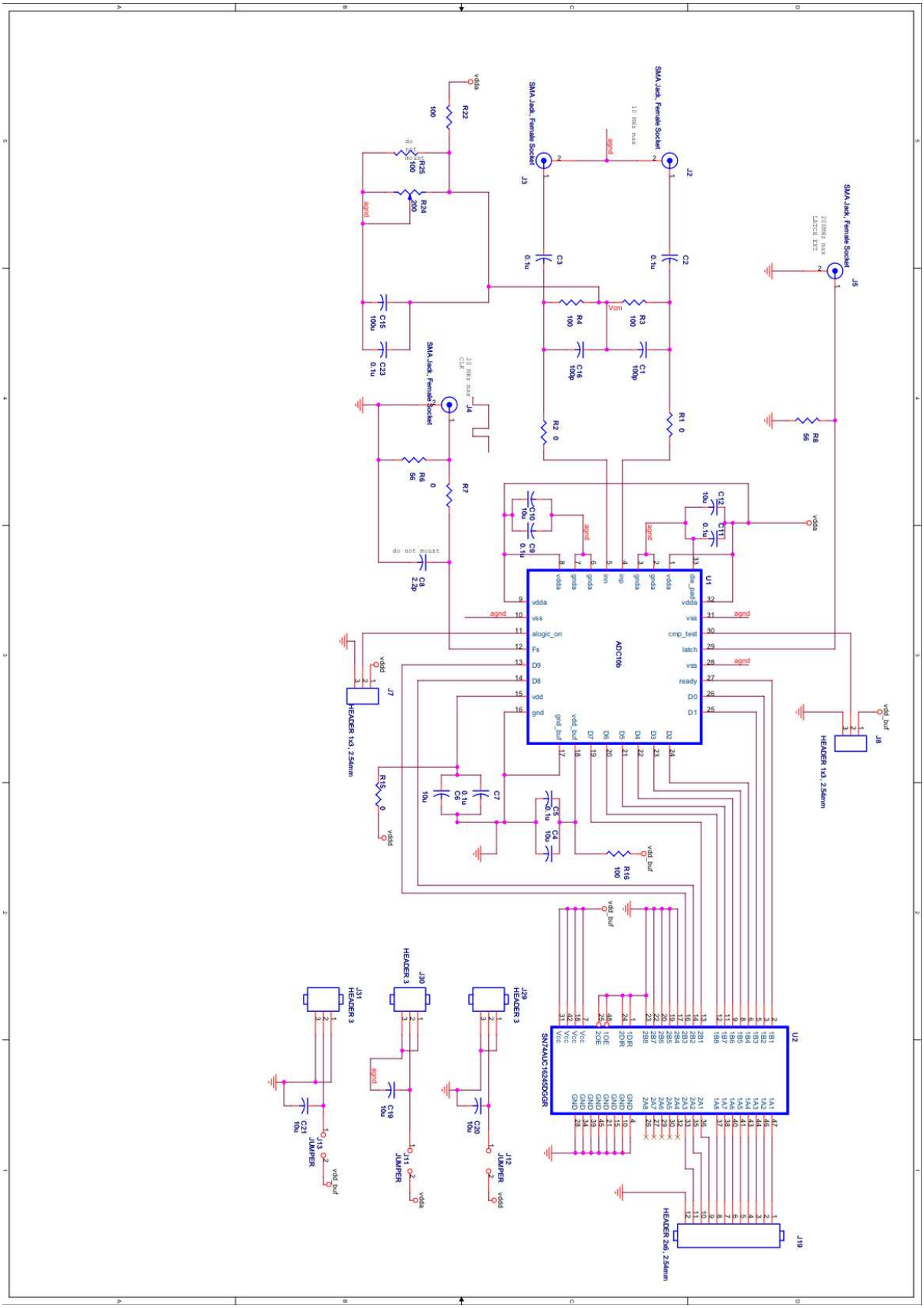
```
    clear str;
end
```

```
function [dec_code,nr_levels]=CrCapArr_chshar_dif(C1,C2)
%The function returns normilized output voltage of a differential charge... redistributing
% DAC with charge sharing.
[code_p,nr_levels]   = CrCapArr_chshar(C1);
[code_n,nr_levels]   = CrCapArr_chshar(C2);
code_p=code_p * 0.5; code_n=code_n * (-0.5);
dec_code = code_p-code_n ;
end
```

```
% The code predicts DNL/INL of a charge redistributing DAC with charge ... sharing using monte-carlo method
clc;close all;
MC_runs =50; % number of runs
maxDNL= zeros(1,MC_runs);
Cp= [256 128 64 32 16 8 4 2 1 1];
Cn=Cp;
N=size(Cp);N=N(2);
Ac=0.32; % matching coefficient ( %/sqrt(fF) )
unit_cap=0.5; %a unit capacitor value fF
sig=Ac/sqrt(unit_cap)/100; % a unit capacitor 1sigma
norm_sig=sig/unit_cap;
for a=1:MC_runs
    fprintf(' %f \n',a);
    C_mis=zeros(1,N);
    for k=1:N % setting random capacitors error
        C_mis_p(k)=sum(randn(1,Cp(k))*norm_sig+1);
        C_mis_n(k)=sum(randn(1,Cn(k))*norm_sig+1);
    end
    [dec_code_ideal, nr_levels] = CrCapArr_chshar_dif(Cp,Cn);
    [dec_code, nr_levels] = CrCapArr_chshar_dif(C_mis_p,C_mis_n);
    % ------------------------ INL calculation ------------------------------
    INL=zeros(0,nr_levels); DNL = INL;
    LSB=1/nr_levels;
    INL=(dec_code_ideal-dec_code)/LSB;
    INL=INL-(max(INL)-min(INL))/2;
%   plot(INL); hold on;
    %------------------------- DNL is a derivitive of INL-------------------
    for k=1:nr_levels-1
        DNL(k)=INL(k+1)-INL(k);
    end
%   figure(1); %   plot(DNL); hold on;
%   finding the largest absolute DNL value
    if abs(min(DNL))>max(DNL)
        maxDNL(a)=min(DNL);
    else
        maxDNL(a)=max(DNL);
    end
end
clc; figure(2); hist(maxDNL);
```

Appendix C

The ADC evaluation PCB


ADC10b
SN74AUC16245DGGR
SMA Jack, Female Socket
HEADER 3
HEADER 1x3, 2.54mm
HEADER 2x6, 2.54mm
JUMPER
vdda
vddd
vdd_buf
agnd
Vcm

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