M.Sc. Thesis

Monolithic Integration of LEDs and SPADs in Standard CMOS Technology for Optical Joystick Application

Nupur Lodha

Abstract

The interest in combining optical functionality with integrated circuits has grown in recent years due to reduced manufacturing costs and increased yields. However, the poor efficiency of silicon based light sources has been a major obstacle in achieving this goal. Single-photon avalanche diode technology has proven to be highly efficient in several low light applications. Owing to their extremely high sensitivity, integrated SPAD arrays have been successfully explored in this thesis for a novel design of monolithically integrated CMOS emitter and detector in a standard CMOS technology.

This work targets a specific consumer application of “Optical Joystick”. The designed emitter is a 16x16 array of avalanche mode silicon light emitting diodes. Four 16x20 arrays of silicon photomultipliers in each direction are designed to give light intensity information. Each pixel incorporates hot pixel elimination and temporal compression with a total area of 19x19 μm².

The realized SPAD has an extremely low median dark count rate (DCR) of 0.75 Hz per μm² of active area, and 20% photon detection probability (PDP) for wavelengths ranging from 450 nm to 550 nm at 2 V excess bias. The system has also been characterized for afterpulsing probability, crosstalk and timing jitter. Measurements involving click and angle detection with a mirror mounted on the top of the chip are included as a proof of concept of the joystick design. The designed chip has an area of 1.7x1.5 mm².
Monolithic Integration of LEDs and SPADs in Standard CMOS Technology for Optical Joystick Application

Thesis

submitted in partial fulfillment of the requirements for the degree of

Master of Science

in

Microelectronics

by

Nupur Lodha
born in Udaipur, India

This work was performed in:

Circuits and Systems Group
Department of Microelectronics & Computer Engineering
Faculty of Electrical Engineering, Mathematics and Computer Science
Delft University of Technology
The undersigned hereby certify that they have read and recommend to the Faculty of Electrical Engineering, Mathematics and Computer Science for acceptance a thesis entitled “Monolithic Integration of LEDs and SPADs in Standard CMOS Technology for Optical Joystick Application” by Nupur Lodha in partial fulfillment of the requirements for the degree of Master of Science.

Dated: 23-10-2012

Chairman: ______________________
prof.dr.ir. Edoardo Charbon

Advisor: ______________________
prof.dr.ir. Edoardo Charbon

Committee Members: ______________________
Frank Thus

__________________________
prof.dr.ir. Kofi Makinwa
Abstract

The interest in combining optical functionality with integrated circuits has grown in recent years due to reduced manufacturing costs and increased yields. However, the poor efficiency of silicon based light sources has been a major obstacle in achieving this goal. Single-photon avalanche diode technology has proven to be highly efficient in several low light applications. Owing to their extremely high sensitivity, integrated SPAD arrays have been successfully explored in this thesis for a novel design of monolithically integrated CMOS emitter and detector in a standard CMOS technology.

This work targets a specific consumer application of “Optical Joystick”. The designed emitter is a 16x16 array of avalanche mode silicon light emitting diodes. Four 16x20 arrays of silicon photomultipliers in each direction are designed to give light intensity information. Each pixel incorporates hot pixel elimination and temporal compression with a total area of 19x19 $\mu m^2$.

The realized SPAD has an extremely low median dark count rate (DCR) of 0.75 Hz per $\mu m$ of active area, and 20% photon detection probability (PDP) for wavelengths ranging from 450 nm to 550 nm at 2 V excess bias. The system has also been characterized for afterpulsing probability, crosstalk and timing jitter. Measurements involving click and angle detection with a mirror mounted on the top of the chip are included as a proof of concept of the joystick design. The designed chip has an area of 1.7x1.5 mm$^2$. 
Acknowledgments

Working on my thesis has been an extremely enriching experience for me. While the whole year was full of challenges and long working hours, it was also dotted with new learning experiences and support from a lot of people, whom I would like to thank hereafter.

First and foremost, I would like to thank my adviser, Prof. Edoardo Charbon for giving me a wonderful opportunity to work on an interesting research topic. His knowledge and experience contributed a great deal to my learning in the past one year, while his continuous motivation and encouragement boosted my confidence greatly.

I would like to thank Frank Thus for providing his support and guidance. I appreciate his help in providing all the necessary support to run this project smoothly. I would also like to thank Sebastien Mouy for contributing on a part of this project despite his own busy schedule. Without his help, it would have been very difficult to successfully complete the project in the given timeline. I would also like to acknowledge Ronald van der Werf for helping me in the layout phase, something I had no prior experience with. I am really grateful for his technical guidance and ideas.

I would like to acknowledge the contributions of all my team members for their valuable time and help. It was amazing to see how Dr. Yuki Maruyama could solve any experimental problem with such an ease, and his guidance provided a great kick start to my project. I would also like thank Shingo Mandai and Matthew Fishburn for helping me in the circuit design and layout phase. I appreciate their patience in answering all my questions, no matter how basic and meaningless they were sometimes. I would also like to acknowledge the guidance and numerous discussions with Chockalingam Veerappan, Vishwas Jain, Venkat Krishnaswami and Sachin Chadha. I am also grateful to Antoon Frehe for his technical support and Minaksie Ramsoekh for taking care of administrative work.

My whole-hearted appreciation and thanks goes to Sachin Chadha, whose constant support and encouragement over these last two years has motivated me to keep going through most of the difficult and frustrating times. His advise to delve deep into the problem helped me to understand the in-depth nuances of many concepts. I am also grateful to all my friends in Netherlands and India who provided me company during frequent bouts of home-sickness, and some great memories to be cherished for life.

I am truly amazed by the constant love and patience from my family all through my life. To venture out far from my own place, was not an easy move; and I was able to do so only because of my lovely parents and wonderful sisters. My heart-felt gratitude for all the sacrifices they made, their words of inspiration and their belief that I could excel.

Nupur Lodha
Delft, The Netherlands
23-10-2012
# Contents

Abstract v

Acknowledgments vii

1 Introduction 1
   1.1 Motivation ........................................... 1
   1.2 Joystick ............................................. 2
   1.3 Thesis contributions .................................. 3
   1.4 Design methodology .................................. 4
   1.5 Organization ........................................ 4

2 Background 5
   2.1 Conventional joystick architectures .................... 5
   2.2 UBA44000 optical joystick chip architecture .......... 6
      2.2.1 Functional overview ................................ 7
      2.2.2 Key Features ...................................... 9
   2.3 Silicon light emitting diode ............................ 9
   2.4 Single-photon avalanche diode ........................ 11
      2.4.1 Device structure ................................ 11
      2.4.2 SPAD performance parameters ..................... 12
      2.4.3 SPAD readout ..................................... 14
      2.4.4 Sensing .......................................... 15
      2.4.5 Quenching ....................................... 15
      2.4.6 Recharge ......................................... 16
   2.5 Summary .............................................. 17

3 System Design 19
   3.1 System objective ..................................... 19
   3.2 Preliminary measurements and experiments ............... 20
      3.2.1 Selection of SPAD device ......................... 20
      3.2.2 Selection of LED device .......................... 25
      3.2.3 Emission-detection experiment .................... 27
      3.2.4 SPADlight on time measurement ................... 27
   3.3 System specifications .................................. 28
   3.4 System architecture ................................... 30
      3.4.1 At the light source ............................... 30
      3.4.2 At the detector end ............................... 31
   3.5 System concepts ...................................... 33
      3.5.1 Hot pixel elimination .............................. 33
      3.5.2 Spatial and temporal compression .................. 34
      3.5.3 Spike filter ..................................... 37
   3.6 SPAD pixel ............................................ 37
3.7 Digital logic ............................................. 38
3.8 Interface between different modules .................. 40
3.9 System operation ...................................... 41
3.10 Design for testing .................................... 42
  3.10.1 SPADlight array .................................. 42
  3.10.2 SPAD array ...................................... 42
3.11 System overview .................................... 43
3.12 Summary ............................................. 44

4 Circuit Design & Implementation 45
  4.1 Chip architecture overview .......................... 45
  4.2 Categorization of internal modules ................. 46
  4.3 Emitter module ...................................... 46
    4.3.1 SPADlight pixel .................................. 46
    4.3.2 SPADlight cluster ................................ 47
    4.3.3 SPADlight driver ................................ 47
    4.3.4 Functional verification .......................... 47
    4.3.5 Layout of the cluster ........................... 50
    4.3.6 Building the array .............................. 51
  4.4 Detector module ..................................... 53
    4.4.1 SPAD pixel ...................................... 54
    4.4.2 Cluster level circuit ......................... 64
    4.4.3 Functional verification ........................ 64
    4.4.4 Full cluster layout implementation .......... 65
    4.4.5 Building SPAD array ........................... 67
    4.4.6 SPAD read-out system ......................... 67
    4.4.7 Spike filter .................................... 69
    4.4.8 Column decoder ................................. 71
  4.5 System integration .................................. 72
  4.6 Summary ............................................. 74

5 Results 75
  5.1 Testing methodology ................................ 75
  5.2 Hardware setup ..................................... 75
  5.3 Software ........................................... 76
  5.4 SPAD Measurement Results .......................... 77
    5.4.1 Breakdown Voltage .............................. 77
    5.4.2 Photon Detection Probability ................... 78
    5.4.3 Dark Count Rate ................................. 79
    5.4.4 Afterpulsing .................................... 81
    5.4.5 Crosstalk ....................................... 83
    5.4.6 SPAD Jitter ..................................... 83
  5.5 SPADlight Measurement Results ...................... 85
  5.6 System Measurement Results ......................... 85
    5.6.1 Intensity Measurement .......................... 85
    5.6.2 Tilt Measurement ............................... 86
<table>
<thead>
<tr>
<th>Figure</th>
<th>Description</th>
<th>Page</th>
</tr>
</thead>
<tbody>
<tr>
<td>1.1</td>
<td>UBA44000 Optical Joystick</td>
<td>2</td>
</tr>
<tr>
<td>1.2</td>
<td>Optical Joystick: Principle</td>
<td>3</td>
</tr>
<tr>
<td>2.1</td>
<td>UBA44000 chip cross-section</td>
<td>6</td>
</tr>
<tr>
<td>2.2</td>
<td>Functional overview of UBA44000</td>
<td>7</td>
</tr>
<tr>
<td>2.3</td>
<td>Band structure of silicon with an indirect bandgap of 1.1 eV, and GaAs with a direct bandgap of 1.4eV</td>
<td>10</td>
</tr>
<tr>
<td>2.4</td>
<td>I-V characteristic and gain of SPAD in Geiger mode of operation</td>
<td>12</td>
</tr>
<tr>
<td>2.5</td>
<td>Device Structure of SPAD</td>
<td>12</td>
</tr>
<tr>
<td>2.6</td>
<td>Voltage at the cathode upon avalanche breakdown (top), and digital signal at the output of inverter (below)</td>
<td>15</td>
</tr>
<tr>
<td>2.7</td>
<td>SPAD Operation in Passive Mode</td>
<td>15</td>
</tr>
<tr>
<td>2.8</td>
<td>SPAD Operation in Active Mode</td>
<td>16</td>
</tr>
<tr>
<td>2.9</td>
<td>Passive Quenching with Active Recharge</td>
<td>17</td>
</tr>
<tr>
<td>3.1</td>
<td>SPAD2</td>
<td>21</td>
</tr>
<tr>
<td>3.2</td>
<td>SPAD4</td>
<td>22</td>
</tr>
<tr>
<td>3.3</td>
<td>SPAD7</td>
<td>23</td>
</tr>
<tr>
<td>3.4</td>
<td>SPAD8</td>
<td>24</td>
</tr>
<tr>
<td>3.5</td>
<td>Comparison of photon detection probability for different SPADs with 4μm active diameter at V_E=2V.</td>
<td>24</td>
</tr>
<tr>
<td>3.6</td>
<td>Comparison of dark count rate for different SPADs with 4μm active diameter at room temperature.</td>
<td>25</td>
</tr>
<tr>
<td>3.7</td>
<td>Comparison of brightness values for different devices</td>
<td>26</td>
</tr>
<tr>
<td>3.8</td>
<td>SPADlight(p+)</td>
<td>26</td>
</tr>
<tr>
<td>3.9</td>
<td>Emission-detection experiment</td>
<td>27</td>
</tr>
<tr>
<td>3.10</td>
<td>Graph indicating on-time of SPADlight</td>
<td>28</td>
</tr>
<tr>
<td>3.11</td>
<td>Minimum power needed to attain an SNR = 1 for various reflectivities.</td>
<td>31</td>
</tr>
<tr>
<td>3.12</td>
<td>SPADlight cluster with driver</td>
<td>31</td>
</tr>
<tr>
<td>3.13</td>
<td>Timing diagram</td>
<td>32</td>
</tr>
<tr>
<td>3.14</td>
<td>Analog SiPM</td>
<td>33</td>
</tr>
<tr>
<td>3.15</td>
<td>Digital SiPM</td>
<td>33</td>
</tr>
<tr>
<td>3.16</td>
<td>DCR cumulative probability for 3V excess bias at room temperature in 0.35 μm CMOS technology.</td>
<td>34</td>
</tr>
<tr>
<td>3.17</td>
<td>Hot pixel elimination technique</td>
<td>34</td>
</tr>
<tr>
<td>3.18</td>
<td>Spatial compression with OR gate tree</td>
<td>35</td>
</tr>
<tr>
<td>3.19</td>
<td>Afterpulsing probability as a function of dead time</td>
<td>36</td>
</tr>
<tr>
<td>3.20</td>
<td>Temporal compression with monostable</td>
<td>36</td>
</tr>
<tr>
<td>3.21</td>
<td>Block diagram of the two compression schemes working in tandem</td>
<td>37</td>
</tr>
<tr>
<td>3.22</td>
<td>Block diagram of spike filter</td>
<td>37</td>
</tr>
<tr>
<td>3.23</td>
<td>Block diagram of the SPAD pixel</td>
<td>38</td>
</tr>
<tr>
<td>3.24</td>
<td>Block diagram of the digital logic</td>
<td>38</td>
</tr>
</tbody>
</table>
3.25 Block diagram of the complete system ........................................... 43
4.1 Architecture of SPADlight pixel ..................................................... 47
4.2 SPADlight cluster ........................................................................... 48
4.3 Driver for SPADlight cluster .......................................................... 48
4.4 Simulation model for SPADlight ...................................................... 49
4.5 Simulation result of SPADlight cluster ............................................ 49
4.6 SPADlight pixel without PMOS clamp ............................................ 50
4.7 SPADlight pixel with PMOS clamp .................................................. 51
4.8 Layout of SPADlight cluster ........................................................... 51
4.9 Layout of SPADlight array ............................................................... 52
4.10 Resistive network for calculating IR drop ....................................... 53
4.11 Layout of power rails. The power rail checker was designed to keep worst
case IR drop within 62.5 mV for \( V_{OP} \) and 80 mV for GND. ............... 54
4.12 Passive quenching and recharge ..................................................... 55
4.13 Change in resistance with increasing length for \( V_{GS} = 0.7 \) V .......... 56
4.14 Change in resistance with increasing \( V_{GS} \) for length = 160 nm ........ 57
4.15 Inverter based latch ..................................................................... 58
4.16 Switches for enabling/disabling quenching transistor ....................... 59
4.17 Row-column approach for writing masking data to 1 bit memory .......... 59
4.18 Monostable architecture ................................................................. 60
4.19 Change in resistance with increasing MBIAS for length = 320 nm ...... 61
4.20 Different pulse widths in 1-10 ns range with programmable monostable 61
4.21 Pixel disable logic ......................................................................... 62
4.22 SPAD pixel architecture ................................................................. 63
4.23 SPAD cluster architecture .............................................................. 64
4.24 Simulation model for SPAD ........................................................... 64
4.25 Simulation result of SPAD cluster .................................................. 65
4.26 Metal stack for CMOS 140 nm process ......................................... 66
4.27 Layout of SPAD cluster ................................................................. 66
4.28 Layout of SPAD array .................................................................... 67
4.29 Layout of power rails for SPAD array ............................................. 68
4.30 Read out system for SPAD array .................................................... 69
4.31 Conventional spike filter ............................................................... 70
4.32 Designed spike filter .................................................................... 71
4.33 Floor plan of the complete system ................................................. 72
4.34 Layout of the complete system ...................................................... 73

5.1 Schematic diagram of the evaluation board ....................................... 76
5.2 Hardware setup for evaluation ....................................................... 76
5.3 Snapshot of the designed software for operating the chip. ................. 77
5.4 Variation in breakdown voltage of 1 pixel with temperature - two different methods are compared for \( V_{BD} \) estimation. ...................... 78
5.5 PDP as a function of wavelength for 4 different excess bias voltages. ... 79
5.6 Distribution of DCR with respect to normalized pixel count. The measurement was performed at \(-40^\circ C, 25^\circ C\) and \(65^\circ C\) at \( V_E = 2V \). ..... 80
5.7 Median DCR as a function of temperature for different excess bias voltages. 81
5.8 Median DCR as a function of excess bias voltage for different temperatures. 81
5.9 Effect of masking on PDE and DCR. The measurement was performed at −40°C, 25°C and 65°C. 82
5.10 Inter-avalanche time measurement at 25 ns dead time. The afterpulsing probability is negligible. 82
5.11 Optical crosstalk measurement - count-rate based method. 83
5.12 Measurement setup for SPAD jitter. 84
5.13 Timing jitter for different excess bias voltages with single pixel enabled. 84
5.14 Comparison of timing jitter at 2 V excess bias before and after enabling complete SPAD array. 84
5.15 Sensor count rate as a function of SPAD light power consumption. 85
5.16 Experimental setup for measuring intensity. 86
5.17 Change in measured light intensity with respect to the distance of the mirror from the chip. 86
5.18 Experimental setup for measuring tilt. 87
5.19 Increasing counts in the top direction array and decreasing counts in the bottom direction array for positive tilt. 87
5.20 Measured count difference as a function of tilt for different distances of the mirror from the chip. 88
5.21 Chip Photomicrograph. 88

A.1 Bonding diagram of the chip for DIL40 package. 95
List of Tables

<table>
<thead>
<tr>
<th>Table</th>
<th>Title</th>
<th>Page</th>
</tr>
</thead>
<tbody>
<tr>
<td>3.1</td>
<td>Relative comparison of performance parameters for different SPADs</td>
<td>23</td>
</tr>
<tr>
<td>3.2</td>
<td>System specifications</td>
<td>29</td>
</tr>
<tr>
<td>6.1</td>
<td>Optical joystick performance summary</td>
<td>92</td>
</tr>
<tr>
<td>A.1</td>
<td>Chip pin list description</td>
<td>96</td>
</tr>
<tr>
<td>B.1</td>
<td>I2C register map</td>
<td>97</td>
</tr>
</tbody>
</table>
Introduction

1.1 Motivation

The integration of electronic and photonic devices on a single platform has been elusive for a long time because of inherent limitations of the available platforms. While the silicon platform provides high performance electronic devices, photonic capabilities are quite limited due to the lack of active photonic devices, a major reason being that silicon does not emit light efficiently at room temperature since it is an indirect band-gap semiconductor. The III-V platform, on the other hand, lacks in high density integration of electronic devices while supporting active photonic devices. Various issues have prevented the development of monolithically, inherently photo-sensing and emitting optoelectronic integrated circuits (OEICs) until today: incompatible process steps and large number of dislocations when III-V compounds are grown on silicon [1]. This fact, in combination with the costs associated with packaging, and the challenges of making high-performance CMOS receiver circuits, has thwarted the efforts to make fully integrated CMOS optoelectronic systems. Only within the last decade has the potential to integrate photonic devices within the silicon platform emerged due to intense research activities.

Currently there is an increasing interest in conjugating optical functionality to integrated circuits. Direct integration of such optoelectronic devices into microelectronic circuitry with standard CMOS processing would effectively reduce the manufacturing costs and increase yields. That is because of the avoidance of expensive and complex compound semiconductor technologies. Furthermore, on-chip electronics can also implement highly complex signal processing functions and thus contribute to the realization of powerful sensor systems.

Many different application areas can be explored with this technology. In the field of computing and communication, optics will overcome interconnect bottlenecks imposed on electronic circuits by speed, power, and space demands. Another wide application can be optocouplers or optical isolators, which can be employed in any situation where complete electrical isolation between two circuits is required. At the same time, optoelectronics can be used for a large set of very specific applications including, e.g., biological sensors, and for human interface devices e.g., displays, hand-held portable devices and image recognition [2].

In this thesis, a novel design of a monolithically integrated CMOS emitter and detector in a standard silicon technology is presented. This work targets a specific application of human interface devices called Optical Joystick.
1.2 Joystick

A joystick is an input device consisting of a stick that pivots on a base and reports its angle or direction to the device it is controlling [3]. Most joysticks are generally configured so that moving the stick left or right signals movement along the X axis, and moving it forward (up) or back (down) signals movement along the Y axis. There exist both analog and digital joysticks. An analog joystick is one which has continuous states, i.e. returns an angle measure of the movement in any direction in the plane or the space, whereas a digital joystick gives only on/off signals for four different directions and its possible combinations.

Joysticks are used in all kinds of applications, ranging from computer game consoles and mobile phones to industrial equipment and military jets [4][5]. All the existing joystick designs are based on one of the following three technologies, namely potentiometric, magnetic and optical measurement [6][7][8]. Potentiometer is the most conventional method. It uses low cost standard components like a resistor and metal wiper, but is highly subjected to wear and tear. On the other hand, magnetic systems are contactless, and hence highly reliable. However, they require magnetic circuits which drift with temperature and stress leading to additional costs. The third technology, based on optical principles alleviates the problem associated with both the above systems. It has the advantage of being both cheap, and robust.

UBA44000 [9] is an example of one such optical joystick system. It is a simple analog joystick, providing angle and click signal information via I²C interface. It allows accurate navigation through menus and screens for applications in gaming and web browsing with variable speeds and unlimited directions. It can effectively be seen as a replacement for the 4-way buttons in cell phone.

The UBA44000 system as shown in Figure 1.1 uses a non-silicon light emitting diode (LED) and electro-sensitive diodes directly built in the IC. A mirror is mounted at the bottom of the joystick pole as shown in Figure 1.1. The different positions of the joystick involve different photodiode illumination. This is indicated by the different photon count and is analyzed by the digital block, in order to deduce usable tilt and click information.

When the joystick is upright in the rest position, light from the LED is reflected by
the mirror and shines a light circle onto the photodiodes which is formed in the center as shown in Figure 1.2(a). When the joystick is tilted, the mirror follows the same motion, and so the light circle moves away from its center position (Figure 1.2(b)) and implies a current differential between the photodiodes, resulting in measurable X and Y. When the joystick is pressed vertically, the received light intensity increases, and can be interpreted as a click signal. The signals from the photodiodes are digitized and converted to the X, Y angles and click signals.

UBA44000 uses a non-silicon LED light source which cannot be integrated into an IC. Hence, it requires extensive calibrations and sophisticated processing leading to additional costs. This thesis proposes a novel design for UBA44000 optical joystick system which uses a CMOS LED as light source, and single-photon avalanche diodes (SPADs), both integrated on a single chip. The design has been motivated by the discussion made in Section 1.1 on the benefits of monolithically integrated optoelectronic systems.

1.3 Thesis contributions

To the best of my knowledge, no monolithically integrated optoelectronic system in a standard CMOS technology has been developed so far, which targets a commercial application like joystick. In this respect, this thesis makes the following contributions.

1. Preliminary study involving some measurements and experiments for selecting appropriate LED and SPAD devices, and also to conceptually validate the system design.

2. Design and implementation of an array of CMOS LED pixels for emission of light and four arrays of SPAD pixels for detection of light.

3. Integration of the designed system with existing UBA44000 interface.
4. Characterization of the fabricated chip including testing of the basic functionality and independent modules.

1.4 Design methodology

A top-down design methodology was undertaken to realize the prototype. At first, an extensive study of the existing prototype of optical joystick [9] was carried out along with the system analysis to understand the operation and requirements of the system. Then, an extensive literature survey was done to understand the theory of SPADs and silicon LEDs. After this step, some preliminary experiments were performed to demonstrate the functionality of the system. The understanding gained from the study and experiments was used to draw out the overall system architecture, its different blocks, their functionality and the desired specifications. During this process, multiple new concepts were also incorporated to increase the efficiency of the system.

The system analysis was followed by circuit level implementation of the system. A bottom-up approach was employed in the circuit design in CMOS14 technology. Each of the blocks identified in system level analysis was independently designed to meet the required specification. It required multiple iterations between circuit design and layout before the desired specifications could be realized.

The circuit and layout of the pixel for both SPADs and silicon LEDs was followed by the integration at the system level. A modular approach to constructing a 2D array was chosen. The system level blocks including the digital and memory blocks from [9] were then integrated with the pixel arrays to realize the full implementation. This step was a major challenge, since these blocks needed to be modified according to the system flow. At each step of circuit and layout design, the performance was verified against the desired system specifications. This approach finally led to a successful design of the prototype which meets the desired system requirements.

1.5 Organization

The organization of the thesis report is along similar lines as the design methodology. Chapter 2 presents the background study. It briefly explains the existing joystick prototype along with the operation of a SPAD and a silicon LED. The conventional methods to build its front-end circuitry are also explained.

Chapter 3 focuses on the system level aspects for designing the optical joystick architecture. It discusses some preliminary experiments which were performed to derive the system specifications. Also, a complete design of the system on block level is presented. Chapter 4 focuses on the design process of a single pixel with respect to desired system specifications for both the emitter and detectors. It also discusses the circuit and layout level implementation of the 2D array of SPADs and SPADlights. Finally, the layout of the whole system is presented.

Chapter 5 presents the characterization results of the designed system.

Chapter 6 concludes this dissertation providing the summary of the work done along with the contributions. It also elaborates on the future scope of the project.
In this chapter, the background of the conventional joystick architectures is presented, with a brief study of UBA44000 Optical Joystick chip. A detailed discussion of the designed chip and pixel architecture is made in Chapter 3 and Chapter 4.

This chapter is organized as follows. Section 2.1 gives an introduction to the conventional joystick architectures. Section 2.2 describes UBA44000 chip, which forms the background of the designed chip. Section 2.3 throws light on Silicon LED and its limitations. Section 2.4 describes the working of SPAD and how its front end circuitry is typically designed in the literature.

2.1 Conventional joystick architectures

Many different types of joystick architectures have been proposed previously in literature, and they all share a number of common features. For example, all joysticks have a shaft which can be gripped at one end by a user and pivoted about a fixed point in a two dimensional (X and Y) space. Coupled to the other end of the shaft is some sort of control system which is operable to convert movement of the shaft in the space into electrical signals. The earliest joysticks were based on potentiometers. They achieved their functions by converting the angular motion of a control rod to circular motion about two perpendicular axes, thereby rotating a potentiometer in each of the two axes. Although operationally satisfactory in most cases, however this type of constructions has a short lifetime for the reasons mentioned in Section 1.2.

To alleviate these problems, it was proposed to use optical components to detect the actions of the user. Mitchell, U.S. Pat. No. 5,117102 [10] describes relative motion detection device for a joystick which contains LEDs and optical detectors placed diametrically opposite about the shaft of the joystick. As the joystick is moved, the shaft itself blocks the light from the LEDs and thus, the action of the user is detected. Another typical prior art method of detection is disclosed in U.S. Pat. No. 4,748,323 by Holiday [11]. In this device, a circular disk is coaxially mounted on the lower portion of the shaft of the joystick. Four LED/detector pairs are mounted on C shaped blocks. Light from the LED to the detector passes parallel to the shafts neutral position. A light blocking disc will interrupt the light from one or two adjacent emitters to the associated detectors. Each detector has a signal processing circuit connected which produces a change in the electrical state and thus detect the motion. Each of these prior art devices suffer from some limitations. Firstly, they do not provide adequate resolution of the joystick motion, and can only report gross motions. Secondly, to attain greater resolution, a large number of discrete components are required which increases the manufacturing cost of such a device. Lastly, control electronics needs to be sophisticated and carefully designed to determine accurate information.
To overcome the first limitation, an optical joystick device UBA44000 was proposed in [9][12]. The architecture of this chip is described briefly in the next section. Though the described joystick is analog and provides practically infinite resolution, however it still uses discrete components and requires sophisticated ADCs. So, as a part of this thesis work, modifications have been made to the architecture of UBA44000 chip, promising a more simple and cost-effective design. The major change involves replacing the emitter and sensors with newer devices. The emitter in UBA44000 is a non-silicon LED, and is replaced by a CMOS LED. These new changes not only overcome all the three limitations mentioned earlier, but also gives the advantage of integrating the whole chip in single silicon. The detectors are replaced with SPADs which are highly sensitive, and can give better resolution. The complete design is explained in greater detail in the following chapters of this thesis.

2.2 UBA44000 optical joystick chip architecture [12]

The UBA44000 optical joystick is a smart-sensor chip as shown in Figure 2.1. It is meant to measure the tilt of a stick/knob, and to detect a pressure on it. It can be done in many different ways and flavors, in a good configurable trade-off between power-consumption and accuracy. The total physical sensor chain consists of mechanics, a solid state LED, reflecting-mirror, photodiodes and ADCs. It also incorporates a digital block whose task is to schedule the chip and to process the received-signals from the photodiodes, in order to extract an accurate tilt and click measure and detection. However, it is very sensitive to imperfections in production like different misalignment of the devices, angle errors, LED luminescence margin, mirror reflectivity margin, different pressures on the springs and aging (LED luminescence drop, corrosion of the mirror, uneven wearing of the springs ), making calibration an important feature of the design.

Figure 2.1: UBA44000 chip cross-section [12]
2.2.1 Functional overview

The chip is divided into two main parts: analog and digital. Each part is further sub-divided into different modules based on the functionality as shown in Figure 2.2.

2.2.1.1 Analog

1. Analog to digital converters:
   To get the motion of the knob/stick, the chip embeds 3 ADCs, directly connected to the photodiodes. The ADC X and Y convert the differential of currents between the right-left photodiodes (X) or top-bottom (Y) to a digital bit-stream. The ADC C collects the current issued by all the photo-diodes in order to detect any important variation in the light-intensity, which represents a click/release. It encodes the total current into a digital bit-stream. Each ADC delivers a stream of 1 bit, synchronous to the internal clock (520 kHz). Integrating these inputs over a period of time gives a positive-integer representation of these 3 dimensions (X, Y, C). The longer the time (in clock-cycles) of integration, the more accurate this representation is.

2. Photodiodes:
   The electro-sensitive diodes collect the light emitted by the LED and reflected by the mirror. These are directly printed in the silicon, and are organized in 4 rectangles representing the 4 directions (left, right, top, bottom), each divided in...
12 segments that can be independently enabled/disabled.

3. **LED pump and driver:**
The LED pump is needed to double the input VDD1V8 voltage (1.8 V) to provide the LED with the required voltage (around 3.3 V). The use of the pump is optional, as the LED can be supplied directly via an external (LEDVDD3V3) pin. The LED driver enables the digital part to tune the light-intensity by controlling the current going through the LED.

4. **Clock generator:**
The processing and sampling of the signals require a clock which is generated on chip in order to simplify the connectivity of the chip. It is made up of a ring-oscillator followed by a two flip-flops clock-divider. As a result, the clock-frequency is highly temperature and voltage dependent, modifying the measurements. However, the signal-processing is able to compensate for these frequency deviations by dynamically re-calibrating the chip as the measurements deviate. It delivers a clock of 540 kHz frequency at nominal condition (1.8 V, 30°C) ± 30%, with a duty cycle between 45% to 50%.

5. **Power-on reset:**
In order to simplify the use of the chip, it resets itself automatically on every power-on, so that it can be used without a special sequence of signal. This functionality is achieved by the POR (Power-on reset) block. It generates the reset at startup, and automatically releases it after a certain time.

### 2.2.1.2 Digital

1. **Non-volatile memory:**
The non-volatile memory is a multiple-time-programmable memory (MTP) that allows saving all the settings of the chip, as well as its product-identification parameters, in order to restore these after power off, or after every reset. An error-correction-check (ECC) is also embedded in order to strengthen the memory robustness, by inserting redundant bits and then enabling error correction of a defective bit in a word.

2. **I^2C:**
This block contains the entire I^2C interface. It decodes the I^2C communication according to the standard protocol, and then sends the received commands into read/write access from/to the register-interface. This is basically a finite-state-machine. It is mainly an asynchronous interface, although it implements metastability filters in order to access the register-interface in a synchronous way. All the features and results of the chip can be accessed by this port.

3. **Register interface:**
The register-interface contains all the instantaneous register-settings of the chip. These registers are organized in addresses, so that the I^2C or the MTP can access them easily, like a memory. The writing is synchronous to the system-clock, but the reading is asynchronous. Apart from this address-access, all the signals issued
by these \(I^2C\) registers are directly input/output to/from the blocks where these are used or issued.

4. **Decoders:**
   There are two types of decoders. XY decoder converts the 1-bit stream from the X and Y ADCs to a stable signed number. It also rescales and readjusts the existing offset in the measurement.
   Click decoder detects a click from the 1-bit stream from the ADC. It also enables to calibrate the current given to the LED in order to optimize the photodiode signal.

5. **Signal processor:**
   The UBA44000 embeds a dedicated signal processor that programs a good trade-off between power and signal-quality. It ensures that the output is stable, re-scaled, re-aligned (calibration and compensation applied), and ready-to-use (swap/invert outputs) to every system it is integrated to. It also enables to adjust the gain in the four directions (up, down, left, right). It is also where a click-stabilization is performed.

2.2.2 **Key Features**

Some of the key features of the designed UBA44000 optical joystick are:

1. Silicon chip + External LED
2. Click and tilt detection
3. Controllable via \(I^2C\)
4. Settings saved on a non-volatile memory
5. Manual and/or automated calibrations
6. Dedicated on-chip signal processing
7. Voltage: 1.8V and 3.3V
8. Very low power consumption: 11\(\mu\)W in rest condition, 32\(\mu\)W when touched

2.3 **Silicon light emitting diode**

Silicon is generally considered to be an unsuitable material for sourcing light. The two most important obstacles that hinder the fabrication of silicon light sources, like light-emitting diodes, are rather fundamental and are due to the fact that silicon is an indirect-bandgap material with a bandgap of 1.1 eV, as can be seen in Figure 2.3. In the case of radiative recombination of holes and electrons, energy and momentum have to be conserved. Energy is conserved by the emission of a photon with the recombination energy. In the case of a normal diode this energy equals the bandgap, in silicon 1.1 eV. In an indirect-bandgap material this transition has to be assisted by a phonon with
a wave factor that is sufficient to conserve crystal momentum. This event is unlikely to take place and an excited electron is unlikely to recombine with the emission of a photon. In the case of direct-bandgap III-V compounds like GaAs, the transition requires no change in crystal momentum and no phonon is needed. Therefore, the probability is much higher.

Another problem with silicon is the low value of the bandgap at 1.1 eV. This is outside the visible part of the spectrum and is not sufficient to generate electron-hole pairs in a silicon photodetector. Therefore it is not possible to use this LED in combination with a silicon photodetector sensitive to visible range. These two problems show that silicon cannot be used as a light source by making silicon light-emitting diodes in forward biasing.

It has been shown that an efficient light emitter in silicon will broaden the spectrum of products from silicon semiconductor industry. This has led to substantial development work in the field of silicon light emitter, such as porous silicon, erbium in silicon or SiO₂, SiGe heterostructures, quantum dots and dislocation engineering [14][15]. But all of these technologies are quite complex and cannot be integrated into the standard CMOS technology process, which is the current multi-billion mainstream technology in integrated circuitry.

Light emission from silicon PN-junction when it operates in the reverse breakdown avalanche mode has been recently observed [16][17][18][19][20]. When used in avalanche mode, the emission spectrum covers the visible range and the range where silicon photodetectors show high sensitivity. Therefore, several optoelectronic applications can be realized.

In this work, such a PN-junction based light emitting diode fabricated in CMOS14 process is used. This LED is a silicon avalanche diode, which is known to emit light
when reverse biased beyond the breakdown voltage in the so called Geiger mode. The depletion region between the p+ ring and n-well interface is formed, and avalanche breakdown will occur at this depletion region when the reverse bias voltage reaches the breakdown level which induces the multiplications of carriers. Then recombination between part of holes and electrons will emit visible light. With such silicon LEDs, the device has the potential of being fully integrable with standard CMOS circuitry, and no adaptation is required to the CMOS design and processing procedures which would effectively reduce the manufacturing costs and increase yields.

2.4 Single-photon avalanche diode

One of the integral blocks of the optical joystick is a photodetector, which is required to sense the light emitted by silicon LED. In this work, a single-photon avalanche diode (SPAD) has been employed. A SPAD is a p-n junction diode biased above breakdown voltage $V_{BD}$, commonly known as operating in Geiger mode. When biased in this mode, a high electric field exists within the junction. If a photon hits the semiconductor surface and is absorbed in the diodes depletion region, it may trigger an avalanche producing electron-hole pairs by impact ionization which discharges the depletion region capacitance very rapidly [21].

SPADs offer virtually infinite gain as compared to the linear gain avalanche photodiodes (APDs), as shown in Figure 2.4. Thus, a SPAD acts like a trigger device for a single photon producing a sharp current pulse on being hit by a photon. Silicon LEDs being not very efficient require the use of SPADs as photodetectors for the application since they are highly sensitive and easily integrable in standard silicon process with conventional analog and digital circuitries.

2.4.1 Device structure

A SPAD is a specifically designed p-n junction photodiode in which premature edge breakdown (PEB) is avoided and a planar multiplication region is formed within the whole junction area. PEB causes spurious, preferential avalanching on the periphery, thus drastically reducing sensitivity. Several techniques exist to implement PEB prevention. In essence, the techniques have in common the reduction of the electric field at the edges and everywhere else in the device, so as to maximize the probability that the avalanche is initiated in the center of the multiplication region. This is the region where the critical electric field for impact ionization is reached and, possibly, exceeded. There exists several implementation styles for SPADs, and the one compatible with planar CMOS processes involves a shallow or medium depth p or n layer to form high-voltage p-n junctions. Several devices designed in this style have been investigated, yielding a number of structures [23]. An example of a SPAD structure in deep sub-micron technology is shown in Figure 2.5. It consists of a circular dual junction structure: p+ anode/deep n-well/p-substrate. The p+ anode/deep n-well junction forms the avalanche multiplication region where the so called Geiger breakdown occurs. A p-well guard-ring surrounds the p+ anode to prevent premature breakdown [24].
2.4.2 SPAD performance parameters

To analyze the operation of SPAD and its interface, it is important to understand its performance determining factors. Few of the performance factors are influenced by the excess bias voltage of SPAD ($V_E$) which is the difference between the operating bias of SPAD $V_{OP}$ and the breakdown voltage $V_{BD}$. Following is a brief discussion of the major influencing factors:

1. **Dark count rate (DCR):**
   Dark counts refer to the triggering of an avalanche by non-photons carriers in the absence of illumination. These carriers produced through tunneling or thermal generation effects can be captured in traps and their random release leads to avalanche current pulses unrelated to a photon event. Such dark counts have a Poissonian distribution and can be seen as a noise source of the device [25]. In Geiger mode, these spurious pulses cannot be distinguished from regular photon
triggered pulses and are produced at a mean frequency known as DCR. The SPAD DCR increases with higher $V_E$ because of two effects: (a) an increase in avalanche triggering probability and (b) higher emission rate from generation centers due to larger field. DCR is strongly dependent on temperature and defines the minimum detectable signal, thereby limiting the dynamic range.

2. **Photon detection probability (PDP):**  
PDP refers to the probability of a photon being absorbed in the detector active area to generate an electron-hole pair capable of triggering an avalanche. The probability of photon detection depends on diode’s quantum efficiency as well as the excess bias voltage $V_E$. PDP increases with higher $V_E$ since a higher electric field increases the sensitivity and thus its triggering probability. Usual values for PDP in CMOS SPADs are in the range of 1% to 30% [21][23].

3. **SPAD timing jitter:**  
It refers to the statistical fluctuation of the time interval between photon arrival at the sensor and pulse generation by the interface circuitry. Also known as timing resolution of SPAD, it improves with increasing $V_E$. At higher $V_E$, the depletion width is greater and thus, only photons of longer wavelengths can be absorbed, giving a sharper timing jitter pulse. At smaller $V_E$, saturation occurs giving a large timing jitter.

4. **Afterpulsing:**  
During a photon triggered avalanche, some carriers can be captured by deep levels in the junction depletion layer and be released at a later arbitrary time. These released carriers can retriggers the avalanche, generating false current pulses correlated with the previous avalanche pulse. Such an after-effect is termed as afterpulsing and denotes the spurious pulses related to previous photon events. The number of carriers captured by deep levels during an avalanche pulse depends on the trap concentration and the total number of carriers generated during a Geiger pulse i.e. the total charge of the pulse. The shorter is the dead time of avalanche current, the higher is the total charge in the pulse and therefore, the higher is the afterpulsing effects. To sum, afterpulsing increases with reducing dead time and with higher avalanche current intensity.

5. **Dead time:**  
After the onset of an avalanche in a SPAD, the avalanche current needs to be controlled and the SPAD needs to be restored to its Geiger mode operating bias in order to detect subsequent photon arrivals. The time required to quench the avalanche and recharge the diode upto 90% of its excess bias is defined as the dead time [21]. Dead time should be as small as possible as it limits the rate of detection of photons, especially at high photon fluxes, thus reducing the dynamic range. However, a small dead time implies larger afterpulsing, therefore leading to a trade-off.

6. **Crosstalk between SPADs:**  
Crosstalk between SPADs can be both electrical and optical in nature. Electrical
Crosstalk occurs when photons absorbed in the substrate generate carriers which diffuse laterally in adjacent pixels and trigger an avalanche. The mean penetration depth of photons depends strongly on the photon wavelength and therefore, photons in red and infrared ranges induce more electrical crosstalk than short wavelength photons [26]. However, electrical crosstalk can be eliminated by proper SPAD device design techniques; for example, introducing wells in SPADs that create a potential barrier for crosstalking photocarriers.

Optical crosstalk refers to the triggering of spurious avalanche currents in the neighboring SPADs. This is due to electroluminescence effects [21] where secondary photons can be emitted and absorbed by the nearby pixels in an array of SPADs. Optical isolation may be employed among the SPAD devices to reduce such an effect.

7. **Fill factor:**
The fill factor is the ratio between the sensitive area and the total area of a pixel. SPADs typically have a very low fill factor as a large guard ring, designed to prevent PEB and to protect the SPAD from the diffusion of free carriers into its sensitive region, surrounds the active region. Additionally, the fabrication of arrays demand pixel-level electronics which further decreases the fill factor. Thus SPAD arrays generally only exhibit fill factors of a few percent [26][27]. However, it is possible to regain some of the light losses by using pixel-level light concentrators or microlenses which redirect the photons onto the SPADs sensitive area. SiPM based structures have also suggested an increase in fill factor by reducing the amount of electronics required and by increasing the size of SPADs. Recently, a silicon digital photomultiplier has been reported with a fill factor upto 78% [28].

8. **Saturation count rate and dynamic range:**
The saturation count rate is defined as the maximum count rate achieved by a SPAD, and is given by $1/t_{\text{dead}}$, neglecting the count rate distortions from dead time. The dynamic range is defined as the maximum output swing divided by the temporal dark noise [26]. The output swing at the low end is limited by the fluctuation in the total counts in the measured time interval, and has two components, one associated to the statistical nature of the incident photon flux, and other due to the detector’s dark count rate. At the high end, the product of saturation count and integration time is the limit.

### 2.4.3 SPAD readout

Once the photon hit creates an avalanche effect in the SPAD device, its front-end circuitry has the following tasks:

1. Sensing
2. Quenching
3. Recharge
2.4.4 Sensing

The photon absorption indicates an event occurrence indicated by the signal generated at the anode of a SPAD. This needs to be sensed and propagated to the processing circuitry. Typically, an inverter is employed to capture the SPAD signal. The output is as shown in Figure 2.6. However, different circuit topologies may be applied depending upon the signal amplitude of a SPAD. A detailed discussion is presented in Chapter 4.

2.4.5 Quenching

Quenching is the process of halting the avalanche breakdown effect. Different techniques have been proposed in the literature and fast quenching is preferred to avoid self-heating, trapping and optical crosstalk [29]. There are two approaches to quenching - passive and active, as described below.
1. **Passive quenching (PQ)**

   When an avalanche occurs in a SPAD, a potential drop can be developed if a serial load is connected. This potential drop brings the SPAD out of Geiger mode. Thus, the SPAD avalanche current can be quenched on its own by developing a potential drop across a high impedance load $R_q$ \[29\] as shown in Figure 2.7(a). The advantage of passive quenching is that the technique is simple in nature and takes less area as it involves passive components (a ballast resistance). However, it suffers from a relatively long and poorly defined dead time. The saturation count rate of the passive quenching is predicted by $1/(e^{*t_{\text{dead}}})$ \[30\].

2. **Active quenching (AQ)**

   An active quenching circuit tracks the SPAD voltage or current by comparing the signal with a threshold to identify an occurrence of avalanche. After an avalanche is detected, it quickly discharges the total capacitance seen by the SPAD through a secondary path, thereby quenching the avalanche. To achieve this, high speed sensing and feedback circuits are employed. The underlying principle of active quenching is to minimize the number of carriers generated in the SPAD and force the carriers to flow through the secondary path. It is a faster way of quenching through positive feedback mechanism and the dead time is small, well-defined and controlled. The active quenching reaches the theoretical saturation count rate of $1/t_{\text{dead}}$ \[30\].

### 2.4.6 Recharge

After the avalanche current in SPAD is quenched, the recharge of the SPAD is needed to prepare it for the next photon detection. This is done by biasing the SPAD back in Geiger mode. In literature, multiple recharge schemes exist and are typically classified into active and passive nature.

1. **Passive recharge (PR)**

   A passive recharge is possible by the same circuit as passive quenching i.e. a
resistor. However, large parasitic capacitance introduces unfavorable effects in terms of afterpulsing and saturation count rate. It is possible to reduce unwanted parasitics to an extent by integration of front-end circuits and SPADs on a single chip. With passive recharge, the recharge time is given by,

\[ t_{\text{recharge}} \propto RC \]  

(2.1)

A small R gives a shorter dead time but larger afterpulsing, as the trapped carriers are released after SPAD recovers from avalanche.

2. Active recharge (AR)

The underlying principle of active recharge is as follows. As soon as the avalanche is quenched, a secondary low resistance path actively recharges the SPAD back to Geiger mode. AR can be performed to advantage with a small dead time implementation.

Amongst those mentioned above, the most common combination employed in literature is passive quenching with active recharge. This has the advantage of being both area and cost effective, with well defined and controlled dead time. In [31], a passive quenching/active recharge circuit is described (Figure 2.9(a)) and it achieves a dead time of 6 ns with a dynamic range of 116 dB at an acquisition time of 20 ms.

2.5 Summary

In this chapter, the conventional joystick architectures were mentioned, with a detailed discussion of UBA44000 Optical Joystick chip architecture. The limitations of using silicon as a light source in conventional ways were explored, and an avalanche mode Silicon LED was discussed. Furthermore, a SPAD photodetector, its structure and performance parameters were explained. Different techniques to build the front end circuitry of SPAD were described.

The next chapter presents the system architecture of the optical joystick chip designed
in this thesis project. A detailed discussion is made to verify the system functionality, derive the system specifications and explain the working of the system.
This chapter discusses the system level aspects for building an opto-electrical system for the joystick application. We have already covered the principle and applications in Chapter 1.

The chapter is organized as follows: It starts with the system objective in Section 3.1. Section 3.2 discusses some preliminary measurements and experiments performed to validate the system at a conceptual level. Section 3.3 derives the system specifications including emitter and detector. Section 3.4 presents the system architecture, while some new concepts are introduced in Section 3.5. Section 3.6 presents the design of a SPAD pixel at block level. Digital logic is mentioned in Section 3.7, and Section 3.8 derives the interface between different blocks. Different operational modes of the system are explained in Section 3.9. Section 3.10 presents an overview of testing strategy and finally the chapter concludes with the system overview in Section 3.11.

3.1 System objective

The aim of the system is to design a monolithically integrated array of CMOS LEDs and SPADs for optical joystick application. This objective has two advantages.

1. A silicon LED allows integrating the complete system on chip, making it easier to implement and manufacture. The numerous calibrations required to get the system to function correctly with a non-silicon LED are no longer required. Moreover, the output from SPAD detectors is digital in nature. This helps to eliminate the ADCs from the system. The reduction in complexity achieved by using silicon LEDs and SPADs will not only simplify the design, but will also reduce the manufacturing cost of the system.

2. Integrating the complete system with both emitter and detector in silicon using standard CMOS process will open the market for many other applications in different fields.

The first step towards system design is to select the appropriate devices to be used for both emitter and detector, such that the above objective can be achieved without compromising system efficiency. After choosing the right devices, the next step is to demonstrate the functionality of the system in an experimental environment with those devices. Therefore, some preliminary measurements and experiments were conducted as a proof of concept before designing the complete system. An overview of the same is presented in the next section.
3.2 Preliminary measurements and experiments

A SPAD farm is a large array of designed test structures of various SPAD devices, where specific parameters are systematically varied to achieve an optimal combination. One such SPAD farm designed in CMOS14 process was characterized to select the appropriate emitter (LED) and detector (SPAD) device for this application.

3.2.1 Selection of SPAD device

In the SPAD farm mentioned above, several different SPAD families were designed. Various layers with different doping profiles were used for the cathode, anode and guard ring for each of these devices, and the parameters like radius, guard ring width etc. were varied to achieve an optimal combination. The detailed discussion of the different SPAD families and layers used can be found in [32], and is beyond the scope of this thesis.

A set of measurements were carried out to characterize these devices. The first set of measurements consisted of measuring the current-voltage (IV) characteristics, and performing the light emission test. The results from these measurements demonstrate the basic SPAD behavior, based on which the selection was narrowed down to the following devices from two different families. All the structures have a 2\( \mu \)m width guard ring, and 4\( \mu \)m diameter active area.

1. SPAD2: This is the conventional, blue or green sensitive SPAD. In this structure, the anode is a P-type diffusion, p+ layer, cathode is a DNWELL and the guard ring is a p-substrate as shown in Figure 3.1(a). The structure’s junction where Geiger breakdown occurs, lie between p+ and DNWELL, and is quite shallow. The device has a breakdown voltage of 17 V as seen in Figure 3.1(b).

2. SPAD4: In this structure, the anode is a shallow p+ layer, cathode is a DNWELL and the guard ring is a p-substrate. The device has a breakdown voltage of 16.5 V. (See Figure 3.2).

In these structures, three regions contribute to the PDP. First, electrons in a p+/shallow p+ layer will diffuse to the junction after absorbed light generates an electron-hole pair, possibly triggering an avalanche. Second, generated electron and holes in the multiplication region may trigger an avalanche. Finally, generated holes by absorbed light in DNWELL also move to the junction and may trigger an avalanche. However, the impact ionization coefficient of holes is lower than that of electrons. This causes lower PDP especially at longer wavelengths, as PDP is a function of the impact ionization coefficients. Hence, PDP will be biased towards shorter wavelength of light, which generates carriers close to the surface. In SPAD4, the shallow p+ layer is used as anode. This layer is more lightly doped, hence the junction will be shallower and PDP more shifted towards shorter wavelengths than in SPAD2.

3. SPAD7: In this structure, the anode is a PWELL layer, the cathode is n+ and the guard ring is NWELL as shown in Figure 3.3(a). The planar n+ PWELL
junction provides the multiplication region where the Geiger breakdown occurs. The device has a breakdown voltage of 20 V as seen in Figure 3.3(b).

4. SPAD8: In this structure, the cathode is a shallow n+ layer, anode is PWELL and the guard ring is NWELL. The device has a breakdown voltage of 20 V. (See Figure 3.4)

In SPAD7 and SPAD8, the PDP peak is shifted to a longer wavelength when compared with SPAD2 and SPAD4 because photon generated electrons in the PWELL are more likely to initiate an avalanche. Furthermore, the doping of PWELL is generally lower than p+, so the drift of generated electrons in PWELL is longer. This implies that the PDP will have a wider spectral range. In SPAD8, the shallow n+ layer is used as cathode. This layer is more lightly doped than n+, and hence PDP will be shifted slightly towards shorter wavelength, when compared to SPAD7, due to thicker multiplication region.

Since photon counting is the primary goal of this application, sensitivity and noise are the two most important performance parameters. In the second set of measurements, PDP and DCR related data were collected for the above mentioned SPAD
families, and analyzed.

Figure 3.5 shows the PDP measured for SPAD2, SPAD4, SPAD7 and SPAD8, all with 4μm diameter, as a function of wavelength. The measurement was done at 2 V excess bias. As seen from the graph, SPAD2 has the highest PDP of 20% from 450 nm to 500 nm, and 16% from 550 nm to 600 nm. SPAD7 and SPAD8 have the PDP peak shifted to longer wavelengths, for the reasons mentioned above.

DCR is measured by counting the number of avalanches while the SPAD is operating at an excess bias voltage above the SPAD’s breakdown voltage. The measurement is carried out in the dark where the chip is shielded completely from light. The graphs in Figure 3.6 show the DCR measured for the above structures (SPAD2, SPAD4, SPAD7, SPAD8), with 4μm active diameter. The bigger devices with 10 μm active diameter have larger noise which is in the range of 30-60 Hz per μm², whereas the DCR of 4μm device is less than 10 Hz/μm². It is for this reason that only 4μm devices are considered for this application. Also, as seen from the graphs, DCR increases with excess bias voltage $V_E$. DCR for SPAD4 and SPAD7 is very low, when compared to SPAD2 and SPAD8.

Table 3.1 gives an overview of the performance parameters of the SPADs selected from the SPAD farm. SPAD7 seems to be the most promising choice since it has very good DCR characteristic and reasonable PDP with wide spectrum.
In this application, the SPAD sensors will be used with transistors. In case of SPAD7, there are two ways to implement avalanche sensing. One way is to connect the cathode to an excess bias voltage ($V_E$) via quenching resistor, and connect the anode to the negative breakdown voltage ($V_{bd}$). This will bias the substrate to negative voltage. The other way is to connect the cathode to the sum of excess bias voltage and breakdown voltage ($V_{bd} + V_c$) via a quenching resistor, and connect the anode (substrate) to ground. In this case, the output from the SPAD will be a high voltage modulated by $V_c$, so a coupling capacitance is required between the SPAD and transistors to shift the voltage to an acceptable range for transistors.

However, both the methods add extra cost and complexity to the design, and hence are avoided. So, SPAD7 is not used for this application. SPAD2 is another reasonable candidate, albeit with higher noise. A circuit level technique can be used to reduce DCR substantially by disabling noisy SPADs from the array with a memory embedded.
Figure 3.4: SPAD8

Figure 3.5: Comparison of photon detection probability for different SPADs with 4µm active diameter at $V_E=2V$. 

24
in each pixel. The technique is explained in detail in Section 3.5.1. Also, by using SPAD2 any extra complexity associated with negative substrate or coupling capacitors is avoided. Hence, SPAD2 has been selected for this application.

### 3.2.2 Selection of LED device

The LED devices belong to the SPADlight family in the SPAD farm. They do not have a guard ring to increase PEB and thus maximise light emission. We therefore refer to them as “Bad SPADs”. Thanks to PEB, the electric field at the edges will be very high, so breakdown will be more likely. This would indicate much quicker response when compared to a SPAD device with PEB prevention. As mentioned in Section 3.3, it is biased in the Geiger mode, and emits light in the visible range (550-600 nm). SPADlight has two types of devices SPADlightPN and SPADlightNP. Each type has several versions of anode or cathode, each with 3 different diameters.

A set of measurements were carried out to choose the most efficient device. Photon emission efficiency or brightness was calculated from the light emission test for all these devices. The initial set of measurements showed that p+ and n+ layers were much more efficient. Also, the devices with small diameter (4 \( \mu \)m) were most efficient. So, the second set of measurements focused on p+ and n+ layers with 4 \( \mu \)m active diameter devices.

The graph in Figure 3.7 shows measured brightness as a function of power compared for some devices from the SPAD farm. The brightness values were extracted from the light emission test.

As indicated by Figure 3.7, SPADlightPN(p+) is the most efficient device. Hence, it was chosen for this application.

Figure 3.8 shows the device structure with its current-voltage characteristics and
Figure 3.7: Comparison of brightness values for different devices

Figure 3.8: SPADlight(p+)
light emission test. As shown in Figure 3.8(a), the anode is p+ layer, the cathode is NWELL, and the device has no guard ring. The light emission test (Figure 3.8(b)) shows the edge breakdown effect. The IV characteristics (Figure 3.8(c)) shows a breakdown voltage of 8 V, which is lower than the SPADs with uniform breakdown, due to PEB.

### 3.2.3 Emission-detection experiment

Emission-detection experiment (SPADlight(p+) was used to emit light, and SPAD was used to detect this light) was conducted to verify the core concept of the application. In this experiment it was shown that the light emitted by the LED device was being detected by the SPAD sensor. A test set up was made as shown in Figure 3.9(a). A chip with LED device was placed horizontally. It was modulated for a range of frequencies. Another chip with a SPAD device was placed upside down and aligned to the LED chip. Due to the package limitations, a distance of approximately 1 mm was established between the two devices. Figure 3.9(b) shows the output of the SPAD as voltage pulses when LED is turned on, indicating that light from the LED is detected by the SPAD. Some dark counts can also be seen. The inset shows the oscilloscope trace. Though in real scenario the two devices will be available in the same package, with a mirror used for reflecting the light, the above experiment was helpful in demonstrating this core concept of the application.

### 3.2.4 SPADlight on time measurement

Another experiment was conducted to estimate the 'on-time' for SPADlight(p+). The same experimental set up as mentioned in the subsection above was used. The total number of photons detected between the falling edge of SPADlight and rising edge of SPAD output were counted, and a histogram was plotted for the same as shown in Figure 3.10. The measurement was carried out at room temperature with 100 Hz frequency, each bin 1 ns wide. The collected data indicated that the response of the SPADlight was in the order of a few nanoseconds, which is sufficiently fast for this application.
3.3 System specifications

The optical joystick system consists of an emitter, detector and digital logic for signal processing. From the discussion in Section 3.2, SPADlight(p+) has been chosen as emitter, and SPAD2 has been chosen for detection. Silicon LEDs being not very efficient, so many of these devices have been implemented in the system to get a sufficiently high number of photons. These SPADlight(p+) devices are arranged in an array of 16x16, with a total of 256 devices.

As mentioned in Section 1.2, the movement of the joystick is determined by sensing the difference between the number of photons detected in X and Y directions. It is for this reason that four identical SPAD devices need to be placed symmetrically in four directions, with East-West constituting X direction and North-South constituting Y direction. Since the photon count is very low, high sensitivity is required.

Two options are available for designing the detectors with respect to size. Either one very large detector can be used for each direction, or an array of small detectors can be used. Since the fill factor increases with the SPAD size (the guard-ring thickness is kept constant while the active diameter increases), large SPADs with high fill factor are preferable to due to their increased photon detection efficiency (PDE). There is however, an opposing constraint in the SPAD design: the noise characteristics increase more than linearly with SPAD area \cite{33}. Both the average DCR and the SPAD yield can be severely compromised in large SPADs. This results in SPAD diameters being limited to few micrometers, and hence an array based design has been chosen to increase sensitivity. Besides the SPAD itself, another factor that impacts the total sensor fill factor is the amount of electronics required. The chosen SPAD design itself limits the fill factor to 10%. Hence, the goal is to minimize the amount of electronics required.

The chip-area is the major cost driving factor of the system built in CMOS technology. To have small area for low-cost system, it is of great interest to have small sized pixels.
<table>
<thead>
<tr>
<th><strong>Emitter (SPADlight(p+))</strong></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>Breakdown Voltage</td>
<td>8V</td>
</tr>
<tr>
<td>Current Consumption</td>
<td>1N mA, N=1 to 64</td>
</tr>
<tr>
<td>Operation Frequency</td>
<td>100 Hz (Maximum)</td>
</tr>
<tr>
<td>Duty Cycle</td>
<td>20% to 60% (programmable)</td>
</tr>
<tr>
<td>Pixel Pitch</td>
<td>20 µm</td>
</tr>
<tr>
<td>Array Size</td>
<td>16x16</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th><strong>Detector (SPAD)</strong></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>SPAD Active Area</td>
<td>4 µm diameter</td>
</tr>
<tr>
<td>Breakdown Voltage</td>
<td>17V</td>
</tr>
<tr>
<td>Sensitivity Spectrum</td>
<td>400-600 nm (≥ 1% PDP)</td>
</tr>
<tr>
<td>PDP</td>
<td>22% peak at 450 nm</td>
</tr>
<tr>
<td>DCR</td>
<td>≤ 800 Hz</td>
</tr>
<tr>
<td>Pixel Pitch</td>
<td>19µm</td>
</tr>
<tr>
<td>Pixel Fill Factor</td>
<td>4%</td>
</tr>
<tr>
<td>Array Size</td>
<td>20x16</td>
</tr>
<tr>
<td>Saturation Count Rate</td>
<td>500 MHz</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th><strong>System</strong></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>CMOS Process</td>
<td>140 nm</td>
</tr>
<tr>
<td>Chip Area</td>
<td>1.5x1.5 mm²</td>
</tr>
<tr>
<td>Frame Rate</td>
<td>10-100 Hz</td>
</tr>
<tr>
<td>Power Consumption</td>
<td>As low as possible</td>
</tr>
</tbody>
</table>

Table 3.2: System specifications

The pixel size is limited by the SPAD design and technological constraints. A pixel pitch of 20µm was chosen which allows a fill factor around 4% and is considered reasonable for so-called smart pixels, capable of high performance. This choice leads to an area of 330x400 µm² for SPAD array, and the core area of chip is 1.5x1.5 mm².

A joystick is a hand held device and hence the major feature is to have low power consumption. With such a complex array of pixels, the challenge is to limit the power consumption to a few microWatts. The final set of specifications is summarized in Table 3.2. Although the specifications have been derived for joystick application; the design with this set of specifications can be easily extended to other opto-electrical applications.
3.4 System architecture

The application determines the system level specifications. It is necessary to perform the system design at the macro level to get a better understanding of the system working along with its requirements. In this section, the system operation, design alternatives and various tradeoffs are discussed.

3.4.1 At the light source

In order to achieve the correct functionality of the system, some minimum number of photons need to be emitted from the light source in a given integration time. A defined percentage of these photons (depending on the efficiency of sensor system i.e. PDE) will be detected, and this will constitute the usable signal. In addition to this, the sensor system has noise characteristics given by the dark counts. At the lower end, this noise will dictate the minimum number of photons that are required to be emitted from the light source, and hence the minimum power necessary for the application to work. The light source used is an array of silicon LEDs, which can be modulated to operate at different intensities. The number of photons emitted from this source per second can be calculated according to Equation 3.1

\[ \text{Number of photons/sec} = \text{Photon Flux} = N = \frac{\text{Power}}{E_o} \]  

where \( E_o \) is the photon energy given by Equation 3.2

\[ E_o = \frac{hc}{\lambda} \]

where \( h = 6.62 \times 10^{-34} \) Js and \( \lambda = 580 \) nm (by assumption).

The signal to noise ratio (SNR) is an important parameter and can be calculated according to Equation 3.3.

\[ \text{SNR} = 20\log_{10}(N \times PDE \times t_i) - 10\log_{10}((N \times PDE \times t_i) + (DCR \times t_i)) \]

where PDE is photon detection efficiency and is taken to be 1%. This value is calculated from 25% PDP and 4% fill factor. The noise is the fluctuation of the total counts in the measured interval and has two components, one associated to the statistical nature of the incident photon flux and other due to DCR. Both these noise sources can be considered Poisson processes, so their variances are equal to their means [34]. A graph depicting SNR as a function of incident optical power is shown in Figure 3.11. A total integration time of 1 second is used. The graph shows three different plots, assuming 10%, 50% and 100% reflection of the light emitted from SPADlight array via mirror. It can be seen that minimum 9*10E-12 W of optical power (10% reflection case) is required to be emitted in order to get useful signal.

Each SPADlight(p+) device consumes 1-1.5 mA current, and has a breakdown voltage of 8V. This leads to considerably high power consumption if all the devices in the array are enabled simultaneously. In order to achieve optimum power consumption, the array is sub divided into clusters of four SPADlight devices. Each cluster is controlled by a driver, which can enable/disable the complete cluster. In this way the devices can be enabled in a granularity of four, until the optimum light intensity is achieved. The block diagram of the SPADlight cluster is shown in Figure 3.12.
3.4.2 At the detector end

The photons emitted from the light source are sensed by the detector arrays in all four directions. By counting these detected photons in a given time frame it is possible to extract the intensity information. Since the detector arrays in all four directions are identical, the architecture for array in one direction is explored here, and is then extended to others.

The sequence of events necessary for calculating the intensity information is mentioned below, and also depicted in the timing diagram in Figure 3.13.

1. Reset the complete system.
2. Enable the light source (SPADlight) and sensor (SPAD) arrays for a fixed time period.

3. When photon strikes a SPAD pixel, an output pulse is generated by the SPAD. During this exposure period many such pulses can be generated by all the pixels in the array.

4. A counter which is synchronous to these output pulses counts them to indicate the number of photons detected by the array in that time period.

5. Now, both the light source and SPAD arrays are disabled.

6. The counter output is then processed to get the intensity information.

Silicon Photomultipliers (SiPMs) [35] are the most suitable candidate to achieve this functionality. There are two common ways to operate SiPMs. The traditional method is based on an analog paradigm and is shown in Figure 3.14. In this method, the passively quenched Geiger-mode cells of the SiPM are connected in parallel through a long interconnection. The resulting output signal is therefore the analog sum of the individual currents of all cells. However, the good intrinsic performance of SPAD is not fully utilized, as the generated signal is deteriorated by the relatively large parasitics of the on-chip interconnect and the external load. Furthermore, susceptibility to electric noise and high sensitivity to temperature variations are typical characteristics of the analog SiPM [36]. Also from the system perspective, large scale applications of analog SiPMs imply some design challenges like reading out every single channel can become a difficult task. It is for all these reasons, that a mixed signal ASIC is needed to condition and digitize the SiPM output signals to generate useful information.

The same functionality can be realized in a single chip via digital SiPMs according to the scheme shown in Figure 3.15. Here, the SPADs are integrated with conventional CMOS circuits on the same substrate. Each SPAD has its own associated electronics in the pixel to achieve smart functions. Each cell or the complete array is then connected to the photon counters to determine the number of detected photons. Eventually, data
processing logic could be implemented on the same chip. Thus, digital SiPMs are simple in nature, and free from issues associated with analog SiPMs. Therefore, digital SiPM based architecture has been chosen to be implemented in this work.

### 3.5 System concepts

Several concepts have been introduced at the system level to make the design more efficient and robust. A discussion of the same has been made in the following section. Detailed implementation is presented in Chapter 4.

#### 3.5.1 Hot pixel elimination

Hot pixels, also called as screamers, consist of SPADs with very high dark count rate. It has been shown in literature [37], that only very few diodes contribute significantly to the total dark count rate of the array. This happens due to the random distributed defects in the SPAD active area. It is also evident from the graph shown in Figure 3.16 that only 1% of the diodes have very high DCR. Switching these diodes off can significantly reduce the total dark count rate of the array. In this case the DCR is reduced by an order of magnitude at almost negligible loss of sensitivity which is a significant gain.

In this application, the photon count is very low and noise might hamper the functionality of the system. It also causes unnecessary power consumption. It is for this
Figure 3.16: DCR cumulative probability for 3V excess bias at room temperature in 0.35 μm CMOS technology. [37]

Figure 3.17: Hot pixel elimination technique

reason that a circuit technique has been employed to switch off the noisy SPADs. While calibrating the device, it can be made known if a particular SPAD is noisy. This can be achieved by monitoring the dark count rate for every pixel. If it crosses a set threshold, then that pixel can be labeled as a hot pixel. This information can then be used to enable/disable a particular pixel. A memory element is required to store and program the pixel with screamer data as shown in Figure 3.17. In case of a hot pixel, logical 0 is written to the memory. This turns off the quenching transistor, thereby disabling the SPAD by increasing the voltage at anode to $V_{DD}$, such that it is no longer biased in Geiger mode. The technique is explained in greater detail in Chapter 4.

3.5.2 Spatial and temporal compression

The architecture based on a digital SiPM has been chosen for this application given its advantages over analog SiPM as mentioned in Section 3.4.2. Now the main challenge is how to efficiently connect the SPADs outputs to the digital counter. Having a single digital counter per pixel would increase the electronics substantially and thus reduce the fill factor. On the other end, using a single counter for many SPAD pixels together or for the complete array has the advantage of significantly increasing the fill factor by reducing the total electronics required for readout. However, summing up a large
number of SPAD outputs, each with a pulse width of hundreds of nanoseconds (given by the dead time) can lead to significant loss of photons. To solve this challenge, two compression techniques were conceived that work in tandem to produce the counter clock signal: spatial and temporal compression.

3.5.2.1 Spatial compression

The spatial compression technique [38] consists of a number of SPAD outputs connected to an OR-like gate tree as shown in Figure 3.18, which performs the digitization of the signals. For all practical aspects, the group of SPADs spatially compressed works as a single large SPAD. A key advantage of this technique is that the DCR scales linearly with area, and since the compressed SPADs are of the same size, the yield is kept constant. This can be a significant improvement over single large SPAD even if the fill factor of the spatially compressed SPADs is the same as the one of the single SPAD.

However, by using this technique the SPADs connected to the same gate which trigger during each others dead time are compressed so that only one is counted. As a result, the SPADs are limited to a maximum count given by the dead time. Previously fabricated SPADs in CMOS technology have shown dead time to be of the order of few hundred nanoseconds [39], which can lead to some photon loss. Several techniques have been proposed in literature to reduce dead time by active quenching, and this
might help to minimize the photon loss. However, reducing the dead time increases afterpulsing probability significantly as can be seen from the graph depicted in Figure 3.19. Reducing the dead time below 100 ns increases afterpulsing by 15-25%. It is for this reason that temporal compression is employed to minimize photon loss without affecting afterpulsing.

3.5.2.2 Temporal compression

While the spatial compression explores the distribution of photons in space, the temporal compression takes advantage of the distribution of photons in time. By adding a monostable circuit [40] with a short pulse width after the SPAD output as shown in Figure 3.20, it is possible to effectively remove the SPAD dead time. These short width pulses are then given as an input to spatial compression logic, where the loss due to compression is almost negligible and the possible photon throughput can be increased significantly.

Depending on the technology, the monostable pulse width can easily be made sub-nanosecond, essentially creating a GHz channel where the SPAD trigger signals are transmitted. Since the data in this channel is flowing in the form of a train of pulses, the output of the final OR gate can be directly connected to the counter clock input. This provides a substantial gain compared to other digital summing solutions as, for instance, a full parallel adder.

Thus, it can be concluded that the spatial compression scheme is particularly advantageous as it can provide a linear relationship between SPAD DC and active area, when
the SPAD noise characteristics usually severely limit the SPAD practical dimensions. It also helps to reduce the electronics required for readout of each individual pixel, and thereby increase the fill factor. On the other hand, a temporal compression scheme creates a high speed channel from the SPADs to the counter by minimizing photon loss without increasing afterpulsing.

The two schemes work in tandem as shown in Figure 3.21, creating a train of pulses output that is fed to the digital counter outside the SPAD array. This way, a further advantage of the logic is that the number of bits to be read out of the array is significantly reduced.

### 3.5.3 Spike filter

The process of summing up the outputs of individual clusters to generate a single output bit stream might cause very short glitches in the bit stream, which, if provided as an input to the counter, might cause it to enter metastable state, and hamper the functionality of the complete system. To avoid this situation, a spike filter has been added. The block diagram is shown in Figure 3.22. The spike filter takes a bitstream of '1' and '0' as an input, removes all the spikes less than a specified duration, and produces a clean output bitstream. Since the counter can count at the maximum frequency of 500 MHz, the spike filter has been designed to remove all glitches from the bitstream which are less than 1 ns.

### 3.6 SPAD pixel

Some of the concepts discussed in the previous section have been employed in the design of the SPAD pixel. Figure 3.23 shows the block diagram of the SPAD pixel. The SPAD
is biased in Geiger mode at a voltage of $V_{bias}$. Whenever a photon strikes the SPAD, a voltage pulse is generated which is immediately quenched and then recharged by the quenching & recharge block. 1 bit memory is required for masking in case of hot pixel elimination. A monostable element is used for temporal compression before feeding the SPAD output to OR gates.

### 3.7 Digital logic

The most important function of the digital module is to analyze the output bit stream generated by SPAD arrays in all four directions to produce usable tilt and click information. It is also responsible to manage the configuration of the entire chip. To achieve these functions, this module is divided into several sub modules as shown in Figure 3.24. A brief description of the sub modules is given below.

1. **Photo decoder:**
   
   This sub module replaces the XY decoder and click decoder from previous version. It contains four counters for each direction. Each counter can count to a maximum
frequency of 500 MHz, and is 24 bits wide. The output from the counters is then converted to a signed number for X and Y difference to detect tilt, and to another signed number for light intensity to detect click.

2. Signal processor:
The processor sub module contains the multi-gain, threshold, click stabilization and swap/invert functionality. It enables to adjust the gain in four directions, ignore small variations around the center-position and scales the response accordingly, thereby ensuring a stable, re-scaled, re-aligned and ready-to-use output.

3. Controller:
In order to save energy, the application has three different power modes, namely sleep, stand by and active (plus a calibration mode). It is the task of the controller to schedule the application to switch between different modes in order to achieve a power demand as low as possible with optimal response. The core functionality of the block is the same as in previous version [9]; however some modifications have been made to schedule SPAD sensors and SPADlight diodes.

4. Register interface:
The register-interface contains all the instantaneous register-settings of the chip. These registers are organized in addresses, so that the IC or the MTP can access them easily, like a memory. The writing is synchronous to the system-clock, but the reading is asynchronous. Apart from this address-access, all the signals issued by these IC registers are directly input/output to/from the blocks where these are used or issued. Some changes have been made to this sub-module to meet the SPAD sensors and SPADlight diodes requirement.

5. I^2C:
This block contains the entire I^2C interface. It decodes the I^2C communication according to the standard protocol, and then sends the received commands into read/write access from/to the register-interface. This is basically a finite-state-machine. It is a mainly asynchronous interface, although it implements metastability filters in order to access the register-interface in a synchronous way.

6. Non-volatile memory:
It is an ultra low cost and low power, multiple time programmable (MTP) memory. It has a total size of 32x22 bits. It returns words of 16 data-bits, with 6 extra bits which are redundant and are used for error-correction coding. It can store most of the settings of register interface in order to restore these automatically after every power-on of the chip, or after every reset.

7. MTP interface:
It enables to adapt the memory interface, addressing 32x16 bits, to the register interface, addressing a virtual range of 64x8 bits. The memory interface also catches the memory feedback signals (error-detection) and handle the memory control request coming from the register-interface itself. Therefore, the register interface access can easily be multiplexed between the memory and I^2C interface.
It is to be noted that Signal Processor, \( \text{I}^2\text{C} \), Non-volatile memory, and MTP interface blocks are the same as in previous version [9]. Also, the detailed description of the digital module is omitted here because it was not implemented as a part of this thesis work.

### 3.8 Interface between different modules

In order to configure and control the emitter and detector module of the chip, some signals are wired to these blocks by digital module. These signals are required to enable/disable a SPADlight cluster and a SPAD pixel, or set/reset the memory associated with each SPAD pixel.

Following control signals are provided by the digital module to the emitter and detector module.

1. **an\_spads\_light\[63:0\]**-
   It is a 64 bit control data to enable/disable a cluster from SPADlight array. Each bit represents one cluster from the array. This functionality enables us to control the light intensity and pattern. Since SPADlight array is the most power consuming module of the design, the above control also provides the flexibility to achieve optimal power consumption.

2. **an\_spads\_sensor\_col\[6:0\]**-
   It is a 7 bit control signal for selecting a single column of a SPAD array in a particular direction, i.e. either top, bottom, left or right. Since each SPAD array has 16 columns, so 4 bits (an\_spads\_sensor\_col[3:0]) are required to select a column, 2 bits (an\_spads\_sensor\_col[5:4]) are required to select the direction and 1 bit (an\_spads\_sensor\_col[6]) is for not selecting any column of any array.

3. **an\_spads\_sensor\_row\[19:0\]**-
   It a 20 bit data for writing to the 1 bit memory associated with each SPAD pixel of the column selected by an\_spads\_sensor\_col\[6:0\] signal. Since there are 20 pixels in one column, so 1 bit represents 1 pixel. It can either write a 0 or 1 to reset or set the pixel respectively.

4. **Reset**-
   It is a global signal associated with all the SPAD arrays. When this signal is high, then the masking memory is cleared. It is a safe back up mechanism, and is not compulsorily required, since the same functionality can be achieved by writing a 0 to the memory.

5. **Spadoff**-
   It is a global signal required to disable all the SPAD pixels simultaneously. It is an active low signal, which implies that the pixels are disabled when Spadoff is 0. It is useful to switch off the pixels in the second half of the time frame when the signal processing is active to avoid interference and minimize power consumption.

There are many other signals provided by the digital part to control the remaining parts of the design. Those signals are unchanged from the previous version, and hence
are not mentioned here. Additionally, some controls signals for the testing purpose are also available.

Four interface signals are wired from the detector module to the digital module. These are as mentioned below.

1. **spads_top** -
   It is an output bit stream of ones and zeros from the top direction SPAD array.

2. **spads_bot** -
   It is an output bit stream of ones and zeros from the bottom direction SPAD array.

3. **spads_left** -
   It is an output bit stream of ones and zeros from the left direction SPAD array.

4. **spads_right** -
   It is an output bit stream of ones and zeros from the right direction SPAD array.

Each of the bit streams has a maximum frequency of 500 MHz. These bit streams are provided as an input to the respective counter, and are further processed to give usable click and tilt information.

### 3.9 System operation

Each time frame can be divided into three different modes based on the operation.

1. **Calibration mode:**
   Before collecting any measurement data, the chip needs to be calibrated. In this mode any offset and alignment related issues are compensated. Also, the calibration for the dark count of SPADs can be performed during this stage, and hot pixels can be marked. The calibration can be performed either automatically or manually. It need not be performed every time a measurement is done. Once calibrated, the settings can be saved on a non volatile memory and retrieved every power-on.

2. **Time uncorrelated photon counting (T UPC) mode:**
   During this mode of operation, both the light source and the sensors in all four directions are enabled. The photons detected by the SPAD sensors are counted by a digital counter to get intensity information. Since there is no correlation with the arrival time of photons, hence the name time uncorrelated photon counting. It is also the most power-consuming stage, and hence it is desired to operate the chip in this mode for as short duration as possible.

3. **Signal processing mode:**
   It is during this mode of operation that all the data processing is performed on chip. The output of the counters in each direction is fed as an input to the signal processor. The data is then processed and analyzed to get any usable click and tilt information for the joystick. Several different functionalities like multi-gain, threshold, swap/invert etc. have been incorporated to achieve this goal.
3.10 Design for testing

To reduce cost and ease the integration of the chip in a system, a testing architecture has been designed to use as few pins as possible. This requires a more creative solution, where signals to be tested are multiplexed, and then observed one by one. The major blocks which need to be tested are categorized into four types:

1. Digital core cells
2. Non-volatile memory
3. SPADlight array
4. SPAD array

The testing methodology for 1 and 2 is essentially the same as in the previous version. Both the modules are fully testable by structural test i.e. scan insertion by switching into testing mode. Memory can also be tested via functional test. It has been extensively covered in [9], and is not in the scope of this thesis. A brief discussion of the design for testing of SPADlight and SPAD array is given below.

3.10.1 SPADlight array

This module is testable in the functional mode, which makes the key internal signals visible via an output test pad. The test involves monitoring the functionality of the SPADlight diodes. Either a separate test cluster can be included on chip, or the pixels from the functional SPADlight array can be observed on the output test pads. However, routing the signals from the SPADlight array to the output pads might lead to routing complications since the array is realized in the center of the chip. Therefore, a separate SPADlight test cluster with a driver has been included on the chip. The cluster is identical to the one designed in Section 3.4. The buffer drives all the four diodes simultaneously. When the output of the driver is high, NMOS transistors connected to the anode of diodes are switched on, which in turn biases the diodes above breakdown voltage, thereby activating them. Since only one pad is available to observe the output, a multiplexer is used to select and monitor the outputs serially.

3.10.2 SPAD array

This module is also testable in the functional mode, and the key internal signals are visible via an output test pad. Three different test nodes have been identified for the detector module.

1. SPAD functionality test:
   Few pixels from the SPAD array in each direction can be tested. The output signal from the anode of the SPAD is buffered for the selected test pixels. Since only one test pad is available for observing the output, all the output signals from the four SPAD arrays are multiplexed, and can be observed one at a time by selecting the appropriate select line.
2. **SiPM output test:**
   The output of the spike filter which is a bit stream of ‘1’s and ‘0’s, with a maximum frequency of 500 MHz can be tested by observing it on a high speed output pad. If the output is as expected, then the complete functionality of the emitter and detector module is verified.

3. **Spike filter functionality test:**
   A high speed input test pad can be used to inject the spike filter with a test signal to verify its functional behavior. This test mechanism also ensures that the digital logic can be tested even if the SiPM output is corrupt.

### 3.11 System overview

Various concepts employed in the system along with the system blocks necessary to build them have been discussed in this chapter. Figure 3.25 shows the block diagram of the system, with the interface signals between the light source, SPAD arrays and digital logic. The internals of the SPAD and SPADlight pixel are omitted here for clarity.
3.12 Summary

In this chapter, the system design was carried out to derive the complete set of specifications for emitter, detector and the system. The architecture is discussed, along with the design of pixel for SPAD and SPADlight. To enhance the performance of the system, multiple concepts are introduced such as hot pixel elimination, spatial and temporal compression and spike filter. Furthermore, the digital block is introduced for completeness, and an interface between different blocks is drawn out. Finally, a brief overview of design for testing the system is presented.
This chapter describes the design and implementation of different blocks of the Optical Joystick system. First, the appropriate design choice is made for each pixel building block, both for SPAD and SPADlight. This is followed by its design to meet the desired specifications and finally, all the building blocks are integrated to fit within a 19 μm x 19 μm pixel area both for SPAD and SPADlight. A modular approach is employed to construct the array and system level blocks are incorporated for correct operation of the system.

This chapter is organized as follows: Section 4.1 summarizes the chip architecture, while Section 4.2 categorizes the internal modules. Section 4.3 discusses emitter module in detail, with pixel and array implementation. Section 4.4 discusses detector module with all building blocks and explains the detailed design process. Finally the complete system integration is presented in Section 4.5

4.1 Chip architecture overview

Before describing the details of the circuit level implementation, a brief overview of the chip architecture derived in Chapter 3 is summarized in this section. The block diagram of the chip is shown in Figure 3.26. The center of the chip has an array of light emitting diodes (SPADlight array) with 16x16 pixels capable of emitting light. Each pixel has a SPADlight diode and some logic to enable/disable the pixel. The drivers on the left and right of the array are capable of turning the diodes on/off with a granularity of 2x2, also known as SPADlight cluster. Hence, there are 8x8 clusters with 64 SPADlight drivers. The chip also has four arrays of single photon avalanche diodes (SPADs) capable of detecting light, in each direction of top, bottom, left and right. All the detector arrays are identical to each other. Each array is composed of 20x16 pixels; where each pixel outputs a voltage pulse corresponding to the detection of a photon, thereby contributing to the total photon intensity. Each pixel consists of a photodiode, quenching circuitry, mask memory, monostable and some associated electronics. The sum of the photons detected by a cluster composed of 2x2 pixels is read out from the array via read out circuitry. The read out system consists of the concatenation of digital OR gates to generate a bit stream indicating the number of photons detected by the SPAD array in one time frame. All configurations and control of the state of the chip are carried out using I²C bus and other digital logic present on the chip.
4.2 Categorization of internal modules

To implement the above mentioned functionality a modular approach is followed, whereby the chip is divided into three different modules, namely: emitter module, detector module and digital module.

1. **Emitter module:**
   This module consists of SPADlight array and associated drivers. It has been designed to replace the solid state LED logic i.e. driver and charge pump used in the previous version. However, for testing purposes and also as a safe back up mechanism, LED driver and charge pump are included in the current design along with the emitter module.

2. **Detector module:**
   This module consists of the SPAD array, digital OR gates for read out and some other electronics in each direction. It has been designed to replace the photodiodes and analog to digital converter module from the previous version.

3. **Digital module:**
   This module is responsible for the configuration of the chip, settings of the registers and analysis of the output bit stream collected from SPAD read-out circuit to give usable tilt and click information. Its core functionality is same as in the digital module from the previous version mentioned in Section 3.7, while some parts of the logic have been adapted according to the new emitter and detector module. The module was not implemented as a part of this thesis, and hence the details are not covered here.

4.3 Emitter module

The emitter module consists of the SPADlight array and drivers. The array consists of 8x8 clusters, where every cluster consists of 2x2 pixels and is designed to emit light for a certain time period. Since the functionality of each cluster is identical and independent of the other clusters, it is possible to define the architecture of one cluster and extend it to the complete array. Since a pixel is the basic unit of cluster, we start by looking at the pixel architecture. And later in this section, the design of the SPADlight cluster, driver and the complete array is explained.

4.3.1 SPADlight pixel

SPADlight pixel consists of a silicon light emitting diode, a strong pull down transistor and a pull-up transistor. The pixel architecture is shown in Figure 4.1. As explained in Section 3.2, the diode is chosen from the SPAD farm study because of its relatively high efficiency and stability. The cathode of the diode is biased at a high voltage of 9.8 V, which is 1.8 V above the breakdown voltage. The diode acts as a current source and can sink maximum current of 2 mA when it is operating in Geiger mode. The anode of the diode is modulated via strong pull down NMOS transistor, which has been sized
Figure 4.1: Architecture of SPADlight pixel

sufficiently wide to sink 2 mA current. The PMOS transistor acts as a clamp, which prevents the voltage at anode from shooting up to a high value when the diode is cut off.

4.3.2 SPADlight cluster

A group of four independent pixels is classified as SPADlight cluster, which is then extended to form an array of 8x8. Each cluster can be enabled/disabled by the associated driver as shown in Figure 4.2. This flexibility allows the SPADlight cluster to be enabled in a controlled manner depending on the application requirement from a minimum of 1 cluster to a maximum of 64 clusters. It further helps to minimize the power consumption, as SPADlight array is the most power hungry block of the designed architecture.

4.3.3 SPADlight driver

Each cluster (group of pixels) of SPADlight array is driven by a buffer. Since the array has 8x8 clusters, 64 identical buffers are designed and placed outside the array. The buffer is designed to drive an output load represented by the input gate capacitance of four NMOS transistors with $W = 20\mu m$. For minimum delay, a fan-out of 3.6 is the typical buffer sizing standard [41].

The sizing of the designed driver is shown in Figure 4.3, and has been optimized for delay and area through simulations.

The control signals (an_spads_light) which drive the buffer are generated in the digital block, and control enabling/disabling of the cluster.

4.3.4 Functional verification

In order to verify the functionality of the emitter module, it is important to model the behavior of SPADlight diode. It is modeled as a switched current source of 2 mA as shown in Figure 4.4. The capacitance at the anode is modeled as 400 fF.

Using the SPADlight model described above, simulations were run on a cluster level to verify its functionality. A control signal with frequency 1 kHz is provided as an input
Figure 4.2: SPADlight cluster

Figure 4.3: Driver for SPADlight cluster

to the driver. Signal “driver_out” shows the output of the driver, which is an input to the gate of pull-down transistors for all four pixels. The remaining signals show the anode of all four pixels switching simultaneously corresponding to the input signal.
4.3.4.1 Parasitic modeling

As mentioned above, a small PMOS transistor has been included in the pixel which acts as a clamp, and prevents the voltage at anode from shooting to a high value when
the pixel is disabled. In order to functionally verify this concept, a worst case scenario has been assumed. A parasitic inductance of 10 nH has been modeled in series with the anode of the diode. This inductance, when coupled with the capacitance of the junction can cause a ringing effect.

Two different cases, with and without PMOS clamp have been simulated to understand this effect.

1. **Case1**: Pixel designed without PMOS clamp.
   We can see from the simulation results (refer Figure 4.6(b)) that voltage at anode overshoots 5 V.

2. **Case2**: Pixel designed with PMOS clamp.
   It can be seen from Figure 4.7(b) that voltage at anode rises to 1.8 V, and is clamped by PMOS, as expected.
   Thus, it can be concluded that even in the case of excessive parasitic effects, the clamp is sufficient to prevent the voltage at the anode from rising beyond the nominal value.

### 4.3.5 Layout of the cluster

The layout of the cluster is shown in Figure 4.8. The pixel pitch is 19 μm, and the cluster has the dimension of 38x38 μm². The wide pull-down transistor M1 has been folded into multiple fingers to make it more compact. The aspect ratio has been adjusted to fit M1 in the available space. Folding also has the added advantage of reduced gate resistance, hence faster frequency response. Three power lines are routed in the cluster for V_{DD}, GND and V_{OP} (bias for SPADlight).
4.3.6 Building the array

At first, a single row was constructed with 8 clusters, and then 8 such row instantiations built the 8x8 array as shown in Figure 4.9. 64 instantiations of drivers were created to drive each cluster independently. All the drivers are placed on the left and right of the array, vertically aligned, thereby saving any extra horizontal space. A control input
(an spad light) to enable/disable a cluster is routed to all four pixels of the cluster in metal 3 in horizontal direction.

Since the current consumed by the array is relatively larger, a careful layout has been done to suppress electromigration and mitigate IR drop. The worst case maximum current carried by the GND and $V_{OP}$ lines is approximately 500 mA if all the clusters in the array are enabled simultaneously. Both the lines are laid in ultra thick metal 5 which has a maximum current density of 9 mA per $\mu m^2$ in this process. Therefore, GND and $V_{OP}$ tracks are designed to be 20 $\mu m$ wide in order to suppress electromigration effect.

4.3.6.1 IR drop

To achieve small IR drop in GND and $V_{OP}$ lines, it is important that these lines are distributed well across the array. The layout was carried out considering the requirement. $V_{OP}$ runs in metal 5 all around and across the array. GND runs in metal 5 around the array and in metal 1 all across the array.

IR drop is analyzed in two steps. The first step involves calculating the IR drop from the bond pads to the array, and the second step involves analyzing the IR drop inside the array. The resistive network for the same is shown in Figure 4.10. The worst case IR drop is experienced by the center most pixel.

1. **IR drop for $V_{OP}$**
   
   Ultra thick metal 5 was used to lay down the tracks for $V_{OP}$ from the bond pad to the array, and also inside the array. The sheet resistance of metal 5 is 10 mΩ/$\square$. Using the length and width information, all the resistances were calculated.
Then the whole network was simulated with worst case current consumption to get an IR drop of 62.5 mV, which is acceptable at system level.

2. IR drop for GND

Ultra thick metal 5 was used to lay down the tracks for GND from the bond pad to the array, and metal 1 was used inside the array. With similar calculation for $V_{OP}$, an IR drop of 80 mV was calculated, which is acceptable at system level.

Figure 4.11 shows the $V_{OP}$ and GND power rails in the array. Both buses run all across the array in a checker configuration to limit the IR drop.

### 4.4 Detector module

The detector module consists of the SPAD array and read-out system in each direction i.e. top, bottom, left and right. The arrays with the read out circuit are identical in all four directions. Each array consists of 20x16 pixels, where every pixel is designed to sense light, and indicate the arrival of photon by a pulse. A cluster consists of 2x2 identical pixels, with digital logic to sum up the output of each pixel. This total output from the cluster is then read outside the array. Since the functionality of each cluster is identical and independent of the other clusters, it is possible to define the architecture of one cluster in one direction and extend it to the complete array in all four directions. Therefore, in this section the complete design of the SPAD pixel and SPAD cluster along with the read out circuit is explained.
Figure 4.11: Layout of power rails. The power rail checker was designed to keep worst case IR drop within 62.5 mV for $V_{OP}$ and 80 mV for GND.

4.4.1 SPAD pixel

Each pixel consists of a SPAD, quenching circuit, 1 bit mask memory, pulse generator and pixel enable/disable logic.

4.4.1.1 SPAD

The photo detector has been selected from the SPAD farm because of the reasons mentioned in Section 3.2. The junction is formed between p+ and DNWELL. The diode is biased above breakdown in the Geiger mode, with the cathode biased at a constant voltage of 18.8 V, which is 1.8 V above the breakdown voltage. Whenever a photon strikes the SPAD, a voltage pulse is generated at anode.

4.4.1.2 Quenching and recharge circuitry

Upon design of a pn junction capable of withstanding relatively high voltages and whereby PEB is practically prevented, the device may be biased above breakdown into Geiger mode. As discussed earlier, in this mode of operation the avalanche must be quenched to prevent destruction of the device. There exist a variety of avalanche quenching techniques, active and passive, that perform this task, and a brief discussion of the same is made in Chapter 2.

In order to design a compact SPAD pixel, passive quenching with passive recharge seems to be the natural choice because it takes less area and it is simple to implement. Moreover, the diodes employed are fully integrable and small in size, implying small capacitance, and thereby leading to small dead time. Hence, passive quenching can provide suitable performance in this case.
Figure 4.12 shows a simple circuitry to perform passive quenching and recharging, with a typical recharge profile. Upon photon detection, buildup and spread force a current through the device and the ballast resistor; this in turn develops a voltage drop that significantly raises voltage $V(t)$, and the avalanche gets quenched [26]. After the avalanche gets quenched, the associated junction capacitance of the SPAD recharges to its original working condition through the ballast resistor. The total time required to quench and recharge the SPAD back to its working condition is called as the dead time of the SPAD. This process generates a current pulse that is converted to a digital voltage level by means of a pulse shaping circuitry, also shown in the figure.

The ballast device may be implemented as a resistor or as an active element acting as a nonlinear resistor (M1 in Fig. 4.12(a)). A resistor of a few kilo Ohms occupies an area on silicon too large to be utilized successfully. So the ballast resistor is designed using a NMOS transistor. Assuming that this NMOS can be approximated as a linear element, recharge voltage $V(t)$ yields:

$$V(t) \approx V_E \exp\left[-\frac{t - t_0}{RC}\right], \quad t \geq t_0 \quad (4.1)$$

where $R$ and $C$ are estimated overall resistance and capacitance to the ground at the cathode, and $V_E$ is the excess bias voltage, that is the voltage above breakdown at which the SPAD is biased. Time $t_0$ is the instant at which the quenching is complete. Since the tunable nature of the resistance allows control of dead time, an external control of the gate voltage of the NMOS transistor is provided. The resistance of MOS in linear region is given by:

$$R = \frac{1}{\frac{dI_{DS}}{dV_{DS}}} = \frac{1}{\frac{d[kL(V_{GS} - V_T)V_{DS} - V_{DS}^2]}{dV_{DS}}} = \frac{1}{kL(V_{GS} - V_T) - V_{DS}}^{-1} \quad (4.2)$$

Thus, longer channel in transistor or smaller $V_{GS}$ leads to larger resistance. The simulation plot in Figure 4.13 shows the range of resistance possible, from 40 k$\Omega$ - 1640 k$\Omega$ over different $V_{DS}$ values.

Resistance values of the order of 100-200 k$\Omega$ are desirable for quenching, hence NMOS with $\frac{W}{L} = \frac{0.232}{0.16}$ was chosen for quenching. Such sizing of NMOS transistor
Figure 4.13: Change in resistance with increasing length for $V_{GS} = 0.7$ V

allows sufficient tuning range, while taking minimum possible area. The change in the resistance with increasing $V_{GS}$ is shown in Figure 4.14.

4.4.1.3 Hot pixel elimination

Hot pixels consists of very noisy SPADs, also called as screamers. While calibrating the device, it can be made known if a particular SPAD is noisy. This can be achieved by monitoring the dark count rate for every pixel. If it crosses a set threshold, then that particular pixel can be labeled as hot pixel. This information can then be used enable/disable a pixel. A memory element is required to store and program the pixel with screamer data. In case of a hot pixel, the SPAD is disabled by increasing the voltage at anode, such that it is no longer biased in Geiger mode. This can be achieved in two ways. Either by using a separate SPADOFF transistor which when switched on raises the voltage at anode to $V_{DD}$, and thereby disables the SPAD. Another method is to cut off the quenching transistor. This also reduces the power consumption by disconnecting the SPAD from the ground path besides disabling it. This method requires two NMOS transistors to switch between ground and bias voltage. The former is required to turn off the quenching transistor in case of a screamer, and the latter to bias the quenching transistor for normal operation.

Several options were explored in this thesis to achieve the above mentioned functionality. A discussion of the same is mentioned below.
1. The first option is to switch off the noisy SPADs at a cluster level, rather than at the pixel level. As mentioned above, each SPAD array is built from a cluster, which in turn is made up of 2x2 pixels. So, a cluster of SPADs contains 4 pixels i.e. 4 detectors. If any of the detectors is hot, then the whole cluster is switched off. The advantage of the above method is that the cluster can be designed to be more compact since one memory element and switch will be shared in four pixels. However, the obvious drawback is the sacrifice of good pixels, and thus a reduction in sensitivity.

2. The second method involves associating a memory element and a switch with every individual pixel. Though this scheme might reduce the fill factor, but now only the real hot pixels will be eliminated. However, again in this scheme the memory element and switch can be placed outside the pixel array to increase fill factor. But, this might cause unwanted complexity with long interconnects.

Simple calculations based on the floor-plan revealed that it is more beneficial to choose for the elimination of screamers on pixel level with in pixel electronics. This choice would lead to optimum area usage for this application. The chosen SPAD has DNWELL, and technology rules constraint a minimum distance of 5 μm between two consecutive diodes, which can be utilized to put front end electronics. Hence, it is justified to eliminate screamers on a pixel level without compromising fill factor.

Two choices were explored to implement 1 bit memory element: flip flop and inverter based latch.
1. **Flip flop**
A conventional D flip flop can be used to implement the memory element. However, it requires more than 20 transistors and will reduce the fill factor substantially.

2. **Inverter based latch**
   It is a very compact 6 transistor structure as shown in Figure 4.15. Two external control signals set and reset the latch as per the requirement. However, the architecture has a limitation due to the presence of a race condition. Contention is possible in design as the functionality is strongly dependent on the sizing of the transistors, and hence a careful design is needed.

   However, this architecture is preferred over the flip flop because of its low transistor count and effective utilization of pixel area. The latch was simulated with corner cases and temperature variations to ensure a more robust design.

   Based on the value in the memory, a SPAD needs to be disabled/enabled. For this reason two NMOS switches are included in the pixel (refer Figure 4.16) for switching between GND if the SPAD is a screamer or to a bias voltage otherwise.

   A row-column approach as shown in Figure 4.17 is used to write the masking data to the 1 bit memory. During the calibration phase, masking data is generated and stored in a non-volatile memory present on chip. Each column is then activated, one at a time, which turns on the SET transistor of that column, and the data is written from this non-volatile memory to the complete column simultaneously. The activation logic of the column is implemented using a column decoder which is explained later in this section.

**4.4.1.4 Monostable**
Silicon LED (light source) being not efficient, makes Optical Joystick a photon starved application. Hence, a high acquisition rate of the SPAD (detector) arrays is very important to get the required photon count in a given time frame. However, the passively quenched SPAD pixel has a dead time of the order of few nanoseconds, which
limits the rate of detection of photons. Also, with spatial compression in SiPM, the output bitstream is the sum of the total number of photons detected by the SPAD array. So, whenever two or more pixels fire during the dead time, the photon count is lost. To reduce this unnecessary loss of photon count, temporal compression technique has been applied (refer Section 3.5), and a monostable logic is used to achieve this. A monostable is a device which when triggered, generates a single output pulse of a specified width, either “HIGH” or “LOW” that is independent of the input pulse width. This trigger signal initiates a timing cycle which causes the output of the monostable
to change its state at the start of the timing cycle and will remain in this second state, which is determined by the time constant of a capacitor C and a resistor R until it resets or returns itself back to its original (stable) state. It will then remain in this original stable state indefinitely until another input pulse or trigger signal is received. Hence, the output pulse width will be a function of the RC time constant.

In the SPAD pixel, the output of the detector which is a voltage pulse of the order of few nanoseconds is fed as an input to the monostable. The pulse generator is designed to reduce the width of the pulse, such that output pulse is between 1-10 ns. Therefore, the acquisition rate for the complete array is increased substantially and can count to a maximum of 500 MHz.

There are various pulse generators available with different features, although, all of them are based on the basic concept of the time constant implemented by resistor and capacitor. A conventional architecture (refer Figure 4.18) has been chosen in this thesis as it is simple and meets the area constraint of the pixel. The resistor is implemented by a MOS transistor, which gives an additional benefit to program the monostable and thereby control the pulse width between 1-10 ns. In order to realize a time constant of the order of 1-10 ns, a capacitor of 20 fF is required which is implemented using \textit{capNwellNpoly} process and takes an area of 2.4x2.8 \( \mu \text{m}^2 \). The MOS transistor can exhibit a resistance controllable from 8K to 600K by changing the MBIAS signal as shown in Figure 4.19.

The programmability of the monostable which is achieved by controlling the bias of MOS transistor externally is used to tune the output pulse width between 1- 10 ns as shown in Figure 4.20. This additional flexibility enables to modulate the pulse width depending on the photon count.

### 4.4.1.5 Pixel disable logic

Disabling the pixel implies biasing the SPAD at or below breakdown voltage such that photon detection is impaired, and hence any measurement associated with that pixel is stopped. This logic is included in the pixel for mainly two reasons:

1. To reduce the power consumption of the entire chip. When the SPADs are disabled, no avalanche pulses are generated when a photon strikes, and hence dy-
Figure 4.19: Change in resistance with increasing MBIAS for length = 320 nm

Figure 4.20: Different pulse widths in 1-10 ns range with programmable monostable
Dynamic power consumption is minimized.

2. To avoid unnecessary interference of the measurement process with the read out of the SPADs, and thereby ensuring clean results.

Once a measurement is completed, all the four SPAD arrays in each direction are disabled until new measurement cycle starts. There are several ways to achieve this functionality.

The most common method which has been employed in several designs in the literature is to connect the SPAD anode to a PMOS transistor as shown in Figure 4.21(a). The source of this MOS is connected to $V_{DD}$, and the gate is biased with SPADOFF signal. When SPADOFF is 0, M1 is switched on, and the anode is charged to $V_{DD}$, thereby biasing the SPAD below breakdown. This arrangement disables the pixel. The pixel is enabled by switching off the PMOS transistor when SPADOFF is logic high.

Though this technique avoids dynamic power consumption, a direct path to ground via quenching transistor leads to static power consumption. It can be avoided by switching off the quenching transistor whenever the pixel is disabled. This technique is used in this thesis and it can be achieved as shown in Figure 4.21(b).

When the SPADOFF signal is '1', the switch connected to ground is enabled, which in turn switches off the quenching transistor, thereby disabling the pixel. However, a MOS transistor connected to SPAD anode, as mentioned above is still added to clamp the voltage at SPAD anode to $V_{DD}$ when the pixel is disabled. This is a safe mechanism to ensure that voltage at anode does not overshoot to a random high value, thereby destroying the entire pixel.

4.4.1.6 Complete SPAD pixel circuit

After constructing each block individually, all the circuits are integrated to form the pixel. The complete pixel level circuit is shown in Figure 4.22. NAND based logic has been added to distinguish the valid output from invalid pulses.
Figure 4.22: SPAD pixel architecture
4.4.2 Cluster level circuit

In order to utilize the space more effectively in the array, four SPAD pixels are combined together with a nand gate to produce an active low output pulse as shown in Figure 4.23. This output bitstream is then read outside the array by other digital circuit. With this organization, only 80 interconnect wires need to be drawn out of the array for read out, instead of 320 wires, and hence it helps to reduce the required interconnect density and complexity.

4.4.3 Functional verification

In order to verify the functionality of detector module, it is important to model the behavior of SPAD diode. It is modeled as a switched voltage source of 18.8 V as shown in Figure 4.24. The capacitance at the anode is modeled as 400 fF.

Using the SPAD model described above, simulations were run on a cluster level to verify its functionality. SPADs in all the four pixels were triggered with photon inputs.
Second pixel is modeled as a hot pixel, and hence is disabled. The top four signals in Figure 4.25 show the photon trigger, SPAD output pulse and monostable output for each of the four pixels in the cluster. It can be seen that the output of second pixel is constant high, implying that the pixel is disabled. The last signal shows the combined output of all four pixels (output of cluster). We can see output pulses corresponding to photon trigger for each of first, third and fourth pixel. However, there is no pulse corresponding to the second pixel.

4.4.4 Full cluster layout implementation

To build the complete cluster, the basic blocks of pixel were first designed, following which the pixel layout was implemented. A modular approach, similar to circuit design was chosen. The basic blocks of pixel are quenching transistor, 6T inverter based latch, monostable and pixel enable/disable logic. In the pixel layout, it is important to consider the placing of metal lines as a sensitive SPAD photodetector is present in the pixel. A 45 degree incident angle of light on SPAD is desirable. To achieve this, the metal lines are placed such that their height from substrate is same as the distance from SPAD. Therefore, metal 1 is allowed to be closest to SPAD than other metals. The metal stack of 140 nm technology with ultra thick metal 5 is shown in Figure 4.26 and
throughout the pixel array layout, such spacing has been maintained as far as possible, except for metal 5 where 30 degree angle is maintained. The placement of each of the designed blocks and other interface logic was done to make the pixel more compact. The cluster layout consisting of four pixels and a nand gate in the center for generating output bitstream is shown in Figure 4.27(a). Apart from the layout of each block, routing of control inputs and outputs is critical as well. In the cluster layout, the control signals (set, reset, spadoff) are laid out in vertical direction in metal 4 whereas some other signals (an_spads_sensor_row, mbias, qbias) and output lines are laid out in horizontal direction in metal 3. This optimizes the area as fewer contacts are required. The signal routing is shown in Figure 4.27(b).
4.4.5 Building SPAD array

The cluster shown in Figure 4.2 is the basic building block for the array. 8 instantiations of this cluster were created to build a row of the array. 10 instantiations of this row were then created to build the complete array. The complete array layout is shown in Figure 4.28.

There are three power rails for the array - $V_{DD}$, GND and $V_{OP}$ (operating bias of SPAD). $V_{DD}$ runs in metal 5 and $V_{OP}$ in metal 4. Both of them run across the array. The GND plane is laid in metal 1, as it can maintain the closest distance to SPAD. Moreover, such a division reduces IR drop in array. Similar calculations like those mentioned for SPADlight array were carried out for SPAD array also to determine IR drop for different power rails. Since the current consumption is not very high, IR drop is small and is acceptable at system level. Also, electromigration is not of much concern due to small current density. Figure 4.29 shows the metal routing in the SPAD array, with GND plane layout on left, and $V_{OP}$ and $V_{DD}$ lines layout on the right of the figure.

4.4.6 SPAD read-out system

The digital nature of the signals generated in Geiger mode, which leads to significant advantages, also holds at least one drawback to be solved at circuit level. Since the parasitic capacitance of a SPAD is fully discharged upon photon detection, it is necessary to add extra circuitry to store photon-generated information. For instance, it might be important to add a counter, so as to store the information on how many photons the pixel has detected in a given time interval. On a conventional image sensor, this
information is stored on the photodiode capacitance (as an integrator). Since the number of transistors required for implementing at least one counter is by far larger than the number of transistors required at the pixel level for a conventional CMOS image sensor, the design of small SPAD pixels involves very important challenges.

A basic idea to address this challenge is to conceive a circuit that allows the designer to place all the circuits required for storage and timing evaluation outside the pixel array. Moreover, such a circuit should require as few transistors as possible to maximize fill factor. It is for this reason that a SiPM based readout was proposed for this application, where the output signal is the sum of the signals from a number of pixels fired by photons.

Here the SiPM sees discrete single photon events rather than large bursts of photons or the continuous flow of multiple overlapping photons. The corresponding charge output from the SiPM is thus many single short duration pulses consisting of the charge produced from single photons hitting the SiPM at random intervals. Under these conditions, the light is measured by counting the number of events over a time period. Since this technique is typically used when the light level is extremely low, it is highly suitable for this application. Moreover, it avoids the complexity of event driven readout, and is much faster than sequential read out [26].

To enable SiPM based readout, concatenation of digital OR gates have been used to sum up the output signals from all the clusters of the arrays. The output signal is a bitstream consisting of ‘1’s and ‘0’s which are counted to indicate photon count from the complete array. Four such bitstreams are generated from four SPAD arrays in each direction i.e. north, south, east and west.

Figure 4.30 shows different levels of hierarchy of OR gates for 1 SPAD array. The gates have been chosen from the standard library and are sized to drive the respective output capacitance at each level.
4.4.7 Spike filter

The process of summing up the outputs of individual clusters to generate a single output bitstream might cause very short glitches in the bitstream, which if provided as an input to the counter might cause it to enter meta stable state, and hamper the functionality of the complete system. To avoid this situation, a spike filter has been added. The spike filter takes a bitstream of '1's and '0's as an input, removes/widens all the spikes less than a specified duration, and produces a clean output bitstream. Glitch elimination by using delay elements is the most common technique. Several such circuits have been reported in literature. One of the most conventional spike filter circuit using inverter delay chain is reported in [42], and shown in Figure 4.31(a). The inverter delay chain is used to delay the input signal by a fixed amount, which is equal to the maximum glitch width which is to be suppressed. The delayed signal and the original signal are then compared. The output of the glitch filter is assigned to the input only when both the inputs have the same value. Figure 4.31(b) shows functional simulation of the glitch removal circuit. It shows the input bit stream with two negative glitches of less than 1 ns and an output signal which is glitch free.

It is evident from Figure 4.31 that, though the above glitch removal circuit can remove glitches as intended, it also combines two pulses separated by a glitch. Thus, the output signal has fewer pulses than the input. Since photon counting is the primary goal of this application, such loss of pulses is not desirable. Therefore, the architecture is modified as shown in Figure 4.32(a).

It uses 3 sequential delay elements, a XOR gate and a multiplexer. The first delay element receives the input signal with negative glitches. The first delay element and
the output of the multiplexer generate the intermediate signals X and Y respectively. If signals X and Y have the same logic values, then the intermediate control signal is logic low, and signal X is provided as an output of the multiplexer. However, if the intermediate signals have different logic values, then the control signal is high, and the current output signal is provided as an output of the multiplexer. Thus, the glitch in the input bit stream is widened by maintaining the previous logic value, i.e. high or low at the output signal during the bit transitions in the input bit stream and updating the new logic values at the output signal during the bit non-transitions in the input bit stream.

Therefore, in this architecture the glitch is not removed, but is widened enough such that counter does not enter meta stable state. Consequently, the output has the same number of pulses as input, and hence no photon count is lost, as can be seen in Figure 4.32(b).

This design has the advantage of widening all the glitches from the input bit stream rather than removing them, which is the major requirement for this application. The only shortcoming is that the bit width in the input bit-stream is shortened in the output signal. Since the application requires counting the number of ones in the bit-stream, so the reduction of pulse width is not of concern and can be tolerated. Hence, this architecture is preferred over other more complex designs suggested in [43][44].
4.4.8 Column decoder

Different decoder designs exist in the literature depending upon the logic family. A static logic decoder was chosen for its fast design time and ease of implementation. Although dynamic logic based decoders are smaller and faster, they pose issues such as leakage and their dynamic nature adds uncertainty to performance.

A 16:1 decoder was designed for selecting one column from 16 columns of SPAD array. This requires 4-bit control signals. 3 additional bits were added to the control signal. Two bits were needed to select the direction of the SPAD array i.e. north, south, east and west. The last bit is needed to have an enable control, such that no column is selected when the enable bit is '0'. This 7-bit control signal is generated from the digital block.
4.5 System integration

With the detector module, emitter module and other designed blocks in place, the system was built by integrating all the parts together. A modular design approach was followed to build the complete system. Emphasis was laid to make a symmetric system. Following the integration of the newly designed system, some blocks from the previous version like the digital module, non-volatile memory, charge pump and LED driver were also included. The last two blocks are included to power up and drive the non-silicon LED. Finally, the IO ring was included and all the remaining empty space was filled with decoupling capacitors. The floor plan of the full system is shown in Figure 4.33.

At first, a single array of detectors was created with 80 clusters, and then four instantiations were created. The emitter module was placed in the center of the chip,
with the four SPAD arrays (north, south, east and west) placed symmetrically around it. Digital OR gates for read-out and spike filter were placed close to the array in each direction to avoid long metal routing. It also ensures that the available area is not wasted and best put to use. After the placement of digital module and some other blocks, the interface signals were routed throughout the chip. Special care was observed while routing critical signals with long interconnects. The delay was approximated through RC network using Elmore delay model [41]. It uses the delay of individual wire segments to estimate the final delay between two nodes. Critical interconnects were designed to be wider to reduce resistance, or laid out at a distance from other metals to reduce coupling capacitance. Input-output pads were placed on the left part of the chip. Power rails run across the arrays and all around the system. Two different grounding schemes were implemented, one for SPADlight ground, and the other for rest of the array. The power tracks were designed sufficiently wide to limit the IR drop and electromigration effect. The complete system layout can be seen in Figure 4.34.
4.6 Summary

In this chapter, a detailed discussion was given of the circuit design of emitter and detector modules and its implementation in a standard 140 nm CMOS technology. We first discussed the pixel level building blocks, following which the array was designed and finally the overall system was built. The next chapter presents the characterization of the designed chip.
In the previous chapters, a detailed discussion of the design and implementation of the designed optical joystick system was made. In this chapter, the obtained characterization results are presented and discussed with respect to system requirements. The chapter is organized as follows. Section 5.1 gives testing overview, with hardware and software setup explained in Section 5.2 and Section 5.3 respectively. Section 5.4 discusses the SPAD measurement results in detail. Section 5.5 presents SPADlight measurement results, while system level results are presented in Section 5.6. Section 5.7 shows chip photograph.

5.1 Testing methodology

In this chapter, the complete testing and characterization of the designed optical joystick system is presented. A bottom up testing methodology was followed. In this approach, the basic functional modules like I²C, digital, detector, and emitter are tested first. Then these modules are grouped together at various levels and tested accordingly. The procedure of testing the chip by grouping the various components is followed until the desired functionality of angle detection is tested. The chip is also characterized for various performance parameters of noise, sensitivity and timing. Power consumption and temperature behavior were also evaluated. In order to carry out all these testing and characterization activities, an extensive evaluation set up was designed. The fabricated chip was first bonded and packaged in standard DIL40 ceramic package. (The bonding diagram and pin list can be found in Appendix A). Next, a testing board and software were designed as explained in the following sections.

5.2 Hardware setup

The hardware setup includes an evaluation board and a Connii MM USB-I²C interface connection box. The schematic of the evaluation board is shown in Figure 5.1. It has a very simple design, and it mainly consists of a socket for DIL40 package, direct connections of the chip pins including VDD/GND pins, some decoupling capacitors and a jumper. When a jumper closes the connection, the VDD of the board can be supplied by the I²C interface, or the I²C can get its VCC reference from the board.

Additionally, the evaluation-board has been designed to be pin-compatible with an I²C-Bird USB interface. However, the software is designed for using a Connii MM2 USB-I²C interface. In order to connect this interface to the evaluation board, a specific cable is used. The hardware setup including evaluation board and Connii MM2 box can be seen in Figure 5.2(a).
As stated before, for joystick functionality measurements involving angle and tilt, a mirror is required. Hence, a micrometer based setup for controlling the motion of the mirror was used and is shown in Figure 5.2(b).

5.3 Software

The software enables to exhaustively tune (control, setup, customize and test) the designed optical joystick system, communicating via Connii MM interface (USB-to-I²C communication). It is developed in Labview 8.5. The software allows to access all the features that are built-in the chip and controllable by the I²C interface, including
configurable reading/writing, intuitive measurement display and quick access to main functions of setup, calibrate, save/load from memory etc. A snapshot of the designed user interface can be seen in Figure 5.3.

5.4 SPAD Measurement Results

This section includes the characterization of SPAD for breakdown voltage, noise, sensitivity, timing resolution, afterpulsing, crosstalk, and a brief discussion is made on the same.

5.4.1 Breakdown Voltage

Breakdown voltage ($V_{bd}$) is defined for a p-n junction to be the voltage when the mean ionization per free carrier, integrated over p-n junction’s depletion region exceeds one [45]. There are different ways to measure the breakdown voltage, two of which are used in this thesis.

1. The I-V method

In this method the quenching resistance of the diode is set low enough, and a resistance-limited I-V curve is acquired by measuring the current output from $V_{OP}$. The voltage at which the current increases suddenly from few nanoamperes to few microamperes is calculated as breakdown voltage. The disadvantage of this method is that the presence of quenching resistor might limit the current, and thereby distort the measurement. The breakdown voltage for the measured SPAD pixel is calculated to be 16.8 V.
2. The sweep and subtract method

This technique relies on the knowledge of the threshold voltage of the comparator at the output of the SPAD. In this method, $V_{OP}$ is swept until pulses appear at the output of the thresholder, with $V_{bd} = V_{OP} - V_{th}$. The breakdown voltage for the same pixel is calculated to be 16.7 V. The disadvantage of this method is that the threshold voltage might vary due to supply voltage and temperature. Also, the height of the output pulses from SPAD might vary, and trigger the comparator at different times. Both these conditions can cause distortions in the measurements.

Figure 5.4 shows the plot of breakdown voltage for a single SPAD as a function of temperature. Both the above methods have been compared for $V_{bd}$ estimation as seen in the graph. The $V_{bd}$ estimates from the I-V method are slightly higher than those from the sweep and subtract method, and are within the range of 150 mV. It can be seen that breakdown voltage increases linearly with temperature, and varies from 15.9 at $-40^\circ$C degree to 17.25 at $65^\circ$C. This experiment is also necessary to correctly characterize the measurements presented hereafter, as $V_{OP}$ should be set for a given temperature to reflect the correct excess bias voltage.

5.4.2 Photon Detection Probability

As mentioned before, photon detection probability is the measure of sensitivity of SPAD. PDP was measured with a measurement set up consisting of a monochromator (Oriel/Newport part 77250) and an integration sphere (Oriel/Newport part 819D-SL-2). A 150 W Xenon lamp was focused on the entrance slit of the monochromator. The output slit of the monochromator was used to illuminate the input port of the integrating sphere, thus providing a monochromatic light beam. The integrating sphere has a calibrated photodiode (Hamamatsu part S1226-BQ) used as a reference at one of the ports. Its photogenerated current is measured, and is used to determine the photon
flux at the output port. The device under test or SPAD is placed on the second output port [26].

Based on the proposed setup, PDP measurements were obtained as a function of incident photon wavelength for different excess biases. The measurements were performed at room temperature from 360 nm to 800 nm as shown in Figure 5.5. It is higher than 30% between 460 nm to 560 nm at 4V excess bias, with a peak of 43% at 480 nm.

5.4.3 Dark Count Rate

As stated earlier, the dark noise is a random event generated by a photon detector in the dark. The generated dark noise can be due to two reasons viz. trap assisted thermal generation noise and band-to-band tunneling noise [46]. For a given SPAD the trap assisted thermal generation noise increases with temperature, whereas the band-to-band tunneling noise depends on the electric field applied across the depletion region. Hence, the band-to-band tunneling noise increases with the bias voltage applied across the SPAD. In literature dark noise of a photon detector is characterized using the Dark Count Rate (DCR). The DCR is measured by counting the number of avalanches observed in one second, when the photon detector is placed in dark. The DCR of a photon detector determines the lower limit for the light intensity that can be detected reliably. Since the optical joystick application has photon-starved light source, it is important to have pixels with low dark count rate.

Figure 5.6 shows the DCR distribution over 20x16 pixel array under 2V excess bias and 3 different temperatures. As can be seen from the figure, 92% of the pixels exhibit DCR lower than 12 Hz at 25°C. The median value of DCR is only 9.5 Hz which leads to an outstanding median DCR density of 0.75 Hz/um². Only 1% of the pixels has DCR higher than 1 kHz. Such low value of DCR can be attributed to small active area and outstanding cleanliness of the CMOS process. Moreover, these high DCR pixels can be switched off by circuit level techniques. This is important for this application.
Figure 5.6: Distribution of DCR with respect to normalized pixel count. The measurement was performed at $-40\, ^\circ\text{C}$, $25\, ^\circ\text{C}$ and $65\, ^\circ\text{C}$ at $V_E = 2\text{V}$.

to achieve wide dynamic range and uniform DCR in four direction SPAD arrays.

5.4.3.1 Effect of temperature and excess bias voltage on DCR

The measurement result of median DCR as a function of temperature for different excess bias voltages is shown in Figure 5.7. The breakdown voltage has been compensated for temperature to reflect true excess bias voltage. From Figure 5.7, it can be inferred that the median DCR of the pixel array reduces with the SPAD bias voltage and with the temperature as expected. From the plot, it can be observed that the median DCR of the pixel reduces to around 2 Hz at $-40\, ^\circ\text{C}$ and 2V excess bias voltage. From these results it can be inferred that the DCR of the SPAD at room temperature corresponds mainly to the trap assisted thermal generation noise. Figure 5.8 shows the same information, with median DCR as a function excess bias voltage for different temperatures.

5.4.3.2 Masking of high DCR pixels

Masking of hot SPAD pixels represents a tradeoff between PDE and DCR. Switching off certain number of pixels will reduce DCR considerably; however, at the same time it will also cause a loss in PDE. The plot in Figure 5.9 shows the tradeoff between PDE and DCR for 1-5% masking of pixels for 3 different temperatures. It has been assumed that PDE does not vary with temperature.

It can be seen from the graph that PDE reduces linearly as expected, from 0.93% at 1% masking of pixels to 4.65% at 5% masking. The X axis of the graph shows that DCR reduces from approximately 93% to 98% while masking 1% to 5% pixels respectively at all three temperatures. It can be seen that DCR reduces exponentially until 1% pixel masking, and after that the reduction in DCR is negligible, while PDE keeps on decreasing linearly. Hence, it can be concluded that 1% of hot pixel masking is
5.4.4 Afterpulsing

An afterpulse is an unwanted avalanche triggered by trapped carriers released during the SPADs recharge time [20]. In dark conditions, the distribution of times between SPAD avalanches should follow the poisson statistics. However due to these unwanted avalanches, the count rate of SPAD does not follow a pure exponential curve. The afterpulsing probability at a specific dead time can be found by taking the inter-avalanche time histogram [45], fitting an exponential to the uncorrelated noise source, and then finding the fraction of events above the fit curve but below the experimental curve.

Figure 5.7: Median DCR as a function of temperature for different excess bias voltages.

Figure 5.8: Median DCR as a function of excess bias voltage for different temperatures.
Figure 5.9: Effect of masking on PDE and DCR. The measurement was performed at $-40\, ^\circ C$, $25\, ^\circ C$ and $65\, ^\circ C$.

Figure 5.10: Inter-avalanche time measurement at 25 ns dead time. The afterpulsing probability is negligible.

The measurement set up consisted of a high performance oscilloscope, LeCroy 8600A which is used to sample and store the waveform. The SPAD was biased at 4V excess bias and illuminated with a constant LED light source. Figure 5.10 shows the measured plot for inter-avalanche time histogram, and an ideal exponential line for comparison. The inset shows the zoom of the main plot until 80 ns of inter-avalanche time. We can see that the SPAD is almost free from afterpulsing, with 2.5% afterpulsing at 25 ns dead time.
5.4.5 Crosstalk

Optical crosstalk is similar to afterpulsing, except that inter-pulses statistics are performed between different SPADs. It can also be observed how a typical SPAD with low DCR is affected by switching on and off a neighboring noisy SPAD (15 μm distance). It can be seen from Figure 5.11 that the array is free from optical crosstalk since the counts from the low DCR SPAD are not affected by high DCR SPAD. It can be concluded from the measurement that crosstalk is less than 0.01% due to very small parasitic capacitance.

Electrical crosstalk was eliminated by design. Minor carriers diffusing in the substrate cannot reach the multiplication region of a pixel since they would be collected by the deep n-well/p-substrate junction.

5.4.6 SPAD Jitter

Timing jitter of a SPAD is the uncertainty of the time interval between the arrival time of the photon at the SPAD and the time when the pulse is generated [20]. To evaluate the timing jitter, the SPAD is illuminated by a picosecond laser source emitting pulses at 40 MHz repetition rate with 405 nm of wavelength. Since the laser intensity is very strong, a neutral density filter (NDF) is inserted between the SPAD and the laser to prevent pile-up effect as shown in Figure 5.12. The time interval between the trigger from the laser and the rising edge of the pulse from the SPAD is measured using a high performance oscilloscope (LeCroy 8600A). By iterating this measurement, a histogram of the time interval is created.

The timing jitter including laser, SPAD and system jitter is shown in Figure 5.13 at different excess bias voltages. It reduces from 130 ps at 1 V excess bias to 118 ps at 4 V excess bias. Figure 5.14 shows the jitter measurement for the same pixel at 2 V excess bias after enabling the complete array to study the effect of coupling and noise. It can
be seen that measurements are almost identical and in accordance with the scalability of SPAD to large arrays.

Figure 5.14: Comparison of timing jitter at 2 V excess bias before and after enabling complete SPAD array.
Figure 5.15: Sensor count rate as a function of SPADlight power consumption

5.5 SPADlight Measurement Results

An experiment was performed to measure the sensor count rate as a function of power consumed by SPADlight array. The noisier SPADs of the array were disabled, such that 305 of the 320 SPADs were active and counting during the measurement. The total dark count rate was lower than 1.3 kHz. Each SPADlight cluster was enabled incrementally, until the complete array was operating.

A graph showing the number of counts in the array as a function of optical power for different number of enabled SPADlight clusters is shown in Figure 5.15. A total integration time of 1 ms was used in the measurement. The sensor dynamic range, limited by the dark count rate shot noise in the low end is around 55 dB. Considering the fact that the efficiency of silicon LED is 3-4 orders of magnitude less than other non-silicon light sources, 30 dB dynamic range is considerable and sufficient for this application.

5.6 System Measurement Results

To demonstrate the functionality of the complete system two types of measurements were performed. The first measurement showed click detection, and the second measurement confirmed angle detection; the two basic functions of a joystick. A micrometer based set up, as mentioned in Section 5.2, was used for aligning a mirror on the top of the chip and controlling its motion and tilt.

5.6.1 Intensity Measurement

In this experiment, the mirror was aligned perpendicularly at a particular distance from the chip, and the count rate was measured for that distance. Next, the distance of the
mirror from the chip was increased as shown in Figure 5.16. Figure 5.17 shows the light intensity measured as a function of the distance of the mirror from the chip. (The distance values on the X axis of the graph are obtained from visual inspection and might not be very accurate). It can be seen from the graph that the light intensity decreases when the distance of the mirror from the chip increases, and vice-versa. The result is in accordance with the expectation and demonstrates successful click detection.

5.6.2 Tilt Measurement

In this set of experiments, the mirror was aligned perpendicularly at a particular distance from the chip, such that the count rate was equal in all directions; indicating neutral position of the joystick. Next, the mirror was tilted in one direction (top) incrementally as shown in Figure 5.18. An increase in the count was observed for that direction, while the counts decreased in the bottom direction. This motion replicated the tilt of the joystick.
Figure 5.18: Experimental setup for measuring tilt.

Figure 5.19: Increasing counts in the top direction array and decreasing counts in the bottom direction array for positive tilt.

Figure 5.19 shows the same information. The motion was restricted to (+/-) 3 degrees due to the physical limitations of the evaluation set up. Figure 5.20 shows the difference in the counts of top and bottom directions as a function of tilt angle for different distances of the mirror from the chip. It can be seen that the distance increases with tilt angle to some extent. But at higher distance and greater tilt, the light circle from the chip is shifted and hence the count difference reduces. These two experiments successfully demonstrates the detection of the tilt of the joystick.

5.7 Chip Photomicrograph

Figure 5.21 shows the photomicrograph of the designed chip. It has been fabricated in a standard 140 nm CMOS process, and occupies an area of 1.7x1.5 mm$^2$. The chip has a total transistor count over 100K.
Figure 5.20: Measured count difference as a function of tilt for different distances of the mirror from the chip.

Figure 5.21: Chip Photomicrograph

5.8 Summary

This chapter presented the evaluation setup and characterization results of the designed optical joystick system implemented in a standard 140 nm CMOS technology. The SPAD array has been characterized for noise, sensitivity and timing behavior. The
system level results substantiate the desired functionality of the system with successful
demonstration of angle and click detection.
Conclusion

6.1 Summary

In this thesis, a monolithically integrated optoelectronic system was designed for an “Optical Joystick” application in a standard CMOS process, for the first time. The system was built after careful study aimed at finding the best light emission and detection devices for the desired specifications. The developed system has the advantage of integrating the light source and sensors in a single silicon, thereby leading to reduced costs and better yields. The first phase of this thesis consisted of performing preliminary experiments to prove the system concept, leading to design, development and characterization in the subsequent phases.

The designed system consists of 16x16 array of pixels of CMOS light emitting diodes (LEDs), and four 16x20 array of pixels of single-photon avalanche diodes (SPADs) in each direction of top, bottom, left and right. A mirror is mounted on top of the chip. The different positions of the joystick involve different photodiode illumination which is indicated by the photon count in each direction. This data is then analyzed by the digital logic to give usable click and tilt information.

The system is divided into emitter, detector and digital module. The emitter module consists of LEDs biased in reverse mode above breakdown voltage. These LEDs are “SPADlight” and emit light in the visible spectrum. Each cluster of SPADlight has 2x2 pixels and is controlled by its own driver. This leads to an additional flexibility of enabling as many clusters as required, depending on the light intensity.

The detector module consists of SPADs, also operating in Geiger mode. Each pixel can detect photons depending on the light intensity, and also incorporates hot pixel elimination and temporal compression. Masking of hot pixels helps to reduce DCR considerably, and is achieved by including a 1 bit memory cell in the pixel. Temporal compression is realized with a monostable element which reduces pulse width, thereby increasing dynamic range. Each pixel has a size of 19x19 \( \mu \text{m}^2 \), with 3.5% fill factor. 16x20 SPAD pixels are arranged in the form of a silicon photomultiplier (SiPM), summing the output of all pixels to give the desired intensity information. Four such identical SiPMs are included, and the light intensity from each one of them is compared to detect angle and click information of joystick. Digital logic is also included in the chip for providing control and configuration information.

The developed system was characterized for noise, sensitivity and timing information. Afterpulsing, crosstalk and temperature behavior of DCR was also evaluated. The results are summarized in Table 6.1. The system achieves remarkably low median DCR of 9.5 Hz at 2 V excess bias and room temperature, and it further reduces to 2 Hz when cooled to \(-40^\circ\text{C}\). To conclude, some experiments were preformed with a mirror for intensity and angle detection. Change in the light intensity from SiPMs was observed.
with the vertical movement and tilt of the mirror which successfully demonstrates the concept of optical joystick.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Measured value</th>
<th>Specifications</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Emitter (SPADlight(p+))</strong></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Breakdown Voltage</td>
<td>8V</td>
<td>8V</td>
</tr>
<tr>
<td>Current Consumption</td>
<td>0.1N mA, N=1 to 64</td>
<td>1N mA, N=1 to 64</td>
</tr>
<tr>
<td>Operation Frequency</td>
<td>100 Hz (Maximum)</td>
<td>100 Hz</td>
</tr>
<tr>
<td>Duty Cycle</td>
<td>20% to 60%</td>
<td>20% to 60%</td>
</tr>
<tr>
<td>Pixel Pitch</td>
<td>20μm</td>
<td>20μm</td>
</tr>
<tr>
<td>Array Size</td>
<td>16x16</td>
<td>16x16</td>
</tr>
<tr>
<td><strong>Detector (SPAD)</strong></td>
<td></td>
<td></td>
</tr>
<tr>
<td>SPAD Active Area</td>
<td>4μm diameter</td>
<td>4μm diameter</td>
</tr>
<tr>
<td>Breakdown Voltage</td>
<td>16.8V</td>
<td>17V</td>
</tr>
<tr>
<td>Sensitivity Spectrum</td>
<td>400-600nm (≥ 1% PDP)</td>
<td>400-600nm (≥ 1% PDP)</td>
</tr>
<tr>
<td>PDP</td>
<td>23% peak at 480nm (V_E=2V)</td>
<td>22% peak at 480 nm (V_E=2V)</td>
</tr>
<tr>
<td>Median DCR(25°C)</td>
<td>9.5 Hz</td>
<td>&lt; 800 Hz</td>
</tr>
<tr>
<td>Median DCR(−40°C)</td>
<td>2 Hz</td>
<td>-</td>
</tr>
<tr>
<td>SPAD Jitter</td>
<td>120 ps</td>
<td>-</td>
</tr>
<tr>
<td>Crosstalk</td>
<td>≤ 0.01%</td>
<td>-</td>
</tr>
<tr>
<td>Afterpulsing</td>
<td>negligible until 25 ns</td>
<td>-</td>
</tr>
<tr>
<td>Pixel Pitch</td>
<td>19μm</td>
<td>19μm</td>
</tr>
<tr>
<td>Pixel Fill Factor</td>
<td>3.5%</td>
<td>4%</td>
</tr>
<tr>
<td>Array Size</td>
<td>20x16</td>
<td>20x16</td>
</tr>
<tr>
<td>Saturation Count Rate</td>
<td>150 MHz</td>
<td>500 MHz</td>
</tr>
<tr>
<td><strong>System</strong></td>
<td></td>
<td></td>
</tr>
<tr>
<td>CMOS Process</td>
<td>140 nm</td>
<td>140 nm</td>
</tr>
<tr>
<td>Chip Area</td>
<td>1.7x1.5 mm²</td>
<td>1.5x1.5 mm²</td>
</tr>
<tr>
<td>Frame Rate</td>
<td>10-100Hz</td>
<td>10-100Hz</td>
</tr>
<tr>
<td>Power Consumption</td>
<td>5 mW (N=6)</td>
<td>≤ 1 mW</td>
</tr>
</tbody>
</table>

Table 6.1: Optical joystick performance summary

### 6.2 Future work

The work done in this thesis achieves the desired set of goals, and successfully proves the concept of monolithic integration of light source and sensors in a standard CMOS
process. However, more work needs to be done before this design can be packaged into a commercial product. In this section, a few recommendations are made.

1. The SPADlight diodes should be characterized for emission spectrum and timing response.

2. SPADlight being the major source of power consumption, a better design for such diodes should be proposed, or such SPAD sensors should be used which are more sensitive to the emission spectrum of emitter.

3. Currently, the process rules for the selected SPAD design layers restrict the pixel size, and hence the fill factor to 3-4%. A new design of SPAD should be proposed with minimal layout restrictions, or better design techniques like DNWELL sharing with multiple SPADs, implementing electronics in DNWELL, guard ring width optimization etc. can be explored.

4. High voltage required for operating SPADs and SPADlights should be generated on chip.

5. An optics based model should be proposed to understand and quantify the change in light intensity with the movement and tilt of the mirror.

6. The proposed monolithically integrated optoelectronic system should be extended to other low light and low cost applications.
Figure A.1: Bonding diagram of the chip for DIL40 package.
<table>
<thead>
<tr>
<th>Package pin</th>
<th>Chip pin name</th>
<th>Direction</th>
<th>Comments</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>VOP25V</td>
<td>-</td>
<td>High voltage for SPAD sensors</td>
</tr>
<tr>
<td>2</td>
<td>QBIAS</td>
<td>IN</td>
<td>0-1.8 V</td>
</tr>
<tr>
<td>3</td>
<td>MBIAS</td>
<td>IN</td>
<td>0-1.8 V</td>
</tr>
<tr>
<td>4</td>
<td>RESET</td>
<td>IN</td>
<td>Asynchronous reset, active low</td>
</tr>
<tr>
<td>5</td>
<td>LEDVDD3V3</td>
<td>-</td>
<td>Power supply for solid-sate LED</td>
</tr>
<tr>
<td>6</td>
<td>TESTOUT2</td>
<td>IN/OUT</td>
<td>Test pin 2</td>
</tr>
<tr>
<td>7</td>
<td>VDD</td>
<td>-</td>
<td>Power supply - 1.8 V</td>
</tr>
<tr>
<td>8</td>
<td>TESTOUT1</td>
<td>IN/OUT</td>
<td>Test pin 1</td>
</tr>
<tr>
<td>9</td>
<td>GND</td>
<td>-</td>
<td>Shared ground of the chip</td>
</tr>
<tr>
<td>10</td>
<td>TESTOUT3</td>
<td>IN/OUT</td>
<td>Test pin 3</td>
</tr>
<tr>
<td>11</td>
<td>SCL</td>
<td>IN</td>
<td>I2C standard port (clock)</td>
</tr>
<tr>
<td>12</td>
<td>GND</td>
<td>-</td>
<td>Second ground</td>
</tr>
<tr>
<td>13</td>
<td>SDA</td>
<td>IN/OUT</td>
<td>I2C standard port (data)</td>
</tr>
<tr>
<td>14</td>
<td>PORTEST</td>
<td>OUT</td>
<td>Power-on-reset</td>
</tr>
<tr>
<td>15</td>
<td>SADDR</td>
<td>IN</td>
<td>I2C standard port</td>
</tr>
<tr>
<td>16</td>
<td>IRQ</td>
<td>OUT</td>
<td>Interrupt request</td>
</tr>
<tr>
<td>17</td>
<td>FILTST</td>
<td>IN</td>
<td>High speed test pin</td>
</tr>
<tr>
<td>18</td>
<td>hsp</td>
<td>OUT</td>
<td>High speed test pin</td>
</tr>
<tr>
<td>19</td>
<td></td>
<td>-</td>
<td>-</td>
</tr>
<tr>
<td>20</td>
<td>VOP12V</td>
<td>-</td>
<td>High voltage for SPADlight</td>
</tr>
</tbody>
</table>

Table A.1: Chip pin list description.
<table>
<thead>
<tr>
<th>Name</th>
<th>Address</th>
<th>Access</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>ACC_LEFT_2</td>
<td>0Eh</td>
<td>R</td>
<td>Raw measurement of the left SPAD sensors, bits [23:16]</td>
</tr>
<tr>
<td>ACC_LEFT_1</td>
<td>0Fh</td>
<td>R</td>
<td>Raw measurement of the left SPAD sensors, bits [16:8]</td>
</tr>
<tr>
<td>ACC_LEFT_0</td>
<td>10h</td>
<td>R</td>
<td>Raw measurement of the left SPAD sensors, bits [7:0]</td>
</tr>
<tr>
<td>ACC_RIGHT_2</td>
<td>11h</td>
<td>R</td>
<td>Raw measurement of the right SPAD sensors, bits [23:16]</td>
</tr>
<tr>
<td>ACC_RIGHT_1</td>
<td>12h</td>
<td>R</td>
<td>Raw measurement of the right SPAD sensors, bits [16:8]</td>
</tr>
<tr>
<td>ACC_RIGHT_0</td>
<td>13h</td>
<td>R</td>
<td>Raw measurement of the right SPAD sensors, bits [7:0]</td>
</tr>
<tr>
<td>ACC_BOT_2</td>
<td>14h</td>
<td>R</td>
<td>Raw measurement of the bottom SPAD sensors, bits [23:16]</td>
</tr>
<tr>
<td>ACC_BOT_1</td>
<td>15h</td>
<td>R</td>
<td>Raw measurement of the bottom SPAD sensors, bits [16:8]</td>
</tr>
<tr>
<td>ACC_BOT_0</td>
<td>16h</td>
<td>R</td>
<td>Raw measurement of the bottom SPAD sensors, bits [7:0]</td>
</tr>
<tr>
<td>ACC_TOP_2</td>
<td>17h</td>
<td>R</td>
<td>Raw measurement of the top SPAD sensors, bits [23:16]</td>
</tr>
<tr>
<td>ACC_TOP_1</td>
<td>18h</td>
<td>R</td>
<td>Raw measurement of the top SPAD sensors, bits [16:8]</td>
</tr>
<tr>
<td>ACC_TOP_0</td>
<td>19h</td>
<td>R</td>
<td>Raw measurement of the top SPAD sensors, bits [7:0]</td>
</tr>
<tr>
<td>SPADS_LIGHT_0</td>
<td>2Ah</td>
<td>R/W</td>
<td>Light-emitting SPADS control row 0</td>
</tr>
<tr>
<td>SPADS_LIGHT_1</td>
<td>2Bh</td>
<td>R/W</td>
<td>Light-emitting SPADS control row 1</td>
</tr>
<tr>
<td>SPADS_LIGHT_2</td>
<td>2Ch</td>
<td>R/W</td>
<td>Light-emitting SPADS control row 2</td>
</tr>
<tr>
<td>SPADS_LIGHT_3</td>
<td>2Dh</td>
<td>R/W</td>
<td>Light-emitting SPADS control row 3</td>
</tr>
<tr>
<td>SPADS_LIGHT_4</td>
<td>2Eh</td>
<td>R/W</td>
<td>Light-emitting SPADS control row 4</td>
</tr>
<tr>
<td>SPADS_LIGHT_5</td>
<td>30h</td>
<td>R/W</td>
<td>Light-emitting SPADS control row 5</td>
</tr>
<tr>
<td>SPADS_LIGHT_6</td>
<td>31h</td>
<td>R/W</td>
<td>Light-emitting SPADS control row 6</td>
</tr>
<tr>
<td>SPADS_LIGHT_7</td>
<td>62h</td>
<td>R/W</td>
<td>Light-emitting SPADS control row 7</td>
</tr>
<tr>
<td>TESTREG_SPADS</td>
<td>62h</td>
<td>R/W</td>
<td>Test register containing settings for SPADs tests</td>
</tr>
<tr>
<td>SPADS_ROW_2</td>
<td>63h</td>
<td>R/W</td>
<td>enable/disable SPAD pixels [23:16]</td>
</tr>
<tr>
<td>SPADS_ROW_1</td>
<td>64h</td>
<td>R/W</td>
<td>enable/disable SPAD pixels [15:8]</td>
</tr>
<tr>
<td>SPADS_ROW_0</td>
<td>65h</td>
<td>R/W</td>
<td>enable/disable SPAD pixels [7:0]</td>
</tr>
<tr>
<td>SPADS_SET</td>
<td>66h</td>
<td>W</td>
<td>Program SPAD columns</td>
</tr>
</tbody>
</table>

Table B.1: I2C register map.


