Single-grain Si thin-film transistors on flexible polyimide substrate fabricated from doctor-blade coated liquid-Si

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Solution process of silicon will provide high-speed transistor fabrication with low-cost by, for example, roll-to-roll process. In this paper, a low-temperature process (350 °C) is reported for fabrication of high-quality Si devices on a polyimide substrate from doctor-blade coated liquid-Si. With this method, different semiconductor devices have been fabricated, reporting a carrier mobility of 460 cm^2/V s and 121 cm^2/V s for electrons and holes, respectively. The devices were peeled off and transferred onto a polyethylene naphthalate foil to achieve flexible devices. CMOS inverters were also fabricated and show full output swing. © *2013 AIP Publishing LLC*.
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Printed flexible electronics have received considerable attention because of the low-cost and applications in displays, sensors, and radio-frequency identification (RFID) tags on flexible substrates. Organic semiconductors offer a low-temperature printing process of TFTs on plastic substrates.[1] However, the carrier mobility and reliability are much inferior in comparison with Si devices. Indium Gallium Zinc Oxide (IGZO), as a metal oxide semiconductor, shows higher electron carrier mobility than that of organic semiconductors, but it is impossible to make both PMOS and NMOS TFTs using the same metal oxide.[2] Transferring of CMOS-SOI chips[3] and amorphous Si (a-Si) transistors on plastics by laser release[4] have been reported. However, the former has cost and technical issues since the limited size of the wafer and pick and place process, and in the latter, the electrical performance is low, although the laser release technique requires less cost. Printing of silicon, however, could provide high carrier mobility[5,6] and at the same time the possibility of fabricating NMOS and PMOS TFTs in the same process on a large area substrate. Silicon can be printed using liquid silicon,[5] which is a mixture of ultraviolet (UV)-irradiated cyclopentasilane (CPS) and a solvent. After forming a-Si by sintering spin-coated liquid-Si at 430 °C followed by dehydrogenation, poly-Si TFTs[5] and single-grain Si TFTs[6] have been fabricated with excimer-laser crystallization. Although mobilities of the resultant TFTs are much superior to those of organic TFTs, the dehydrogenation process with a temperature of more than 550 °C is not suitable for polymeric substrates. In this paper, we report in the fabrication of single-grain Si TFTs on a polyimide-coated substrate with a maximum process temperature of 350 °C using liquid-Si, which was deposited by doctor-blade coating, which is compatible with a roll-to-roll process. The carrier mobility is 460 cm^2/V s and 121 cm^2/V s for electrons and holes, respectively. The devices were peeled off and transferred onto a Polyethylene naphthalate (PEN) foil to achieve flexible devices.

As shown in Fig. 1, first, a quasi-plastic substrate is prepared with spin-coating 10-μm-thick polyimide layer on top of a supporting crystalline Si substrate, which is subsequently cured at 400 °C. Then, by the μ-Czochralski process,[7] small indentations called "grain-filters" (100 nm diameter and 750 nm depth) are made in 4-μm-thick SiO_2 deposited by plasma-enhanced chemical vapor deposition (PECVD) of tetraethyl orthosilicate (TEOS) at 350 °C on the substrate, on which pure CPS (without solvents) is coated using a Si_3N_4 doctor-blade in a low oxygen-level environment (<10 ppm). To polymerize the layer and increase the boiling point, the coated CPS is irradiated with UV lamp for 20 min. Then the polysilane layer was transformed to a-Si film with a thickness of 100 nm by a 1-h thermal treatment at 350 °C on a hot plate in the same environment. This temperature is lower than the 430 °C reported in the previous studies.[5,6] The cross-section of a grain-filter completely filled with the a-Si (see supplemental material[8]). The Raman spectroscopy of the layer shows a broad peak at around 480 cm^{-1}, which indicates that the film was converted into a-Si (see supplemental material[8]). Hydrogen concentration in the layer is measured to be 13 at. % by Elastic Recoil Detection (ERD) (see supplemental material[8]).

For crystallization of the a-Si film, a XeCl excimer-laser (308 nm, 250 ns) is employed. To avoid Si eruption due to hydrogen effusion during the laser irradiation,[6] the sample is dehydrogenated by laser annealing using the same laser with multiple shots at lower energies. During the laser, the energy density is gradually increased from 300 mJ/cm^2 to 900 mJ/cm^2 with steps of 50 mJ/cm^2, while the number of shots for each energy density is decreased from 100 to 1 with a step of 10 shots. After laser annealing until 500 mJ/cm^2, the peak hydrogen concentration decreases

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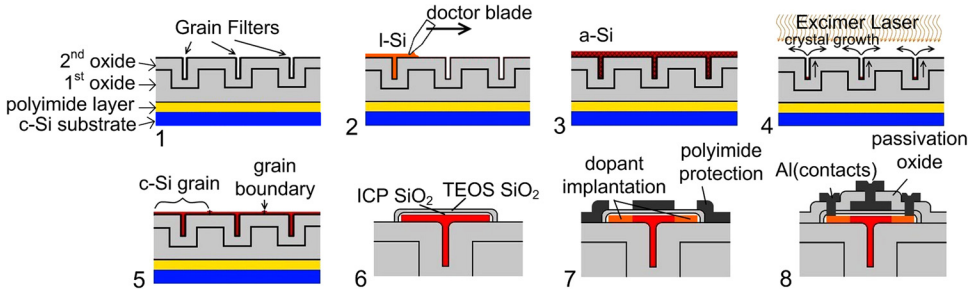

FIG. 1. Schematic of SG-TFT fabrication process with liquid-Si on polyimide substrate.

from 13 at. % to 10 at. %, while at the surface, the concentration decreases to 3 at. % (see supplemental material[8]). After the dehydrogenation, the a-Si film is crystallized by the excimer-laser at room temperature with an energy density of 950 mJ/cm^2. Si grains are created on predetermined positions of the grain-filters with a maximum grain size of 3 μm, as can be seen in Fig. 2.

TFTs are fabricated inside the grain with a process similar to as described in Ref. 6. After forming Si islands by patterning the Si film, 40 nm gate SiO_2 is formed by inductively coupled plasma (ICP) oxidation at 250 °C and additional SiO_2 deposited by PECVD-TEOS at 350 °C. The SEM image of the silicon islands shows the channel covered by a single grain (see supplemental material[8]). After that the Al gate is deposited and source and drain regions are ion-implanted with boron and phosphorus using self-alignment by the gate. The impurities are activated by the excimer-laser. To prevent thermal damage to the polyimide substrate from the laser, an Al layer covers the area outside the gate, source, and drain. Passivation SiO_2 deposition at 350 °C by PECVD TEOS and contact hole and Al pad formations complete the TFT fabrication. Both channel length and width are 1 μm. Finally, the polyimide substrate is etched away using oxygen plasma. The TFTs can now be peeled off from the crystalline Si wafer by an acrylic-based dicing tape and transferred to a 125 μm thick flexible PEN foil using a glue made of polymers, as shown in Fig. 3. The transfer process is not necessary and the TFTs could be directly fabricated on the polyimide foil as the maximum process temperature was below 350 °C. We have introduced the transfer process just because of the ease of handling and processing in our lab if the crystalline-Si substrate was employed as a carrier.

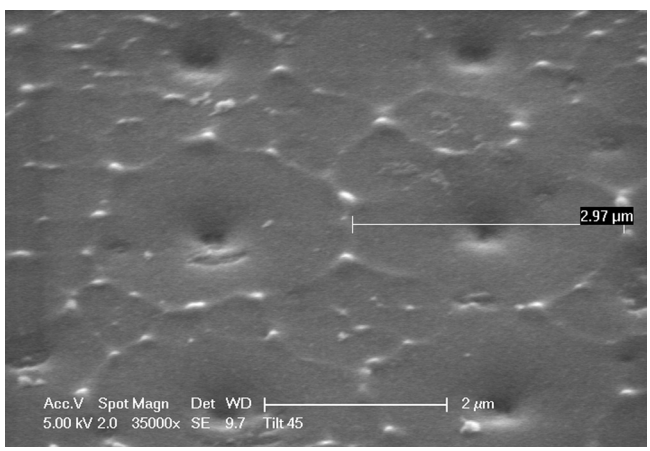

FIG. 2. SEM image of the crystallized grains at predetermined positions with a maximum diameter of 3 μm.

Figs. 4–6 show the transfer and output characteristics of the NMOS and PMOS TFTs. The carrier mobility estimated in the linear region with a low drain voltage is 460 cm^2/V s and 121 cm^2/V s for electrons and holes, respectively. Table I summarizes the device characteristic values. The mobilities are much higher than those of the organic (0.5 cm^2/V s, Ref. 1) and metal oxide (~10 cm^2/V s, Ref. 9) TFTs on a plastic substrate. The values are higher than poly-Si TFTs (50 cm^2/V s, Ref. 10) as well because of the absence of the random grain-boundaries inside the channel. The leakage current is below 0.1 pA/μm, which is lower than that of the poly-Si TFTs and suitable for display application.[11] Fig. 7 shows the output characteristic of the CMOS inverter, with a full output swing (4.997 V out of 5.000 V) and with V_{TH} of 2.14 V. Table II presents the summary of the inverter characteristics.

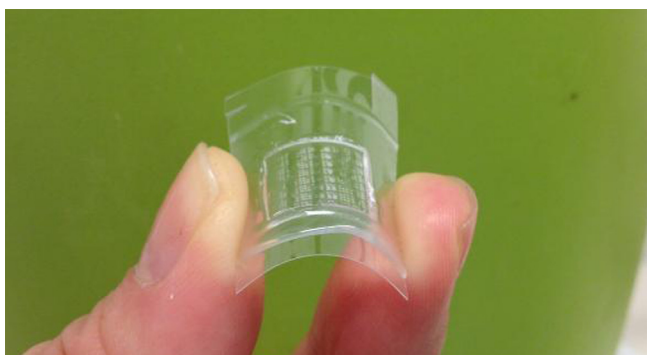

FIG. 3. Image of SG-TFTs on polyimide layer (1 × 1 cm^2) peeled off and transferred to a PEN foil.

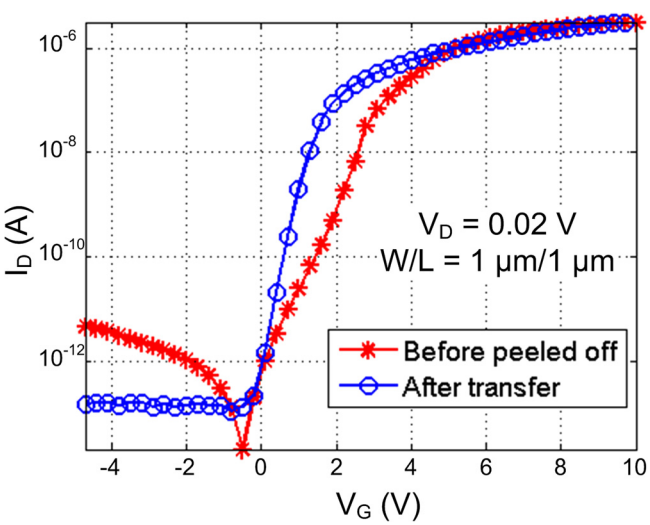

FIG. 4. Transfer characteristics of NMOS TFTs before the peeling-off and after the transfer.

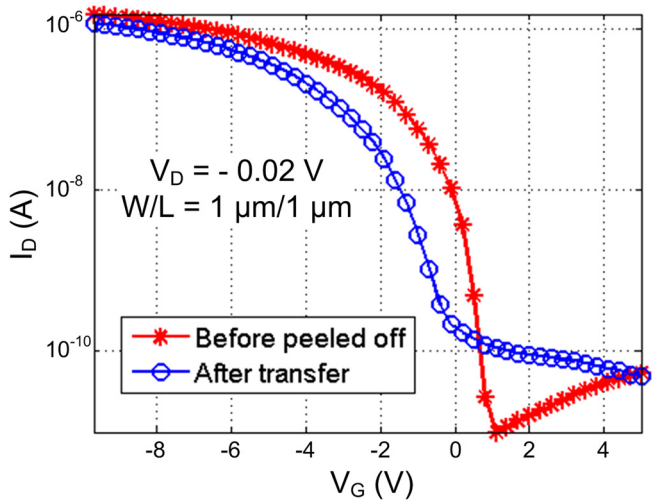

FIG. 5. Transfer characteristics of PMOS TFTs before the peeling-off and after the transfer.

After being peeled off with dicing tape and transferred to the flexible foil, the circuit still shows functioning transfer characteristics of NMOS and PMOS TFTs, as shown in Figs. 4 and 5. The NMOS TFTs before and after being peeled off are measured on the same transistor, which also applies for PMOS TFTs and inverters. The estimated carrier mobility is 310 cm^2/V s and 110 cm^2/V s for electrons and holes, respectively, which is lower than before they were peeled off. The leakage current of NMOS transistors at high negative gate voltage decreases comparing to that before peeled off. The reason of the reduced carrier mobility is assumed to be the

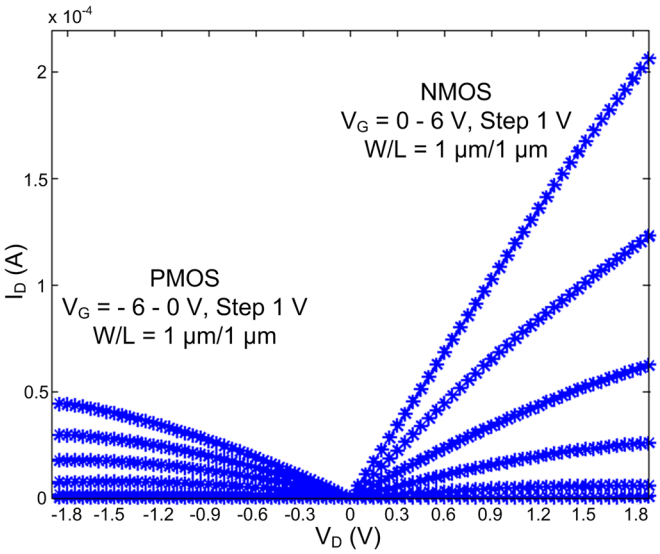

FIG. 6. Output characteristics of NMOS (a) and PMOS (b) TFTs before the peeling-off.

TABLE I. Summary of NMOS TFT and PMOS TFT characteristics.

TFT	NMOS	NMOS after peeling	PMOS	PMOS after peeling
μ_{FE} (cm^2/V s)	460	310	121	110
V_{TH} (V)	3.62	2.55	−0.94	−2.02
I_{ON}/I_{OFF}	7×10^5	2×10^7	3×10^4	2.5×10^4
S (V/dec)	0.3	0.26	0.24	0.67

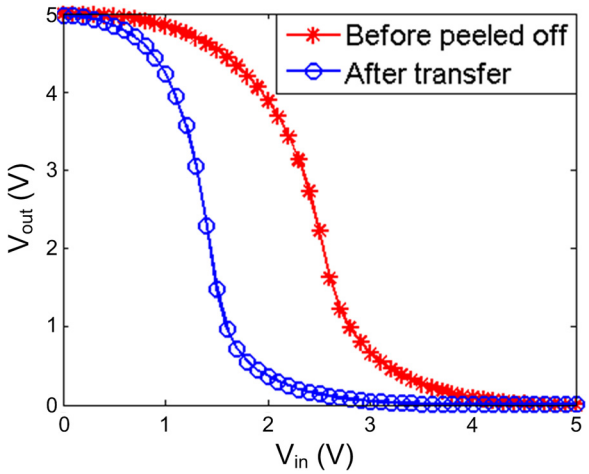

FIG. 7. Output characteristic of CMOS inverter with the ratio of 2 of W/L between PMOS and NMOS TFTs (red) before peeled off and (blue) after transfer.

TABLE II. Summary of the CMOS inverter characteristics.

Inverter	Before peeling	After peeling
V_{TH} (V)	2.14	1.50
V_{OH} (V)	4.9972	4.9805
V_{OL} (V)	0.0096	0.0006
NM_H (V)	2.3275	3.04
NM_L (V)	1.3968	0.76

mechanical stress caused by the transfer process and/or stress during the measurement since the substrate is not rigid. The leakage current at Vg = −5 V becomes lower than 1 pA/μm. Fig. 7 shows the output curve of the CMOS inverter on the flexible foil, with a V_{TH} of 1.50 V, a full output swing (4.981 V out of 5.000 V), and less-balanced noise margin compared to before being peeled off, since the threshold voltage of both NMOS and PMOS TFTs shifted to more negative values.

Amorphous Si was formed by doctor-blade coating and annealing of liquid-Si on a polyimide-coated substrate. With subsequent crystallization by excimer-laser, grains with a maximum diameter of 3 μm were obtained. Single-grain Si TFTs fabricated inside the grain showed mobilities of 460 cm^2/V s and 121 cm^2/V s for electrons and holes, respectively. The devices were peeled off and transferred to a flexible PEN foil, with carrier mobilities of 310 cm^2/V s and 110 cm^2/V s, for electrons and holes, respectively. CMOS inverters were also fabricated and showed full output swing.

These results suggest that the approach presented in this paper can open a new route for achieving high-performance and flexible Si thin-film electronic devices on plastic with printing method compatible with a roll-to-roll process.

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[8]See supplementary material at http://dx.doi.org/10.1063/1.4811356 for experimental data, Fig. S1 (cross-sectional SEM image of a grain-filter, completely filled with a-Si), Fig. S2 (Raman spectroscopy of the a-Si film formed with the liquid-Si at 350 °C), Fig. S3 (hydrogen concentration measured with ERD for the a-Si film before and after laser annealing at 500 mJ/cm^2), and Fig. S4 (SEM image of patterned silicon islands).
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