Master Thesis project 2014-2015

Integrating a Temperature Sensor into a CMOS Image Sensor.

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Contents

Chapter 1

Introduction

Application The majority of mobile devices that can capture images nowadays, are based on CMOS technology. CMOS technology is low cost and is highly integratable in devices like mobile phones, tablets and laptops. These mobile devices have the image sensor as an extra functionality and a mechanical shutter is lacking. Dark current noise is one of the main contributors of noise in the images of these devices.

Next to process dependencies, temperature plays a big role in the amount of dark current noise that an image pixel is generating. Self-heating of the surrounding circuitry contributes locally to a temperature difference. With a mechanical shutter, dark frame subtraction is possible to easily compensate for the dark current signal. This is what is being done in photo camera's with a shutter and is still the main technique to compensate for dark current noise, in the digital image of these devices afterwards.

If it would be possible to measure the temperature gradient of the pixel array of an image sensor, it would be possible to compensate for dark current noise. To see effectiveness of dark current noise compensation caused by temperature difference in the image sensor, a test sensor has been designed. The design and implementation of this sensor are described in this thesis.

Challenges The problem in sensing temperature at pixel level, lies in the fact that a light sensing part is being replaced and therefore image quality is being sacrificed. To reduce the area of the temperature sensing part, a form of 'long range' sensing can be opted as is being done in microprocessors, where the most valuable area of the chip is the most important to monitor [1].

It would be of much interest if the temperature signal readout can be done with the circuitry of the image device. For this reason there has been chosen to use the widely used 4 transistor active pixel sensor (4T APS) as pixel of choice and the corresponding column readout circuit. The pixel and readout of our test device are both taken form a different design, in which many different pixel designs and readouts have been implemented for testing, as part of the 'Ultra-Low Noise CMOS Imager Sensor for Single Photon Detection' (U-LONO) project.

Literature about temperature sensing at pixel level cannot be found. And there is no work that can be used to build upon concerning this topic. For that reason a portion of this thesis is spent on the design options and the choice of temperature sensing device.

Technology The technology used is from TowerJazz. TowerJazz is a company that has a lot of experience in CMOS image sensor (CIS) technology, with the emphasis on low dark current. The technology used in this design is TowerJazz 0.18μm CIS Technology.

Organization of chapters The pixel and column readout that are being used in the design of this thesis are presented in chapter 2. The temperature sensor is integrated in an existing pixel array, therefore the schematics and layout of the pixel design are shown. Also the schematic and the main functionality of the column readout circuit are being discussed.

To give the reader a better idea of dark current noise, in chapter 3 in short is explained what the effects are and an example is given.

No literature can be found of temperature sensing inside image devices with the purpose of dark current noise compensation, therefore some research has been done in selecting the best temperature sensing device based on some specifications, as can be read in chapter 4. The device selected is the parasitic pnp BJT, that is widely available in CMOS processes.

In chapter 5, in detail is explained how a pnp BJT can be used to sense temperature via the measurement of a base-emitter voltage. The process and temperature dependencies of the BJT are described. And there is explained how a difference in two base-emitter voltages can be used to counter these. As the difference between two base-emitter voltages will be the main method used to derive the temperature, also the non-idealities of a base-emitter measurement are described.

The design consideration that have been made, based on the pnp BJT as temperature sensing device, are explained in chapter 6. In this chapter is explained why the design of the readout circuit of the image sensor has not been altered and which techniques have been used to improve temperature measurement.

The implementation of the temperature sensor, bias current sources, pixel array, readout circuit and full chip can be found in chapter 7. In this chapter in detail images of the layouts and schematics with device sizes of all designed components are shown.

At the end of this thesis a conclusion and recommendations are given. In chapter 8 can be read whether the implementation of a temperature sensor inside a pixel array has been successful. Also is told what could have been done better, and advice is given on the integration of temperature sensors in pixel arrays of image devices in the future.

As the chip still is waiting for tape-out at the moment of writing, no measurement results can be presented in this thesis.

Chapter 2

Image sensor

The image sensor that is being used in this thesis, is based on a familiar design of the four transistor active pixel sensor (4T APS) with pinned photodiode (PPD). It has been designed by X. Ge and is part of the Ultra Low Noise (U-LONO) project. In the design many different kind of pixels and readouts have been implemented for testing. One of the pixel designs has been copied and is being used in the design of this thesis in a 192x64 test array. On top of that also one of the column readout designs and digital signal generation blocks have been copied.

There are two main reasons to copy these designs, the first is that the readout circuitry has been manufactured and has proven to work. The second is the lack of time during this thesis project to integrate a temperature sensor in Ge's design and also re-design the complete readout and digital signal generation blocks. In chapter 6 will be discussed what kind of implications this has for the chosen design for temperature sensing.

In Figure 2.1 a top level layout overview of the design of Ge can be seen. In this overview, from left to right, three area's can be distinguished: capacitive readout, pMOS source follower readout and NMOS source follower readout. Within these areas different pixel designs have been implemented for testing purposes. The areas indicated in red squares represent the layouts that are being used in the design in this thesis: row signal decoder and generator (1), part of the NMOS pixel array (2), column readout and amplification (3), output buffer stage (4).

An overview of how these parts will work together to form the image sensor, can be seen in Figure 2.2. Here can be seen that a row decoder generates three control signals for every row of pixels: RS for Row Select, RST for Reset and TG for Transfer Gate. Inside the pixel a video signal V_{signal} and a noise signal n_{reset} is generated. In two phases these signals are transferred to the column amplifier, that subtracts the two signals in the analog domain and amplifies the outcome. Then the signal is transferred to a general output buffer, that amplifies the signal again before it goes off-chip to an ADC. In this test set-up a 16-bit ADC will be used.

2.1 4T pixel

The main challenge in integrating a temperature sensor into an existing image array lies in the fact that the same interconnect lines for control and bias signals have to be used. There is hardly any room to fit any extra interconnects. If a full design of both image sensor and temperature is being done at the same time, before hand can be thought of clever interconnect routing throughout the array for both sensors. Some signals are able to be used for both signals, others need a dedicated signal line as can be read in chapter 7.

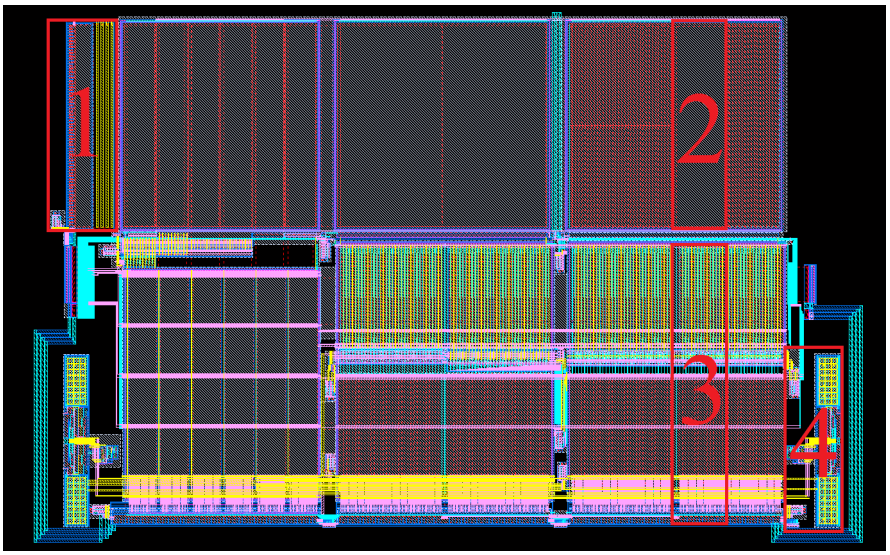

Figure 2.1: Top level layout overview of Ge's design. Indicated areas: row signal decoder and generator (1), part of the NMOS pixel array (2), column readout and amplification (3), output buffer stage (4).

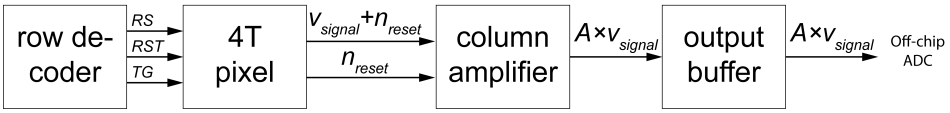

Figure 2.2: Overview of the stages the column.

2.1.1 Schematic

In Figure 2.3 the schematic of the pixel design of Ge can be seen that is also being used in this thesis. The pixel consists of a photodiode, a transistor as transfer gate (TG), a transistor (RST) to reset the floating diffusing, a transistor as driver of the NMOS source follower and a transistor (RS) to switch the pixel to the column bus. The current source that is needed for the NMOS source follower to work can be disconnected from the column bus for testing purposes.

2.1.2 Layout

In Figure 2.4 the layout of the pixel design of Ge can be seen that is also being used in this thesis. The photodiode can be recognized by the red layer. The 4T structure together with the substrate ground are located to the bottom right of the photodiode.

One interconnect wire, that is needed to switch the current source on/off in the temperature sensor, has been added to this layout and can be seen in Figure 2.5. In the temperature sensor the same wire layout has been used as in the image pixel.

2.2 Column readout with CDS

In the design of this thesis the same column amplifier from Ge's design will be used. The full overview of the components in the column can be seen in Figure 2.6. Here can be seen that the column circuitry consists of a programmable gain amplifier with correlated double sampling (CDS), a sample and hold

(S/H) circuit and an output buffer. Mainly the the programmable gain amplifier with CDS will of interest in the design, therefore the schematic can be seen in Figure 2.7 and its functioning will be explained as well.

The amplification ranges from 1x to 16x. A reference voltage (V_{ref}) is being used to keep the amplifier in the preferred operating range and can be adjusted off-chip. The sampling of the signals happens in two phases, determined by the position of switch ϕ_s:

Phase 1: Switch ϕ_s is closed and the difference between input signal and reference voltage is sampled on capacitor C_1. In this phase a sample V_{in_1} is taken.

Phase 2: Switch ϕ_s is open and a new input signal V_{in_2} is applied. The difference between the sampled voltage on capacitor C_1 and a new input signal V_{in_2} makes that charge is put on capacitor C_2.

This charge will be multiplied by a capacitor ratio of $\frac{C_1}{C_2}$ and can be adjusted by a programmable capacitor bank. By shorting the input to ground in phase 2, it is possible to do a normal measurement of the input voltage V_{in}.

The schematic and specifications of the amplifier can be found in Appendix A.

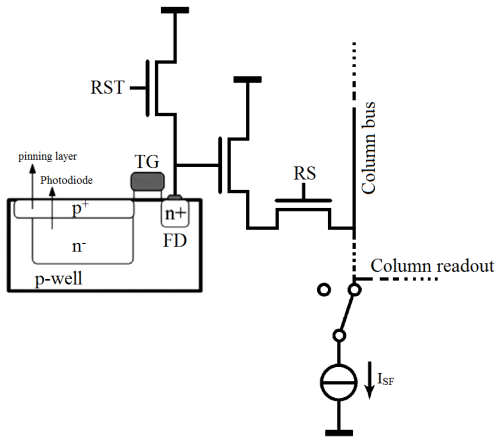

Figure 2.3: Schematic of the 4T pixel with NMOS source follower.

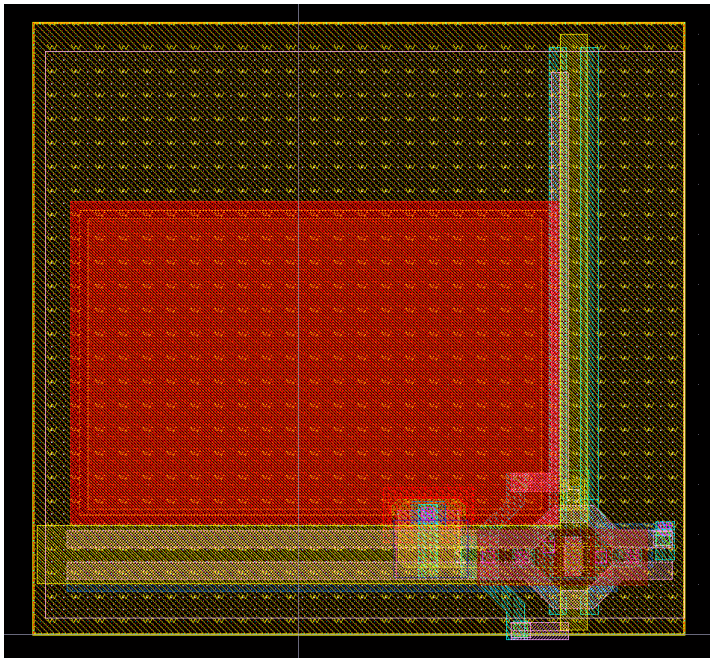

Figure 2.4: Layout of the 4T pixel with NMOS source follower.

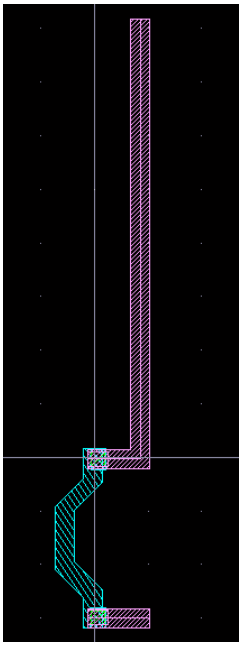

Figure 2.5: Added metal layer to the 4T pixel.

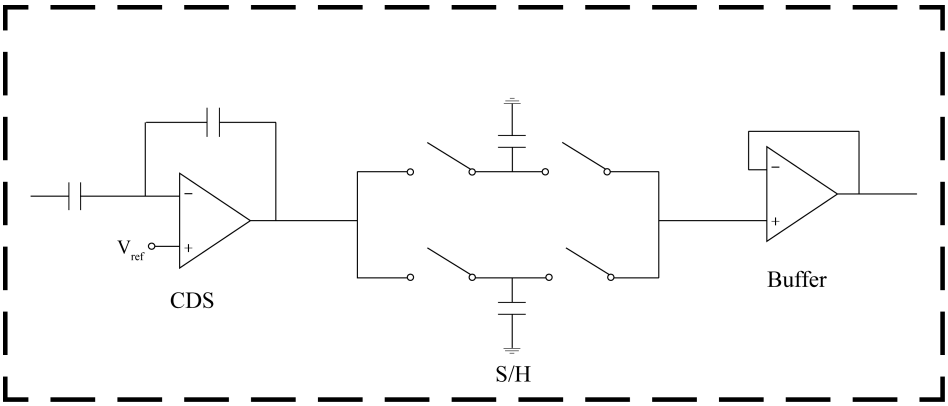

Figure 2.6: Schematic overview of the stages in the column amplifier.

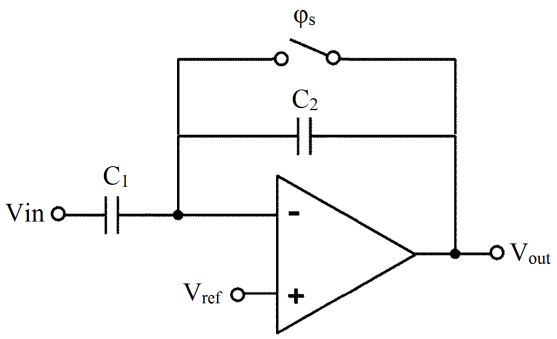

Figure 2.7: Schematic of the amplifier used in the column.

Chapter 3

Dark current noise

Dark current noise is caused by crystalline defects and mechanical stress in a photosensitive device. By random generation of holes and electrons, charge in the photodiode is accumulating that is not caused by photocarriers. This introduces a signal, even when no light is exposed to the image sensor.

Dark current noise has a spatially varying part and a temporal varying part. The spatially varying part contributes to the fixed pattern noise, while the temporal part is caused by dark current shot noise [2]. The spatially varying part is random and mostly caused by process variation, while the temporal part is random.

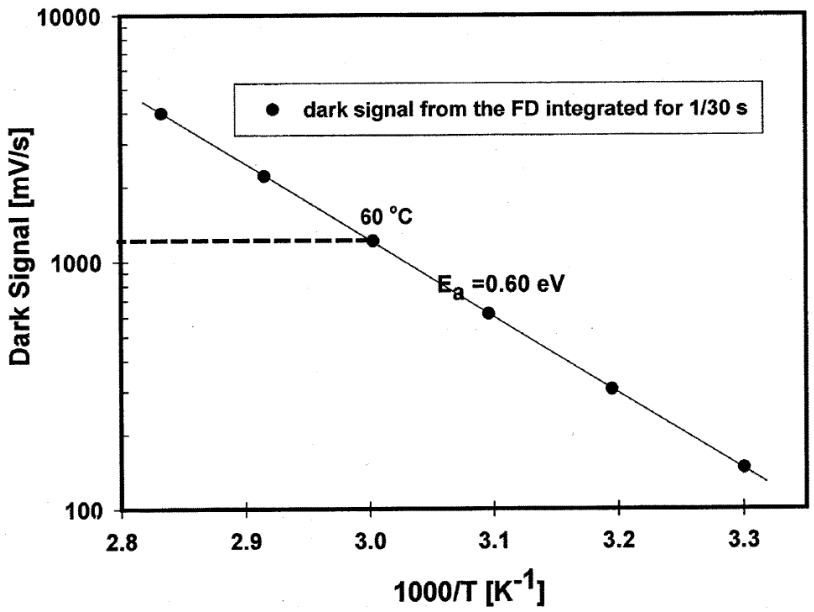

Figure 3.1: An example of the temperature dependence of dark current noise [2].

Dark current is temperature dependent as can be seen in Figure 3.1. At lower temperatures the recombination-generation mechanism is dominant, at higher temperatures the diffusion mechanism is dominant [2]. This is due to different activation energies for both components at different temperatures.

Generation rate of dark current, k_{gen}, is given as

$$k_{gen} = A \cdot exp(-\frac{E_a}{kT}) \tag{3.1}$$

where E_a, the activation energy, k, Boltzmann's constant, T, the temperature in Kelvin, and A, a photodiode specific coefficient [3]. From Equation 3 can be seen that next to process parameters, temperature has a great influence on dark current generation. For example, the percentage change in generation rate can be found as

$$\frac{\delta k_{gen}}{\delta T} / k_{gen} = \frac{E_a}{kT^2}, \tag{3.2}$$

which gives approximately an 8% change in generation of dark current per degree Kelvin, at T=300, with an activation energy of $E_a = 0.60$eV.

Especially a temperature gradient across the surface of an image sensor will cause dark current noise that is non-uniform and will be visible in the image. These temperature differences are mainly caused by surrounding circuits. An example of a dark image that shows dark current noise can be seen in Figure 3.2. In the middle of this image the noise is uniformly distributed and looks random, but on the top and bottom the noise levels are higher. This is mainly caused by circuits that deliver control signals, the column readout and the ADC. In the bottom left the hot spot of the ADC is clearly visible. This just an example of a tempeture gradient and not per se the temperature difference that is going to be measured with this test sensor.

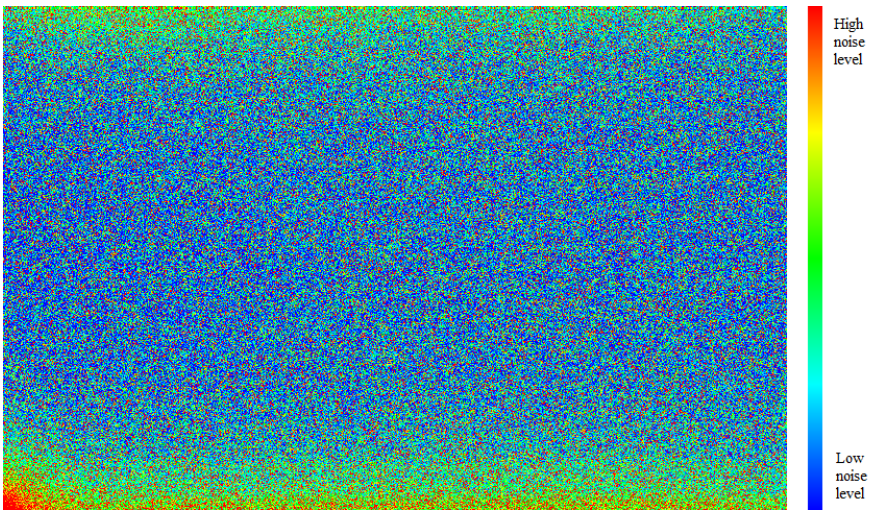

Figure 3.2: An example of a dark image that shows dark current noise. Color gradient bar on the right to show intensity difference.

Chapter 4

Specifications and device choice

To integrate a temperature sensor in the design of the image sensor, first of all it has to be CMOS-compatible. Different devices can be distinguished that are CMOS-compatible for temperature sensing: The BJT, the MOSFET, the diode and the thermistor. On top of that thermal diffusivity can be used as well, since the substrate used for IC fabrication is highly pure [4].

4.1 Specifications

A list of specifications can be made which the temperature sensor has to apply to. First of all, if the influence of temperature on dark current is going to be measured, the sen sor has to be close to the image pixel inside the array. Replacing an image pixel by a temperature sensor reduces the quality of the image taken. So the size of the temperature sensor directly influences the image quality and the temperature sensor should be as small as possible.

Second of all, to see whether or not a temperature sensor can be integrated into a pixel array, it is of interest that the same readout circuity is being used for the temperature signal, as well as for the video signal.

Third of all, the temperature measuring technique should be accurate enough on the specified range of -40 to 100°C. This is the same range on which the image sensor is specified to work.

Fourth of all, the accuracy of the temperature measuring device doesn't have to be very accurate. A couple of degrees difference in temperature at room temperature, already has great influence on dark current generation. After calibration, an 3σ inaccuracy of 5 degrees in the specified temperature range is specified.

Fifth of all, the measurement time should be fast enough to be used within the cycle used for the read out of the image sensor. A temperature sample should be available within the settling time of the column amplifier of 150ns.

Sixth of all, the temperature sensor should not be light sensitive. Because the temperature sensor is in between the image pixels, there will be no light shielding from the package in that area. Therefore some other kind of shielding, at chip level, should be implemented to counter the influence of light on the sensor.

To summaries the specs, above stated:

1. Reduce the size of the temperature sensor as much as possible to minimize image quality loss.

2. Use the same readout circuitry for both image and temperature signals.

3. The temperature sensing technique should measure on the range of -40 to 100°C.
4. The temperature sensing technique should have a maximum 3σ inaccuracy of 5 degrees.
5. The temperature sensing technique should have a sub 150ns sampling time.
6. The temperature sensor should be made insensitive to light.

4.2 Choice of device

The devices mentioned above, have different temperature and process dependencies. And different devices require different kinds of trimming or calibration to cope with these [4]. To make a comparison, all devices will be compared to each other with regard to the specifications.

To start of, the accuracy that can be obtained with the different devices as temperature sensor are similar in comparison and can be well below spec 4 [5]. Also the shielding can and should be implemented at chip level. Therefore specification 6, that states that the temperature sensor is light insensitive, is regardless of device choice.

4.2.1 Thermistor

In [6] a very small thermistor can be found. The space occupied by the temperature sensing part of a thermistor, namely the resistor, is 0.35x0.125 mm^2. This is too large to integrate in the pixel array without degrading image quality too much (spec 1 cannot be met).

4.2.2 Thermal diffusivity

In [5] is shown that temperature sensors based on thermal diffusivity in general take a long time (>1sec) to measure temperature. The fastest measurement done with this technique is reported in [7]. Then again, a trade-off can be made between measurement time and accuracy. But the space occupied by the temperature sensor in that report is $135x60\mu m^2$, which is too large to integrate in the pixel array without degrading image quality too much (spec 1 cannot be met).

4.2.3 Diode

In [8] the use of a diode as temperature sensing part is reported. The readout speed and area occupied are promising, but the architecture, with comparator and TDC used for this sensor, is not compatible with the readout circuitry of the image sensor (spec 2 is not met).

4.2.4 MOSFET or BJT

Both MOSFET and BJT, as devices for temperature sensing, can be used in conjunction with the readout architecture of the image sensor. For both MOSFET and BJT based designs, the temperature sensing part doesn't have to occupy a lot of area and can measure fast and accurately, based on bandgap-voltage reference.

For example in [9], a temperature sensing part as small as two MOSFETs and three resistors is reported. Which would benefit the specification of size. And for example in [10] and [11], BJT designs are reported with a 3σ inaccuracy of $\pm$ 0.3°C, with a measurement time as fast as 5.0ms

and 2.2ms, respectively. Which would benefit specification 5. Also faster measurement times can be found, but these come at the cost of a reduced accuracy of a couple of degrees.

Overall it can be found, that temperature sensors designed with MOSFETs show much less accuracy and long-term stability than BJTs, due to mismatching of components, drift, temperature effects, $1/f$ noise, and mechanical stress [12]. Temperature sensors, based on a BJT as temperature sensing part, have shown that they can be used in a variety of designs and accurate temperature measurements can be achieved [5]. Since the parasitic BJT is available in TowerJazz 0.18μm CIS technology, this is the device of choice.

Chapter 5

The vertical pnp BJT

In many CMOS processes a so called parasitic bipolar junction transistor (BJT) is available. These kind of BJTs have a relative large base width, which results in a lower common-emitter current-gain β_F. Because these parasitic BJTs are mostly used in CMOS designs as temperature reference and/or temperature independent voltage reference, the current-gain doesn't need to be high but needs to be constant with temperature and current variation.

In BJTs the collector current is, among other factors, dependent on temperature and is described by the well-known relation:

$$I_C = I_S exp(\frac{qV_{BE}}{kT}), \tag{5.1}$$

where T, the absolute temperature, V_{BE}, the base-emitter voltage, q, the electron charge, k, the Boltzmann constant, and I_S, the saturation current. Unfortunately the saturation current I_S and the base-emitter voltage V_{BE} are strongly dependent on process and temperature.

5.1 Process dependency

To see the influence of process variations, the saturation current I_S from Equation 5.1 can be written as:

$$I_S = \frac{q^2 n_i^2 A_E \tilde{D}_B}{Q_B} \tag{5.2}$$

where A_E, the emitter-junction area, n_i, the intrinsic carrier concentration in the base, $\tilde{D}_B$, the effective minority-carrier diffusion constant in the base, and Q_B, the charge represented by the net number of doping atoms in the neutral base per unit area [13, p.3]. Variations in the parameters of Equation 5.2 are mainly caused by:

- Variation in the doping profile,
- Variations in the transistor geometry,
- Variations in mechanical stress,
- Variation in leakage current.

5.2 Temperature dependency

To see the influence of temperature variations on parameters from Equation 5.2, these parameters can be written as:

$$n_i^2 = T^3 exp(\frac{-qV_g}{kT}), \tag{5.3}$$

$$\tilde{D}_B = \bar{\mu}_B(\frac{kT}{q}), \tag{5.4}$$

where $\bar{\mu}_B$, the effective value of the mobility of electrons in the base, and V_g, the bandgap voltage of the base material [13, p. 4].

The temperature dependence of the base charge due to variations in the boundaries of the base are negligible. The mobility $\bar{\mu_B}$ and bandgap voltage V_g depend highly on temperature in a nonlinear way:

$$\bar{\mu}_B \propto T^{-n} \tag{5.5}$$

$$V_g = V_{g0} - \alpha T \tag{5.6}$$

where n and α are constants and V_{g0} is the extrapolated bandgap voltage at 0 K. In this way the saturation current I_S becomes

$$I_S = CT^{\eta} exp(-\frac{qV_{g0}}{kT}), \tag{5.7}$$

where C is a process dependent constant, and $\eta = 4 - n$, a process dependent temperature coefficient. To see the influence of temperature variations on the collector current together with the saturation current, Equation 5.1 can be written as [13, p. 4]:

$$I_C = CT^{\eta} exp(\frac{q(V_{BE} - V_{g0}}{kT}) \tag{5.8}$$

5.3 Delta V_{BE}

By measuring the difference of two V_{BE} voltages, many process and temperature dependencies can be eliminated. The difference in V_{BE} voltage can be achieved by using one or two BJTs either with different emitter area sizes of by biasing them with different collector currents. If Equation 5.1 is rewritten and the difference in V_{BE} voltage between two BJTs (with subscript 1 and 2) is taken, this will result in:

$$V_{BE1} - V_{BE2} = \Delta V_{BE} = \frac{kT}{q}\left[ln\left(\frac{I_{C1}}{I_{S1}}\right) - ln\left(\frac{I_{C2}}{I_{S2}}\right)\right] = ln\left(\frac{I_{C1}I_{S2}}{I_{S1}I_{C2}}\right) \tag{5.9}$$

By using two BJTs from the same process and measuring a ΔV_{BE} voltage at one temperature, the process dependencies of I_S will almost be equal for both V_{BE} voltages and in Equation 5.9 these cancel against each other. In this way a ratio between the two collector current densities is left, based on either emitter area size ratio $r = \frac{A_{E1}}{A_{E2}}$, or based on bias collector current ratio $p = \frac{I_{C1}}{I_{C2}}$. This also holds for a single BJT, but obviously then only a collector current ratio can be applied.

In this way ΔV_{BE} becomes proportional to absolute temperature (PTAT) and temperature can be accurately derived from ΔV_{BE} measurement:

$$\Delta V_{BE} = \frac{kT}{q} ln(pr) \longrightarrow T = \frac{q}{k}\frac{\Delta V_{BE}}{ln(pr)} \tag{5.10}$$

Although the difference in V_{BE} voltage is an accurate measure for temperature, the difference (for ratio's of $3 < pr < 16$) in voltage per degree Kelvin is small (0.1 - 0.25mV/K) and the signal needs to be adequately amplified [14, p. 4].

5.4 Non-idealities of Delta V_{BE} measurement

5.4.1 Current-gain variation

Retaining an accurate current-gain factor $\beta_F = I_C/I_B$, is essential to allow ΔV_{BE} voltage measurement based on current ratio's to be effective. The current gain-factor needs to stay constant with different bias currents. A difference in current-gain factor between two collector currents $I_{C1,2}$ will result in a difference in ΔV_{BE} [15] as:

$$\Delta V_{BE} = \frac{kT}{q} ln\left[\frac{I_{E2}}{I_{E1}} \frac{\beta_{F2}(\beta_{F1}+1)}{(\beta_{F2}+1)\beta_{F1}}\right]. \tag{5.11}$$

It is shown that the current-gain factor of a parasitic pnp BJT stays relatively constant (less than 1% decrease for a $1 < p <$10 ratio), if the unity bias current is chosen well [15]. In this case the remaining error is almost independent of temperature and can be treated as a systematic offset. The exponential decrease above $p < 10$ ratio's is due to high-level current injection, as will be discussed in 5.4.3.

If is looked at Figure 5.1, a graph with arbitrary units (which cannot be disclosed) from a Tower-Jazz characterization report, it can be seen that for a certain collector current range and temperatures upto 100°C, the beta stays almost constant [16]. Unfortunately this characterization only goes as low as 25°C. Test BJTs have been implemented on-chip, to measure variation in the current-gain factor for the test chip, and to also determine how the beta fluctuates in the range of -40 to 25°C.

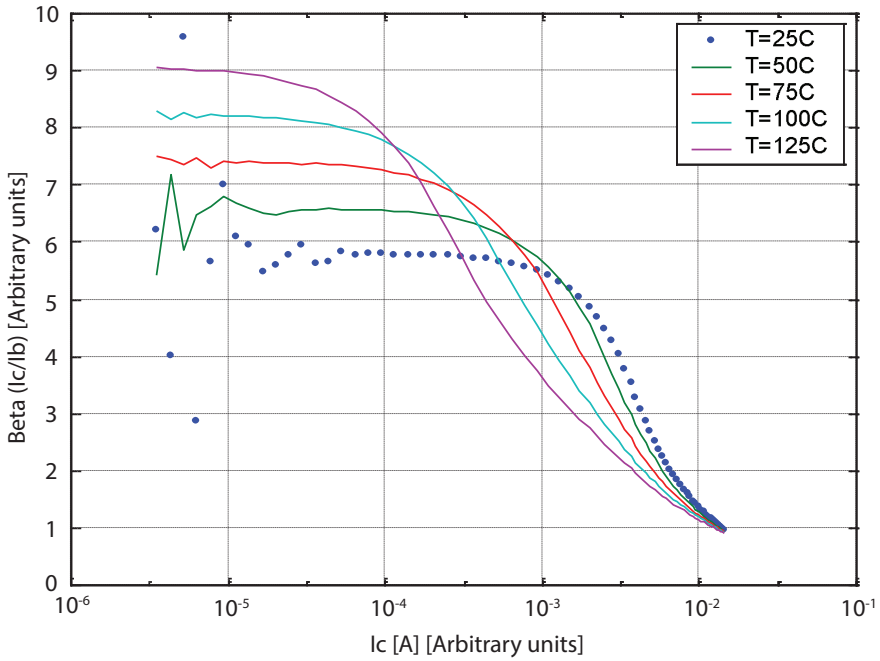

Figure 5.1: The beta versus collector current of a 5x5μm vertical pnp BJT in TowerJazz 0.18 CIS technology, for various temperatures.

5.4.2 Series resistance

Because the voltage difference per degree Kelvin in ΔV_{BE} is small, the voltage drop by wire resistance can cause inaccuracies. The resistance in the base (r_b) and emitter (r_e) all contribute to a voltage drop in the measurement of the base-emitter voltage. According to [17], in a ΔV_{BE} measurement this results in:

$$\Delta V_{BE} = \frac{kT}{q} ln\Big(\frac{I_{C1}}{I_{C2}}\Big) + (I_{b2} - I_{b1})r_b + (I_{E2} - I_{E1})r_e. \tag{5.12}$$

With the relation for the gain factor ($I_B = \frac{I_e}{\beta_F + 1}$) this becomes:

$$\Delta V_{BE} = \frac{kT}{q} ln\Big(\frac{I_{C1}}{I_{C2}}\Big) + \Big(\frac{I_{E2}}{\beta_{F1} + 1} - \frac{I_{E1}}{\beta_{F2} + 1}\Big)r_b + (I_{E2} - I_{E1})r_e. \tag{5.13}$$

Research in [15] shows that the current gain of a parasitic pnp BJT stays almost constant with the same temperature for a range of several orders of emitter current. So we can expect the current gain factors of two bias currents to be similar for a ΔV_{BE} measurement done at the same temperature.

If we take $\beta_{F1} = \beta_{F2} = \beta_F$ and a series resistance relation $r_s = (\frac{1}{\beta_F + 1})r_b + r_e$, this allows for a cancellation of the series resistance by introducing a second ΔV_{BE} measurement [15]:

$$\Delta V_{BE1,2} = \frac{kT}{q} ln\Big(\frac{I_{C1}}{I_{C2}}\Big) + (I_{E2} - I_{E1})r_s, \tag{5.14}$$

$$\Delta V_{BE1,3} = \frac{kT}{q} ln\Big(\frac{I_{C1}}{I_{C3}}\Big) + (I_{E3} - I_{E1})r_s. \tag{5.15}$$

By knowing the accurate values of bias currents $I_{E1,2,3}$, these equations can be solved for T and r_s.

In a design where these values are not accurately known, but only accurate ratio's between the bias currents $I_{E1,2,3}$ are known, as $I_{E2} = aI_{E1}$ and $I_{E3} = bI_{E1}$, temperature can be calculated, according to [17], as:

$$T = \frac{q}{k} \frac{(\Delta V_{BE1,3})(a-1) - (\Delta V_{BE1,2})(b-1)}{ln(b)(a-1) - ln(a)(b-1)}. \tag{5.16}$$

5.4.3 High-level current injection

When the concentration of minority carriers in the base becomes significant compared to the majority-carrier concentration, there is an onset of high-level current injection. In this region the slope of $V_{BE} = \frac{kT}{q} ln(\frac{I_C}{I_S})$ changes gradually to $V_{BE} = \frac{2kT}{q} ln(\frac{I_C}{I_S})$ and it cannot be used anymore as a PTAT measure [15].

Bias currents should be chosen below this level for the temperature sensor to work more accurately. The onset of high-level injection goes together with the drop in current-gain factor β_F. With the implementation of test BJTs on-chip, it should be possible to measure this drop in gain, to determine how large the maximum bias current should be.

5.4.4 Early Effects

The forward Early Effect and the reverse Early Effect influence the base-collector voltage $V_{B'C'}$ and base-emitter voltage $V_{B'E'}$ respectively. Gummel and Poon [18] model the effect of the forward Early voltage, V_A, and the reverse Early voltage, V_B, on the base-emitter voltage as:

$$V_{B'E'} = \frac{kT}{q} \Big\{ ln\Big(\frac{I_C}{I_S}\Big) + \frac{V_{B'C'}}{V_A} + \frac{V_{B'E'}}{V_B} \Big\}. \tag{5.17}$$

The intrinsic base-collector voltage changes due to the voltage drop across the base resistance r_b and the collector resistance r_c, similar to series resistance,

$$V_{B'C'} = \big(\beta_F r_c - r_b\big) I_B. \tag{5.18}$$

As $kT/q << V_A$, the forward Early Effect is negligible. On top of that the series compensation technique described in 5.4.2 should compensate for this effect [15]. If the forward Early effect is ignored, Equation 5.17 can be rewritten as:

$$V_{B'E'} = \frac{kT/q}{1 - kT/qV_B} ln\Big(\frac{I_C}{I_S}\Big). \tag{5.19}$$

To model this, a factor n, called *effective emission coefficient* or *nonideality factor* is introduced [18],[15],

$$\Delta V_{BE} = \frac{\mathbf{n}kT}{q} ln(p). \tag{5.20}$$

Factor n can be regarded temperature dependent as:

$$n = \frac{1}{1 - kT/qV_b}. \tag{5.21}$$

A big problem with this approach is the unknown value for the reverse Early voltage V_B. This value is not the same as the reverse Early voltage, as can be found in process characterization reports to which it normally refers to, because the transistor in this situation is not operating in its reverse active region, since the base-emitter junction is forward biased [19]. For example in [15], the value for V_B was chosen to get a temperature dependent n factor that minimizes the error.

5.5 Voltage reference

In most electronic devices a dedicated on-board voltage reference is already implemented. For no particular reason it might be interesting to use the temperature sensor in the pixel array as a voltage reference. The base emitter voltage of a single BJT is complementary to absolute temperature (CTAT) and can be added to the delta V_{BE} voltage that is PTAT, to create a temperature reference. To allow for good precision different methods for calibration and curvature correction are described in this section.

5.5.1 Calibration for CTAT

There are methods to extract the parameters that model the process dependencies of the collector current of a single BJT. In [20], Meijer et al. propose a method of determining parameters V_{g0} and η of Equation 5.8. From Equation 5.8, with three V_{BE} voltage measurements and three corresponding temperatures, can be derived:

$$T_2 V_{BE}(T_1) - T_1 V_{BE}(T_2) = (T_2 - T_1) V_{g0} + \eta \frac{kT_1T_2}{q} ln\frac{T_2}{T_1}, \tag{5.22}$$

$$T_3 V_{BE}(T_2) - T_2 V_{BE}(T_3) = (T_3 - T_2) V_{g0} + \eta \frac{kT_2T_3}{q} ln\frac{T_3}{T_2}. \tag{5.23}$$

For $T_1 < T_r < T_3$ only one reference temperature ($T_2 = T_r$) has to be accurately known to derive the other two temperatures:

$$T_1 = \frac{\Delta V_{BE}(T_1)}{\Delta V_{BE}(T_r)} T_r \quad \text{and} \quad T_3 = \frac{\Delta V_{BE}(T_3)}{\Delta V_{BE}(T_r)} T_r. \tag{5.24}$$

This allows for a single calibration at room temperature, but puts more weight on the accuracy of the V_{BE} measurements.

5.5.2 Curvature approximation

In [21] is explained how from parameters V_{g0} and η, for $\Delta T/T_2 << 1$, a good second order curvature approximation for a reference voltage can be made:

$$V_{REF} = V_{g0} + (\eta - 1)\frac{kT_2}{q}\left[1 - \frac{1}{2}\left(\frac{\Delta T}{T_2}\right)^2\right] \tag{5.25}$$

Note that in this curvature correction technique the effective emission coefficient n as discussed in 5.4.4 has not been taken into account yet.

5.5.3 Ratiometric curvature correction

In [14, p. 53], Pertijs proposes to use V_{REF} as a ratio to the proportional $V_{PTAT} = \alpha \Delta V_{BE}$ voltage:

$$\mu = \frac{V_{PTAT}}{V_{REF}} = \frac{\alpha \Delta V_{BE}}{V_{BE} + \alpha \Delta V_{BE}} \tag{5.26}$$

Because the V_{BE} voltage is added to the PTAT, the created voltage reference becomes higher order non-linear due to process spread, curvature, series resistances, finite current-gain, etc. This non-linearity is modeled as [14, p. 22-23]

$$V_{BE}(T) = V_{BE0} - \lambda T + c(T) \tag{5.27}$$

where V_{BE0} is the base-emitter voltage at reference temperature T_r, λ is the slope of the tangent,

$$\lambda = \frac{V_{BE0} - V_{BE}(T_r)}{T_r} \tag{5.28}$$

and $c(T)$ the curvature that models the non-linearity,

$$c(T) = \frac{k}{q}\eta\left(T - T_r - T ln\left(\frac{T}{T_r}\right)\right) + \frac{k}{q}\left(T ln\left(\frac{I_C(T)}{I_C(T_r)}\right) - (T - T_r)\frac{T_r}{I_C(T_r)}\left[\frac{\delta I_C}{\delta T}\right]_{T=T_r}\right). \tag{5.29}$$

For the design in this thesis, an external bias current is used, that is independent of temperature. Therefore it holds that $\left[\frac{\delta I_C}{\delta T}\right] \approx 0$ and $ln\left(\frac{I_C(T)}{I_C(T_r)}\right) \approx 0$. So curvature $c(T)$ can be simplified to [14, p. 78]

$$c(T) = \frac{k}{q}\eta\left(T - T_r - T ln\left(\frac{T}{T_r}\right)\right). \tag{5.30}$$

By substituting Equations 5.27 and 5.10 into Equation 5.26, the transfer function is found as

$$\mu = \frac{\frac{kT}{q} ln(pr)}{V_{BE0} - \lambda T + \frac{kT}{q} ln(pr) + c(T)}. \tag{5.31}$$

To improve the linearity of the output of the ADC, another form of ratiometric curvature correction can be applied [14, p. 88-89]. If $V_{REF}(T_r) = V_{BE0}$, there is no temperature coefficient at $T = T_r$ and a second order non-linearity is left. By choosing a higher value for V_{REF}, its temperature coefficient becomes slightly positive, but the non-linearity decreases to third-order, that is much less than before. The condition under which the non-linearity is minimized is

$$\left[\frac{\delta^2 \mu}{\delta T^2}\right]_{T=T_r} = 0, \tag{5.32}$$

and V_{REF} can, in this case, be found as

$$V_{REF}(T_r) = \frac{V_{BE0}}{V_{BE0} - \frac{k\eta}{2q} T_r} V_{BE0}. \tag{5.33}$$

5.5.4 Higher order curvature correction

In [14, p. 90] another example is given, in which, by varying the amplification levels of ΔV_{BE} measurements, different transfers for μ can be found:

$$\mu_1 = \frac{\alpha_1 \Delta V_{BE}}{V_{BE} + \alpha_1 \Delta V_{BE}}, \tag{5.34}$$

$$\mu_2 = \frac{\alpha_2 \Delta V_{BE}}{V_{BE} + \alpha_2 \Delta V_{BE}}. \tag{5.35}$$

The digital output, D_{out}, generated this way then becomes

$$D_{out} = A(\mu_1 - c \cdot \mu_2) + B, \tag{5.36}$$

where A and B are coefficients to scale to degrees Celsius. Parameters α_1,α_2 and c should be chosen in such a way that the curvature in the desired operating range is minimized.

5.6 Summary

The vertical pnp BJT is greatly affected by process and temperature dependencies. To eliminate these dependencies effectively, the difference in base-emitter voltage can be measured. For a single BJT, two base-emitter voltages have to be measured and subtracted from each other to get a delta V_{BE} measurement.

This delta V_{BE} method shows non-idealities which have to be taken into account, like: current-gain variation, series resistance, high-level current injection and Early Effects. The first three non-idealities can be countered respectively, by: choosing a certain bias current range, solving for series resistance with an extra measurement and keeping the bias current low enough.

The forward Early Effect can be neglected and will also be countered by solving for the series resistance. The reverse Early Effect has to be taken into account by measuring the reverse Early voltage and use this value to model the effective emission coefficient.

A delta V_{BE} measurement is proportional to absolute temperature. It is also possible to use the base-emitter voltage of a single vertical pnp BJT as complement to absolute temperature. By adding a CTAT to a PTAT, a voltage reference can be created in this test device. For this to be accurate enough, calibration and curvature approximation will be needed.

Calibration, in which certain process dependent parameters are derived, can be done relatively simple via delta V_{BE} measurements and one known (room) temperature. The derived parameters can then be used for a second order curvature correction or a ratiometric curvature correction. Also with the use of the programmable gain amplifier, different amplification levels can be used to create different transfer functions as digital output for the ADC. With the different outputs and the right choice of parameters the curvature in the desired operating range can then be further reduced.

Chapter 6

Design of the temperature sensor

The kind of BJT mostly used for temperature sensing is the *parasitic* or *vertical* pnp BJT, which is widely available in CMOS processes. With the use of a diode connected bipolar pair with different emitter area ratio's, as showed in Figure 6.1, a difference in base-emitter voltages ΔV_{BE} is created due to the difference in current density that runs through both BJTs. This can also be achieved by biasing the two BJTs with different emitter currents. This can even be done with a single BJT, as shown in Figure 6.2, and measuring two base-emitter voltages separately. The difference in voltage measured is proportional to absolute temperature (PTAT) as explained in section 5.3.

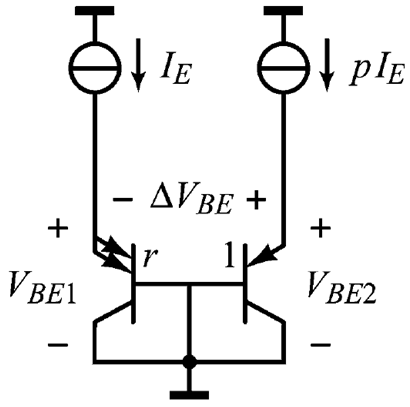

Figure 6.1: Diode connected BJT pair with emitter area size ratio r [15].

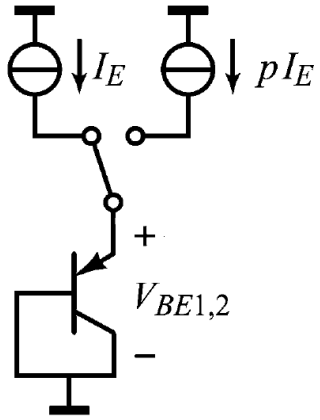

Figure 6.2: Single diode connected BJT with emitter current ratio p [15].

There has been chosen to use the column readout of the imager in conjunction to the BJT as bandgap reference. A schematic overview of temperature sensor (T-sensor) integration with the readout of the imager, can be seen in Figure 6.3. Further in this chapter is the reason explained not to implement chopping or sigma-delta modulation. Also is explained how a dynamic element matching scheme is being used in the current sources and how a source follower is being used to drive the column in the pixel array.

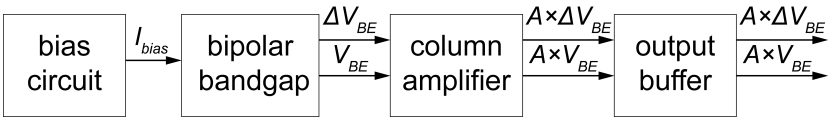

Figure 6.3: Schematic overview of the temperature sensor in conjunction with the imagers readout.

6.1 Possibility of chopping and sigma-delta modulation

The direct availability of a ΔV_{BE} voltage in a pair of diode connected BJTs allows for circuit techniques like chopping and sigma-delta modulation [1], [22], [23]. For the temperature measurement across the whole surface of the image sensor array, many T-sensors are going to be implemented. Sigma-delta modulation, as shown in Figure 6.4, would require the implementation of a sigma-delta modulator and decimation filter for every T-sensor; hence every column. These structures would then have to be integrated along side the readout circuitry with CDS, since these two are not compatible. There would hardly be enough space in the columns of the imager to do this and integration would be very complex and time consuming.

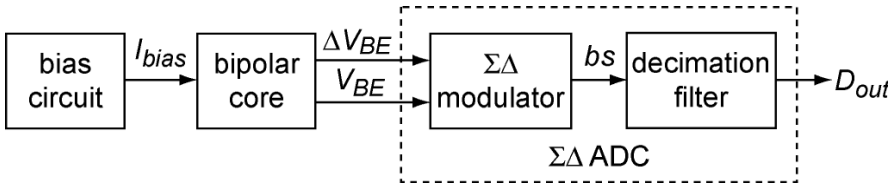

Figure 6.4: Overview of the implementation of Sigma-Delta modulation [23].

If chopping is considered, a nested chopper scheme, like the one shown in Figure 6.5, would require a different structure for the front-end amplifier. The front-end amplifier is already designed with the focus on low noise ($33\mu W$@gain=16), therefore implementation of a chopper amplifier will have very limited benefit versus the introduced complexity. In the interest of time there has been chosen not to try to implement chopping and sigma-delta modulation in the design of this thesis.

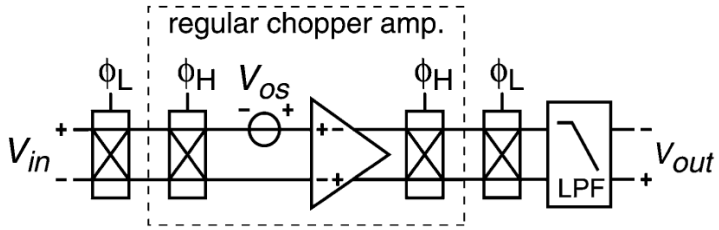

Figure 6.5: Overview of the implementation of nested chopping [24].

If circuit techniques like the ones mentioned above are not going to be used, a pair of diode connected BJTs can be replaced by a single BJT to save area as shown in Figure 6.2. The single BJT configuration has the disadvantage that two samples have to be taken, instead of one. But the base-emitter voltage V_{BE} is still available to measure and can possibly be used as a complementary to absolute temperature (CTAT), for the construction of a voltage reference.

6.2 Dynamic element matching of current sources

The ratio of the bias emitter currents, used to generate a voltage difference in the BJT, has to be very precise. These currents are generated outside the pixel array by 4 unit element sources and switches, as can be seen in Figure 6.6. There has been chosen for only 4 unit element sources, because the range of current ratio's cannot be too large to prevent the onset of high-level current injection or current-gain variations, as explained in section 5.4.

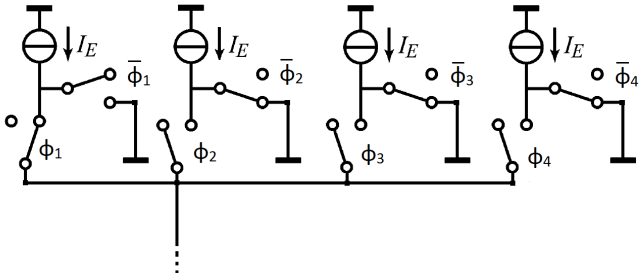

Figure 6.6: Schematic of the four current sources used to generate an emitter current ratio to bias the BJT.

The 4 unit current sources can generate different current ratio's of 1:2, 1:3, 1:4, and can be used in a dynamic element matching (DEM) scheme to reduce process mismatch. Another choice could be that of binary current sources, which would decrease switch complexity, but matching of binary current sources is inferior to unit element ones.

Two DEM schemes are possible; one in the analog and one in the digital domain. Analog DEM involves switching the sources in high speed manner within the settling time of the front-end amplifier ($150ns$). This will also show a reduction in flicker noise if the corner frequency of the flicker noise (10kHz for this design) is less than the cycling frequency chosen in the DEM scheme [12].

The slower method would be digitally averaging the output samples and this way averaging away the mismatch error. This last method will show less accuracy.

The current generated by the current sources is not only process dependent but also temperature dependent. To reduce the error in the measurement, this current dependence has to be countered. Therefore in this design, for simplicity reasons and testing reasons, there has been chosen to use an off-chip reference current as bias in the current mirror of the current sources.

The schematic of one of the current sources together with switches, and the bias current mirror can be seen in Figure 6.7. A BJT is used as load to reduce the current swing during switching. The control signals ϕ and $\bar{\phi}$ for switching between sources is digital and off-chip. This way the duty cycles of signals ϕ and $\bar{\phi}$ can be programmed to have a certain overlap, to have less current swing. In Figure 6.8 can be seen that the settling time of a switched current source is about 6ns.

6.3 Source follower in sensor

The wires of a column bus in a pixel array are connected to many pixels and therefore have a large capacitance. To still drive the column bus with a signal generated at pixel level, a source follower (SF) is being used. A SF has greater driving capabilities but has a random, process dependent offset. This offset can be canceled by correlated double sampling (CDS) as is already done in image sensors, to cancel the reset noise/kTC-noise of the floating diffusion.

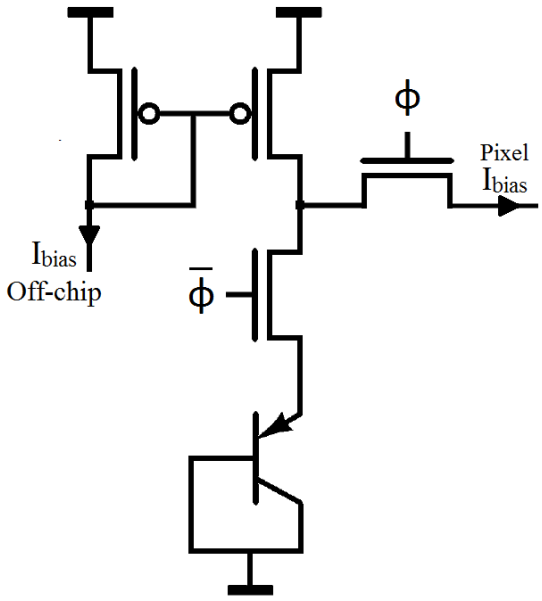

Figure 6.7: Schematic of a single current source with switches, BJT load and off-chip bias current mirror.

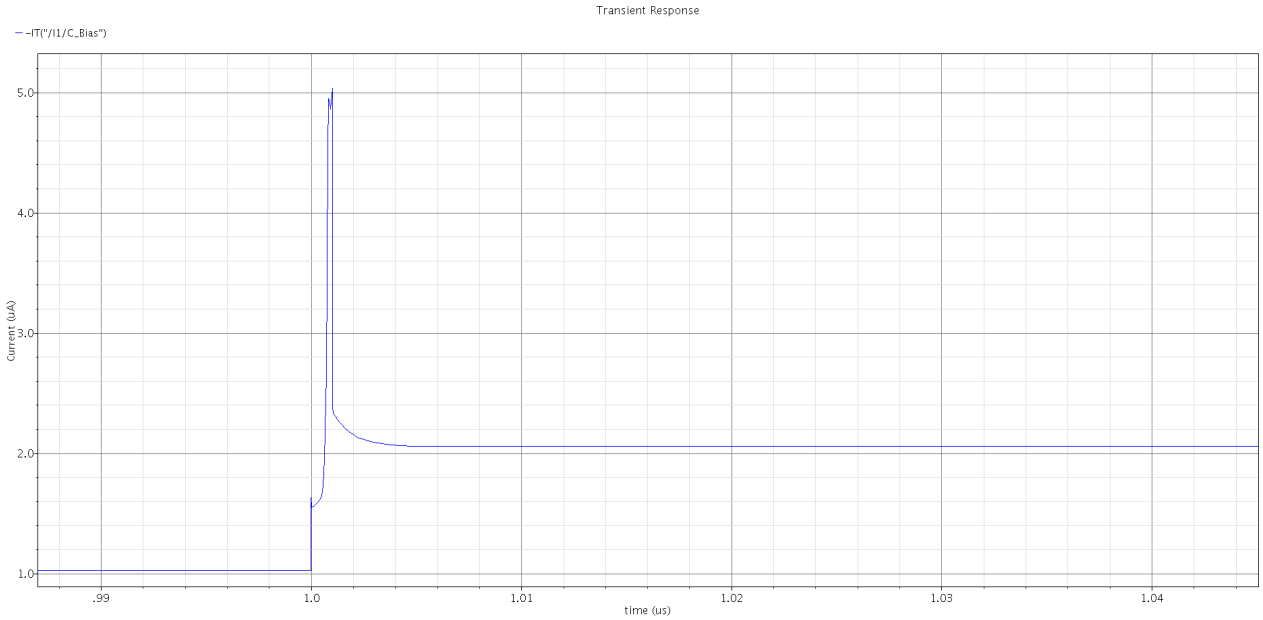

Figure 6.8: Settling time of a single current source, when switching from 1μA to 2μA.

The SF that is used for this buffered V_{BE} measurement, has to show great linearity. The V_{BE} voltage that is going to be measured, ranges from 0.6 to 0.8V for operation in a temperature range of -40 to 100°C. The nMOS SF shows bad linearity in this voltage range and therefore there has been opted for a pMOS SF. In Figure 6.9 the simulated linearity in this range is indicated by the red circle

(note that Vdd is 3.3V in the pixel array).

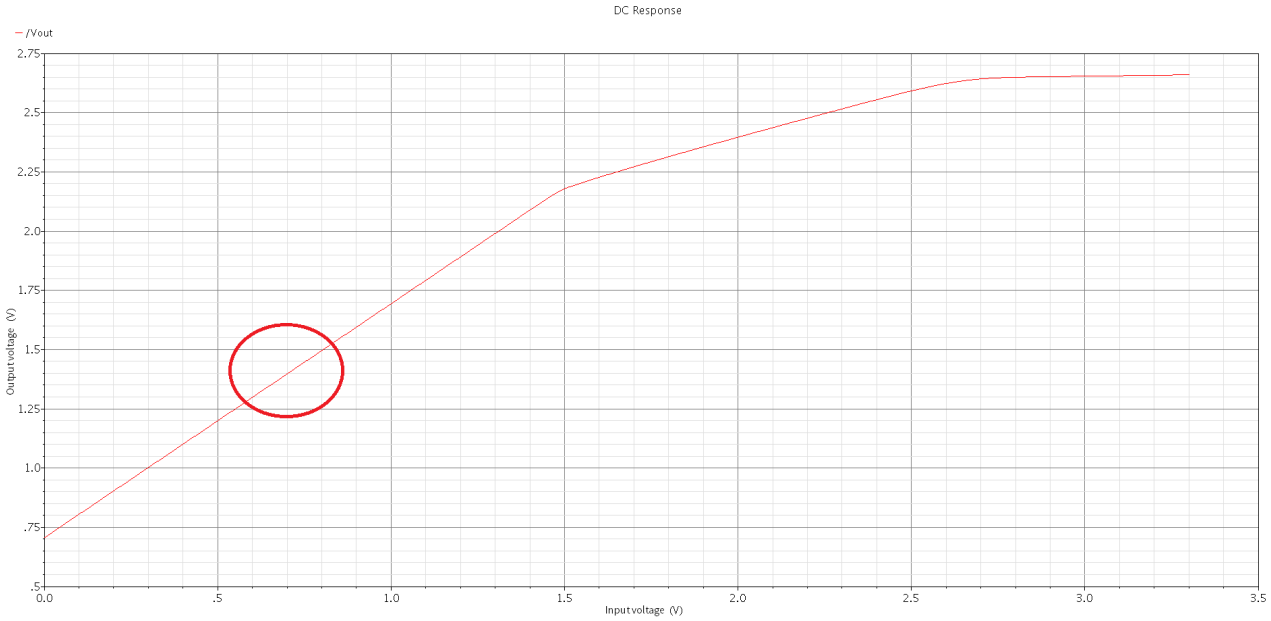

Figure 6.9: Simulation of input voltage vs output voltage of the pMOS source follower (range of interest is highlighted by red circle).

In Figure 6.10 the schematic of the pMOS source follower can be seen. By connecting the substrate well to the source of the transistor, that functions as the driver, the bulk modulation effect is countered and precision is improved [25].

The implication of using a pMOS SF instead of the nMOS SF, is that the current source from the nMOS SF cannot be used anymore. This load for the nMOS SF is located outside the pixel array in the column bus, as can be seen in Figure 2.3. The transistor that is going to act as load for the pMOS SF can be placed at pixel level, or can be placed outside the pixel array at column or row level.

Since, in this design, the signal *RS* of the imager is applied per row and is being used to switch on the SF, the current provided for the SF should be per column to be able to provide a single current per SF. Unfortunately there is no more room left for interconnects in the current architecture of the pixel array to do this, and there has been chosen to implement a load current source at pixel level for each temperature sensing BJT.

6.4 Temperature sensor operation

To give a better understanding of the operation of the sensor, a full overview with signals and device parts can be seen in Figure 6.11. In theory, only ΔV_{BE} is necessary to acquire a temperature measurement. For testing purposes there has been chosen for a second 'direct V_{BE}' mode to see if driving capabilities are adequate enough and to see whether a single BJT in this configuration can be used to make a reference voltage.

The schematic of the temperature sensor together with the SF can be seen in Figure 6.12. There are two operation modes that can get controlled at pixel level: direct V_{BE} measurement, controlled by signal VS (=RST for the image pixels), or an indirect V_{BE} measurement, controlled by signal RS via the SF. In both modes a bias current, I_{bias}, controlled by signal CS is provided to the BJT.

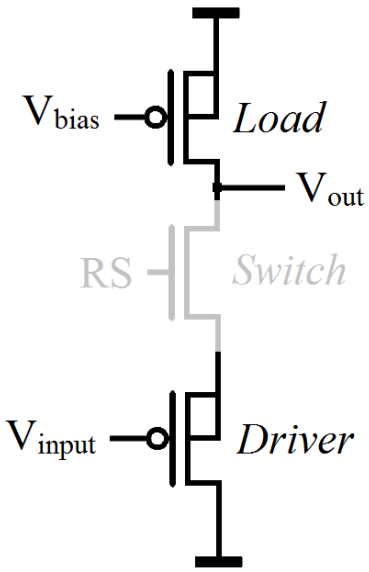

Figure 6.10: Schematic of the pMOS source follower used inside the temperature sensor, to drive the column bus of the imager. (Switch indicated in gray, as it is not part of the SF.)

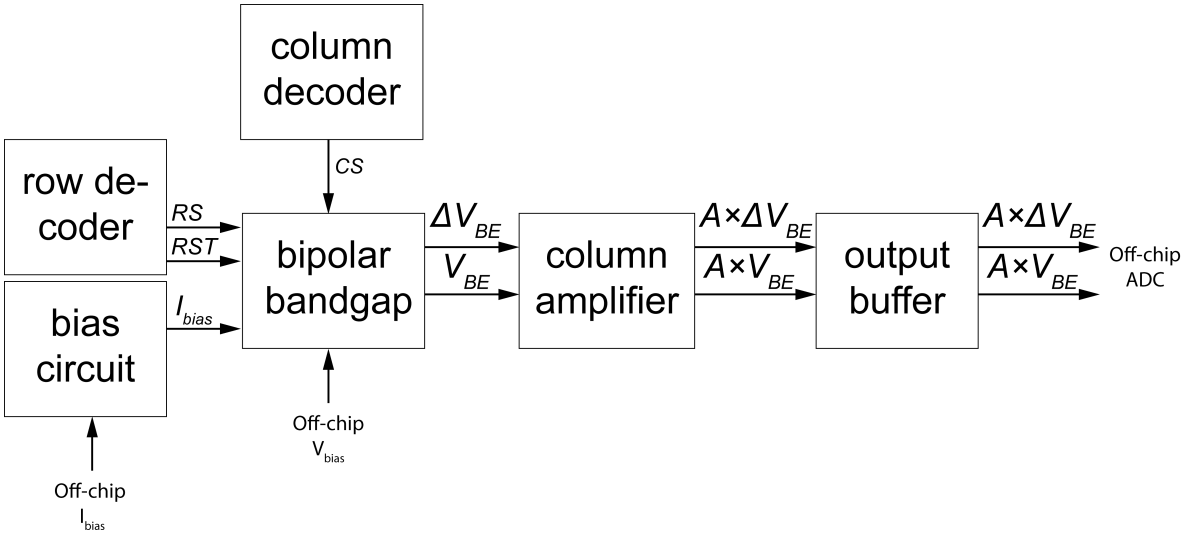

Figure 6.11: Full overview of the temperature measurement operation at chip level.

Signals *RS* and *RST* (=*VS* in the temperature sensor) are row signals that are connected to pixels and T-sensors in the row. Together with signal Tx, the conventional timing diagram of a pinned photo diode active-pixel sensor (APS) can be seen in Figure 6.13. In this figure can also been seen how the column bus signal changes, gets sampled and what the signal is after CDS.

The indirect V_{BE} measurement can be read out simultaneously with the readout operation of the image pixels. Its timing diagram can be seen in Figure 6.14. Here can be seen that signals *RS*, *RST*

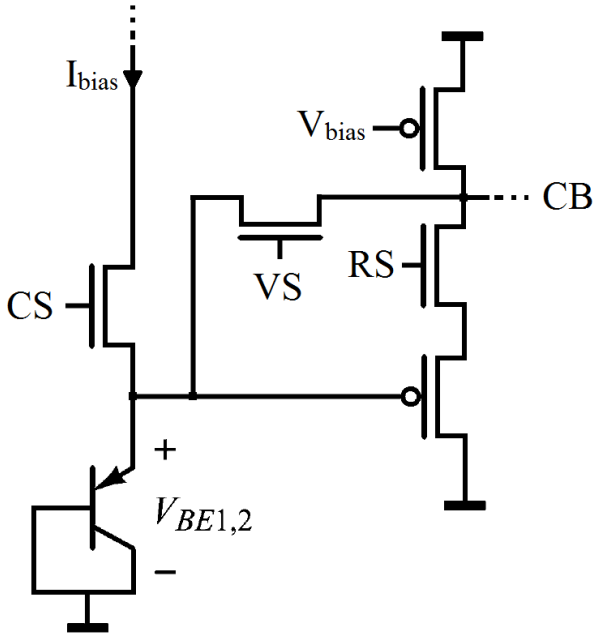

Figure 6.12: Schematic of the temperature sensor, control switches and SF at pixel level.

and Tx are the same as for the pixel readout operation. The signal of switch CS is shown together with an indication of the bias current provided. The change in bias current will create different column bus signals, that contain the V_{BE} signal, the offset from the SF and noise. After CDS these two signals become a ΔV_{BE} signal, where the offset is canceled and noise is still present.

The timing diagram of a direct V_{BE} measurement can be seen in Figure 6.15. Here can be seen that signal RS cannot be high during operation. For this reason the direct V_{BE} measurement cannot be performed while the image pixels readout operation takes place. The change in bias current will create different column bus signals, that contain the V_{BE} signal and noise. After CDS these two signals also become a ΔV_{BE} signal where noise is still present.

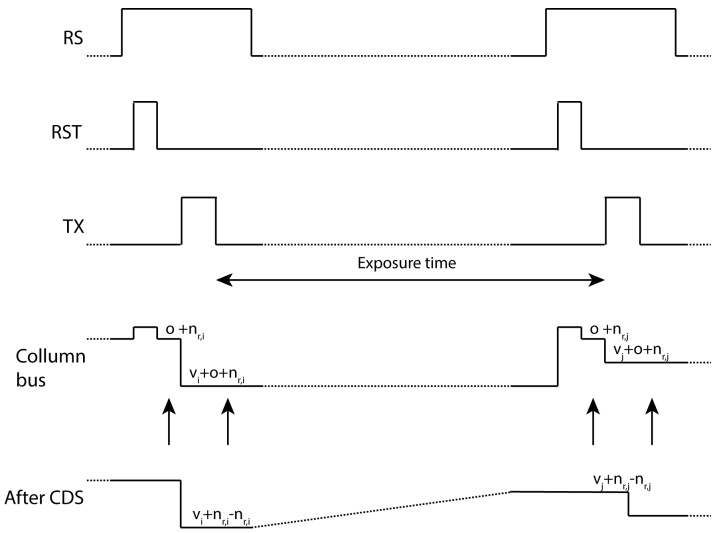

Figure 6.13: Timing diagram of a conventional pinned photo diode active-pixel sensors (APS) [26]

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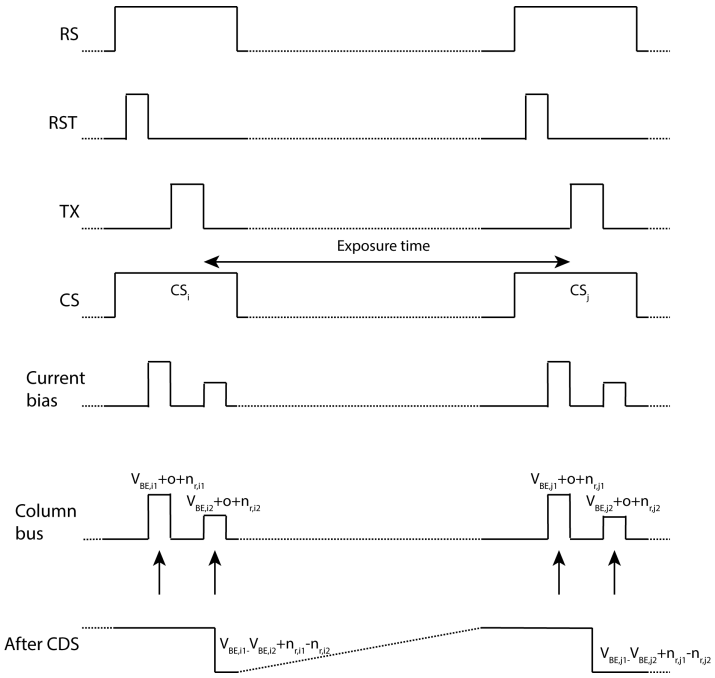


Figure 6.14: Timing diagram of the indirect V_{BE} measurement of the T-sensor.

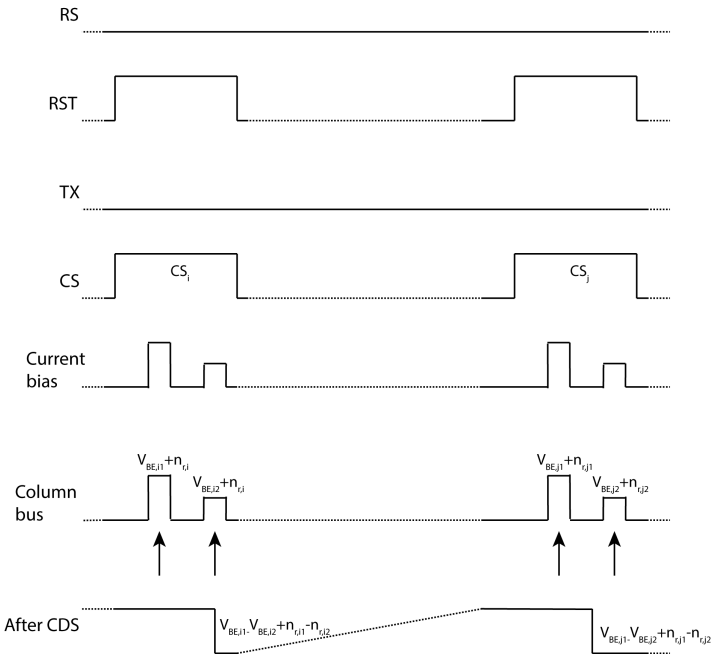


Figure 6.15: Timing diagram of the direct V_{BE} measurement of the T-sensor.

Chapter 7

Implementation of the temperature sensor

7.1 Current Sources

7.1.1 Schematic

A pMOS transistor is being used as current source that is either supplying current to the temperature sensors in the pixel array or to a BJT that functions as load and is connected to ground. This is done to minimize the current swing between switching. To reduce mismatch and flicker noise, and increase linearity, the pMOS transistors have been made relatively large. The current mirror, the control switches ϕ and $\bar{\phi}$ and the BJT load for a single current source with $\frac{W}{L}$ ratio's, can be seen in Figure 7.1.

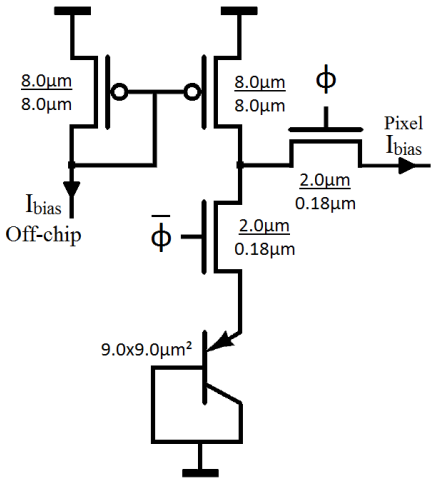


Figure 7.1: Schematic of the current mirror, the switches ϕ and $\bar{\phi}$ and the BJT load for a single current source with $\frac{W}{L}$ ratio's.

7.1.2 Layout

The layout of a single current source, with BJT load and switches, can be seen in Figure 7.2. The different devices and signals are indicated in yellow.

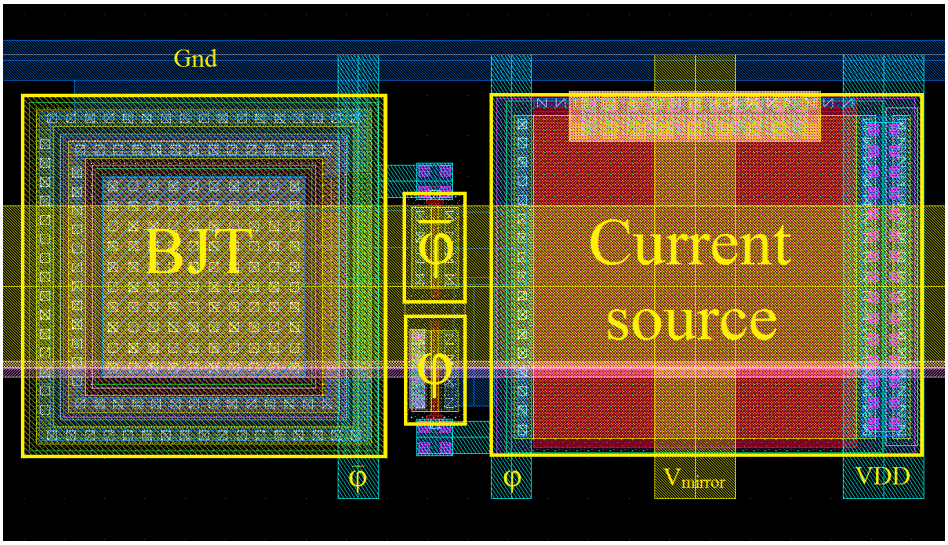


Figure 7.2: Layout of a single current source, with BJT load and switches.

The layout of four rows of four current sources can be seen in Figure 7.3.

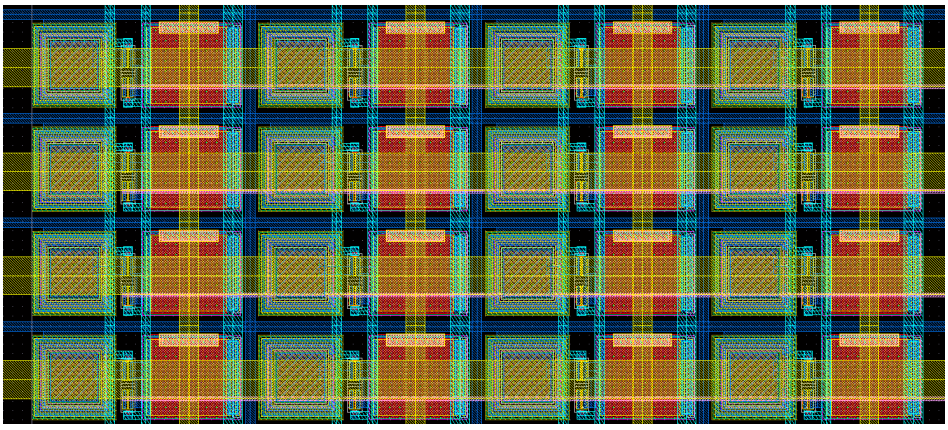


Figure 7.3: Layout of four rows of four current sources (zoomed in view of the whole array with current sources).

7.2 Temperature sensor

The pnp BJT chosen to use as bandgap reference is a standard library cell with a size of 9x9μm^2 and emitter area size of 5x5μm^2. The base and emitter of the BJT are directly shorted by a *metal-1* layer to create a base-emitter voltage. The BJT gets biased from outside the pixel array and the V_{BE} voltage also gets measured outside the pixel array.

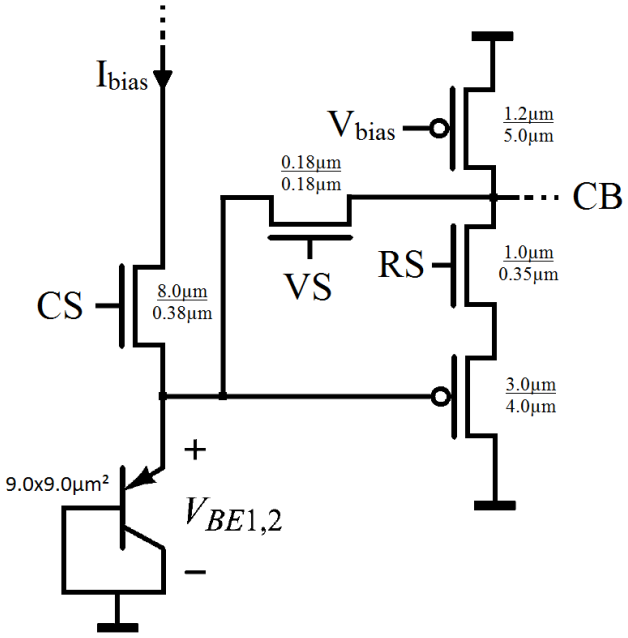


Figure 7.4: Schematic of the temperature sensor, control switches and SF at pixel level.

7.2.1 Schematic

The schematic of the temperature sensor together with the source follower (SF), with $\frac{W}{L}$ ratio's, at pixel level can be seen in Figure 7.4. There are two operation modes that can get controlled at pixel level: direct V_{BE} measurement controlled by signal VS (=RST for the imager) or an indirect V_{BE} measurement, controlled by signal RS via a SF. In both modes a bias current, I_{bias}, controlled by signal CS is provided to the BJT. The bias voltage V_{bias} for the load transistor is provided off-chip by an extra interconnect per row and is about $2.5V$. This voltage bias doesn't have to be very accurate for the SF, but constant, to function good. The sizes of the load and driver of the SF are chosen for better linearity.

7.2.2 Layout

The layout, with indicated transistor and wires names of the temperature sensor in yellow, can be seen in Figure 7.5. It upholds the area of 2 pixels, so a total area of $22\text{x}11\mu m^2$. To see the influence of light on the temperature sensor, a shielded and non-shielded version are laid out on chip with an almost 50-50 ratio.

There are two column bus interconnects running through the layout, but only one of them is being used to read out the signal. To have better matching between the two columns, dummy switches have been attached to the unused column.

7.3 Pixel array

Around every 5 pixels a temperature sensor has been laid out across the whole pixel array. This is far more than necessary to sense a temperature gradient, and will degrade the image quality of the picture severely, but has been done for testing purposes.

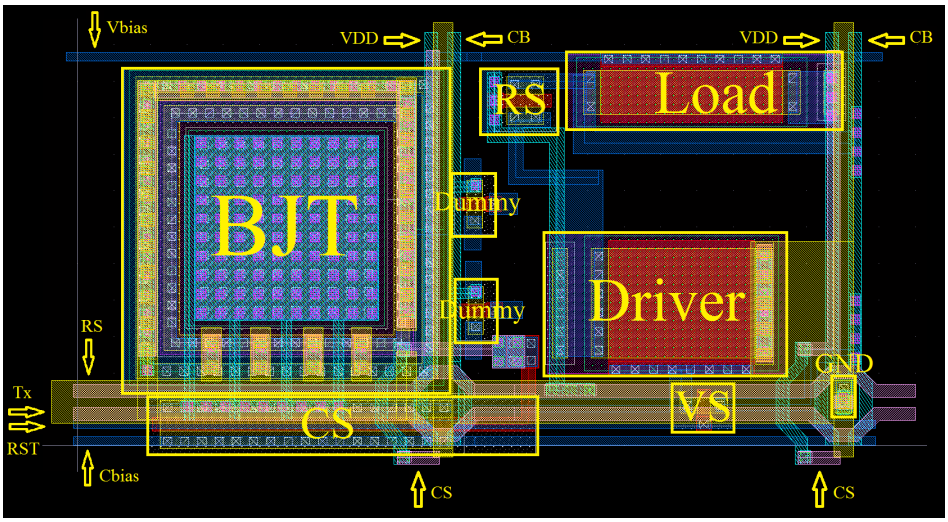


Figure 7.5: Layout of the temperature sensor with transistor and wires names indicated in yellow.

7.3.1 Layout

The total pixel array is 198x66 and the effective array size is 192x64 as can be seen in the build up in Table 7.1. The test columns are directly read out by the chip output buffer and column amplification is skipped, to see its output. The dummy columns are readout normally, but also a test input signal can be connected to the column amplifier to test the column readout.

Table 7.1: Build up of full pixel array.

66 rows	1 dummy
	64 normal
	1 dummy

198 columns				
2 test	1 dummy	192 normal	1 dummy	2 test

A close up view of the layout of the pixel array can be seen in Figure 7.6. In this view the non-shielded version of the temperature sensor and the (by *top metal* layer) shielded version can be seen. A total of 266 non-shielded and 276 shielded temperature sensors have been implemented in the array.

To enhance a temperature gradient across the array two heaters have been placed to the top and the bottom of the array. These are implemented by a wide *metal-1* layer, with resistances of 6.9Ω and 6.6Ω, for the top and bottom heater respectively. A close up layout of a part of the heaters, indicated in yellow, next to the pixel array can be seen in Figure 7.7. The voltages are supplied separately to each heater from off-chip.

7.4 Chip

7.4.1 Layout

A top level lay out view, with the most important area's indicated, can be seen in Figure 7.8. A full layout view of the complete chip, with bondpads and decoupling capacitors, can be seen in Figure 7.9.

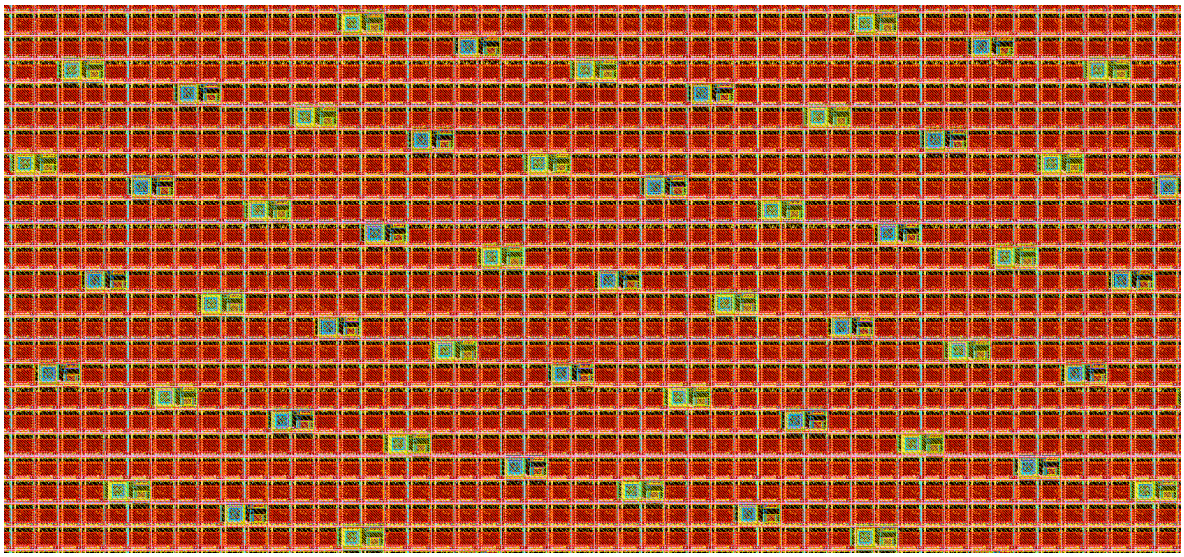


Figure 7.6: Close up view of the layout of the pixel array. Note the implementation of a shielded and non-shielded version of the temperature sensor.

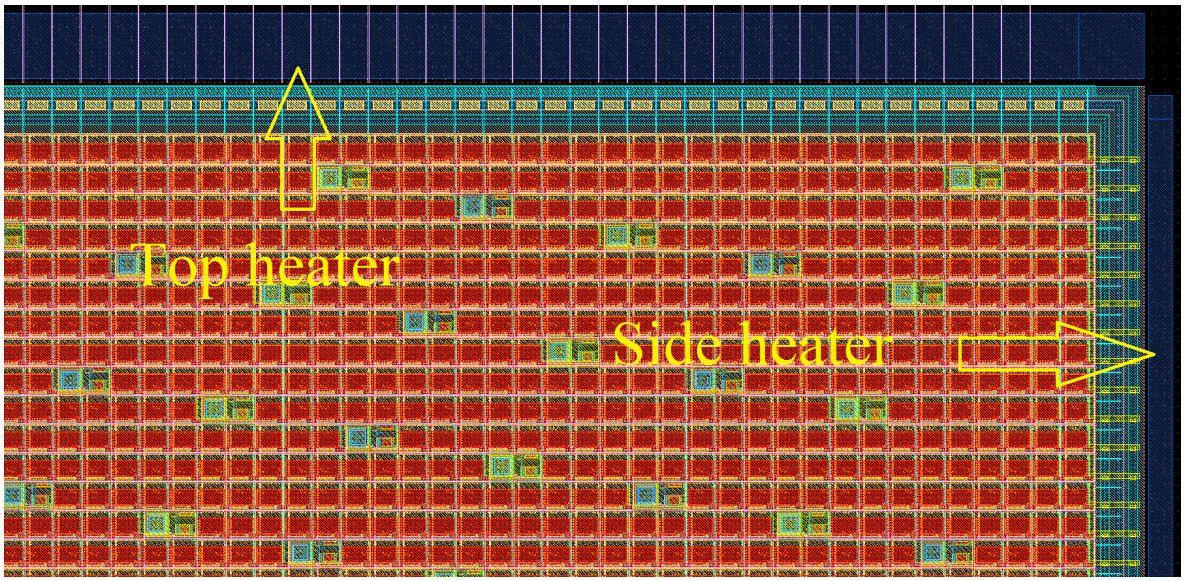


Figure 7.7: Position of the top and side heater with regard to the pixel array in the layout.

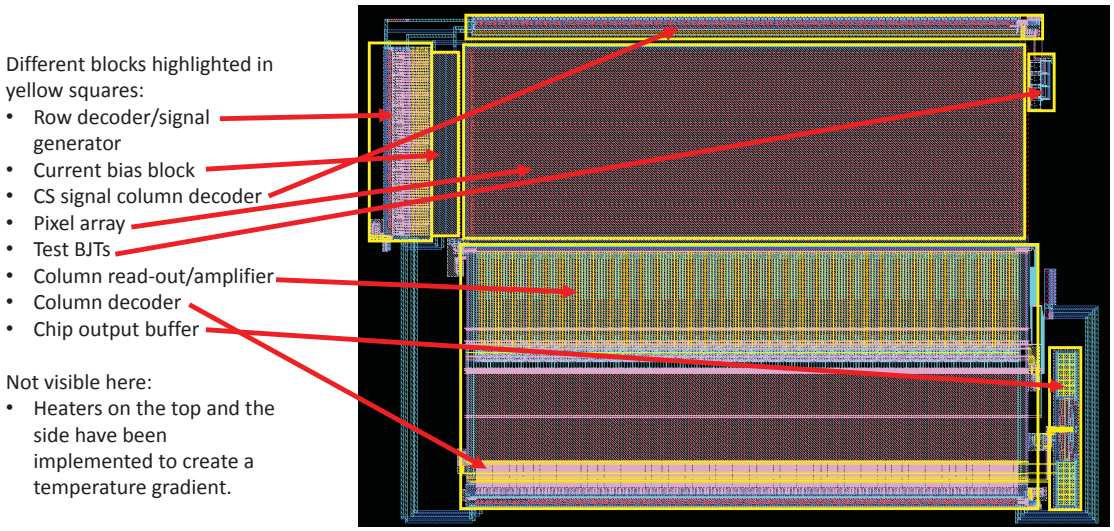


Figure 7.8: Overview with all the functional layout blocks indicated in yellow squares, and their functionality indicated by red arrows.

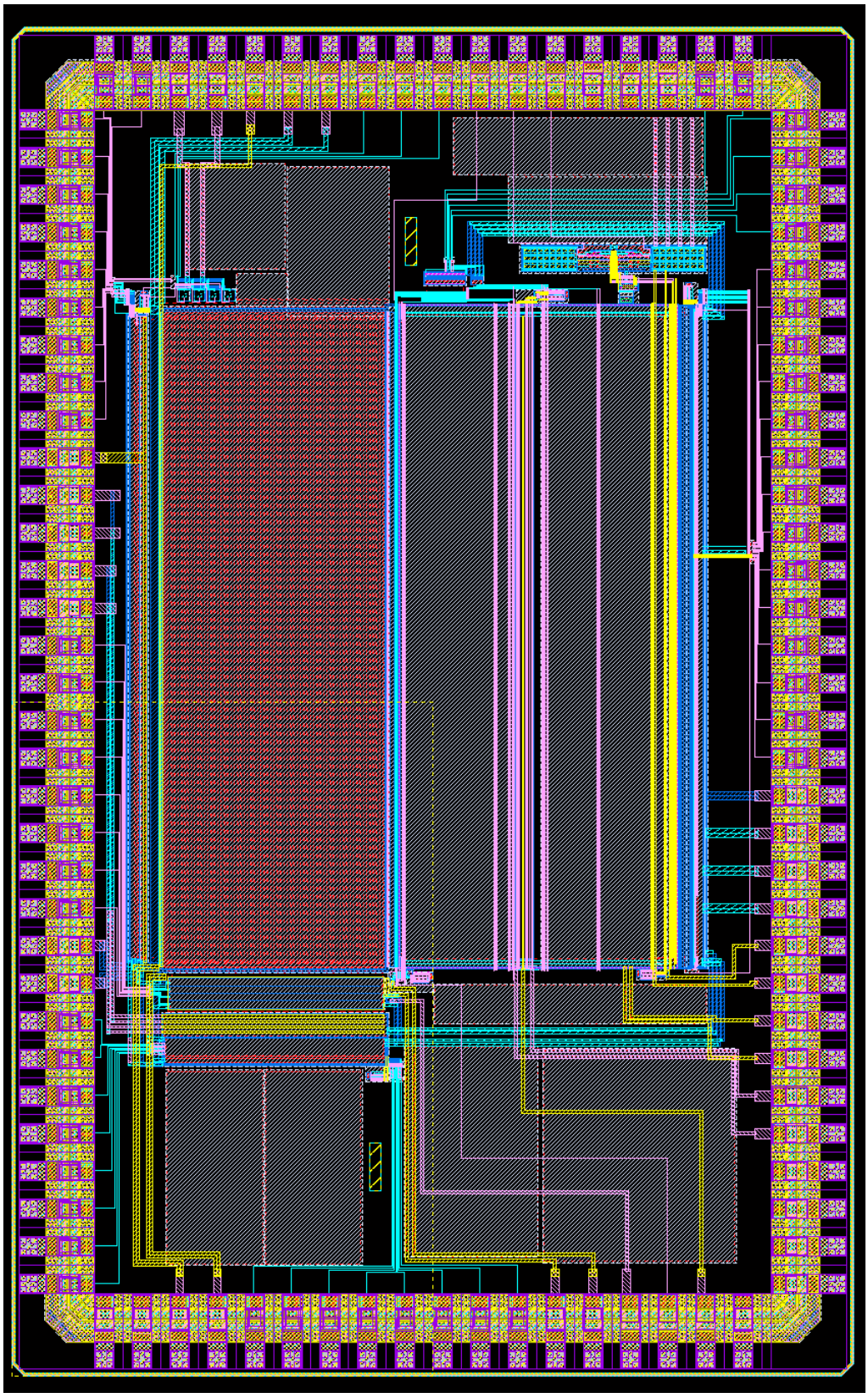


Figure 7.9: Complete layout overview of the chip, including bondpads, connecting wires and decoupling capacitors.

Chapter 8

Conclusion and recommendations

Conclusion Research done has shown that the parasitic pnp BJT is the best device to be used in the design of a temperature sensor for integration, because of its small occupied area and good stress sensitivity compared to other devices. This type of BJT is widely available in CMOS processes and temperature could easily be extracted by the readout of an image sensor with CDS, with the use of a ΔV_{BE} measurement.

A single pnp BJT, a pMOS source follower and control switches have been successfully used in the design and layout of the temperature sensing part at pixel level, that only occupies 22x11μm^2. In this design the base-emitter voltage can directly be sampled, or via the source follower, and both modes are controlled by the same signals as the image pixels. One interconnect for the bias voltage of the source follower has been added to the array.

Four current sources have been used to produce different bias current ratio's for the temperature sensor, and can work in a DEM scheme to improve accuracy. The speed and matching performance of the DEM scheme has yet to be determined by testing. The bias currents are supplied from outside the array by an interconnect. Another interconnect has been added to control the current supply per sensor.

For both the readout of the temperature signal and the video signal, the same column amplifier circuit is used. This shows the high integratabilty of a pnp BJT based temperature sensor into this kind of image array.

The accuracy of the temperature sensor, as designed in this thesis, will not show very high accuracy compared to dedicated temperature sensors. But for this application very high accuracy is not needed. Circuit techniques, to more adequately counter noise sources, mismatch, temperature dependence, etc. can be implemented, but this requires a far more complex readout circuit, which alters the structure overall.

At the moment of writing the designed layout still is waiting for tape-out. Therefore there are no measurement results present in this thesis.

To conclude, in this thesis a successful integration of a temperature sensor into an image array has been presented.

Recommendations The set-up of this design has its emphasis on a lot of sensors, mainly for testing purposes. This degrades the quality of the image sensor so much, that it will be unpractical to use. In a more practical design, there should be chosen to have less sensors, for example only 10 in a far larger array size. Together then with high accuracy temperature sensors just outside the array, also a temperature gradient can be extracted and be used for compensation.

If is chosen for even a few sensors, there is also the choice of having a different readout circuit overall. That circuit would be different from the column readout that is being used in this thesis, and in that case doesn't have to be read out column wise. It just requires extra interconnects to bias the BJT and to transfer the bandgap signal outside the array.

A big step can also be made when both temperature sensor and image pixel are designed at the same time to have better integration. This will deliver a far more efficient layout with better interconnect management and less image quality degradation. Also a change in source follower type in the image pixel from nMOS to pMOS, allows for the sharing of the load current source used in the temperature sensor. This way this load can be at column level in stead of pixel level, which saves area.

A totally different approach could be to use a shielded image pixel to measure dark current to extract temperature. From calibration the temperature dependence of the dark current of the shielded pixel can be determined. The extracted temperature can then be used to compensate for dark current noise of the surrounding pixels.

Appendix A

Analog Front-End Circuit

Table A.1: Specification of the front-end amplifier

Power Dissipation	3.3Vx30μA
Output range	1.5V
Common Mode Voltage	1.1V
Open-loop Gain	85dB
-3dB Bandwidth	6.5Hz $\sim$ 2.4MHz(@ gain = 16)
Gain Bandwidth	50MHz
Input referred Noise	33μV (@ gain = 16)
Settling time	150ns
PSRR	vs. Power Supply 60dB (@ 2MHz)
	vs. Groud 28dB (@ 2MHz)
Load Capacitance	700fF

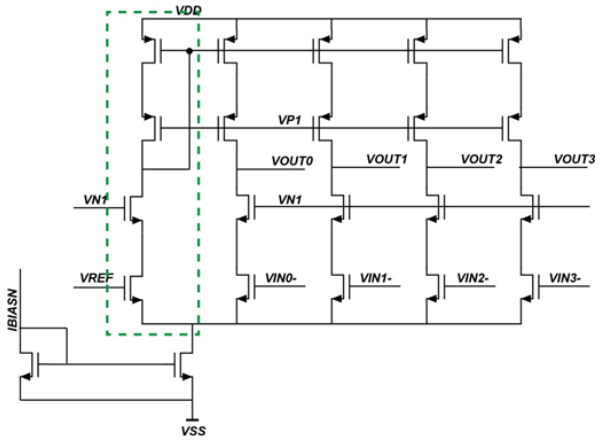


Figure A.1: Schematic of the front-end amplifier with the implementation of OTA sharing technique.

Appendix B

Technical report

On the next page a technical report of the chip can be found. In this document is further explained how the chip works and are all input/output signals explained.

Technical report

Integrating a temperature sensor into a cmos image sensor

Author: BSc. J. Markenhof

Supervisor: Prof. Dr. Ir. A.J.P. Theuwissen

Co-design: Ir. X. Ge

Introduction

The image pixel design/readout was copied from Xiaoliang Ge, so for these parts she knows the design better than me. I suggest that also is looked in Cadence to the overall (schematic) design. Files *top_level_chip7* and *top_level4* in folder *4M1L_top* of my directory are the top level design files.

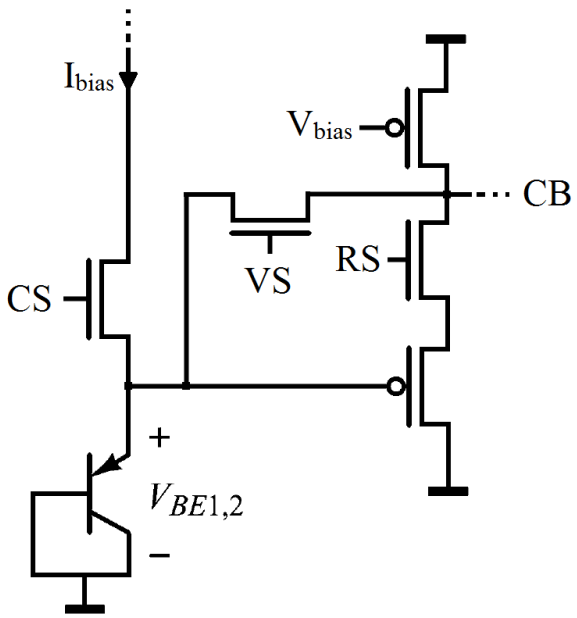
There are too many layers and black boxes to put in this file. For example many control signals are generated on chip to decrease input bondpads, that are not being discussed at this top level approach.

Array build-up

The total array consists of 198x66 pixels. The buildup of the array is as follows:

	1 dummy	row<0>		198 columns				
	64 normal	row<1:62>		2 test	1 dummy	192 normal	1 dummy	2 test
66 rows	1 dummy	row<63>		column<0:1>	column<2>	column<3:194>	column<195>	column<196:197>

Pixel layout



The T-sensor (figure 1) is controlled by signal VS of RS. VS is actually signal RST, but named differently since it has a different function. Signals RS and RST are the same signal as the image pixel signals. For an 4T image pixel at some point in the readout, both RS and RST will be high, in the T-sensor this will create a problem, so the T-sensor cannot be read out together with the image pixels.

When the image pixels are read out RST and RS are applied per row to also the T-sensors, so switch CS needs to be closed (low signal) to make sure that the T-sensor is not operating. Also voltage V_bias needs to be off. This will prevent any signal to the column bus (CB).

Figure 1: Schematic overview of the T-sensor.

Row signals

The control row signals are IN_ROW<0:6>. By binary row decoding every row can be enabled for reading. To enable the IN_ROW signals, DIRECTION_ROW has to be high; this is digital.

For every row, signals RST, TG, RS, RSTB can be enabled by RSTEN, TGEN, RSEN, RSTBEN **and** RST_IN, TG_IN, RS_IN, RSTB_IN; these are digital. The value of RST, TG, RS, RSTB can be set by RST_HIGH, TG_ HIGH, RS_ HIGH, RSTB_ HIGH; these are analog.

At pixel level the VDD33 voltage is 3.3V and so for the T-sensor operation a voltage of 3.3V is advised. But these can be varied up to 5.0V.

Column signals

The control column signals are IN_COL<0:7>. By binary column decoding every column can be enabled for reading. These are all digital. To enable the IN_COL signals, DIRECTION_COL has to be high; this is digital.

For every column, signals COL_CONTROL_IN, COL_READR_IN, COL_READS_IN, INIT_IN, SHS_IN, SHR_IN are used to control the different steps in the column amplifier, like sampling, holding, buffering, etc. (Also see table 1 of this document)

The output signal of columns <3:195> (the normal columns) is put out to CHIP_OUT1.

Bias current

The current bias is generated for every row regardless. The current bias is supplied by C_BIAS_CS to a current mirror, that is parallel to the current sources. The current needs to around 1uA. This way every unit current source is 1uA and the maximum current will be 4uA. This should be low enough to prevent any form of high/low level current injection (read thesis for more details).

Per column the bias current switch inside the T-sensor can be switch on/off by IN_CS<0:7> by binary decoding; these are digital signals. To enable the IN_CS signals, DIRECTION_CS has to be high; this is digital. The value of CS can be set by CS_ HIGH; this is analog.

The amount of unit current per row and the switching of the current sources (DEM) are controlled by Phi_not<0:3> and Phi<0:3>. The current to every single temperature sensor is controlled at column level by IN_CS<0:7>. This means that multiple T-sensors in a column will be supplied by a bias current, but the readout is done per row (by signals RST, TG, RS, RSTB) and this makes that a single T-sensor can be read out.

Test BJTs

Select_test_BJT0, Select_test_BJT1 are digital and binary decoded to control the 4 test BJTs. Test_BJT_C, Test_BJT_E, Test_BJT_B are respectively the collector, emitter and collector access for the selected BJT; these are analog.

The test BJT's can be used to characterize the BJT more precise. For example more than in the characterization report of Tower: **'TS18 Analog Device Characterization Report', Doc. Name: CZ2 ANTS18, Rev. Num: 1.5, FIGURE 12-15: BETA VS. COLLECTOR CURRENT (5X5 muM2 Emitter).**

Heaters

On the top and side of the array heaters have been implemented. By applying a voltage to V_heater_top and V_heater_side a current will run; these are analog. The resistance of the top heater is 6.9Ohm and of the side heater is 6.6Ohm. It is not clear how much the heaters will heat up for the amount of current that will run.

Test signals

A0 and A1 are digital and binary decoded to control the 4 test columns (0, 1, 196, 197). This allows to put the output of every selected test column to CHIP_OUT2.

Test column readout

TEST_OUT_SIG1, TEST_OUT_SIG2 are digital and control an input test signal to the dummy columns (column 2 and 195) to test the column readout. The test signal is generation inside the chip via the SPI input.

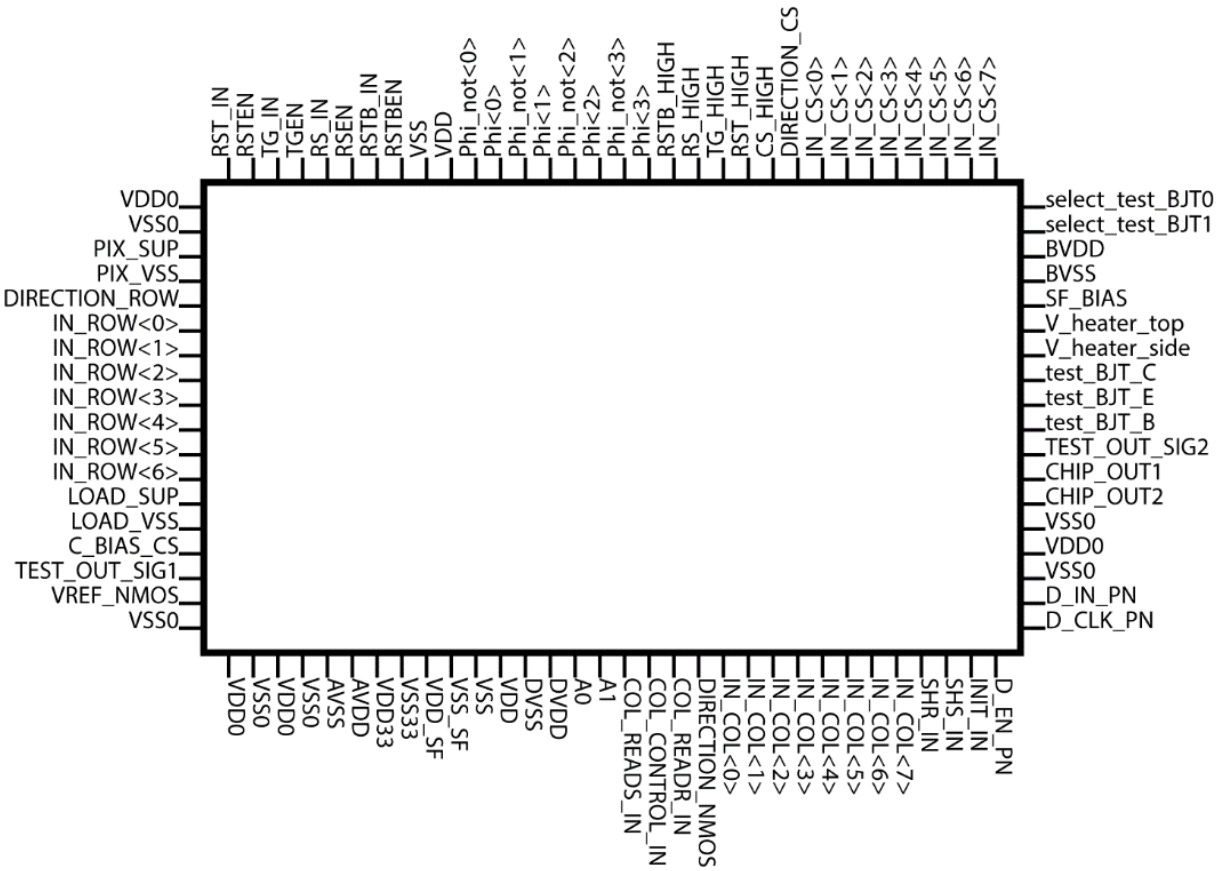


Figure 2: Chip bondpad connection overview.

Table 1: List of input/output signals with function description.

Port name	Type of signal	Description
A0/A1	Digital (1.8V)	Control for 4 test columns
DIRECTION_ROW	Digital (1.8V)	Global control for IN_ROW
IN_ROW<0:6>	Digital (1.8V)	Binary row encoder to control row signals RST, TG, RS, RSTB.
RSTEN, TGEN, RSEN, RSTBEN, RST_IN, TG_IN, RS_IN, RSTB_IN	Digital (1.8V)	Control signals to enable RST, TG, RS, RSTB
RST_HIG, TG_HIGH, RS_HIGH, RSTB_HIGH	Analog	The supply voltages of the row level shift for RST, TG, RS, RSTB
select_test_BJT0, select_test_BJT1	Digital (1.8V)	Control signals for the 4 test BJTs, via binary decoding.

Phi_not<0:3>, Phi<0:3>	Digital (1.8V)	Control signals to switch on/off current bias sources. (4 per row)
TEST_OUT_SIG1, TEST_OUT_SIG2	Digital (1.8V)	Signals to create test signals at the readout of the dummy columns (2, 195). The test signal is generated on chip via SPI.
VSS33, VDD33	Analog	Ground and supply voltage for 3.3V devices
VSS, VDD	Analog	Ground and supply voltage for 1.8V devices
VSS0, VDD0	Analog	Ground and supply voltage paddings
LOAD_VSS, LOAD_SUP	Analog	Ground and supply voltage for nmos pixel bias circuit.
AVSS, AVDD	Analog	Ground and supply voltage for telescopic gain amplifier bias circuit, and telescopic gain amplifier.
BVSS, BVDD	Analog	Ground and supply voltage for test BJT guard rings.
DVSS, DVDD	Analog	Ground and supply voltage for row/column logic level shift.
PIX_VSS, PIX_SUP	Analog	Ground and supply voltage for pixels
VSS_SF, VDD_SF	Analog	Ground and supply voltage for unity gain buffers
V_heater_top	Analog	Supply voltage for heater at the top
V_heater_side	Analog	Supply voltage for heater at the side
SF_BIAS	Analog	Supply bias voltage for T-sensor source follower (driver).
test_BJT_E	Analog	Emitter connection for selected test BJT
test_BJT_C	Analog	Collector connection for selected test BJT
test_BJT_B	Analog	Base connection for selected test BJT
DIRECTION_COL	Digital (1.8V)	Global control for IN_COL
IN_COL<0:7>	Digital (1.8V)	Binary column encoder to control column signals COL_CONTROL_IN, COL_READR_IN, COL_READS_IN.
D_IN_PN, D_CLK_PN, D_EN_PN	Digital (1.8V)	Control signals for the SPI interface.
COL_CONTROL_IN	Digital (1.8V)	On/off signal for column switch
COL_READR_IN	Digital (1.8V)	Signal to read S/H caps
COL_READS_IN	Digital (1.8V)	Signal to read S/H caps
INIT_IN	Digital (1.8V)	Signal for sampling of CDS
SHS_IN	Digital (1.8V)	Signal to sample S/H caps
SHR_IN	Digital (1.8V)	Signal to sample S/H caps
VREF_NMOS	Analog	Reference voltage for programmable gain amplifier.
DIRECTION_CS	Digital (1.8V)	Global control for IN_CS
IN_CS<0:7>	Digital (1.8V)	Binary column encoder to control column signal CS
CS_HIGH	Analog	Supply voltage for column logic level shift.
C_BIAS_CS	Analog	Supply bias current for current mirror current sources.
CHIP_OUT1	Digital (1.8V)	Output for pixel column signals

CHIP_OUT2	Digital (1.8V)	Output for test column signals (selected by A0/A1)

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Summary

Dark current noise in image sensors is highly sensitive to temperature, and a difference in temperature in image sensors can be seen in the image as a non-uniform noise source. Many CMOS image sensors are integrated in mobile devices and lack a physical shutter to generate dark frame subtraction to compensate for dark current noise. In this thesis, the design and implementation of a bandgap based temperature sensor into an image array is proposed. A single parasitic pnp BJT, together with a source follower and control switches, is integrated inside an image array and is biased from outside the array. By means of CDS in the column amplifier of the imager, the difference in base-emitter voltage of a single BJT, that is being biased by a known current ratio, can be measured to calculate temperature. A total of 542 temperature sensors are fully integrated in a 192x64 test array of 4T APS based pixels and share the same readout as the image pixels. At the moment of writing, the chip was still waiting for tape-out and no measurement results can be presented in this thesis.