Analysis of Negative Sequence Current Control for MMC HVDC Transmission Systems

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Analysis of Negative Sequence Current Control for MMC HVDC Transmission Systems

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Abstract

High Voltage Direct Current (HVDC) transmission system technology has recently attracted a lot of attention within the power system community. Modular Multilevel Converter (MMC) HVDC is the state of the art HVDC transmission technology, which contains hundreds and even thousands of submodules. It is the modularity, scalability and efficiency that are the most striking advantages[1] of the MMC HVDC next to the reduced harmonic content of the output currents and the smaller AC filter size [2]. The Electro Magnetic Transient (EMT) type simulation of the MMC HVDC transmission system faces the challenge of large computation time. In tackling that problem, the efficient model offers great improvements in terms of simulation time duration without compromising the accuracy[3].

One of the grid code requirements which is under discussion and is being proposed nowadays involves the control of the negative sequence current components by means of Voltage Source Converter (VSC) HVDC systems during asymmetrical faults. The VSC HVDC system should be able to withstand the negative phase loading during asymmetrical faults without tripping the converter[4]. This negative sequence component can be controlled with the enhanced control scheme which is known as Negative Sequence Current Control (NSCC). It allows negative sequence currents in VSC HVDC either to be suppressed or injected depending on the choice of Transmission System Operators (TSO). Suppression or injection of the negative sequence current demonstrates a different response to the power system performance during asymmetrical faults.

This MSc thesis discusses the NSCC implementation using the efficient model of MMC HVDC transmission in the PSCAD / EMTDC. This thesis shows that the suppression of the negative sequence current (it is commonly applied by vendors) by the MMC HVDC converter leads to reduced negative sequence current components. With only the positive sequence current present, three phase currents appear as balanced [5] during asymmetrical voltage conditions and so the converter is able to withstand the asymmetrical current fault. However, although this is beneficial from the power electronic component perspective, it has the drawbacks firstly of the double frequency power oscillations in the DC link, and secondly of the increased overvoltage which occurs because of the rise in the negative sequence voltages. Furthermore, the fault currents at the converter terminals appear to be very low in the steady state values range.
As an alternative approach, the injection of negative sequence current is studied here. The motivation for the negative sequence current injection is either the enhancement of AC system protection schemes or the suppression of double frequency harmonics in the output power during faults. These are the different ways and methods that are evaluated in this work. The adequate injection of the negative sequence current during asymmetrical faults shows improvements in the DC voltage and power ripples in different case studies.

Both the NSCC suppression and the NSSC injection in relation to the MMC HVDC are tested in the point to point MMC HVDC, 3 terminal MTDC and 9 bus AC grid connected Western System Coordinating Council (WSCC) with point to point MMC HVDC connection. In the 3 Terminal MMC HVDC applications, NSCC implementation shows optimal effects in the terminal where the single line to ground fault is applied. In the point to point MMC HVDC interconnection with 9 bus AC system, NSCC shows its effect in every section of the AC system. Moreover, the effect of NSCC is strongest near the MMC HVDC terminal in which NSCC is activated.
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<td>DC</td>
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<td>DEM</td>
<td>Detailed Equivalent Model</td>
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<tr>
<td>DLG</td>
<td>Double Line to Ground</td>
</tr>
<tr>
<td>EMT</td>
<td>Electro Magnetic Transient</td>
</tr>
<tr>
<td>FACTS</td>
<td>Flexible AC Transmission Systems</td>
</tr>
<tr>
<td>HVAC</td>
<td>High Voltage Alternating Current</td>
</tr>
<tr>
<td>HVDC</td>
<td>High Voltage Direct Current</td>
</tr>
<tr>
<td>IGBT</td>
<td>Inter Gate Bipolar Transistor</td>
</tr>
<tr>
<td>LCC</td>
<td>Line Commutated Converter</td>
</tr>
<tr>
<td>MMC</td>
<td>Modular Multilevel Converter</td>
</tr>
<tr>
<td>MTDC</td>
<td>Multi Terminal DC</td>
</tr>
<tr>
<td>NF</td>
<td>Notch Filter</td>
</tr>
<tr>
<td>NFSS</td>
<td>Nested Fast and Simultaneous Solutions</td>
</tr>
<tr>
<td>NSCC</td>
<td>Negative Sequence Current Control</td>
</tr>
<tr>
<td>PCC</td>
<td>Point of Common Coupling</td>
</tr>
<tr>
<td>PI</td>
<td>Proportional - Integral</td>
</tr>
</tbody>
</table>

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<table>
<thead>
<tr>
<th>Abbreviation</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>PS-PWM</td>
<td>Phase-Shifted Carrier PWM</td>
</tr>
<tr>
<td>PSCAD</td>
<td>Power Systems Computer Aided Design</td>
</tr>
<tr>
<td>PLL</td>
<td>Phase Locked Loop</td>
</tr>
<tr>
<td>PWM</td>
<td>Pulse Width Modulation</td>
</tr>
<tr>
<td>SLG</td>
<td>Single Line to Ground</td>
</tr>
<tr>
<td>SM</td>
<td>Submodule</td>
</tr>
<tr>
<td>SRF</td>
<td>Synchronous Reference Frame</td>
</tr>
<tr>
<td>TDM</td>
<td>Traditional Detailed Model</td>
</tr>
<tr>
<td>TSO</td>
<td>Transmission System Operators</td>
</tr>
<tr>
<td>VSC</td>
<td>Voltage Source Converter</td>
</tr>
<tr>
<td>WSCC</td>
<td>Western System Coordinating Council</td>
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</tbody>
</table>
Acknowledgements

For me, pursuing the master of science in Delft University of Technology is one of the gift from God. I am very grateful that I have this special opportunity to deepen my knowledge about electrical power engineering.

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Alhamdulillah

Delft, University of Technology
February 29, 2016

Hariadi Aji
“Acquire knowledge, and learn tranquility and dignity.”

— Omar ibn al-Khattab
1-1 Background Considerations

Electricity cannot be separated from the economic and social activities. It is also well known that electricity demand around the world is rapidly increasing. The technology required to support this demand is getting more and more sophisticated.

This growth seen in power engineering technology started with the invention of electricity in the late 19th century. Nikola Tesla and Thomas Alva Edison were embroiled in a battle for electricity which was known as the War of the Currents [7]. Edison developed a Direct Current (DC) system, but with rising demand, problems arose for DC. DC systems could not be easily converted to different voltage levels using the technologies available at that time. This problem was a huge disadvantage for long distance electricity transmission. With that prospect in mind, Tesla developed what is known nowadays as the Alternating Current (AC) power system. The benefit was that the voltage could be easily converted to higher or lower levels using power transformers.

AC systems started to be established around the globe as the backbone of the electricity grid through transmission lines known today as High Voltage Alternating Current (HVAC). Several decades later, High Voltage Direct Current (HVDC) also became commercially connected to the AC grid for the first time by ABB in Gotland (1954) [8]. HVDC transmission offers more controllability, flexibility and the ability to transmit power over theoretically very long distances [9]. This is a major reason why HVDC technology is continuing to develop today.

HVDC technologies vary based on the types of transistors being used. Line Commutated Converter (LCC) HVDC uses thyristors and Voltage Source Converter (VSC) HVDC uses Inter Gate Bipolar Transistor (IGBT) [10]. For state of the art purposes, HVDC technology is delivered in a modular form of IGBT, also known as Modular Multilevel Converter (MMC) HVDC. MMC HVDC has become an interesting technology because of its advantageous capabilities:

1. MMC HVDC does not need a large AC filter to filter the harmonic components which
are present in the output voltage and current. This is where it differs from the two and three level VSC HVDC[2].

2. With a high number of levels the switching frequency of individual semiconductors can be reduced. Since each switching event creates losses in the semiconductors, converter losses can be effectively reduced[11].

3. MMC HVDC offers high modularity, scalability to meet any voltage level and efficiency which is of importance to high voltage and power applications. Furthermore, it also does not require a DC link capacitor [1].

4. MMC HVDC is based on the Voltage Source Converter (VSC) HVDC which offers enhanced controllability that is able to separately manage active and reactive power. The part which differ from LCC technology is the modulation and the firing technique for the IGBTs [12].

There are many existing and upcoming MMC HVDC projects. The Trans Bay Cable Project[11], for instance, connects Pittsburgh to San Francisco using MMC HVDC which contains more than 200 submodules in each arm [13]. France and Spain will be connected with MMC HVDC in INELFE project[13]. Many publications and research reports have recently been published for MMC HVDC. Most of the studies that refer to MMC HVDC focus on modeling and control both during normal and faulted conditions.

The time domain simulation of MMC HVDC is not a straight forward task given the very large number of submodules. It takes a massive amount of time to simulate every active component within every submodule in detail. Recently, many researchers have been able to find alternative efficient methods using equivalent models to simulate MMC HVDC transmission. One method is known as the efficient modeling approach, which is able to significantly reducing the simulation time duration[3]. This efficient model of MMC HVDC is capable of simulating MMC HVDC in reasonable even faster simulation time for Electro Magnetic Transient (EMT) type studies, both during AC and DC faults.

Using the efficient model of MMC HVDC, the simulation of the MMC HVDC is easier. One of the recently conducted studies concerns the unbalanced fault behavior of MMC HVDC. Some improvements could be made to manage the unbalanced fault with the addition of Negative Sequence Current Control (NSCC) to MMC HVDC control systems. Many Transmission System Operators (TSO) that are working on the grid code proposal mention the need to implement NSCC. The grid code mentions that the HVDC converter should be capable to withstand without tripping an unbalanced fault[4]. Thus, it is important to investigate the NSCC effects in relation to unbalanced fault in MMC HVDC interconnection that might be related to the future or existing grid code.

1-2 Research Objectives

This thesis focuses on the Negative Sequence Current Control (NSCC) implementations in the MMC HVDC for improving the behavior of MMC HVDC during unbalanced fault conditions. The efficient model of MMC HVDC [3] was used to reduce the simulation time duration
without decreasing the overall performance and the accuracy [3],[6]. The simulations were executed using the Power Systems Computer Aided Design (PSCAD)/EMTDC [14].

The main objective of this thesis is to implement NSCC and to analyse the unbalanced fault response of the MMC HVDC system as well as its effect on the power system’s unbalanced fault response. The implementation of NSCC on MMC HVDC is delivered in several schemes and case studies, such as: 1. The suppression of negative sequence current and 2. Several other negative sequence current injection scenarios.

After implementing NSCC in MMC HVDC, another objective was to test its effect for the point to point HVDC interconnection, 3 terminal Multi Terminal DC (MTDC) and connection between the point to point MMC HVDC into 9 bus AC grids. Later, an analysis was performed and discussion were carried out within the scope of the power system dynamic responses to asymmetrical AC faults on the AC and DC sides.

1-3 Research Approach

The methodologies used in the approach to the research project were:

1. Literature review. Conducted a literature review using international journals, trans-
action proceedings, and related websites. The topics concerned MMC HVDC control and simulation, NSCC, power system and dynamic analysis.

2. Modeling of MMC HVDC. The main work involved modifying the MMC HVDC model and implementing the NSCC. An efficient model approach as referred to [3] was used in PSCAD. Control system tuning and parameter matching were performed, which proved to be the most time consuming part and required massive numbers of simulations. The modified model was then applied to different case studies: Point to point MMC HVDC; 3 terminal MMC MTDC; point to point MMC HVDC connected to AC 9 bus system.

3. Analysis. Based on the simulation results, a thorough analysis was performed which was then validated against the theory and supported with references.

4. Conclusion. The final conclusions of the thesis were drawn based on the simulated cases and the hypothesis.

1-4 Hypothesis

The main hypothesis of the work is: MMC HVDC systems, when they utilize adequate control loops in the positive and negative sequence, are capable of riding through unbalanced faults while at the same time improving the impact on both the HVDC system and the connected AC system.

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1-5 Thesis Contributions

This thesis delivers a study of Negative Sequence Current Control (NSCC) on MMC HVDC using the efficient model. Negative sequence current control management has been implemented in the efficient model of MMC HVDC. The suppression and injection schemes of NSCC have been simulated and analyzed in case by case scenarios.

NSCC effects on the point to point MMC HVDC, 3 Terminal MTDC and expanded AC grid networks have also been examined and discussed. These discussions could form a starting point for specifying MMC HVDC requirements of NSCC in the future grid codes.

1-6 Thesis Outline

This thesis report is organized as follows. The introduction gives a brief explanation of the thesis and is delivered in this first chapter. The basic theories and technologies of MMC HVDC are explained in Chapter 2. Chapter 3 introduces the normal operations of the point to point MMC HVDC interconnection. Chapter 4 explains the analysis of NSCC in single line to ground fault in the point to point MMC HVDC. An insight into the NSCC effects in 3 terminal MMC MTDC is discussed in Chapter 5. Chapter 6 shows NSCC effects in larger AC test system which contains several buses. Finally Chapter 7 discusses the general conclusions and provides further recommendations for the thesis.

***
Chapter 2

The Efficient Model of MMC HVDC with Negative Sequence Current Control (NSCC)

This chapter discusses some basic theories required for this thesis. A basic explanation of HVDC technology and MMC HVDC model used in this thesis are also provided here. Section 2-1 provides basic knowledge of MMC HVDC. References are given for the interested reader. Several modeling approaches of MMC HVDC including the efficient model used in this thesis are reviewed in Section 2-2. Negative Sequence Current Control (NSCC) cases are used to control the negative sequence components in the Double Synchronous Reference Frame (DSRF) which are proposed in Section 2-3.

2-1 MMC HVDC Technology

After a long and successful history of Flexible AC Transmission Systems (FACTS) and Line Commutated Converter (LCC) HVDC technology which uses thyristor based switches, new technologies in high voltage power electronic components are emerging and developing rapidly. High voltages Inter Gate Bipolar Transistor (IGBT) are used in VSC HVDC [9][10]. They offer a higher flexibility of the control system to perform active and reactive power management. To optimize performances and gain more benefits of power electronic systems, the VSC HVDC level is increased towards more than two or three levels, which are known as Modular Multilevel Converter (MMC) HVDC [11]. Another publication mentions it as VSC MMC HVDC [15]. The basic control system of MMC HVDC is similar to the two and three level VSC HVDC. They operate as voltage sources. However, MMC HVDC uses higher numbers of voltage levels with IGBT switches. They are stacked in modular form improving the converter’s AC waveform. This configuration gives many advantages compared to the two or three level VSC HVDC.
2-1-1 Topology of MMC HVDC

The topology of one terminal MMC HVDC is depicted in Figure 2-1. Every single MMC converter consists of three phase units. Phase units are also being introduced as legs. Every leg or phase unit contains 2 multivalves, which are separated into the upper and lower part. Multivalves are also being introduced as arms. In every arm, arm inductance ($L_{arm}$) and $n$ number of Submodule (SM) exist[2][3][12]. The terms legs and arms are used in this thesis.

![Figure 2-1: Typical three phase half bridge MMC HVDC circuit diagram](image)

Every MMC converter contains 3 legs, 6 arms and ($6 \times n$) number of SMs, with $n$ is the number of SM in each arm [2].

![Figure 2-2: Element of a single half bridge submodule in MMC HVDC](image)

One SM of MMC HVDC is depicted in Figure 2-2. Configured as half bridge, it contains a combination of 2 IGBTs (T1 and T2) with 2 reversing diodes D1 and D2. These IGBTs are
also connected with a paralleled capacitor C [2]. These IGBTs and reversing diodes can be represented as controllable switches. These switches receive pulse signals from Phase-Shifted Carrier PWM (PS-PWM) and control the capacitor voltage $V_C$ [1], which is an element of leveled voltage in MMC. The total DC voltage ($V_{dc}$) are added up from the sum of all SM voltages. Every SM has a role to form every step of sinusoidal AC waveform in the AC side of MMC system. This is the reason why MMC HVDC with a sufficient number of levels does not require a harmonic filter. However, it depends on the number of levels used in a single MMC system. The harmonic filter is still required in a low level MMC HVDC.

To understand the principles and operation of the single half bridge in a SM, the current direction and the switching state are presented. There are four states to describe the operation modes of SM in MMC. The first two are the ON states, and the following two are the OFF states. In the ON state, which is depicted in Figure 2-3, the objective is to build the $V_{SM}$ voltage equal to $V_C$. The upper combinations of the IGBT and diode are active. When $I_{SM}$ is positive, the current flows through D1 and the capacitor is charged. When $I_{SM}$ is negative, the current flows through T1 and in this way the capacitor is being discharged.

![Figure 2-3: ON state of a submodule in the MMC HVDC](image)

In the OFF states, as depicted in Figure 2-4, the lower combination of the transistor T2 and the diode D2 are active. The current flows through the conducting IGBT or diode. When $I_{SM}$ is positive, the current flows through T2. When $I_{SM}$ is negative, the current flows through the diode D2 as a freewheeling diode. In this state, $V_C$ keeps its value as $V_C$ but $V_{SM}$ is zero[2]. In summary, the review of voltage states is written in Table 2-1.

![Figure 2-4: OFF state of a submodule in the MMC HVDC](image)
**Table 2-1:** State table of a submodule

<table>
<thead>
<tr>
<th>State</th>
<th>T1</th>
<th>D1</th>
<th>T2</th>
<th>D2</th>
<th>VS/M</th>
</tr>
</thead>
<tbody>
<tr>
<td>ON</td>
<td>-</td>
<td>on</td>
<td>-</td>
<td>-</td>
<td>Vc</td>
</tr>
<tr>
<td>ON</td>
<td>on</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>Vc</td>
</tr>
<tr>
<td>OFF</td>
<td>-</td>
<td>-</td>
<td>on</td>
<td>-</td>
<td>0</td>
</tr>
<tr>
<td>OFF</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>on</td>
<td>0</td>
</tr>
</tbody>
</table>

2-1-2 The Basic Control System of MMC HVDC

The control system of the MMC HVDC transmission is similar to the two or three level VSC HVDC with several addition [1]. They all use a cascaded control structure with an upper level control which includes inner control and outer control. With plenty numbers of submodules in MMC, it has a lower level control which controls firing pulses of every submodule with a suitable modulation scheme. The MMC HVDC has a more sophisticated modulation strategy compared to the two and three level VSC HVDC. It consists of many frequency carriers and firing pulses which controls every level of submodules in MMC HVDC. More details about the modulation techniques can be found in [1][16].

The control structure of MMC HVDC is illustrated in Figure 2-5.

The measured active power (P), reactive power(Q), AC voltage (V), AC current(I) and direct voltage (Vdc) are used as inputs by the upper controller. It consists of outer and inner current control. The upper controller brings the outputs to be directly used as the inputs to the lower control. The lower control is mainly used to drive the converter, which is the MMC HVDC itself. In the lower control of MMC HVDC, the reference voltages to generate AC waveform is used as a component to activate the firing pulses. The Pulse Width Modulation (PWM) which contains multiple frequency carriers is commonly used for MMC. There are many PWM techniques for utilizing MMC, one of them is the Phase-Shifted Carrier PWM (PS-PWM) which is used in this thesis.

The complete block diagram of the outer and inner control loops are shown in Figure 2-6. The
control is based on a voltage vector oriented direct and quadrature (dq) control. It consists of setpoints to control MMC HVDC in the direct and the quadrature axis. The direct axis of the outer control can be selected either to control the DC voltage or the active power. Both the DC voltage and the active power control use Proportional-Integral (PI) controllers to set the parameters to their referenced value. The tuning of the PI controller uses recursive trial and error method until it reaches the stable condition. The active power control uses rate limiter block so that the rate of change of active power can be managed not to be very fast. This is a degree of freedom which is chosen based on each system needs.

The quadrature axis of the upper control can be selected either to control the AC voltage or the reactive power control. The AC voltage control loop contains an AC voltage droop block which is a proportional controller with constant k AC droop. This AC voltage droop configuration manages the AC voltage control method with reactive power compensation.

The direct axis of the outer controller yields $i_d^{(ref)}$ signal and the quadrature axis of the outer controller yields $i_q^{(ref)}$ signal. The subscript $^+$ stands for the positive sequence control loop. These signals are further processed in the inner control as reference values. Other input signals of the inner controller are measured by transforming voltage and current into dq-axis using Park transformation [17]. The transformation angle is obtained from the Phase Locked Loop (PLL) extraction block. Signals in dq-axis offer more controllability because dq signals appear in DC form. Hence, the signals are easily controlled by the dq control loops. PI controllers are able to handle dq signal to control active and reactive power.

The output of this inner controller is the inner voltage behind the phase reactor of the converter, which is already transformed into the three phase abc frame. Finally, this output voltage is a reference signal $e_{abc}$ which is going to be used for PS-PWM input signal.

### 2-1-3 Circulating Current Suppression Controller (CCSC)

One of the problems associated with the MMC is the circulating currents in the legs of the converter, as illustrated in Figure 2-7.

The circulating current in the MMC HVDC appears between the arms of the converter. It appears because of voltage difference between the legs of the submodules in the DC side and AC side [18]. It also appears because of voltage differences between the top and the bottom arms. The circulating current of an HVDC converter can be mathematically expressed in

$$i_{diff_k} = \frac{i_{k-up} + i_{k-low}}{2}, k = a, b, c.$$  \hspace{1cm} (2-1)

where $i_{diff_k}$ is the circulating current of phase-$k$ in MMC HVDC. $i_{k-up}$ and $i_{k-low}$ are upper and lower leg currents in each phase of $k$. This circulating current can be suppressed with cross direct-quadrature axis control scheme as can seen in Figure 2-8. The circulating current $i_{diff_k}$ is then transformed into the dq reference frame with the Park transformation [17], but with the phase sequence of $acb$ instead of $abc$. The circulating current appears with a $2\omega$ frequency, thus, the transformation angle is set to have a doubled value from the base frequency. The references of direct and quadrature circulating current are set to zero to suppress the circulating current in the dq reference frame. Finally, the transformed dq circulating current...
is returned with inverse Park transformation resulting in a CCSC reference voltage. To suppress the circulating current, this CCSC reference voltage is added to the reference voltage that come from the output of inner current control before used as an input in PS-PWM.

The MMC HVDC gives rise to circulating currents which appear at $2\omega$ frequency and more apparent during unbalanced fault. Further information and technique of CCSC can be found in [1][18][19][20].

2-2 MMC HVDC Modeling

Modeling of the MMC HVDC is definitely required in every proposal of HVDC project. It is not as simple as standard two and three level VSC HVDC. It faces many challenges because MMC HVDC contains thousands of submodules as mentioned in Chapter 1. With normal traditional simulation model and tools for a detailed EMT model, a single simulation will cost hours or even a day. In the next section, the modeling approaches which offer solutions to that unbearable simulation time is discussed.

2-2-1 Traditional Detailed Model for MMC HVDC

The Traditional Detailed Model (TDM) [6] is also known as full Physics-Based Model[12] or Detailed IGBT Based Model [21]. An illustration of the detailed models is depicted in

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Figure 2-7: Circulating current in MMC HVDC

Figure 2-8: Circulating Current Suppression Controller (CCSC) block diagram

Figure 2-9 [3]. TDM consists of actual active electronic components as can be seen in the left part of the figure. Every SM contains 2 sets of IGBTs, diodes and a capacitor as their actual components. Every active component has its dynamic characteristic. This model is not built with an equivalent circuit. Also, no approaches for lowering admittance matrix used for simulation. The simulation is built just as the physical components, without replacing the components with an equivalent circuit. This model has the drawback of a very long duration of simulation time and very high computational burden.

2-2-2 Efficient Model for MMC HVDC

To reduce the simulation time for MMC HVDC, active components are replaced by passive components in the efficient model [3]. This model is also called as Detailed Equivalent Model (DEM) in [6]. The efficient model consists of 2 computational reduction methods. The methods have goals for minimizing the duration of simulation time:

1. **Nested Fast and Simultaneous Solutions (NFSS)**. This method allows a single network parted into small subnetworks as illustrated in Figure 2-10. The computational system is clustered into subnetworks as expressed in Equation (2-2).

   \[
   \begin{pmatrix}
   Y_{11} & Y_{12} \\
   Y_{21} & Y_{22}
   \end{pmatrix}
   \begin{pmatrix}
   V_1 \\
   V_2
   \end{pmatrix}
   =
   \begin{pmatrix}
   J_1 \\
   J_2
   \end{pmatrix}
   \]  

   (2-2)
The Efficient Model of MMC HVDC with Negative Sequence Current Control (NSCC)

This method increases the number of simulation steps, but makes the size of the admittance matrices smaller. The main burden of simulation is the inverse operation of admittance matrix. The higher levels of MMC HVDC yields to the bigger order of admittance matrix, which increases the computational load. This is the reason why the order of the admittance matrix should be separated into smaller subnetworks.

2. Thevenin-Norton equivalent approaches. In this method, every submodule is simplified by a Thevenin or Norton equivalent. Basically, IGBT with reverse diode has a function to switch on and switch off the submodule using the gate signal. In the efficient model, these IGBT and reverse diode can be replaced with a variable controlled resistor. On state will return a resistor value of 0.001 Ohms, and off state will return a resistor value of 1 MOhms. This illustration is depicted in the center part of Figure 2-9. After replacing each element in a submodule, every multivalve is replaced into an MMC equivalence as depicted in the right part of Figure 2-9.

The capacitor current is given in Equation (2-3). The voltage capacitor can be expressed as (2-4) using the trapezoidal method to represent capacitor as an equivalent voltage source and resistor.

\[ I_c(t) = C \frac{dV_c(t)}{dt} \]  \hspace{1cm} (2-3)

\[ V_c(t) = R_e I_e(t) + V_{eq}(t - \Delta t). \]  \hspace{1cm} (2-4)
The terminal voltage of an individual submodule $I_{SM}$ can be determined as a function of its current (2-5, 2-6, 2-7).

\begin{equation}
V_{EQ(t)} = R_{eqv(t)}I_{PM(t)} + V_{eqv(t - \Delta t)}.
\end{equation}

\begin{equation}
R_{eqv(t)} = \sum_{i=1}^{n} \left[ R_2 \left(1 - \frac{R_2}{R_1 + R_2 + R_C} \right) \right].
\end{equation}

\begin{equation}
V_{eqv(t-\Delta t)} = \sum_{i=1}^{n} \frac{R_2}{R_1 + R_2 + R_C} V_{Ceq}(t - \Delta t).
\end{equation}

A comparison of the simulation time durations and errors between both models is given in Table 2-2 [6].

The table shows an observed simulation time improvement with the higher MMC level. This thesis makes explicit use of the efficient model which recently becomes available from PSCAD [14] in 2015. Several modifications of upper and lower controller have been done in order to retrieve the required model of NSCC.
2-3 MMC HVDC with Double Synchronous Reference Frame (DSRF) Control Systems

The Negative Sequence Current Control (NSCC) implemented in a power converter is required to reduce the unwanted effects in the grid when asymmetrical faults or unbalanced conditions occur. NSCC in a voltage source converter device could manage three phase balanced or unbalanced currents during asymmetrical faulted voltages, depending on the offered strategy. On the voltage source converters, the unwanted conditions appear when asymmetrical fault occurs. The anomaly is mainly the appearance of ripples in HVDC link voltage, active and reactive power. These ripples result in high stressed disadvantageous system performance, increasing the risks of power converter tripping.

In that prospect, NSCC offers flexibility to control the unbalanced short circuit current using controllable positive and negative sequence which is done simultaneously [22]. The main contribution of the positive and the negative sequence separation are to reduce the oscillatory active power and to fully utilize the converter limits for grid reactive current support active and reactive power injection [23]. The positive and negative sequence components are controlled to achieve different goals, namely:

1. Minimization of the ripple in DC Voltage due to unbalance AC faults [23].
2. Reduction of the oscillation or drop of active and reactive power [23].
3. Improvement of the post fault behavior at Point of Common Coupling (PCC) of MMC HVDC [5].
4. Offers a solution to grid code requirement of a converter station that must support the grid voltage under faults with reactive current injection [4][20].

The implementation of NSCC is performed using a Double Synchronous Reference Frame (DSRF) which is the most intuitive way to control a current vector which consists of positive and negative sequence components [24]. It is a current controller based on two synchronous reference frames, rotating at the fundamental grid frequency in the positive and negative directions respectively [24]. Easily, DSRF is a flexible control system to manage the positive and negative sequence separately.

In the conventional model of MMC HVDC, the control system works only with the positive sequence. The reason is that the model is built for use in symmetrical conditions where negative sequence components do not appear. In addition, since \(\Delta - Y/\)grounded transformer exists, no zero sequence current components appears in the grid. In this thesis, the PSCAD’s MMC HVDC efficient model has been modified. The modified control diagram uses a DSRF controller which is depicted in Figure 2-11. In the inner current control loop, the three phase voltages and currents from converter transformed into dq reference frame with Park transformation[17] with positive PLL angle.

For the negative sequence extraction, the three phase voltage and current are transformed with Park transformation, with the angle of negative PLL. In the negative SRF, three phase voltages are transformed into \(v_d^-\) and \(v_q^-\) with the negative sequence extraction. \(v_d\) and \(v_q\) are direct and quadrature voltage, respectively. Superscript \((-)\) shows a negative sequence.
Figure 2-11: Inner current control of Double Synchronous Reference Frame (DSRF). DSRF is consists of positive and negative Synchronous Reference Frame (SRF). This configuration allows control of negative sequence components.

Component. Three phase current also transformed into $i_d^-$ and $i_q^-$. Transforming three phase voltage and currents with the negative PLL angle will make direct and quadrature voltages and current components appearances of oscillating waveform with $2\omega$ frequency [24]. This oscillation should be damped out in order to proceed the signal into PI-controller negative SRF and apply NSCC scheme, otherwise, PI controllers cannot handle it. A Notch Filter (NF) is used to eliminate $2\omega$ frequency [22]. It is used in every direct and quadrature voltage and currents. NF is a band stop filter which is tuned in a very narrow frequency cutoff.

Figure 2-12 shows an unfiltered and filtered negative sequence current $i_d^-$. Unfiltered negative sequence current $i_d^- (idneg)$ is plotted with the blue color, and filtered $i_d^- (idnegnf)$ is plotted with red color. The NF is tuned at double frequency of $2\omega$. This will block only the frequency of 120Hz. Special case needs to be taken in the design of NF. It can be seen that $i_d^- nf$ which is a filtered result of $i_d^- (idneg)$ comes to zero after a while. In the beginning of the plot, at $t=0.8-0.9s$, $i_d^- (idnegnf)$ has not reached zero value and forms a dynamic response due to the response time of NF. In this thesis, the filtered negative sequence dq current is used for discussion.

These $i_d^-$, $i_q^-$, $v_d^-$ and $v_q^-$ are then processed with the same structure used for positive inner current control. PI controllers are used, similar to positive synchronous reference frame as depicted in Figure 2-11. The dq-frame output of negative sequence inner current control is transformed into three phases abc frame. Finally, positive sequence reference waveform $e_{abc}^+$ is added to the negative sequence reference waveform $e_{abc}^-$. The addition of positive and negative
sequence of the inner current controller is a reference voltage input for the PS-PWM. The method of controlling positive and negative sequence currents first appeared in [22] and is commonly used in power AC/DC converters. Other techniques like Proportional-Resonant and Proportional-Integral-Resonant techniques are available in the literature [20][24][25]. In this work, only the negative sequence control strategy using DSRF which is shown in Figure 2-11 is implemented.

***
Chapter 3

The Normal Operation of the Point to Point MMC HVDC Link

This chapter delivers simulation results about the normal operation of a point to point MMC HVDC system using the efficient model [3] in Figure 3-1. The efficient model [3] from PSCAD [14] is used with modified control systems, configurations and parameters. This chapter mainly discusses energization events, such as the closure of the MMC’s internal breaker and deblocking of MMC HVDC controller. Furthermore, a Circulating Current Suppression Controller (CCSC) and a Negative Sequence Current Control (NSCC) activation are also discussed.

3-1 System Configuration of the Point to Point MMC HVDC

The test system for the point to point MMC HVDC consists of 2 MMC HVDCs which are identical in the rating. The test system of 2 Terminals MMC HVDC is depicted in Figure 3-1.

![Figure 3-1: 2 Terminal MMC HVDC test system](image)

It consists of two identical 115-levels MMC HVDC which are connected with a 400 km DC overhead line. For this case study, each HVDC terminal has a power of 1000 MVA, occupying ±320 KV DC direct voltage with 370 KV AC voltage at the grid. Both of MMC HVDC
Table 3-1: Point to point MMC HVDC system parameters

<table>
<thead>
<tr>
<th>No</th>
<th>Item</th>
<th>Terminal 1</th>
<th>Terminal 2</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>Rated MVA, base frequency</td>
<td>1000 MVA, 60 Hz</td>
<td></td>
</tr>
<tr>
<td>2</td>
<td>Type of HVDC</td>
<td>MMC HVDC 115 levels</td>
<td></td>
</tr>
<tr>
<td>3</td>
<td>Voltage level (pole-pole)</td>
<td>± 320 KV DC; 370 KV AC</td>
<td></td>
</tr>
<tr>
<td>4</td>
<td>Direct control</td>
<td>Vdc control 640 KV P control 800 MW</td>
<td></td>
</tr>
<tr>
<td>5</td>
<td>Reactive power control</td>
<td>Vac control 1pu</td>
<td></td>
</tr>
<tr>
<td>6</td>
<td>Arm inductances</td>
<td>50 mH</td>
<td></td>
</tr>
<tr>
<td>7</td>
<td>Cell DC capacitor</td>
<td>2800 uF</td>
<td></td>
</tr>
<tr>
<td>8</td>
<td>Interfacing transformer</td>
<td>230 Yg / 370 Δ</td>
<td></td>
</tr>
<tr>
<td>9</td>
<td>Transformers leakage reactance</td>
<td>0.2 pu</td>
<td></td>
</tr>
<tr>
<td>10</td>
<td>Load inductances</td>
<td>40 mH</td>
<td></td>
</tr>
<tr>
<td>11</td>
<td>X/R</td>
<td>20</td>
<td></td>
</tr>
<tr>
<td>12</td>
<td>SCR</td>
<td>2.5</td>
<td></td>
</tr>
</tbody>
</table>

are configured to control the AC Voltage for quadrature axis reactive power control, which is referenced to rated AC voltages, 370 KV. A conventional HVDC link has one terminal configured as DC Voltage (Vdc) control, and the second terminal is configured in active power (P) control. In this test system, terminal 1 is configured as Vdc control and terminal 2 is configured as P control.

MMC HVDC connected with a smoothing reactor. A Δ- Y/grounded transformer is then connected to each MMC HVDC’s reactor in order to step the voltage down to 230 KV. A voltage source is connected in each end of the terminal.

The system parameters are given in Table 3-1.

3-1-1 Energization of the Point to Point MMC HVDC Link

The operation of the MMC HVDC link starts with its energization steps of which processes can be seen in Table 3-2. The simulation starts from zero condition when all of AC voltage sources have values from totally zero at t = 0 second. The same condition holds for the DC circuit. Gradually, AC voltage sources in each terminal increases and reaches its rated voltage of 230 KV at t=0.06s. Voltage sources are transformed into higher voltage rating of 370 KV and reach every internal circuit breaker which is located between reactor and transformer in each terminal. At t=0.1 seconds, the internal breaker of terminal 1 is closed and the voltage energizes the power electronic components in terminal 1. The closing of internal breakers is shown by an instant increase of $P_1$ and $Q_1$, which immediately go back to its initial value. This event is known as an overshoot. It is shown with an arrow at t=0.1s in Figure 3-2.

Figure 3-2 shows plots of active and reactive power at both terminals during energization and interconnection process.

After the power electronics in the terminal 1 are energized, the next step is to activate the direct voltage control system of terminal 1. The activation is done by turning on the control system which contains the Proportional - Integral (PI) controller. After the deblocking signal is turned on, every PI controller in outer and inner controller becomes active and they start
Table 3-2: Energization of the Point to Point MMC HVDC link

<table>
<thead>
<tr>
<th>Time</th>
<th>Event</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>Simulation starts and CCSC is activated</td>
</tr>
<tr>
<td>0.1s</td>
<td>Internal Breaker of terminal 1 is closed</td>
</tr>
<tr>
<td>0.3s</td>
<td>Deblocking of terminal 1 control system</td>
</tr>
<tr>
<td>0.5s</td>
<td>Internal Breaker of terminal 2 is closed</td>
</tr>
<tr>
<td>0.6s</td>
<td>Deblocking of terminal 2 control system</td>
</tr>
<tr>
<td>0.8s</td>
<td>NSCC is activated</td>
</tr>
</tbody>
</table>

Figure 3-2: P [MW] and Q [MVAR] plots of point to point MMC HVDC energization process

operating to control the parameters. The control systems of terminal 1 MMC HVDC are deblocked at t=0.3s.

It is also shown with an arrow in Figure 3-2 that terminal 1 needs a big instantaneous active power to energize the control systems for the first time and brings DC voltage to its normal operating point.

Figure 3-3 shows DC voltage plots at both terminals. When the deblocking process of terminal 1 occurs, at t=0.3s, \( V_{dc1} \) starts increasing. PI controller helps the DC voltage to reach the reference value of ±320 KV, which is measured as 640 KV pole to pole. DC voltage rises from zero to the reference value of 640 KV for about 100 ms. The rising of DC voltage shows the HVDC link between terminal 1 and 2 is energized directly. This happens because no DC circuit breaker is being modeled in this test system.

At terminal 2, the DC voltage during t=0.3-0.5s shows different forms compared to terminal 1. \( V_{dc1} \) is not rippled, however \( V_{dc2} \) suffers from a ripple. It shows that 400km DC transmission line model is causing the DC voltage to oscillate. This happens because the internal breaker of terminal 2 has not closed yet, thus, the condition at terminal 2 is an open conductor. Terminal 1 does not show similar oscillation because PI control of terminal 1 is already activated and is tuned in a good manner.
At t=0.5s, the internal breaker of terminal 2 is closed. Terminal 1 and terminal 2 are finally connected. 2 terminals MMC HVDC interconnection is established, but the process is not completed yet. Next step is to activate the control system of terminal 2 to control the active power. At t=0.6s, the deblocking scheme of terminal 2 is activated as a P-Control. A similar deblocking response of active power appears. Overshoot happens with $P_2 = \pm 300\text{MW}$. Terminal 1 shows mirrored response which is the same with terminal 2 because terminal 1 is a sender side.

At t=0.6s, the control systems of terminal 2 are deblocked. An overshoot occurs in $P_2$ but it is not as high as $P_1$. This happened because $P_2$ takes the control of active power. Finally, a complete 2 terminal MMC HVDC interconnection is established. Terminal 2 increases its active power into the desired reference value of 800 MW. With the configured rate of change of active power, the active power in terminal 2 reaches its referenced value at t=2s. Slight $Q_1$ and $Q_2$ overshoots occur in every connection of internal breaker and deblocking process.

### 3-1-2 Activation of Negative Sequence Current Control (NSCC)

The NSCC activation requires switching from positive control into positive and negative control, from the positive Synchronous Reference Frame (SRF) into Double Synchronous Reference Frame (DSRF) which contains positive and negative SRF. The diagram can be seen at Figure 2-11 in the previous chapter. Direct and quadrature currents and voltages are switched from unfiltered into filtered signal with Notch Filter (NF) to eliminate $2\omega$ oscillation.

This procedure starts from t=0.8s.

In negative SRF, three phase voltage and current are transformed into negative dq-axis using Park Transformation [17] with a negative transformation angle. The transformation yields an unfiltered negative sequence voltages and currents in dq-axis, which have an oscillating frequency of $2\omega$ in normal condition as discussed earlier in Section 2-3. A notch filtered negative direct and quadrature voltage and current are used to control the negative SRF.

As an effect of switching to DSRF to control the negative sequence components at t=0.8s, $P_1$, $P_2$, $Q_1$ and $Q_2$ showed some small overshoot. After a while, the P and Q values go back to the normal and continue reaching the referenced steady state condition as pictured in Figure 3-4.

For a thorough observation, the positive sequence voltage and current control signal on the terminal 2 is pictured in Figure 3-5. This figure shows the positive sequences of $i_d$, $i_q$, $v_d$ and
$v_q$ plots. It shows that $i_d$ is proportional to $P$, and $i_q$ is proportional to $Q$ of terminal 2. PI controller also works without significant noise. This is a sign that the NSCC is activated and working properly.

Figure 3-4: $P[\text{MW}]$ and $Q[\text{MVAR}]$ plots of point to point MMC HVDC during NSCC activation process. NSCC is activated at $t=0.8s$.

For the comparison, the filtered negative sequence voltage and current in direct and quadrature axis $i_d^-, i_q^-, v_d^-$ and $v_q^-$ are depicted in Figure 3-6. The simulation is done in normal condition without any unbalanced fault. The negative sequence voltage and current show zero value. A small noise occurs due to the response of PI parameter and NF. Many small overshoots occur at the closing of internal breaker and the activation of deblocking signal which immediately return to zero.

Figure 3-5: $i_d, i_q, v_d$ and $v_q$ plots of terminal 2. The figure shows the positive sequence component. At $t=0.8s$ overshoot in $i_d$ shows NSCC is activated.
### 3-1-3 Activation of Circulating Current Suppression Controller (CCSC)

The basic theory of CCSC has been discussed in Section 2-1-3 [1][19][18][20]. CCSC is also implemented in the efficient model of MMC HVDC used in this thesis section. In the simulation, CCSC is activated even at the beginning of the simulation, from \( t=0 \)s. But, to have a deeper understanding about CCSC, in this section, a simulation is set to have CCSC disabled at the beginning of the simulation and activated at \( t=2.4 \)s. Based on the theory, \( i_{\text{diff}-d} \) and \( i_{\text{diff}-q} \), which are Park transformed circulating current, are pictured in Figure 3-7. \( i_{\text{diff}-d} \) and \( i_{\text{diff}-q} \) show rippled values before activation of CCSC. After \( t=2.4 \)s, \( i_{\text{diff}-d} \) and \( i_{\text{diff}-q} \) are suppressed to zero.

![Figure 3-7: Park transformed circulating current in dq frame. CCSC is activated at t=2.4s](image)

The circulating current itself should be suppressed to make MMC HVDC operation more stable. Without CCSC, \( i_{\text{diff}} \) would be disorganized as depicted in Figure 3-8. It can be seen that after CCSC activation, \( i_{\text{diff}} \) immediately goes to certain fixed value.

### Summary of Energization Events

The energization events of 2 terminal MMC HVDC interconnection are already written in Table 3-2. The simulation shows that the process of establishing 2 Terminal MMC HVDC
interconnection could take at least 0.8 seconds to establish the initial operation. It could take 2 seconds to reach the steady state operating point of 2 Terminal MMC HVDC interconnection.

***
Chapter 4

The Effect of Negative Sequence Current Control (NSCC) in the Point to Point MMC HVDC during the Asymmetrical Fault

The normal operation of a point to point MMC HVDC link has been discussed in Section 3-1. In this chapter, an asymmetrical fault is applied at terminal 2 of MMC HVDC interconnection. The asymmetrical fault is a Single Line to Ground (SLG) fault. This chapter discusses the fault effect with and without NSCC strategies. Different NSCC control strategies are discussed with the term of 'Case'. A comparison of several NSCC schemes is discussed case by case. These cases can be configured by setting the references of negative sequence direct axis current \( (i_{d(\text{ref})}) \) and negative sequence quadrature axis current \( (i_{q(\text{ref})}) \). In this thesis four control strategies are simulated as can be seen in Table 4-1.

In Table 4-1 all of simulated scenarios are given in the first left column. A scenario without NSCC scheme is named as NO NSC scenario. NO NSC has a control system which consists of only positive sequence control without negative sequence current and voltage extraction in Double Synchronous Reference Frame (DSRF). All of the scenarios, named Case 0 to Case 4, are NSCC schemes which configured as either suppression or injection of NSCC.

<table>
<thead>
<tr>
<th>Scenario Name</th>
<th>NSCC type</th>
<th>( i_{d(\text{ref})} )</th>
<th>( i_{q(\text{ref})} )</th>
</tr>
</thead>
<tbody>
<tr>
<td>NO NSC</td>
<td>n/a</td>
<td>n/a</td>
<td>n/a</td>
</tr>
<tr>
<td>Case 0</td>
<td>Suppression</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>Case 1</td>
<td>Injection</td>
<td>2 ( \omega ) damping equation of P</td>
<td>0</td>
</tr>
<tr>
<td>Case 2</td>
<td>Injection</td>
<td>k * V-</td>
<td>0</td>
</tr>
<tr>
<td>Case 3</td>
<td>Injection</td>
<td>0</td>
<td>k * V-</td>
</tr>
</tbody>
</table>
In Case 0, NSCC is being suppressed. It means that negative sequence current is forced to zero. This configuration is reached by setting $i_{d}^{(-)}(\text{ref})$ and $i_{q}^{(-)}(\text{ref})$ to zero in the negative Synchronous Reference Frame (SRF). Case 0 is being discussed in recent grid code, about the ability of HVDC stations to be able to withstand negative current during a fault [4]. It says "any constituent Power Park Unit thereof will be required to withstand, without tripping, the negative phase sequence loading incurred by clearance of a close-up phase-to-phase fault, by System Back-Up Protection on the Onshore Transmission System operating at Supergrid Voltage". It is obvious that the grid code requires the HVDC module to be able to be in operation during an asymmetrical fault. The NSCC suppression strategy (Case 0) is required to fulfill that requirement. Case 0 is discussed in Section 4-1-2.

Beside the suppression, another type of NSCC is the injection of negative sequence current. Case 1, 2, 3 are negative sequence current injection cases. This injection of negative sequence current result to many different effects, one of the effect is to reduce the power ripples which appear in faulted terminal. This is obtained by setting $i_{d}^{(-)}(\text{ref})$ and $i_{q}^{(-)}(\text{ref})$ with power ripple damping equation [23]. Another configuration which also will be discussed is an injection of $i_{d}^{(-)}(\text{ref})$ and $i_{q}^{(-)}(\text{ref})$ with a proportional value to the negative sequence voltage. The proportion is denoted by constant ‘k’.

With the different configuration of injections in direct or quadrature axis, the cases are categorized into Case 2 and 3. Case 2 is an injection only in the direct negative sequence current reference $i_{d}^{(-)}(\text{ref})$, with the negative quadrature part $i_{q}^{(-)}(\text{ref})$ is set to zero. Case 3 is the injection of negative sequence voltage in the negative sequence quadrature reference $i_{q}^{(-)}(\text{ref})$, but $i_{d}^{(-)}(\text{ref})$ is set to zero. These cases are going to be discussed in Section 4-1-3.

### 4-1 NSCC Strategies in the Point to Point MMC HVDC during Asymmetrical Fault

#### 4-1-1 SLG Fault without NSCC (NO NSC)

The system diagram of the point to point MMC HVDC which is used in this section can be seen in Figure 4-1. An SLG fault is applied at the AC side of 2 terminal MMC HVDC. The fault is applied at the inverter side of receiver terminal-2. The fault is applied after the system reaches the normal steady state condition of 230 kV rms after $t > 2s$. In the simulation, 2 terminal MMC HVDC system reaches its steady state condition with active power $P = 800$ MW and DC voltages $V_{dc} = 640$ kV at approximately $t = 2s$. The SLG fault is applied at $t$
= 3 s for a duration of 250 ms. The fault is applied at terminal 2 to ensure that the system is stable for the analysis.

![Diagram](image_url)

**Figure 4-2:** Vdc, P and Q plots at terminal 1 and 2 MMC HVDC. SLG fault is applied at terminal 2.

### DC Side Condition at Terminal 2

The plots of DC voltage, active and reactive power are pictured in Figure 4-2. The first column on the left shows plots of Vdc, P and Q at terminal 1. Another column on the right shows terminal 2’s. Terminal 1 is a DC Voltage controller. It controls the DC voltage using the PI controller in the outer control loop. At the steady state condition before fault applies at t=3s, the DC voltage in terminal 1 (Vdc1) is stable at Vdc reference value of 640 kV, which is denoted in red dashed line. Vdc2 voltage slightly has a value lower than 640 kV because of the HVDC interconnection is connected with 400 km DC overhead line. Therefore, a slight loss at terminal 2 occurs, leaves Vdc2 stable at 625kV, with approximately 15kV voltage drop.

In the remote terminal, the active power of MMC HVDC is controlled by P control of terminal 2. The reference power is assigned as -800 MW using the PI controller in the outer control loop. Note that the minus sign shows that the active power flows from the DC side to the AC side in terminal 2. In the steady state condition before t=3s, terminal 2 active power is stable at P2 = -800 MW. A loss can be seen in terminal 2 because terminal 1 sends the active power slightly higher, at approximately P1 = 820 MW. An excess of 20 MW occurs at terminal 1.
As SLG fault is applied at \( t = 3s \), the DC side of terminal 2 is disturbed. The DC voltage, active and reactive power responses are observed. Both terminal 1 and terminal 2 suffer from changing magnitude. \( V_{dc} \) rises slightly for approximately 15 kV. \( P_1 \) and \( P_2 \) are dropped from 800 MW to approximately 550 MW. There are also ripples at \( V_{dc} \), \( P \) and \( Q \) of Terminal 2. Those ripples do not exist in terminal 1. This happens due to the long DC transmission lines and the fine tuning of DC voltage control in terminal 1.

The ripples that appear in terminal 2 have a frequency of \( 2\omega_0 \). In the simulation, the base frequency is 60 Hz, thus, the ripples oscillate with a frequency of 120 Hz. This happens as discussed in [24],[23]. A current representation in complex number can be represented in equation 4-1 with the abc frame as:

\[
\vec{I}_p = I_p e^{j\omega t} = I_p [\cos(\omega t) + j \sin(\omega t)]. \tag{4-1}
\]

Subscript p denotes a positive sequence. When an asymmetrical fault occurs, a negative sequence voltage and current appears. The negative sequence current can be expressed by the equation 4-2.

\[
\vec{I}_n = I_n e^{-j\omega t} = I_p [\cos(-\omega t) + j \sin(-\omega t)]. \tag{4-2}
\]

Thus, the instantaneous current representation which contains a positive and negative sequence can be expressed as a sum of instantaneous positive and negative sequence current (4-3).

\[
\vec{I} = I_p e^{j\omega t} + I_n e^{-j\omega t}.
\]

\[
\vec{I} = [I_p + I_n] \cos(\omega t) + j[I_p - I_n] \sin(\omega t). \tag{4-3}
\]

The resultant magnitude of the current positive and negative sequence than can be written as:

\[
I = \sqrt{([I_p + I_n] \cos(\omega t))^2 + ([I_p - I_n] \sin(\omega t))^2}. \tag{4-4}
\]

\[
I = \sqrt{I_p^2 + I_n^2 + 2I_pI_n \cos(2\omega t)}. \tag{4-5}
\]

The Equation 4-5 has a value of \( \cos (2\omega t) \). It indicates the double frequency appearances. Equation (4-5) shows that current magnitude suffers from oscillation with the value of double frequency because of the presence of the negative sequence component when the asymmetrical fault occurs.

**AC Side Condition at Terminal 2**

The plot of the instantaneous three phase AC voltage and current at terminal 2 can be seen in Figure 4-3 and 4-4, respectively. Figure 4-3 shows the voltages on both sides of \( \Delta 320 \text{ kV} \).
Y/grounded 230kV transformer. The fault occurs at $t=3s$ at Y/grounded side, which is also mentioned as grid or generator side. It causes one of the three phase voltage to drops to zero. The RMS voltage, which is plotted with a dashed line, at Y/grounded side of terminal 2 is dropped from rated voltage of 230 kV to a faulted voltage of 200 kV.

The AC current also shows similar behavior at terminal 2. At the grid side, one phase of faulted terminal dropped, and another two phases of currents show rising values. This can be examined in the increasing envelope of non-faulted 2 phases of the current. On the other side, the reactor side of the transformer shows balanced AC current with slightly increasing magnitude.

Another approach to examine the fault behavior in a power system is to observe the symmetrical components of voltage and current. Positive, negative and zero component magnitude can be extracted with function block of PSCAD. Figure 4-5 shows positive, negative and zero voltage at both sides of the transformer in terminal 2. When a fault is applied, the impedance of the network at the faulted point changes and the positive sequence voltage drops to approximately 155 kV. Due to the effect of SLG fault, the negative sequence voltage appears at 120 kV. Zero sequence voltage shows a return vector between the positive and negative sequence.

The symmetrical current components are depicted in Figure 4-6. When the fault occurs, the faulted terminal suffers from over current phenomena. During the SLG fault in the Point of Common Coupling (PCC), the zero and the negative sequence currents appear indicating the unbalance in the current. In a $\Delta$ - Y/grounded transformer, $\Delta$ side of a transformer does...
The Effect of Negative Sequence Current Control (NSCC) in the Point to Point MMC HVDC during the Asymmetrical Fault

not have a return path for the zero current component, thus, zero sequence current is totally blocked to zero value. Only positive and negative sequence current components in the reactor side exist due to the $\Delta$ winding.

To complete the analysis of power system, an approach based on the asymmetrical component is discussed. The phenomena can be illustrated in the equivalent sequence diagram which contains positive, negative and zero sequence components[26]. The positive, negative and zero components of SLG faulted terminal 2 MMC HVDC are depicted in Figure 4-7 in the sequence circuit equivalent diagram.

The first circuit on top shows a positive sequence of terminal 2 DC-AC side. The left side is the MMC HVDC side and the right side is the grid or generator side. The positive sequence of MMC HVDC can be represented with current source $I_{\text{pos MMC}}$. The positive sequence of the generator can be represented with a voltage source $E_{\text{pos grid}}$.

The second and the third circuit shows the negative and the zero sequence circuits. Every positive, negative and zero sequence circuit has its components of impedance. $Z_{\text{HVDC}}$ is the internal impedance of HVDC. $Z_{\text{trafo}}$ is transformer’s reactance, while $Z_{\text{TLine}}$ is a half of AC transmission line’s impedance. $Z_{\text{grid}}$ is the internal impedance of the generator. In a $\Delta$ - Y/grounded configuration of the transformer, zero sequence current is totally blocked[27][26]. This can be represented by the open circuit at MMC $\Delta$ side and a short circuit in Y/grounded side of the transformer in zero sequence circuit.

The SLG fault is applied in the middle of AC transmission line. When an SLG fault occurs, the positive, negative and zero sequence circuits are connected in the fault area, and the current flows through the sequences. In NO NSC case, the negative sequence of MMC side
4-1 NSCC Strategies in the Point to Point MMC HVDC during Asymmetrical Fault

**Figure 4-7**: Positive, negative and zero sequence circuit equivalent diagram at terminal 2 for case without NSCC (NO NSC)

... does not apply additional control, thus, the negative sequence current appears.

**Control System Response of SLG Fault without NSCC**

The plot of voltage and current in the dq positive reference frame is depicted in Figure 4-8. The first two columns show dq voltages and currents in terminal 1. In terminal 1 $i_{d1}$ shows disturbance, which is proportional to $V_{dc1}$, $i_{q1}$, $v_{d1}$ and $v_{q1}$ show the stable behavior.

The last 2 columns show dq voltages and currents at terminal 2, $i_{d2}$ shows dropped oscillating value which is proportional to $P_2$. $i_{q2}$ also shows dropped value, it shows the condition of faulted AC voltage in terminal 2. $v_{d2}$ and $v_{q2}$ shows oscillation of $2 \omega$.

In NO NSC scheme, only the positive reference frame is being used for the control, as showed in Figure 2-5. That means only the positive sequence control is working. However, for the illustration, a negative sequence $i_{d}$ and $i_{q}$ are plotted in Figure 4-9. These $i_{d}$ and $i_{q}$ have been filtered by NF at 120 Hz. Before the fault, $i_{d}$ and $i_{q}$ show zero value with small noise. When the SLG fault occurs, $i_{d}$ and $i_{q}$ are oscillating with a non zero value.

The rest of the simulation results are plotted in the Appendix (A).

**4-1-2 Suppression Scheme of NSCC (Case 0)**

The suppression scheme is obtained by assigning negative sequence current references $i_{d(\text{ref})}$ and $i_{q(\text{ref})}$ to zero. These reference values have been discussed earlier in the Figure 2-11 in

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Chapter 2. The negative sequence references in DSRF can be expressed in Equation 4-6 and 4-7.

\[ i_{d\text{ (ref)}} = 0. \]  \hspace{1cm} (4-6)

\[ i_{q\text{ (ref)}} = 0. \]  \hspace{1cm} (4-7)

The PI controller suppresses \( i_d^- \) and \( i_q^- \) to zero during SLG fault. The zero value of \( i_d^- \) and \( i_q^- \) yields zero negative sequence current. The negative sequence dq-currents during fault are showed in Figure 4-10.

Before the fault applied, \( i_d^- \) and \( i_q^- \) showed zero value in the normal condition obviously because the three phase currents are balanced. Then, at \( t = 3 \) s SLG fault is applied thus unbalanced condition occurs. That makes \( i_d^- \) and \( i_q^- \) suffer from a rising value which oscillates and immediately damped after approximately 700 ms. This overshoot occurs due to the dynamic response of NF. The damping time shows the response of NF to damp 2\( \omega \) oscillation.

The noticeable difference is the negative sequence current component itself. A plot of symmetrical current component is depicted in Figure 4-12. When SLG fault occurs, negative sequence current rises and then immediately suppresses to zero after approximately 700 ms. This is a similar response that appears due to dynamic response of NF. The difference can be seen refer to NO NSC configuration. It is clear that with Case 0 scenario, negative sequence current is suppressed.

The sequence diagram for Case 0 can be seen in Figure 4-13. The negative sequence components of MMC HVDC acts like an open circuit. This shows no negative sequence current flows in the MMC HVDC. It concludes that \( I_{neg}^{MMC} = 0 \).
Damping of Active Power Ripple (Case 1)

References [23][24] show the instantaneous active power associated with active rectifier under unbalanced condition. It can be expressed in Equation 4-8.

$$P_{total} = P_0 + P_{c2} \cos(2\omega t) + P_{s2} \sin(2\omega t). \quad (4-8)$$

Where $P_0$ is the average value of the instantaneous active power associated with the active power. $P_{c2}$ and $P_{s2}$ represent the magnitude of the oscillating terms in the instantaneous active power. Since the DSRF is used to control the negative sequence components, the equation can be adapted to positive and negative sequence voltage and current in direct and quadrature axis. Hence, the amplitude of the active power can be calculated as a matrix in Equation 4-9.

$$\begin{pmatrix} P_0 \\ P_{c2} \\ P_{s2} \end{pmatrix} = \begin{pmatrix} i_d^+ & i_q^+ & i_d^- & i_q^- \\ i_d^+ & i_q^+ & i_d^- & i_q^- \\ i_d^- & i_d^+ & i_q^- & i_q^+ \end{pmatrix} \begin{pmatrix} v_d^+ \\ v_q^+ \\ v_d^- \\ v_q^- \end{pmatrix} \quad (4-9)$$

$v_d^+$ and $v_q^+$ represent direct and quadrature voltage in positive sequence reference frame. $i_d^+$ and $i_q^+$ represent direct and quadrature current in positive sequence reference frame. $v_d^-$, $v_q^-$,
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**Figure 4-11:** Positive sequence direct and quadrature current of NSCC Case 0

**Figure 4-12:** Positive, negative and zero sequence current components of Case 0

\( i_d^+ \) and \( i_q^+ \) calculated by Park transformation [17] rotating at the fundamental frequency of \( \omega \). \( v_d^- \) and \( v_q^- \) are direct and quadrature voltage in negative sequence frame, respectively. \( i_d^- \) and \( i_q^- \) are direct and quadrature current in negative sequence frame. All of negative sequence direct and quadrature voltage and current obtained also by Park transformation rotating at \(-\omega\).

In order to reduce the \( 2\omega \) oscillation in the active power, \( P_{c2} \) and \( P_{s2} \) are replaced with the value of zero (4-10).

\[
\begin{pmatrix}
P_{c2} \\
P_{s2}
\end{pmatrix} = \begin{pmatrix}
0 \\
0
\end{pmatrix}
\] (4-10)

Doing an inverse operation, \( i_d^- \) and \( i_q^- \) value can be expressed in (4-11s). It is a function of voltage \( (v_d^+, v_q^+, v_d^-, v_q^-) \) and positive sequence current \( (i_d^+ \) and \( i_q^+ \)). The voltages can be represented with matrix \([A]\).

\[
(A) = \begin{pmatrix}
A_{11} & A_{12} \\
A_{21} & A_{22}
\end{pmatrix}
\] (4-11)

\[
\begin{pmatrix}
i_d^-(ref) \\
i_q^-(ref)
\end{pmatrix} = - \begin{pmatrix}
v_d^+ & v_q^+ \\
v_d^- & v_q^-
\end{pmatrix}^{-1} \begin{pmatrix}
v_d^- & v_q^- \\
v_d^+ & v_q^+
\end{pmatrix} \begin{pmatrix}
i_d^+ \\
i_q^+
\end{pmatrix}
\]

A simulation to reduce the active power ripples has been done. The \( P_3 \) ripples show improvement compared to the one without negative sequence control. The comparison can be
Figure 4-13: Positive, negative and zero sequence equivalent circuit diagram of Case 0 (Suppression) at terminal 2

Table 4-2: Active power ripple improvement with NSCC Case 1

<table>
<thead>
<tr>
<th>Case</th>
<th>Ripple [kV]</th>
<th>Improvement</th>
</tr>
</thead>
<tbody>
<tr>
<td>ΔP_{2-NONSC}</td>
<td>85.4</td>
<td>49.18 %</td>
</tr>
<tr>
<td>ΔP_{2-Case1}</td>
<td>42</td>
<td></td>
</tr>
</tbody>
</table>

examined in Figure 4-14. The active power ripples without NSCC appear around 85.4 kV, meanwhile, the power ripples with NSCC Case 1 are improved into an average of 42 kV. It shows a 49.18 % improvement of damping the active power ripples as given in Table 4-2.

A deeper observation can be seen into what happened in negative sequence current controller. The plot of the negative sequence current controller is showed in Figure 4-15. It shows that when fault applied, i_d^- and i_q^- are controlled into some degree of magnitude instead of zero.

This injection scheme of Case 1 uses more reactive power for the drawback, it also shows deeper active power drop during the fault. However, if active power ripple is the main problem which should be mitigated, Case 1 is able to show the solution.

Injection of Negative Sequence Current (Case 2 and 3)

In these cases, negative dq current references \((i_{d(ref)}^-, i_{q(ref)}^-)\) are set to have some value in proportion to the negative sequence voltage. The negative sequence voltage which is injected to the negative current direct and quadrature references are expressed in Equation 4-12 and 4-13.

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Figure 4-14: Active power ripple comparison of Case without NSCC (NO NSC) and NSCC Case 1

Figure 4-15: \(i_d^{-}\) and \(i_q^{-}\) of NSCC Case 1

\[
i_{d(\text{ref})}^{-} = k_{\text{neg}} \cdot V_{\text{neg}} = k \cdot \sqrt{(v_d^{-})^2 + (v_q^{-})^2}. \quad (4-12)
\]

\[
i_{q(\text{ref})}^{-} = 0. \quad (4-13)
\]

The Case 2 has the negative sequence voltage injected in negative sequence direct current reference axis \(i_{d(\text{ref})}^{-}\). The negative sequence quadrature current reference is set to zero. The different approach is done to the Case 3, which is treated conversely as expressed in Equation 4-14 and 4-15.

\[
i_{d(\text{ref})}^{-} = 0. \quad (4-14)
\]

\[
i_{q(\text{ref})}^{-} = k_{\text{neg}} \cdot V_{\text{neg}} = k \cdot \sqrt{(v_d^{-})^2 + (v_q^{-})^2}. \quad (4-15)
\]

The \(k_{\text{neg}}\) value is in proportion with the negative sequence voltage. \(V_{\text{neg}}\) is negative sequence voltage, which can be retrieved from square root of summation of notch-filtered \(v_d^{-}\) and \(v_q^{-}\), as written in the configuration Table 4-1. The value of \(k_{\text{neg}}\) is proportional to the injection level of the negative sequence current. A sensitivity of the different \(k_{\text{neg}}\) value has been done.
and delivered in Appendix A. The optimal results show $k_{\text{neg}} = 1$ for Case 2 and $k_{\text{neg}} = 2$ for Case 3 as written down in equation (4-16), (4-17).

\begin{align}
  k_{\text{neg-Case2}} &= 1. \\
  k_{\text{neg-Case3}} &= 2. 
\end{align}  

(4-16)  

(4-17)

This configuration yields the negative sequence direct and quadrature current as depicted in Figure 4-16. In Case 2, $i_d^-$ has a proportional value to negative sequence voltage, otherwise $i_q^-$ is zero. Conversely, in Case 3, $i_d^-$ is zero, however $i_q^-$ has a proportional value to the negative sequence voltage.

\[\text{CASE 2 and 3 - Negative Sequence Direct and Quadrature Current}\]

\[\text{CASE 2 and 3 - Positive Sequence Direct and Quadrature Current}\]

The positive sequence direct and quadrature current can be seen in Figure 4-17. $i_d^+$ and $i_q^+$ of Case 2 and 3 show similar behavior with slightly different magnitude and ripple behavior. The magnitude and ripple behavior affect the active and reactive power control of MMC HVDC.

\[\text{Figure 4-16: } i_d^- \text{ and } i_q^- \text{ of NSCC Case 2 and 3}\]

\[\text{Figure 4-17: } i_d^+ \text{ and } i_q^+ \text{ of NSCC Case 2 and 3}\]

The sequence diagram for the injection of the negative sequence current can be seen in Figure 4-18. The negative sequence components of MMC HVDC is boosted by a current source. This shows that the MMC HVDC injects the negative sequence current. The effect is shown in negative sequence currents which can be seen in Figure 4-23. For Case 1, 2, and 3, the negative sequence currents are significantly higher than the NO NSC Case.
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Figure 4-18: Sequence Diagram of NSCC injection scheme in terminal 2.

4-1-4 Comparison Between NSCC Cases

The comparison of NSCC scenarios as general is depicted in Figure 4-19. The figure shows Vdc, P and Q parameters behavior during SLG fault at terminal 2. Every parameter contains the case without NSCC and NSCC Cases of Case 0, 1, 2 and 3. Those results are illustrated in a single plot. The figure can distinguish the ripple and magnitude drops of the parameters. It shows which NSCC Cases are suitable to improve the asymmetrical fault effects.

Figure 4-19 shows every response of dq current signal of the positive and the negative sequence $i_+^d$, $i_+^q$, $i_-^d$ and $i_-^q$ in a separate manner. It shows clearly that suppression scheme of negative sequence (Case 0) suppresses the negative sequence current to zero, while injection of negative sequence (Case 1-3) injects $i_-^d$ and $i_-^q$ into having some non zero values higher than NO NSC’s negative sequence current.

Because it is difficult to see the plots piled up with each other in Figure 4-19, a small section of $t=3.15-3.25$ s is plotted in a sequence of time for every Vdc, P and Q. The figure shows instantaneous Vdc, P and Q value in order to compare the ripple and magnitudes.

During the asymmetrical fault, a $2\omega$ ripple appears in every Vdc, P and Q. Also, those parameters suffer from the change of magnitudes during asymmetrical faults, which already mentioned as drop. The main objectives are to find the smallest ripple and drop. In $V_{dc}$, Case 2 is able to suppress the ripple yet Case 3 yields to bigger ripple. With the same analysis, in P, Case 1 and 2 are good for minimizing P ripples but they show very high P drop. Case 3 is good in maintaining slightest P drop. Q is in the best condition of drop with Case 3, due to the improvement in both ripple and drop. A brief summary of the comparison is written in Table 4-3. Zero (0) is an indication of no improvement. The positive (+) sign indicates an improvement and the negative (−) sign indicates a bad drawback.

The graph of Vdc, P and Q ripple in effect of NSCC implementation are shown in Figure 4-21, while the graph of P and Q drops in effect of NSCC implementation are shown in Figure

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4-1 NSCC Strategies in the Point to Point MMC HVDC during Asymmetrical Fault

Comparison of Cases: No NSC, case0, case1, case2, case3

SLG fault at receiver terminal (T2)

Figure 4-19: Vdc, P and Q plots for every NSCC Cases

4-22. The Positive, negative and zero sequence components of terminal 2 during SLG fault are plotted in Figure 4-23 and Figure 4-24. NSCC cases are given in columns. The phase voltages, symmetrical voltages, phase currents and symmetrical currents are given in rows. The grid side measurement is shown in Figure 4-23. Grid side is located in the Y/grounded side of the transformer. The figure shows that during the SLG fault, one of the phase voltages returns to zero, while another two phase voltages are still operating with the, at least, same value, or it could be a decreasing value. This unbalanced voltage shows an increasing value of the negative sequence voltage. The zero sequence voltage appears in a fixed value. The negative sequence current appearance is proportional to positive sequence voltage drop. It can be seen that generally, NSCC scheme does not really affecting the symmetrical components of the voltage on the grid side. The Case 1 and 3 show slightly deeper voltage drop. This happens because both Cases inject $i_{q}^-$, which affects the reactive power of the MMC HVDC.

The Y/grounded configuration allows the flow of zero sequence currents. The zero sequence current appears in every NSCC scenario. It appears as a return vector between positive and negative sequence currents. The negative sequence current in Case 0 shows suppression into...
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The value of zero.

On the other side, in Case 1-3, the negative sequence currents are injected. Different $k_{neg}$ values lead to the different degree of negative sequence current injection. In Case 2, $k_{neg}$ value is 1, as given in Equation 4-12, 4-13 and 4-16. Meanwhile, in Case 3, the $k_{neg}$ value is 2, as given in Equation 4-14, 4-15 and 4-17. The negative sequence current shows a higher injection in Case 3 compared to Case 2. But, in Case 1, the negative sequence current injection is the highest because it is injected in both in the negative direct and quadrature axis $i_{-d}$ and $i_{-q}$.

The unbalanced three phase currents appear due to the appearance of the zero and negative sequence current components. Case 1 and 2 injects $i_{-d}$ to increase the negative sequence current. The negative sequence current in these cases are proportional to the severity of un-

Table 4-3: Comparison summary between Cases of NSCC. Positive (+) sign shows improvement, negative (−) sign shows bad effect. Zero (0) shows no improvement.

<table>
<thead>
<tr>
<th>Case</th>
<th>Description</th>
<th>Vdc Ripple</th>
<th>P Drop</th>
<th>P Ripple</th>
<th>Q Drop</th>
<th>Q Ripple</th>
</tr>
</thead>
<tbody>
<tr>
<td>Case 0</td>
<td>Suppression</td>
<td>0</td>
<td>0</td>
<td>+</td>
<td>-</td>
<td>0</td>
</tr>
<tr>
<td>Case 1</td>
<td>Damping of P Ripple</td>
<td>+</td>
<td>-</td>
<td>++</td>
<td>-</td>
<td>0</td>
</tr>
<tr>
<td>Case 2</td>
<td>Injection d axis</td>
<td>++</td>
<td>-</td>
<td>++</td>
<td>-</td>
<td>0</td>
</tr>
<tr>
<td>Case 3</td>
<td>Injection q axis</td>
<td>-</td>
<td>++</td>
<td>-</td>
<td>-</td>
<td>+</td>
</tr>
</tbody>
</table>
balanced three phase currents. It makes one of three phase currents to have a big magnitude. Meanwhile in Case 3 which injects $i_q^-$, the three phases currents show similar unbalance with the case without NSCC.

The converter side measurement is shown in Figure 4-23. The measurement is located in the reactor side of the MMC HVDC, which is a $\Delta$ side of the transformer. Generally, the symmetrical voltages show the positive sequence voltage drop which is proportional to the grid side measurement. In three phase voltages, the delta side of transformer allows the third harmonic injection to the voltages. The faulted voltage is not returned to zero because of the transfer characteristic of the transformer. Instead of returns to zero, the faulted voltage behaves as a triangular waveform.

Transformer with $\Delta$ winding configuration does not allow the zero sequence current to flow [26]. It shows in the figure that no zero sequence current is completely blocked. The NSCC suppression scheme (Case 0) returns the negative sequence to zero value, but without the sparking dynamic response of NF. NSCC injection schemes (Case 1-3) inject the negative sequence currents.

**Brief Summary**

The grid code requires the HVDC converter to be able to ride through and withstand the negative phase sequence which appears from unbalanced fault [4]. The NSCC strategies which consists of the suppression and injection of negative sequence currents are simulated.

The NSCC suppression strategy shows balanced three phase currents. This condition ensures the security in the power electronic components of MMC HVDC. A slight increase of
the positive sequence voltage is observed. The power electronic components suffer from overvoltages.

The NSCC injection strategy shows unbalanced three phase currents, and also the overcurrent phenomena. This ensures the protection system to detect the fault overcurrent. The injection strategy also shows results of the DC voltage, active and reactive power improvement in ripples and drops during the unbalanced fault. However, the injection of negative sequence current should be limited, in order to protect the power electronic components from overcurrent.

***
Figure 4-23: Instantaneous three phase voltage and current alongside with positive, negative and zero sequence voltage and current. Measurements are performed in grid (generator) side.
The Effect of Negative Sequence Current Control (NSCC) in the Point to Point MMC HVDC during the Asymmetrical Fault

Figure 4-24: Instantaneous three phase voltage and current alongside with positive, negative and zero sequence voltage and current. Measurements are performed in converter (reactor) side.
Chapter 5

3-Terminal MMC MTDC Controls and Asymmetrical Fault Analysis

5-1 Power Dispatch of 3-Terminals MMC MTDC

After the discussion on the point to point MMC HVDC in Chapter 3 and 4, an expansion is going to be applied to the HVDC network. In this chapter, a Multi Terminal HVDC (MTDC) application is simulated using efficient model of MMC HVDC [3] which comes from PSCAD [14]. A modification of the control system is implemented so that the MMC HVDC is capable of controlling the negative sequence components [24][22]. This MTDC consists of 3 terminal identical MMC HVDC, with the adaptable configuration of control in the different terminal. Many MMC MTDC systems have been studied in several listed publications [28][29][30].

The single converter model used in this chapter are identical with mentioned MMC which is used in Section 3-1. One terminal is configured as the Vdc control, and the other terminals are configured as the P control. The system diagram of 3-Terminal MTDC Test System is depicted in Figure 5-1. The third terminal is added as terminal 3 with identical topology from terminal 1 and 2. The DC side of Terminal 3 is connected with the redundant lines which come from terminal 1 and terminal 2 with the length of 400 km. Terminal 3 is connected to terminal 1 with the 200 km DC transmission lines and is connected to terminal 2 with 250 km transmission lines. The third terminal is configured as P control, thus, the system becomes Vdc-P-P control respectively for terminal 1, 2 and 3.

The terminal 3 is connected to 2 terminal system after the terminal 1-2 connection is established into the steady state condition at $t = 1.7s$. The power flow is configured to flow from terminal 1 as a sender terminal into terminal 2 and 3 as the receiver terminals. The active power flow is illustrated with arrows in Figure 5-1. This means terminal 1 is a bottleneck. To keep terminal 1 to work beyond its maximum active power capability, the summation of active power references between terminal 2 and terminal 3 should be lower than maximum active power capability of terminal 1.
### 5-1-1 Vdc-P-P Configuration

The Vdc control which is being used in this section is the one which is depicted in Figure 2-5. In a Vdc-P-P configuration of 3 terminal MTDC, the maximum power capability of terminal 1, 2 and 3 is 1000 MW. To maintain the normal operation without exceeding the maximum power capability, the terminal 2 active power reference is set to 400 MW at \( t = 3s \) and the active power reference of terminal 3 is set to 500 MW at \( t = 5s \). The references are set with a step function. This step change of active power references makes \( P_2 \) and \( P_3 \) change with a rising response time. The plots for this scenario is depicted in Figure 5-2.

At \( t = 3s \), \( P_2 \) reference in Terminal 2 is changed from 0 to -400 MW in the form of a step function. It should be noted that the plus and minus sign of \( P_2 \) and \( P_3 \) is because of the multimeter which is used in reversed polarity from flows of \( P_1 \). \( P_2 \) is increasing not instantaneously but with an increasing rate of \( dP/dt \). This condition happens because of the response of passive element of HVDC, such as the rated inductor, resistor, capacitors and also because of the \( P_{dc} \) outer control configuration of MMC HVDC which uses P rate limiter. After approximately 900ms, \( P_2 \) reaches its reference value. \( P_1 \) follows \( P_2 \) because terminal 1 is configured as Vdc control. However, terminal 3 is still in its initial power of 0, fixed with the reference value of \( P_3 \).

At \( t = 5s \), a step change of \( P_3 \) reference is applied. \( P_3 \) reference changed from 0 into -500 MW. \( P_1 \) the follows increasing value of \( P_3 \), and \( P_2 \) is still in its fixed value. It can be seen that \( P_1 \) is the summation of \( P_2 \) and \( P_3 \) during normal condition. \( P_1 \) should be lower than the maximal power rating of terminal 1 to avoid MTDC control error due exceeding the over-limit value.

The reactive power of Terminal 1, 2 and 3 are also changed while the P step function is applied to \( P_2 \) and \( P_3 \). This shows that the sources need a reactive power compensation in the
Figure 5-2: Vdc, P and Q responses for power step change in 3 terminal MMC MTDC. MTDC is configured as Vdc-P-P control

proportion of the active power transferred.

The responses of the DC voltages are also important to be discussed. Every changes in the reference power of $P_2$ and $P_3$, there are changing responses in DC voltages. It can be seen that $V_{dc1}$, $V_{dc2}$ and $V_{dc3}$ have a slight disturbance every changing P value. $V_{dc}$ changes from 640 KV into 620 KV every occurrence of step changes then it goes back to normal again after 1 second. This response could be improved by modifying Vdc control into Vdc droop control, which is going to be discussed in next subsection.

5-1-2 Vdc droop-P-P Configuration

A fast changing rate of active power may make the DC voltage to become unstable. In previous section, a slight disturbance is found due to the changing value of P. To mitigate the problem, Vdc droop control is implemented on the active power control in the outer control. The block diagram of Vdc droop control is depicted in Figure 5-3 [31].

The Vdc droop control is a simple addition of active power error in Vdc outer loop before the input of the PI controller. A constant of $k^{droopDC}$ is a multiplication factor of active power which has an effect of different slope in changing DC voltage. This $k^{droopDC}$ is basically a proportional controller. With this DC voltage droop controller, a DC voltage will result to a more stable value every changing of the P value.

A simulation has been done to demonstrate this Vdc droop control response. The MMC MTDC model which is used in the previous section is modified to Vdc droop-P-P control.
for Terminal 1, 2 and 3 respectively. Three values of $k_{droopDC}$ proportional controller are simulated for sensitivity. The results can be seen in Figure 5-4.

The plots in Figure 5-5 shows different responses for $k_{droopDC} = 10, 20$ and $30$. It shows that bigger $k_{droopDC}$ yields to smoother $V_{dc}$ response and less overshoot in $P_1$. This configuration is an enhancement of Vdc-P-P, however, it results in a better stabilization during active power change.
5-1 Power Dispatch of 3-Terminals MMC MTDC

5-1-3 Vdc droop-P-Vdc droop Configuration

A further approach has been studied by configuring the MTDC as Vdc droop-P-Vdc droop controller. A Vdc droop constants of 30 is used in terminal 1 and 3. The simulation results can be seen in Figure 5-4.

At t=3s, a step function is applied for $P_2$ reference from 0 to -400 MW. The reference value of $P_1$ is also configured from 0 to 400 MW. Due to Vdc droop control scheme, $P_3$ shows changing value at t=3 from 0 to -50 MW and then immediately reversed to approximately 50 MW. $P_3$ shows this behavior to compensate the Vdc response during active power step changes. Even though $P_1$ reference is set to 400 MW, $P_1$ only reaches approximately 350 MW due to the load is shared with $P_3$. $P_2$, which terminal 2 is a P control, reaches its reference value of -400 MW.

At t=5s, the reference of $P_3$ is set from 0 to -500 MW. As a P control, $P_2$ stays in its fixed value of -400 MW. $P_3$ changes from 50 MW into -350 MW trying to reach its reference value of -500 MW, but $P_3$ does not reach -500 MW due to the shared load with terminal 1, which is another Vdc droop control. From another point of view, at t=5s, $P_1$ reference is changed from 400 MW to 900 MW, which changes $P_1$ value from 350 MW into approximately 750 MW. The simulation result shows that with an MTDC, when more then one terminal configured as Vdc droop control, those terminal share power loads between each other. It is obvious that terminal 1 and 3 share the power loads between each other.

The configuration also shows advantageous effect, which is an enhanced stability of DC voltages. It is clearly showed in the simulation result in Figure 5-6 that $V_{dc1}$, $V_{dc2}$ and $V_{dc3}$ have very stable DC voltage even when step function is applied in each terminal.
5-2 Asymmetrical Fault in the 3-Terminals MMC MTDC

After a simple power dispatch operation has been discussed in the previous section, it is possible to study the NSCC effects in MTDC operation. The Single Line to Ground (SLG) fault is applied in terminal 2 at t=4s as depicted in Figure 5-7. To ensure the stable condition, the setpoints of P2 and P3 are changed into $P_2 = -300$ MW and $P_3 = -400$ MW, which makes $P_1 = 700$ MW. The fault is applied after the system reaches the steady state condition at t=4s.

5-2-1 SLG Fault in a Vdc-P-P MTDC without Activation of Negative Sequence Current Control (NSCC)

In this section, an SLG fault is applied at terminal 2 of the MTDC. All of the 3 terminals are configured without NSCC. This control scheme only has positive sequence controller in the inner current control loop. The simulation results can be seen in Figure 5-8.

It can be seen in the center column, $V_{dc2}$, $P_2$ and $Q_2$ are plotted. Terminal 2 is a faulted terminal so it shows changing magnitude and rippled behavior of $V_{dc2}$, $P_2$ and $Q_2$ when fault
5-2 Asymmetrical Fault in the 3-Terminals MMC MTDC

**Figure 5-7:** Asymmetrical fault test system for 3 terminal MMC MTDC in a Vdc-P-P configuration. SLG fault is applied at AC side of terminal 2

is applied. With the same discussion as delivered in Section 4-1-1, $P_1$ shows similar behavior as 2 terminal configurations. The similarity appears in only the dropping value of Vdc, P and Q. The terminal 1 suffers from magnitude drop but not with the ripple.

The third terminal also shows some response due to the fault. $V_{dc3}$ has a changing value which is similar with $V_{dc1}$. This happens because terminal 3 is connected with terminal 1 and terminal 2 in a redundant configuration. It means there are always a connection to another terminal. Terminal 1 is connected directly to 2 and 3, also terminal 2 is connected directly to 1 and 3. This makes the Vdc fault in terminal 2 shows mirrored behavior in $V_{dc1}$ and $V_{dc3}$.

A different power response is shown in terminal 3. Terminal 3 always has a fixed value of $P_3 = -400$ MW, even if SLG fault is applied at terminal 2, without any power drop or ripple. The power drop does not happened in $P_3$ because the fault is applied at terminal 2 as a receiver terminal. Terminal 3 is also a receiver terminal, moreover, terminal 3 and terminal 2 are separated by a 250km HVDC transmission lines. It is not the same as $P_1$ which suffers from power drop because terminal 1 is a sender terminal, configured as Vdc-control. The $P_3$ also withstand the effect of power drop and ripple because terminal 3 is a P-controlled terminal.

### 5-2-2 SLG Fault With NSCC to damp active power ripple (Case 1) in a Vdc-P-P MTDC configuration

The simplest way to see the effect of NSCC is to configure NSCC as an active power ripple damper [23][20][24]. This is the Case 1 of NSCC which has already discussed in Chapter 4. This scenario of NSCC could damp the active power ripple. If the active power ripple is damped, it means that the NSCC Case 1 is working properly.

The response of $P_2$ during fault without NSCC can be compared side by side with $P_2$ with activation of NSCC Case 1. The comparison can be seen in Figure 5-9. It is obvious that NSCC Case 1 is capable of minimizing the ripple in $P_2$. 

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Figure 5-8: Vdc, P and Q responses for SLG fault in 3 Terminal MMC MTDC. An SLG fault is applied at terminal 2 without NSCC capability

The complete simulation result of a 3 terminal MTDC grid which in Vdc-P-P control is configured with activation of NSCC Case 1 has been done. The simulation result is showed in Figure 5-10.

The second column consists of the plots of $V_{dc2}$, $P_2$ and $Q_2$. Compared to the results without NSCC, the $V_{dc}$ shows different effects in maintaining the oscillation. The oscillation which occurs after the SLG fault is cleared observed by the additional control response of PI controller in the negative SRF. This after clearance oscillation of $V_{dc2}$ is mirrored to $V_{dc1}$ and $V_{dc3}$, because DC side of terminal 1, 2 and 3 are all connected.

As discussed before, during the SLG fault, the oscillation of $P_2$ is damped compared to the NO NSC Case. After the SLG fault is cleared at $t=4.25s$, $P_2$ shows an after-clearance oscillation, that happened because of negative SRF of the inner current controller. This after-clearance oscillation is observed in $P_1$. $P_3$ does not show any difference due to terminal 3 is P-controlled terminal.

Terminal 2 shows a bigger reactive power consumption during the SLG fault compared to the one without NSCC scheme (NO NSC). It happens because of the negative sequence current is injected in NSCC Case 1.
Overall, the previous simulations conclude that the efficient model of MMC HVDC is capable to be used to simulate 3 terminal MTDC. Different control modification are also performed, one of them is a modification of Vdc droop control in the upper level control. The modified Vdc droop configuration shows enhanced stability in DC voltage during the change of active power. The NSCC is capable to be implemented in the efficient model of MMC MTDC. This is showed by NSCC Case 1. It shows the effect in the terminal which asymmetrical fault is suffered. One of the effects is the damping improvement of the active power ripples during a single line to ground fault. This shows the NSCC could be applied to damp the active power ripples in the MMC MTDC system.
Figure 5-10: Vdc, P and Q response for SLG fault in 3 terminal MMC MTDC. SLG fault is applied at terminal 2, with NSCC to damp active power ripple (Case 1)
Chapter 6

Point to Point MMC HVDC Connection with IEEE 9 Bus Test Systems

In order to understand the effect of MMC HVDC connection to the unbalanced faulted system behavior, one terminal of the point to point MMC HVDC is connected to the AC grid system. The model of Western System Coordinating Council (WSCC)/IEEE 9 bus system is used for this test [32]. This model consists of 9 buses, 3 generators and 3 loads in different buses. The system diagram of WSCC 9 bus system is depicted in Figure 6-1. The figure contains some notation and several measurement points. For the time being, it should be considered that the simulation is executed without SLG fault.

![Figure 6-1: IEEE/WSCC 9 bus test system](image)

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### Table 6-1: Normal operating point of WSCC 9 bus system

<table>
<thead>
<tr>
<th>Bus</th>
<th>Rated KV</th>
<th>Type</th>
<th>Measured</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
<td>P (MW)</td>
</tr>
<tr>
<td>1</td>
<td>16.5</td>
<td>Generator</td>
<td>70</td>
</tr>
<tr>
<td>2</td>
<td>18</td>
<td>Generator</td>
<td>167</td>
</tr>
<tr>
<td>3</td>
<td>13.8</td>
<td>Generator</td>
<td>82.5</td>
</tr>
<tr>
<td>4</td>
<td>230</td>
<td>Busbar</td>
<td>-</td>
</tr>
<tr>
<td>5</td>
<td>230</td>
<td>Load</td>
<td>125</td>
</tr>
<tr>
<td>6</td>
<td>230</td>
<td>Load</td>
<td>90</td>
</tr>
<tr>
<td>7</td>
<td>230</td>
<td>Busbar</td>
<td>-</td>
</tr>
<tr>
<td>8</td>
<td>230</td>
<td>Load</td>
<td>100</td>
</tr>
<tr>
<td>9</td>
<td>230</td>
<td>Busbar</td>
<td>-</td>
</tr>
</tbody>
</table>

Three different generators connected in three different buses namely bus 1, 2 and 3. The generators also work in different operating points and different rated voltage of 16.5 kV, 18 kV and 13.8 kV respectively. These generators are loaded by three loads in bus 5, 6 and 8 at 230 kV voltages. The generators are connected to the step up Y/grounded - Y/grounded transformer to reach 230 kV voltage level. Using PSCAD/EMTDC[14], the generators are modeled as the equivalent voltage sources. The simulation result of WSCC 9 bus can be seen in Table 6-1. The table contains rated and measured normal operating points at steady state condition.

### 6-1 Connection of WSCC 9 Bus System to the Point to Point MMC HVDC

After the discussion of the WSCC 9 bus system in the normal operation, a connection to the point to point MMC HVDC is established. One side of 2 terminal MMC HVDC is connected to bus 7 of WSCC 9 bus system at voltage level of 230 kV. The active power (P) reference and AC voltage (Vac) reference of MMC HVDC is configured as similar as possible to follow the normal operating point as showed in Table 6-1. The system diagram of this test system is depicted in Figure 6-2. Several measurement points are added into the generators G1, G2 and G3, several transmission line T54, T65, T78, load L8.

Due to the point to point MMC HVDC connection to the WSCC 9 bus system, a new normal operating point is reached. The equivalent voltage sources G1, G2, G3 share the load with new connected voltage source of terminal 2 MMC HVDC.

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6-2 Asymmetrical Fault at WSCC 9 Bus System and the Effect of Negative Sequence Current Control (NSCC)

A Single Line to Ground (SLG) fault is applied at the transmission line in the vicinity of bus 8 in WSCC 9 bus system, as depicted in Figure 6-1 before. The fault is applied at $t=3s$ for a duration of 250ms. When the fault is applied, the dynamic behavior of the voltage changes. The active power of G1, G2 and G3 slightly increase into their maximal active power. T2 as a P controlled MMC HVDC shows slightly decreases $P_2$ but it has a strong control to keep $P_2$ around 700MW. The illustration is given in Figure 6-3

Due to the SLG fault, every node in the WSCC 9 bus system and terminal 2 of MMC HVDC suffers from voltage dip. The voltage dip magnitudes are different between each node. It depends on the distances from the source of the disturbance. The voltage dip plot of every measured when SLG fault occurs is given in Figure 6-4. The figure shows the effect of SLG fault for the time duration of 250ms, after that, the fault is cleared and the system immediately goes to the normal stable condition.
2.8 2.9 3 3.1 3.2 3.3 3.4 3.5
100
200
300
400
500
600
700
800P [MW]
Generator and HVDC P Response
T2
G1
G2
G3

Figure 6-3: Active power responses of G1, G2, G3 and T2

Table 6-2: NSCC strategies of Chapter 6

<table>
<thead>
<tr>
<th>Scenario Name</th>
<th>NSC type</th>
<th>idref-</th>
<th>iqref-</th>
<th>fault</th>
</tr>
</thead>
<tbody>
<tr>
<td>Normal</td>
<td>n/a</td>
<td>n/a</td>
<td>n/a</td>
<td>No fault</td>
</tr>
<tr>
<td>No NSC</td>
<td>n/a</td>
<td>n/a</td>
<td>n/a</td>
<td>SLG</td>
</tr>
<tr>
<td>Case 0</td>
<td>suppression</td>
<td>0</td>
<td>0</td>
<td>SLG</td>
</tr>
<tr>
<td>Case 3</td>
<td>injection</td>
<td>0</td>
<td>k * V-</td>
<td>SLG</td>
</tr>
</tbody>
</table>

6-3 The Effect of NSCC Strategies in the MMC HVDC Connected to WSCC 9 Bus System

In this part, the normal condition with and without a fault is simulated. Then, two kinds of NSCC scenario are compared. The first NSCC is the suppression of negative sequence current, which is known as Case 0. Another one is the injection scenario with injection in quadrature axis, which is known as Case 3. These cases have been discussed earlier in Chapter 4. The complete simulation scenarios are given in Table 6-2.

The positive sequence voltages in different buses are measured to compare the voltage responses before fault and after the fault with three scenarios: NONSC, Case 0 and Case 3. When the SLG fault is applied, all of the buses and generators are affected with a voltage drop, but with different drop levels. These positive sequence voltages resemble the voltage drop at different nodes. And also, the severity of fault can be examined. The deeper the drop is, the more severe the fault which means it is nearer to where the fault is applied.

A further response can be examined from Figure 6-5. It is a collection of instantaneous
voltages from HVDC terminal 2 and generator buses measured at $t = 3.075$ s. The blue column chart (Normal) is a normal condition which does not suffer from the SLG fault. Another colored chart is No NSC, Case 0 and Case 3 which suffers from SLG fault. It can be seen that G1 and G2 suffer from the voltage drop the least. This happens because of the parameter of the transmission line, and also the HVDC control strategy. Moreover, G1 and G2 are separated from the faulted bus with transformers. The leakage reactance of transformers should decrease the fault’s severity.

Figure 6-6 shows the positive sequence voltage at different transmission lines and load buses. It can be seen for the fault in bus 8, L8 suffers from a biggest voltage drop. Compared with NONSC, NSCC Case 0 is not giving any major effects related to positive sequence voltage. They show relatively same value with NONSC. However, NSCC injection shows a significant effect in voltage dip improvement. With the injection of NSCC Case 3, voltage drop went deeper in every node. Also, this effect of NSCC agrees in every node. This shows that NSCC effect is not only applied in the AC terminal of HVDC, but also in the vicinity of the nearby AC system.

Another way to observe the severity of the fault is to examine the negative sequence current which appears when SLG fault occurs. The negative sequences currents in different buses are depicted in Figure 6-7. It can be seen that in the normal condition, the negative sequence current shows zero value. This happens because the three phase currents are in stable condition.

A massive amount of negative sequence can be seen at T78. This happened because when the fault happened the positive sequence current also very big, due to T78 is a line which connects the fault and T2 MMC HVDC. T2 HVDC controls P that flows the current into the faulted location.

The effect of NSCC suppression can be seen in the figure. The negative sequence current
6-3-1 Brief Summary

The Negative Sequence Current Control (NSCC)-implemented MMC HVDC shows its effect not only in the Point of Common Coupling (PCC). It also shows some effects in the vicinity of the PCC. The effect depends on the impedance from where the fault is located and the MMC HVDC itself.

The AC systems in the vicinity of the fault suffers from the SLG. However, NSCC is able to manage the effects of negative sequence currents and voltage appearance.

Case 0 of NSCC suppresses negative sequence current and slightly suppress the negative sequence voltage compared to the case without NSCC (NO NSC), while case 3 of NSCC injects the negative sequence current. Other references can be studied to observe the interaction of MMC HVDC with AC System [15].

Figure 6-5: Positive sequence voltage components on HVDC terminal and generator buses with different NSCC cases at t=3.075s

differences between NONSC and Case 0 can be seen in T2, G1, G2, G3, T54, T64, T98 and L8. It has a lower value in Case 0, reaching nearly zero value.

The injection of negative sequence Case 3 shows obvious increasing negative sequence current value. This also concludes that NSCC has taken every effect in every single node of WSCC 9 bus system.
Figure 6-6: Positive sequence voltage responses on transmission line and load buses with different NSCC cases measured at t=3.075s

<table>
<thead>
<tr>
<th></th>
<th>Normal</th>
<th>No NSC</th>
<th>Case 0</th>
<th>Case 3</th>
</tr>
</thead>
<tbody>
<tr>
<td>T2</td>
<td>0.0007</td>
<td>0.2728</td>
<td>0.2526</td>
<td>0.3997</td>
</tr>
<tr>
<td>T4</td>
<td>0.0006</td>
<td>0.2272</td>
<td>0.2108</td>
<td>0.3269</td>
</tr>
<tr>
<td>T5</td>
<td>0.0006</td>
<td>0.2315</td>
<td>0.2181</td>
<td>0.2946</td>
</tr>
<tr>
<td>T6</td>
<td>0.0008</td>
<td>0.2047</td>
<td>0.1907</td>
<td>0.2828</td>
</tr>
<tr>
<td>T8</td>
<td>0.0007</td>
<td>0.2727</td>
<td>0.2530</td>
<td>0.3924</td>
</tr>
</tbody>
</table>

Figure 6-7: Negative sequence current responses at different buses and NSCC scenarios measured at t=3.075s. SLG fault is applied at bus 8

<table>
<thead>
<tr>
<th></th>
<th>Normal</th>
<th>No NSC</th>
<th>Case 0</th>
<th>Case 3</th>
</tr>
</thead>
<tbody>
<tr>
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<td>0.0007</td>
<td>0.1834</td>
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<td>1.9949</td>
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<tr>
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<td>0.0005</td>
<td>0.1489</td>
<td>0.1392</td>
<td>0.2229</td>
</tr>
<tr>
<td>T5</td>
<td>0.0004</td>
<td>0.1474</td>
<td>0.1390</td>
<td>0.2241</td>
</tr>
<tr>
<td>T6</td>
<td>0.0002</td>
<td>0.0736</td>
<td>0.0650</td>
<td>0.2441</td>
</tr>
<tr>
<td>T8</td>
<td>0.0003</td>
<td>0.0658</td>
<td>0.0650</td>
<td>0.2441</td>
</tr>
</tbody>
</table>

Master of Science Thesis 
Hariadi Aji
Conclusions and Recommendations

7-1 General Conclusions

This MSc thesis evaluates different Negative Sequence Current Control (NSCC) schemes using the efficient Electro Magnetic Transient (EMT) type model of the MMC HVDC transmission system. A modification of the basic positive sequence MMC HVDC control systems into the positive and the negative sequence controllers with a Double Synchronous Reference Frame (DSRF) has been implemented in this work.

Different NSCC strategies were tested under Single Line to Ground (SLG) faults. The evaluated NSCC strategies consist of the suppression and injection of the negative sequence current as discussed in Chapter 4. The simulation results have been analyzed and on the basis of the results several conclusions have been drawn:

1. During SLG faults at the converter terminals, the NSCC suppression strategy eliminates the negative sequence current resulting in a balanced three phase current. This is due to the presence of only positive sequence currents which exists in the delta side of converter. In this way the power electronic components of MMC HVDC are secured from asymmetrical fault currents. However, MMC HVDC suffers from over-voltages and active power ripples due to the negative sequence voltage which exists.

2. The NSCC injection strategies could be applied either to damp the power ripples or to provide enhancement of the protection schemes operation in the AC grid. Based on the presented result for the MMC-HVDC, it is shown that the minimization of the active power ripple has been achieved. Perfect power ripple elimination cannot be achieved with the present double synchronous reference scheme due to the circulating currents within the arms of MMC HVDC. The application of NSCC injection also prevents high over-voltage phenomena during asymmetrical faults. This is due to the reduction of the negative sequence voltage.

3. The efficient MMC HVDC model is demonstrated in the MTDC connection in Chapter 5. The injection of NSCC to eliminate active power ripples is performed in the faulted
terminal. It has been shown that the power ripples have been improved compared to cases without NSCC strategies. However, the active power ripples not completely eliminated because of the appearance of circulating current which demands further research of Circulating Current Suppression Controller (CCSC).

4. In the case of point to point MMC HVDC connections with an expanded 9 bus AC system, as discussed in Chapter 6, it has been shown that the NSCC affects the asymmetrical response of the AC system near the converter, thus, the effects of NSCC could be perceived in expanded AC system. Overall, the suppression strategy of the NSCC reduces the negative sequence currents in the transmission system during an SLG fault, so it will affect and protect the generators from a high negative sequence current. Conversely, the injection strategy of NSCC increases the negative sequence current and reduces the positive sequence voltage, which could create some issues in the stability of the AC system.

7-2 Recommendations for Further Research

Other studies that could be suggested for further works are:

1. Other Circulating Current Suppression Controller (CCSC) strategies which separately control the upper and lower legs of MMC HVDC could be implemented in order to improve the stability of MMC HVDC during asymmetrical faults[19],[18].

2. The use of notch filters to eliminate double base frequency ($2\omega$) oscillation during an asymmetrical fault has drawbacks in the form of a dynamic response errors in every fault and switching action. In order to improve the mentioned dynamic response, an enhanced control system with Proportional-Integral-Resonant (PIR) controller [24],[25] could be developed with the modification of the MMC HVDC model used in this thesis.

3. Other control strategies to eliminate the active, reactive AC power ripples and also the DC voltage ripples during asymmetrical faults could be implemented using a zero sequence controller[20]. This zero sequence controller should be used in a cascading configuration alongside DSRF. The zero sequence controller is capable of eliminating zero sequence components on the Y-grounded side of the transformer during asymmetrical faults [20].

4. Different types of asymmetrical faults beside the SLG fault could be studied to obtain a deeper knowledge about asymmetrical fault behavior under the NSCC scheme[23][1].

***

Haridhi Aji

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Appendix A

Appendix: Point to Point MMC HVDC

System parameters used in this thesis are shown in Table A-1.

A-1 Another Parameter Used in this Appendix

This section shows the simulation using another parameter with less tuning accuracy compared to the one in Chapter 4. The usage of different NF and different sequence diagram parameter shows some differences. Moreover, in the Appendix, NSCC scenarios used is slightly different from Chapter 4. The difference is located at CASE 3 and 4. Chapter 4 does not have CASE 4. CASE 4 in the Appendix is actually CASE 3 in Chapter 4. The table for NSCC scenarios used in this appendix is shown in Table A-3.

In this appendix, 5 CASES simulated as shown in Table A-3

***
### Table A-1: System parameters used in Chapter 4

<table>
<thead>
<tr>
<th>No</th>
<th>Item</th>
<th>Terminal 1</th>
<th>Terminal 2</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>Rated MVA</td>
<td>1000 MVA</td>
<td></td>
</tr>
<tr>
<td>2</td>
<td>Type of HVDC</td>
<td>MMC HVDC 115 levels</td>
<td></td>
</tr>
<tr>
<td>3</td>
<td>Frequency</td>
<td>60 Hz</td>
<td></td>
</tr>
<tr>
<td>4</td>
<td>Voltage level</td>
<td>AE 640 KV DC, 370 KV AC</td>
<td></td>
</tr>
<tr>
<td>5</td>
<td>Direct Control</td>
<td>Vdc control 640 KV 1pu</td>
<td>P control 800 MW 1pu</td>
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<tr>
<td>6</td>
<td>Quadrature Control</td>
<td></td>
<td></td>
</tr>
<tr>
<td>7</td>
<td>Arm Inductances</td>
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<td></td>
</tr>
<tr>
<td>8</td>
<td>Cell DC Capacitor</td>
<td>2800 uF</td>
<td></td>
</tr>
<tr>
<td>9</td>
<td>Interfacing transformer</td>
<td></td>
<td></td>
</tr>
<tr>
<td>10</td>
<td>Transformers Leakage Reactance</td>
<td></td>
<td></td>
</tr>
<tr>
<td>11</td>
<td>Load inductances</td>
<td>40 mH</td>
<td></td>
</tr>
<tr>
<td>12</td>
<td>X/R</td>
<td>20</td>
<td></td>
</tr>
<tr>
<td>13</td>
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<td></td>
</tr>
<tr>
<td>14</td>
<td>Tid,q(pos,neg)</td>
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<td></td>
</tr>
<tr>
<td>15</td>
<td>KpAC</td>
<td>1</td>
<td></td>
</tr>
<tr>
<td>16</td>
<td>TiAC</td>
<td>0.1</td>
<td></td>
</tr>
<tr>
<td>17</td>
<td>TiDC</td>
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<td></td>
</tr>
<tr>
<td>18</td>
<td>NF</td>
<td>Orde 2 Transfer Function, 120Hz, Gain 1</td>
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### Table A-2: System parameter for simulation used in Appendix A

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<th>Item</th>
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<tbody>
<tr>
<td>1</td>
<td>Rated MVA</td>
<td>1000 MVA</td>
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</tr>
<tr>
<td>2</td>
<td>Type of HVDC</td>
<td>MMC HVDC 76 levels</td>
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<td>3</td>
<td>Frequency</td>
<td>60 Hz</td>
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<td>4</td>
<td>Voltage level</td>
<td>AE 640 KV DC, 370 KV AC</td>
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<td>5</td>
<td>Direct Control</td>
<td>Vdc control 640 KV 1pu</td>
<td>P control 800 MW 1pu</td>
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<td>Quadrature Control</td>
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<td>7</td>
<td>Arm Inductances</td>
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<td>Cell DC Capacitor</td>
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<td>9</td>
<td>Interfacing transformer</td>
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<td>10</td>
<td>Transformers Leakage Reactance</td>
<td>0.2 pu</td>
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<td>Load inductances</td>
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<td>12</td>
<td>X/R</td>
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<td>Kpd,q(pos,neg)</td>
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<td>14</td>
<td>Tid,q(pos,neg)</td>
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<td></td>
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<tr>
<td>15</td>
<td>KpAC</td>
<td>1</td>
<td></td>
</tr>
<tr>
<td>16</td>
<td>TiAC</td>
<td>0.1</td>
<td></td>
</tr>
<tr>
<td>17</td>
<td>TiDC</td>
<td>0.08</td>
<td></td>
</tr>
<tr>
<td>18</td>
<td>NF</td>
<td>Chebyshev, Q=10, f=120Hz</td>
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Table A-3: NSCC cases which are used in Appendix A

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<td>n/a</td>
<td>n/a</td>
<td>n/a</td>
</tr>
<tr>
<td>Case 0</td>
<td>suppression</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>Case 1</td>
<td>injection</td>
<td>2\omega damping equation of PQ</td>
<td></td>
</tr>
<tr>
<td>Case 2</td>
<td>injection</td>
<td>k * V_d-</td>
<td>0</td>
</tr>
<tr>
<td>Case 3</td>
<td>injection</td>
<td>k * V_d-</td>
<td>k * V_q-</td>
</tr>
<tr>
<td>Case 4</td>
<td>injection</td>
<td>0</td>
<td>k * V_d-</td>
</tr>
</tbody>
</table>

Figure A-1: Plots of 2 Terminal Vdc, P and Q. SLG fault is applied at terminal 2 (sender terminal) without NSCC (NO NSC). Terminal 2 suffers from 2\omega oscillation due to the fault location. Terminal 1 only suffers from voltage and power drops without the oscillation.
Figure A-2: Plots of 2 terminal Vdc, P and Q. SLG Fault is applied at terminal 2 (receiver terminal). NSCC CASE 0 (Suppression) is used.
Figure A-3: This figure shows positive and negative sequence direct and quadrature voltage and current in unfiltered manner. These are unfiltered control signal, before notch filter is added in every signal. Negative sequence shows $2\omega$ oscillation all over the simulation.
Figure A-4: This figure shows SLG fault is applied at terminal 2 which acts as a receiver terminal. Sensitivity of different constant $k$ are tested on NSCC CASE 1. When $k_q$ is set to zero, terminal 2 suffers from more P drop. Positive and negative sequence voltage and current shows ripple during the fault because of the usage of $f=50$Hz (it should be 60Hz) in the sequential extractor block of PSCAD. This problem is fixed in the main body of the thesis.
Figure A-5: This Figure shows SLG fault is applied at terminal 2 which acts as a receiver terminal. Sensitivity of kd = 1, 2 are tested on NSCC CASE 2. kd=1 shows the most optimal configuration. With the same ripple of Vdc and P with k=1, it shows smaller P and Q drops. Positive and negative sequence voltage and current shows ripple during the fault because of the usage of f=50Hz (it should be 60HZ) in the sequential extractor block of PSCAD. This problem is fixed in the main body of the thesis.
Figure A-6: This Figure shows SLG fault at terminal 2 acts as a receiver terminal. Sensitivity of \( k_q = 1, 2 \) and 5 are tested on NSCC CASE 3. \( k_d,k_q=1 \) shows the most optimal configuration. With the same ripple of \( V_{dc} \) and \( P \) with \( k=2 \), it shows smaller \( P \) and \( Q \) drops. Constant \( k = 5 \) is not considered because it leads to unstability. Positive and negative sequence voltage and current shows ripple during the fault because of the usage of \( f=50\text{Hz} \) (it should be 60HZ) in the sequential extractor block of PSCAD. This problem is fixed in the main body of the thesis.
Figure A-7: This figure shows SLG fault is applied at terminal 2 which acts as a receiver terminal. Sensitivity of $k_q = 1$ and $2$ are tested on NSCC CASE 4. Constant $k_q=2$ shows the most optimal configuration. With the same ripple of $V_{dc}$ and $P$ with $k = 1$, it shows smaller $P$ drop. Positive and negative sequence voltage and current shows ripple during the fault because of the usage of $f=50$Hz (it should be 60HZ) in the sequential extractor block of PSCAD. This problem is fixed in the main body of the thesis.
Figure A-8: This figure shows SLG fault is applied at terminal 2 which acts as a sender terminal. Sensitivity of constant $k = 1$ and 2 are tested on NSCC CASE 2. Constant $k=1$ shows the most optimal configuration. With the same ripple of Vdc and $P$ with $k = 2$, it shows smaller Q drop. Positive and negative sequence voltage and current shows ripple during the fault because of the usage of $f=50$Hz (it should be 60HZ) in the sequential extractor block of PSCAD. This problem is fixed in the main body of the thesis.
Figure A-9: This Figure shows SLG fault is applied at terminal 2 which acts as a sender terminal. Sensitivity of $k=1,2,\text{ and }5$ are tested on NSCC Case 3. Constant $k=1$ shows the most optimal configuration. With the same ripple of $V_{dc}$ and $P$ with $k=2$, it shows smaller $Q$ drop. However, $k=5$ shows more $P$ drop compared to another $k$, so it does not qualify. Positive and negative voltage and current sequence shows ripple during the fault because of the usage of $f=50\text{Hz}$ (it should be $60\text{Hz}$) in the sequential extractor block of PSCAD. This problem is fixed in the main body of the thesis.
Figure A-10: $V_{dc}$, $P$, $Q$, $V^+$, $I^+$, $V^-$ and $I^-$ comparison among the case without NSCC, NSCC Case 0, 1, 2, 3 and 4. $k$ CASE 2 = 1, $k$ CASE 3 = 1, $k$ CASE 4 = 2.
Figure A-11: $V_{dc}$, $P$ and $Q$ plots with enhanced details which delivered separately in time manner. This figure shows the ripples and drops in each parameter.
Appendix B

Appendix: 3 Terminal MTDC

Figure B-1: Comparison of different Vdc droop constant in 3 terminal MMC MTDC

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Figure B-2: System diagram for MMC MTDC Double Line to Ground (DLG) fault in terminal 1. Simulation result is showed in Figure B-3.

Figure B-3: Vdc, P and Q plots during DLG fault at terminal 1 without activated NSCC. System diagram is showed in Figure B-2.
Figure B-4: System diagram for MMC MTDC DLG fault at terminal 2. Simulation result is in Figure B-3.

Figure B-5: Vdc, P and Q plots during DLG fault at terminal 2 without activated NSCC. System diagram is showed in Figure B-4.
Appendix C

Appendix: WSCC Bus Interconnection

The complete plots of Positive, negative and zero sequence of Chapter 6 is given in this chapter at Figure C-1 - C-6. Another figures are simulation from different configuration.

### POSITIVE SEQUENCE VOLTAGE COMPONENTS OF SLG FAULT AT DIFFERENT BUSES

![Positive sequence voltage plot](image)

**Figure C-1:** Positive sequence voltage of every point in WSCC 9 bus interconnection

### C-1 Bus 8 of WSCC 9 bus System Connected into Terminal 2

In this appendix, a different configuration as depicted in Figure C-7 is simulated. Terminal 2 is connected to Bus 8 WSCC 9 Bus System. Moreover, the MMC HVDC system configuration used is as listed in Table A-2 and NSCC scenarios used is given in Table C-1.

***
Figure C-2: Positive sequence current of every point in WSCC 9 bus interconnection

Table C-1: NSCC cases which are used in Appendix C

<table>
<thead>
<tr>
<th>Scenario Name</th>
<th>NSC type</th>
<th>idnegref-</th>
<th>iqnegref-</th>
</tr>
</thead>
<tbody>
<tr>
<td>No NSC</td>
<td>n/a</td>
<td>n/a</td>
<td>n/a</td>
</tr>
<tr>
<td>Case 0</td>
<td>suppression</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>Case 1</td>
<td>injection</td>
<td>2w damping equation of PQ</td>
<td></td>
</tr>
<tr>
<td>Case 2</td>
<td>injection</td>
<td>k * V-</td>
<td>0</td>
</tr>
<tr>
<td>Case 3</td>
<td>injection</td>
<td>k * Vd-</td>
<td>k * Vq-</td>
</tr>
<tr>
<td>Case 4</td>
<td>injection</td>
<td>0</td>
<td>k * V-</td>
</tr>
</tbody>
</table>

Figure C-3: Negative sequence voltage of every point in WSCC 9 bus interconnection
**Figure C-4:** Negative sequence current of every point in WSCC 9 bus interconnection

**Figure C-5:** Zero sequence voltage of every point in WSCC 9 bus interconnection
Figure C-6: Zero sequence current of every point in WSCC 9 bus interconnection

Figure C-7: System diagram of MMC HVDC interconnection with WSCC 9 bus to bus 8
Figure C-8: Active power flow operating point before and after the connection

Figure C-9: Reactive power flow operating point before and after the connection
Figure C-10: Positive sequence voltage in buses and terminals with different NSCC cases

Figure C-11: Positive sequence current in buses and terminals with different NSCC cases
Figure C-12: Negative sequence voltage in buses and terminals with different NSCC cases

Figure C-13: Negative sequence current in buses and terminals with different NSCC cases
Figure C-14: Zero sequence voltage in buses and terminals with different NSCC cases

Figure C-15: Zero sequence current in buses and terminals with different NSCC cases
Appendix D

Fortescue’s Theorem of Positive, Negative and Zero Sequence Component

This appendix gives some required basic theory on positive, negative and zero sequence component theory.

The most powerful tools for dealing with unbalanced three phase circuit is the method of symmetrical components introduced by C.L. Fortescue [33],[26]. Fortescue’s theorem is a relation between three phase circuit and symmetrical components. It consist of positive, negative and zero component, as expressed in (D-1).

\[
\begin{bmatrix}
V_a \\
V_b \\
V_c
\end{bmatrix}
= 
\begin{bmatrix}
V_a^{(0)} + V_a^{(1)} + V_a^{(2)} \\
V_b^{(0)} + V_b^{(1)} + V_b^{(2)} \\
V_c^{(0)} + V_c^{(1)} + V_c^{(2)}
\end{bmatrix}
\]  
(D-1)

$V_a^{(0)}$, $V_a^{(1)}$ and $V_a^{(2)}$ are zero, positive and negative components, respectively of phase voltage $a$. The relation also agree with voltage phase $b$ and $c$. From the basic theory, three phase voltages could be retrieved from symmetrical component with the operation of matrix $[A]$ (D-2). Matrix $[A]$ contains phasor operation of $a$, which rotates 120 degrees of rotation. Meanwhile, $a^2$ rotates the phasor as much as 240 degrees (D-3).

\[
\begin{bmatrix}
V_a \\
V_b \\
V_c
\end{bmatrix}
= 
\begin{bmatrix}
1 & 1 & 1 \\
1 & a^2 & a \\
1 & a & a^2
\end{bmatrix}
\begin{bmatrix}
V_a^{(0)} \\
V_a^{(1)} \\
V_a^{(2)}
\end{bmatrix}
= 
\left[ A \right]
\begin{bmatrix}
V_a^{(0)} \\
V_a^{(1)} \\
V_a^{(2)}
\end{bmatrix}
\]  
(D-2)

\[
a \equiv 1 \angle 120^\circ \\
a^2 \equiv 1 \angle 240^\circ
\]  
(D-3)

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Thus, the symmetrical components can be retrieved from inverse operation of matrix \([A]\) (D-4)

\[
\begin{bmatrix}
V_a^{(0)} \\
V_a^{(1)} \\
V_a^{(2)}
\end{bmatrix} = [A]^{-1} \begin{bmatrix} V_a \\ V_b \\ V_c \end{bmatrix} = \frac{1}{3} \begin{bmatrix} 1 & 1 & 1 \\ 1 & a & a^2 \\ 1 & a^2 & a \end{bmatrix} \begin{bmatrix} V_a \\ V_b \\ V_c \end{bmatrix}
\] (D-4)

Balanced three phase system only consists of positive sequence without appearance of negative and zero sequence.

Positive sequence components rotates with the same angle of 3 phase component. Negative sequence components have the opposite rotation from positive sequence. Zero sequence is a returning vector which connect positive and negative sequence as a vector in a system which has available grounding system.


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